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(54) ULTRASOUND BEAMFORMER WITH SCALABLE RECEIVER BOARDS

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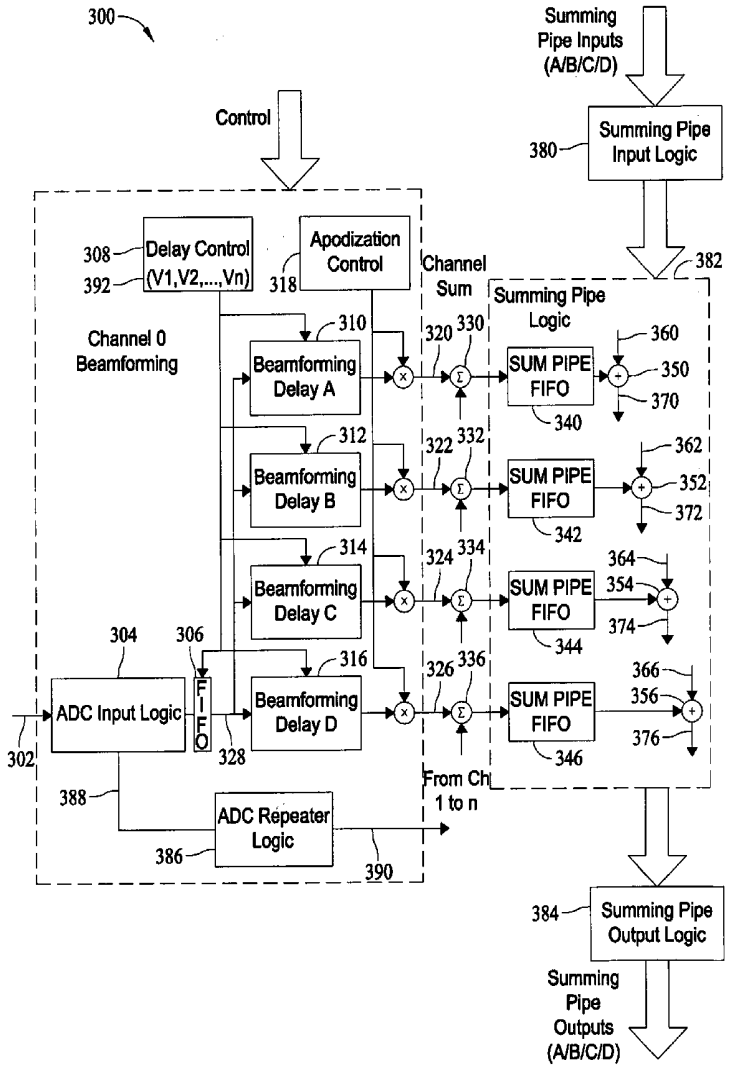
(57) **ABSTRACT**

A beamformer for an ultrasound system and a method for developing a beamformer are provided. The beamformer includes an RF interface configured to be connected to receiver boards that are connected to a probe. The method includes providing receiver boards, wherein each of the receiver boards is capable of conveying a common number of channels per board and has substantially similar circuit components and layouts. The method also includes selecting a number of channels per probe to be conveyed in parallel between a probe and the receiver boards, wherein the channels per probe is an integer multiple of the channels per board. The method further includes determining a combination of the receiver boards to use in the beamformer based on the number of channels per probe, wherein the receiver boards are capable of being used in at least first and second different combinations that support first and second different numbers of channels per probe.



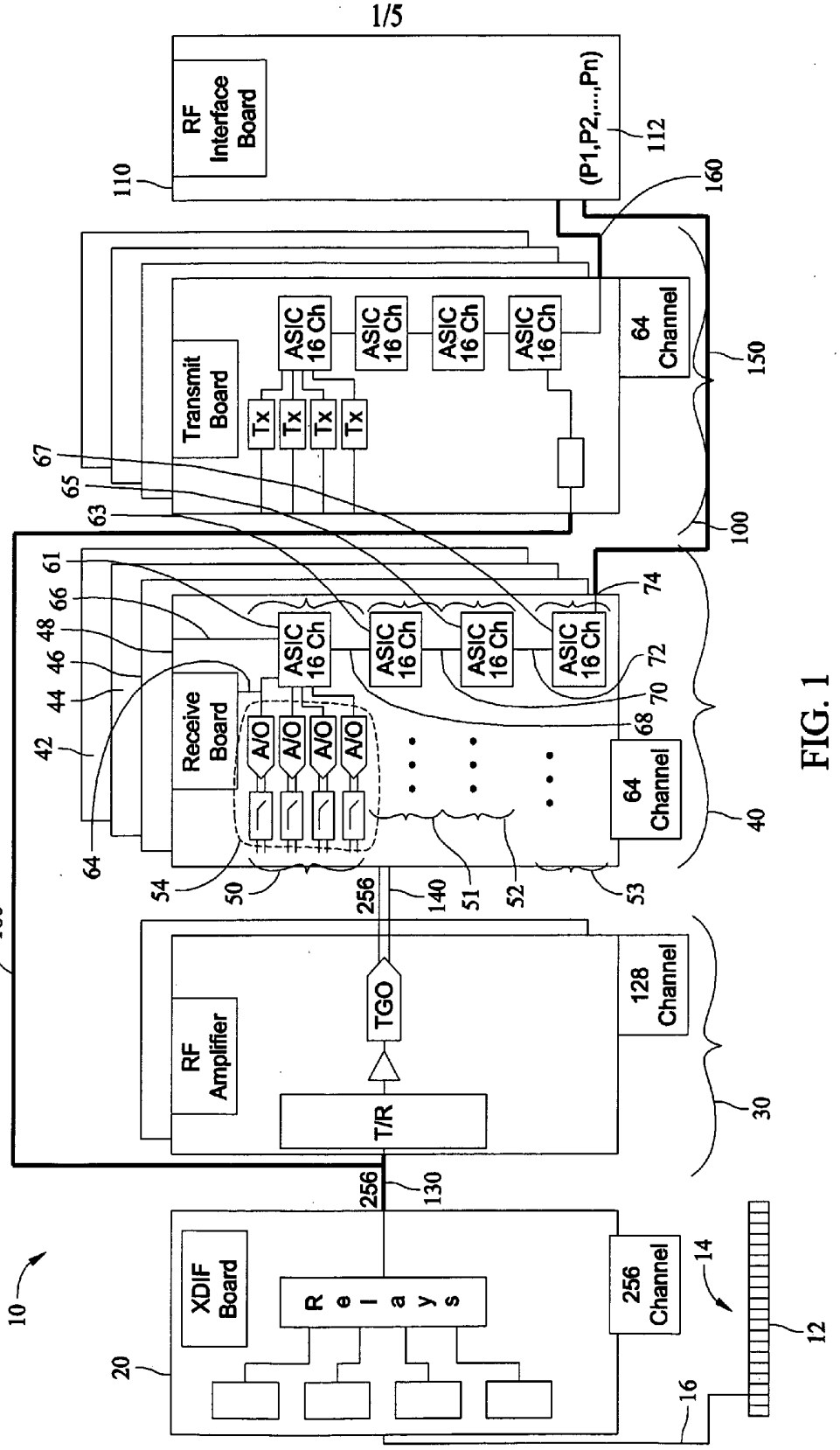

1/5
RF Interface Board
110
(P1,P2,...,Pn)
112
160
Transmit Board
ASIC 16 Ch
Tx
64 Channel
150
67
65
63
100
61
66
48
46
44
42
Receive Board
A/O
74
72
70
68
64
54
50
256
140
51
52
53
40
180
RF Amplifier
TGO
T/R
128 Channel
30
256
130
XDIF Board
Relays
256 Channel
14
12
16
20
10

FIG. 1

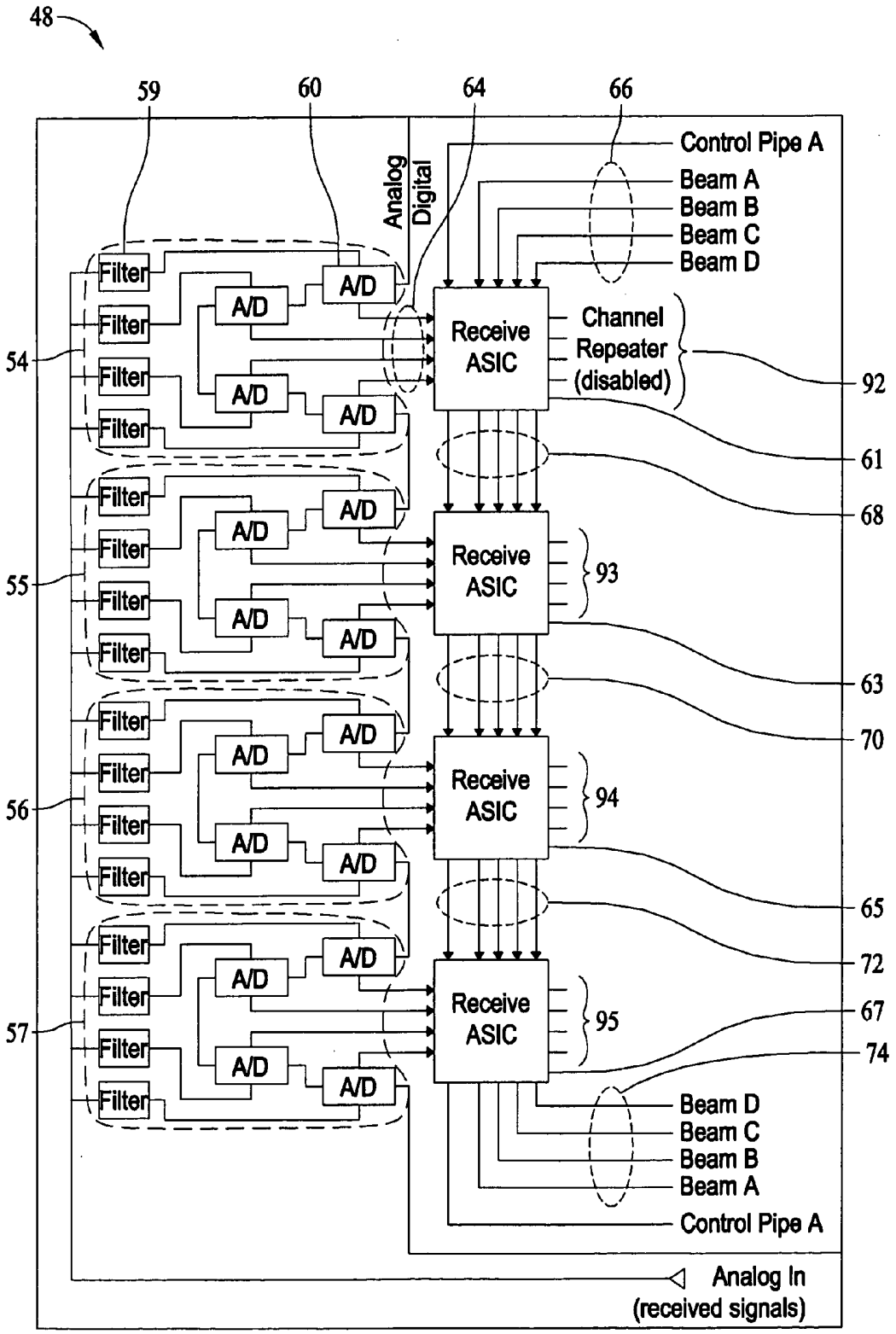

48
59
60
64
66
Analog
Digital
Control Pipe A
Beam A
Beam B
Beam C
Beam D
Filter
A/D
Receive ASIC
Channel Repeater (disabled)
54
55
56
57
92
61
68
93
63
70
94
65
72
95
67
74
Beam D
Beam C
Beam B
Beam A
Control Pipe A
Analog In (received signals)

FIG. 2

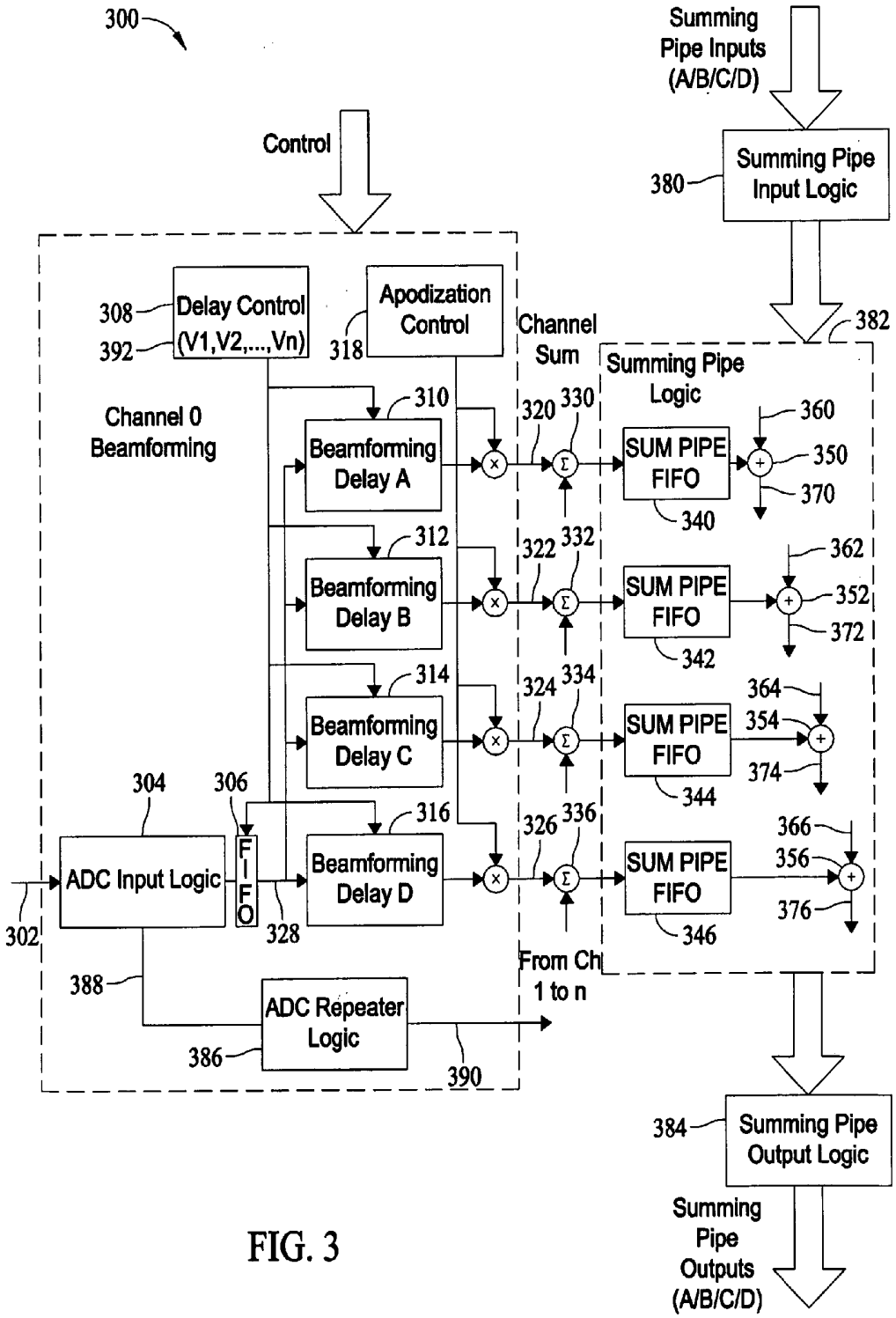

300
Summing Pipe Inputs (A/B/C/D)
Control
380
Summing Pipe Input Logic
308
Delay Control (V1,V2,...,Vn)
392
318
Apodization Control
Channel Sum
382
Summing Pipe Logic
Channel 0 Beamforming
310
Beamforming Delay A
320
330
SUM PIPE FIFO
340
360
350
370
312
Beamforming Delay B
322
332
SUM PIPE FIFO
342
362
352
372
314
Beamforming Delay C
324
334
SUM PIPE FIFO
344
364
354
374
304
306
316
Beamforming Delay D
326
336
SUM PIPE FIFO
346
366
356
376
ADC Input Logic
FIFO
302
328
From Ch 1 to n
388
ADC Repeater Logic
386
390
384
Summing Pipe Output Logic
Summing Pipe Outputs (A/B/C/D)

FIG. 3

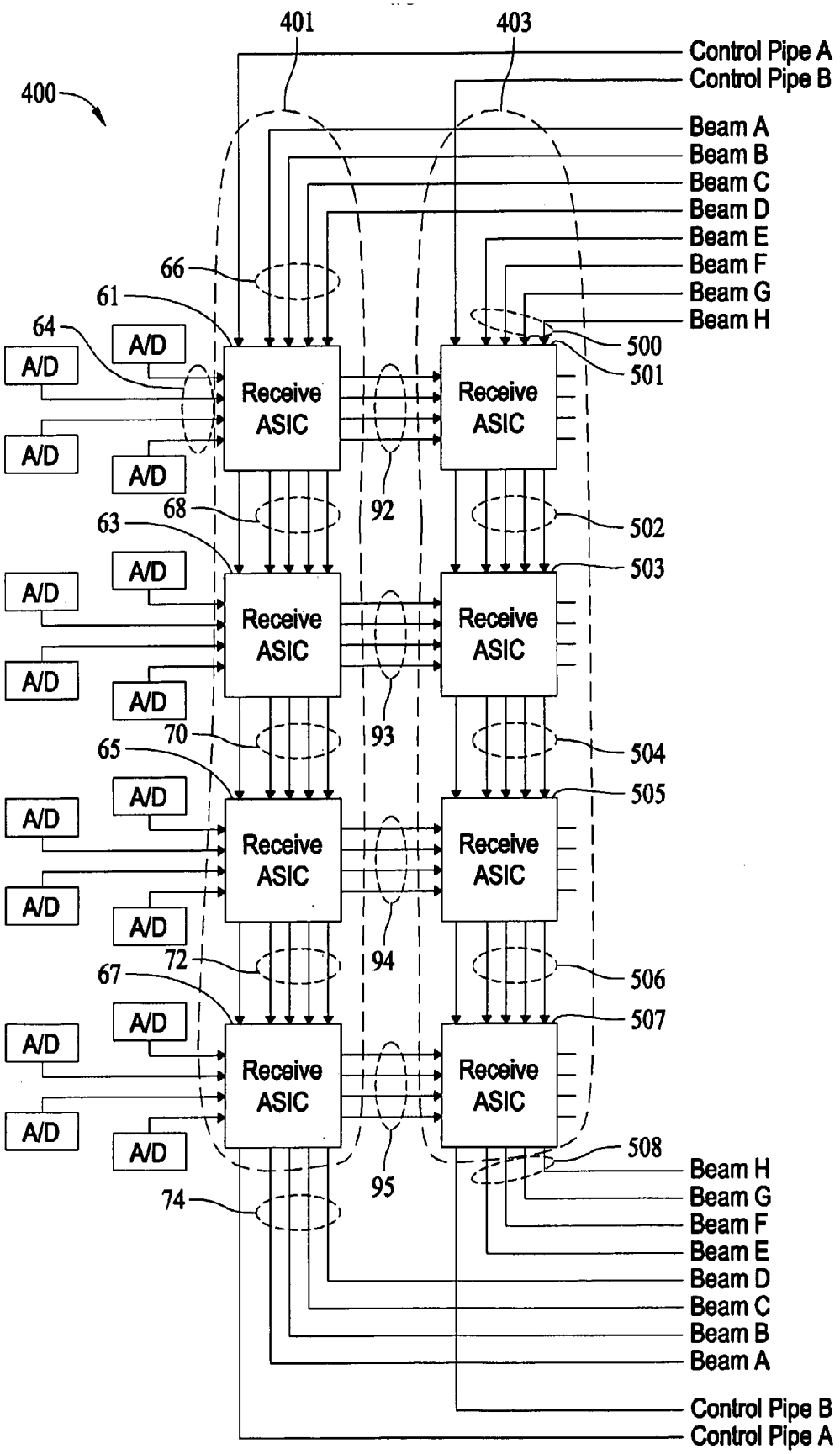

400
401
403
Control Pipe A
Control Pipe B
Beam A
Beam B
Beam C
Beam D
Beam E
Beam F
Beam G
Beam H
66
61
64
63
68
65
70
67
72
74
A/D
Receive ASIC
92
93
94
95
500
501
502
503
504
505
506
507
508

FIG. 4

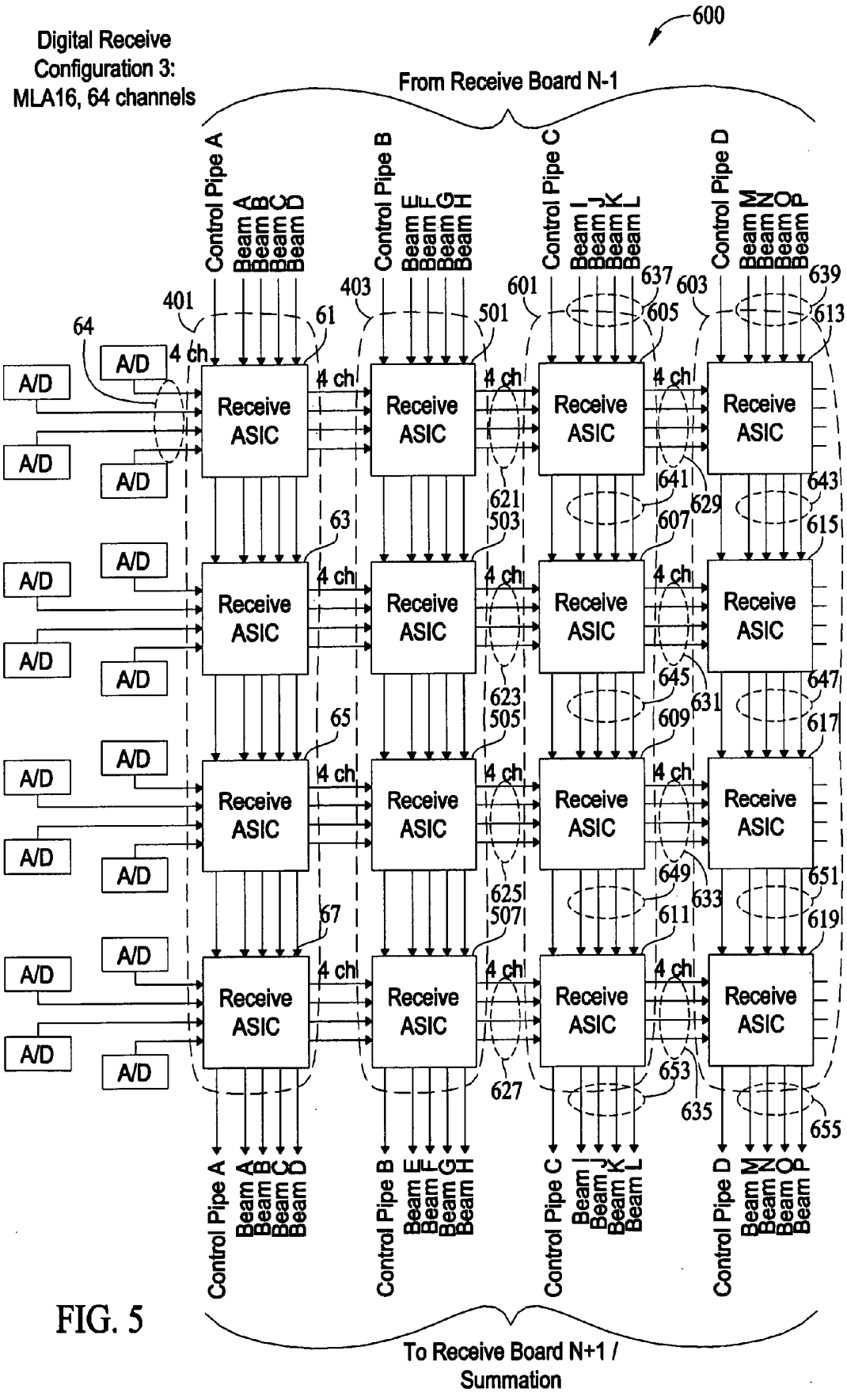

600
Digital Receive Configuration 3: MLA16, 64 channels
From Receive Board N-1
Control Pipe A
Beam A
Beam B
Beam C
Beam D
Control Pipe B
Beam E
Beam F
Beam G
Beam H
Control Pipe C
Beam I
Beam J
Beam K
Beam L
Control Pipe D
Beam M
Beam N
Beam O
Beam P
401
403
601
603
637
639
605
613
64
61
501
A/D
4 ch
Receive ASIC
621
503
641
629
643
607
615
63
623
505
645
631
647
609
617
65
625
507
649
633
651
611
619
67
627
653
635
655
To Receive Board N+1 / Summation

FIG. 5

ULTRASOUND BEAMFORMER WITH SCALABLE RECEIVER BOARDS

BACKGROUND OF THE INVENTION

[0001] The invention relates generally to various aspects of a beamformer (BF) for an ultrasound system.

[0002] Current state-of-the-art beamformers (BFs) use digital custom integrated circuit (CIC) chips to perform the functions of the beamformer associated with the signals transmitted to and received from transducer elements of an ultrasound probe. A CIC chip performs signal processing on a matrix of input signals received from a number of the transducer elements. The transducer elements generate input signals when the transducer elements receive ultrasound echoes from a region of interest in response to an ultrasound scan pulse. The CIC chip combines the matrix of input signals into one or more BF receive beams. Each input signal is also referred to as an input or transducer channel. Conventional CIC chips may handle 64 or 128 or 256 transducer channels on one common chip. The CIC chip uses predetermined sets of delays to form each receive beam from the input signals.

[0003] A CIC chip is designed to use a different set of delays with the same set of input channels or input signals to obtain or form multiple receive beams. The multiple receive beams are associated with the ultrasound echoes from focal points along multiple scan lines for a given ultrasound pulse. In this case, the signals received from multiple transducer elements may be processed simultaneously into multiple receive beams, this process being referred to as multi-line acquisition (MLA). The simultaneous collecting and processing of echo information along multiple scan lines within the subject is referred to as multi-line acquisition (MLA). MLA allows multiple beams to be assembled or formed simultaneously. As the number of MLA beams increases, the CIC chip size (e.g. amount of circuitry) also increases. An alternative to increasing the CIC chip size is to reduce the number of receive inputs in the matrix of receive inputs when increasing the number of MLA beams to be processed by the CIC chip.

[0004] Conventional BF technology dedicates a given size CIC chip and its associated board to a particular MLA size or capability. For example, a system having MLA4 (e.g. simultaneously producing 4 receive beams or 4 multi-line acquisitions) would use a specially designed MLA4 CIC chip and specially designed boards for the MLA4 CIC chips. In order to upgrade an ultrasound system from MLA4 to, for example, MLA8 (e.g., simultaneously producing 8 receive beams or 8 multi-line acquisitions), entirely different dedicated CIC chips and CIC boards would be designed and customized for the MLA8 system. Hence, each CIC chip is customized to produce the receive beams needed from a particular matrix of input signals. As the number of receive beams increases, the internal circuitry of the CIC chip increases. With each increase in the number of receive beams to be produced, the number of duplicated circuits internal to the CIC chip increases, and the CIC chip becomes larger and larger.

[0005] Further, each newly designed CIC chip is masked in silicon which is an expensive nonrecurring engineering (NRE) cost. In the case of MLA8 or MLA16 (8 MLA beams or 16 MLA beams, correspondingly), the CIC chip may cost two to four times more than a CIC chip designed for MLA2 (2 MLA beams). Although lower tier MLA systems do not need and do not have the additional MLA capabilities of higher tier MLA systems, the lower tier MLA systems still bear a significant portion of the costs.

[0006] A seemingly obvious solution is to connect the analog-to-digital converter (ADC) output to multiple CICs. However conventional ADCs have a limited drive capability and most can not drive multiple CIC inputs. In addition, newer ADCs utilize source-synchronous LVDS (Low Voltage Differential Serial) Interfaces. These interface have a significant advantage with reduced I/O and power dissipation for the many ADCs and CICs. This leads to miniaturization with higher levels of integration, i.e. more channels per device. However this type of interface is inherently point-to-point. It typically can not drive multiple inputs without risk of data corruption.

[0007] A need exists for an improved beamformer architecture capable of being scalable between different MLA sizes using the latest, commercially available ADCs

BRIEF DESCRIPTION OF THE INVENTION

[0008] In one exemplary embodiment, a method for developing a beamformer for an ultrasound system is provided. The beamformer includes an RF interface configured to be connected to receiver boards that are connected to a probe. The method includes providing receiver boards, wherein each of the receiver boards is capable of conveying a common number of channels per board and has substantially similar circuit components and layouts. The method also includes selecting a number of channels per probe to be conveyed in parallel between a probe and the receiver boards, wherein the channels per probe is an integer multiple of the channels per board. The method further includes determining a combination of the receiver boards to use in the beamformer based on the number of channels per probe, wherein the receiver boards are capable of being used in at least first and second different combinations that support first and second different numbers of channels per probe.

[0009] In another exemplary embodiment, a beamformer for an ultrasound system is provided and includes an input for receiving ultrasound signals from a probe and an interface for communicating with an ultrasound processor. The beamformer also includes a receiver board interconnecting the input and the interface. The receiver board includes multiple ASICs connecting with one another, with the ASICs including data repeaters to convey the ultrasound signals received at the input between the ASICs.

[0010] In yet another embodiment, a method of performing beamforming in an ultrasound system is provided. The method includes obtaining ultrasound signals from a probe. The ultrasound signals have receive signals associated with channels of the probe. The method also includes configuring an array of ASICs to simultaneously process at least first and second subsets of the receive signals, with the first and second subsets being associated with first and second acquisition lines, respectively. The method further includes passing a portion of the receive signals obtained from the probe between at least two ASICs in substantially an unmodified repeating form.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIG. 1** is a block diagram of an ultrasound system formed in accordance with an embodiment of the present invention;

[0012] **FIG. 2** is a block diagram of the beamformer receive board components in more detail;

[0013] **FIG. 3** is a block diagram illustrating circuitry within an ASIC that processes a receive channel input; and

[0014] **FIG. 4** illustrates an upgrade to the receive board shown in **FIG. 2** when scaling up from an MLA4 arrangement to an MLA8 arrangement.

[0015] **FIG. 5** illustrates yet another upgrade to the receive board shown in **FIG. 2** when scaling up from an MLA4 arrangement to an MLA16 arrangement.

DETAILED DESCRIPTION OF THE INVENTION

[0016] **FIG. 1** is a schematic block diagram of a scalable ultrasound system **10** formed in accordance with an embodiment of the present invention. The ultrasound system **10** includes a transducer array **14** having transducer elements **12**, transducer interface board **20**, preamplifier boards **30**, and receive boards group **40**. Each of the receive boards are identified as receive board **42**, receive board **44**, receive board **46**, and receive board **48**. The ultrasound system **10** also includes transmit boards group **100**, Radio Frequency Interface (RFI) board **110**, and Doppler board **120**. The receive boards group **40**, the transmit boards group **100**, and the RFI board **110** form the beamformer (BF).

[0017] Each of the receive boards in the receive boards group **40**, shown in **FIG. 1** as receive board **42**, receive board **44**, receive board **46**, and receive board **48**, has a similar scalable architecture, and thus only one receive board is described in detail, e.g. receive board **48**. Receive board **48** is comprised of a plurality of Application Specific Integrated Circuit (ASIC) component groups, namely ASIC group **50**, ASIC group **51**, ASIC group **52**, and ASIC group **53**. Each of the ASIC component groups has a similar architecture, and thus only one ASIC group needs to be described in detail, e.g ASIC group **50**. ASIC group **50** has an A/D converter group **54** and an ASIC **61**, the A/D converter group **54** providing inputs **64** to ASIC **61**. The inputs **64** of the ASIC **61** have a repeater function capability which enables the ASIC **61** to supply the inputs **64** of the A/D converter group **54** to another ASIC residing on a receive board (not shown in **FIG. 1**).

[0018] The flow of information and processing in **FIG. 1** is described as follows. The RFI board **110** receives commands from a control processor (not shown in **FIG. 1**) regarding the formation of an ultrasound pulse to be emitted into a region of interest. The RFI board **110** creates transmit parameters from the received commands that determine a transmit beam of a certain shape and from a certain point or points at the surface of the transducer array **14**. The transmit parameters are sent over connection **160** from the RFI board **110** to the transmit boards group **100**. The transmit boards group **100** generate transmit signals from the received transmit parameters. The transmit signals are set at certain levels and are phased with respect to each other to steer and focus the transmit signals into one or more transmit pulses or firings.

[0019] The transmit boards group **100** send the transmit signals over connection **180** through the transducer interface board **20** to drive a plurality of transducer elements **12** within a transducer array **14**. The connection **180** contains a number of individual channels or lines that may equal the number of transducer elements **12**. The transmit signals excite the transducer elements **12** to emit ultrasound pulses. The ultrasound pulses are phased to form a focused beam along a desired scan line. Ultrasound echoes, which are backscattered ultrasound waves from tissue and blood samples within the scanned structure, arrive at the transducer elements **12** at different times depending on the distance into the tissue, from which they return and the angle, at which they contact the surface of the transducer array **14**. The transducer array **14** is a two-way transducer and converts the backscattered waves (ultrasound echoes) of energy into received signals.

[0020] The received signals are conveyed in separate channels from the transducer array **14** over connection **16** to the transducer interface board **20**, which relays the received signals over connection **130** to the preamplifier boards **30**. The preamplifier boards **30** perform time gain compensation (TGC), a.k.a. swept gain, to increase the amplitude of received signals from increasing depths in the body to compensate for the progressive attenuation of the deeper echoes. The amplified received signals from the preamplifier boards **30** are passed over connection **140** to the receive boards group **40**. In the illustrated example, connections **16**, **130**, and **140**, each include 256 channels and the channels in the connection **140** are divided into four groups of 64 channels. Each of the receive boards in the receive boards group **40**, e.g. receive board **48**, receives a group of 64 channels from the preamplifier boards **30**.

[0021] **FIG. 2** is an expanded view of receive board **48**. The receive board **48** receives 64 channels that are divided into four groups of 16 channels. Each channel is formed as a low voltage differential pair which is joined to a corresponding filter and AID converter, e.g. filter **59** and A/D converter **60**. Each filter **59** filters the corresponding signal and each A/D converter **60** converts the filtered signal to a digital signal. Under the guidance of control instructions received from the control processor via the RFI board **110** (control processor and control signaling lines not shown in **FIG. 1**), the filtered, digitized input signals (e.g. inputs **64**) are processed by an ASIC (e.g. ASIC **61**). The processing may include performing time delaying and summation of processed received signals, potentially with summation of prior beam data (e.g. the beam data from bus **66**), so as to construct a received beam from the echoes reflected from a given point within the subject's body. The beam data from ASIC **61** is passed along to a next entity, e.g. to the next ASIC **63** on the same receive board **48** or to an ASIC on the next receive board in the **FIG. 1** receive boards group **40**.

[0022] **FIG. 1** shows four receive boards, **42**, **44**, **46**, and **48**, that are inter-connected such that beam data flows serially from receive board **42** to receive board **44** to receive board **46** to receive board **48**. **FIG. 2** shows that receive board **48** includes ASICs **61**, **63**, **65**, **67** joined serially with one another, such as in a column direction. Each ASIC **61**, **63**, **65**, and **67** receives 16 digitized receive signal inputs, e.g. inputs **64**, from 4 Quad channel A/D converters, e.g. A/D converter group **54**. The received signals at ASIC **61** are processed and summed with one another and potentially also

summed with beam data arriving on bus **66** from a previous receive board **46**. The resulting beam data is placed on bus **68**. Bus **68** conveys the beam data, hereon also referred to as simply data, to ASIC **63**. The beam data received on bus **68** by ASIC **63** may simply be passed, without further processing, onto bus **70** depending upon the source of the beam data. Each of ASICs **61**, **63**, **65** and **67** identify incoming beam data from the bus inputs of buses **66**, **68**, **70** and **72**, respectively,. e.g. beam data for beams A, B, C, and D.. Depending upon the identified beam data, the beam data received on bus **68** by ASIC **63** will be further processed by ASIC **63** in connection with received signals provided directly to the ASIC **63** from A/D converter group **55**. The ASIC **63** will then place the resulting data on bus **70** which is passed to ASIC **65**. The ASIC **65** will either pass data incoming on bus **70** directly to bus **72** without further processing or process the data in connection with received signals provided directly to the ASIC **65** by A/D converter group **56**. The AISC **67** will either pass data incoming on bus **72** directly to bus **74** without further processing or process the data in connection with received signals provided directly to the ASIC **67** by A/D converter group **57**. The beam data on bus **74** is then either passed to a next receive board of the receive boards group **40** (**FIG. 1**) or to high speed serial data bus (HSSDB) **150**[**FIG. 1**].

[**0023**] In **FIG. 1**, processed beam data is passed from receive board **42** to receive board **44**, and then from-receive board **44** to receive board **46**, and then from receive board **46** to receive board **48**. Receive board **48** delivers the resulting fully formed beam data sets for one or more completely constructed beams to the RFI board **110**.

[**0024**] More than one beam may be constructed simultaneously at the receive boards group **40** of **FIG. 1**. The simultaneous collecting and processing of echo information along multiple scan lines within the subject is referred to as multi-line acquisition (MLA). The one or more fully formed beam data sets are passed from the receive boards group **40** over the high speed serial data bus (HSSDB) **150** to the RFI board **110**.

[**0025**] The beam data sets received over the HSSDB **150** are demodulated at the RFI board **110** to create I/Q pairs of demodulated data values. The demodulated data is further processed on the RFI to provide image scan line data including, echo envelope data (B-mode), Color Doppler, and Spectral Doppler and B-Flow. The image scan line data is processed by scan conversion to perform a translation from scan sequence format to display format. The scan converted pixel data is then sent to display component architecture (not shown in **FIG. 1**) to convert the digital pixel data to analog data for display on a monitor.

[**0026**] The ultrasound system **10** has a scalable architecture in that the ultrasound system **10** may be expanded or upgraded on demand by adding ASICs to existing receive boards and/or adding receive boards. A system can be configured in the factory, late in the assembly process, to provide the number of channels and MLA for a specific model or customer order. The ASICs and receive boards already in the ultrasound system **10** do not require a redesign in order to expand or reduce the system and/or its capacity. Each receive board of the receive boards group **40** is comprised of substantially similar circuitry and components and layouts such that each receive board can be easily expanded or scaled upwards in capacity by adding similar components. An expanded board will still work properly with other system components or boards without requiring re-design, the components or boards being similarly scaled upwards as required by adding similar component modules. One possible scalable configuration is exhibited by the configuration of receive board **48** in **FIG. 1**.

[**0027**] In this configuration, each of the receive boards, **42**, **44**, **46**, and **48**, of the receive boards group **40** handles a common number of channels, in this example 64 channels per board. A channel supplies a single receive signal corresponding to one of the transducer elements **12** of the transducer array **14**. Any number of receive boards similar to receive board **48** may be joined in a daisy chain or serial arrangement depending upon the number of channels to support. For example, two receive boards may be used each with 128 channels, or eight received boards may be used each with 512 channels, and the like.

[**0028**] **FIG. 3** illustrates an individual ASIC receive circuit block **300** for processing serial channel input **302**. Each ASIC may include multiple ASIC receive circuit blocks **300**. For example, ASIC **61** may have 16 ASIC receive circuit blocks **300** for processing 16 individual channel inputs. Each serial channel input may be received as a filtered, digitized serial stream of bits in the form of low voltage differential signaling (LVDS) at ADC input logic **304**. For example, the channel input may be a series of 12 bits as opposed to clocking in 12 parallel inputs to 12 signal pins. Input logic **304** converts the serial channel input **302** into parallel outputs, which are interpolated (upsampled) and input to a FIFO buffer **306**. Delay control **308** informs the FIFO buffer **306** of the predetermined delay to create the data for a beam. Examples of beams are partial beam A **320**, partial beam B **322**, partial beam C **324**, and partial beam D **326**. The FIFO buffer **306** receives input data from input logic **304** and produces, in this example, four times as much data. In this example, the FIFO buffer **306** may receive one value every 10 nanoseconds and produce four consecutive values every 10 nanoseconds for each of the four beamforming delays, beamforming delay A **310**, beamforming delay B **312**, beamforming delay C **314**, and beamforming delay D **316**. Each of the four beamforming delays, e.g. beamforming delay A **310**, receives an input value from the FIFO buffer **306** over bus **328** in round robin fashion. The FIFO buffer **306** uses different delays to produce data for each of the four beamforming delayscorresponding to four-different beams (MLA4). Each of the four beamforming delays interpolate the input value received. An apodization calculation (from an apodization control **318**) is applied to each of the interpolated values produced from the four beamforming delays **310**, **312**, **314**, and **316** that results in corresponding outputs of partial beams A **320**, B **322**, C **324**, and D **326**. Each resulting partial beam output, e.g. partial beam A **320**, may not be a complete beam, but only part of a complete beam. Often beams are formed using array apertures greater than 16 channels. In this case the beamformer sums the partially beamformed signal from multiple ASICs. In the example case of a 256 element aperture with MLA4 , the beamformer sums the outputs from 16 receive ASICs, each providing partial sums of 16 channels.

[**0029**] Partial beam A **320** is summed by ASIC summation **330** with partial beam A output data from other similar circuit blocks **300** of the ASIC, resulting in a summed partial

beam A that is stored in sum pipe FIFO **340**. Likewise, ASIC summations **332**, **334**, and **336** produce summed partial beams for partial beams B **322**, C **324**, and D **326** that are correspondingly stored in sum pipe FIFOs **342**, **344**, and **346**. Summing pipe input logic **380** may receive processed beam data in the form of serial input from a previous ASIC (possibly from an ASIC of a different board) and generate parallel outputs corresponding to accumulated beams A **360**, B **362**, C **364**, and D **366** for use in a summing pipe logic **382**. Adders **350**, **352**, **354**, and **356** correspondingly add the accumulated beams A **360**, B **362**, C **364**, and D **366** to the summed partial beams A, B, C, and D from corresponding FIFOs **340**, **342**, **344**, and **346** to produce the corresponding accumulated beams **370**, **372**, **374**, and **376**. For example, adder **350** adds the accumulated beam A **360** to the summed partial beam A from FIFO **340** to produce the accumulated beam A **370**. Likewise, adder **352** adds the accumulated beam B **362** to the summed partial beam B from FIFO **342** to produce the accumulated beam B **372**, adder **354** adds the accumulated beam C **364** to the summed partial beam C from FIFO **344** to produce the accumulated beam C **374**, and adder **356** adds the accumulated beam D **366** to the summed partial beam D from FIFO **346** to produce the accumulated beam D **376**. Summing pipe output logic **384** receives the accumulated beams A **370**, B **372**, C **374**, and D **376** and produces a serialized output of the accumulated beams for use by a next ASIC.

[**0030**] Translating the above for all receive ASICs, a summing pipe composed of the individual summing pipe logic of each ASIC (e.g. summing pipe logic **382**) provides the summation of the 16 channel partial sums to provide a complete beam, e.g. Beam A. This summing pipe is composed of adders in each ASIC. The summing pipe logic of an ASIC adds the **16** channel partial sum with a summing input from the previous ASIC, and then outputs this new sum to the summing pipe input of the next ASIC in a column. A FIFO between the apodization circuit and summing pipe adder, e.g. summing pipe FIFO **340**, aligns the partial sum with the summing pipe data. The summing pipe FIFO, e.g. FIFO **340**, needs more delay to align partial data with summing pipe data in ASICs further along the summing pipe.

[**0031**] The serial summing pipe input to ASIC **61** is deserialized and passed as parallel data within the ASIC **61** from internal component to internal component (described within the description of **FIG. 3**). The resultant beam data from the ASIC **61** is again serialized for delivery to the next ASIC in the chain or column of ASICs of a receive board, or to the next ASIC on the next ASIC receive board in the chain of ASIC receive boards, or to the HSSDB.

[**0032**] ASIC **61** of **FIG. 2** also has a repeater function or repeater capability, e.g. an ADC repeater logic **386** as shown in **FIG. 3**. To afford the repeater functionality, the deserialized channel output **388** of the ASIC receive circuit block **300** is tapped off and combined with likewise other deserialized channel outputs **388** from the receive circuit blocks **300** of the ASIC **61**. The combination of deserialized channel outputs **388** are then serialized by the ADC repeater logic **386** to produce a serial output **390** (same as serial output **92** of **FIG. 2**) from the ASIC **61**. In **FIG. 2**, channel repeater outputs **92** are identical to the inputs **64**. The channel repeater outputs **92** are not further used, and are shown disabled, because channel repeater outputs **92** are not needed in producing the four MLA4 receive beams for the example of **FIG. 2**. However, **FIG. 4** shows an MLA8 scaled up version of the receive board of **FIG. 2** that utilizes the channel repeater outputs **92**.

[**0033**] **FIG. 4** shows a receive board **400** that has been scaled up from the capacity of receive board **48** of **FIG. 2**. The receive board **400** includes two columns **401** and **403** of ASICs **61**, **63**, **65**, **67** and **501**, **503**, **505** and **507**, respectively. The ASICs **501**, **503**, **505**, and **507** each receive corresponding channel repeater outputs **92**, **93**, **94**, and **95** from ASICs **61**, **63**, **65** and **67**. The second column **403** of ASICs may receive signal inputs directly from an A/D converter group, e.g. inputs **64**, or from a repeater, e.g. channel repeater outputs **92**. The second column **403** of ASICs process receive signal inputs to produce beam data in addition to the beam data produced by the first column **401** of ASICs, ASICs **61**, **63**, **65**, and **67**. Thus, in the example of **FIG. 4**, the first column **401** performs beam processing for beams A, B, C, and D, and the second column **403** perform beam processing for beams E, F, G, and H. Alternatively, more columns, for example, two more columns may be added, giving a total of four columns of ASICs on the receive board, for an MLA16 configuration for processing 16 MLA beams.

[**0034**] In general, each column of ASICs functions similarly. An ASIC may receive filtered, digitized input signals from either the repeater of another ASIC or from an A/D converter group. An ASIC processes the needed beam data from the input signals, and potentially adds to the processed beam data. Beam data to potentially be added may be received from a previous ASIC in the column of ASICs or received from an ASIC of an ASIC column on a previous ASIC receive board. ASIC beam data is passed downwards in a column of ASICs from one ASIC to the next (a next ASIC possibly being in a column of ASICs on a next receive board). In the case of the last ASIC, the ASIC beam data is output onto the HSSDB **150**.

[**0035**] In one embodiment, the output from a column **401** (**FIG. 4**) of ASICs of a receive board is passed over a backplane (not shown in the figures) to provide the input to a column on a next receive board. The last receive board is connected to the RFI board **110** via the HSSDB **150** (**FIG. 1**). The first receive board has inputs logically set to zero. In an alternative embodiment, each receive board contains another interface FPGA/ASIC (not shown in the figures) which converts the data streams into a high speed data bus (HSDB). The HSDB transports data from a receive board over a backplane and either to a next receive board where the HSDB data is summed in the summing pipe of the next receive board, or to the RFI board **110** via the HSSDB **150**. Although a serial interface is preferred for the HSDB, a parallel interface could be used as well.

[**0036**] In the example of **FIG. 4**, ASIC **501** may receive beam data from bus **500** from a previous receive board. ASIC **503** receives beam data on bus **502** and outputs beam data on bus **504**. ASIC **505** receives beam data on bus **504** and outputs beam data on bus **506**. ASIC **507** receives beam data on bus **506** and outputs beam data on bus **508**. Bus **508** may connect to a next receive board of ASICs or, in the case whereby beam processing is complete, may connect to the HSSDB **150** of **FIG. 1**.

[**0037**] **FIG. 5** shows a receive board **600** that has been scaled up from the capacity of receive board **48** of **FIG. 2**.

The receive board **600** includes four columns **401**, **403**, **601** and **603** of ASICs **61**, **63**, **65**, **67**, ASICs **501**, **503**, **505**, **507**, ASICs **605**, **607**, **609**, **611**, and ASICs **613**, **615**, **617** and **619** respectively. The ASICs **605**, **607**, **609**, and **611** each receive corresponding channel repeater outputs **621**, **623**, **625**, and **627** from ASICs **501**, **503**, **505** and **507**. The ASICs **613**, **615**, **617**, and **619** each receive corresponding channel repeater outputs **629**, **631**, **633**, and **635** from ASICs **605**, **607**, **609** and **611**. The third column **601** of ASICs may receive signal inputs directly from an A/D converter group, e.g. inputs **64**, or from a repeater, e.g. channel repeater outputs **621**. The fourth column **603** of ASICs may receive signal inputs directly from an A/D converter group, e.g. inputs **64**, or from a repeater, e.g. channel repeater outputs **629**. The third column **601** of ASICs process receive signal inputs to produce beam data in addition to the beam data produced by the first column **401** and second column **403** of ASICs. The fourth column **603** of ASICs process receive signal inputs to produce beam data in addition to the beam data produced by the first column **401**, second column **403**, and third column **601** of ASICs. Thus, in the example of **FIG. 5**, the first column **401** performs beam processing for beams A, B, C, and D, the second column **403** performs beam processing for beams E, F, G, and H, the third column **601** performs beam processing for beams I, J, K, and L, and the fourth column **603** performs beam processing for beams M, N, O, and P.

[**0038**] In general, each column of ASICs functions similarly. An ASIC may receive filtered, digitized input signals from either the repeater of another ASIC or from an A/D converter group. An ASIC processes the needed beam data from the input signals, and potentially adds to the processed beam data. Beam data to potentially be added may be received from a previous ASIC in the column of ASICs or received from an ASIC of an ASIC column on a previous ASIC receive board. ASIC beam data is passed downwards in a column of ASICs from one ASIC to the next (a next ASIC possibly being in a column of ASICs on a next receive board). In the case of the last ASIC, the ASIC beam data is output onto the HSSDB.

[**0039**] In the example of **FIG. 5**, ASIC **605** may receive beam data from bus **637** from a previous receive board and ASIC **613** may receive beam data from bus **639** from a previous receive board. ASIC **607** receives beam data on bus **641** and outputs beam data on bus **645**, and ASIC **615** receives beam data on bus **643** and outputs beam data on bus **647**. ASIC **609** receives beam data on bus **645** and outputs beam data on bus **649**, and ASIC **617** receives beam data on bus **647** and outputs beam data on bus **651**. ASIC **611** receives beam data on bus **649** and outputs beam data on bus **653**, and ASIC **619** receives beam data on bus **651** and outputs beam data on bus **655**. Bus **653** and **655** may connect to next receive boards of ASICs or, in the case whereby beam processing is complete, may connect to the HSSDB **150** of **FIG. 1**.

[**0040**] Optionally, all of the MLA beams may not be processed in one ASIC. By not attempting to process all MLA beams for the system within one ASIC, the circuitry of the ASIC need not grow in size as the MLA size increases or is up scaled. Rather than increasing the ASIC circuitry (e.g. the summing pipe circuitry) to handle more MLA beams as the system is up scaled for a greater number of MLAs, the up scaled system may be obtained by adding more ASICs of substantially similar construction. The ASIC in this way serves as a modular component whereby the system MLA size may be increased by adding more ASICs, for example, by adding more columns of ASICs.

[**0041**] The ASIC is modular in that the ASIC need not be re-designed when up scaling the MLA number, but rather up scaling of the MLA number may be achieved by adding more of the same kind of ASIC to the receive boards. The receive board may also be made modular. Although the receive board of **FIG. 2** shows only one column of ASICs, the board may be designed with empty sockets or space for a pad of the empty sockets.

[**0042**] When the number of MLA beams increases, a number of columns of ASICs may be added to the receive board to perform the processing for the increased number of MLA beams. For example, in **FIG. 4**, the first column of ASICs, ASICs **61**, **63**, **65**, and **67**, may process beams A, B, C, and D for an MLA4 system. Empty ASIC sockets or space for a pad of ASICs could be provided on the receive board for future growth. When the customer needs to up scale from an MLA4 system (see **FIG. 2**) to an MLA8 system (see **FIG. 4**), the second column of ASICs of **FIG. 4**, ASICs **501**, **503**, **505**, and **507**, may be added to the receive boards. In likewise manner, a receive board may be designed to hold four columns of ASICs, and when fully populated with four columns of ASICs, would be able to perform the processing for an MLA16 system wherein 16 MLA beams are processed. Thus, the receive board may be modular in that the receive board need not be re-designed when the MLA number for the system is increased.

[**0043**] As the number of MLA beams to be processed is increased, the amount of data being passed from the receive boards to the RFI board increases dramatically from one ultrasound pulse or firing to the next. A HSSDB, as exemplified by HSSDB **150** in **FIG. 1**, may be used to transport the large amounts of beam data collected between ultrasound pulses or firings. Without the use of a HSSDB, the time to transport the larger amount of beam data for higher MLA numbers could become significant enough to impact the framing rate, or time between pulses.

[**0044**] Optionally, control processor (not shown in **FIG. 1**) or the RFI board (or a board with similar functionality, hereon referred to as RFI or RFI board) may perform calculations on global parameters (the global parameters **112** as shown in **FIG. 1**) to obtain receive delay control values. Alternatively, the RFI board may broadcast the global parameters **112** over a high speed serial control bus (HSSCB) (not shown in **FIG. 1**) to all the ASICs of the receive boards group **40**. The global parameters **112** provide a global or system level description of the focus trajectories for the receive beams. Each ASIC uses the received global parameters as input for a starting point to compute receive delay control values, as exemplified by the receive delay control values **392** in **FIG. 3**. The computed receive delay control values determine for every receive channel the delay values for every beam to be processed from the receive channel. By sending the global parameters, instead of the receive delay control values, from the RFI to the receive boards, a much lesser amount of control data may be transported from the RFI to the receive boards over the HSSCB. Lesser control data being transported may result in less time being needed between ultrasound pulses for setup

of control information, and may result in more time being available for beam data processing.

[0045] Examples of global parameter information are the coordinates within a coordinate space, such as the starting focus point and the ending focus point, and the rate at which the focus point changes along the MLA line or focus trajectory. Examples of receive delay control values are the initial delay, the start delay, the delay rate of change, and the different delay inflection points. All the receive delay control values are at the transducer element level in that the receive delay control values would have to be calculated and passed down from the RFI to the receive ASICs for every transducer element or receive channel, if not being computed by the ASICs based on the global parameters information.

[0046] While the invention has been described in terms of various specific embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the claims.

What is claimed is:

1. A method for developing a beamformer for an ultrasound system, the beamformer having an RF interface configured to be connected to receiver boards that are connected to a probe, said method comprising:

providing receiver boards, wherein each of said receiver boards is capable of conveying a common number of channels per board and has substantially similar circuit components and layouts;

selecting a number of channels per probe to be conveyed in parallel between a probe and the receiver boards, wherein the channels per probe is an integer multiple of the channels per board; and

determining a combination of the receiver boards to use in the beamformer based on the number of channels per probe, wherein the receiver boards are capable of being used in at least first and second different combinations that support first and second different numbers of channels per probe.

2. The method of claim 1, wherein the number of channels per board is one of 256, 192, 128, and 64 channels.

3. The method of claim 1, wherein the numbers of channels per probe is one of 256, 192, 128 and 64.

4. The method of claim 1, wherein the number if channels per board is 64 and the number of channels per probe is 256.

5. The method of claim 1, further compromising selecting first and second probes that use different first and second numbers of channels per probe, wherein the first probe is joined with two receiver boards and the second probe is joined with four receiver boards.

6. A beamformer for an ultrasound system, comprising:

an input for receiving ultrasound signals from a probe;

an interface for communicating with an ultrasound processor; and

a receiver board interconnecting said input and said interface, said receiver board including multiple ASICs connecting with one another, said ASICs including data repeaters to convey said ultrasound signals received at said input between said ASICs.

7. The beamformer of claim 6, wherein said ASICs are interconnected in a two dimensional array of rows and columns.

8. The beamformer of claim 6, where in said ASICs are connected in a cascade configuration in a first direction and in a flow-through configuration in a second direction.

9. The beamformer of claim 6, wherein said ASICs process said ultrasound data and pass processed ultrasound data between one another.

10. The beamformer of claim 6, further compromising multiple receiver boards connected in a daisy chain configuration to pass processed and unprocessed ultrasound data therebetween.

11. The beamformer of claim 6, wherein said ASICs each include channel inputs configured to accept receive signals associated with individual transducer elements of said probe, said ASICs each including bus inputs configured to accept beam data from other ASICs.

12. The beamformer of claim 6, wherein at least one of said ASICs processes a subset of said ultrasound signals to produce beam data forming a portion of a beam data set that defines an acquisition line in an area of interest.

13. The beamformer of claim 6, wherein first and second subsets of said ASICs process portions of said ultrasound signals to produce first and second beam data sets that define first and second acquisition lines, respectively.

14. The beamformer of claim 6, wherein said ASICs are joined by data buses that convey beam data between said ASICs, said ASICs processing said ultrasound signals from said input to generate said beam data in a cascaded manner.

15. The beamformer of claim 6, wherein said data repeater output, from a corresponding ASIC, said ultrasound signals received at said input substantially unchanged.

16. The beamformer of claim 6, wherein said ASICs are joined by a bus conveying beam data between said ASICs, said ASICs modifying a portion of said beam data based on said ultrasound signals for a predetermined acquisition line.

17. A method of performing beamforming in an ultrasound system, said method comprising:

obtaining ultrasound signals from a probe, said ultrasound signals having receive signals associated with channels of the probe;

configuring an array of ASICs to simultaneously process at least first and second subsets of said receive signals, said first and second subsets being associated with first and second acquisition lines, respectively; and

passing a portion of said receive signals obtained from said probe between at least two ASICs in substantially an unmodified repeating form.

18. The method of claim 17, further comprising interconnecting the array of ASICs into a two dimensional array of rows and columns.

19. The method of claim 17, wherein the array is one dimensional.

20. The method of claim 17, further comprising connecting the ASICs in a cascade configuration in a first direction and in a flow-through configuration in a second direction.

21. The method of claim 17, wherein said configuring includes the ASICs in a daisy-chain configuration.

22. The method of claim 17, further comprising generating at a first ASIC a partial beam data set from said first subset of said receive signals and conveying said partial beam data set to a second ASIC.

23. The method of claim 17, further comprising generating as a first ASIC a partial beam data set from said first

subset of said receive signals and passing said partial beam data set through a second ASIC in a substantially unmodified, repeated form.

24. The method of claim 17, wherein said processing generates first and second partial beam data sets, further comprising conveying said first and second partial beam data sets in cascade between ASICs.

25. The method of claim 17 generating, at a first ASIC, a partial beam data set based on a first group of receive signals associated with said first acquisition line, passing said partial beam data set to a second ASIC and passing said first group of receive signals to a third ASIC.

* * * * *

专利名称(译)	具有可伸缩接收器板的超声波束形成器		
公开(公告)号	US20060173335A1	公开(公告)日	2006-08-03
申请号	US11/033188	申请日	2005-01-11
[标]申请(专利权)人(译)	通用电气公司		
申请(专利权)人(译)	通用电气公司		
当前申请(专利权)人(译)	通用电气公司		
[标]发明人	SHAH SNEHAL CHANDRAKANT MILLER STEVEN CHARLES MORITZ MICHAEL RICHARD		
发明人	SHAH, SNEHAL CHANDRAKANT MILLER, STEVEN CHARLES MORITZ, MICHAEL RICHARD		
IPC分类号	A61B8/06		
CPC分类号	G01S7/52023		
其他公开文献	US8002708		
外部链接	Espacenet USPTO		

摘要(译)

提供了一种用于超声系统的波束形成器和用于开发波束形成器的方法。波束形成器包括RF接口，RF接口被配置为连接到连接到探针的接收器板。该方法包括提供接收器板，其中每个接收器板能够为每个板传送共同数量的通道并且具有基本相似的电路组件和布局。该方法还包括选择每个探针的多个通道以在探针和接收器板之间并行传送，其中每个探针的通道是每个板的通道的整数倍。该方法还包括基于每个探针的通道数确定要在波束形成器中使用的接收器板的组合，其中接收器板能够以支持第一和第二不同数量的至少第一和第二不同组合的至少第一和第二不同组合使用。每个探针的通道。