



US 20080071171A1

(19) **United States**(12) **Patent Application Publication**
Amemiya(10) **Pub. No.: US 2008/0071171 A1**(43) **Pub. Date: Mar. 20, 2008**(54) **ULTRASONIC TRANSDUCER DRIVING CIRCUIT AND ULTRASONIC DIAGNOSTIC APPARATUS****Publication Classification**(51) **Int. Cl.**
A61B 8/00 (2006.01)
H01L 41/09 (2006.01)(52) **U.S. Cl. 600/437; 310/314; 310/318; 310/319; 600/443**(76) **Inventor:** Shinichi Amemiya, Tokyo (JP)**Correspondence Address:****Patrick W. Rasche****Armstrong Teasdale LLP****Suite 2600, One Metropolitan Square****St. Louis, MO 63102**(21) **Appl. No.:** 11/854,255(22) **Filed:** Sep. 12, 2007(30) **Foreign Application Priority Data**

Sep. 14, 2006 (JP) 2006-248830

(57) **ABSTRACT**

With the aim of quickly returning the voltage of an output line to an ultrasonic transducer from a positive voltage or a negative voltage to the ground voltage and reducing the circuit size, immediately after turning on and turning off of a positive FET in accordance with a positive pulse signal, a negative FET goes on for only a pull-back period allowing for the output line to return to the ground voltage. Also, immediately after turning on and turning off of the negative FET in accordance with a negative pulse signal, the positive FET goes on for only a pull-back period allowing for the output line to return to the ground voltage.

ULTRASONIC TRANSDUCER DRIVING CIRCUIT

10

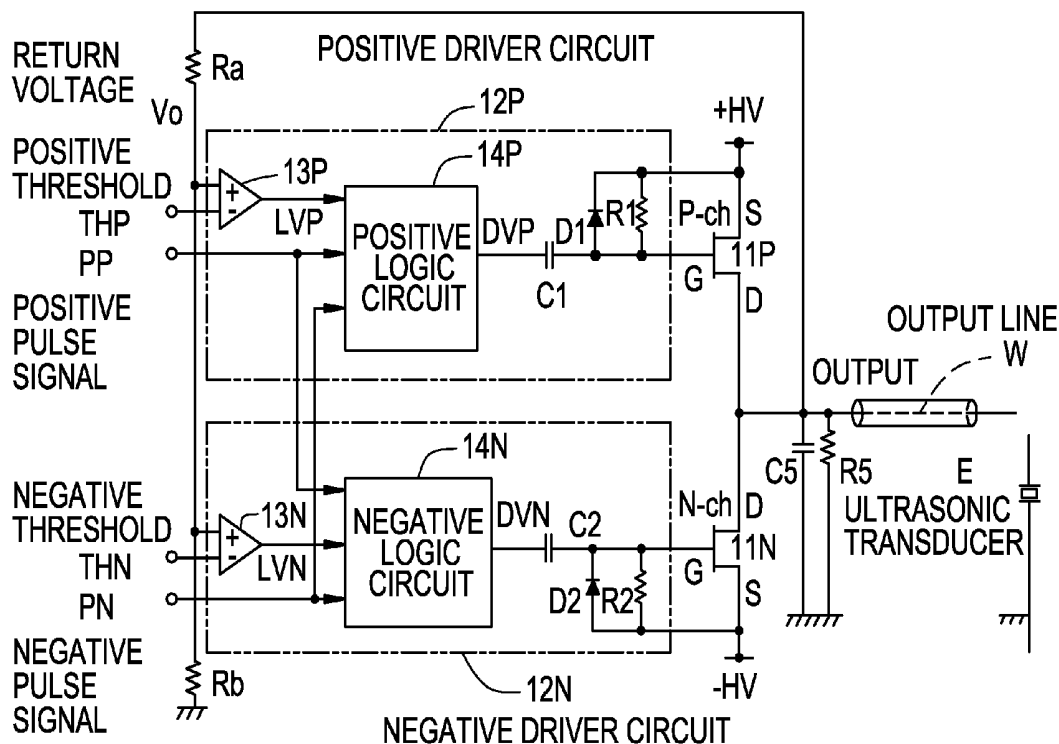


FIG. 1

ULTRASONIC DIAGNOSTIC APPARATUS

100

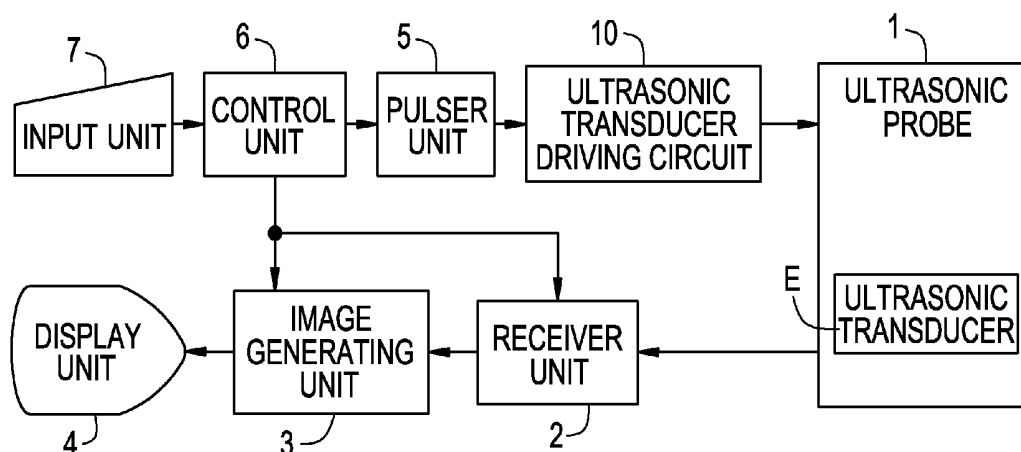


FIG. 2

ULTRASONIC TRANSDUCER DRIVING CIRCUIT

10

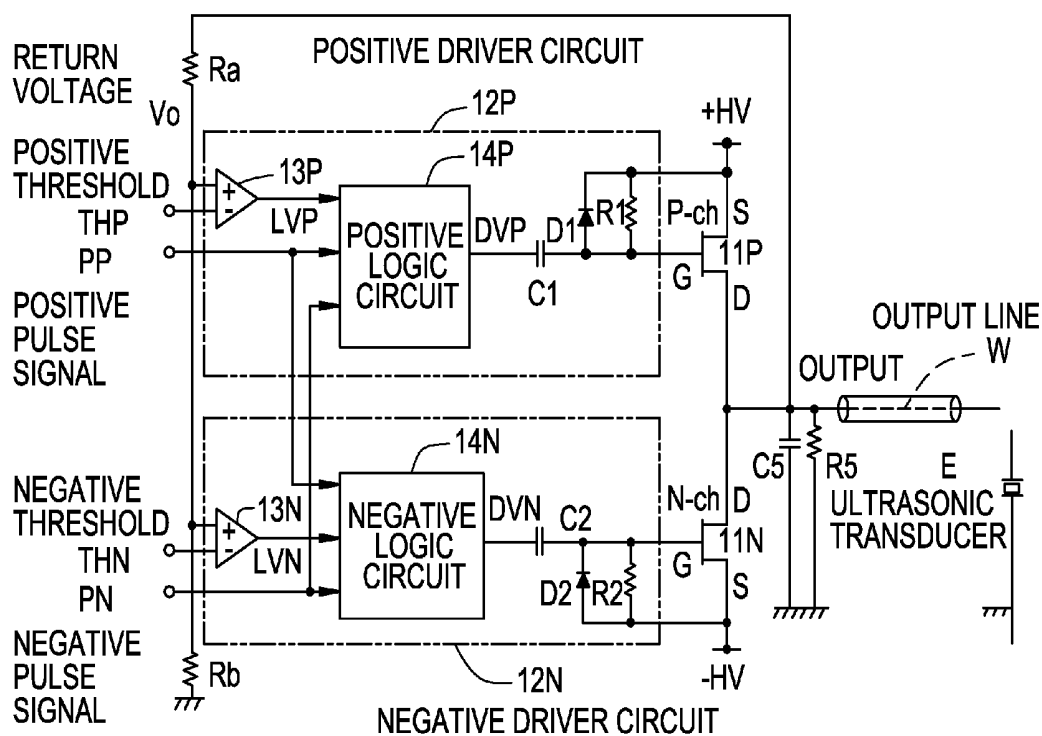


FIG. 3

POSITIVE LOGIC CIRCUIT

14P

PP	PN	LVP	DVP
L	L	L	Xh
L	L	H	L
L	H	L	Xh
L	H	H	Xh
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	H

NEGATIVE LOGIC CIRCUIT

14N

PP	PN	LVN	DVN
L	L	L	L
L	L	H	L
L	H	L	X1
L	H	H	X1
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	H

FIG. 4

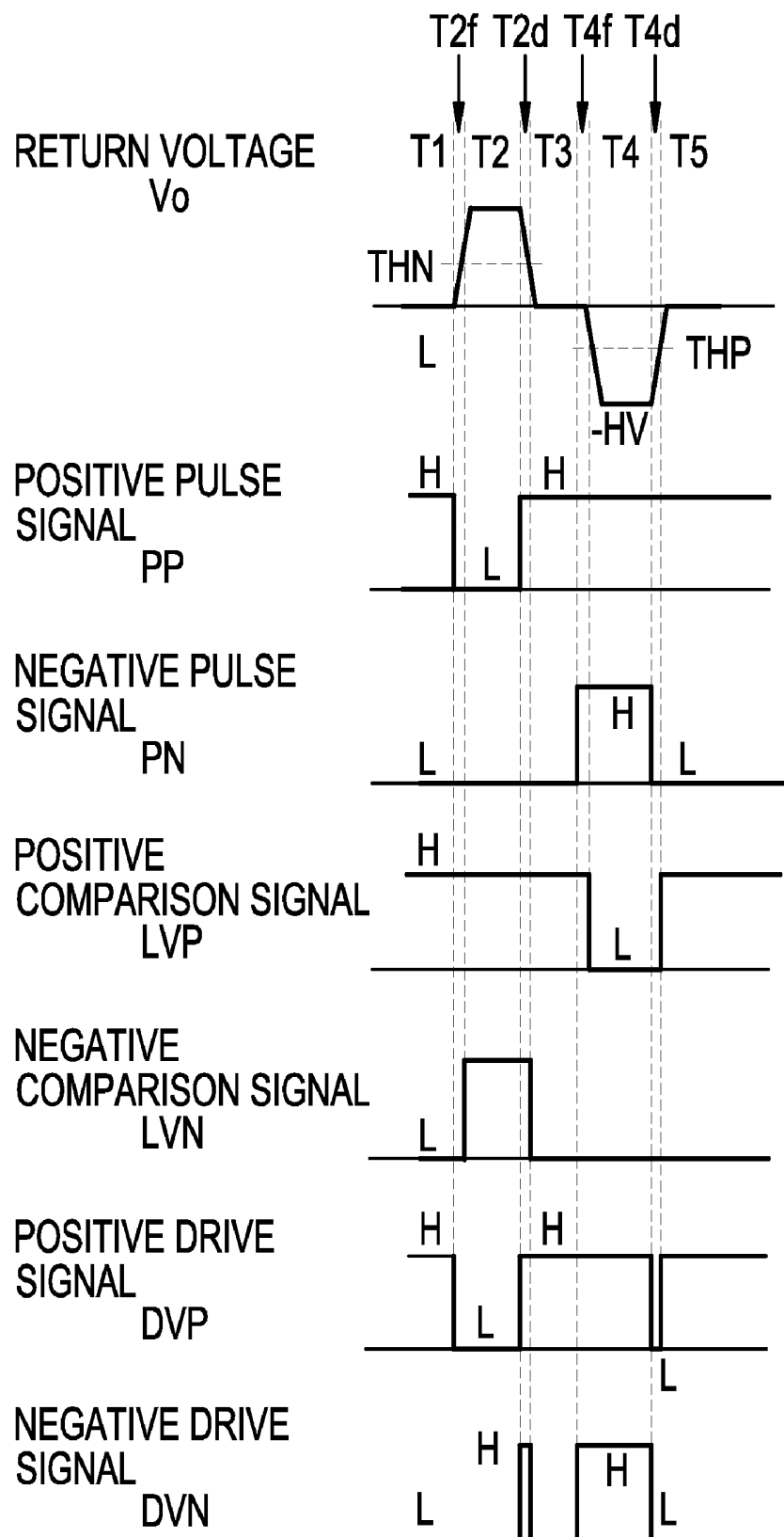


FIG. 5

	PP	PN	LVP	LVN	DVP	DVN
T1	H	L	H	L	H	L
T2f	L	L	H	L	L	L
T2	L	L	H	H	L	L
T2d	H	L	H	H	H	H
T3	H	L	H	L	H	L
T4f	H	H	H	L	H	H
T4	H	H	L	L	H	H
T4d	H	L	L	L	L	L
T5	H	L	H	L	H	L

FIG. 6

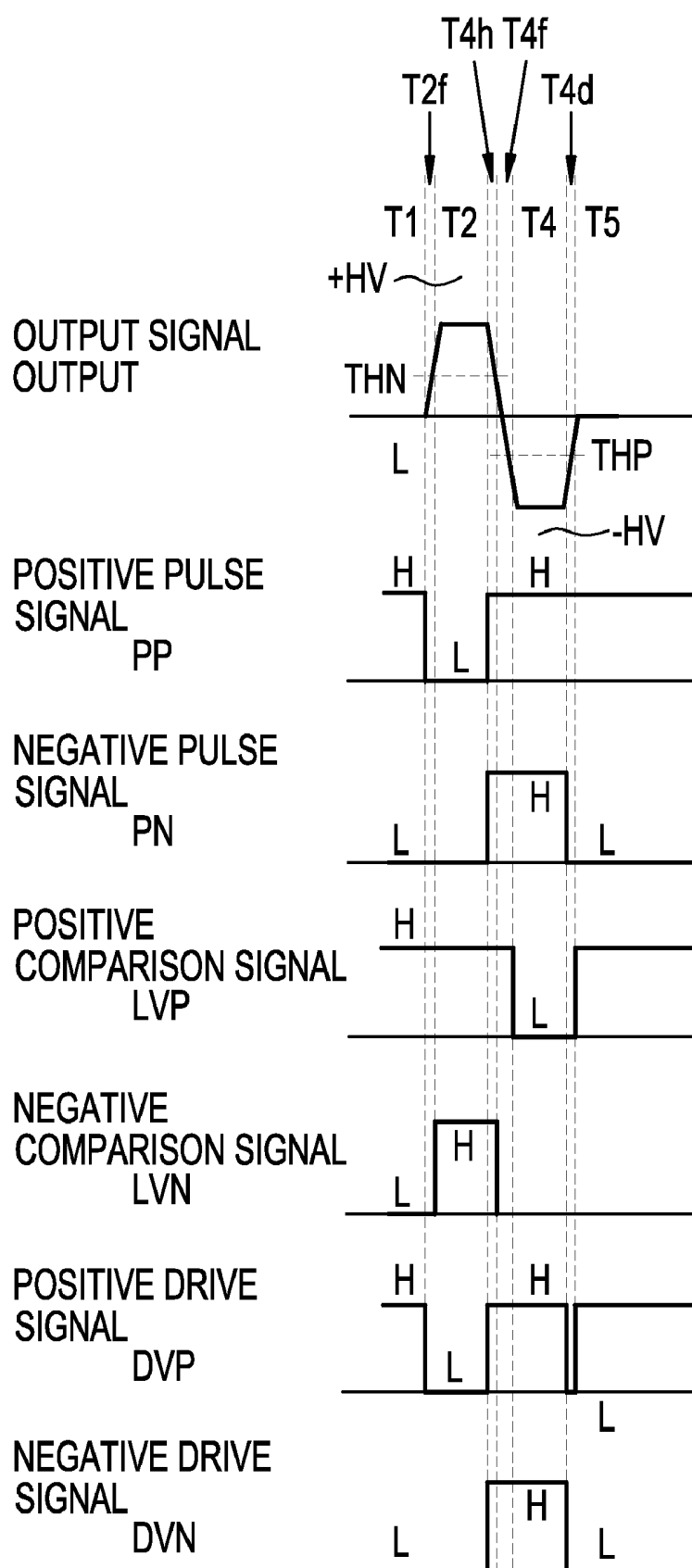


FIG. 7

	PP	PN	LVP	LVN	DVP	DVN
T1	H	L	H	L	H	L
T2f	L	L	H	L	L	L
T2	L	L	H	H	L	L
T4h	H	H	H	H	H	H
T4f	H	H	H	L	H	H
T4	H	H	L	L	H	H
T4d	H	L	L	L	L	L
T5	H	L	H	L	H	L

ULTRASONIC TRANSDUCER DRIVING CIRCUIT AND ULTRASONIC DIAGNOSTIC APPARATUS

BACKGROUND OF THE INVENTION

[0001] The present invention relates to an ultrasonic transducer driving circuit and an ultrasonic diagnostic apparatus and, more particularly, relates to an ultrasonic transducer driving circuit and an ultrasonic diagnostic apparatus that make it possible to quickly return, from a positive voltage or negative voltage to a ground voltage, the voltage of an output line which outputs the positive voltage or the negative voltage or the ground voltage to an ultrasonic transducer, and that allow for a reduction in circuit size.

[0002] Heretofore, there is known an ultrasonic diagnostic apparatus including a positive FET (Field Effect Transistor) which outputs a positive voltage onto an output line to an ultrasonic transducer at on state, a negative FET which outputs a negative voltage onto the output line to the ultrasonic transducer at on state, and a driver circuit which turns the positive FET and the negative FET on/off (e.g., see Patent Document 1 and Patent Document 2).

[0003] [Patent Document 1] Japanese Unexamined Patent Publication No. 2006-101997 (FIG. 10, FIG. 12, FIG. 14)

[0004] [Patent Document 2] Japanese Unexamined Patent Publication No. 2004-358133 (FIG. 2)

[0005] The above ultrasonic diagnostic apparatus of prior art has a problem in which, when a pulse of a positive voltage or negative voltage is applied to the output line, the voltage on the output line does not quickly return from the positive voltage or negative voltage to the ground voltage because of capacitance of the output line.

[0006] To address this, it is conceivable to incorporate an active ground clamp circuit that forcibly returns the output line to the ground voltage. However, a FET with a capacity of 1 A or more is needed in the active ground clamp circuit and this poses a problem that the circuit size becomes larger.

SUMMARY OF THE INVENTION

[0007] In a first aspect, the present invention provides an ultrasonic transducer driving circuit characterized by comprising a positive field effect transistor which outputs a positive voltage onto an output line to an ultrasonic transducer at on state, a negative field effect transistor which outputs a negative voltage onto the output line to the ultrasonic transducer at on state, and a driver circuit which carries out at least one of turning on of said negative field effect transistor for only a pull-back period allowing for said output line to return to the ground voltage immediately after turning on and turning off said positive field effect transistor in accordance with a positive pulse signal supplied, and turning on of said positive field effect transistor for only a pull-back period allowing for said output line to return to the ground voltage immediately after turning on and turning off said negative field effect transistor in accordance with a negative pulse signal supplied.

[0008] In the ultrasonic transducer driving circuit according to the above first aspect, immediately after turning on and turning off of the positive field effect transistor in accordance with the positive pulse signal, turning on of the negative field effect transistor for only the pull-back period occurs to forcibly return the output line to the ground voltage; thus, the voltage on the output line can quickly be

returned from the positive voltage to the ground voltage. Also, immediately after turning on and turning off of the negative field effect transistor in accordance with the negative pulse signal, turning on of the positive field effect transistor for only the pull-back period occurs to forcibly return the output line to the ground voltage; thus, the voltage on the output line can quickly be returned from the negative voltage to the ground voltage. Since the driver circuit is a logic circuit through which only little current flows, its circuit size can be made smaller as compared with an active ground clamp circuit.

[0009] In a second aspect, the present invention provides an ultrasonic transducer driving circuit characterized in that said driver circuit in the ultrasonic transducer driving circuit according to said first aspect drives the positive field effect transistor and the negative field effect transistor based on said positive pulse signal, said negative pulse signal, and a return voltage returned from said output line.

[0010] In the ultrasonic transducer driving circuit according to the above second aspect, the return voltage returned from the output line is used; thus, the pull-back period for returning the voltage on the output line from the positive voltage or negative voltage to the ground voltage can be determined properly.

[0011] In a third aspect, the present invention provides an ultrasonic transducer driving circuit characterized in that said driver circuit in the ultrasonic transducer driving circuit according to said second aspect comprises a positive driver circuit which drives said positive field effect transistor and a negative driver circuit which drives said negative field effect transistor.

[0012] In the ultrasonic transducer driving circuit according to the above third aspect, the positive driver circuit and the negative driver circuit are separate; thus, each respective logic circuit becomes easy to construct.

[0013] In a fourth aspect, the present invention provides an ultrasonic transducer driving circuit characterized in that said positive driver circuit in the ultrasonic transducer driving circuit according to said third aspect includes: a positive comparator which compares a positive threshold and said return voltage; and a positive logic circuit which outputs a drive signal based on said positive pulse signal, said negative pulse signal, and an output voltage of said positive comparator.

[0014] In the ultrasonic transducer driving circuit according to the above fourth aspect, the pull-back period can be adjusted by adjusting the positive threshold.

[0015] In a fifth aspect, the present invention provides an ultrasonic transducer driving circuit characterized in that said positive threshold in the ultrasonic transducer driving circuit according to said fourth aspect is a voltage depending on a negative transmit voltage.

[0016] In the ultrasonic transducer driving circuit according to the above fifth aspect, the pull-back period can be terminated slightly before returning from the negative voltage to the ground voltage, e.g., at 0% to 20% of the negative voltage; thus, a large overshoot can be prevented from occurring.

[0017] In a sixth aspect, the present invention provides an ultrasonic transducer driving circuit characterized in that said native driver circuit in the ultrasonic transducer driving circuit according to any of said third through fifth aspects includes: a negative comparator which compares a negative threshold with said return voltage; and a negative logic

circuit which outputs a drive signal based on said positive pulse signal, said negative pulse signal, and an output voltage of said negative comparator.

[0018] In the ultrasonic transducer driving circuit according to the above sixth aspect, the pull-back period can be adjusted by adjusting the negative threshold.

[0019] In a seventh aspect, the present invention provides an ultrasonic transducer driving circuit characterized in that said negative threshold in the ultrasonic transducer driving circuit according to said sixth aspect is a voltage depending on a positive transmit voltage.

[0020] In the ultrasonic transducer driving circuit according to the above seventh aspect, the pull-back period can be terminated slightly before returning from the positive voltage to the ground voltage, e.g., at 0% to 20% of the positive voltage; thus, a large overshoot can be prevented from occurring.

[0021] In an eighth aspect, the present invention provides an ultrasonic diagnostic apparatus characterized by comprising an ultrasonic probe, an ultrasonic transducer driving circuit according to any of said first through seventh aspects, a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal, an image generating means which generates an ultrasonic image based on said acoustic beam signal, and a display means which displays said ultrasonic image.

[0022] In the ultrasonic diagnostic apparatus according to the above eighth aspect, the size of the ultrasonic transducer driving circuit can be reduced.

[0023] According to the ultrasonic transducer driving circuit and the ultrasonic diagnostic apparatus of the present invention, the voltage on the output line can quickly be returned from the positive voltage or negative voltage to the ground voltage. Besides, the circuit size can be reduced.

[0024] The ultrasonic transducer driving circuit and the ultrasonic diagnostic apparatus of the present invention can be utilized to improve the performance of ultrasonic diagnostic apparatus and reduce the size thereof.

[0025] Further objects and advantages of the present invention will be apparent from the following description of the preferred embodiments of the invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. 1 is a block diagram showing an ultrasonic diagnostic apparatus relevant to Embodiment 1.

[0027] FIG. 2 is a circuit diagram showing an ultrasonic transducer driving circuit relevant to Embodiment 1.

[0028] FIG. 3 shows the true tables for a positive logic circuit and a negative logic circuit relevant to Embodiment 1.

[0029] FIG. 4 is a timing chart for a period in which a positive voltage is applied to an ultrasonic transducer, followed by a return to the ground voltage and application of a negative voltage.

[0030] FIG. 5 lists the logical values of the signals for each time phase in FIG. 4.

[0031] FIG. 6 is a timing chart for a period in which the positive voltage is applied to the ultrasonic transducer, followed by application of the negative voltage.

[0032] FIG. 7 lists the logical values of the signals for each time phase in FIG. 6.

DETAILED DESCRIPTION OF THE INVENTION

[0033] In the following, the present invention will be described in more detail by way of its embodiments that are shown in the drawings. These embodiments are not intended to limit the present invention.

Embodiment 1

[0034] FIG. 1 is a structural diagram showing an ultrasonic diagnostic apparatus 100 relevant to Embodiment 1.

[0035] This ultrasonic diagnostic apparatus 100 comprises an ultrasonic probe 1 within which multiple ultrasonic transducers E are installed to transmit ultrasonic pulses from the transducer into a specimen body and receives ultrasonic echoes from within the specimen body, a receiver unit 2 which generates and outputs an acoustic beam signal from the ultrasonic echoes, an image generating unit 3 which generates an ultrasonic image based on the acoustic beam signal, a display unit which displays the ultrasonic image, an ultrasonic transducer driving circuit 10 which drives the ultrasonic transducer E for transmitting the ultrasonic pulses, a pulser unit 5 which inputs a signal for transmission to the ultrasonic transducer driving circuit 10, a control unit which takes overall control of the apparatus, and an input unit 7 which is used for an operator to operate the apparatus.

[0036] FIG. 2 is a circuit diagram showing the ultrasonic transducer driving circuit 10 relevant to Embodiment 1.

[0037] The ultrasonic transducer driving circuit 10 comprises a positive FET 11P which outputs a positive voltage +HV onto an output line W to the ultrasonic transducer E at on state, a negative FET 11N which outputs a negative voltage -HV onto the output line W at on state, a positive driver circuit 12P which drives the positive FET 11P based on a positive pulse signal PP and a negative pulse signal supplied from the pulser unit 5 as well as a positive threshold THP and a return voltage Vo returned from the output line W, and a negative driver circuit 12N which drives the negative FET 11N based on the positive pulse signal PP and the negative pulse signal PN as well as a negative threshold THN and the return voltage Vo.

[0038] The positive threshold THP is a value in relation to the negative voltage -HV as a transmit voltage and is supplied from the pulser unit 5.

[0039] The negative threshold THN a value in relation to the positive voltage +HV as a transmit voltage and is supplied from the pulser unit 5.

[0040] The positive driver circuit 12P includes: a comparator 13P which outputs a positive comparison signal LVP being "H" when the return voltage Vo is higher than the positive threshold THP and "L" otherwise; and a positive logic circuit 14P which outputs a positive drive signal DVP based on the positive pulse signal PP, the negative pulse signal PN, and the positive comparison signal LVP.

[0041] The negative driver circuit 12N includes: a comparator 13N which outputs a negative comparison signal LVN being "H" when the return voltage Vo is higher than the negative threshold THN and "L" otherwise; and a negative logic circuit 14N which outputs a negative drive signal DVN based on the positive pulse signal PP, the negative pulse signal PN, and the positive comparison signal LVN.

[0042] A resistor R5 and a capacitor C5 which are shown in FIG. 2 are omissible.

[0043] FIG. 3 shows a true table listing logic values of the positive logic circuit 14P and a true table listing logic values of the negative logic circuit 14N.

[0044] "Xh" denotes that it is desirably "H" from a fail-safe perspective, although it may be either "H" or "L".

[0045] "Xl" denotes that it is desirably "L" from the fail-safe perspective, although it may be either "H" or "L".

[0046] FIG. 4 is a timing chart for a period in which the positive voltage +HV is applied to the ultrasonic transducer E, followed by a return to the ground voltage and application of the negative voltage -HV. FIG. 5 lists the logical values of the signals for each time phase.

[0047] When the positive drive signal DVP is "L", the positive FET 11P is in on state. When the negative drive signal DVN is "H", the negative FET 11N is in on state.

[0048] As can be seen from the positive drive signal DVP and the negative drive signal DVN, immediately after turning on and turning off of the positive FET 11P in accordance with the positive pulse signal PP, turning on of the negative FET 11N for only a short pull-back period T2d occurs, thereby quickly returning the output line L to the ground voltage. Also, immediately after turning on and turning off of the negative FET in accordance with the negative pulse signal PN, turning on of the positive FET 11P for only a short pull-back period T4d occurs, thereby quickly returning the output line L to the ground voltage.

[0049] FIG. 6 is a timing chart for a period in which the positive voltage +HV is applied to the ultrasonic transducer E, followed by application of the negative voltage -HV. FIG. 7 lists the logical values of the signals for each time phase.

[0050] As can be seen from the positive drive signal DVP and the negative drive signal DVN, immediately after turning on and turning off of the negative FET 11N in accordance with the negative pulse signal PN, turning on of the positive FET 11P for only a short pull-back period T4d occurs, thereby quickly returning the output line L to the ground voltage.

[0051] According to the ultrasonic transducer driving circuit 10 and the ultrasonic transducer driving circuit 100 of Embodiment 1, immediately after turning on and turning off of the positive FET 11P in accordance with the positive pulse signal PP, turning on of the negative FET 11N for only the pull-back period T2d occurs and, thus, the voltage on the output line W can quickly be returned from the positive voltage +HV to the ground voltage. Also, immediately after turning on and turning off of the negative FET 11N in accordance with the negative pulse signal PN, turning on of the positive FET 11P for only the pull-back period T4d occurs and, thus, the voltage on the output line W can quickly be returned from the negative voltage -HV to the ground voltage. Since the driver circuits 12P, 12N are logic circuits through which only little current flows, their circuit size can be made smaller as compared with an active ground clamp circuit.

Embodiment 2

[0052] The present invention can be applied in the same manner as for Embodiment 1, when the negative voltage -HV is applied to the ultrasonic transducer E, followed by a return to the ground voltage and application of the positive voltage +HV, and even when the negative voltage -HV is

applied to the ultrasonic transducer E, followed by application of the positive voltage +HV.

[0053] Many widely different embodiments of the invention may be configured without departing from the spirit and the scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

1. An ultrasonic transducer driving circuit comprising:
 - a positive field effect transistor which outputs a positive voltage onto an output line to an ultrasonic transducer at on state;
 - a negative field effect transistor which outputs a negative voltage onto the output line to the ultrasonic transducer at on state; and
 - a driver circuit which carries out at least one of turning on of said negative field effect transistor for only a pull-back period allowing for said output line to return to the ground voltage immediately after turning on and turning off said positive field effect transistor in accordance with a positive pulse signal supplied, and turning on of said positive field effect transistor for only a pull-back period allowing for said output line to return to the ground voltage immediately after turning on and turning off said negative field effect transistor in accordance with a negative pulse signal supplied.

2. The ultrasonic transducer driving circuit according to claim 1, wherein said driver circuit drives said positive field effect transistor and said negative field effect transistor based on said positive pulse signal, said negative pulse signal, and a return voltage returned from said output line.

3. The ultrasonic transducer driving circuit according to claim 2, wherein said driver circuit comprises a positive drive circuit which drives said positive field effect transistor and a negative drive circuit which drives said negative field effect transistor.

4. The ultrasonic transducer driving circuit according to claim 3, wherein said positive drive circuit includes: a positive comparator which compares a positive threshold and said return voltage; and a positive logic circuit which outputs a drive signal based on said positive pulse signal, said negative pulse signal, and an output voltage of said positive comparator.

5. The ultrasonic transducer driving circuit according to claim 4, wherein said positive threshold is a voltage depending on a negative transmit voltage.

6. The ultrasonic transducer driving circuit according to claim 3, wherein said negative drive circuit includes: a negative comparator which compares a negative threshold with said return voltage; and a negative logic circuit which outputs a drive signal based on said positive pulse signal, said negative pulse signal, and an output voltage of said negative comparator.

7. The ultrasonic transducer driving circuit according to claim 4, wherein said negative drive circuit includes: a negative comparator which compares a negative threshold with said return voltage; and a negative logic circuit which outputs a drive signal based on said positive pulse signal, said negative pulse signal, and an output voltage of said negative comparator.

8. The ultrasonic transducer driving circuit according to claim 5, wherein said negative drive circuit includes: a negative comparator which compares a negative threshold with said return voltage; and a negative logic circuit which

outputs a drive signal based on said positive pulse signal, said negative pulse signal, and an output voltage of said negative comparator.

9. The ultrasonic transducer driving circuit according to claim 6, wherein said negative threshold is a voltage depending on a positive transmit voltage.

10. The ultrasonic transducer driving circuit according to claim 7, wherein said negative threshold is a voltage depending on a positive transmit voltage.

11. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 1; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

12. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 2; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

13. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 3; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

14. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 4; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

15. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 5; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which

generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

16. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 6; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

17. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 7; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

18. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 8; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

19. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 9; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

20. An ultrasonic diagnostic apparatus comprising: an ultrasonic probe, an ultrasonic transducer driving circuit as recited in claim 10; a receiver circuit which receives echo signals acquired at said ultrasonic probe and outputs an acoustic beam signal; an image generating device which generates an ultrasonic image based on said acoustic beam signal; and a display device which displays said ultrasonic image.

* * * * *

专利名称(译)	超声换能器驱动电路和超声诊断设备		
公开(公告)号	US20080071171A1	公开(公告)日	2008-03-20
申请号	US11/854255	申请日	2007-09-12
[标]申请(专利权)人(译)	雨宫SHINICHI		
申请(专利权)人(译)	雨宫SHINICHI		
当前申请(专利权)人(译)	雨宫SHINICHI		
[标]发明人	AMEMIYA SHINICHI		
发明人	AMEMIYA, SHINICHI		
IPC分类号	A61B8/00 H01L41/09		
CPC分类号	G01S7/52023 H03K17/6874 H03K17/04206 G01S15/8909		
优先权	2006248830 2006-09-14 JP		
其他公开文献	US7777394		
外部链接	Espacenet USPTO		

摘要(译)

为了快速将输出线的电压从正电压或负电压恢复到超声换能器到接地电压并减小电路尺寸，在正负FET导通和关断之后立即按照正在脉冲信号中，负FET仅持续一个回拉期，允许输出线返回到地电压。而且，在根据负脉冲信号接通和关断负FET之后，正FET仅接通一个回拉时段，允许输出线返回到地电压。

