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(54) ULTRASONIC TRANSDUCERS IN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) WAFERS AND RELATED APPARATUS AND METHODS

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(57) **ABSTRACT**

Micromachined ultrasonic transducers formed in complementary metal oxide semiconductor (CMOS) wafers are described, as are methods of fabricating such devices. A metallization layer of a CMOS wafer may be removed by sacrificial release to create a cavity of an ultrasonic transducer. Remaining layers may form a membrane of the ultrasonic transducer.

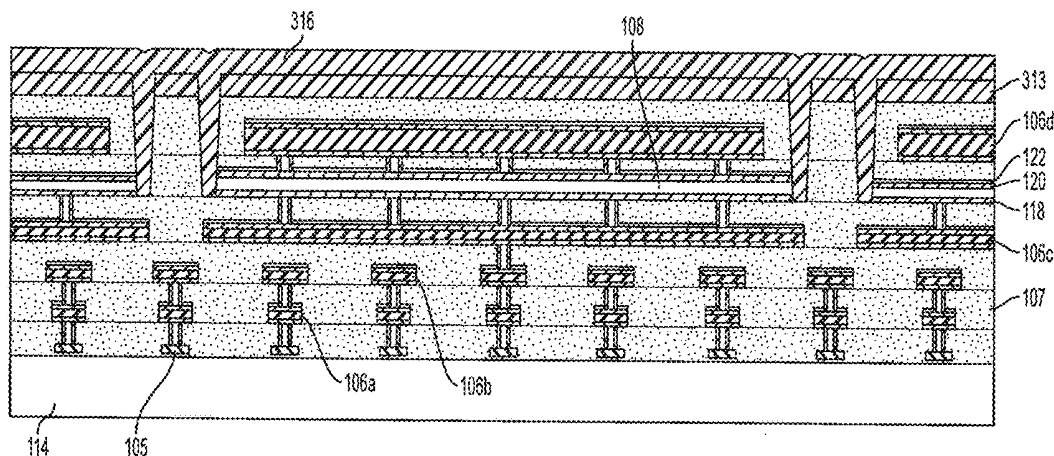

FIG. 1

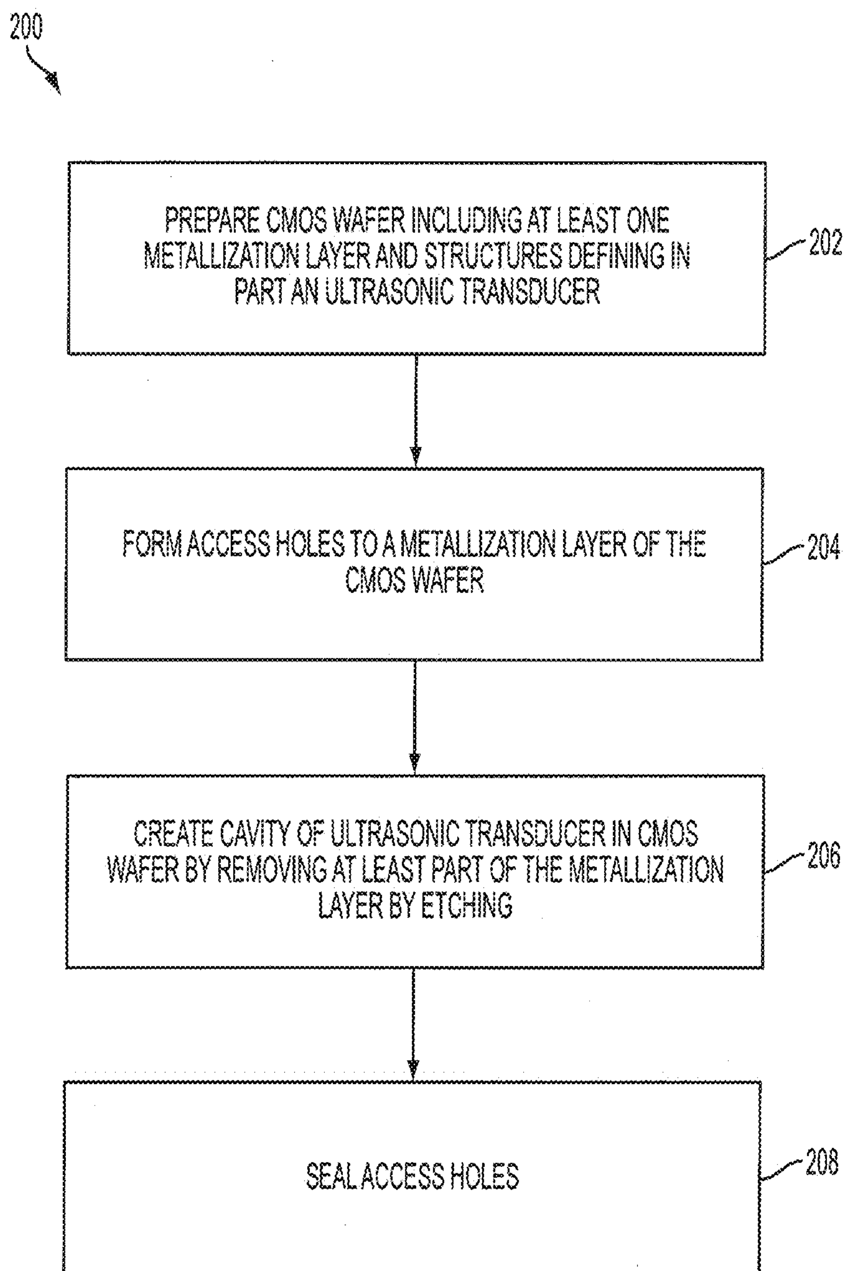

FIG. 2

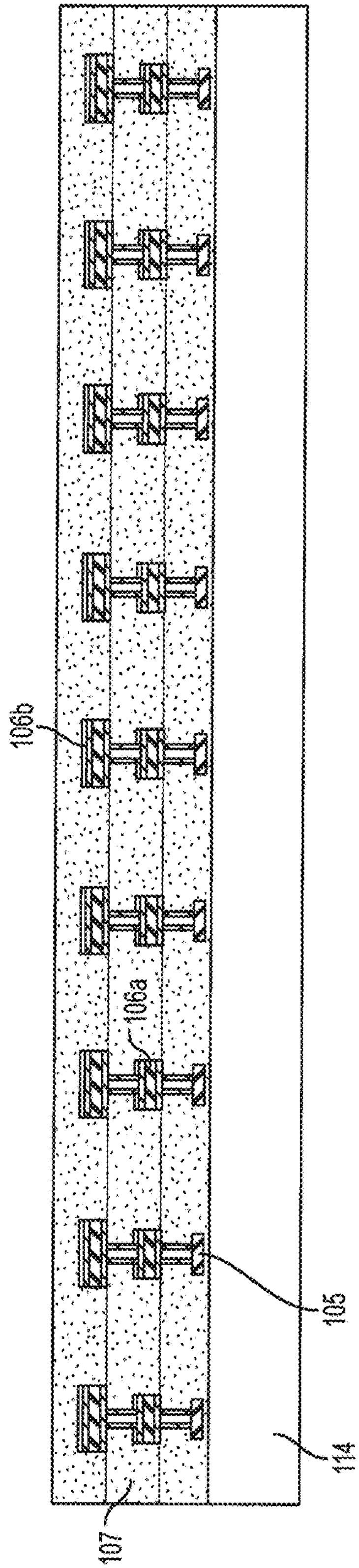

FIG. 3A

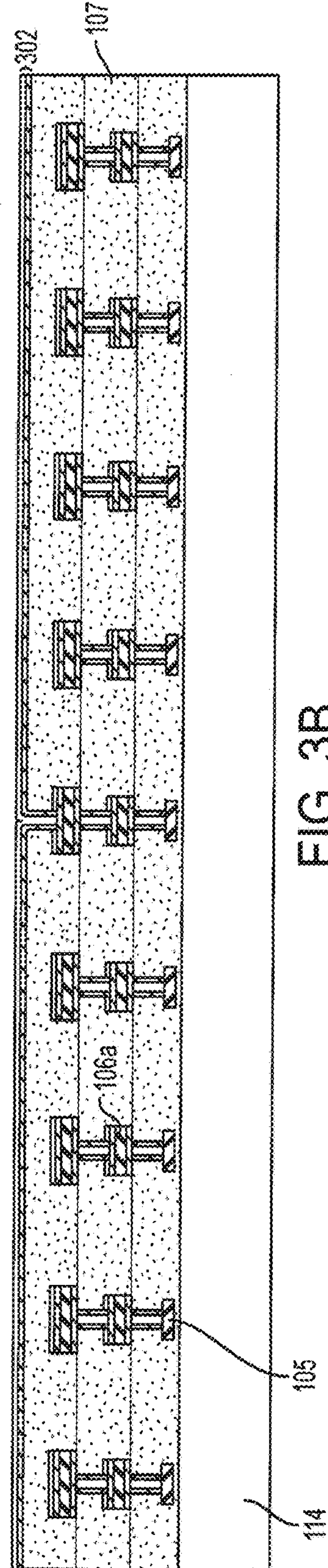

FIG. 3B

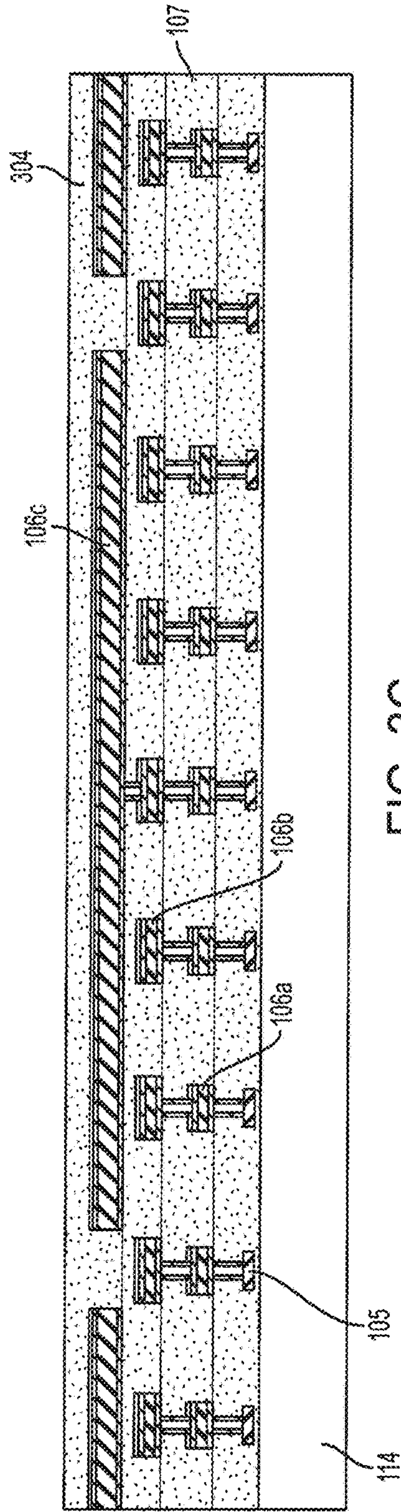

FIG. 3C

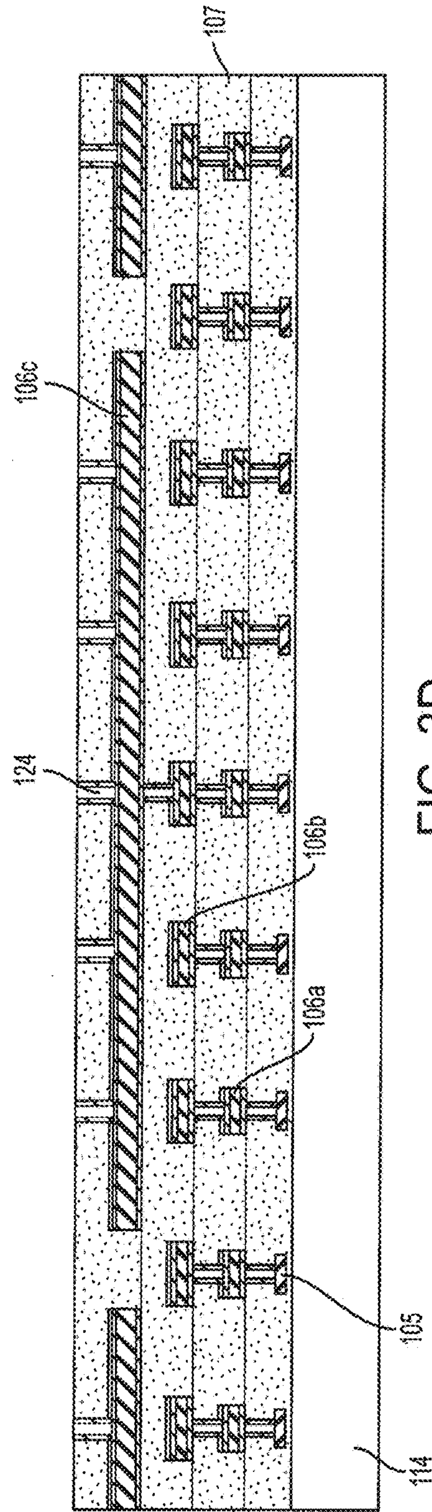

FIG. 3D

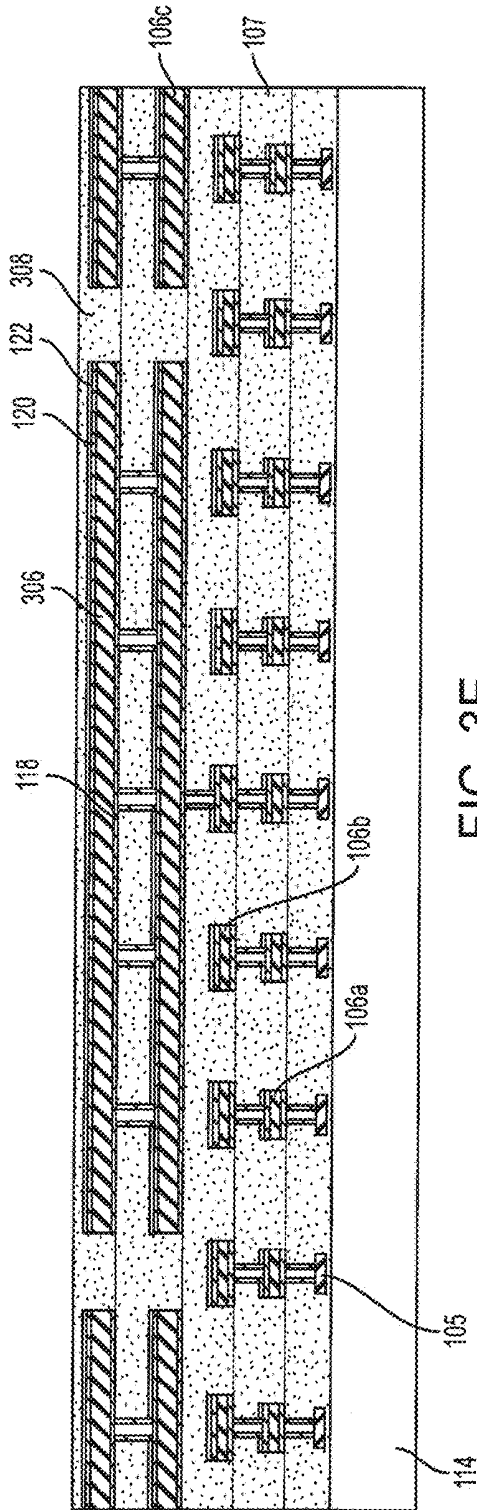

FIG. 3E

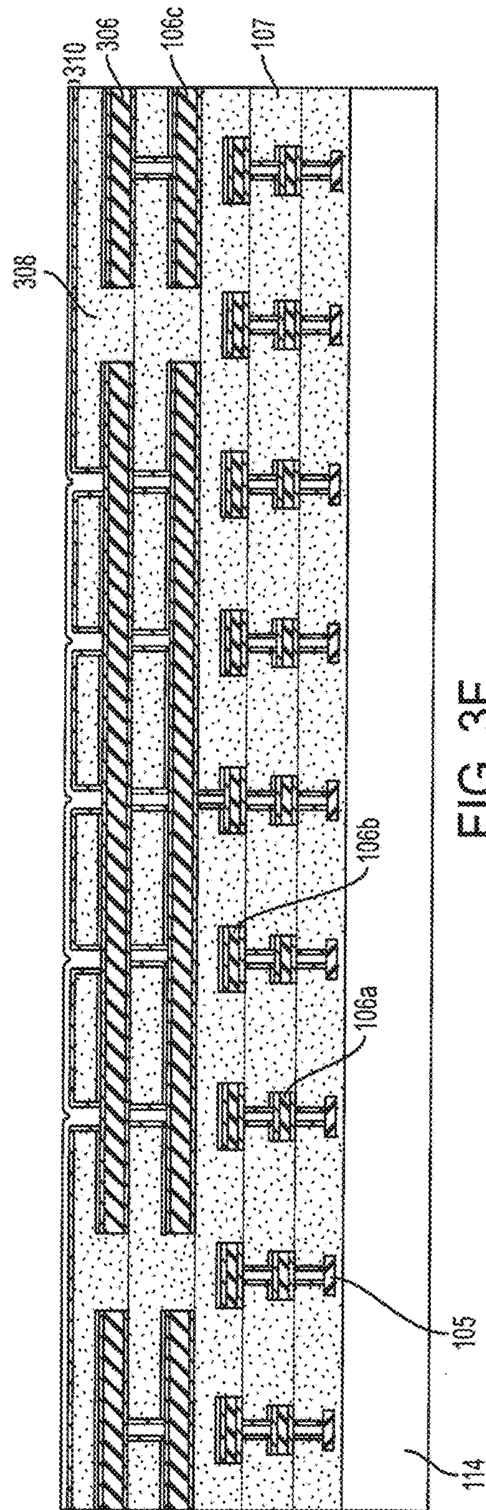

FIG. 3F

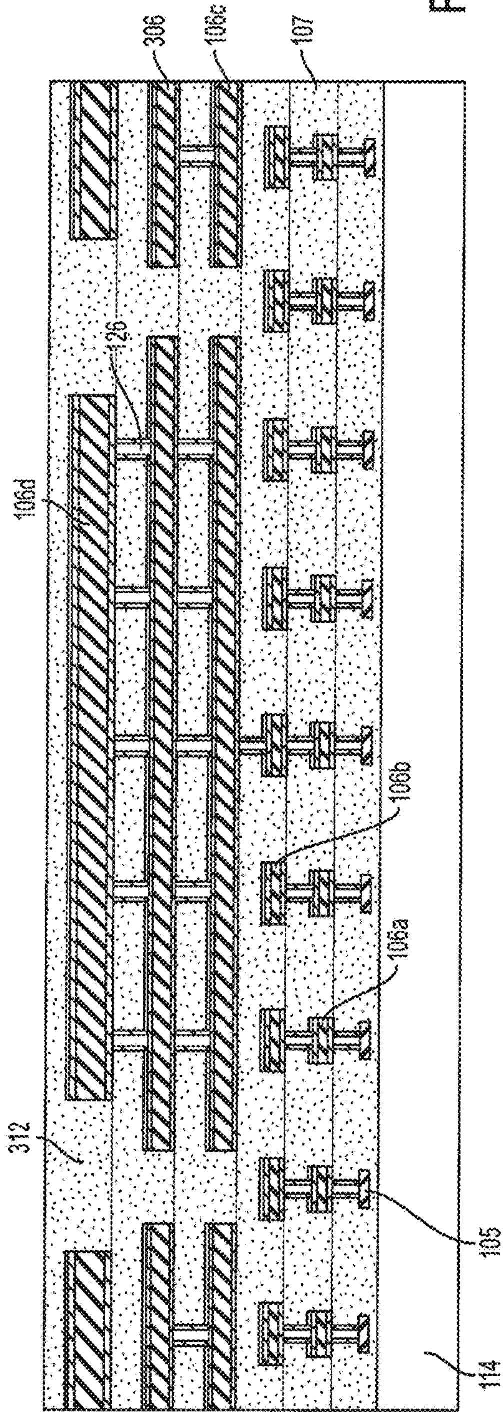

FIG. 3G

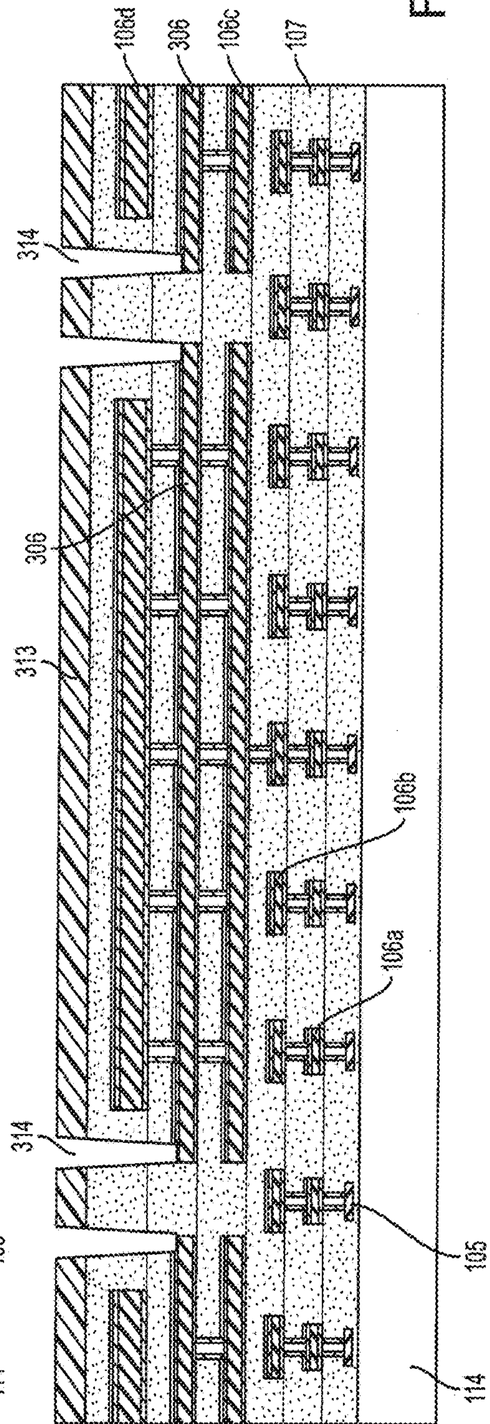

FIG. 3H

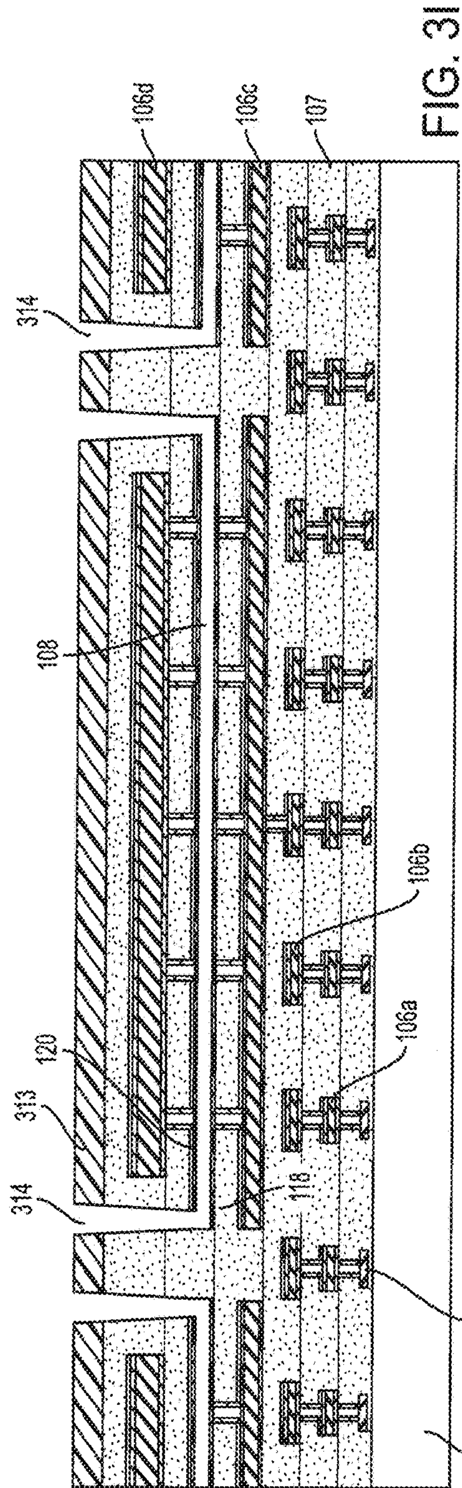
FIG. 3I
106d
106c
107
314
108
106b
106a
313
120
118
105
114

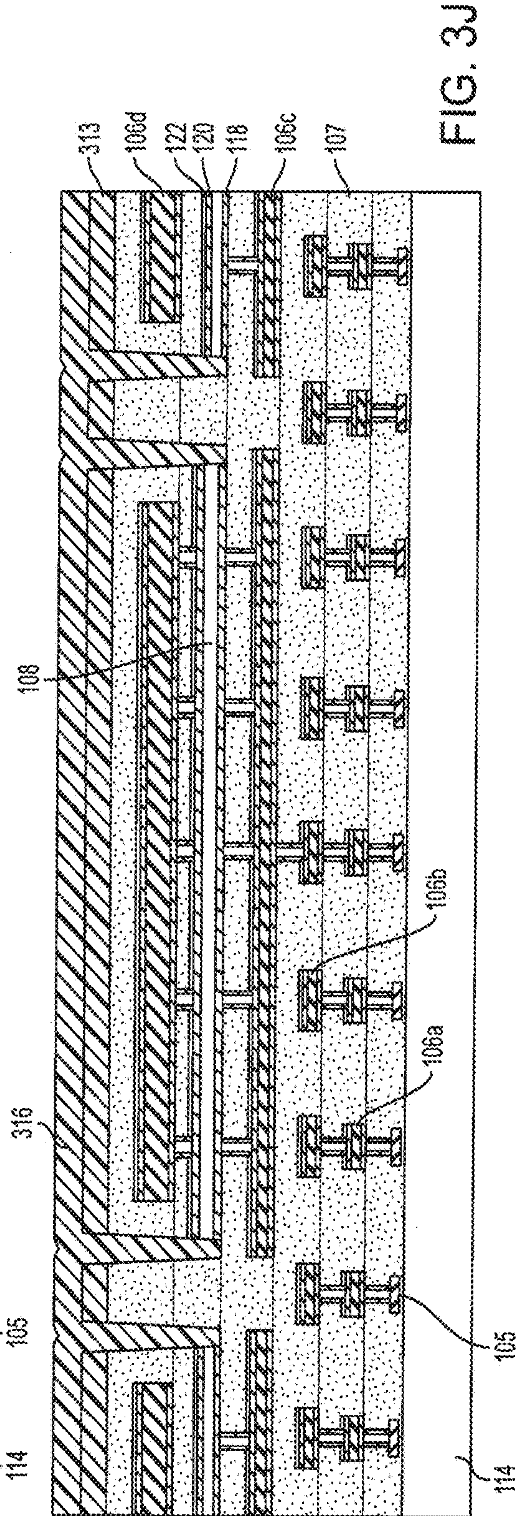
FIG. 3J
313
106d
122
120
118
106c
107
108
316
106b
106a
105
114

ULTRASONIC TRANSDUCERS IN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) WAFERS AND RELATED APPARATUS AND METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation claiming the benefit under 35 U.S.C. § 120 of U.S. patent application Ser. No. 15/865,774, filed Jan. 9, 2018 under Attorney Docket No. B1348.70010US03, and entitled "ULTRASONIC TRANSDUCERS IN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) WAFERS AND RELATED APPARATUS AND METHODS," which is hereby incorporated herein by reference in its entirety.

[0002] U.S. patent application Ser. No. 15/865,774 is a continuation claiming the benefit under 35 U.S.C. § 120 of U.S. patent application Ser. No. 15/259,243, filed Sep. 8, 2016 under Attorney Docket No. B1348.70010US02, and entitled "ULTRASONIC TRANSDUCERS IN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) WAFERS AND RELATED APPARATUS AND METHODS," which is hereby incorporated herein by reference in its entirety.

[0003] U.S. patent application Ser. No. 15/259,243 is a divisional claiming the benefit of U.S. patent application Ser. No. 14/689,119 entitled "ULTRASONIC TRANSDUCERS IN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) WAFERS AND RELATED APPARATUS AND METHODS," filed Apr. 17, 2015 under Attorney Docket No. B1348.70010US01, which is incorporated herein by reference in its entirety, and which claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Patent Application Ser. No. 61/981,464 entitled "ULTRASONIC TRANSDUCERS IN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) WAFERS AND RELATED APPARATUS AND METHODS," filed Apr. 18, 2014 under Attorney Docket No. B1348.70010US00, which is incorporated herein by reference in its entirety.

BACKGROUND

Field

[0004] The technology described herein relates to micromachined ultrasonic transducers and related apparatus and methods.

Related Art

[0005] Capacitive Micromachined Ultrasonic Transducers (CMUTs) are known devices that include a membrane above a micromachined cavity. The membrane may be used to transduce an acoustic signal into an electric signal, or vice versa. Thus, CMUTs can operate as ultrasonic transducers.

[0006] Two types of processes can be used to fabricate CMUTs. Sacrificial layer processes form the membrane of the CMUT on a substrate above a sacrificial layer which is then removed to form the cavity of the CMUT beneath the membrane. Wafer bonding processes bond two wafers together to form a cavity with a membrane.

SUMMARY

[0007] Aspects of the present technology provide micromachined ultrasonic transducers (e.g., CMUTs) in complementary metal oxide semiconductor (CMOS) wafers, utilizing a removed metallization of the CMOS wafer as an acoustic cavity for one or more micromachined ultrasonic transducers. Accordingly, the ultrasonic transducers may be integrated with the CMOS wafers and formed in the wafers, avoiding any requirement for wafer bonding to fabricate ultrasonic transducers. Integration of the ultrasonic transducers with the CMOS wafers may therefore be simplified and made more robust compared to if wafer bonding was used. Moreover, use of a removed CMOS metallization layer as the cavity of an ultrasonic transducer may facilitate formation of integrated circuits (ICs) on the CMOS wafer beneath the ultrasonic transducer, thus reducing or minimizing the space on the CMOS wafer needed to form integrated ultrasonic transducers and integrated circuits. As a result, compact complementary metal oxide semiconductor (CMOS) ultrasonic transducers (CUTs) having monolithically integrated ultrasonic transducers and CMOS ICs may be formed in accordance with some embodiments.

[0008] According to an aspect of the technology, a complementary metal oxide semiconductor (CMOS) wafer comprises a semiconductor substrate and an ultrasonic transducer. The ultrasonic transducer comprises a cavity representing a removed first metallization layer of the CMOS wafer, an electrode disposed between the cavity and the semiconductor substrate, and an acoustic membrane of the CMOS wafer comprising a dielectric layer and a second metallization layer of the CMOS wafer. The cavity may be disposed between the semiconductor substrate and the acoustic membrane. The CMOS wafer may further comprise integrated circuitry on the semiconductor substrate, coupled to the ultrasonic transducer and configured to control operation of the ultrasonic transducer.

[0009] According to an aspect of the present technology, an apparatus comprises an ultrasonic transducer in a complementary metal oxide semiconductor (CMOS) wafer for which a removed portion of a metallization layer defines at least part of an acoustic cavity of the ultrasonic transducer.

[0010] According to an aspect of the present technology, a complementary metal oxide semiconductor (CMOS) wafer comprises a semiconductor substrate, a first metallization layer, and an ultrasonic transducer. The ultrasonic transducer comprises a cavity formed in the first metallization layer, an electrode disposed between the cavity and the semiconductor substrate, and an acoustic membrane of the CMOS wafer comprising a dielectric layer and a second metallization layer of the CMOS wafer. The cavity may be disposed between the semiconductor substrate and the acoustic membrane. The CMOS wafer further comprises integrated circuitry on the semiconductor substrate, coupled to the ultrasonic transducer and configured to control operation of the ultrasonic transducer.

[0011] According to an aspect of the technology, a method comprises forming an acoustic membrane of an ultrasonic transducer in a complementary metal oxide semiconductor (CMOS) wafer by stacking multiple layers of the CMOS wafer including at least one dielectric layer and a first metallization layer of the CMOS wafer. The method further comprises creating at least one access hole to a second metallization layer of the CMOS wafer, the second metallization layer comprising an inner metal layer bounded by first and second conductive liner layers, which in some embodiments include a metal. The method further comprises forming a cavity in the CMOS wafer by removing at least a

portion of the inner metal layer of the first metallization layer through the at least one access hole using a selective etch, thereby releasing the acoustic membrane while substantially retaining the first and second conductive liner layers. The method further comprises sealing the at least one access hole with an insulating material, and coupling the first and second conductive liner layers to integrated circuitry of the CMOS wafer.

[0012] According to an aspect of the present application, a method comprises defining at least in part an acoustic cavity of an ultrasonic transducer in a complementary metal oxide semiconductor (CMOS) wafer by removing at least part of a metallization layer of the CMOS wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

[0014] FIG. **1** illustrates a capacitive micromachined ultrasonic transducer (CMUT) formed in a CMOS wafer and integrated with a CMOS IC to form a CUT, according to a non-limiting embodiment of the present application.

[0015] FIG. **2** is a flowchart illustrating a process of fabricating a CMUT in a CMOS wafer, according to a non-limiting embodiment of the present application.

[0016] FIGS. **3**A-**3**J illustrate a fabrication sequence for fabricating a CMUT in a CMOS wafer consistent with the process of FIG. **2**, according to a non-limiting embodiment of the present application.

DETAILED DESCRIPTION

[0017] Aspects of the present technology arise from Applicants' appreciation that certain feature dimensions of standard CMOS wafers substantially correspond to certain target feature dimensions of ultrasonic transducers for at least some applications, and thus that ultrasonic transducers may be fabricated in CMOS wafers by taking advantage of such correspondence. That is, Applicants have appreciated that at least some metallization layers of CMOS wafers have thicknesses substantially matching target cavity depths of ultrasonic transducers. Applicants have also appreciated that the thickness of layers of a CMOS wafer overlying the metallization layer substantially matches target membrane thicknesses of ultrasonic transducers. Thus, Applicants have appreciated that ultrasonic transducers may be fabricated in (and therefore integrated with) CMOS wafers by utilizing an appropriately dimensioned CMOS metallization layer as a sacrificial layer to be released to define the cavity of the ultrasonic transducer. Such fabrication provides a simple and robust manner of attaining a high degree of integration of an ultrasonic transducer with a CMOS wafer. Thus, aspects of the present application may facilitate formation of ultrasound system-on-a-chip devices having integrated ultrasonic transducers and circuitry.

[0018] Moreover, Applicants have appreciated that using a sacrificial CMOS metallization layer having appropriately situated liner layers may further simplify fabrication of an ultrasonic transducer in a CMOS wafer. By removing only the inner metal of the sacrificial CMOS metallization layer, the remaining liner layers may serve as electrodes for the ultrasonic transducer, obviating any need for further processing to create the electrodes. In this sense, the ultrasonic transducer electrodes are already "built in" to the CMOS metallization layer.

[0019] Accordingly, aspects of the present technology provide micromachined ultrasonic transducers (e.g., CMUTs) in CMOS wafers, utilizing a removed metallization of the CMOS wafer as an acoustic cavity for one or more micromachined ultrasonic transducers. The metallization may represent a signal line metallization for routing signals on the CMOS wafer, and portions of the metallization layer which do not need to be removed to form an acoustic cavity of an ultrasonic transducer may be retained on the CMOS wafer and configured as a signal line. The metallization layer may have a multi-layer configuration, including an inner metal and one or more liner layers. In some embodiments, the inner metal may be removed to form the acoustic cavity, while the liner layers may be retained and configured as electrodes of the ultrasonic transducer.

[0020] According to an aspect of the present technology, a sacrificial release technique is utilized to remove a CMOS metallization layer from a CMOS wafer to create an acoustic cavity of an ultrasonic transducer formed in the CMOS wafer. The metallization targeted with the sacrificial release may have a thickness substantially corresponding to a target depth of the acoustic cavity. In some embodiments, the ultrasonic transducer may be substantially completed prior to the sacrificial release being performed, such that the sacrificial release may complete (or nearly complete) formation of the ultrasonic transducer. Integrated circuitry may optionally be formed in the CMOS wafer beneath the ultrasonic transducer, and in some embodiments may be configured to control operation of the ultrasonic transducer.

[0021] The aspects and embodiments described above, as well as additional aspects and embodiments, are described further below. These aspects and/or embodiments may be used individually, all together, or in any combination of two or more, as the application is not limited in this respect.

[0022] According to an aspect of the present technology, a CMOS wafer includes one or more ultrasonic transducers formed therein, for which a partially or completely removed metallization layer of the CMOS wafer defines at least in part a cavity of the ultrasonic transducer(s). FIG. **1** illustrates a non-limiting example of such a device.

[0023] As shown, the device **100** includes a CMOS wafer **102**, with an ultrasonic transducer **104** formed in the CMOS wafer **102**. A single ultrasonic transducer **104** is illustrated, but it should be appreciated that aspects of the present application provide for a plurality of ultrasonic transducers in a CMOS wafer, and thus FIG. **1** is a non-limiting illustration. Such a configuration may facilitate formation of an ultrasound system-on-a-chip device or an ultrasound sub-system-on-a-chip device including integrated ultrasonic transducers and circuitry (e.g., analog and/or digital circuitry such as front-end and/or back-end circuitry for controlling operation of the ultrasonic transducers and/or processing signals produced by such transducers, for example to form and/or display ultrasound images). In at least some embodiments, an ultrasound system-on-a-chip device may include, on a single substrate, an arrangement of ultrasonic transducers integrated with analog and digital circuitry, and may be capable of performing ultrasound imaging functions such as emitting and receiving ultrasound waves and processing received ultrasound waves to produce ultrasound images.

[0024] The CMOS wafer **102** includes a polysilicon layer **105**, a plurality of metallization layers **106***a*-**106***d*, and a removed metallization layer defining at least in part an acoustic cavity **108** of the ultrasonic transducer **104**. A membrane **110** of the ultrasonic transducer **104** is formed of a combination of layers of the CMOS wafer **102** remaining above the cavity **108**. Integrated circuitry **112** may be formed in the base layer **114**, beneath the ultrasonic transducer **104**. The integrated circuitry may be CMOS circuitry and may be integrated with the ultrasonic transducer **104** to form a CUT. In the non-limiting example shown, the integrated circuitry is directly beneath the ultrasonic transducer **104**. The polysilicon layer **105** may form part of the integrated circuitry, for instance representing a gate layer for transistors. In some non-limiting embodiments high voltage wiring lines may be disposed above the cavity, but all circuitry may be positioned beneath the ultrasonic transducer.

[0025] The CMOS wafer **102** may be any suitable CMOS wafer for the formation of CMOS integrated circuitry and including one or more metallization layers. In the illustrated example, the CMOS wafer **102** includes five metallization layers (metallization layers **106***a*-**106***d* in addition to the removed metallization layer representing the cavity **108**), but other numbers may alternatively be used.

[0026] The metallization layers **106***a*-**106***d*, as well as the removed metallization layer used to form the cavity **108**, may be configured as standard CMOS metallization layers for signal routing. Thus, in at least some embodiments they may be substantially planar and may occupy an appropriate portion of a plane within the CMOS wafer for functioning as a signal routing layer. For example, in some embodiments one or more of the metallization layers may occupy substantially an entire plane within the CMOS wafer prior to patterning to define desired signal routing configurations. Moreover, the metallization layers may be formed of any suitable material(s). For example, aluminum (Al), copper (Cu), or other metals may be used.

[0027] In some embodiments, including that illustrated, one or more of the metallization layers may include multiple layers (i.e., a multi-layer configuration), such as an inner metal layer with lower and upper liner (or barrier) layers. In the example of FIG. **1**, each of the illustrated metallization layers includes a bottom liner layer (e.g., of titanium nitride (TiN)), a layer of Al, a top liner layer (e.g., of TiN), and a layer of silicon oxynitride (SiON) above the top liner layer to serve as an anti-reflective coating during lithography stages. A multi-layer structure for the metallization which is to be sacrificially removed may be beneficial because the liner layers may be configured and retained as electrodes of the ultrasonic transducer. In this manner, the electrodes of the ultrasonic transducer are formed simply and robustly when initially forming the metallization layer that is to be sacrificially removed. The cavity **108** may be formed by removing only the inner metal layer of the metallization while leaving behind the liner layers. Such selective removal may be achieved using a suitably selective etch process, such as a selective wet etch that is selective for (i.e., etches) the inner metal material of the metallization and which is non-selective for (i.e., does not etch) the material of the liner layers. In this manner, fabrication of the cavity is also simplified in that a timed etch is not needed to obtain the desired cavity dimensions. In some embodiments, the etch may be a hydrofluoric acid (HF) etch, although alternatives are possible.

[0028] For example, referring to device **100**, the cavity **108** is bounded on the bottom by layer **118** and on the top by layers **120** and **122**. The layer **118** may represent a bottom liner layer (e.g., of TiN) of the metallization layer, an internal part of which is partially removed to define the cavity **108**. The layer **120** may represent a top liner layer (e.g., of TiN) of the removed metallization layer. The layer **122** may represent an anti-reflective coating of the removed metallization layer. Layers **118** and **120** may be configured as electrodes of the ultrasonic transducer **104**. Electric connection to the electrodes (for example by one or more remaining metallization layers of the CMOS wafer) may be made by one or more conductive lines (e.g., vias), such as vias **124** and **126**, or in any other suitable manner.

[0029] In some embodiments, a multi-layer metallization layer may be configured with an insulating membrane when an inner metal material is removed. For example, the metallization layer may including, in order, TiN-aluminum oxide-Al-aluminum oxide-TiN—SiON, such that when the aluminum is removed an insulating membrane is formed over the TiN electrodes.

[0030] In at least some embodiments, the metallization layer that is at least partially removed to form the cavity of an ultrasonic transducer is in fact not completely removed. In this sense, the removal may be local, rather than global. Portions of the metallization layer may be retained to function as signal lines in areas of the CMOS wafer other than where the acoustic cavity is formed, for example to carry signals of various types applicable to the device **100**, such as power, control signals, or sensed signals as non-limiting examples. That is, the same CMOS metallization layer may be used in one or more areas of the CMOS wafer as a signal line and may be removed in other areas of the CMOS wafer to define an acoustic cavity of one or more ultrasonic transducers. Such dual functionality is to be distinguished from depositing a metal on a CMOS wafer solely for the purpose of using the metal as a sacrificial layer.

[0031] FIG. **1** also illustrates that the CMOS wafer **102** includes suitable dielectric or insulating layers between the metallization layers, such as layers **107**. These may be formed of any suitable material (e.g., non-conducting, such as SiO_2) and with any suitable thicknesses.

[0032] Sealed access holes **116** are also included. One or more access holes may be formed by suitable etching (e.g., a directional etch, such as a reactive ion etch) to access the metallization layer that is removed to form the cavity **108**. The metal material of the metallization layer may be removed through the one or more access holes, for example by selective wet etching (e.g., by HF etch). Subsequently, the access holes may be sealed to create a sealed cavity, as shown, which may be a vacuum cavity in some embodiments, although non-vacuum cavities may also be formed. Any suitable sealant material may be used, a non-limiting example of which is Si_3N_4.

[0033] FIG. **1** illustrates two access holes for the cavity **108**. However, it should be appreciated that other numbers (any one or more) may be used. The access holes may be positioned at any suitable location(s) relative to the cavity (e.g., at a periphery as shown, centrally, at both a periphery and a center, etc.) to allow for sufficient removal of the metal material of the metallization layer to create the cavity. Also,

holes may optionally be etched and then optionally filled around the borders of the cavity to provide isolation (e.g., acoustic isolation) between transducers or groups of transducers. In such embodiments, the holes may not pass through the membrane **110** but may optionally extend to the cavity **108**.

[0034] In some embodiments, a plurality of access holes may be positioned suitably to allow removal of the metal material of the metallization layer while also being arranged suitably to allow metal signal connections to run across the chip (e.g., between neighboring ultrasonic transducers). As a specific, but non-limiting, example, a plurality of access holes may be arranged at the periphery of a cavity but there may be enough space between at least two of the access holes to allow metal signal lines to interconnect the metallization layers **106***d* of neighboring ultrasonic transducers. Considering a top view of such a configuration, the cavity may have a circular shape and the plurality of access holes may be formed around the perimeter in a circle, with metal signal lines running between some of the access holes. Alternatives are possible. For example, the described circular cavity shape may alternatively be rectangular, square, hexagonal, or have any other suitable shape.

[0035] The ultrasonic transducer **104** may have any suitable dimensions. The dimensions may be dictated at least in part by an intended application for the transducer, for example to provide desired frequency behavior, desired device size, desired imaging aperture, or other characteristics of interest. Non-limiting examples are provided below.

[0036] In some embodiments, the cavity dimensions and/or the membrane thickness of any membrane overlying the cavity may impact the frequency behavior of the membrane, and thus may be selected to provide a desired frequency behavior (e.g., a desired resonance frequency of the membrane). For example, it may be desired in some embodiments to have an ultrasonic transducer with a center resonance frequency of between approximately 20 kHz and approximately 200 MHz, between approximately 1 MHz and approximately 40 MHz, between approximately 1 MHz and approximately 10 MHz, between approximately 2 MHz and approximately 5 MHz, between approximately 5 MHz and approximately 15 MHz, between approximately 10 MHz and approximately 20 MHz, between approximately 20 MHz and approximately 40 MHz, between approximately 50 kHz and approximately 200 kHz, of approximately 2.5 MHz, approximately 4 MHz, any frequency or range of frequencies in between, or any other suitable frequency. For example, it may be desired to use the devices in air, gas, water, or other environments, for example for medical imaging, materials analysis, or for other reasons for which various frequencies of operation may be desired. The dimensions of the cavity and/or membrane may be selected accordingly.

[0037] As non-limiting examples, the width W**1** of the cavity **108** may be between approximately 5 microns and approximately 500 microns, between approximately 20 microns and approximately 100 microns, may be approximately 30 microns, approximately 40 microns, approximately 50 microns, any width or range of widths in between, or any other suitable width. In some embodiments, the width may be selected to maximize the void fraction, i.e., the amount of area consumed by the cavity compared to the amount of area consumed by surrounding structures. The width dimension may also be used to identify the aperture size of the cavity, and thus the cavities may have apertures of any of the values described above or any other suitable values.

[0038] The cavity **108** may have a depth D**1**, which may be between approximately 0.05 microns and approximately 10 microns, between approximately 0.1 microns and approximately 5 microns, between approximately 0.5 microns and approximately 1.5 microns, any depth or range of depths in between, or any other suitable depth. As previously described, Applicants have appreciated that the thickness of some metallization layers used in standard CMOS wafers may substantially correspond to target depths of the acoustic cavity, and thus the depth of the cavity **108** may be defined at least in part by the thickness of the metallization layer used as the sacrificial layer. For instance, in one embodiment the depth D**1** may be approximately ¼ micron, which may substantially correspond to a metallization thickness offered on CMOS wafers.

[0039] The membrane **110** may comprise one or more layers and/or structures of the CMOS wafer **102** defining a thickness Tm. In the non-limiting example of FIG. **1**, the membrane **110** includes vias (e.g., vias **126**), metal layers (e.g., metallization layer **106***d*), and dielectric or insulating layers (e.g., layers **107**). A passivation layer **128** (e.g., formed of Si_3N_4) passivates the surface. The thickness Tm (e.g., as measured in the direction generally parallel to the depth D**1**) may be less than 100 microns, less than 50 microns, less than 40 microns, less than 30 microns, less than 20 microns, less than 10 microns, less than 5 microns, less than 1 micron, less than 0.1 microns, any range of thicknesses in between (e.g., between approximately 1-5 microns, between approximately 1-2 microns, etc.), or any other suitable thickness. The thickness may be selected in some embodiments based on a desired acoustic behavior of the membrane, such as a desired resonance frequency of the membrane. Moreover, Applicants have appreciated that for some standard CMOS wafers, using the metallization layer beneath the top metallization layer as the sacrificial layer for defining the ultrasonic transducer cavity results in the overlying membrane **110** having approximately (and in some cases, substantially) the target thickness for the ultrasonic transducer (e.g., between approximately 1-2 microns). Thus, use of the metallization layer beneath the top metallization layer as the sacrificial layer can significantly simplify fabrication of the ultrasonic transducers in the CMOS wafer.

[0040] The thickness Tm may be adjusted by adding/removing material from the upper surface of the membrane. Removal of such material may be accomplished using chemical mechanical polishing (CMP), any form of etching including selective etch, directional etch, wet etch, or laser etch, or any other suitable technique. Furthermore, in some embodiments, the membrane may have a non-uniform thickness, for example being thicker in a center portion over the cavity and thinner above the periphery of the cavity, to form a piston structure. Such structures may provide control over the operating frequency of the ultrasonic transducer.

[0041] As a non-limiting example of suitable dimensions of the cavity depth and width and the membrane thickness, in one embodiment the depth D**1** may be approximately ¼ micron, the width W**1** may be approximately 50 microns, and the thickness Tm of the membrane **110** may be approximately 1-2 microns. Alternatives are possible.

[0042] The integrated circuit **112** may be formed in the base layer **114** of the CMOS wafer **102**. For example, the

base layer **114** may be a bulk silicon layer or other semiconductor substrate, and the integrated circuit **112** may include one or more active silicon circuit elements (e.g., MOS transistors having doped source and drain regions in the silicon), capacitors, resistors, or other circuit components. The integrated circuit **112** may be suitable to operate the ultrasonic transducer **104** in transmit and/or receive modes.

[0043] As shown, the ultrasonic transducer **104** may be connected to the IC **112**, for example by the illustrated connection of the layer **118** to the via **124**. Other manners of making connection are possible.

[0044] According to an aspect of the present technology, a method of fabricating an ultrasonic transducer in a CMOS wafer is provided, involving removing at least a portion of a metallization layer of the CMOS wafer to create a cavity of the ultrasonic transducer. FIG. **2** is a flowchart illustrating an example of the method.

[0045] The method **200** includes, at stage **202**, preparation of a CMOS wafer. The CMOS wafer includes at least one metallization layer and structures defining in part an ultrasonic transducer. For example, electrodes and an acoustic membrane may be formed, such as electrodes defined by metallization liner layers and an acoustic membrane of the type represented by acoustic membrane **110** of FIG. **1**.

[0046] At stage **204** one or more access holes are formed to a metallization layer of the CMOS wafer. As previously described in connection with FIG. **1**, the access holes may be created in any suitable manner (e.g., a directional etch) and may be positioned at any suitable location(s) relative to the ultrasonic transducer, including at a periphery and/or center of the area which is to become the cavity of the ultrasonic transducer.

[0047] At stage **206**, the cavity of the ultrasonic transducer may be created in the CMOS wafer by removing at least part of the metallization layer using a suitable etch technique. For example, a selective etch may be used that is selective for the material (e.g., metal) of the metallization layer to be removed. The removal may be local in some embodiments, but not global. That is, the metallization layer may be removed in the area of the CMOS wafer in which the ultrasonic transducer is located, but may be retained in other areas of the CMOS wafer, for example as a signal line.

[0048] At stage **208**, the access holes formed in stage **204** may be sealed, to create a sealed ultrasonic transducer cavity. The access holes may be sealed in any suitable manner using any suitable material, such as an insulating material. In some embodiments, a plasma enhanced chemical vapor deposition (PECVD) may be performed to seal the access holes. For example, PECVD Si_3N_4 may be used in some embodiments, which may minimize lateral intrusion of the sealing material into the cavity.

[0049] The method **200** may be performed at the wafer level, as should be appreciated by the reference to a CMOS wafer throughout FIG. **2**. Thus, multiple ultrasonic transducers may be formed in the CMOS wafer, in arrays or other arrangements. One benefit of such a fabrication technique is that large numbers of ultrasonic transducers (e.g., CMUTs) may be formed on a single wafer in a relatively simple, cost-effective manner. Such technology may therefore facilitate fabrication of ultrasound system-on-a-chip devices utilizing arrays (or other arrangements) of micromachined ultrasonic transducers.

[0050] It should be appreciated that the stages of method **200** may be performed by different parties in some embodiments. For example, one party in the business of fabricating CMOS wafers may perform stage **202**. A second party (e.g., a purchaser of the CMOS wafer) may then perform stages **204**, **206**, and **208**. In other embodiments, a single entity may perform all stages of the method.

[0051] FIGS. **3**A-**3**J illustrate a fabrication sequence for fabricating a CMUT in a CMOS wafer consistent with the process of FIG. **2**, according to a non-limiting embodiment of the present application. The starting point for the sequence is shown in FIG. **3**A, and includes the base layer **114**, patterned polysilicon layer **105**, metallization layer **106***a*, and metallization layer **106***b*, with layers **107**.

[0052] As shown in FIGS. **3**B-**3**D, the via **124** of FIG. **1** (shown completed below in FIG. **3**D) may be formed. In anticipation of forming the via, as shown in FIG. **3**B, the uppermost layer **107** may be suitably etched and a conductive layer **302** may be deposited. The conductive layer **302** may be formed of a desired via material, such as tungsten (W). A liner material (e.g., TiN) may be deposited prior to the tungsten, and thus the conductive layer **302** may have a multi-layer configuration as shown.

[0053] As shown in FIG. **3**C, the conductive layer **302** may be planarized (e.g., using CMP), and then metallization layer **106***c* may be formed and patterned. A dielectric or insulating layer **304** (e.g., SiO_2) may be formed over the surface.

[0054] As shown in FIG. **3**D, the dielectric layer **304** may be patterned to allow formation of vias **124**. The vias **124** may be formed of a desired via material, such as tungsten (W). A liner material (e.g., TiN) may be deposited prior to the tungsten, giving rise to the multi-layer features of vias **124** illustrated.

[0055] Then, in FIG. **3**E, a metallization layer **306** is formed. The metallization layer **306** may represent the sacrificial metallization layer from which the cavity **108** of FIG. **1** (and also shown in FIG. **3**I) is to be formed. Thus, the previously described layers **118**, **120**, and **122** are included. A dielectric or insulating layer (e.g., SiO_2) **308** may be formed on the uppermost surface.

[0056] In FIG. **3**F the dielectric layer **308** may be patterned and a conductive layer **310** deposited in anticipation of forming vias **126** from FIG. **1** (also shown in FIG. **3**G). The conductive layer **310** may be formed of a desired via material, such as tungsten (W). A liner material (e.g., TiN) may be deposited prior to the tungsten, and thus the conductive layer **310** may have a multi-layer configuration as shown.

[0057] As shown in FIG. **3**G, the conductive layer **310** may be planarized to form vias **126** and metallization layer **106***d* may be formed and patterned. A dielectric or insulating layer **312** may be formed on the uppermost surface of the structure.

[0058] In FIG. **3**H a passivation layer (e.g., of Si_3N_4) **313** may be formed and access holes **314** may be formed to the metallization layer **306**. A suitable etch process may be used to form the access holes.

[0059] Then, as shown in FIG. **3**I, the cavity **108** may be created by removing at least a portion of the metallization layer **306** via the access holes **314**. For example, the metallization layer may include an inner metal layer which is selectively etched (for example by wet etch, such as HF etch), leaving behind the layers **118** and **120**.

[0060] In FIG. 3J the access holes 314 may be sealed with a suitable sealant layer 316. The sealant layer may comprise a passivating material, such as Si_3N_4 . Other materials are also possible. Thus, the device 100 of FIG. 1 may be achieved through this fabrication sequence.

[0061] While FIGS. 3A-3J illustrate a fabrication sequence suitable for use with aluminum metallization layers, it should be appreciated that the various aspects described herein are not limited in this respect. For example, aspects of the present technology may utilize copper metallization layers instead of aluminum. In some embodiments, copper lined with tantalum may be used.

[0062] Also, while aspects of the present application have been described as utilizing multi-layer metallization layers of CMOS wafers to define a cavity of an ultrasonic transducer, an alternative may utilize metal-insulator-metal (MIM) layers instead. For example, the insulator of a MIM layer may be removed from between adjacent metal layers in the manner described herein with respect to removing an inner metal material of a metallization layer.

[0063] Moreover, according to some embodiments, an ultrasonic transducer may be formed without metal liner layers configured as electrodes adjacent the cavity of the transducer. For example, referring to FIG. 1, in an alternative embodiment the layers 118 and 120 (and also 122) may be omitted, and instead the vias 126 may be disposed suitably to operate in combination as an electrode. For example, the vias 126 may be spaced relative to each other by between approximately 0.1 micron and approximately 0.5 microns (e.g., between approximately 0.2 microns and approximately 0.3 microns). An array of such vias may be operated in combination as an electrode for controlling operation of the ultrasonic transducer. In such embodiments, the vias may have any suitable dimensions, non-limiting examples of which are approximately 0.2 microns×0.2 microns in cross-section, approximately 0.3×microns 0.3 microns in cross-section, or any other suitable dimensions.

[0064] Aspects of the present application may be used to build ultrasound devices such as ultrasound probes. The probes may be suitable for imaging a variety of subjects. Ultrasound probes in accordance with some embodiments may include a variety of front-end and/or back-end electronics. In some embodiments, the probes may be ultrasound system-on-a-chip devices.

[0065] The aspects of the present application may provide one or more benefits, some of which have been previously described. Now described are some non-limiting examples of such benefits. It should be appreciated that not all aspects and embodiments necessarily provide all of the benefits now described. Further, it should be appreciated that aspects of the present application may provide additional benefits to those now described.

[0066] Aspects of the present application provide manufacturing processes suitable for formation of monolithically integrated ultrasonic transducers and CMOS structures (e.g., CMOS ICs). In at least some embodiments, the processes may be simple, robust, relatively inexpensive to perform, and may be scalable to large quantities of ultrasonic transducers. The difficulties associated with wafer bonding, such as poor bond strength, low yield, and the use of high temperature anneals may be avoided. Aspects of the present application provide processes for manufacturing suitably sized ultrasonic transducers for operation in connection with low voltage CMOS ICs. Other benefits may also be provided in accordance with one or more aspects of the present application.

[0067] Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the technology described in the application. For example, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the embodiments described herein. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described. In addition, any combination of two or more features, systems, articles, materials, kits, and/or methods described herein, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present disclosure.

[0068] Also, as described, some aspects may be embodied as one or more methods. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0069] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0070] The indefinite articles “a” and “an,” as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean “at least one.”

[0071] The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with “and/or” should be construed in the same fashion, i.e., “one or more” of the elements so conjoined. Elements other than those specifically identified by the “and/or” clause may optionally be present, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to “A and/or B”, when used in conjunction with open-ended language such as “comprising” can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

[0072] As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the

list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

[0073] Also, the phraseology and terminology used herein is for the purpose of description and should not be regarded as limiting. The use of "including," "comprising," or "having," "containing," "involving," and variations thereof herein, is meant to encompass the items listed thereafter and equivalents thereof as well as additional items.

[0074] In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively.

1. An ultrasound device, comprising:
- a complementary metal oxide semiconductor (CMOS) wafer comprising:
  - an integrated circuit having a transistor gate layer;
  - a plurality of metallization layers disposed above the transistor gate layer; and
  - an ultrasonic transducer formed in the plurality of metallization layers above the transistor gate layer, the ultrasonic transducer comprising:
    - a bottom electrode formed above a first of the plurality of metallization layers;
    - a cavity disposed above the bottom electrode; and
    - a top electrode disposed above the cavity and formed below a second of the plurality of metallization layers;
  - wherein the bottom electrode comprises a first plurality of vias disposed between the first of the plurality of metallization layers and the cavity, and the top electrode comprises a second plurality of vias disposed between the cavity and the second of the plurality of metallization layers.

2. The ultrasound device of claim **1**, wherein the first plurality of vias are spaced relative to each other by between approximately 0.1 microns and approximately 0.5 microns.

3. The ultrasound device of claim **1**, wherein the first plurality of vias are spaced relative to each other by between approximately 0.2 microns and approximately 0.3 microns.

4. The ultrasound device of claim **1**, wherein the second plurality of vias are spaced relative to each other by between approximately 0.1 microns and approximately 0.5 microns.

5. The ultrasound device of claim **1**, wherein the second plurality of vias are spaced relative to each other by between approximately 0.2 microns and approximately 0.3 microns.

6. The ultrasound device of claim **1**, wherein the first plurality of vias are each approximately 0.2 microns×0.2 microns in cross-section.

7. The ultrasound device of claim **1**, wherein the first plurality of vias are each approximately 0.3 microns×0.3 microns in cross-section.

8. The ultrasound device of claim **1**, wherein the second plurality of vias are each approximately 0.2 microns×0.2 microns in cross-section.

9. The ultrasound device of claim **1**, wherein the second plurality of vias are each approximately 0.3 microns×0.3 microns in cross-section.

10. The ultrasound device of claim **1**, further comprising a third and a fourth of the plurality of metallization layers disposed between the first of the plurality of metallization layers and the transistor gate layer.

11. The ultrasound device of claim **1**, wherein the integrated circuit is disposed directly beneath the ultrasonic transducer.

12. The ultrasound device of claim **1**, wherein the second of the plurality of metallization layers is a topmost metallization layer of the plurality of metallization layers, and no metallization layers are disposed between the cavity and the second of the plurality of metallization layers.

13. The ultrasound device of claim **1**, wherein the ultrasonic transducer further comprises an acoustic membrane that includes the top electrode and the second of the plurality of metallization layers.

14. The ultrasound device of claim **13**, wherein the acoustic membrane further comprises a dielectric layer in which the second of the plurality of metallization layers is disposed.

15. The ultrasound device of claim **13**, wherein the acoustic membrane further comprises:
- a first passivation layer disposed over the second of the plurality of metallization layers; and
- a second passivation layer disposed over the first passivation layer, the second passivation layer sealing access holes to the cavity.

16. The ultrasound device of claim **1**, wherein the cavity comprises a void of a third of the plurality of metallization layers.

17. The ultrasound device of claim **16**, wherein the ultrasonic transducer further comprises an acoustic membrane that includes:
- the top electrode;
- the second of the plurality of metallization layers;
- a first dielectric layer in which the third of the plurality of metallization layers is disposed; and
- a second dielectric layer in which the second of the plurality of metallization layers is disposed.

18. The ultrasound device of claim **1**, wherein the plurality of metallization layers are configured as CMOS metallization layers for signal routing.

19. The ultrasound device of claim **1**, further comprising sealed access holes to the cavity.

20. The ultrasound device of claim **20**, wherein the sealed access holes are formed around a perimeter of the cavity and the plurality of metallization layers run between the sealed access holes.

* * * * *

专利名称(译)	互补金属氧化物半导体（CMOS）晶片中的超声换能器和相关的装置和方法		
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[标]申请(专利权)人(译)	蝴蝶网络有限公司		
申请(专利权)人(译)	蝶形网络，INC.		
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CPC分类号	H01L27/0617 H01L27/092 H01L23/528 H01L23/5226 H01L21/76838 B81C1/00158 B06B1/02 H01L27/0688 B06B1/0292 H01L21/56 B81C1/00246 H01L21/32134 H01L21/823871 A61B8/4494 H01L21/768 A61B8/00 B81B3/0021 B81B7/0006 B81C2203/0771 B81B2201/0271 B81C2203/0735 H01L2224/16225 B06B2201/51		
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摘要(译)

描述了在互补金属氧化物半导体（CMOS）晶片中形成的微机械超声换能器，以及制造这种器件的方法。可以通过牺牲释放来去除CMOS晶片的金属化层，以产生超声换能器的腔。剩余的层可以形成超声换能器的膜。