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(54) **PIEZOELECTRIC MICROMACHINED ULTRASONIC TRANSDUCER (PMUT)**

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CPC ..... **G01S 7/521** (2013.01); **A61B 5/1172** (2013.01); **A61B 8/4483** (2013.01); **B06B 1/0622** (2013.01); **G01S 15/89** (2013.01); **H01L 41/047** (2013.01); **H01L 41/0973** (2013.01); **B06B 1/0688** (2013.01)

(58) **Field of Classification Search**

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See application file for complete search history.

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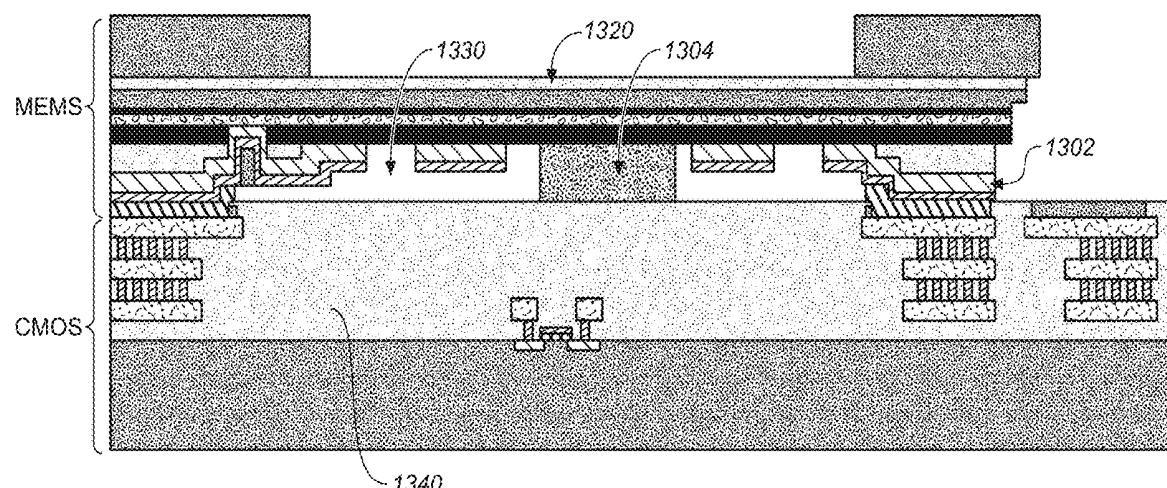
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(57) **ABSTRACT**

A Piezoelectric Micromachined Ultrasonic Transducer (PMUT) device is provided. The PMUT includes a substrate and an edge support structure connected to the substrate. A membrane is connected to the edge support structure such that a cavity is defined between the membrane and the substrate, where the membrane is configured to allow movement at ultrasonic frequencies. The membrane includes a piezoelectric layer and first and second electrodes coupled to opposing sides of the piezoelectric layer. An interior support structure is disposed within the cavity and connected to the substrate and the membrane.

**30 Claims, 8 Drawing Sheets**



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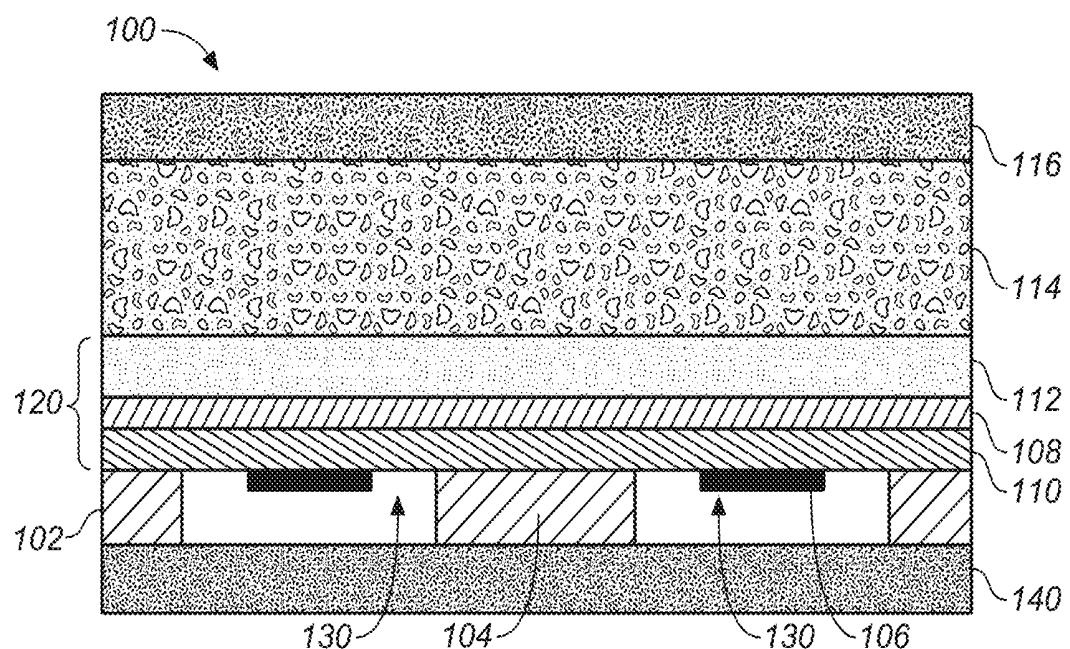
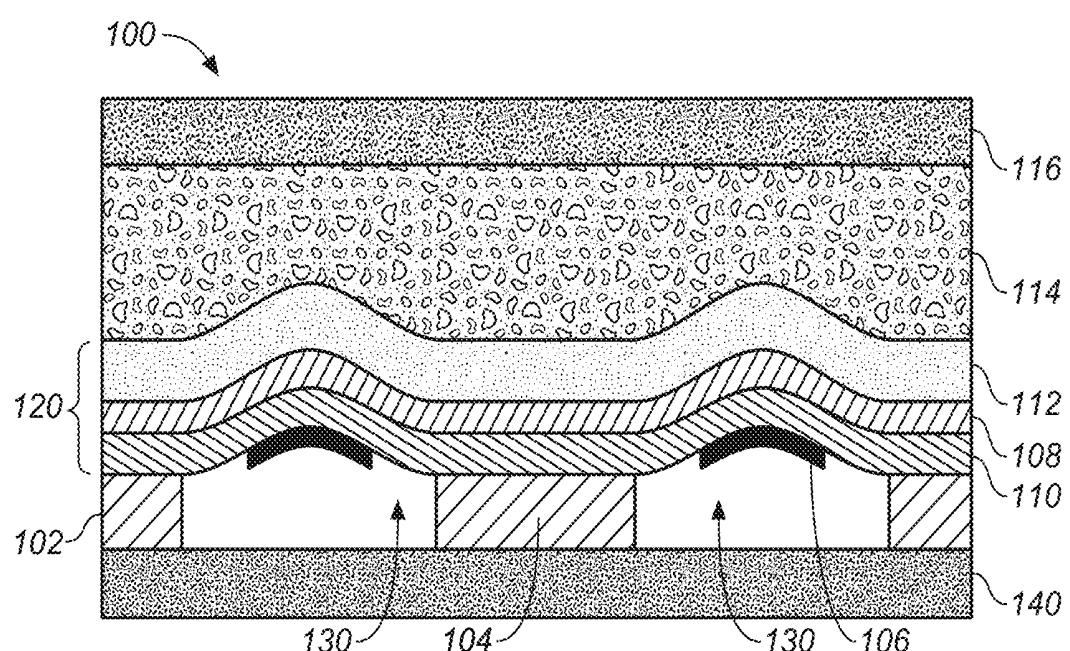
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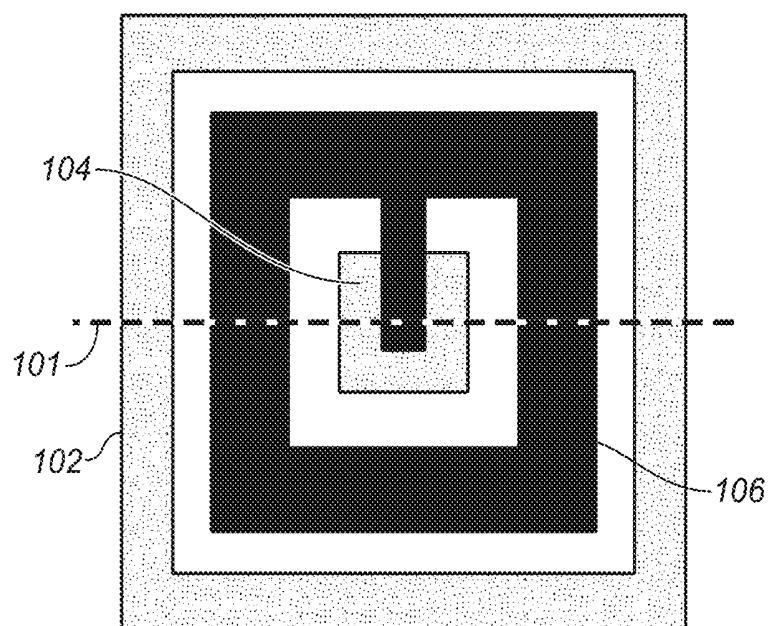
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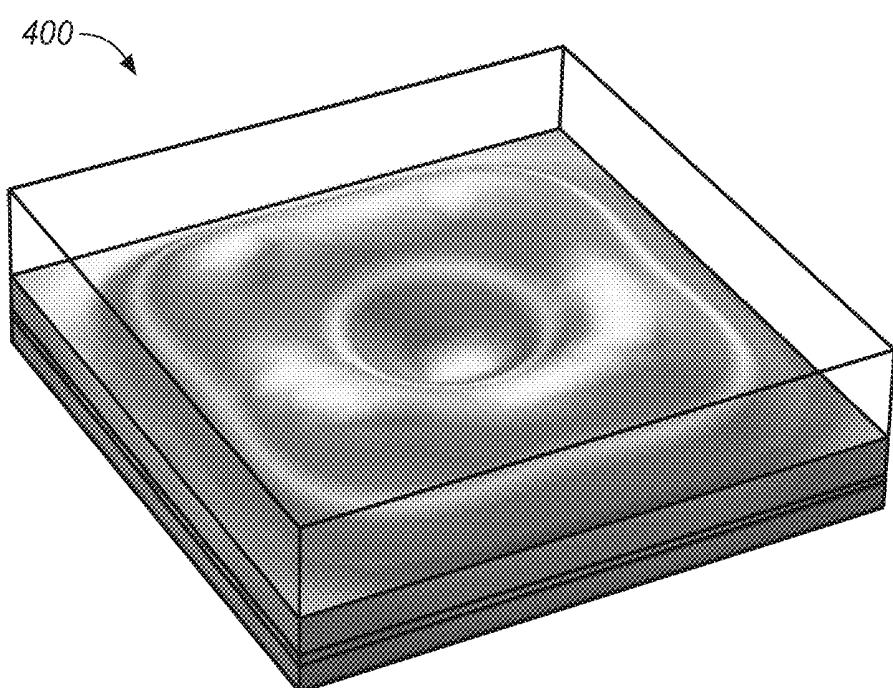
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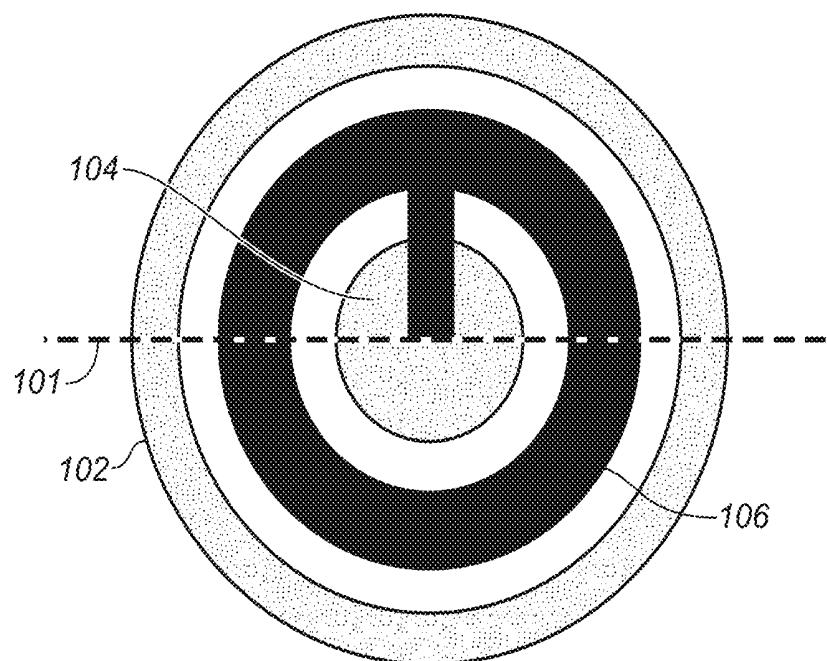
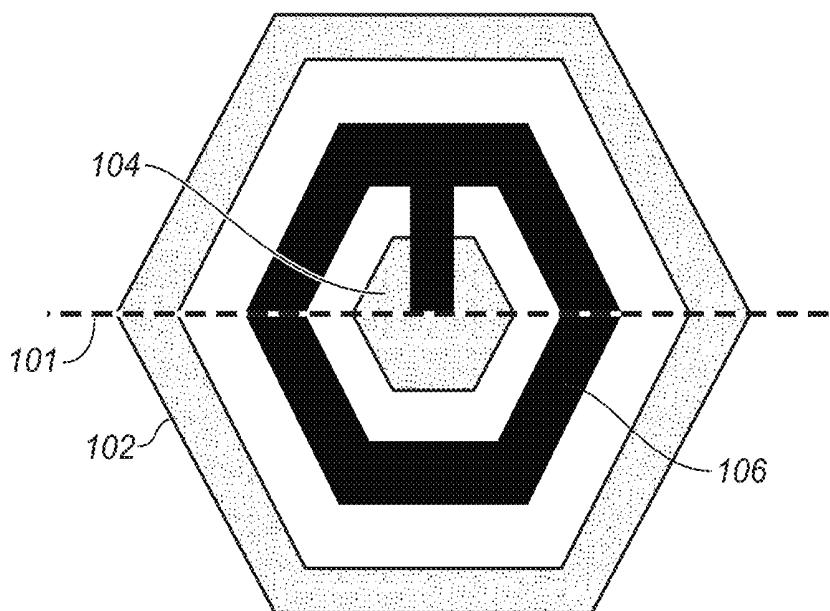
**FIG. 1****FIG. 2**

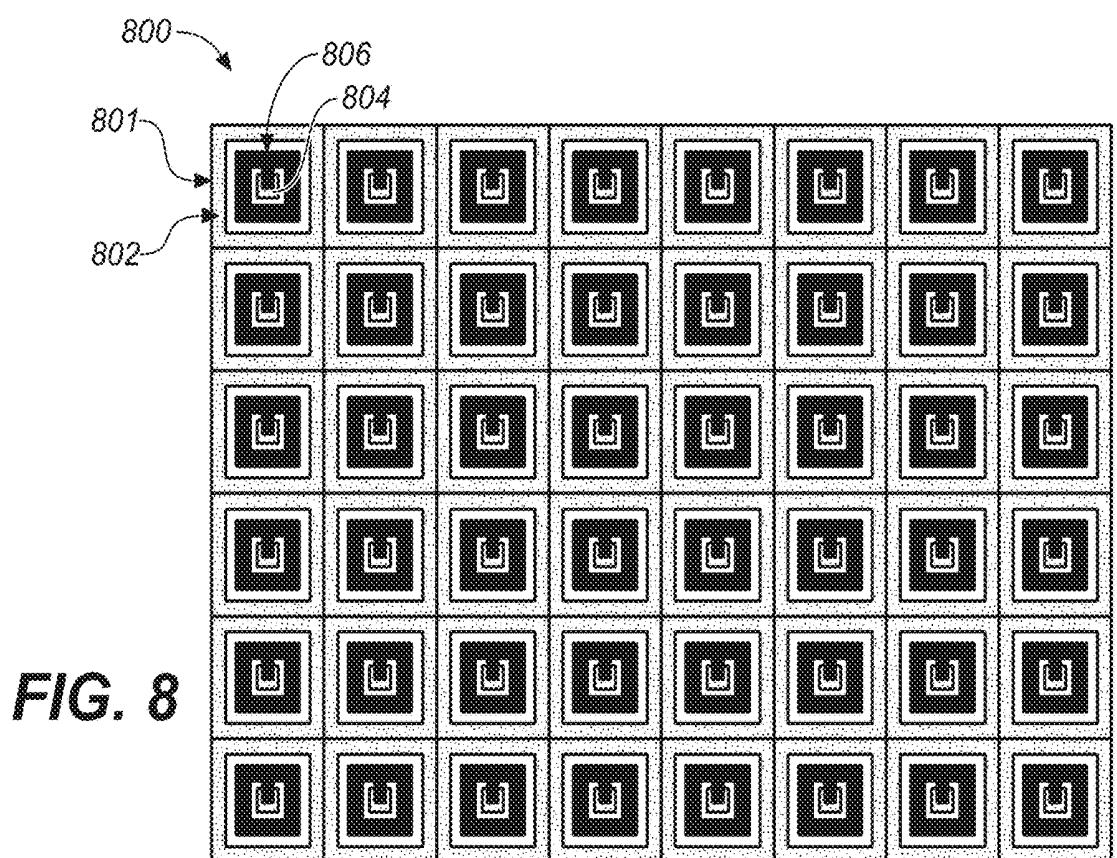
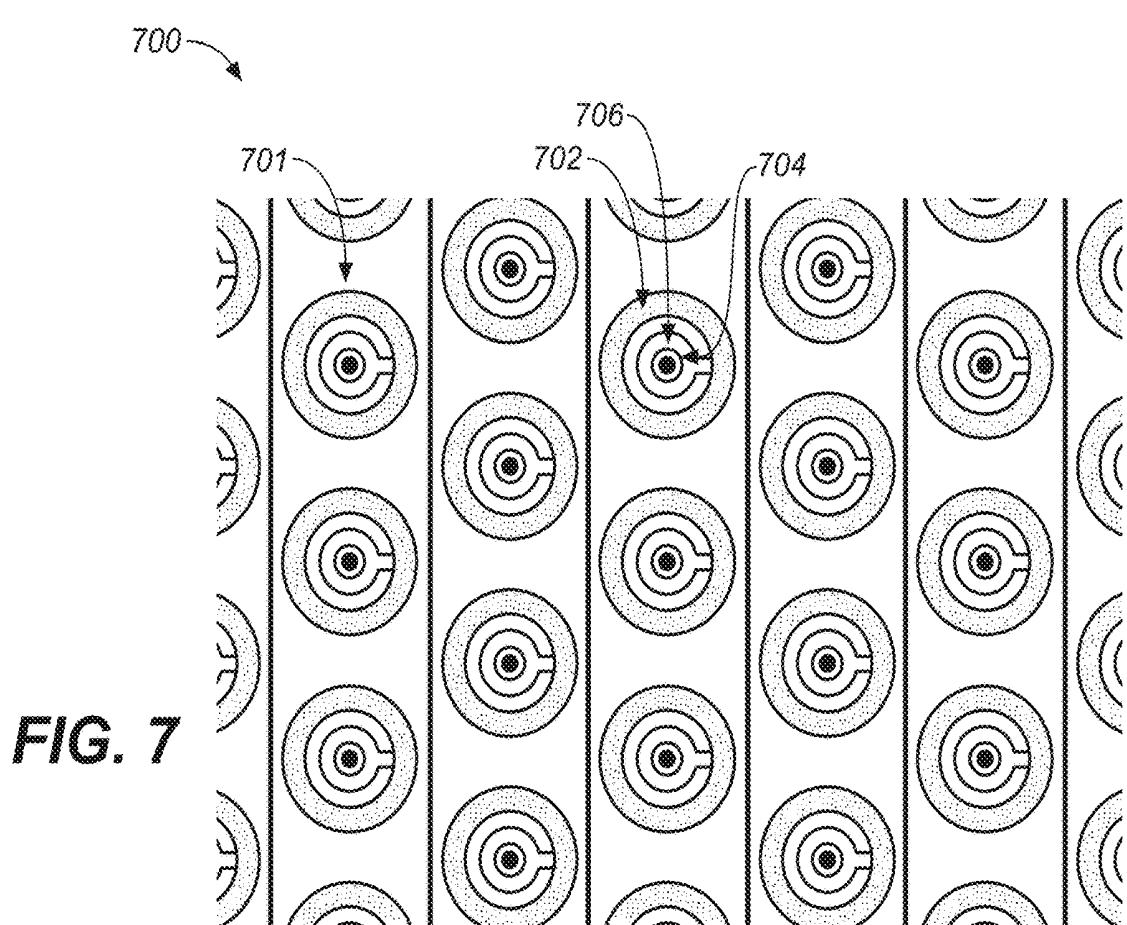


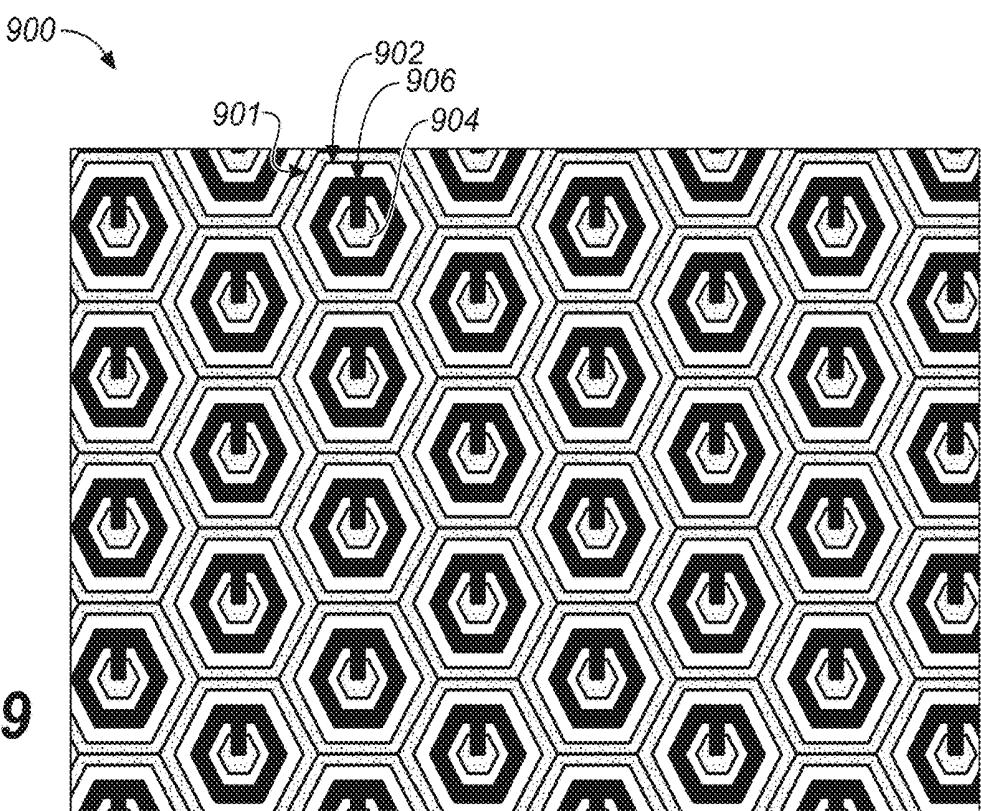
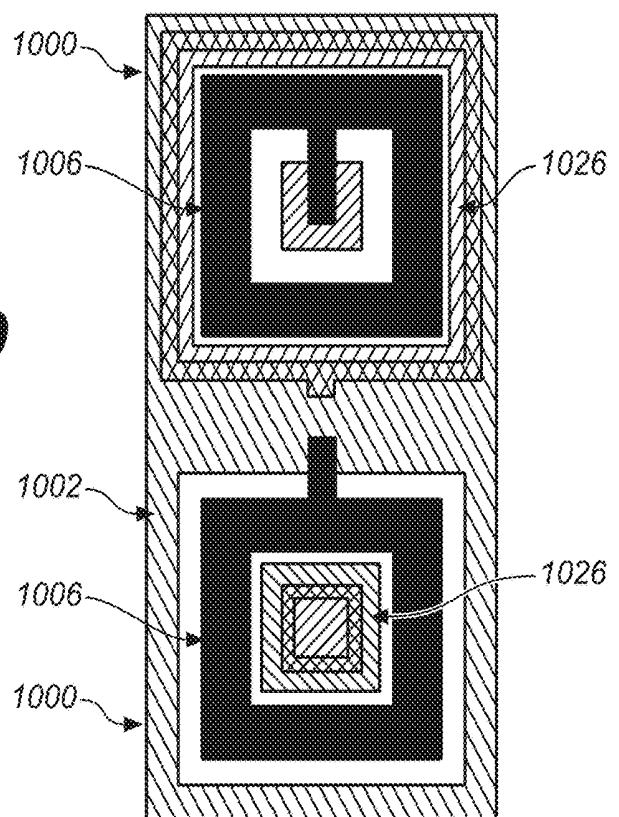
***FIG. 3***

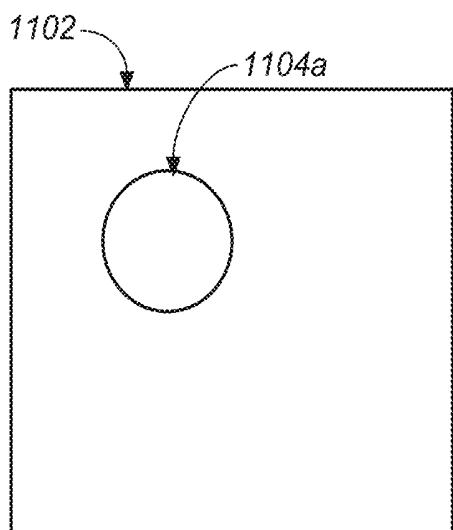
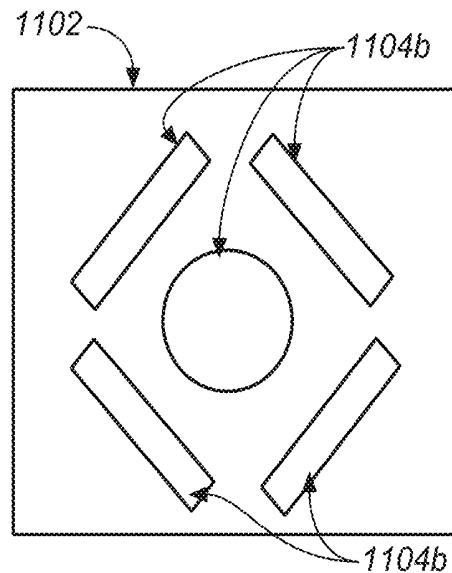
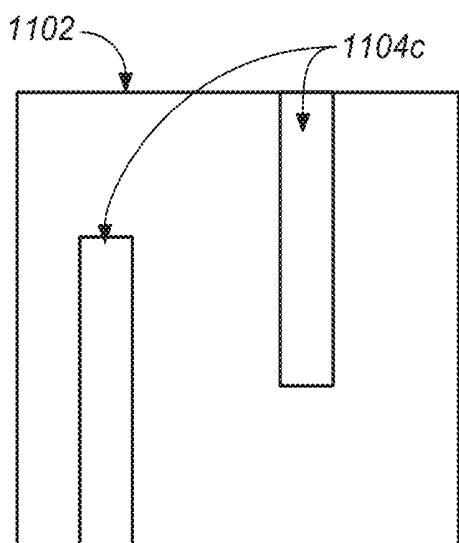
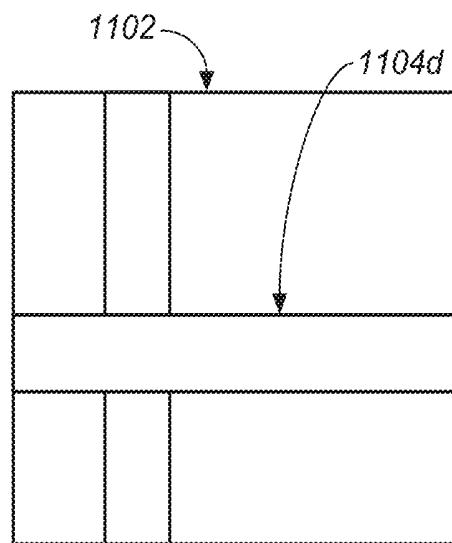


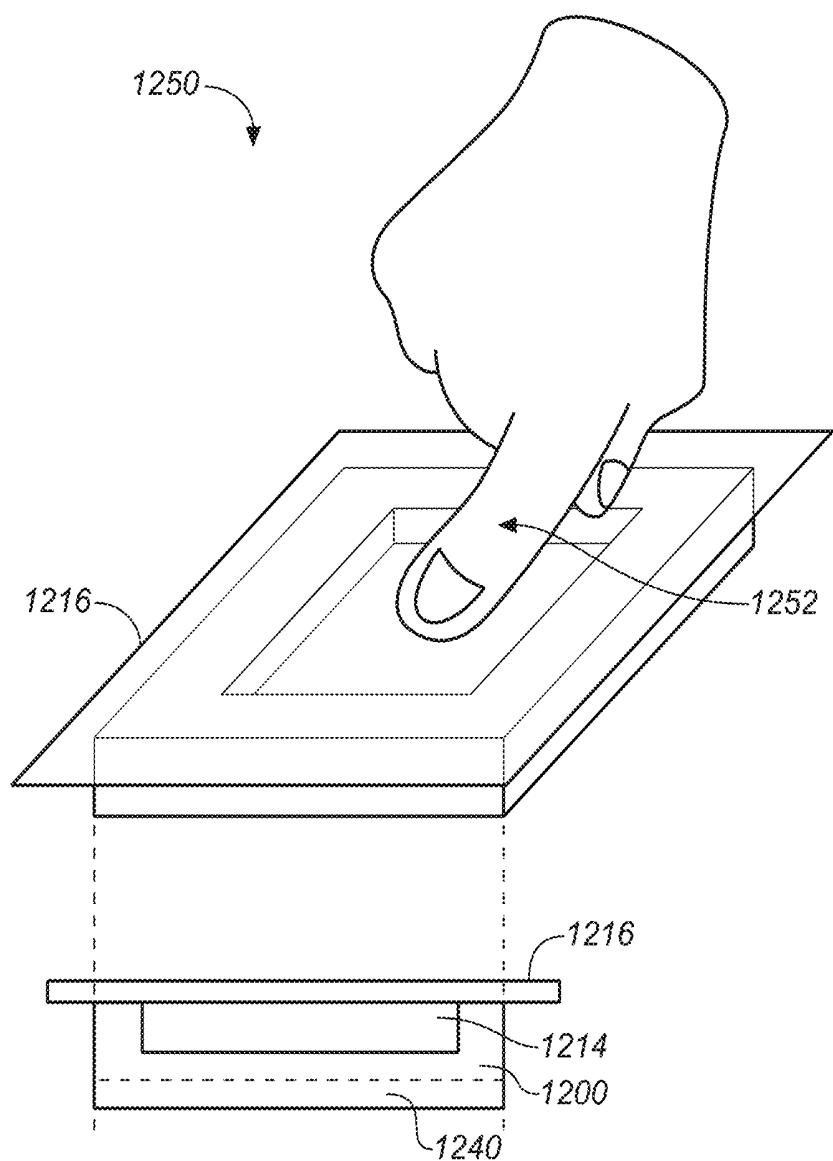
***FIG. 4***

**FIG. 5****FIG. 6**



**FIG. 9****FIG. 10**

**FIG. 11A****FIG. 11B****FIG. 11C****FIG. 11D**



**FIG. 12**

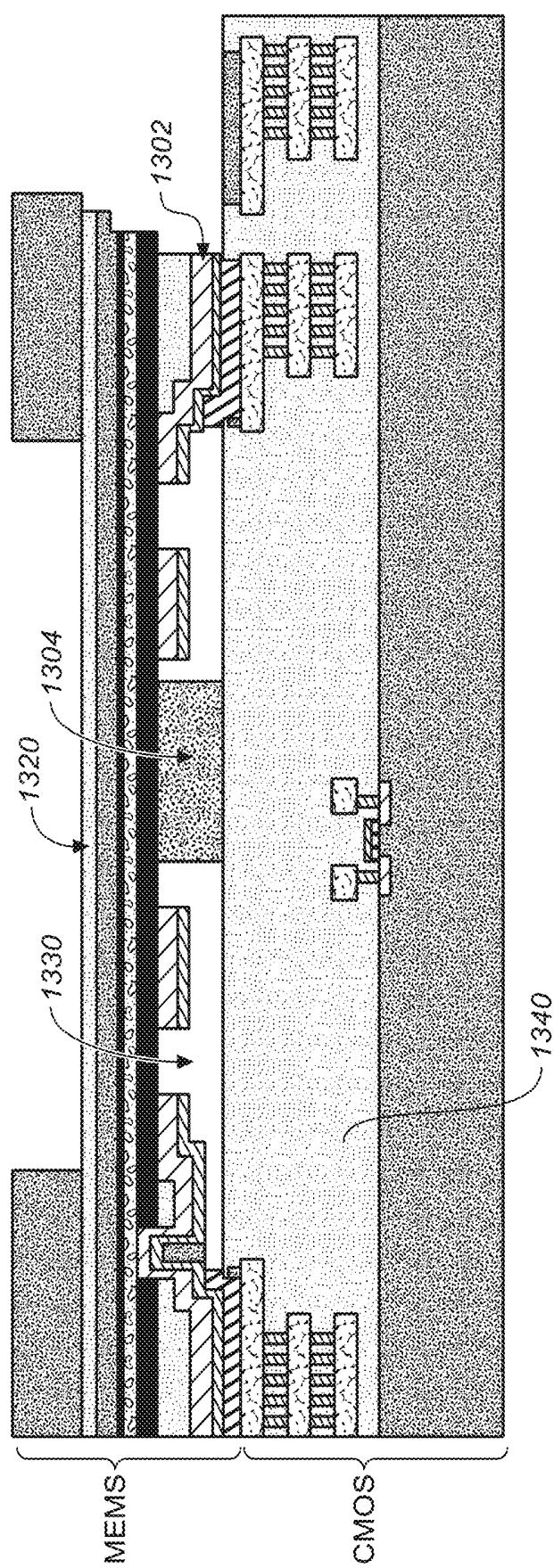


FIG. 13

# PIEZOELECTRIC MICROMACHINED ULTRASONIC TRANSDUCER (PMUT)

## RELATED APPLICATIONS

This application claims priority to and the benefit of U.S. Patent Provisional Patent Application 62/331,919, filed on May 4, 2016, entitled "PINNED ULTRASONIC TRANSDUCERS," by Ng et al., and assigned to the assignee of the present application, which is incorporated herein by reference in its entirety.

## BACKGROUND

Piezoelectric materials facilitate conversion between mechanical energy and electrical energy. Moreover, a piezoelectric material can generate an electrical signal when subjected to mechanical stress, and can vibrate when subjected to an electrical voltage. Piezoelectric materials are widely utilized in piezoelectric ultrasonic transducers to generate acoustic waves based on an actuation voltage applied to electrodes of the piezoelectric ultrasonic transducer.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of the Description of Embodiments, illustrate various embodiments of the subject matter and, together with the Description of Embodiments, serve to explain principles of the subject matter discussed below. Unless specifically noted, the drawings referred to in this Brief Description of Drawings should be understood as not being drawn to scale. Herein, like items are labeled with like item numbers.

FIG. 1 is a diagram illustrating a PMUT device having a center pinned membrane, according to some embodiments.

FIG. 2 is a diagram illustrating an example of membrane movement during activation of a PMUT device, according to some embodiments.

FIG. 3 is a top view of the PMUT device of FIG. 1, according to some embodiments.

FIG. 4 is a simulated map illustrating maximum vertical displacement of the membrane of the PMUT device shown in FIGS. 1-3, according to some embodiments.

FIG. 5 is a top view of an example PMUT device having a circular shape, according to some embodiments.

FIG. 6 is a top view of an example PMUT device having a hexagonal shape, according to some embodiments.

FIG. 7 illustrates an example array of circular-shaped PMUT devices, according to some embodiments.

FIG. 8 illustrates an example array of square-shaped PMUT devices, according to some embodiments.

FIG. 9 illustrates an example array of hexagonal-shaped PMUT devices, according to some embodiments.

FIG. 10 illustrates an example pair of PMUT devices in a PMUT array, with each PMUT having differing electrode patterning, according to some embodiments.

FIGS. 11A, 11B, 11C, and 11D illustrate alternative examples of interior support structures, according to various embodiments.

FIG. 12 illustrates a PMUT array used in an ultrasonic fingerprint sensing system, according to some embodiments.

FIG. 13 illustrates an integrated fingerprint sensor formed by wafer bonding a CMOS logic wafer and a microelectromechanical (MEMS) wafer defining PMUT devices, according to some embodiments.

## DESCRIPTION OF EMBODIMENTS

The following Description of Embodiments is merely provided by way of example and not of limitation. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding background or in the following Description of Embodiments.

Reference will now be made in detail to various embodiments of the subject matter, examples of which are illustrated in the accompanying drawings. While various embodiments are discussed herein, it will be understood that they are not intended to limit to these embodiments. On the contrary, the presented embodiments are intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope the various embodiments as defined by the appended claims. Furthermore, in this Description of Embodiments, numerous specific details are set forth in order to provide a thorough understanding of embodiments of the present subject matter. However, embodiments may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the described embodiments.

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### Notation and Nomenclature

Some portions of the detailed descriptions which follow are presented in terms of procedures, logic blocks, processing and other symbolic representations of operations on data within an electrical device. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. In the present application, a procedure, logic block, process, or the like, is conceived to be one or more self-consistent procedures or instructions leading to a desired result. The procedures are those requiring physical manipulations of physical quantities. Usually, although not necessarily, these quantities take the form of acoustic (e.g., ultrasonic) signals capable of being transmitted and received by an electronic device and/or electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in an electrical device.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the description of embodiments, discussions utilizing terms such as "transmitting," "receiving," "sensing," "generating," "imaging," or the like, refer to the actions and processes of an electronic device such as an electrical device.

Embodiments described herein may be discussed in the general context of processor-executable instructions residing on some form of non-transitory processor-readable medium, such as program modules, executed by one or more computers or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc., that perform particular tasks or implement particular abstract data types. The functionality of the program modules may be combined or distributed as desired in various embodiments.

In the figures, a single block may be described as performing a function or functions; however, in actual practice, the function or functions performed by that block may be

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performed in a single component or across multiple components, and/or may be performed using hardware, using software, or using a combination of hardware and software. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, logic, circuits, and steps have been described generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure. Also, the example fingerprint sensing system and/or mobile electronic device described herein may include components other than those shown, including well-known components.

Various techniques described herein may be implemented in hardware, software, firmware, or any combination thereof, unless specifically described as being implemented in a specific manner. Any features described as modules or components may also be implemented together in an integrated logic device or separately as discrete but interoperable logic devices. If implemented in software, the techniques may be realized at least in part by a non-transitory processor-readable storage medium comprising instructions that, when executed, perform one or more of the methods described herein. The non-transitory processor-readable data storage medium may form part of a computer program product, which may include packaging materials.

The non-transitory processor-readable storage medium may comprise random access memory (RAM) such as synchronous dynamic random access memory (SDRAM), read only memory (ROM), non-volatile random access memory (NVRAM), electrically erasable programmable read-only memory (EEPROM), FLASH memory, other known storage media, and the like. The techniques additionally, or alternatively, may be realized at least in part by a processor-readable communication medium that carries or communicates code in the form of instructions or data structures and that can be accessed, read, and/or executed by a computer or other processor.

Various embodiments described herein may be executed by one or more processors, such as one or more motion processing units (MPUs), sensor processing units (SPUs), host processor(s) or core(s) thereof, digital signal processors (DSPs), general purpose microprocessors, application specific integrated circuits (ASICs), application specific instruction set processors (ASIPs), field programmable gate arrays (FPGAs), a programmable logic controller (PLC), a complex programmable logic device (CPLD), a discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein, or other equivalent integrated or discrete logic circuitry. The term “processor,” as used herein may refer to any of the foregoing structures or any other structure suitable for implementation of the techniques described herein. As it is employed in the subject specification, the term “processor” can refer to substantially any computing processing unit or device comprising, but not limited to comprising, single-core processors; single-processors with software multithread execution capability; multi-core processors; multi-core processors with software multithread execution capability; multi-core processors with hardware multithread technology; parallel platforms; and parallel platforms with distributed shared memory. Moreover, processors can exploit nano-scale architectures such as, but not limited to, molecu-

lar and quantum-dot based transistors, switches and gates, in order to optimize space usage or enhance performance of user equipment. A processor may also be implemented as a combination of computing processing units.

In addition, in some aspects, the functionality described herein may be provided within dedicated software modules or hardware modules configured as described herein. Also, the techniques could be fully implemented in one or more circuits or logic elements. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of an SPU/MPU and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with an SPU core, MPU core, or any other such configuration.

## OVERVIEW OF DISCUSSION

Discussion begins with a description of an example piezoelectric micromachined ultrasonic transducer (PMUT), in accordance with various embodiments. Example arrays including PMUT devices are then described. Example operations of the example arrays of PMUT devices are then further described.

A conventional piezoelectric ultrasonic transducer able to generate and detect pressure waves can include a membrane with the piezoelectric material, a supporting layer, and electrodes combined with a cavity beneath the electrodes. Miniaturized versions are referred to as PMUTs. Typical PMUTs use an edge anchored membrane or diaphragm that maximally oscillates at or near the center of the membrane at a resonant frequency ( $f$ ) proportional to  $h/a^2$ , where  $h$  is the thickness, and  $a$  is the radius of the membrane. Higher frequency membrane oscillations can be created by increasing the membrane thickness, decreasing the membrane radius, or both. Increasing the membrane thickness has its limits, as the increased thickness limits the displacement of the membrane. Reducing the PMUT membrane radius also has limits, because a larger percentage of PMUT membrane area is used for edge anchoring.

Embodiments described herein relate to a PMUT device for ultrasonic wave generation and sensing. In accordance with various embodiments, an array of such PMUT devices is described. The PMUT includes a substrate and an edge support structure connected to the substrate. A membrane is connected to the edge support structure such that a cavity is defined between the membrane and the substrate, where the membrane is configured to allow movement at ultrasonic frequencies. The membrane includes a piezoelectric layer and first and second electrodes coupled to opposing sides of the piezoelectric layer. An interior support structure is disposed within the cavity and connected to the substrate and the membrane.

The described PMUT device and array of PMUT devices can be used for generation of acoustic signals or measurement of acoustically sensed data in various applications, such as, but not limited to, medical applications, security systems, biometric systems (e.g., fingerprint sensors and/or motion/gesture recognition sensors), mobile communication systems, industrial automation systems, consumer electronic devices, robotics, etc. In one embodiment, the PMUT device can facilitate ultrasonic signal generation and sensing (transducer). Moreover, embodiments described herein provide a

sensing component including a silicon wafer having a two-dimensional (or one-dimensional) array of ultrasonic transducers.

Embodiments described herein provide a PMUT that operates at a high frequency for reduced acoustic diffraction through high acoustic velocity materials (e.g., glass, metal), and for shorter pulses so that spurious reflections can be time-gated out. Embodiments described herein also provide a PMUT that has a low quality factor providing a shorter ring-up and ring-down time to allow better rejection of spurious reflections by time-gating. Embodiments described herein also provide a PMUT that has a high fill-factor providing for large transmit and receive signals.

#### Piezoelectric Micromachined Ultrasonic Transducer (PMUT)

Systems and methods disclosed herein, in one or more aspects provide efficient structures for an acoustic transducer (e.g., a piezoelectric actuated transducer or PMUT). One or more embodiments are now described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the various embodiments. It may be evident, however, that the various embodiments can be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form in order to facilitate describing the embodiments in additional detail.

As used in this application, the term “or” is intended to mean an inclusive “or” rather than an exclusive “or”. That is, unless specified otherwise, or clear from context, “X employs A or B” is intended to mean any of the natural inclusive permutations. That is, if X employs A; X employs B; or X employs both A and B, then “X employs A or B” is satisfied under any of the foregoing instances. In addition, the articles “a” and “an” as used in this application and the appended claims should generally be construed to mean “one or more” unless specified otherwise or clear from context to be directed to a singular form. In addition, the word “coupled” is used herein to mean direct or indirect electrical or mechanical coupling. In addition, the word “example” is used herein to mean serving as an example, instance, or illustration.

FIG. 1 is a diagram illustrating a PMUT device 100 having a center pinned membrane, according to some embodiments. PMUT device 100 includes an interior pinned membrane 120 positioned over a substrate 140 to define a cavity 130. In one embodiment, membrane 120 is attached both to a surrounding edge support 102 and interior support 104. In one embodiment, edge support 102 is connected to an electric potential. Edge support 102 and interior support 104 may be made of electrically conducting materials, such as and without limitation, aluminum, molybdenum, or titanium. Edge support 102 and interior support 104 may also be made of dielectric materials, such as silicon dioxide, silicon nitride or aluminum oxide that have electrical connections the sides or in vias through edge support 102 or interior support 104, electrically coupling lower electrode 106 to electrical wiring in substrate 140.

In one embodiment, both edge support 102 and interior support 104 are attached to a substrate 140. In various embodiments, substrate 140 may include at least one of, and without limitation, silicon or silicon nitride. It should be appreciated that substrate 140 may include electrical wirings and connection, such as aluminum or copper. In one embodiment,

substrate 140 includes a CMOS logic wafer bonded to edge support 102 and interior support 104. In one embodiment, the membrane 120 comprises multiple layers. In an example embodiment, the membrane 120 includes lower electrode 106, piezoelectric layer 110, and upper electrode 108, where lower electrode 106 and upper electrode 108 are coupled to opposing sides of piezoelectric layer 110. As shown, lower electrode 106 is coupled to a lower surface of piezoelectric layer 110 and upper electrode 108 is coupled to an upper surface of piezoelectric layer 110. It should be appreciated that, in various embodiments, PMUT device 100 is a microelectromechanical (MEMS) device.

In one embodiment, membrane 120 also includes a mechanical support layer 112 (e.g., stiffening layer) to mechanically stiffen the layers. In various embodiments, mechanical support layer 140 may include at least one of, and without limitation, silicon, silicon oxide, silicon nitride, aluminum, molybdenum, titanium, etc. In one embodiment, PMUT device 100 also includes an acoustic coupling layer 114 above membrane 120 for supporting transmission of acoustic signals. It should be appreciated that acoustic coupling layer can include air, liquid, gel-like materials, or other materials for supporting transmission of acoustic signals. In one embodiment, PMUT device 100 also includes platen layer 116 above acoustic coupling layer 114 for containing acoustic coupling layer 114 and providing a contact surface for a finger or other sensed object with PMUT device 100. It should be appreciated that, in various embodiments, acoustic coupling layer 114 provides a contact surface, such that platen layer 116 is optional. Moreover, it should be appreciated that acoustic coupling layer 114 and/or platen layer 116 may be included with or used in conjunction with multiple PMUT devices. For example, an array of PMUT devices may be coupled with a single acoustic coupling layer 114 and/or platen layer 116.

FIG. 2 is a diagram illustrating an example of membrane movement during activation of PMUT device 100, according to some embodiments. As illustrated with respect to FIG. 2, in operation, responsive to an object proximate platen layer 116, the electrodes 106 and 108 deliver a high frequency electric charge to the piezoelectric layer 110, causing those portions of the membrane 120 not pinned to the surrounding edge support 102 or interior support 104 to be displaced upward into the acoustic coupling layer 114. This generates a pressure wave that can be used for signal probing of the object. Return echoes can be detected as pressure waves causing movement of the membrane, with compression of the piezoelectric material in the membrane causing an electrical signal proportional to amplitude of the pressure wave.

The described PMUT device 100 can be used with almost any electrical device that converts a pressure wave into mechanical vibrations and/or electrical signals. In one aspect, the PMUT device 100 can comprise an acoustic sensing element (e.g., a piezoelectric element) that generates and senses ultrasonic sound waves. An object in a path of the generated sound waves can create a disturbance (e.g., changes in frequency or phase, reflection signal, echoes, etc.) that can then be sensed. The interference can be analyzed to determine physical parameters such as (but not limited to) distance, density and/or speed of the object. As an example, the PMUT device 100 can be utilized in various applications, such as, but not limited to, fingerprint or physiologic sensors suitable for wireless devices, industrial systems, automotive systems, robotics, telecommunications, security, medical devices, etc. For example, the PMUT device 100 can be part of a sensor array comprising a

plurality of ultrasonic transducers deposited on a wafer, along with various logic, control and communication electronics. A sensor array may comprise homogenous or identical PMUT devices 100, or a number of different or heterogeneous device structures.

In various embodiments, the PMUT device 100 employs a piezoelectric layer 110, comprised of materials such as, but not limited to, Aluminum nitride (AlN), lead zirconate titanate (PZT), quartz, polyvinylidene fluoride (PVDF), and/or zinc oxide, to facilitate both acoustic signal production and sensing. The piezoelectric layer 110 can generate electric charges under mechanical stress and conversely experience a mechanical strain in the presence of an electric field. For example, the piezoelectric layer 110 can sense mechanical vibrations caused by an ultrasonic signal and produce an electrical charge at the frequency (e.g., ultrasonic frequency) of the vibrations. Additionally, the piezoelectric layer 110 can generate an ultrasonic wave by vibrating in an oscillatory fashion that might be at the same frequency (e.g., ultrasonic frequency) as an input current generated by an alternating current (AC) voltage applied across the piezoelectric layer 110. It should be appreciated that the piezoelectric layer 110 can include almost any material (or combination of materials) that exhibits piezoelectric properties, such that the structure of the material does not have a center of symmetry and a tensile or compressive stress applied to the material alters the separation between positive and negative charge sites in a cell causing a polarization at the surface of the material. The polarization is directly proportional to the applied stress and is direction dependent so that compressive and tensile stresses results in electric fields of opposite polarizations.

Further, the PMUT device 100 comprises electrodes 106 and 108 that supply and/or collect the electrical charge to/from the piezoelectric layer 110. It should be appreciated that electrodes 106 and 108 can be continuous and/or patterned electrodes (e.g., in a continuous layer and/or a patterned layer). For example, as illustrated, electrode 106 is a patterned electrode and electrode 108 is a continuous electrode. As an example, electrodes 106 and 108 can be comprised of almost any metal layers, such as, but not limited to, Aluminum (Al)/Titanium (Ti), Molybdenum (Mo), etc., which are coupled with an on opposing sides of the piezoelectric layer 110. In one embodiment, PMUT device also includes a third electrode, as illustrated in FIG. 10 and described below.

According to an embodiment, the acoustic impedance of acoustic coupling layer 114 is selected to be similar to the acoustic impedance of the platen layer 116, such that the acoustic wave is efficiently propagated to/from the membrane 120 through acoustic coupling layer 114 and platen layer 116. As an example, the platen layer 116 can comprise various materials having an acoustic impedance in the range between 0.8 to 4 MRayl, such as, but not limited to, plastic, resin, rubber, Teflon, epoxy, etc. In another example, the platen layer 116 can comprise various materials having a high acoustic impedance (e.g., an acoustic impedance greater than 10 MiRayl), such as, but not limited to, glass, aluminum-based alloys, sapphire, etc. Typically, the platen layer 116 can be selected based on an application of the sensor. For instance, in fingerprinting applications, platen layer 116 can have an acoustic impedance that matches (e.g., exactly or approximately) the acoustic impedance of human skin (e.g.,  $1.6 \times 10^6$  Rayl). Further, in one aspect, the platen layer 116 can further include a thin layer of anti-scratch material. In various embodiments, the anti-scratch layer of the platen layer 116 is less than the wavelength of the

acoustic wave that is to be generated and/or sensed to provide minimum interference during propagation of the acoustic wave. As an example, the anti-scratch layer can comprise various hard and scratch-resistant materials (e.g., having a Mohs hardness of over 7 on the Mohs scale), such as, but not limited to sapphire, glass, MN, Titanium nitride (TiN), Silicon carbide (SiC), diamond, etc. As an example, PMUT device 100 can operate at 20 MHz and accordingly, the wavelength of the acoustic wave propagating through the acoustic coupling layer 114 and platen layer 116 can be 70-150 microns. In this example scenario, insertion loss can be reduced and acoustic wave propagation efficiency can be improved by utilizing an anti-scratch layer having a thickness of 1 micron and the platen layer 116 as a whole having a thickness of 1-2 millimeters. It is noted that the term "anti-scratch material" as used herein relates to a material that is resistant to scratches and/or scratch-proof and provides substantial protection against scratch marks.

In accordance with various embodiments, the PMUT device 100 can include metal layers (e.g., Aluminum (Al)/Titanium (Ti), Molybdenum (Mo), etc.) patterned to form electrode 106 in particular shapes (e.g., ring, circle, square, octagon, hexagon, etc.) that are defined in-plane with the membrane 120. Electrodes can be placed at a maximum strain area of the membrane 120 or placed at close to either or both the surrounding edge support 102 and interior support 104. Furthermore, in one example, electrode 108 can be formed as a continuous layer providing a ground plane in contact with mechanical support layer 112, which can be formed from silicon or other suitable mechanical stiffening material. In still other embodiments, the electrode 106 can be routed along the interior support 104, advantageously reducing parasitic capacitance as compared to routing along the edge support 102.

For example, when actuation voltage is applied to the electrodes, the membrane 120 will deform and move out of plane. The motion then pushes the acoustic coupling layer 114 it is in contact with and an acoustic (ultrasonic) wave is generated. Oftentimes, vacuum is present inside the cavity 130 and therefore damping contributed from the media within the cavity 130 can be ignored. However, the acoustic coupling layer 114 on the other side of the membrane 120 can substantially change the damping of the PMUT device 100. For example, a quality factor greater than 20 can be observed when the PMUT device 100 is operating in air with atmosphere pressure (e.g., acoustic coupling layer 114 is air) and can decrease lower than 2 if the PMUT device 100 is operating in water (e.g., acoustic coupling layer 114 is water).

FIG. 3 is a top view of the PMUT device 100 of FIG. 1 having a substantially square shape, which corresponds in part to a cross section along dotted line 101 in FIG. 3. Layout of surrounding edge support 102, interior support 104, and lower electrode 106 are illustrated, with other continuous layers not shown. It should be appreciated that the term "substantially" in "substantially square shape" is intended to convey that a PMUT device 100 is generally square-shaped, with allowances for variations due to manufacturing processes and tolerances, and that slight deviation from a square shape (e.g., rounded corners, slightly wavering lines, deviations from perfectly orthogonal corners or intersections, etc.) may be present in a manufactured device. While a generally square arrangement PMUT device is shown, alternative embodiments including rectangular, hexagon, octagonal, circular, or elliptical are contemplated. In other embodiments, more complex electrode or PMUT device shapes can

be used, including irregular and non-symmetric layouts such as chevrons or pentagons for edge support and electrodes.

FIG. 4 is a simulated topographic map 400 illustrating maximum vertical displacement of the membrane 120 of the PMUT device 100 shown in FIGS. 1-3. As indicated, maximum displacement generally occurs along a center axis of the lower electrode, with corner regions having the greatest displacement. As with the other figures, FIG. 4 is not drawn to scale with the vertical displacement exaggerated for illustrative purposes, and the maximum vertical displacement is a fraction of the horizontal surface area comprising the PMUT device 100. In an example PMUT device 100, maximum vertical displacement may be measured in nanometers, while surface area of an individual PMUT device 100 may be measured in square microns.

FIG. 5 is a top view of another example of the PMUT device 100 of FIG. 1 having a substantially circular shape, which corresponds in part to a cross section along dotted line 101 in FIG. 5. Layout of surrounding edge support 102, interior support 104, and lower electrode 106 are illustrated, with other continuous layers not shown. It should be appreciated that the term “substantially” in “substantially circular shape” is intended to convey that a PMUT device 100 is generally circle-shaped, with allowances for variations due to manufacturing processes and tolerances, and that slight deviation from a circle shape (e.g., slight deviations on radial distance from center, etc.) may be present in a manufactured device.

FIG. 6 is a top view of another example of the PMUT device 100 of FIG. 1 having a substantially hexagonal shape, which corresponds in part to a cross section along dotted line 101 in FIG. 6. Layout of surrounding edge support 102, interior support 104, and lower electrode 106 are illustrated, with other continuous layers not shown. It should be appreciated that the term “substantially” in “substantially hexagonal shape” is intended to convey that a PMUT device 100 is generally hexagon-shaped, with allowances for variations due to manufacturing processes and tolerances, and that slight deviation from a hexagon shape (e.g., rounded corners, slightly wavering lines, deviations from perfectly orthogonal corners or intersections, etc.) may be present in a manufactured device.

FIG. 7 illustrates an example two-dimensional array 700 of circular-shaped PMUT devices 701 formed from PMUT devices having a substantially circular shape similar to that discussed in conjunction with FIGS. 1, 2 and 5. Layout of circular surrounding edge support 702, interior support 704, and annular or ring shaped lower electrode 706 surrounding the interior support 704 are illustrated, while other continuous layers are not shown for clarity. As illustrated, array 700 includes columns of circular-shaped PMUT devices 701 that are offset. It should be appreciated that the circular-shaped PMUT devices 701 may be closer together, such that edges of the columns of circular-shaped PMUT devices 701 overlap. Moreover, it should be appreciated that circular-shaped PMUT devices 701 may contact each other. In various embodiments, adjacent circular-shaped PMUT devices 701 are electrically isolated. In other embodiments, groups of adjacent circular-shaped PMUT devices 701 are electrically connected, where the groups of adjacent circular-shaped PMUT devices 701 are electrically isolated.

FIG. 8 illustrates an example two-dimensional array 800 of square-shaped PMUT devices 801 formed from PMUT devices having a substantially square shape similar to that discussed in conjunction with FIGS. 1, 2 and 3. Layout of square surrounding edge support 802, interior support 804, and square-shaped lower electrode 806 surrounding the

interior support 804 are illustrated, while other continuous layers are not shown for clarity. As illustrated, array 800 includes columns of square-shaped PMUT devices 801 that are in rows and columns. It should be appreciated that rows or columns of the square-shaped PMUT devices 801 may be offset. Moreover, it should be appreciated that square-shaped PMUT devices 801 may contact each other or be spaced apart. In various embodiments, adjacent square-shaped PMUT devices 801 are electrically isolated. In other embodiments, groups of adjacent square-shaped PMUT devices 801 are electrically connected, where the groups of adjacent square-shaped PMUT devices 801 are electrically isolated.

FIG. 9 illustrates an example two-dimensional array 900 of hexagon-shaped PMUT devices 901 formed from PMUT devices having a substantially hexagon shape similar to that discussed in conjunction with FIGS. 1, 2 and 6. Layout of hexagon-shaped surrounding edge support 902, interior support 904, and hexagon-shaped lower electrode 906 surrounding the interior support 904 are illustrated, while other continuous layers are not shown for clarity. It should be appreciated that rows or columns of the hexagon-shaped PMUT devices 901 may be offset. Moreover, it should be appreciated that hexagon-shaped PMUT devices 901 may contact each other or be spaced apart. In various embodiments, adjacent hexagon-shaped PMUT devices 901 are electrically isolated. In other embodiments, groups of adjacent hexagon-shaped PMUT devices 901 are electrically connected, where the groups of adjacent hexagon-shaped PMUT devices 901 are electrically isolated. While FIGS. 7, 8 and 9 illustrate example layouts of PMUT devices having different shapes, it should be appreciated that many different layouts are available. Moreover, in accordance with various embodiments, arrays of PMUT devices are included within a MEMS layer.

In operation, during transmission, selected sets of PMUT devices in the two-dimensional array can transmit an acoustic signal (e.g., a short ultrasonic pulse) and during sensing, the set of active PMUT devices in the two-dimensional array can detect an interference of the acoustic signal with an object (in the path of the acoustic wave). The received interference signal (e.g., generated based on reflections, echoes, etc. of the acoustic signal from the object) can then be analyzed. As an example, an image of the object, a distance of the object from the sensing component, a density of the object, a motion of the object, etc., can all be determined based on comparing a frequency and/or phase of the interference signal with a frequency and/or phase of the acoustic signal. Moreover, results generated can be further analyzed or presented to a user via a display device (not shown).

FIG. 10 illustrates a pair of example PMUT devices 1000 in a PMUT array, with each PMUT sharing at least one common edge support 1002. As illustrated, the PMUT devices have two sets of independent lower electrode labeled as 1006 and 1026. These differing electrode patterns enable antiphase operation of the PMUT devices 1000, and increase flexibility of device operation. In one embodiment, the pair of PMUTs may be identical, but the two electrodes could drive different parts of the same PMUT antiphase (one contracting, and one extending), such that the PMUT displacement becomes larger. While other continuous layers are not shown for clarity, each PMUT also includes an upper electrode (e.g., upper electrode 108 of FIG. 1). Accordingly, in various embodiments, a PMUT device may include at least three electrodes.

FIGS. 11A, 11B, 11C, and 11D illustrate alternative examples of interior support structures, in accordance with various embodiments. Interior supports structures may also be referred to as “pinning structures,” as they operate to pin the membrane to the substrate. It should be appreciated that interior support structures may be positioned anywhere within a cavity of a PMUT device, and may have any type of shape (or variety of shapes), and that there may be more than one interior support structure within a PMUT device. While FIGS. 11A, 11B, 11C, and 11D illustrate alternative examples of interior support structures, it should be appreciated that these examples or for illustrative purposes, and are not intended to limit the number, position, or type of interior support structures of PMUT devices.

For example, interior supports structures do not have to be centrally located with a PMUT device area, but can be non-centrally positioned within the cavity. As illustrated in FIG. 11A, interior support 1104a is positioned in a non-central, off-axis position with respect to edge support 1102. In other embodiments such as seen in FIG. 11B, multiple interior supports 1104b can be used. In this embodiment, one interior support is centrally located with respect to edge support 1102, while the multiple, differently shaped and sized interior supports surround the centrally located support. In still other embodiments, such as seen with respect to FIGS. 11C and 11D, the interior supports (respectively 1104c and 1104d) can contact a common edge support 1102. In the embodiment illustrated in FIG. 11D, the interior supports 1104d can effectively divide the PMUT device into subpixels. This would allow, for example, activation of smaller areas to generate high frequency ultrasonic waves, and sensing a returning ultrasonic echo with larger areas of the PMUT device. It will be appreciated that the individual pinning structures can be combined into arrays.

FIG. 12 illustrates an embodiment of a PMUT array used in an ultrasonic fingerprint sensing system 1250. The fingerprint sensing system 1250 can include a platen 1216 onto which a human finger 1252 may make contact. Ultrasonic signals are generated and received by a PMUT device array 1200, and travel back and forth through acoustic coupling layer 1214 and platen 1216. Signal analysis is conducted using processing logic module 1240 (e.g., control logic) directly attached (via wafer bonding or other suitable techniques) to the PMUT device array 1200. It will be appreciated that the size of platen 1216 and the other elements illustrated in FIG. 12 may be much larger (e.g., the size of a handprint) or much smaller (e.g., just a fingertip) than as shown in the illustration, depending on the particular application.

In this example for fingerprinting applications, the human finger 1252 and the processing logic module 1240 can determine, based on a difference in interference of the acoustic signal with valleys and/or ridges of the skin on the finger, an image depicting epi-dermis and/or dermis layers of the finger. Further, the processing logic module 1240 can compare the image with a set of known fingerprint images to facilitate identification and/or authentication. Moreover, in one example, if a match (or substantial match) is found, the identity of user can be verified. In another example, if a match (or substantial match) is found, a command/operation can be performed based on an authorization rights assigned to the identified user. In yet another example, the identified user can be granted access to a physical location and/or network/computer resources (e.g., documents, files, applications, etc.).

In another example, for finger-based applications, the movement of the finger can be used for cursor tracking/

movement applications. In such embodiments, a pointer or cursor on a display screen can be moved in response to finger movement. It is noted that processing logic module 1240 can include or be connected to one or more processors configured to confer at least in part the functionality of system 1250. To that end, the one or more processors can execute code instructions stored in memory, for example, volatile memory and/or nonvolatile memory.

FIG. 13 illustrates an integrated fingerprint sensor 1300 formed by wafer bonding a CMOS logic wafer and a MEMS wafer defining PMUT devices, according to some embodiments. FIG. 13 illustrates in partial cross section one embodiment of an integrated fingerprint sensor formed by wafer bonding a substrate 1340 CMOS logic wafer and a MEMS wafer defining PMUT devices having a common edge support 1302 and separate interior support 1304. For example, the MEMS wafer may be bonded to the CMOS logic wafer using aluminum and germanium eutectic alloys, as described in U.S. Pat. No. 7,442,570. PMUT device 1300 has an interior pinned membrane 1320 formed over a cavity 1330. The membrane 1320 is attached both to a surrounding edge support 1302 and interior support 1304. The membrane 1320 is formed from multiple layers.

What has been described above includes examples of the subject disclosure. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the subject matter, but it is to be appreciated that many further combinations and permutations of the subject disclosure are possible. Accordingly, the claimed subject matter is intended to embrace all such alterations, modifications, and variations that fall within the spirit and scope of the appended claims.

In particular and in regard to the various functions performed by the above described components, devices, circuits, systems and the like, the terms (including a reference to a “means”) used to describe such components are intended to correspond, unless otherwise indicated, to any component which performs the specified function of the described component (e.g., a functional equivalent), even though not structurally equivalent to the disclosed structure, which performs the function in the herein illustrated exemplary aspects of the claimed subject matter.

The aforementioned systems and components have been described with respect to interaction between several components. It can be appreciated that such systems and components can include those components or specified sub-components, some of the specified components or sub-components, and/or additional components, and according to various permutations and combinations of the foregoing. Sub-components can also be implemented as components communicatively coupled to other components rather than included within parent components (hierarchical). Additionally, it should be noted that one or more components may be combined into a single component providing aggregate functionality or divided into several separate sub-components. Any components described herein may also interact with one or more other components not specifically described herein.

In addition, while a particular feature of the subject innovation may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular application. Furthermore, to the extent that the terms “includes,” “including,” “has,” “contains,” variants thereof, and other similar words are used in either the detailed description or the claims, these terms are intended

to be inclusive in a manner similar to the term "comprising" as an open transition word without precluding any additional or other elements.

Thus, the embodiments and examples set forth herein were presented in order to best explain various selected embodiments of the present invention and its particular application and to thereby enable those skilled in the art to make and use embodiments of the invention. However, those skilled in the art will recognize that the foregoing description and examples have been presented for the purposes of illustration and example only. The description as set forth is not intended to be exhaustive or to limit the embodiments of the invention to the precise form disclosed.

What is claimed is:

1. A Piezoelectric Micromachined Ultrasonic Transducer (PMUT) device comprising:

a substrate;  
an edge support structure connected to the substrate;  
a membrane connected to the edge support structure such that a cavity is defined between the membrane and the substrate, the membrane configured to allow movement at ultrasonic frequencies, the membrane comprising:  
a piezoelectric layer configured to generate an electric charge under stress such that the piezoelectric layer senses mechanical vibrations caused by an ultrasonic signal and produces the electric charge responsive to the stress of the piezoelectric layer; and  
first and second electrodes coupled to opposing sides of the piezoelectric layer and configured to collect the electric charge; and  
an interior support structure disposed within the cavity and connected to the substrate and the membrane, wherein the interior support structure contacts the edge support structure.

2. The PMUT device of claim 1, further comprising:  
a second interior support structure disposed within the cavity and connected to the substrate and the membrane.

3. The PMUT device of claim 1, wherein the interior support structure is non-centrally positioned within the cavity.

4. The PMUT device of claim 1, wherein the first electrode defines a continuous layer.

5. The PMUT device of claim 1, wherein the first electrode is a patterned layer.

6. The PMUT device of claim 1, the membrane further comprising:

a mechanical support layer connected to the first electrode.

7. The PMUT device of claim 6, wherein the mechanical support layer defines a continuous layer.

8. The PMUT device of claim 6, wherein the mechanical support layer is a patterned layer.

9. The PMUT device of claim 1, wherein the piezoelectric layer defines a continuous layer.

10. The PMUT device of claim 1, wherein the piezoelectric layer is a patterned layer.

11. The PMUT device of claim 1, wherein the second electrode extends into the cavity and defines an area between the edge support structure and the interior support structure.

12. The PMUT device of claim 1, wherein the interior support structure is connected to the piezoelectric layer of the membrane.

13. The PMUT device of claim 1, wherein the PMUT device is substantially circular such that the edge support structure and the membrane are substantially circular.

14. The PMUT device of claim 1, wherein the PMUT device is substantially square-shaped such that the edge support structure and the membrane are substantially square-shaped.

15. The PMUT device of claim 1, wherein at least one of the first electrode and the second electrode is electrically coupled through the interior support structure.

16. The PMUT device of claim 1, the membrane further comprising:

a third electrode coupled to the piezoelectric layer on an opposing side of the piezoelectric layer as the first electrode.

17. The PMUT device of claim 1, wherein the edge support structure is connected to an electric potential.

18. The PMUT device of claim 1, wherein the substrate comprises a CMOS logic wafer.

19. A Piezoelectric Micromachined Ultrasonic Transducer (PMUT) array comprising:

a plurality of PMUT devices, wherein at least one PMUT device of the plurality of PMUT devices comprises:

a substrate;  
an edge support structure connected to the substrate, wherein the edge support structure is connected to an electric potential;

a membrane connected to the edge support structure such that a cavity is defined between the membrane and the substrate, the membrane configured to allow movement at ultrasonic frequencies, the membrane comprising:  
a piezoelectric layer configured to generate an ultrasonic wave responsive to receiving an electric charge by vibrating in an oscillatory fashion at a frequency related to the electric charge;

first and second electrodes coupled to opposing sides of the piezoelectric layer and configured to apply the electric charge to the piezoelectric layer; and  
a mechanical support layer connected to the first electrode; and  
an interior support structure disposed within the cavity and connected to the substrate and the membrane, wherein the interior support structure contacts the edge support structure.

20. The PMUT array of claim 19, wherein the at least one PMUT device of the plurality of PMUT devices further comprises:

a second interior support structure disposed within the cavity and connected to the substrate and the membrane.

21. The PMUT array of claim 19, wherein the interior support structure is non-centrally positioned within the cavity.

22. The PMUT array of claim 19, wherein the second electrode extends into the cavity and defines an area between the edge support structure and the interior support structure.

23. The PMUT array of claim 19, wherein the interior support structure is connected to the piezoelectric layer of the membrane.

24. The PMUT array of claim 19, wherein at least one of the first electrode and the second electrode is electrically coupled through the interior support structure.

25. The PMUT array of claim 19, wherein the substrate comprises a CMOS logic wafer.

26. The PMUT array of claim 19, wherein adjacent PMUT devices of the plurality of PMUT devices are electrically isolated.

27. The PMUT array of claim 19, wherein groups of adjacent PMUT devices of the plurality of PMUT devices

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are electrically connected, and wherein adjacent groups of adjacent PMUT devices are electrically isolated.

**28.** An image sensing system comprising:

a plurality of Piezoelectric Micromachined Ultrasonic Transducer (PMUT) devices, wherein at least one PMUT device of the plurality of PMUT devices comprises:

a substrate;

an edge support structure connected to the substrate;

a membrane connected to the edge support structure such that a cavity is defined between the membrane and the substrate, the membrane configured to allow movement at ultrasonic frequencies, the membrane comprising:

a piezoelectric layer configured to generate a first electric charge under stress such that the piezoelectric layer senses mechanical vibrations caused by an ultrasonic signal and produces the first electric charge responsive to the stress of the piezoelectric layer, and configured to generate an ultrasonic wave responsive to receiving a second electric charge by vibrating in an oscillatory fashion at a frequency related to the second electric charge;

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first and second electrodes coupled to opposing sides of the piezoelectric layer, the first and second electrodes configured to collect the first electric charge from the piezoelectric layer and configured to apply the second electric charge to the piezoelectric layer; and

a mechanical support layer connected to the first electrode; and

an interior support structure disposed within the cavity and connected to the substrate and the membrane, wherein the interior support structure contacts the edge support structure; and

control logic electrically coupled to the plurality of PMUT devices, the control logic for sensing an image.

**29.** The image sensing system of claim **28**, wherein the second electrode extends into the cavity and defines an area between the edge support structure and the interior support structure.

**30.** The image sensing system of claim **29**, wherein at least one of the first electrode and the second electrode is electrically coupled through the interior support structure.

\* \* \* \* \*

专利名称(译)	压电微机械超声换能器 ( PMUT )		
公开(公告)号	<a href="#">US10656255</a>	公开(公告)日	2020-05-19
申请号	US15/205743	申请日	2016-07-08
[标]申请(专利权)人(译)	因文森斯公司		
申请(专利权)人(译)	InvenSense公司 , INC.		
当前申请(专利权)人(译)	InvenSense公司 , INC.		
[标]发明人	NG ELDWIN TSAI JULIUS MING LIN APTE NIKHIL		
发明人	NG, ELDWIN TSAI, JULIUS MING-LIN APTE, NIKHIL		
IPC分类号	H01L41/047 G01S7/521 H01L41/09 A61B5/1172 A61B8/00 G01S15/89 B06B1/06		
CPC分类号	A61B5/1172 B06B1/0622 A61B8/4483 H01L41/0973 G01S7/521 H01L41/047 G01S15/89 B06B1/0688		
优先权	62/331919 2016-05-04 US		
其他公开文献	US20170322290A1		
外部链接	<a href="#">Espacenet</a>		

### 摘要(译)

提供了一种压电微机械超声换能器 ( PMUT )。 PMUT包括基板和连接到基板的边缘支撑结构。膜片连接到边缘支撑结构，使得在膜片和基底之间限定空腔，其中膜片被配置为允许以超声频率运动。该膜片包括压电层和耦合到压电层的相对侧的第一和第二电极。内部支撑结构设置在空腔内并连接至基底和膜。

