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(54) **ULTRASONIC TRANSDUCERS IN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) WAFERS AND RELATED APPARATUS AND METHODS**

ULTRASCHALLWANDLER IN CMOS-HALBLEITERWAFERN UND ZUGEHÖRIGE VORRICHTUNG UND VERFAHREN

TRANSDUCTEURS ULTRASONIQUES DANS DES TRANCHES DE SEMI-CONDUCTEUR À OXYDE DE MÉTAL COMPLÉMENTAIRE (CMOS) AINSI QU'APPAREIL ET PROCÉDÉS ASSOCIÉS

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Description

BACKGROUND

Field

[0001] The technology described herein relates to micromachined ultrasonic transducers and related apparatus and methods.

Related Art

[0002] Capacitive Micromachined Ultrasonic Transducers (CMUTs) are known devices that include a membrane above a micromachined cavity. The membrane may be used to transduce an acoustic signal into an electric signal, or vice versa. Thus, CMUTs can operate as ultrasonic transducers.

[0003] Two types of processes can be used to fabricate CMUTs. Sacrificial layer processes form the membrane of the CMUT on a substrate above a sacrificial layer which is then removed to form the cavity of the CMUT beneath the membrane. Wafer bonding processes bond two wafers together to form a cavity with a membrane.

[0004] US 2007/0167811 A1 discloses a first integrated circuit/transducer device of a handheld probe which includes CMOS circuits and CMUT elements. The CMUT elements function to generate an ultrasonic beam, detect an ultrasonic echo and output electrical signals, while the CMOS circuits function to perform analog or digital operations on the electrical signals generated through operation of the CMUT elements. The manufacturing method for the first integrated circuits/transducer device of the preferred embodiment includes the steps of depositing the lower electrode, depositing a sacrificial layer, depositing a dielectric layer; depositing the upper electrode; depositing a protective layer on the upper electrode; and removing the sacrificial layer. In the preferred embodiment, the manufacturing method also includes the step of depositing a sealant layer to seal a cavity between the lower electrode and the upper electrode.

[0005] In the paper entitled "A 32 x 32 Capacitive Micromachined Ultrasonic Transducer Array Manufactured in the Standard CMOS", the authors disclose a 32 x 32 ultrasound array prototype, manufactured using a CMUT-in-CMOS approach whereby ultrasonic transducer elements and readout circuits are integrated on a single chip using a standard integrated circuit manufacturing process in a commercial CMOS foundry. Only blanket wet-etch and sealing steps are added to complete the MEMS devices after the CMOS process. The process typically yields better than 99% working elements per array, with less than $\pm$1.5 dB variation in receive sensitivity among the 1024individually addressable elements. The CMUT pulse-echo frequency response is typically centered at 2.1 MHz with a -6 dB fractional bandwith of 60%, and elements are arranged on a 250 μm hexagonal grid (less than half-wavelength pitch). Multiplexers and CMOS buffers within the array are used to make on-chip routing manageable, reduce the number of physical output leads, and drive the transducer cable. The array has been interfaced to a commercial imager as well as a set of custom transmit and receive electronic, and volumetric images of nylon fishing line targets have been produced.

[0006] In the paper entitled "Dual-bottom-electrode CMUT Base on Standard CMOS Process", the authors disclose a capacitive micromachined ultrasonic transducer (CMUT) with dual-bottom-electrode based on standard CMOS and post-CMOS processes is presented. Compared to the traditional CMUT with single-bottom-electrode, the presented one has larger equivalent gap in the emission and smaller air gap in the reception for the membrane is biased much closed to the bottom electrode. A structure model is proposed for the present CMUT and finite element analysis (FEA) is carried out by commercial software ANSYS. Based on the simulation results, it is shown a 5.655dB improvement in maximum output pressure at 914 kHz without collapse, and a 9.3% improvement in maximum receive sensitivity for the presented CMUT compared with the traditional structure.

[0007] In the paper entitled "Investigation of Thermal Stress Influence on CMUT in Standard CMOS Process", the authors disclose a capacitive micromachined ultrasonic transducer (CMUT) fabricated in standard CMOS and post-SMOS processes which undergoes a series of thermal process at about 1000°C. Thermal stress is generated in the membrane during such process. This paper studies the most severe influence of thermal stress on the performance of CMUT, such as stiffness, collapse voltage, resonant frequency, transformer ratio, coupling coefficient, sensitivity, and bandwidth for the worst-case design, assuming no thermal stress relief by annealing. A membrane in the shape of square microbridge is modelled and some finite element analysis (FEA) is carried out using ANSYS 11.0. A convex membrane with the deformation up to 17% of the initial air gap is obtained in the worst case. Then the influence of thermal stress is investigated based in the comparison between ideal and deformed membrane.

[0008] US 2013/0161702 A1 discloses an integrated MEMS device is provided, including, from bottom up, a bonding wafer layer, a bonding layer, an aluminium layer, a CMOS substrate layer defining a large back chamber area (LBCA), a small back chamber area (SBCA) and a sound damping path (SDP), a set of CMOS wells, a field oxide (FOX) layer, a set of CMOS transistor sources/drains, a first polysilicon layer forming CMOS transistor gates, a second polysilicon layer, said CMOS wells, said CMOS transistor sources/drains and said CMOS gates forming CMOS transistors, an oxide layer embedded with a plurality of metal layers interleaved with a plurality of via hole layers, and a gap control layer, an oxide layer, a first Nitride deposition layer, a metal deposition layer, a second Nitride deposition layer, an under bump metal (UBM) layer made of preferably A1/NiV/Cu and a plurality of solder spheres.

SUMMARY OF THE INVENTION

[0009] The present invention provides a complementary metal oxide semiconductor (CMOS) wafer, according to claim 1.

[0010] The present invention also provides a method according to claim 12.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

FIG. 1 illustrates a capacitive micromachined ultrasonic transducer (CMUT) formed in a CMOS wafer and integrated with a CMOS IC to form a CUT, according to a non-limiting embodiment of the present application.

FIG. 2 is a flowchart illustrating a process of fabricating a CMUT in a CMOS wafer, according to a non-limiting embodiment of the present application.

FIGs. 3A-3J illustrate a fabrication sequence for fabricating a CMUT in a CMOS wafer consistent with the process of FIG. 2, according to a non-limiting embodiment of the present application.

DETAILED DESCRIPTION

[0012] Aspects of the present technology provide micromachined ultrasonic transducers (e.g., CMUTs) in complementary metal oxide semiconductor (CMOS) wafers, utilizing a removed metallization of the CMOS wafer as an acoustic cavity for one or more micromachined ultrasonic transducers. Accordingly, the ultrasonic transducers may be integrated with the CMOS wafers and formed in the wafers, avoiding any requirement for wafer bonding to fabricate ultrasonic transducers. Integration of the ultrasonic transducers with the CMOS wafers may therefore be simplified and made more robust compared to if wafer bonding was used. Moreover, use of a removed CMOS metallization layer as the cavity of an ultrasonic transducer may facilitate formation of integrated circuits (ICs) on the CMOS wafer beneath the ultrasonic transducer, thus reducing or minimizing the space on the CMOS wafer needed to form integrated ultrasonic transducers and integrated circuits. As a result, compact complementary metal oxide semiconductor (CMOS) ultrasonic transducers (CUTs) having monolithically integrated ultrasonic transducers and CMOS ICs may be formed in accordance with some embodiments.

[0013] According to an aspect of the technology, a complementary metal oxide semiconductor (CMOS) wafer comprises a semiconductor substrate and an ultrasonic transducer. The ultrasonic transducer comprises a cavity representing a removed first metallization layer of the CMOS wafer, an electrode disposed between the cavity and the semiconductor substrate, and an acoustic membrane of the CMOS wafer comprising a dielectric layer and a second metallization layer of the CMOS wafer. The cavity may be disposed between the semiconductor substrate and the acoustic membrane. The CMOS wafer may further comprise integrated circuitry on the semiconductor substrate, coupled to the ultrasonic transducer and configured to control operation of the ultrasonic transducer.

[0014] According to an aspect of the present technology, an apparatus comprises an ultrasonic transducer in a complementary metal oxide semiconductor (CMOS) wafer for which a removed portion of a metallization layer defines at least part of an acoustic cavity of the ultrasonic transducer.

[0015] According to an aspect of the present technology, a complementary metal oxide semiconductor (CMOS) wafer comprises a semiconductor substrate, a first metallization layer, and an ultrasonic transducer. The ultrasonic transducer comprises a cavity formed in the first metallization layer, an electrode disposed between the cavity and the semiconductor substrate, and an acoustic membrane of the CMOS wafer comprising a dielectric layer and a second metallization layer of the CMOS wafer. The cavity may be disposed between the semiconductor substrate and the acoustic membrane. The CMOS wafer further comprises integrated circuitry on the semiconductor substrate, coupled to the ultrasonic transducer and configured to control operation of the ultrasonic transducer.

[0016] According to an aspect of the technology, a method comprises forming an acoustic membrane of an ultrasonic transducer in a complementary metal oxide semiconductor (CMOS) wafer by stacking multiple layers of the CMOS wafer including at least one dielectric layer and a first metallization layer of the CMOS wafer. The method further comprises creating at least one access hole to a second metallization layer of the CMOS wafer, the second metallization layer comprising an inner metal layer bounded by first and second conductive liner layers, which in some embodiments include a metal. The method further comprises forming a cavity in the CMOS wafer by removing at least a portion of the inner metal layer of the first metallization layer through the at least one access hole using a selective etch, thereby releasing the acoustic membrane while substantially retaining the first and second conductive liner layers. The method further comprises sealing the at least one access hole with an insulating material, and coupling the first and second conductive liner layers to integrated circuitry of the CMOS wafer.

[0017] According to an aspect of the present application, a method comprises defining at least in part an acoustic cavity of an ultrasonic transducer in a comple-

mentary metal oxide semiconductor (CMOS) wafer by removing at least part of a metallization layer of the CMOS wafer.

[0018] Aspects of the present technology arise from Applicants' appreciation that certain feature dimensions of standard CMOS wafers substantially correspond to certain target feature dimensions of ultrasonic transducers for at least some applications, and thus that ultrasonic transducers may be fabricated in CMOS wafers by taking advantage of such correspondence. That is, Applicants have appreciated that at least some metallization layers of CMOS wafers have thicknesses substantially matching target cavity depths of ultrasonic transducers. Applicants have also appreciated that the thickness of layers of a CMOS wafer overlying the metallization layer substantially matches target membrane thicknesses of ultrasonic transducers. Thus, Applicants have appreciated that ultrasonic transducers may be fabricated in (and therefore integrated with) CMOS wafers by utilizing an appropriately dimensioned CMOS metallization layer as a sacrificial layer to be released to define the cavity of the ultrasonic transducer. Such fabrication provides a simple and robust manner of attaining a high degree of integration of an ultrasonic transducer with a CMOS wafer. Thus, aspects of the present application may facilitate transducer with a CMOS wafer. Thus, aspects of the present application may facilitate formation of ultrasound system-on-a-chip devices having integrated ultrasonic transducers and circuitry.

[0019] Moreover, Applicants have appreciated that using a sacrificial CMOS metallization layer having appropriately situated liner layers may further simplify fabrication of an ultrasonic transducer in a CMOS wafer. By removing only the inner metal of the sacrificial CMOS metallization layer, the remaining liner layers may serve as electrodes for the ultrasonic transducer, obviating any need for further processing to create the electrodes. In this sense, the ultrasonic transducer electrodes are already "built in" to the CMOS metallization layer.

[0020] Accordingly, aspects of the present technology provide micromachined ultrasonic transducers (e.g., CMUTs) in CMOS wafers, utilizing a removed metallization of the CMOS wafer as an acoustic cavity for one or more micromachined ultrasonic transducers. The metallization may represent a signal line metallization for routing signals on the CMOS wafer, and portions of the metallization layer which do not need to be removed to form an acoustic cavity of an ultrasonic transducer may be retained on the CMOS wafer and configured as a signal line. The metallization layer may have a multi-layer configuration, including an inner metal and one or more liner layers. In some embodiments, the inner metal may be removed to form the acoustic cavity, while the liner layers may be retained and configured as electrodes of the ultrasonic transducer.

[0021] According to an aspect of the present technology, a sacrificial release technique is utilized to remove a CMOS metallization layer from a CMOS wafer to create an acoustic cavity of an ultrasonic transducer formed in the CMOS wafer. The metallization targeted with the sacrificial release may have a thickness substantially corresponding to a target depth of the acoustic cavity. In some embodiments, the ultrasonic transducer may be substantially completed prior to the sacrificial release being performed, such that the sacrificial release may complete (or nearly complete) formation of the ultrasonic transducer. Integrated circuitry may optionally be formed in the CMOS wafer beneath the ultrasonic transducer, and in some embodiments may be configured to control operation of the ultrasonic transducer.

[0022] The aspects and embodiments described above, as well as additional aspects and embodiments, are described further below. These aspects and/or embodiments may be used individually, all together, or in any combination of two or more, as the application is not limited in this respect.

[0023] According to an aspect of the present technology, a CMOS wafer includes one or more ultrasonic transducers formed therein, for which a partially or completely removed metallization layer of the CMOS wafer defines at least in part a cavity of the ultrasonic transducer(s). FIG. 1 illustrates a non-limiting example of such a device.

[0024] As shown, the device 100 includes a CMOS wafer 102, with an ultrasonic transducer 104 formed in the CMOS wafer 102. A single ultrasonic transducer 104 is illustrated, but it should be appreciated that aspects of the present application provide for a plurality of ultrasonic transducers in a CMOS wafer, and thus FIG. 1 is a non-limiting illustration. Such a configuration may facilitate formation of an ultrasound system-on-a-chip device or an ultrasound sub-system-on-a-chip device including integrated ultrasonic transducers and circuitry (e.g., analog and/or digital circuitry such as front-end and/or back-end circuitry for controlling operation of the ultrasonic transducers and/or processing signals produced by such transducers, for example to form and/or display ultrasound images). In at least some embodiments, an ultrasound system-on-a-chip device may include, on a single substrate, an arrangement of ultrasonic transducers integrated with analog and digital circuitry, and may be capable of performing ultrasound imaging functions such as emitting and receiving ultrasound waves and processing received ultrasound waves to produce ultrasound images.

[0025] The CMOS wafer 102 includes a polysilicon layer 105, a plurality of metallization layers 106a-106d, and a removed metallization layer defining at least in part an acoustic cavity 108 of the ultrasonic transducer 104. A membrane 110 of the ultrasonic transducer 104 is formed of a combination of layers of the CMOS wafer 102 remaining above the cavity 108. Integrated circuitry 112 may be formed in the base layer 114, beneath the ultrasonic transducer 104. The integrated circuitry may be CMOS circuitry and may be integrated with the ultrasonic transducer 104 to form a CUT. In the non-limiting exam-

ple shown, the integrated circuitry is directly beneath the ultrasonic transducer 104. The polysilicon layer 105 may form part of the integrated circuitry, for instance representing a gate layer for transistors. In some non-limiting embodiments high voltage wiring lines may be disposed above the cavity, but all circuitry may be positioned beneath the ultrasonic transducer.

[0026] The CMOS wafer 102 may be any suitable CMOS wafer for the formation of CMOS integrated circuitry and including one or more metallization layers. In the illustrated example, the CMOS wafer 102 includes five metallization layers (metallization layers 106a-106d in addition to the removed metallization layer representing the cavity 108), but other numbers may alternatively be used.

[0027] The metallization layers 106a-106d, as well as the removed metallization layer used to form the cavity 108, may be configured as standard CMOS metallization layers for signal routing. Thus, in at least some embodiments they may be substantially planar and may occupy an appropriate portion of a plane within the CMOS wafer for functioning as a signal routing layer. For example, in some embodiments one or more of the metallization layers may occupy substantially an entire plane within the CMOS wafer prior to patterning to define desired signal routing configurations. Moreover, the metallization layers may be formed of any suitable material(s). For example, aluminum (Al), copper (Cu), or other metals may be used.

[0028] In some embodiments, including that illustrated, one or more of the metallization layers may include multiple layers (i.e., a multi-layer configuration), such as an inner metal layer with lower and upper liner (or barrier) layers. In the example of FIG. 1, each of the illustrated metallization layers includes a bottom liner layer (e.g., of titanium nitride (TiN)), a layer of Al, a top liner layer (e.g., of TiN), and a layer of silicon oxynitride (SiON) above the top liner layer to serve as an anti-reflective coating during lithography stages. A multi-layer structure for the metallization which is to be sacrificially removed may be beneficial because the liner layers may be configured and retained as electrodes of the ultrasonic transducer. In this manner, the electrodes of the ultrasonic transducer are formed simply and robustly when initially forming the metallization layer that is to be sacrificially removed. The cavity 108 may be formed by removing only the inner metal layer of the metallization while leaving behind the liner layers. Such selective removal may be achieved using a suitably selective etch process, such as a selective wet etch that is selective for (i.e., etches) the inner metal material of the metallization and which is non-selective for (i.e., does not etch) the material of the liner layers. In this manner, fabrication of the cavity is also simplified in that a timed etch is not needed to obtain the desired cavity dimensions. In some embodiments, the etch may be a hydrofluoric acid (HF) etch, although alternatives are possible.

[0029] For example, referring to device 100, the cavity 108 is bounded on the bottom by layer 118 and on the top by layers 120 and 122. The layer 118 may represent a bottom liner layer (e.g., of TiN) of the metallization layer removed to define the cavity 108. The layer 120 may represent a top liner layer (e.g., of TiN) of the removed metallization layer. The layer 122 may represent an anti-reflective coating of the removed metallization layer. Layers 118 and 120 may be configured as electrodes of the ultrasonic transducer 104. Electric connection to the electrodes (for example by one or more remaining metallization layers of the CMOS wafer) may be made by one or more conductive lines (e.g., vias), such as vias 124 and 126, or in any other suitable manner.

[0030] In some embodiments, a multi-layer metallization layer may be configured with an insulating membrane when an inner metal material is removed. For example, the metallization layer may including, in order, TiN-aluminum oxide-Al-aluminum oxide-TiN-SiON, such that when the aluminum is removed an insulating membrane is formed over the TiN electrodes.

[0031] In at least some embodiments, the metallization layer that is at least partially removed to form the cavity of an ultrasonic transducer is in fact not completely removed. In this sense, the removal may be local, rather than global. Portions of the metallization layer may be retained to function as signal lines in areas of the CMOS wafer other than where the acoustic cavity is formed, for example to carry signals of various types applicable to the device 100, such as power, control signals, or sensed signals as non-limiting examples. That is, the same CMOS metallization layer may be used in one or more areas of the CMOS wafer as a signal line and may be removed in other areas of the CMOS wafer to define an acoustic cavity of one or more ultrasonic transducers. Such dual functionality is to be distinguished from depositing a metal on a CMOS wafer solely for the purpose of using the metal as a sacrificial layer.

[0032] FIG. 1 also illustrates that the CMOS wafer 102 includes suitable dielectric or insulating layers between the metallization layers, such as layers 107. These may be formed of any suitable material (e.g., non-conducting, such as SiO_2) and with any suitable thicknesses.

[0033] Sealed access holes 116 are also included. One or more access holes may be formed by suitable etching (e.g., a directional etch, such as a reactive ion etch) to access the metallization layer that is removed to form the cavity 108. The metal material of the metallization layer may be removed through the one or more access holes, for example by selective wet etching (e.g., by HF etch). Subsequently, the access holes may be sealed to create a sealed cavity, as shown, which may be a vacuum cavity in some embodiments, although non-vacuum cavities may also be formed. Any suitable sealant material may be used, a non-limiting example of which is Si_3N_4.

[0034] FIG. 1 illustrates two access holes for the cavity 108. However, it should be appreciated that other numbers (any one or more) may be used. The access holes may be positioned at any suitable location(s) relative to the cavity (e.g., at a periphery as shown, centrally, at

both a periphery and a center, etc.) to allow for sufficient removal of the metal material of the metallization layer to create the cavity. Also, holes may optionally be etched and then optionally filled around the borders of the cavity to provide isolation (e.g., acoustic isolation) between transducers or groups of transducers. In such embodiments, the holes may not pass through the membrane 110 but may optionally extend to the cavity 108.

[0035] In some embodiments, a plurality of access holes may be positioned suitably to allow removal of the metal material of the metallization layer while also being arranged suitably to allow metal signal connections to run across the chip (e.g., between neighboring ultrasonic transducers). As a specific, but non-limiting, example, a plurality of access holes may be arranged at the periphery of a cavity but there may be enough space between at least two of the access holes to allow metal signal lines to interconnect the metallization layers 106d of neighboring ultrasonic transducers. Considering a top view of such a configuration, the cavity may have a circular shape and the plurality of access holes may be formed around the perimeter in a circle, with metal signal lines running between some of the access holes. Alternatives are possible. For example, the described circular cavity shape may alternatively be rectangular, square, hexagonal, or have any other suitable shape.

[0036] The ultrasonic transducer 104 may have any suitable dimensions. The dimensions may be dictated at least in part by an intended application for the transducer, for example to provide desired frequency behavior, desired device size, desired imaging aperture, or other characteristics of interest. Non-limiting examples are provided below.

[0037] In some embodiments, the cavity dimensions and/or the membrane thickness of any membrane overlying the cavity may impact the frequency behavior of the membrane, and thus may be selected to provide a desired frequency behavior (e.g., a desired resonance frequency of the membrane). For example, it may be desired in some embodiments to have an ultrasonic transducer with a center resonance frequency of between approximately 20 kHz and approximately 200 MHz, between approximately 1 MHz and approximately 40 MHz, between approximately 1 MHz and approximately 10 MHz, between approximately 2 MHz and approximately 5 MHz, between approximately 5 MHz and approximately 15 MHz, between approximately 10 MHz and approximately 20 MHz, between approximately 20 MHz and approximately 40 MHz, between approximately 50 kHz and approximately 200 kHz, of approximately 2.5 MHz, approximately 4 MHz, any frequency or range of frequencies in between, or any other suitable frequency. For example, it may be desired to use the devices in air, gas, water, or other environments, for example for medical imaging, materials analysis, or for other reasons for which various frequencies of operation may be desired. The dimensions of the cavity and/or membrane may be selected accordingly.

[0038] As non-limiting examples, the width ***W1*** of the cavity 108 may be between approximately 5 microns and approximately 500 microns, between approximately 20 microns and approximately 100 microns, may be approximately 30 microns, approximately 40 microns, approximately 50 microns, any width or range of widths in between, or any other suitable width. In some embodiments, the width may be selected to maximize the void fraction, i.e., the amount of area consumed by the cavity compared to the amount of area consumed by surrounding structures. The width dimension may also be used to identify the aperture size of the cavity, and thus the cavities may have apertures of any of the values described above or any other suitable values.

[0039] The cavity 108 may have a depth ***D1,*** which may be between approximately 0.05 microns and approximately 10 microns, between approximately 0.1 microns and approximately 5 microns, between approximately 0.5 microns and approximately 1.5 microns, any depth or range of depths in between, or any other suitable depth. As previously described, Applicants have appreciated that the thickness of some metallization layers used in standard CMOS wafers may substantially correspond to target depths of the acoustic cavity, and thus the depth of the cavity 108 may be defined at least in part by the thickness of the metallization layer used as the sacrificial layer. For instance, in one embodiment the depth ***D1*** may be approximately ¼ micron, which may substantially correspond to a metallization thickness offered on CMOS wafers.

[0040] The membrane 110 may comprise one or more layers and/or structures of the CMOS wafer 102 defining a thickness ***Tm.*** In the non-limiting example of FIG. 1, the membrane 110 includes vias (e.g., vias 126), metal layers (e.g., metallization layer 106d), and dielectric or insulating layers (e.g., layers 107). A passivation layer 128 (e.g., formed of Si_3N_4) passivates the surface. The thickness ***Tm*** (e.g., as measured in the direction generally parallel to the depth ***D1***) may be less than 100 microns, less than 50 microns, less than 40 microns, less than 30 microns, less than 20 microns, less than 10 microns, less than 5 microns, less than 1 micron, less than 0.1 microns, any range of thicknesses in between (e.g., between approximately 1-5 microns, between approximately 1-2 microns, etc.), or any other suitable thickness. The thickness may be selected in some embodiments based on a desired acoustic behavior of the membrane, such as a desired resonance frequency of the membrane. Moreover, Applicants have appreciated that for some standard CMOS wafers, using the metallization layer beneath the top metallization layer as the sacrificial layer for defining the ultrasonic transducer cavity results in the overlying membrane 110 having approximately (and in some cases, substantially) the target thickness for the ultrasonic transducer (e.g., between approximately 1-2 microns). Thus, use of the metallization layer beneath the top metallization layer as the sacrificial layer can significantly simplify fabrication of the ultrasonic

transducers in the CMOS wafer.

[0041] The thickness ***Tm*** may be adjusted by adding/removing material from the upper surface of the membrane. Removal of such material may be accomplished using chemical mechanical polishing (CMP), any form of etching including selective etch, directional etch, wet etch, or laser etch, or any other suitable technique. Furthermore, in some embodiments, the membrane may have a non-uniform thickness, for example being thicker in a center portion over the cavity and thinner above the periphery of the cavity, to form a piston structure. Such structures may provide control over the operating frequency of the ultrasonic transducer.

[0042] As a non-limiting example of suitable dimensions of the cavity depth and width and the membrane thickness, in one embodiment the depth ***D1*** may be approximately ¼ micron, the width ***W1*** may be approximately 50 microns, and the thickness ***Tm*** of the membrane 110 may be approximately 1-2 microns. Alternatives are possible.

[0043] The integrated circuit 112 may be formed in the base layer 114 of the CMOS wafer 102. For example, the base layer 114 may be a bulk silicon layer or other semiconductor substrate, and the integrated circuit 112 may include one or more active silicon circuit elements (e.g., MOS transistors having doped source and drain regions in the silicon), capacitors, resistors, or other circuit components. The integrated circuit 112 may be suitable to operate the ultrasonic transducer 104 in transmit and/or receive modes.

[0044] As shown, the ultrasonic transducer 104 may be connected to the IC 112, for example by the illustrated connection of the layer 118 to the via 124. Other manners of making connection are possible.

[0045] According to an aspect of the present technology, a method of fabricating an ultrasonic transducer in a CMOS wafer is provided, involving removing at least a portion of a metallization layer of the CMOS wafer to create a cavity of the ultrasonic transducer. FIG. 2 is a flowchart illustrating an example of the method.

[0046] The method 200 includes, at stage 202, preparation of a CMOS wafer. The CMOS wafer includes at least one metallization layer and structures defining in part an ultrasonic transducer. For example, electrodes and an acoustic membrane may be formed, such as electrodes defined by metallization liner layers and an acoustic membrane of the type represented by acoustic membrane 110 of FIG. 1.

[0047] At stage 204 one or more access holes are formed to a metallization layer of the CMOS wafer. As previously described in connection with FIG. 1, the access holes may be created in any suitable manner (e.g., a directional etch) and may be positioned at any suitable location(s) relative to the ultrasonic transducer, including at a periphery and/or center of the area which is to become the cavity of the ultrasonic transducer.

[0048] At stage 206, the cavity of the ultrasonic transducer may be created in the CMOS wafer by removing at least part of the metallization layer using a suitable etch technique. For example, a selective etch may be used that is selective for the material (e.g., metal) of the metallization layer to be removed. The removal may be local in some embodiments, but not global. That is, the metallization layer may be removed in the area of the CMOS wafer in which the ultrasonic transducer is located, but may be retained in other areas of the CMOS wafer, for example as a signal line.

[0049] At stage 208, the access holes formed in stage 204 may be sealed, to create a sealed ultrasonic transducer cavity. The access holes may be sealed in any suitable manner using any suitable material, such as an insulating material. In some embodiments, a plasma enhanced chemical vapor deposition (PECVD) may be performed to seal the access holes. For example, PECVD Si_3N_4 may be used in some embodiments, which may minimize lateral intrusion of the sealing material into the cavity.

[0050] The method 200 may be performed at the wafer level, as should be appreciated by the reference to a CMOS wafer throughout FIG. 2. Thus, multiple ultrasonic transducers may be formed in the CMOS wafer, in arrays or other arrangements. One benefit of such a fabrication technique is that large numbers of ultrasonic transducers (e.g., CMUTs) may be formed on a single wafer in a relatively simple, cost-effective manner. Such technology may therefore facilitate fabrication of ultrasound system-on-a-chip devices utilizing arrays (or other arrangements) of micromachined ultrasonic transducers.

[0051] It should be appreciated that the stages of method 200 may be performed by different parties in some embodiments. For example, one party in the business of fabricating CMOS wafers may perform stage 202. A second party (e.g., a purchaser of the CMOS wafer) may then perform stages 204, 206, and 208. In other embodiments, a single entity may perform all stages of the method.

[0052] FIGs. 3A-3J illustrate a fabrication sequence for fabricating a CMUT in a CMOS wafer consistent with the process of FIG. 2, according to a non-limiting embodiment of the present application. The starting point for the sequence is shown in FIG. 3A, and includes the base layer 114, patterned polysilicon layer 105, metallization layer 106a, and metallization layer 106b, with layers 107.

[0053] As shown in FIGs. 3B-3D, the via 124 of FIG. 1 (shown completed below in FIG. 3D) may be formed. In anticipation of forming the via, as shown in FIG. 3B, the uppermost layer 107 may be suitably etched and a conductive layer 302 may be deposited. The conductive layer 302 may be formed of a desired via material, such as tungsten (W). A liner material (e.g., TiN) may be deposited prior to the tungsten, and thus the conductive layer 302 may have a multi-layer configuration as shown.

[0054] As shown in FIG. 3C, the conductive layer 302 may be planarized (e.g., using CMP), and then metallization layer 106c may be formed and patterned. A dielectric or insulating layer 304 (e.g., SiO_2) may be formed

over the surface.

[0055] As shown in FIG. 3D, the dielectric layer 304 may be patterned to allow formation of vias 124. The vias 124 may be formed of a desired via material, such as tungsten (W). A liner material (e.g., TiN) may be deposited prior to the tungsten, giving rise to the multi-layer features of vias 124 illustrated.

[0056] Then, in FIG. 3E, a metallization layer 306 is formed. The metallization layer 306 may represent the sacrificial metallization layer from which the cavity 108 of FIG. 1 (and also shown in FIG. 3I) is to be formed. Thus, the previously described layers 118, 120, and 122 are included. A dielectric or insulating layer (e.g., SiO_2) 308 may be formed on the uppermost surface.

[0057] In FIG. 3F the dielectric layer 308 may be patterned and a conductive layer 310 deposited in anticipation of forming vias 126 from FIG. 1 (also shown in FIG. 3G). The conductive layer 310 may be formed of a desired via material, such as tungsten (W). A liner material (e.g., TiN) may be deposited prior to the tungsten, and thus the conductive layer 310 may have a multi-layer configuration as shown.

[0058] As shown in FIG. 3G, the conductive layer 310 may be planarized to form vias 126 and metallization layer 106d may be formed and patterned. A dielectric or insulating layer 312 may be formed on the uppermost surface of the structure.

[0059] In FIG. 3H a passivation layer (e.g., of Si_3N_4) 313 may be formed and access holes 314 may be formed to the metallization layer 306. A suitable etch process may be used to form the access holes.

[0060] Then, as shown in FIG. 3I, the cavity 108 may be created by removing at least a portion of the metallization layer 306 via the access holes 314. For example, the metallization layer may include an inner metal layer which is selectively etched (for example by wet etch, such as HF etch), leaving behind the layers 118 and 120.

[0061] In FIG. 3J the access holes 314 may be sealed with a suitable sealant layer 316. The sealant layer may comprise a passivating material, such as Si_3N_4. Other materials are also possible. Thus, the device 100 of FIG. 1 may be achieved through this fabrication sequence.

[0062] While FIGs. 3A-3J illustrate a fabrication sequence suitable for use with aluminum metallization layers, it should be appreciated that the various aspects described herein are not limited in this respect. For example, aspects of the present technology may utilize copper metallization layers instead of aluminum. In some embodiments, copper lined with tantalum may be used.

[0063] Also, while aspects of the present application have been described as utilizing multi-layer metallization layers of CMOS wafers to define a cavity of an ultrasonic transducer, an alternative may utilize metal-insulator-metal (MIM) layers instead. For example, the insulator of a MIM layer may be removed from between adjacent metal layers in the manner described herein with respect to removing an inner metal material of a metallization layer.

[0064] Moreover, according to some embodiments, an ultrasonic transducer may be formed without metal liner layers configured as electrodes adjacent the cavity of the transducer. For example, referring to FIG. 1, in an alternative embodiment the layers 118 and 120 (and also 122) may be omitted, and instead the vias 126 may be disposed suitably to operate in combination as an electrode. For example, the vias 126 may be spaced relative to each other by between approximately 0.1 micron and approximately 0.5 microns (e.g., between approximately 0.2 microns and approximately 0.3 microns). An array of such vias may be operated in combination as an electrode for controlling operation of the ultrasonic transducer. In such embodiments, the vias may have any suitable dimensions, non-limiting examples of which are approximately 0.2 microns $\times$ 0.2 microns in cross-section, approximately 0.3 $\times$ microns 0.3 microns in cross-section, or any other suitable dimensions.

[0065] Aspects of the present application may be used to build ultrasound devices such as ultrasound probes. The probes may be suitable for imaging a variety of subjects. Ultrasound probes in accordance with some embodiments may include a variety of front-end and/or back-end electronics. In some embodiments, the probes may be ultrasound system-on-a-chip devices.

[0066] The aspects of the present application may provide one or more benefits, some of which have been previously described. Now described are some non-limiting examples of such benefits. It should be appreciated that not all aspects and embodiments necessarily provide all of the benefits now described. Further, it should be appreciated that aspects of the present application may provide additional benefits to those now described.

[0067] Aspects of the present application provide manufacturing processes suitable for formation of monolithically integrated ultrasonic transducers and CMOS structures (e.g., CMOS ICs). In at least some embodiments, the processes may be simple, robust, relatively inexpensive to perform, and may be scalable to large quantities of ultrasonic transducers. The difficulties associated with wafer bonding, such as poor bond strength, low yield, and the use of high temperature anneals may be avoided. Aspects of the present application provide processes for manufacturing suitably sized ultrasonic transducers for operation in connection with low voltage CMOS ICs. Other benefits may also be provided in accordance with one or more aspects of the present application.

[0068] Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the scope of the technology described in the application. For example, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such varia-

tions and/or modifications is deemed to be within the scope of the embodiments described herein. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described. In addition, any combination of two or more features, systems, articles, materials, kits, and/or methods described herein, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present disclosure.

[0069] Also, as described, some aspects may be embodied as one or more methods. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0070] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0071] The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

[0072] The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, i.e., "one or more" of the elements so conjoined. Elements other than those specifically identified by the "and/or" clause may optionally be present, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

[0073] As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

[0074] Also, the phraseology and terminology used herein is for the purpose of description and should not be regarded as limiting. The use of "including," "comprising," or "having," "containing," "involving," and variations thereof herein, is meant to encompass the items listed thereafter and equivalents thereof as well as additional items.

[0075] In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of' and "consisting essentially of' shall be closed or semi-closed transitional phrases, respectively.

Claims

1. A complementary metal oxide semiconductor (CMOS) wafer (102), comprising:

a semiconductor substrate (114);
an ultrasonic transducer (104) comprising

a cavity (108) defined by the partial removal of a first metallization layer (306) of the CMOS wafer (102);
an electrode (118) disposed between the cavity (108) and the semiconductor substrate (114); and
an acoustic membrane (110) of the CMOS wafer (102) comprising a dielectric layer (107) and a second metallization layer (106d) of the CMOS wafer (102), the cavity (108) being disposed between the semiconductor substrate (114) and the acoustic membrane (110); and

integrated circuitry (112) on the semiconductor substrate (114), coupled to the ultrasonic transducer (104) and configured to control operation of the ultrasonic transducer (104);

wherein the electrode (118) disposed between the cavity (108) and the semiconductor substrate (114) is a first electrode of the ultrasonic transducer (104), and wherein the ultrasonic transducer (104) further comprises a second electrode (120) disposed opposite the first electrode (118), the second electrode (120) disposed in the acoustic membrane (110) between the cavity (108) and the second mettalization layer (106d).

2. The CMOS wafer (102) of claim 1, wherein the electrode (118) disposed between the cavity (108) and the semiconductor substrate (114) represents a liner layer of the partially removed first metallization layer (306) of the CMOS wafer (102) .

3. The CMOS wafer of claim 1, wherein the electrode (118) disposed between the cavity (108) and the semiconductor substrate (114) is a bottom electrode of the ultrasonic transducer (104), and wherein the electrode (120) disposed in the acoustic membrane (110) between the cavity (108) and the second metalization layer (106d) is a top electrode of the ultrasonic transducer (104), with the cavity (108) being disposed between the bottom electrode (118) and the top electrode (120), and wherein the bottom and top electrodes represent liner layers of the partially removed first metallization layer (306) of the CMOS wafer (102).

4. The CMOS wafer (102) of claim 1, wherein the acoustic membrane (110) of the CMOS wafer (102) comprises one or more conductive vias (124; 126).

5. The CMOS wafer (102) of claim 4, wherein at least one of the one or more conductive vias (124; 126) of the acoustic membrane (110) is electrically connected to the second electrode (120).

6. The CMOS wafer (102) of claim 1, further comprising at least one filled access hole (116) passing through at least part of the acoustic membrane (110) to the cavity (108).

7. The CMOS wafer (102) of claim 1, comprising a plurality of ultrasonic transducers including the ultrasonic transducer (104) .

8. The CMOS wafer (102) of claim 1, wherein the second metallization layer (106d) is embedded within the dielectric layer (107) of the acoustic membrane (110).

9. The CMOS wafer (102) of claim 1, further comprising at least one hole (116) positioned to not pass through the acoustic membrane (110).

10. The complementary metal oxide semiconductor (CMOS) wafer (102) of claim 1, wherein the first metallization layer (306) is configured to transmit electrical signals in a peripheral area of the substrate (114).

11. The complementary metal oxide semiconductor (CMOS) wafer (102) of claim 1, wherein the first metallization layer (306) has a plurality of cavities formed therein, and wherein each cavity (108) corresponds to a different ultrasonic transducer (104) .

12. A method, comprising:

forming an acoustic membrane (110) of an ultrasonic transducer (104) in a complementary metal oxide semiconductor (CMOS) wafer (102) by stacking multiple layers of the CMOS wafer (102) including at least one dielectric layer (107) and first and second metallization layers (306, 106d) of the CMOS wafer (102);
forming at least one access hole (116) to the second metallization layer (106d) of the CMOS wafer (102), the second metallization layer (106d) comprising an inner metal layer bounded by first and second conductive liner layers (118; 120);
forming a cavity (108) in the CMOS wafer (102) by removing at least a portion of the inner metal layer of the first metallization layer (306) through the at least one access hole (116) using a selective etch, thereby releasing the acoustic membrane (110) comprising the dielectric layer (107) and the second metallization layer (106d) of the CMOS wafer (102), while substantially retaining the first and second conductive liner layers (118; 120) and configuring the retained lines layers as electrodes of the ultrasonic transducer (104);
sealing the at least one access hole with an insulating material (316); and
coupling the first and second conductive liner layers (118; 120) to integrated circuitry (112) of the CMOS wafer.

13. The method of claim 12, wherein forming the acoustic membrane (110) further comprises coupling the first metallization layer (306) of the CMOS wafer to the first conductive liner layer of the second metallization layer (106d) with one or more conductive vias (126).

14. The method of claim 12, wherein coupling the first and second conductive liner layers (118; 120) to integrated circuitry (112) of the CMOS wafer (102) comprises coupling the first conductive liner layer (118; 120) to integrated circuitry (112) in a semiconductor substrate (114) of the CMOS wafer (102) by one or more conductive vias.

15. The method of claim 12, wherein the inner metal layer comprises aluminum, and wherein using a selective etch comprises using a hydrofluoric acid etch.

Patentansprüche

1. Komplementärer Metalloxid-Halbleiter (CMOS)-Wafer (102), umfassend:

ein Halbleitersubstrat (114);
einen Ultraschallwandler (104), umfassend

einen Hohlraum (108), der durch das teilweise Entfernen einer ersten Metallisierungsschicht (306) des CMOS-Wafers (102) definiert ist;
eine Elektrode (118), die zwischen dem Hohlraum (108) und dem Halbleitersubstrat (114) angeordnet ist; und
eine Akustik-Membran (110) des CMOS-Wafers (102), umfassend eine dielektrische Schicht (107) und eine zweite Metallisierungsschicht (106d) des CMOS-Wafers (102), wobei der Hohlraum (108) zwischen dem Halbleitersubstrat (114) und der Akustik-Membran (110) angeordnet ist; und

einen integrierten Schaltkreis (112) auf dem Halbleitersubstrat (114), der mit dem Ultraschallwandler (104) gekoppelt und konfiguriert ist, den Betrieb des Ultraschallwandlers (104) zu steuern;
wobei die Elektrode (118), die zwischen dem Hohlraum (108) und dem Halbleitersubstrat (114) angeordnet ist, eine erste Elektrode des Ultraschallwandlers (104) ist, und wobei der Ultraschallwandler (104) weiter eine zweite Elektrode (120) umfasst, die gegenüber der ersten Elektrode (118) angeordnet ist, wobei die zweite Elektrode (120) in der Akustik-Membran (110) zwischen dem Hohlraum (108) und der zweiten Metallisierungsschicht (106d) angeordnet ist.

2. CMOS-Wafer (102) nach Anspruch 1, wobei die Elektrode (118), die zwischen dem Hohlraum (108) und dem Halbleitersubstrat (114) angeordnet ist, eine Einlageschicht der teilweise entfernten ersten Metallisierungsschicht (306) des CMOS-Wafers (102) repräsentiert.

3. CMOS-Wafer nach Anspruch 1, wobei die Elektrode (118), die zwischen dem Hohlraum (108) und dem Halbleitersubstrat (114) angeordnet ist, eine untere Elektrode des Ultraschallwandlers (104) ist, und wobei die Elektrode (120), die in der Akustik-Membran (110) zwischen dem Hohlraum (108) und der zweiten Metallisierungsschicht (106d) angeordnet ist, eine obere Elektrode des Ultraschallwandlers (104) ist, wobei der Hohlraum (108) zwischen der unteren Elektrode (118) und der oberen Elektrode (120) angeordnet ist, und wobei die untere und obere Elektrode Einlageschichten der teilweise entfernten ersten Metallisierungsschicht (306) des CMOS-Wafers (102) repräsentieren.

4. CMOS-Wafer (102) nach Anspruch 1, wobei die Akustik-Membran (110) des CMOS-Wafers (102) eine oder mehrere leitende Durchverbindungen (124; 126) umfasst.

5. CMOS-Wafer (102) nach Anspruch 4, wobei zumindest eine von der einen oder den mehreren leitenden Durchverbindungen (124; 126) der Akustik-Membran (110) mit der zweiten Elektrode (120) elektrisch verbunden ist.

6. CMOS-Wafer (102) nach Anspruch 1, weiter zumindest ein volles Zugangsloch (116) umfassend, das durch zumindest einen Teil der Akustik-Membran (110) zu dem Hohlraum (108) durchführt.

7. CMOS-Wafer (102) nach Anspruch 1, umfassend eine Vielzahl von Ultraschallwandlern, die den Ultraschallwandler (104) beinhalten.

8. CMOS-Wafer (102) nach Anspruch 1, wobei die zweite Metallisierungsschicht (106d) innerhalb der dielektrischen Schicht (107) der Akustik-Membran (110) eingebettet ist.

9. CMOS-Wafer (102) nach Anspruch 1, weiter zumindest ein Loch (116) umfassend, das so positioniert ist, dass es nicht durch die Akustik-Membran (110) durchführt.

10. Komplementärer Metalloxid-Halbleiter (CMOS)-Wafer (102) nach Anspruch 1, wobei die erste Metallisierungsschicht (306) konfiguriert ist, elektrische Signale in einem peripheren Bereich des Substrats (114) zu übertragen.

11. Komplementärer Metalloxid-Halbleiter (CMOS)-Wafer (102) nach Anspruch 1, wobei die erste Metallisierungsschicht (306) eine Vielzahl von Hohlräumen aufweist, die darin gebildet sind, und wobei jeder Hohlraum (108) einem anderen Ultraschallwandler (104) entspricht.

12. Verfahren, umfassend:

Bilden einer Akustik-Membran (110) eines Ultraschallwandlers (104) in einem komplementären Metalloxid-Halbleiter (CMOS)-Wafer (102) mittels Stapeln von mehreren Schichten des CMOS-Wafers (102), zumindest eine dielektri-

sche Schicht (107) und erste und zweite Metallisierungsschichten (306, 106d) des CMOS-Wafers (102) beinhaltend;
Bilden zumindest eines Zugangslochs (116) zu der zweiten Metallisierungsschicht (106d) des CMOS-Wafers (102), wobei die zweite Metallisierungsschicht (106d) eine innere Metallschicht umfasst, die von einer ersten und zweiten leitenden Einlageschicht (118; 120) begrenzt wird;
Bilden eines Hohlraums (108) in dem CMOS-Wafer (102) mittels Entfernen zumindest eines Teils der inneren Metallschicht der ersten Metallisierungsschicht (306) durch das zumindest eine Zugangsloch (116) unter Verwendung von selektivem Ätzen, dadurch Freilegen der Akustik-Membran (110), die die dielektrische Schicht (107) und die zweite Metallisierungsschicht (106d) des CMOS-Wafers (102) umfasst, dabei im Wesentlichen Beibehalten der ersten und zweiten leitenden Einlageschichten (118; 120) und Konfigurieren der beibehaltenen Einlageschichten als Elektroden des Ultraschallwandlers (104);
Abdichten des zumindest einen Zugangslochs mit einem Isoliermaterial (316); und
Koppeln der ersten und zweiten leitenden Einlageschichten (118; 120) an den integrierten Schaltkreis (112) des CMOS-Wafers.

13. Verfahren nach Anspruch 12, wobei Bilden der Akustik-Membran (110) weiter Koppeln der ersten Metallisierungsschicht (306) des CMOS-Wafers an die erste leitende Einlageschicht der zweiten Metallisierungsschicht (106d) mit einem oder mehreren leitenden Durchgangslöchern (126) umfasst.

14. Verfahren nach Anspruch 12, wobei Koppeln der ersten und zweiten leitenden Einlageschichten (118; 120) an einen integrierten Schaltkreis (112) des CMOS-Wafers (102) Koppeln der ersten leitenden Einlageschicht (118; 120) an den integrierten Schaltkreis (112) in einem Halbleitersubstrat (114) des CMOS-Wafers (102) mittels einem oder mehreren leitenden Durchgangslöchern umfasst.

15. Verfahren nach Anspruch 12, wobei die innere Metallschicht Aluminium umfasst, und wobei Verwenden von selektivem Ätzen Verwenden von Flusssäure-Ätzen umfasst.

Revendications

1. Tranche de semi-conducteur à oxyde de métal complémentaire (CMOS) (102), comprenant :

un substrat semi-conducteur (114) ;

un transducteur ultrasonique (104) comprenant

une cavité (108) définie par l'élimination partielle d'une première couche de métallisation (306) de la tranche de CMOS (102) ;
une électrode (118) disposée entre la cavité (108) et le substrat semi-conducteur (114) ; et
une membrane acoustique (110) de la tranche de CMOS (102) comprenant une couche diélectrique (107) et une seconde couche de métallisation (106d) de la tranche de CMOS (102), la cavité (108) étant disposée entre le substrat semi-conducteur (114) et la membrane acoustique (110) ; et

un circuit intégré (112) sur le substrat semi-conducteur (114), couplé au transducteur ultrasonique (104) et configuré pour commander le fonctionnement du transducteur ultrasonique (104) ;
dans laquelle l'électrode (118) disposée entre la cavité (108) et le substrat semi-conducteur (114) est une première électrode du transducteur ultrasonique (104), et dans laquelle le transducteur ultrasonique (104) comprend en outre une seconde électrode (120) disposée en face de la première électrode (118), la seconde électrode (120) étant disposée dans la membrane acoustique (110) entre la cavité (108) et la seconde couche de métallisation (106d).

2. Tranche de CMOS (102) selon la revendication 1, dans laquelle l'électrode (118) disposée entre la cavité (108) et le substrat semi-conducteur (114) représente une couche de revêtement de la première couche de métallisation partiellement éliminée (306) de la tranche de CMOS (102).

3. Tranche de CMOS selon la revendication 1, dans laquelle l'électrode (118) disposée entre la cavité (108) et le substrat semi-conducteur (114) est une électrode inférieure du transducteur ultrasonique (104), et dans laquelle l'électrode (120) disposée dans la membrane acoustique (110) entre la cavité (108) et la seconde couche de métallisation (106d) est une électrode supérieure du transducteur ultrasonique (104), la cavité (108) étant disposée entre l'électrode inférieure (118) et l'électrode supérieure (120), et dans laquelle les électrodes inférieure et supérieure représentent des couches de revêtement de la première couche de métallisation partiellement éliminée (306) de la tranche de CMOS (102).

4. Tranche de CMOS (102) selon la revendication 1, dans laquelle la membrane acoustique (110) de la tranche de CMOS (102) comprend un ou plusieurs trous d'interconnexion conducteurs (124 ; 126).

5. Tranche de CMOS (102) selon la revendication 4, dans laquelle au moins un des un ou plusieurs trous d'interconnexion conducteurs (124; 126) de la membrane acoustique (110) est connecté électriquement à la seconde électrode (120).

6. Tranche de CMOS (102) selon la revendication 1, comprenant en outre au moins un trou d'accès rempli (116) passant à travers au moins une partie de la membrane acoustique (110) jusqu'à la cavité (108).

7. Tranche de CMOS (102) selon la revendication 1, comprenant une pluralité de transducteurs ultrasoniques comportant le transducteur ultrasonique (104).

8. Tranche de CMOS (102) selon la revendication 1, dans laquelle la seconde couche de métallisation (106d) est noyée dans la couche diélectrique (107) de la membrane acoustique (110).

9. Tranche de CMOS (102) selon la revendication 1, comprenant en outre au moins un trou (116) placé de manière à ne pas passer à travers la membrane acoustique (110).

10. Tranche de semi-conducteur à oxyde de métal complémentaire (CMOS) (102) selon la revendication 1, dans laquelle la première couche de métallisation (306) est configurée pour transmettre des signaux électriques dans une zone périphérique du substrat (114).

11. Tranche de semi-conducteur à oxyde de métal complémentaire (CMOS) (102) selon la revendication 1, dans laquelle la première couche de métallisation (306) comporte une pluralité de cavités formées dans celle-ci, et dans laquelle chaque cavité (108) correspond à un transducteur ultrasonique (104) différent.

12. Procédé, comprenant :

la formation d'une membrane acoustique (110) d'un transducteur ultrasonique (104) dans une tranche de semi-conducteur à oxyde de métal complémentaire (CMOS) (102) par empilement de plusieurs couches de la tranche de CMOS (102) comportant au moins une couche diélectrique (107) et des première et seconde couches de métallisation (306, 106d) de la tranche de CMOS (102) ;
la formation d'au moins un trou d'accès (116) à la seconde couche de métallisation (106d) de la tranche de CMOS (102), la seconde couche de métallisation (106d) comprenant une couche métallique interne délimitée par des première et seconde couches de revêtement conductrices (118 ; 120) ;
la formation d'une cavité (108) dans la tranche de CMOS (102) par élimination d'au moins une partie de la couche métallique interne de la première couche de métallisation (306) à travers le au moins un trou d'accès (116) en utilisant une gravure sélective, en libérant ainsi la membrane acoustique (110) comprenant la couche diélectrique (107) et la seconde couche de métallisation (106d) de la tranche de CMOS (102), tout en conservant sensiblement les première et seconde couches de revêtement conductrices (118 ; 120) et en configurant les couches de lignes conservées comme des électrodes du transducteur ultrasonique (104) ;
le scellement du au moins un trou d'accès avec un matériau isolant (316) ; et
le couplage des première et seconde couches de revêtement conductrices (118 ; 120) au circuit intégré (112) de la tranche de CMOS.

13. Procédé selon la revendication 12, dans lequel la formation de la membrane acoustique (110) comprend en outre le couplage de la première couche de métallisation (306) de la tranche de CMOS à la première couche de revêtement conductrice de la seconde couche de métallisation (106d) avec un ou plusieurs trous d'interconnexion conducteurs (126).

14. Procédé selon la revendication 12, dans lequel le couplage des première et seconde couches de revêtement conductrices (118 ; 120) au circuit intégré (112) de la tranche de CMOS (102) comprend le couplage de la première couche de revêtement conductrice (118 ; 120) au circuit intégré (112) dans un substrat semi-conducteur (114) de la tranche de CMOS (102) par un ou plusieurs trous d'interconnexion conducteurs.

15. Procédé selon la revendication 12, dans lequel la couche métallique interne comprend de l'aluminium, et dans lequel l'utilisation d'une gravure sélective comprend l'utilisation d'une gravure à l'acide fluorhydrique.

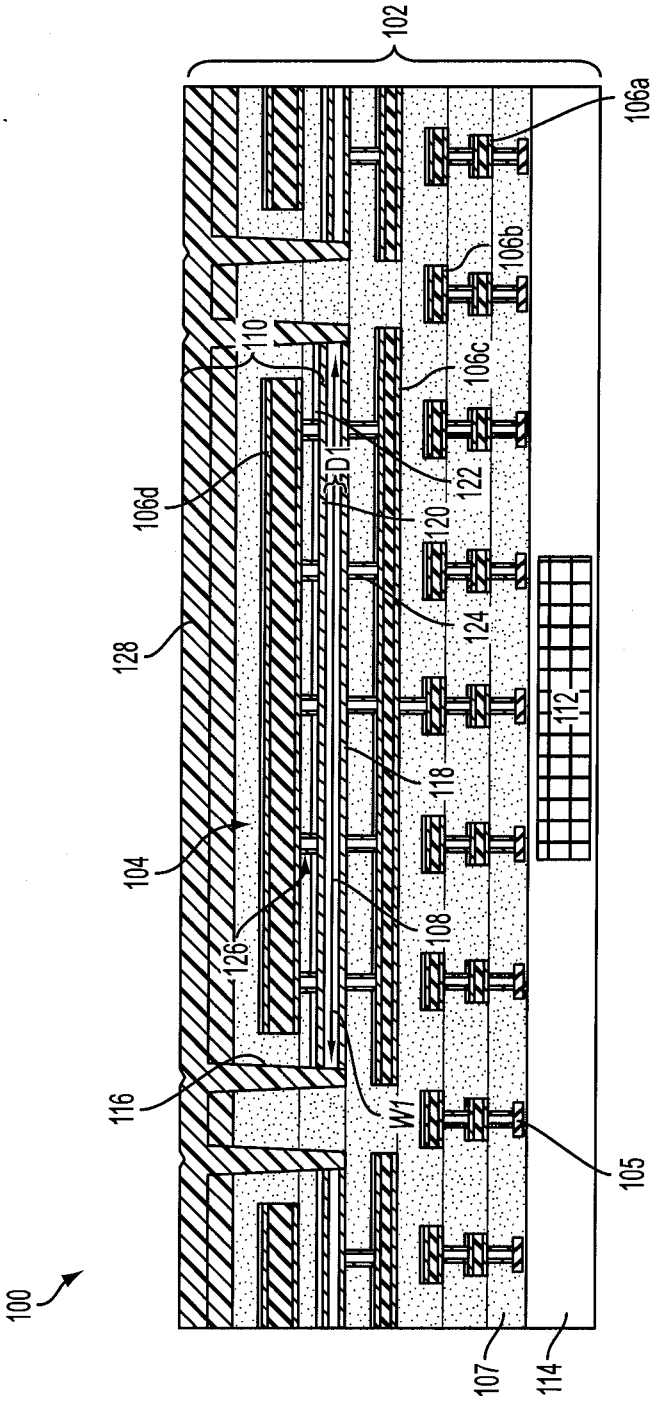
102
106a
106b
106c
106d
110
D1
122
120
124
128
112
118
104
126
108
116
W1
105
100
107
114

FIG. 1

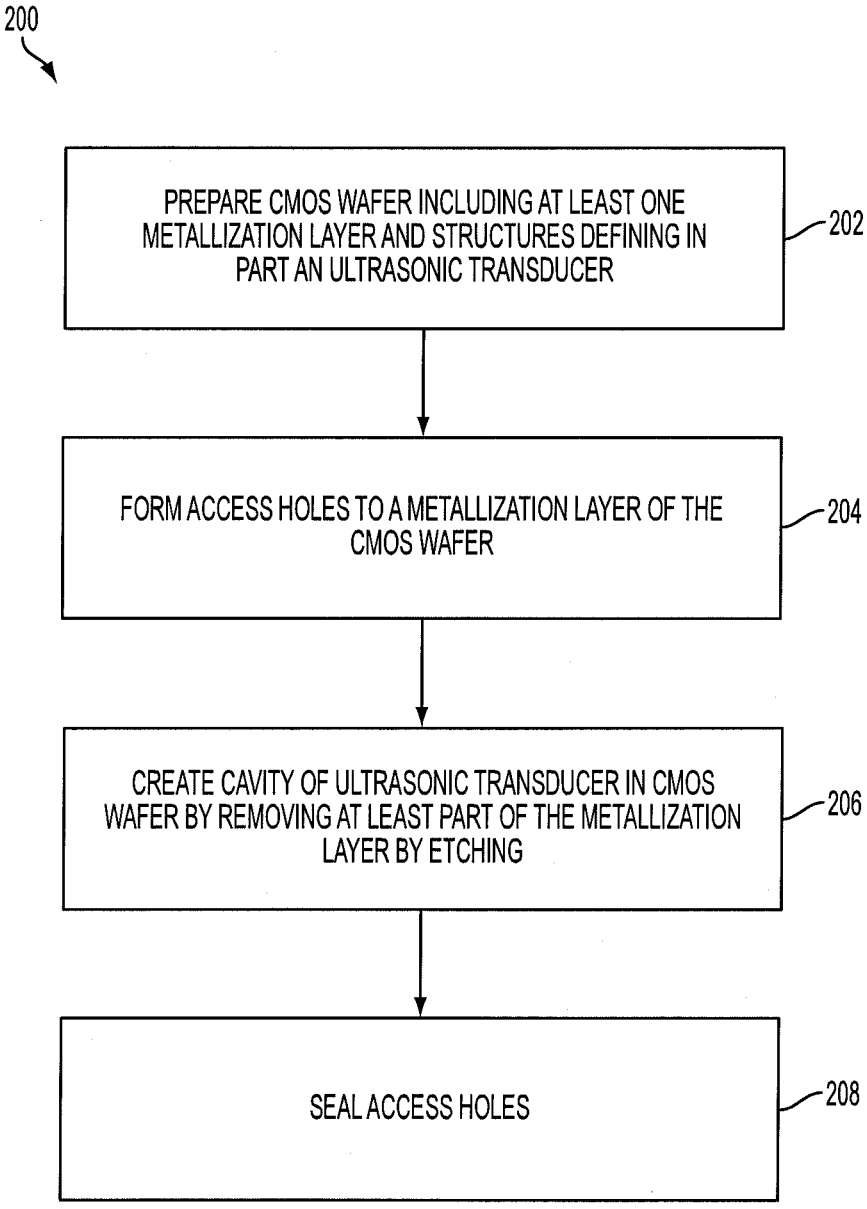
200
PREPARE CMOS WAFER INCLUDING AT LEAST ONE METALLIZATION LAYER AND STRUCTURES DEFINING IN PART AN ULTRASONIC TRANSDUCER
202
FORM ACCESS HOLES TO A METALLIZATION LAYER OF THE CMOS WAFER
204
CREATE CAVITY OF ULTRASONIC TRANSDUCER IN CMOS WAFER BY REMOVING AT LEAST PART OF THE METALLIZATION LAYER BY ETCHING
206
SEAL ACCESS HOLES
208

FIG. 2

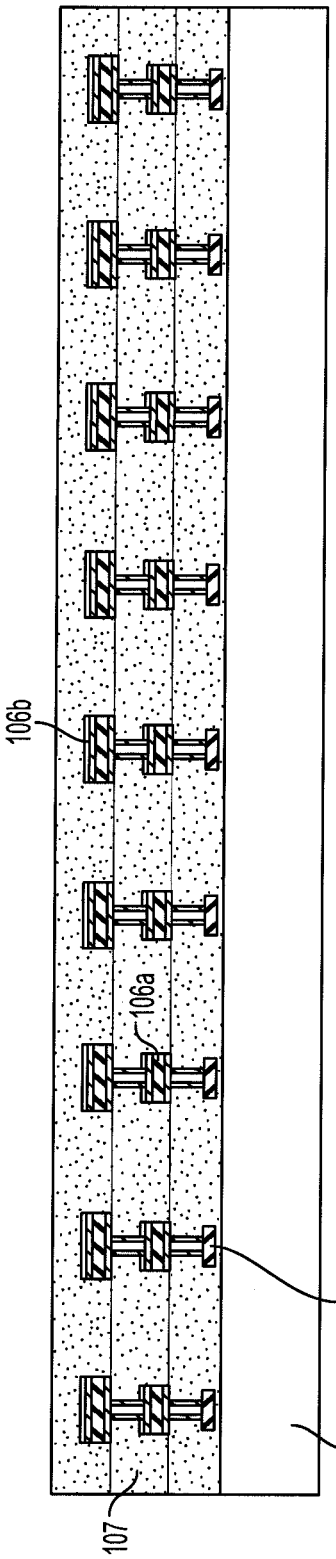

FIG. 3A

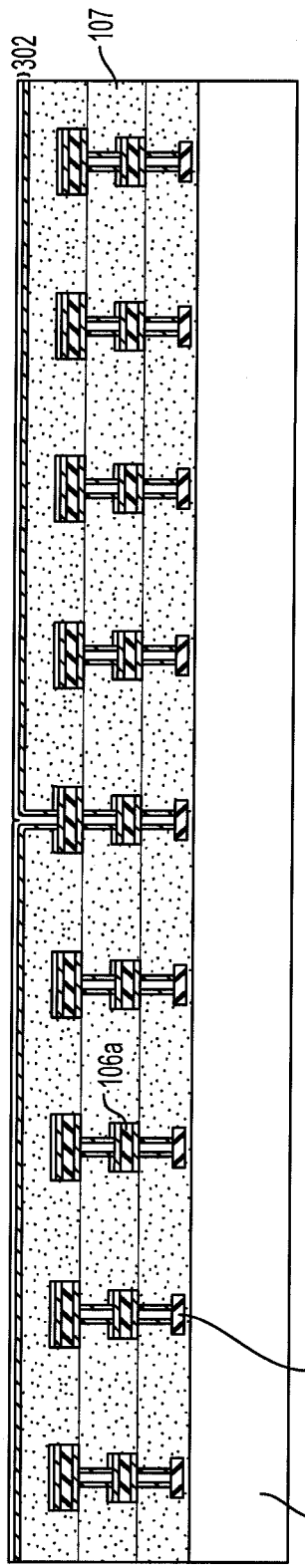

FIG. 3B

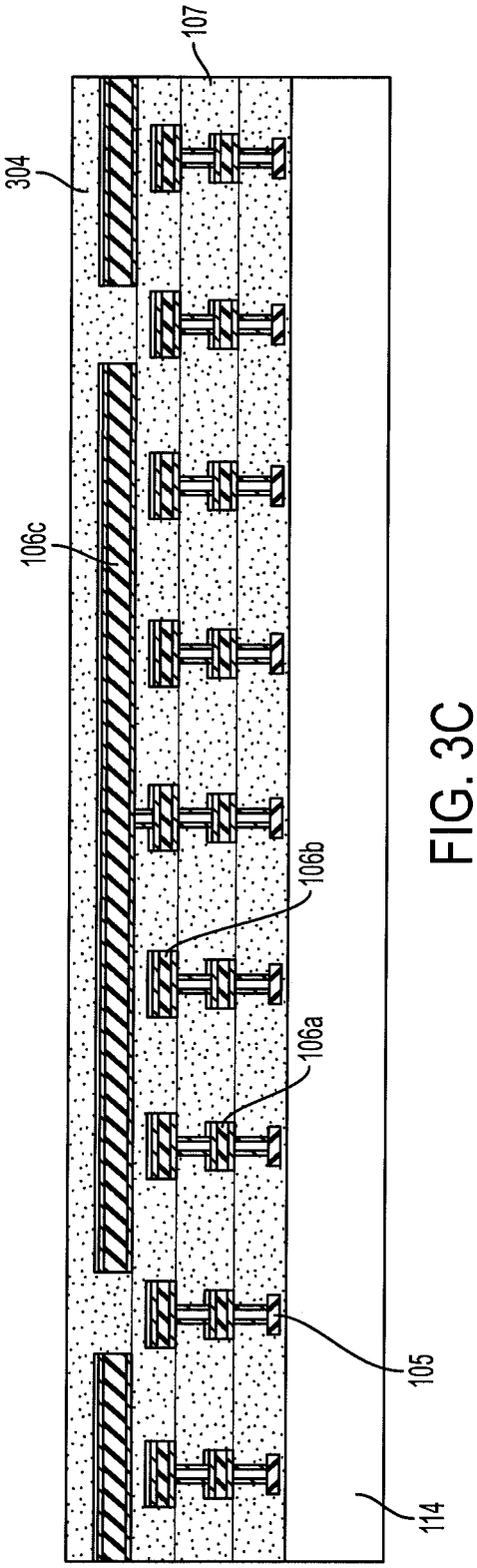

FIG. 3C

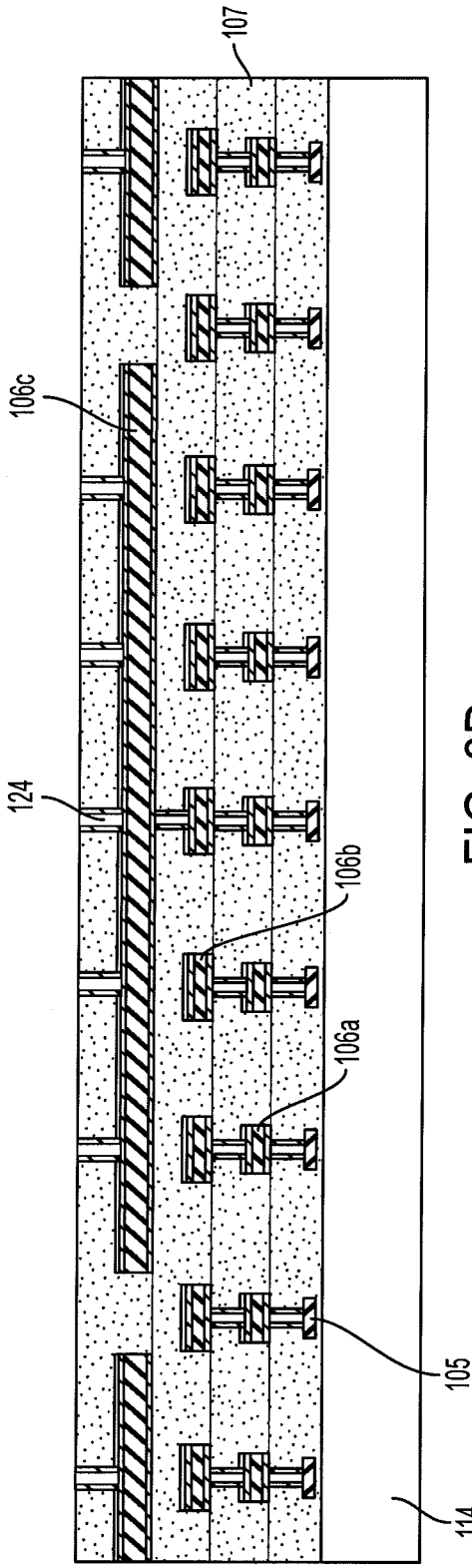

FIG. 3D

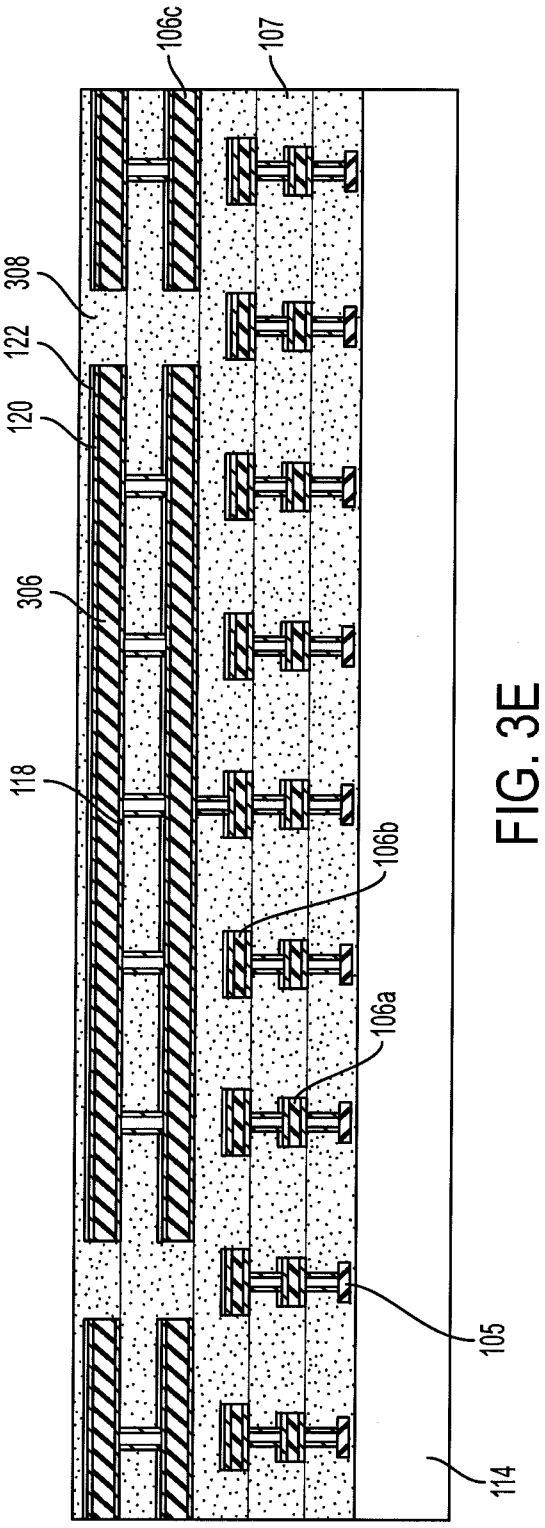
106c
107
308
122
120
306
118
106b
106a
105
114

FIG. 3E

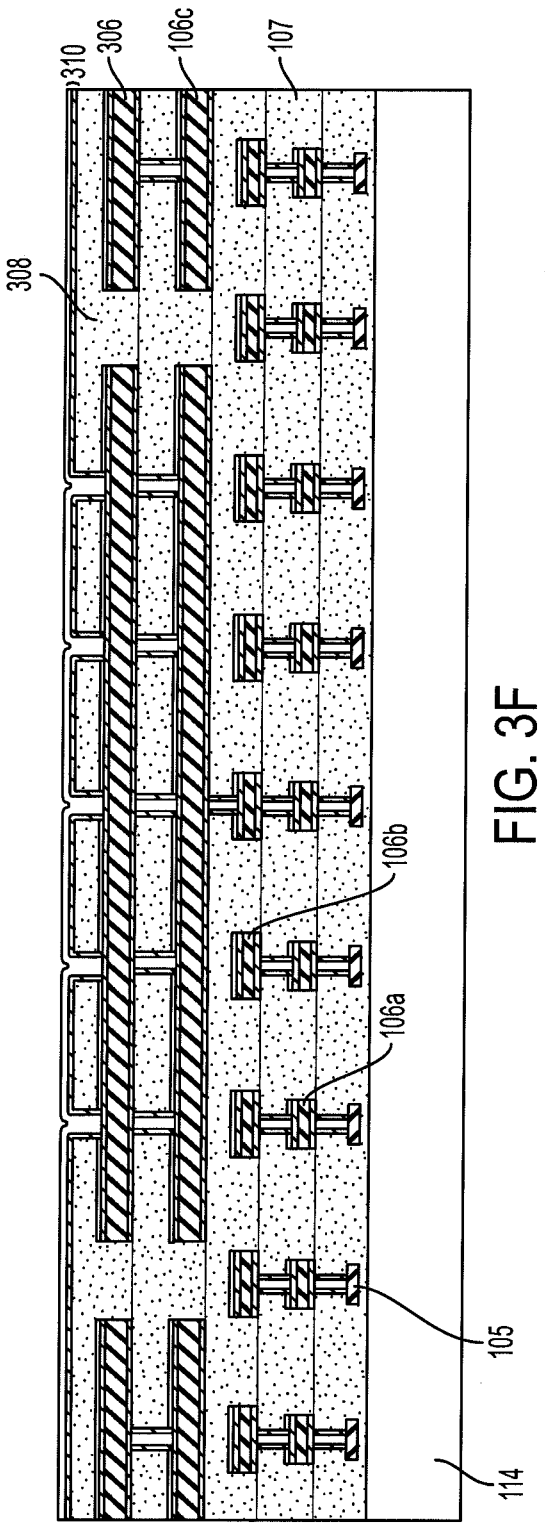
310
306
106c
107
308
106b
106a
105
114

FIG. 3F

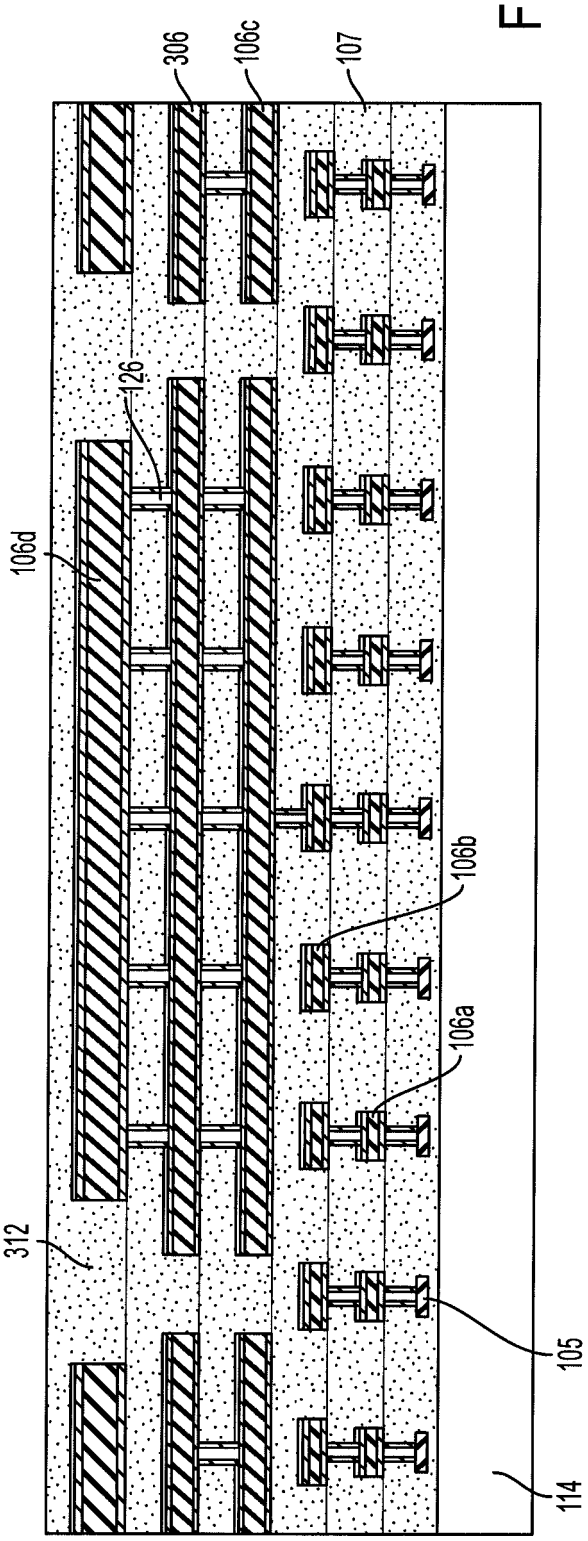
306
106c
107
126
106d
106b
106a
312
105
114

FIG. 3G

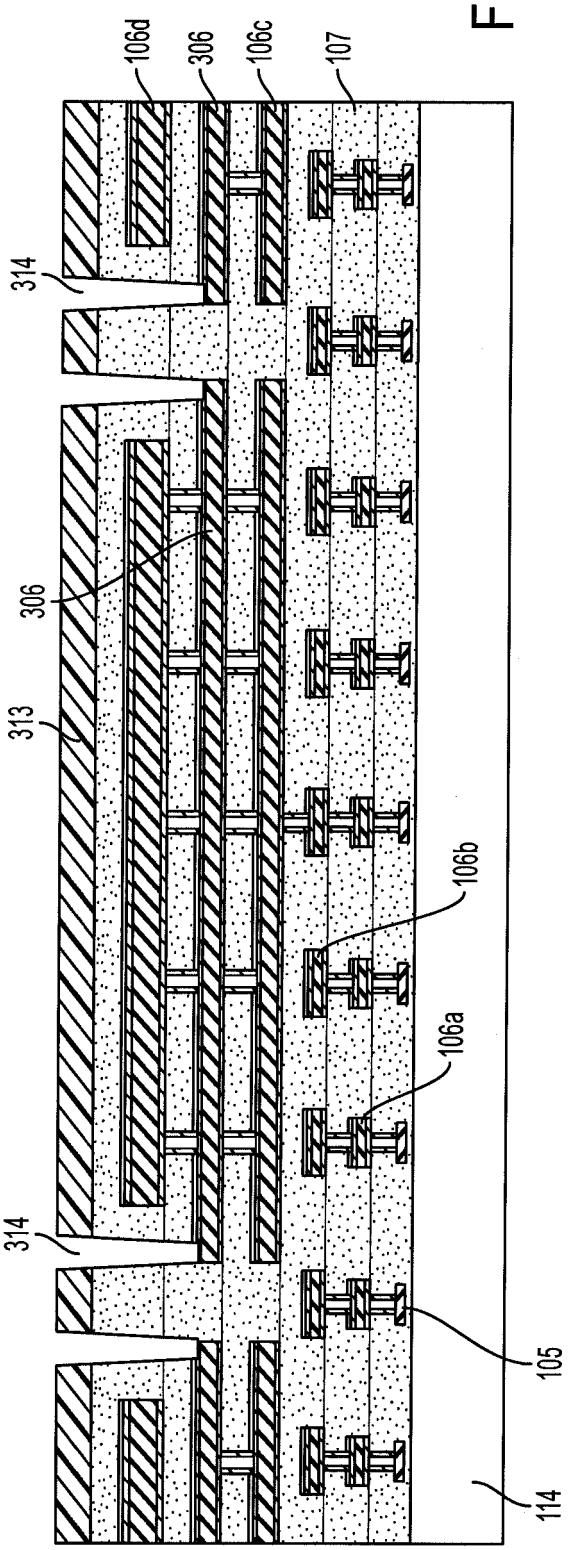
106d
306
106c
107
314
306
313
106b
106a
314
105
114

FIG. 3H

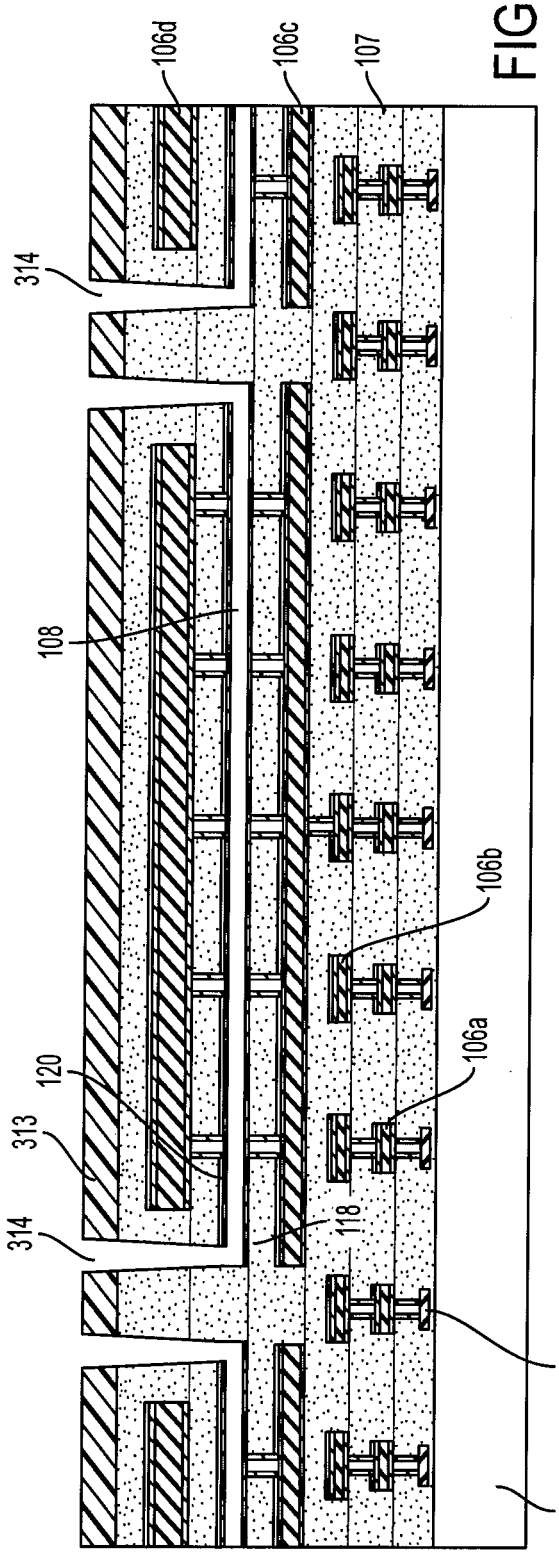
106d
106c
107
314
108
106b
120
313
106a
314
118
105
114

FIG. 3I

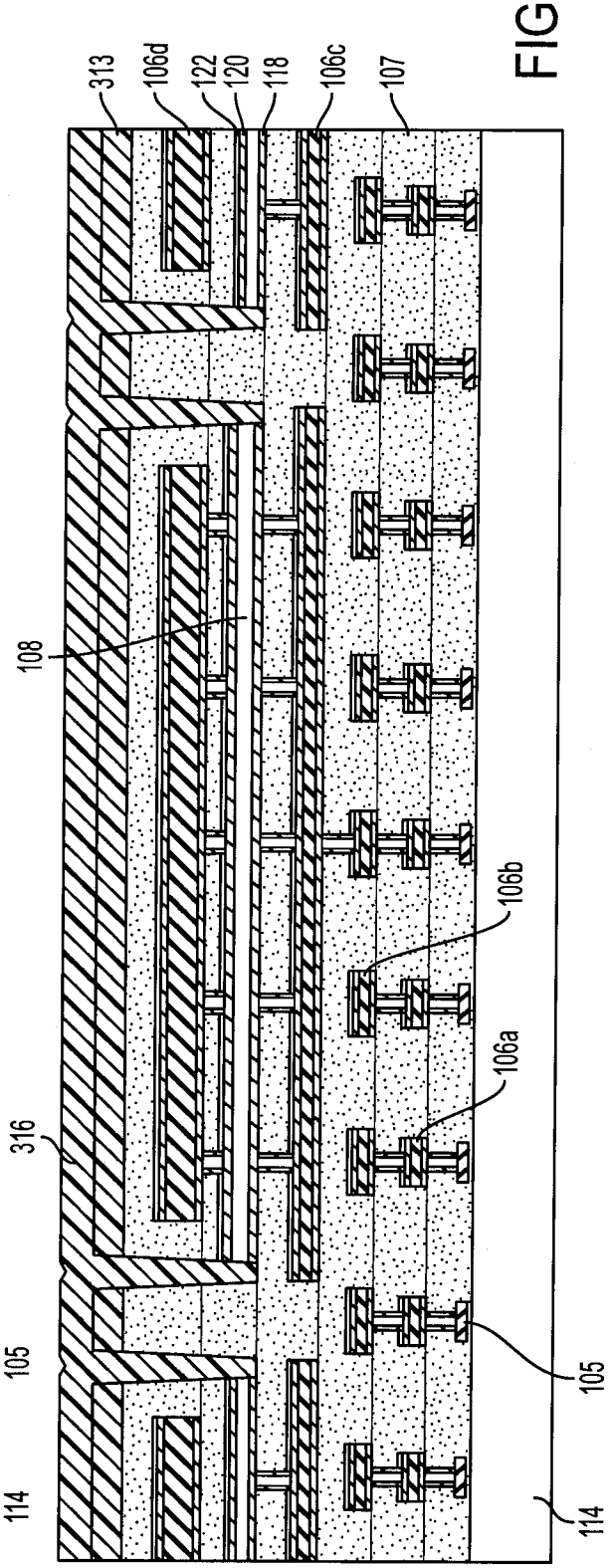
313
106d
122
120
118
106c
107
108
106b
106a
316
105
114

FIG. 3J

REFERENCES CITED IN THE DESCRIPTION

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- US 20130161702 A1 **[0008]**

专利名称(译)	互补金属氧化物半导体（CMOS）晶片中的超声换能器和相关的装置和方法		
公开(公告)号	EP3132470A1	公开(公告)日	2017-02-22
申请号	EP2015721395	申请日	2015-04-17
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申请(专利权)人(译)	蝶形网络INC.		
当前申请(专利权)人(译)	蝶形网络INC.		
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发明人	ROTHBERG, JONATHAN, M. FIFE, KEITH, G. SANCHEZ, NEVADA, J. ALIE, SUSAN, A.		
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CPC分类号	A61B8/00 A61B8/4494 B06B1/02 B06B1/0292 B06B2201/51 B81B3/0021 B81B7/0006 B81B2201/0271 B81C1/00158 B81C1/00246 B81C2203/0735 B81C2203/0771 H01L21/32134 H01L21/56 H01L21/768 H01L21/76838 H01L21/823871 H01L23/5226 H01L23/528 H01L27/0617 H01L27/0688 H01L27/092 H01L2224/16225		
优先权	61/981464 2014-04-18 US		
其他公开文献	EP3132470B1		
外部链接	Espacenet		

摘要(译)

描述了在互补金属氧化物半导体（CMOS）晶片中形成的微机械超声换能器，以及制造这种器件的方法。可以通过牺牲释放来去除CMOS晶片的金属化层，以产生超声换能器的腔。剩余的层可以形成超声换能器的膜。