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(54) PRODUCTION OF PRE-COLLAPSED CAPACITIVE MICRO-MACHINED ULTRASONIC TRANSDUCERS AND APPLICATIONS THEREOF

HERSTELLUNG VORGEFALTETER MIKROMECHANISCHER KAPAZITIVER ULTRASCHALLWANDLER UND IHRE ANWENDUNG

FABRICATION DE TRANSDUCTEURS ULTRASONORES MICRO-USINÉS CAPACITIFS PRÉAFFAISSÉS ET APPLICATIONS DE CES TRANSDUCTEURS

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Description

BACKGROUND:

1. Technical Field:

[0001] The present disclosure is generally directed towards the field of acoustic imaging, e.g., photoacoustic imaging, ultrasonic imaging, and the like. More particularly, exemplary embodiments of the present disclosure relate to new and useful methods for the production of high-end transducer arrays, e.g., transducer arrays that may be advantageously employed in acoustic imaging applications. Exemplary embodiments of the present disclosure also relate to capacitive micro-machined ultra sonic transducers (cMUTs) that provide improved uniformity and reliability based on the advantageous production methods disclosed herein.

2. Background Art:

[0002] In acoustic imaging applications, high-end two-dimensional arrays of ultrasound (US) transducers enable active beam steering/focusing and offer/support real-time three-dimensional imaging applications. Furthermore, the quality of such transducer arrays is a key to overall acoustic imaging product performance and often times is a decisive factor in product differentiation. To this end, methods affecting reliable, efficient, low-cost production of US transducer arrays are in high demand.

[0003] Current technology for manufacture of US transducer arrays generally involves one of: (i) techniques for fabrication of piezoelectric micro-machined ultrasonic transducers (pMUTs) that generally involve thin-film processes and application of piezoelectric stack technology, and (ii) techniques for fabrication of capacitive micro-machined ultrasonic transducers (cMUTs) that generally involve a sacrificial release process wherein a cavity is created underneath a membrane by depositing a sacrificial layer on the carrier substrate.

[0004] In pMUT manufacture, bonded layers of piezoelectric ceramic, composite and simple polymer matching layers are provided. A diamond saw may be used to dice individual elements. Interconnection may be achieved by a conductive layer on the front surface for common, flex traces to element. Alternatively, pMUTs can be made using lithographic techniques, whereby the need for a diamond saw is obviated. Signals are generally transmitted from the pMUT to an ancillary system through coaxial cable or the like. Single crystal manufacture can provide/support improved performance, but at a cost that may not be competitively viable..

[0005] Current methods for the production of cMUTs may involve sacrificial etch processes, whereby a vacuum cavity is created beneath a silicon nitride membrane. For an overview of current cMUT-related processing methods, see "Capacitive Micromachined Ultrasonic Transducers: Fabrication Technology," A. S. Ergun, et al., IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, Vol. 52, (12), December 2005. Wafer bonding techniques for manufacture of cMUTs have also been disclosed.

[0006] A schematic cross-section of an exemplary conventional one-dimensional cMUT element 10 is depicted in Figure 1 (prior art). As depicted therein, a typical cMUT element (un-collapsed) includes (from bottom up) a bottom electrode 12b on a silicon substrate, an insulating layer 14b, a membrane 14a, a top electrode 12a, and an oxide passivation layer 18. Typically, the membrane 14a and insulating layer 14b are configured so as to define a vacuum cavity 16, e.g., a cylindrical cavity, therebetween. The conventional cMUT element may also comprise a plurality of the top and/or bottom electrodes as described in US 2005/200241 A1.

[0007] Application of a bias voltage effects a charge which pulls the membrane and substrate closer together. However, if the membrane/substrate are brought too close together, collapse may occur. In traditional production of cMUT arrays as described in EP1764162, for example, small holes (often times in the sub-100 nm order) and channels are etched through the membrane layer to produce the depicted structure, although larger etched channels (on the order of 2-5 microns) have been disclosed. Relatively expensive and complicated equipment/techniques may be needed to pattern the holes in the membrane for the sacrificial etch, e.g., high-resolution e-beam lithography.

[0008] Conventional cMUTs (uncollapsed) carry with them inherent disadvantages, including non-linear behaviour, narrow operating range, low capacitance, and high sensitivity to manufacturing variability. In addition, a relatively high bias voltage is required. It is noted that, for an un-collapsed cMUT, the force on the membrane is proportional to the square of the charge. Thus, increasing the force decreases separation which, in turn, increases capacitance, and (with a voltage bias) increases the charge. Consequently, the membrane will eventually collapse when positive feedback overcomes the rigidity of the membrane; the result of this collapse is formation of a collapsed cMUT.

[0009] Collapsed cMUTs have been investigated. For example, collapsed cMUTs have been formed wherein the membrane is collapsed to the bottom of the cavity by applying a

[0010] DC bias voltage. Collapsed cMUTs can offer improved performance. However, problems specific to collapsed cMUTs have yet to be adequately resolved and/or addressed, e.g., manufacturing-related problems, issues related to array uniformity, and overall reliability. For example, the relatively high voltage needed to produce membrane collapse creates significant complications, e.g., increased cMUT sensitivity to charging. Such relatively high voltages may also negatively impact on associated electronics, e.g., chips.

[0011] Thus, a need remains for effective and reliable manufacturing methods for fabrication of collapsed

cMUTs that exhibit desirable performance properties on a consistent and cost-effective basis. As will be apparent to persons skilled in the art from the disclosure which follows, the advantageous methods disclosed herein meet this unresolved need and support commercial manufacture of collapsed cMUTs, with the attendant benefits associated therewith.

SUMMARY OF THE DISCLOSURE:

[0012] The method according to the present invention is defined by the subject-matter of claim 1. The device according to the present invention is defined by the subject-matter of claim 23.

[0013] Advantageous methods for production of pre-collapsed cMUTs are provided according to the present disclosure. More particularly, exemplary embodiments of the disclosed methods provide for significant cost-effective improvements in standards of manufacture and overall efficacy of collapsed cMUTs. Indeed, exemplary embodiments of the methods disclosed effectively solve previously unresolved problems associated with collapsed cMUTs, including the necessity for a relatively high collapse voltage and a related sensitivity to charging. While exemplary embodiments of the present disclosure generally relate to acoustic imaging applications and, more specifically, photoacoustic (PA) imaging applications, it is specifically contemplated that the methods disclosed herein apply with equal utility and benefit to any field wherein compact transducer arrays may be desirable.

[0014] Generally, exemplary embodiments of the present disclosure relate to methods for production of pre-collapsed cMUTs that follow conventional manufacturing steps to form/fabricate nearly completed, conventional cMUTs. These nearly completed cMUTs are generally include groupings, e.g., arrays, of cMUT elements, wherein each individual cMUT element includes (from bottom up) (1) a substrate layer, (2) an electrode plate, (3) a membrane layer, and (4) an electrode.

[0015] The substrate layer is typically constructed from an industry standard substrate material such as silicon. In exemplary embodiments of the present disclosure, the electrode plate is circularly configured and embedded in the top face of the substrate layer. The membrane layer is typically configured so as to define a cylindrical cavity between the substrate layer and membrane, whereby the embedded electrode plate is enclosed therewithin. The membrane layer is typically constructed from an industry standard membrane material such as silicon nitride. The electrode ring may be advantageously fixed relative to the top face of the membrane layer such that the center of the electrode ring is positioned directly above the center of the electrode plate. Indeed, the outer diameter of the electrode ring may be substantially equal to the diameter of the circularly configured electrode plate in exemplary implementations. Typically, the electrode ring is configured and dimensioned such that the inner diameter of the electrode ring defines an membrane layer area for patterning and/or etching.

[0016] According to the present disclosure, the manufacturing method deviates from conventional cMUT fabrication techniques with respect to final (or near-final) processing steps. More particularly, according to the present disclosure, the conventional steps associated with etching of the sacrificial layer and sealing of the membrane layer are replaced and/or improved upon. Thus, in exemplary embodiments of the present disclosure, methods for production of pre-collapsed cMUTs involve the following steps: (1) obtaining a nearly completed cMUT as described herein, (2) defining a hole through the membrane layer for each cMUT element (wherein the hole is generally defined through the center of the electrode ring), (3) applying a bias voltage (typically a well-defined bias voltage) across the membrane and substrate layers so as to collapse the membrane layer to and/or toward the substrate layer proximate to each hole, and (4) fixing/sealing the collapsed membrane layer relative to the substrate layer.

[0017] Dimensional characteristics of the holes defined through the membrane layer according to the disclosed manufacturing method may differ relative to dimensions common to traditional cMUT production. Thus, exemplary hole dimensions defined through the membrane layer may be between about 1 and 25 microns. In exemplary embodiments, the holes have a diameter on the order of 10 to 20 μm, although holes of smaller dimension, e.g., hole diameters on the order of about 3 or 4 microns, may be employed according to the present disclosure. In general, the disclosed holes are patterned such that each hole is defined through the membrane layer at (or substantially near) the center point of the corresponding electrode ring. Of note, the diameter of the hole is smaller than the inner diameter of the electrode ring.

[0018] In exemplary implementations of the disclosed manufacturing techniques, the holes are defined/formed through the substrate layer by etching sacrificial layer(s) so as to free the membrane layer. Due to the relatively large size of the holes that may be employed according to the present disclosure, traditional etching techniques that required and/or utilized high resolution e-beam lithography may be advantageously avoided. Instead, exemplary techniques for patterning the holes of the present disclosure include the use of "g-line" or "i-line" lithography, thus cutting costs and providing for a greater degree of array uniformity. As used herein, "g-line" lithography involves UV radiation involving a high intensity line at 436 nm wavelength, and "i-line" lithography involves UV radiation involving a high intensity line at 365 nm wavelength. Alternative techniques for forming/patterning the holes according to the present disclosure employ optical lithography at exemplary wavelengths of 248 nm (deep ultraviolet/DUV), 365 nm, 436 nm and the like. Still further, e-beam and/or imprint lithography may be employed for hole forming/patterning according to the

present disclosure.

[0019] Additional advantages are achieved according to the disclosed manufacturing techniques. For example, due to the size of the holes in the disclosed manufacturing technique, higher etching rates may be advantageously achieved relative to traditional etching techniques. In addition, since no channels are necessarily created during the disclosed patterning and etching process for pre-collapsed cMUTs, a near-100% array density is possible.

[0020] In exemplary embodiments of the present disclosure, the bias voltage applied across the membrane and substrate layers is a DC coupling voltage is between 10 and 250V, e.g., on the order of approximately 100V. The amount of pre-collapse can be regulated by changing the magnitude of the DC coupling voltage, thus allowing for flexible customization and optimization of array properties. Of note, external electrical contacts may be applied to a wafer during the deposition process for purposes of effecting the desired coupling voltage. Of note, the bias voltage may be reduced following collapse of the membrane layer, provided that the voltage remains sufficient to maintain the collapsed state.

[0021] According to the present disclosure, the collapsed membrane is fixed and sealed relative to the substrate, e.g., applying an encasing layer to the collapsed assembly. The encasing layer may be an industry standard material, e.g., Si_3N_4. During deposition of the encasing layer, the bias voltage is typically maintained active across the membrane and substrate layers. However, in exemplary embodiments of the present disclosure, the bias voltage may be reduced prior to and/or during the fixing and sealing process. After the encasing layer is applied, the bias voltage becomes unnecessary and may be discontinued or reduced to an operating voltage.

[0022] The disclosed manufacturing techniques offer many clear advantages over prior art manufacturing techniques. For example, exemplary methods disclosed herein provide for a higher etching rate of the sacrificial layer relative to conventional means. Furthermore, the disclosed etching/patterning steps may be achieved using relatively inexpensive technology, e.g., g-line lithography or i-line lithography, as opposed to the prior art requirement that high resolution e-beam lithography be employed. Exemplary methods of the present disclosure result in pre-collapsed cMUTs with a near-100% array density, high array uniformity and high collapse uniformity. The collapsed cMUTs fabricated according to the present disclosure also exhibit improved linearity, with substantial elimination of any potential hysteresis loop. Furthermore, the amount of pre-collapse can be effectively regulated by varying the magnitude of the bias voltage. Exemplary methods disclosed also have the advantage of reducing the operating voltage for producing a collapsed cMUT and thus exponentially reducing the charging scale. Still further, continued application of a bias voltage during the fixing/sealing process advantageously prevents potential complications during the post-etching drying process.

[0023] The disclosed pre-collapsed cMUTs may be packaged to provide an advantageous assembly. For example, a water proof packaging may be formed to encase and protect a pre-collapsed cMUT of the present disclosure. The disclosed cMUTs may also be combined with a focusing lens to facilitate delivery of emitted waves, e.g., ultrasound, to a desired target.

[0024] The present disclosure also extends to advantageous applications of the pre-collapsed cMUTs disclosed herein. Thus, in a first exemplary implementation of the disclosed pre-collapsed cMUTs, an integrated assembly is provided that includes, *inter alia,* a pre-collapsed cMUT and an integrated circuit/chip that includes, *inter alia,* beam-steering functionality. The beam-steering chip generally includes various features/functionalities, including a pulse generator, one or more drivers (e.g., to boost output voltage), a pre-amplifier, a processor, and/or input/output control functionality. Integration of a pre-collapsed cMUT and a beam-steering chip advantageously facilitates control/optimization of ultrasound delivery from the pre-collapsed cMUT of the present disclosure. An integrate assembly also supports and/or facilitates operative control and data receipt/processing.

[0025] The pre-collapsed cMUTs of the present disclosure have wide ranging, advantageous applications. For example, the pre-collapsed cMUTs may be used in various transducer applications that extend beyond ultrasound transducer implementations. For example, the pre-collapsed cMUTs (whether alone or in combination with an integrated chip/IC) may be employed in various catheter-based applications, needle insertion units, ultrasound flow meter implementations and the like. Indeed, in exemplary catheter-based and/or needle-based implementation, a pre-collapsed cMUT according to the present disclosure may be used to locate an anatomical structure, e.g., vessel, or to otherwise facilitate anatomical navigation. Alternative applications that may operate within or outside the ultrasound regimen may benefit from implementation of the pre-collapsed cMUTs disclosed herein, as will be apparent to persons skilled in the art from the description which follows.

[0026] Although the present disclosure is described with reference to exemplary embodiments and implementations thereof, the present disclosure is not to be limited by or to such exemplary embodiments and/or implementations. Rather, the apparatus, systems and methods of the present disclosure are susceptible to various modifications, variations and/or enhancements without departing from the scope of the present disclosure. Accordingly, the present disclosure expressly encompasses all such modifications, variations and enhancements within its scope.

[0027] The scope of the present invention is defined by the claims.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0028] To assist those of ordinary skill in the relevant art in making and using the subject matter hereof, reference is made to the appended drawings, wherein:

Figure 1 depicts a schematic cross-section of an exemplary conventional one-dimensional cMUT element.

Figure 2 depicts a schematic cross-section of a single element of a nearly completed cMUT.

Figure 3 depicts a schematic cross-section of the element depicted in **Figure 2,** wherein a hole has been defined through the membrane layer relative to the center of the electrode ring.

Figure 4 depicts a schematic cross-section of the element depicted in **Figure 3,** wherein a bias voltage has been applied across the membrane and substrate layers so as to collapse the membrane layer relative to the substrate layer.

Figure 5 depicts a schematic cross-section of the element depicted in **Figure 4,** wherein the collapsed membrane layer has been fixed and sealed relative to the substrate layer by applying an encasing layer.

Figure 6 is a schematic view of an alternative exemplary cMUT of the present disclosure.

Figure 7 are schematic views of an exemplary packaged cMUT-containing unit according to the present disclosure;

Figure 8 depicts a schematic view of an exemplary integrated assembly according to the present disclosure that includes a cMUT and a beam-steering chip.

Figure 9 depicts a schematic view of an exemplary assembly that includes a pre-collapsed cMUT and lens according to the present disclosure.

Figure 10 provides three (3) SEM images of exemplary cMUTs of the present disclosure.

Figure 11 provides three (3) SEM images related to sealing of etching holes of a cMUT according to the present disclosure.

DESCRIPTION OF EXEMPLARY EMBODIMENTS:

[0029] Exemplary methods for production of pre-collapsed cMUTs are provided according to the present disclosure. To assist those of ordinary skill in the relevant art in making and using such exemplary methods, appended figures are provided, wherein sequential steps of exemplary manufacturing methods are depicted.

[0030] Exemplary methods for fabrication of collapsed cMUTs according to the present disclosure typically include the following steps: (1) obtaining a nearly completed cMUT as depicted in **Figure 2,** (2) defining at least one hole (and optionally a plurality of holes) through the membrane layer for each cMUT element as depicted in **Figure 3,** (3) applying a bias voltage across the membrane and substrate layers so as to collapse the membrane layer relative to the substrate layer as depicted in **Figure 4,** and (4) fixing and sealing the collapsed membrane layer relative to the substrate layer as depicted in **Figure 5.**

[0031] With initial reference to **Figure 2,** a schematic cross-section of a cMUT element 5 is depicted, wherein the obtained nearly completed cMUT includes a grouping (e.g., an array) of cMUT elements. Exemplary cMUT element 5 includes a substrate layer 20, an electrode plate 22b, a membrane layer 24, and an electrode ring 22a. In the exemplary embodiment, the electrode plate 22b is circularly configured and embedded in the substrate layer 20. In addition, the membrane layer 24 is fixed relative to the top face of the substrate layer 20 and configured/dimensioned so as to define a cylindrical cavity 26 in between the membrane layer 24 and the substrate layer 20. Of note, cylindrical cavity 26 may define alternative geometries, whether in whole or in part. For example, cavity 26 could define a rectangular and/or square cross-section, a hexagonal cross-section, an elliptical cross-section, or an irregular cross-section, as will be apparent to persons skilled in the art.

[0032] The bottom electrode 22b is typically insulated with an additional layer (not pictured). The disclosed components may be fabricated from CMOS compatible materials, e.g., Al, Ti, nitrides (e.g., silicon nitride), oxides (various grades), tetra ethyl oxysilane (TEOS), poly-silicon and the like.

[0033] Exemplary techniques for producing the disclosed cavity 26 involves defining such cavity in an initial portion of the membrane layer 24 before adding a top face of the membrane layer 24. In the exemplary embodiment depicted in **Figure 2,** the diameter of the cylindrical cavity 26 is larger than the diameter of the circularly configured electrode plate 22b. Electrode ring 22a may have the same outer diameter as the circularly configured electrode plate 22b, although such conformance is not required according to the present disclosure. Thus, in an exemplary embodiment of the present disclosure, the electrode ring 22a is fixed relative to the top face of the membrane layer 24 so as to align with the electrode plate 22b below.

[0034] With reference now to **Figure 3,** a schematic cross-section of exemplary cMUT element 5 is depicted, wherein a hole 27 has been defined through the top face of the membrane layer 24 relative to the center of the electrode ring 22a. As noted previously, hole 27 may be augmented with additional holes to define a plurality of holes. As shown in **Figure 3,** exemplary hole 27 is circularly configured with a diameter that is less than the inner diameter of the electrode ring 22a. Hole 27 may be advantageously formed using optical lithography, e.g., g-line lithography, i-line lithography, nano-imprint lithography, and/or e-beam lithography. Hole 27 is typically characterized by a diameter of between about 1 and 25 microns.

[0035] With reference now to **Figure 4,** a schematic cross-section of exemplary cMUT element 5 is depicted, wherein a bias voltage has been applied across the mem-

brane layer 24 and substrate layer 20 so as to collapse the membrane layer 24 relative to the substrate layer 20. An exemplary resulting angular configuration of the electrode ring 22a can be seen. In the exemplary embodiment depicted in **Figure 4,** the top face of the membrane layer 24 proximate to the hole 27 is thus brought into contact with the electrode plate 22b.

[0036] With reference now to **Figure 5,** a schematic cross-section of exemplary cMUT element 5 is depicted, wherein the collapsed membrane layer 24 has been fixed and sealed relative to the substrate layer 20 and the electrode plate 22b by applying an encasing layer 28 over the top face of the membrane layer 24 and the electrode ring 22a. The final resulting cMUT element 5 is thus an exemplary embodiment of one of many pre-collapsed cMUT elements that may be fabricated according to the disclosed manufacturing methodology. Fabrication of the disclosed cMUT may employ plasma-enhanced chemical vapor deposition (PECVD) and/or low pressure chemical vapor deposition (LPCVD). The disclosed electrode plates/members may be fabricated from a suitable conductive material, e.g., a metallic or non-metallic conductive material.

[0037] An alternative embodiment of the present disclosure is schematically depicted in **Figure 6.** Exemplary cMUT 40 includes a plurality of holes 42, e.g., relatively small etched holes, formed in membrane 44. Holes 42 are surrounded by ring electrode 46. Thus, in the alternative embodiment of **Figure 6,** a single central hole is replaced by a number of relatively small holes 42 that are positioned approximately in the center of the membrane 44, such holes 42 being located within the inner diameter of the ring electrode 46. Fabrication and functionality of the alternative cMUT 40 of **Figure** 6 corresponds to the fabrication/functionality of the previously disclosed exemplary pre-collapsed cMUT (see **Figures 1-5**).

[0038] In exemplary embodiments of the present disclosure, an additional insulation layer may be provided on top of bottom electrode 22b. In addition, the metallic bottom electrode 22b may be replaced by a conductive non-metallic layer that provides the same functionality.

[0039] In further exemplary embodiments of the present disclosure and with reference to **Figure 7,** a packaged unit 50 that includes a pre-collapsed cMUT 52 is schematically disclosed. Bond pads 54 are formed along or adjacent the periphery of cMUT 52 and communicate with an interconnect feature 56 through conductive members, e.g., gold bumps 58 that are defined on cMUT 52. A flow barrier 60 is also defined on cMUT 52, internal to gold bumps 58 and surrounding an energy path 62. Energy path 62 facilitates transmission of ultrasound waves and the like. Flow barrier 60 may take the form of an SU-8 flow barrier or other photoresist material. SU-8 is a viscous polymer that defines a commonly used negative photoresist. As assembled, packaged unit 52 advantageously defines a water proof unit having widespread application. Background information related to packaged biosensors is provided in a publication entitled "A new package for silicon biosensors," EMPC 2005, June 12-15, Brugge, Belgium, the contents of which are incorporated herein by reference.

[0040] With reference to **Figure 8,** a schematic depiction of an exemplary integrated assembly according to the present disclosure is provided. Assembly 100 includes cMUT 102 and beam-steering chip 104 mounted with respect to each other to define an integrated unit. cMUT 102 and beam-steering chip 104 are in communication such that chip 104 provides input to cMUT 102 for ultrasound delivery therefrom. Chip 104 typically includes various features and functionalities, e.g., a pulse generator, one or more drivers (e.g., to boost output voltage), a pre-amplifier, a processor, and input/output control functionality. Design and fabrication of an appropriate beam-steering chip/integrated circuit 104, e.g., an ASIC, is well known to skilled practitioners.

[0041] With reference to **Figure 9,** a further assembly 150 including a pre-collapsed cMUT transducer 152 and a lens 154 is schematically depicted. The disclosed lens 154 is generally adapted to focus the emissions from cMUT transducer 152, e.g., ultrasound waves emitted therefrom. Lens 154 may take the form of a plastic unit with appropriate transmission properties.

[0042] SEM images associated with the present disclosure are provided in **Figure 10** and **Figure 11** hereto. **Figure 10** provides three (3) SEM images related to fabrication of the disclosed cMUTs and **Figure 11** provides three (3) SEM images related to sealing of etching holes associated with the disclosed cMUTs.

[0043] The disclosed cMUT fabrication techniques/methods are adapted to produce pre-collapsed cMUTs with broad application and advantageous functionality. For example, the pre-collapsed cMUTs disclosed herein are advantageously adapted to generate ultrasound waves in predetermined frequency ranges, e.g., 1-5 MHz and 5-50 MHz. Alternative frequency ranges may be supported and/or generated with the pre-collapsed cMUTs of the present disclosure. The pre-collapsed cMUTs of the present disclosure have wide ranging, advantageous applications, e.g., in transducer applications that extend beyond ultrasound transducer implementations. Among the exemplary implementations of the pre-collapsed cMUTs are catheter-based applications, needle insertion applications, ultrasound flow meter applications, and the like. The pre-collapsed cMUTs may be employed alone or in combination with an integrated chip/IC to provide additional features/functionalities. In exemplary catheter-based and/or needle-based implementation, a pre-collapsed cMUT may be used to locate an anatomical structure, e.g., a vessel, organ, etc., or to otherwise facilitate anatomical navigation. Alternative applications that may operate within or outside the ultrasound regimen may benefit from implementation of the pre-collapsed cMUTs disclosed herein.

[0044] As noted above, although the present disclosure is described with reference to exemplary embodi-

ments and implementations thereof, the present disclosure is not to be limited by or to such exemplary embodiments and/or implementations.

Claims

1. A method for producing a cMUT, comprising:

   providing a nearly completed cMUT, wherein the nearly completed cMUT defines one or more cMUT elements that include: (i) a substrate layer (20), (ii) an electrode plate (22b), (iii) a membrane layer (24), and (iv) an electrode ring (22a), defining at least one hole (27) through the membrane layer (24) for each cMUT element,
   applying a bias voltage across membrane (24) and substrate layers (20) of the one or more cMUT elements so as to collapse the membrane layer (24) relative to the substrate layer (20),
   fixing and sealing the collapsed membrane layer (24) relative to the substrate layer (20) by applying an encasing layer (28).

2. The method according to claim 1, additionally comprising: (i) discontinuing the bias voltage, (ii) reducing the bias voltage to an operating voltage, or (iii) a combination thereof.

3. The method according to claim 1, wherein the bias voltage is a well-defined DC voltage supplied by a battery.

4. The method according to claim 3, wherein the well-defined DC voltage falls is between 10 and 250V.

5. The method according to claim 1, wherein the bias voltage is effective to regulate the amount of collapse.

6. The method according to claim 5, wherein the regulation of the amount of collapse is effective to optimize performance.

7. The method according to claim 1, wherein the one or more holes (27) are between
   about 1 and 25 microns in diameter.

8. The method according to claim 1, wherein the holes (27) are defined using an optical lithography technique selected from the group consisting of g-line lithography, i-line lithography, nano-imprint lithography and e-beam lithography.

9. The method according to claim 1, wherein the electrode (22b) is a circular electrode plate fabricated from a conductive material (metal or non-metal).

10. The method according to claim 9, wherein the outer diameter of the electrode ring is configured and dimensioned to substantially match the diameter of the circular electrode plate and wherein the center of electrode the ring and center of the circular electrode plate are substantially aligned.

11. The method according to claim 1, wherein the substrate layer (20) comprises silicon.

12. The method according to claim 1, wherein the membrane layer (24) comprises a CMOS compatible material, e.g., a nitride (e.g., silicon nitride), an oxide (various grades), tetra ethyl oxysilane (TEOS), polysilicon and the like.

13. The method according to claim 1, wherein the cMUT is fabricated, at least in part, using plasma-enhanced chemical vapor deposition (PECVD) and/or low pressure chemical vapor deposition (LPCVD).

14. The method according to claim 1, wherein the electrode plate (22b) of the cMUT element is fixed relative to the top surface of the substrate layer (20).

15. The method according to claim 1, wherein the membrane of the cMUT element is fixed relative to a top face of the substrate layer (20) so as to define a cavity between the membrane (24) and substrate layer.

16. The method according to claim 1, wherein the electrode ring (22a) is fixed relative to a top face of the membrane layer (24).

17. The method according to claim 1, wherein the at least one hole (27) is defined through the membrane (24) relative to the center of the electrode ring (22a).

18. The method according to claim 1, wherein the diameter of the hole (27) is less than the inner diameter of the electrode ring (22a).

19. The method according to claim 1, wherein the area of collapse of the membrane layer is proximate to the hole. (27)

20. The method according to claim 1, wherein the bias voltage is: (i) maintained throughout the fixing and sealing process, (ii) reduced prior to the fixing and sealing process, (iii) reduced during the fixing and sealing process; or (iv) a combination thereof.

21. The method according to claim 1, wherein the cMUT is adapted to produce ultrasound waves in a predetermined frequency range said range including frequencies of between about 1-5 MHz or 5-50 MHz.

22. A cMUT device comprising: (i) a substrate layer (20), (ii) an electrode plate (22b), (iii) an electrode ring (22a), (iv) a membrane layer (24), wherein the membrane (24) has at least one hole (27) and is collapsed relative to the substrate layer (20), and (v)an encasing layer (28) applied to the membrane layer (24) and adapted to fix and seal the membrane layer (24) relative to the substrate (20).

23. An integrated assembly, comprising:

the cMUT device according to claim 22; and
an integrated circuit/chip that includes beam-steering functionality; wherein the pre-collapsed cMUT and the beam-steering integrated circuit/chip are mounted with respect to each other to define an integrated unit.

24. A packaged cMUT-containing unit, comprising:

the cMUT device according to claim 22 alone or in combination with an integrated circuit/chip;
at least one bond pad in communication with a conductive interconnect; and
a flow barrier surrounding an energy path.

25. The packaged unit according to claim 24, wherein the flow barrier is fabricated from a photoresist material.

Patentansprüche

1. Verfahren zur Herstellung eines cMUTs, wonach:

ein nahezu kompletter cMUT vorgesehen wird, wobei der nahezu komplette cMUT ein oder mehrere cMUT-Elemente definiert, die enthalten: (i) eine Substratschicht (20), (ii) eine Elektrodenplatte (22b), (iii) eine Membranschicht (24) sowie (iv) einen Elektrodenring (22a),
wobei für jedes cMUT-Element mindestens ein Loch (27) durch die Membranschicht (24) definiert wird,
eine Vorspannung über die Membran- (24) und Substratschicht (20) des einen oder mehrerer cMUT-Elemente angelegt wird, damit die Membranschicht (24) relativ zu der Substratschicht (20) kollabiert,
die kollabierte Membranschicht (24) relativ zu der Substratschicht (20) durch Aufbringen einer Hüllschicht (28) fixiert und gekapselt wird.

2. Verfahren nach Anspruch 1, wonach darüber hinaus: (i) die Vorspannung ausgesetzt wird, (ii) die Vorspannung auf eine Betriebsspannung reduziert wird oder (iii) eine Kombination daraus angewandt wird.

3. Verfahren nach Anspruch 1, wobei die Vorspannung eine von einer Batterie abgegebene, klar definierte DC-Spannung ist.

4. Verfahren nach Anspruch 3, wobei die Abfälle der klar definierten DC-Spannung zwischen 10 und 250 V liegen.

5. Verfahren nach Anspruch 1, wobei die Vorspannung so effektiv ist, dass sie das Ausmaß des Kollabierens reguliert.

6. Verfahren nach Anspruch 5, wobei die Regulierung des Ausmaßes des Kollabierens so effektiv ist, dass die Leistung optimiert wird.

7. Verfahren nach Anspruch 1, wobei das eine oder mehrere Löcher (27) einen Durchmesser zwischen etwa 1 und 25 Mikrometer haben.

8. Verfahren nach Anspruch 1, wobei die Löcher (27) unter Anwendung einer Technik der optischen Lithographie definiert werden, die aus der Gruppe, bestehend aus g-Line-Lithographie, i-Line-Lithographie, Nano-Imprint-Lithographie und E-Beam-Lithographie, ausgewählt wird.

9. Verfahren nach Anspruch 1, wobei die Elektrode (22b) eine aus einem leitenden Material (Metall oder Nicht-Metall) hergestellte kreisförmige Elektrodenplatte ist.

10. Verfahren nach Anspruch 9, wobei der Außendurchmesser des Elektrodenrings so ausgeführt und bemessen ist, dass er dem Durchmesser der kreisförmigen Elektrodenplatte im Wesentlichen entspricht, und wobei der Mittelpunkt des Elektrodenrings und der Mittelpunkt der kreisförmigen Elektrodenplatte im Wesentlichen ausgefluchtet werden.

11. Verfahren nach Anspruch 1, wobei die Substratschicht (20) Silicium enthält.

12. Verfahren nach Anspruch 1, wobei die Membranschicht (24) ein CMOSkompatibles Material, z.B. ein Nitrid (z.B. Siliciumnitrid), ein Oxid (verschiedene Güteklassen), Tetraethyloxysilan (TEOS), Poly-Silicium und ähnliches, enthält.

13. Verfahren nach Anspruch 1, wobei der cMUT, zumindest teilweise, unter Anwendung einer plasmaunterstützten chemischen Gasphasenabscheidung (PECVD) und/oder Niederdruck-Gasphasenabscheidung (LPCVD) hergestellt wird.

14. Verfahren nach Anspruch 1, wobei die Elektrodenplatte (22b) des cMUT-Elements relativ zu der Oberfläche der Substratschicht (20) fixiert wird.

15. Verfahren nach Anspruch 1, wobei die Membran des cMUT-Elements relativ zu einer Oberseite der Substratschicht (20) fixiert wird, um einen Hohlraum zwischen der Membran (24) und der Substratschicht zu definieren.

16. Verfahren nach Anspruch 1, wobei der Elektrodenring (22a) relativ zu einer Oberseite der Membranschicht (24) fixiert wird.

17. Verfahren nach Anspruch 1, wobei das mindestens eine Loch (27) durch die Membran (24) relativ zu dem Mittelpunkt des Elektrodenrings (22a) definiert wird.

18. Verfahren nach Anspruch 1, wobei der Durchmesser des Loches (27) kleiner als der Innendurchmesser des Elektrodenrings (22a) ist.

19. Verfahren nach Anspruch 1, wobei sich der Bereich des Kollabierens der Membranschicht in der Nähe des Loches befindet-

20. Verfahren nach Anspruch 1, wobei die Vorspannung: (i) in dem gesamten Fixier- und Dichtungsprozess aufrechterhalten wird, (ii) vor dem Fixier- und Dichtungsprozess reduziert wird, (iii) während des Fixier- und Dichtungsprozesses reduziert wird; oder (iv) eine Kombination daraus angewandt wird.

21. Verfahren nach Anspruch 1, wobei der cMUT so eingerichtet ist, dass er Ultraschallwellen in einem vorher festgelegten Frequenzbereich erzeugt, wobei der besagte Bereich Frequenzen zwischen etwa 1-5 MHz oder 5-50 MHz umfasst.

22. cMUT-Bauelement, umfassend: (i) eine Substratschicht (20), (ii) eine Elektrodenplatte (22b), (iii) einen Elektrodenring (22a), (iv) eine Membranschicht (24), wobei die Membran (24) mindestens ein Loch (27) aufweist und relativ zu der Substratschicht (20) kollabiert wird, sowie (v) eine Hüllschicht (28), die auf die Membranschicht (24) aufgetragen wird und so vorgesehen ist, dass sie die Membranschicht (24) relativ zu dem Substrat (20) fixiert und kapselt.

23. Integrierte Anordnung, umfassend:

das cMUT-Bauelement nach Anspruch 22; sowie
eine integrierte Schaltung/Chip, die/der Beam-Steering-Funktionalität enthält;
wobei der vor-kollabierte cMUT und die integrierte Beam-Steering Schaltung/Chip zueinander montiert sind, um eine integrierte Einheit zu definieren.

24. Gehäuste, c-MUT-enthaltende Einheit, umfassend:

das cMUT-Bauelement nach Anspruch 22 allein oder in Kombination mit einer integrierten Schaltung/Chip;
mindestens ein Bond-Pad in Kommunikation mit einer leitenden Zwischenverbindung; sowie
eine, eine Energiebahn umgebende Fließbarriere.

25. Gehäuste Einheit nach Anspruch 24, wobei die Fließbarriere aus einem Fotoresistmaterial hergestellt ist.

Revendications

1. Procédé de production d'un cMUT, comprenant :

la fourniture d'un cMUT presque achevé, dans lequel le cMUT presque achevé définit un ou plusieurs éléments cMUT comprenant : (i) une couche de substrat (20), (ii) une plaque d'électrode (22b), (iii) une couche de membrane (24), et (iv) un anneau d'électrode (22a), définissant au moins un trou (27) à travers la couche de membrane (24) pour chaque élément cMUT,
l'application d'une tension de polarisation à travers la couche de membrane (24) et la couche de substrat (20) de l'un ou plusieurs éléments cMUT de manière à affaisser la couche de membrane (24) par rapport à la couche de substrat (20),
la fixation et le scellage de la couche de membrane affaissée (24) par rapport à la couche de substrat (20) par l'application d'une couche de recouvrement (28).

2. Procédé selon la revendication 1, comprenant en outre : (i) la discontinuation de la tension de polarisation, (ii) la réduction de la tension de polarisation à une tension de fonctionnement, ou (iii) une combinaison de ce qui précède.

3. Procédé selon la revendication 1, dans lequel la tension de polarisation est une tension CC bien définie fournie par une batterie.

4. Procédé selon la revendication 3, dans lequel la tension CC bien définie est entre 10 et 250 V.

5. Procédé selon la revendication 1, dans lequel la tension de polarisation est efficace pour réguler la quantité d'affaissement.

6. Procédé selon la revendication 5, dans lequel la régulation de la quantité d'affaissement est efficace pour optimiser les performances.

7. Procédé selon la revendication 1, dans lequel l'un

ou plusieurs trous (27) ont un diamètre entre environ 1 et 25 microns.

8. Procédé selon la revendication 1, dans lequel les trous (27) sont définis en utilisant une technique de lithographie optique sélectionnée dans le groupe se composant d'une lithographie de ligne g, une lithographie de ligne i, une lithographie par nano-empreinte et une lithographie par faisceau d'électrons.

9. Procédé selon la revendication 1, dans lequel l'électrode (22b) est une plaque d'électrode circulaire fabriquée à partir d'un matériau conducteur (métal ou non-métal).

10. Procédé selon la revendication 9, dans lequel le diamètre extérieur de l'anneau d'électrode est configuré et dimensionné pour correspondre sensiblement au diamètre de la plaque d'électrode circulaire et dans lequel le centre de l'anneau d'électrode et le centre de la plaque d'électrode circulaire sont sensiblement alignés.

11. Procédé selon la revendication 1, dans lequel la couche de substrat (20) comprend du silicium.

12. Procédé selon la revendication 1, dans lequel la couche de membrane (24) comprend un matériau compatible CMOS, par exemple un nitrure (par exemple du nitrure de silicium), un oxyde (diverses catégories), du tétra éthyle oxysilane (TEOS), du polysilicium et des éléments similaires.

13. Procédé selon la revendication 1, dans lequel le cMUT est fabriqué, au moins en partie, par dépôt chimique en phase vapeur activé par plasma (PECVD) et/ou par dépôt chimique en phase vapeur à basse pression (LPCVD).

14. Procédé selon la revendication 1, dans lequel la plaque d'électrode (22b) de l'élément cMUT est fixe par rapport à la surface supérieure de la couche de substrat (20).

15. Procédé selon la revendication 1, dans lequel la membrane de l'élément cMUT est fixe par rapport à une face supérieure de la couche de substrat (20) de manière à définir une cavité entre la membrane (24) et la couche de substrat (20).

16. Procédé selon la revendication 1, dans lequel l'anneau d'électrode (22a) est fixe par rapport à une face supérieure de la couche de membrane (24).

17. Procédé selon la revendication 1, dans lequel au moins un trou (27) est défini à travers la membrane (24) par rapport au centre de l'anneau d'électrode (22a).

18. Procédé selon la revendication 1, dans lequel le diamètre du trou (27) est inférieur au diamètre intérieur de l'anneau d'électrode (22a).

19. Procédé selon la revendication 1, dans lequel la zone d'affaissement de la couche de membrane est à proximité du trou.

20. Procédé selon la revendication 1, dans lequel la tension de polarisation est : (i) maintenue par le processus de fixation et de scellage, (ii) réduite avant le processus de fixation et de scellage, (iii) réduite pendant le processus de fixation et de scellage ; ou (iv) une combinaison de ce qui précède.

21. Procédé selon la revendication 1, dans lequel le cMUT est apte à produire des ondes ultrasonores dans une plage de fréquences prédéterminée, ladite plage comprenant des fréquences entre environ 1 et 5 MHz ou 5 et 50 MHz.

22. Dispositif cMUT comprenant : (i) une couche de substrat (20), (ii) une plaque d'électrode (22b), (iii) un anneau d'électrode (22a), (iv) une couche de membrane (24), dans lequel la membrane (24) comporte au moins un trou (27) et est affaissée par rapport à la couche de substrat (20), et (v) une couche de recouvrement (28) appliquée à la couche de membrane (24) et apte à fixer et sceller la couche de membrane (24) par rapport au substrat (20).

23. Ensemble intégré, comprenant :

le dispositif cMUT selon la revendication 22 ; et
un circuit intégré/une puce comprenant une fonctionnalité de direction de faisceau ;
dans lequel le cMUT pré-affaissé et le circuit intégré/la puce de direction de faisceau sont montés l'un par rapport à l'autre pour définir une unité intégrée.

24. Unité conditionnée contenant un cMUT, comprenant :

le dispositif cMUT selon la revendication 22 seul ou en combinaison avec un circuit intégré/une puce :

au moins une plage de contact en communication avec une interconnexion conductrice : et
une barrière de flux entourant une voie d'énergie.

25. Unité conditionnée selon la revendication 24, dans laquelle la barrière de flux est constituée d'un matériau de photoréserve.

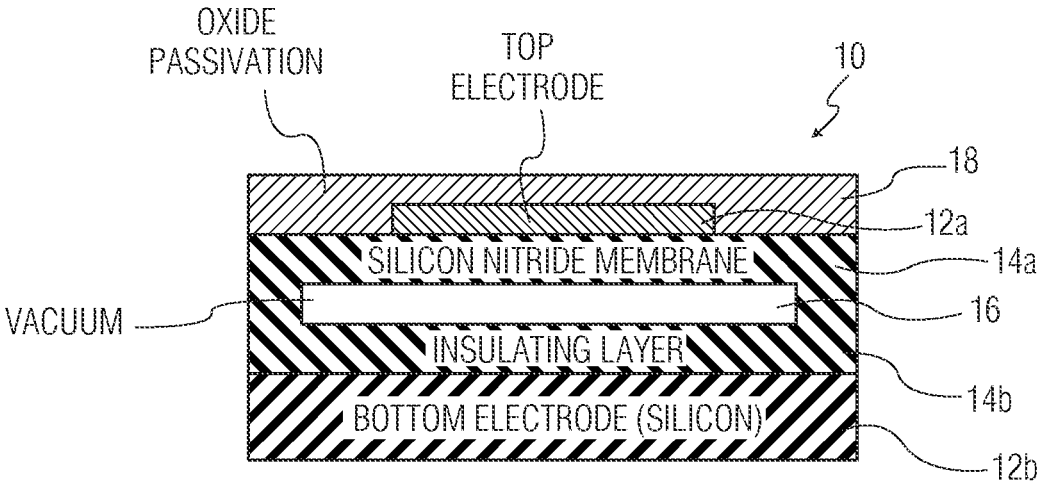


FIG. 1

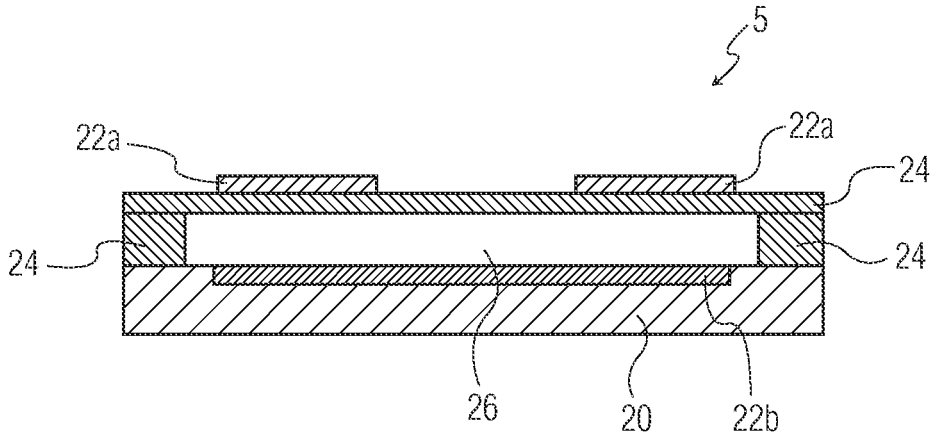


FIG. 2

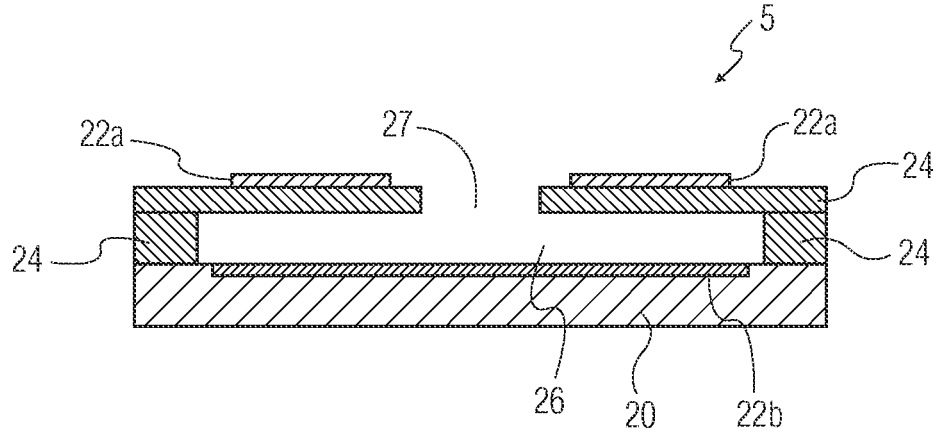


FIG. 3

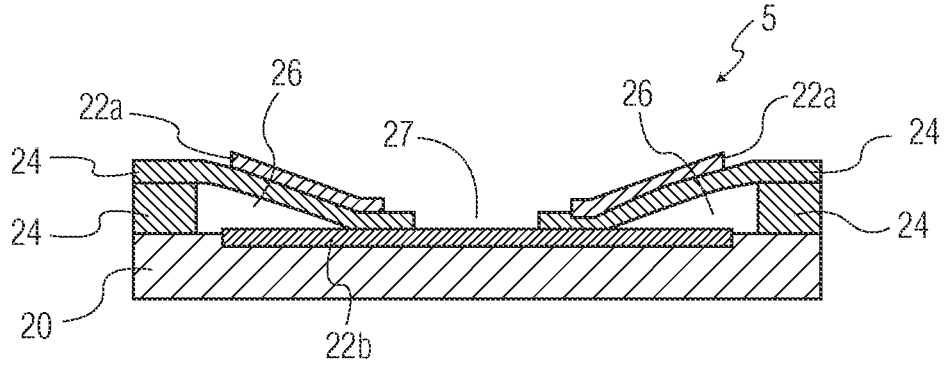


FIG. 4

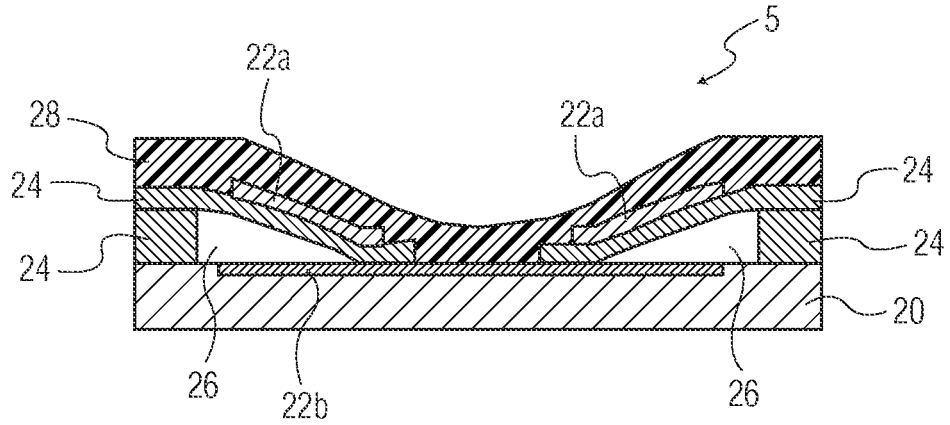


FIG. 5

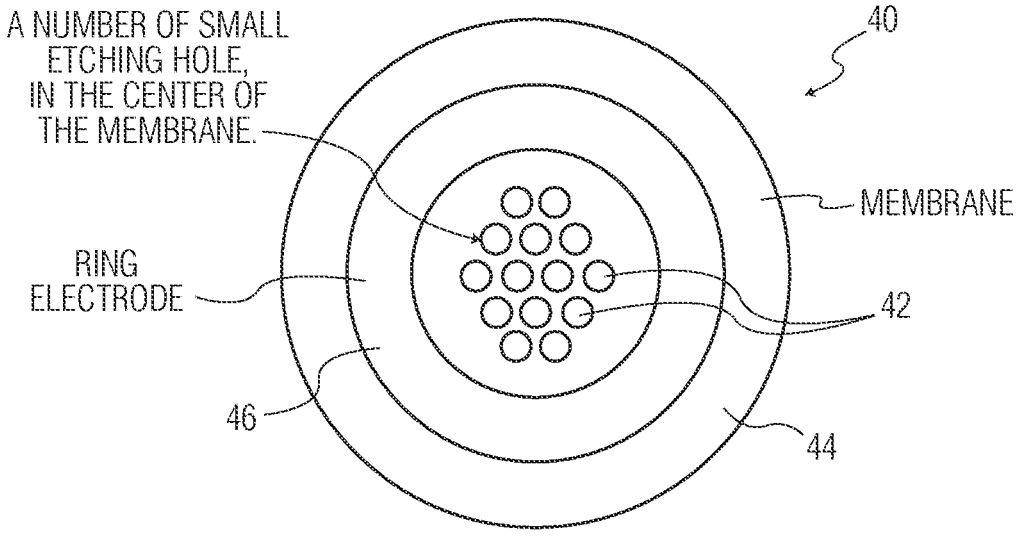


FIG. 6

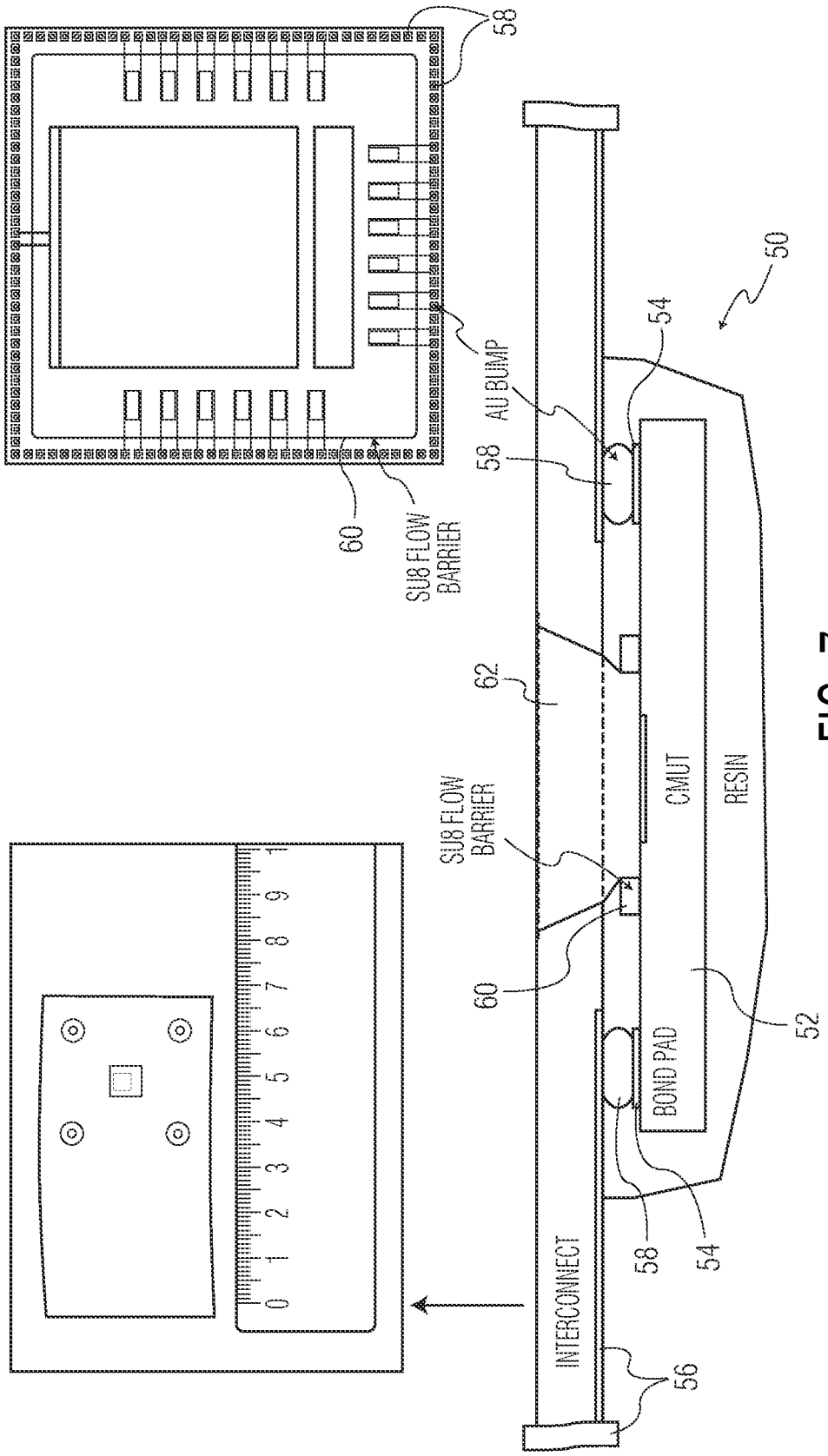

58
AU BUMP
58
60
SU8 FLOW BARRIER
50
54
62
SU8 FLOW BARRIER
CMUT
RESIN
60
52
BOND PAD
58
54
INTERCONNECT
56
0 1 2 3 4 5 6 7 8 9 1

FIG. 7

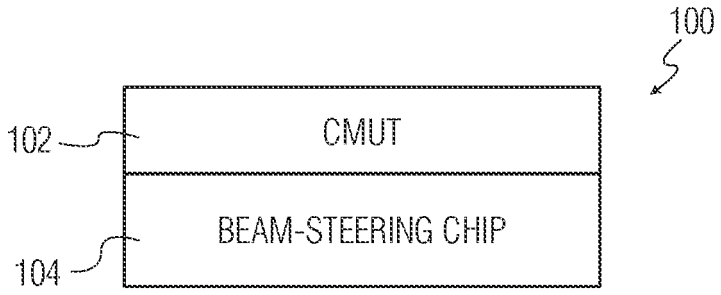


FIG. 8

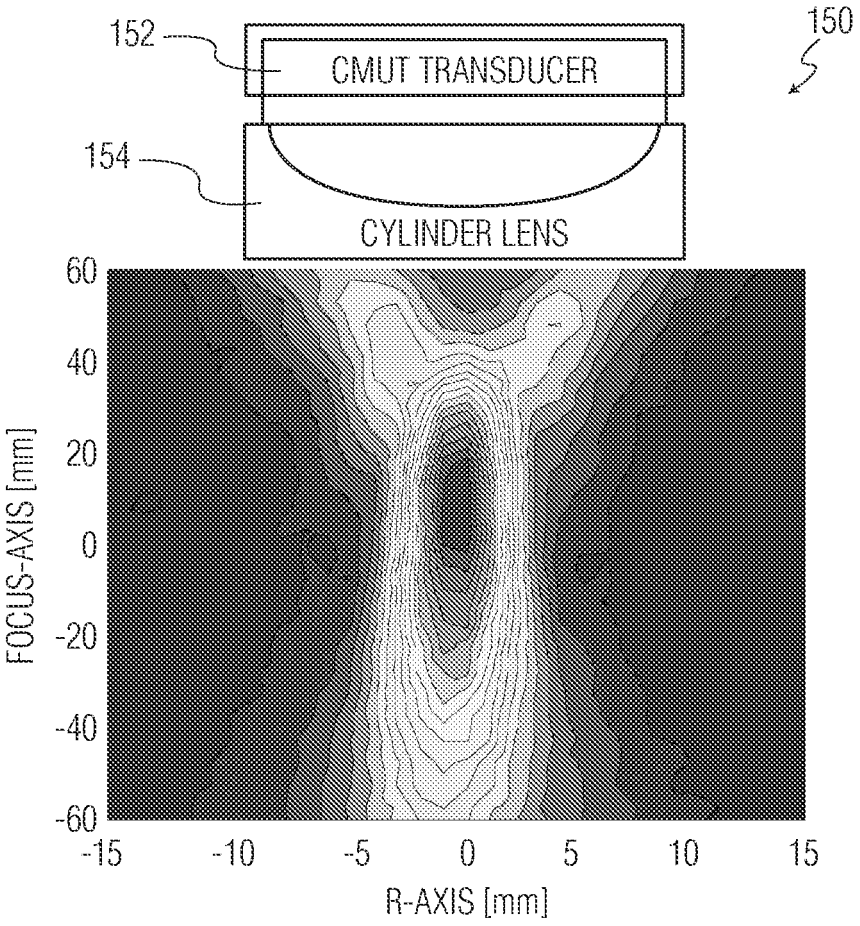
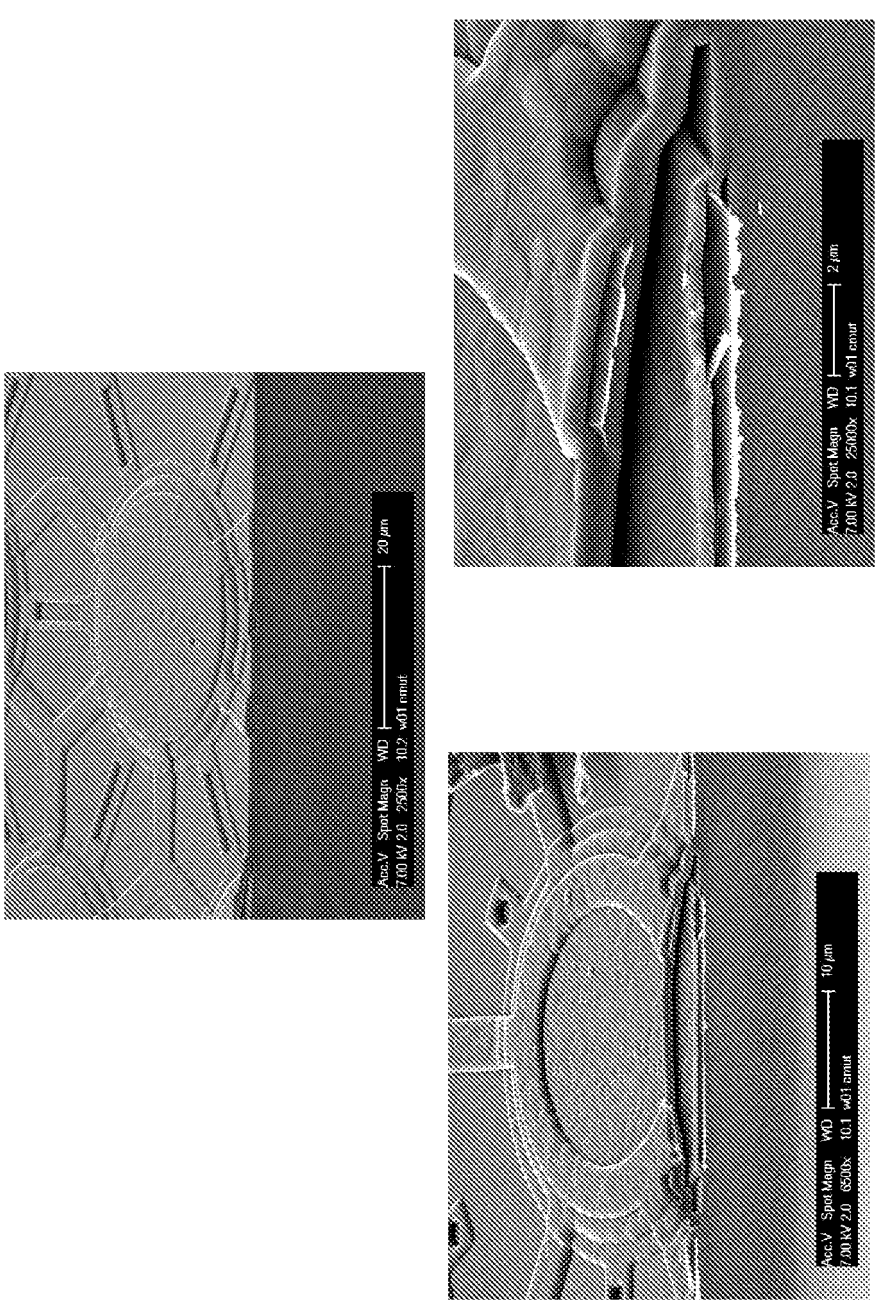

152
CMUT TRANSDUCER
150
154
CYLINDER LENS
60
40
20
0
-20
-40
-60
FOCUS-AXIS [mm]
-15
-10
-5
0
5
10
15
R-AXIS [mm]

FIG. 9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7.00 kV 2.0 2500x 10.2 x01 cmut
Acc.V Spot Magn WD 2 µm
7.00 kV 2.0 25000x 10.1 x01 cmut
Acc.V Spot Magn WD 10 µm
7.00 kV 2.0 6500x 10.1 x01 cmut

FIG. 10

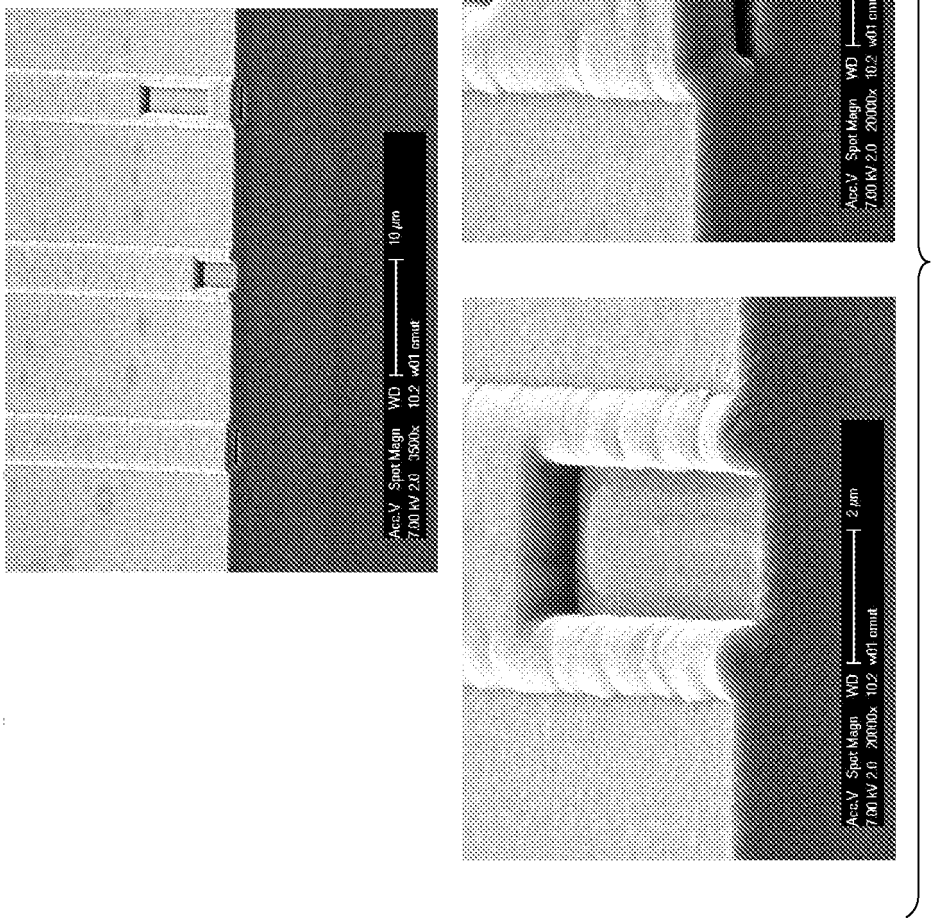
Acc.V Spot Magn WD
7.00 kV 2.0 3500x 10.2 w01 cmut
10 µm
Acc.V Spot Magn WD
7.00 kV 2.0 20000x 10.2 w01 cmut
2 µm
Acc.V Spot Magn WD
7.00 kV 2.0 20000x 10.2 w01 cmut
2 µm

FIG. 11

REFERENCES CITED IN THE DESCRIPTION

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- US 2005200241 A1 **[0006]**
- EP 1764162 A **[0007]**

Non-patent literature cited in the description

- **A. S. ERGUN et al.** Capacitive Micromachined Ultrasonic Transducers: Fabrication Technology. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control,* December 2005, vol. 52 (12 **[0005]**
- A new package for silicon biosensors. *EMPC,* 12 June 2005 **[0039]**

专利名称(译)	预塌陷的电容式微机械超声换能器的制造及其应用		
公开(公告)号	EP2207484B1	公开(公告)日	2016-11-09
申请号	EP2008807701	申请日	2008-09-17
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司		
申请(专利权)人(译)	皇家飞利浦电子N.V.		
当前申请(专利权)人(译)	皇家飞利浦N.V.		
[标]发明人	DIRKSEN PETER VAN DER LUGT ANTHONIE		
发明人	DIRKSEN, PETER VAN DER LUGT, ANTHONIE		
IPC分类号	A61B8/00 B06B1/02		
CPC分类号	B06B1/0292 A61B8/00 H04R19/005 Y10T29/43 Y10T29/49005 Y10T29/4908		
优先权	60/972836 2007-09-17 US		
其他公开文献	EP2207484A2		
外部链接	Espacenet		

摘要(译)

提供了用于制造预塌陷的电容式微机械超声换能器（cMUT）的方法。所公开的方法通常包括以下步骤：在蚀刻和密封膜之前获得几乎完成的传统cMUT结构，为每个相对于膜的顶面固定的电极环限定穿过cMUT结构的膜的孔，施加偏压cMUT结构的膜和基底，以便将靠近孔的膜区域折叠到基底或朝向基底，通过施加包覆层将膜的收缩区域固定和密封到基底，并且中断或减少偏压。提供CMUT组件，包括封装组件，具有集成电路/芯片（例如，光束控制芯片）和cMUT /透镜组件的集成组件。还提供了利用所公开的预塌陷cMUT的有利的基于cMUT的应用，例如基于超声换能器的应用，基于导管的应用，基于针的应用和流量计应用。

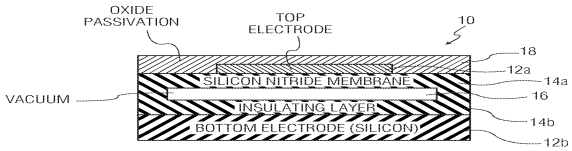

FIG. 1

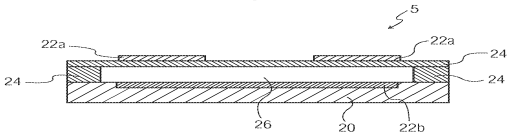

FIG. 2

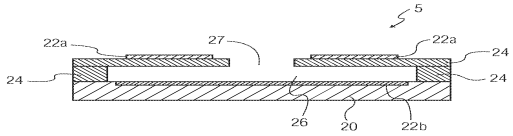

FIG. 3