



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
20.08.2014 Bulletin 2014/34

(51) Int Cl.:
A61B 5/04 (2006.01) **A61B 5/00** (2006.01)
G01R 35/00 (2006.01) **G01R 27/14** (2006.01)

(21) Application number: **14155380.0**

(22) Date of filing: **17.02.2014**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(71) Applicant: **IMEC**
3001 Leuven (BE)

(72) Inventors:
• **Yazicioglu, Refet Firat**
3001 Leuven (BE)
• **Kim, Sunyoung**
3001 Leuven (BE)

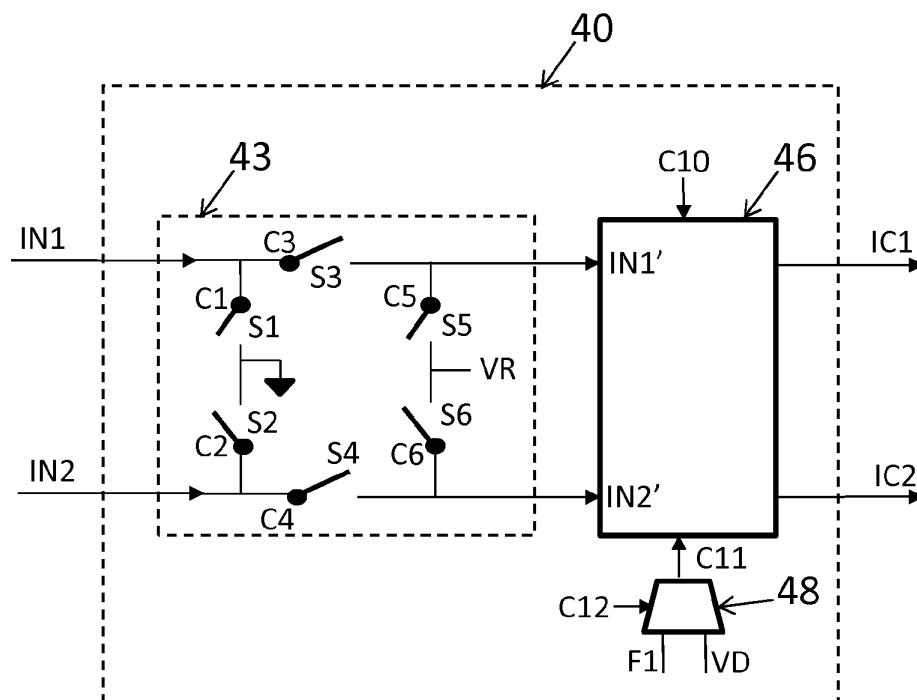
(30) Priority: **15.02.2013 EP 13155550**

(54) **Circuit, system and method for impedance measurements**

(57) The invention relates to a circuit (40) for impedance measurement comprising a switch matrix (43) connected to a chopper (46). The switch matrix (43) comprises a plurality of switches (S1 to S6) and is configured to receive an analogue signal (IN1, IN2). In operation, during a calibration period (PH1), the circuit (40) is configured to activate the chopper (46) and to control the switch matrix (43) in order to disconnect the received analog signal (IN1, IN2) from the chopper inputs (IN1',

IN2') and to connect a voltage reference signal (VR) to the chopper inputs (IN1', IN2'). In operation, during a measurement period (PH2), the circuit (40) is configured to deactivate the chopper (46) and to control the switch matrix (43) in order to disconnect the voltage reference signal (VR) from the chopper inputs (IN1', IN2') and to connect the received analog signal (IN1, IN2) to the chopper inputs (IN1', IN2'). The invention also relates to a system and to a method for impedance measurement.

Figure 3



Description

Technical Field

[0001] The present disclosure relates generally to systems and devices for performing measurement of physical qualities based on a change of an electrical impedance, and more specifically to impedance measurement circuits and methods.

Background

[0002] Conventional impedance measurement systems and circuits are generally based on injecting a differential current signal into the unknown source of impedance and measuring the resulting differential voltage. Biomedical application systems often require high precision impedance measurements, for example down to milliohm range to detect variable impedance changes superimposed on up to kilo-ohm range baseline impedances. The limitations of integrated circuit design, due to the effect of non-linearity, mismatch, and offset, lead to errors and reduce the accuracy of such impedance measurements. Therefore, there is the need to improve the accuracy and/or reduce error when measuring an electrical impedance.

[0003] A known biomedical acquisition system that performs impedance monitoring using two-terminals, also known as a bipolar electrode configuration, is disclosed in patent application EP 2 298 164. The impedance measurement circuit, as in the exemplary embodiment shown in figure 27 of that document, comprises two AC stimulation current sources that generate a differential mode stimulation current through two electrodes. Additionally, an impedance readout circuit in the analogue domain is configured to extract, from the analogue signals received from those two electrodes, the imaginary and real parts of the measured electrode-tissue impedance.

Summary

[0004] According to one aspect of the present invention, a new circuit and system with improved impedance measurement is provided. According to another aspects, the invention is also advantageous for use in ambulatory and/or low power biomedical monitoring applications. The invention is particularly advantageous for the measurements of bio-impedance information. Other possible applications are, for example, galvanic skin response or skin impedance measurement, impedance cardiography or contact impedance.

[0005] According to an exemplary embodiment, there is provided a circuit for impedance measurement comprising a switch matrix connected to a chopper; wherein the switch matrix comprises a plurality of switches and is configured to receive an analogue signal; wherein, in operation, during a calibration period, the circuit is con-

figured to activate the chopper and to control the switch matrix in order to disconnect the received analog signal from the chopper inputs and to connect a voltage reference signal to the chopper inputs; and wherein, in operation, during a measurement period, the circuit is configured to deactivate the chopper and to control the switch matrix in order to disconnect the voltage reference signal from the chopper inputs and to connect the received analog signal to the chopper inputs.

[0006] According to an exemplary embodiment, there is provided a system for impedance measurement configured to receive an analogue sensor signal sensed from an element that presents a certain electrical impedance; wherein the system comprises a circuit according to claim 1; an analogue impedance readout unit configured to calculate, derived from said analogue sensor signal, an impedance value signal of the electrical impedance; wherein, in operation, during the calibration period, the system is configured to calculate an offset error of the analogue impedance readout unit; and wherein, in operation, during the measurement period, the system is configured to measure impedance value signals of the electrical impedance.

[0007] According to an exemplary embodiment, the system further comprises an ADC unit configured to digitize the impedance signal generated by the analogue impedance readout unit; and a DSP unit configured to receive a digital version of the impedance signal and to store it in a memory unit; wherein, in operation, during the calibration period, the DSP unit is configured to store a value of an offset error related to the analogue impedance readout unit and the ADC unit; and wherein, in operation, during the measurement period, the DSP unit is configured to calculate an electrical impedance value by subtracting the offset error from the digitized impedance value signal calculated at the analogue impedance readout unit.

[0008] According to an exemplary embodiment, the system further comprises a current generator unit configured to generate a differential alternate current signal to an element that presents a certain electrical impedance.

[0009] According to an exemplary embodiment, during the calibration period, the circuit is configured to activate the chopper by providing a frequency signal which has the same frequency as the differential alternate current signal generated by the current generator unit.

[0010] According to an exemplary embodiment, the system further comprises a high-pass filter unit configured to adapt the received analogue sensor signal so as to reject DC offset.

[0011] According to an exemplary embodiment, the calculated offset error comprises a DC offset and drift due to process, voltage and temperature variations of the analogue impedance readout unit.

[0012] According to an exemplary embodiment, the impedance measurement is a bio-impedance measurement.

[0013] There is also provided a biopotential signal acquisition system and an electronic device comprising a circuit for impedance measurements according to any of the embodiments herein described.

[0014] There is also provided a method for impedance measurement comprising, in a system according to any of claims 2 to 8; calculating, during a calibration period, an impedance offset error value of an analogue impedance readout unit; and calculating, during a measurement period, an electrical impedance value by subtracting the calculated offset error value from the impedance value signal measured by the analogue impedance readout unit.

[0015] Advantageously, by using the circuit and system according to exemplary embodiments of the invention, the offset error in the analogue readout channel is advantageously reduced. The offset error may include process, temperature and/or voltage variations. According to exemplary embodiments, in operation, an calculation error correction is performed, first measuring the error in the analogue readout channel and then subtracting this error from the impedance measurements. Advantageously, impedance measurement accuracy is increased. According to exemplary embodiments, the solution improves the accuracy of a DC bio-impedance measurement.

[0016] Certain objects and advantages of various new and inventive aspects have been described above. It is to be understood that not necessarily all such objects or advantages may be achieved in accordance with any particular embodiment of the present invention. Those skilled in the art will recognize that the solution of the present invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages without necessarily achieving other objects or advantages.

Brief description of the drawings

[0017] The above and other aspects of the circuit, system and method for impedance measurement according to the present invention will be shown and explained with reference to the non-restrictive example embodiments described hereinafter.

Figure 1 shows a first exemplary block diagram of a system for impedance measurements according to an embodiment of the invention.

Figure 2 shows a second exemplary block diagram of a system for impedance measurements according to an embodiment of the invention.

Figure 3 shows a first exemplary block diagram of a circuit for impedance measurements according to an embodiment of the invention.

Figure 4 shows a second exemplary block diagram of a circuit for impedance measurements according to an embodiment of the invention.

Figures 5A and 5B show a third exemplary block

diagram of a circuit for impedance measurements in operation according to an embodiment of the invention.

Figures 6A and 6B show a fourth exemplary block diagram of a circuit for impedance measurements in operation according to an embodiment of the invention.

Figures 7A and 7B show a fifth exemplary block diagram of a circuit for impedance measurements in operation according to an embodiment of the invention.

Figure 8 illustrates a flow diagram of a method for impedance measurements according to an embodiment of the invention.

Figure 9 illustrates a third exemplary block diagram of a system for impedance measurements according to an embodiment of the invention.

Detailed description

[0018] In the following, in the description of exemplary embodiments, various features may be grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This is however not to be interpreted as the invention requiring more features than the ones expressly recited in the main claim. Furthermore, combinations of features of different embodiments are meant to be within the scope of the invention, as would be clearly understood by those skilled in the art. Additionally, in other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure the conciseness of the description.

[0019] **Figure 1** shows a first exemplary block diagram of a system for impedance measurements according to an embodiment of the invention. Such a system may be, for example, a biopotential signal acquisition system, in connection with the acquisition of biopotential signals such as electrocardiogram (ECG), electroencephalogram (EEG) or electromyogram (EMG) signals. The system may comprise a current generator unit **10**, a high-pass filter (HPF) unit **30**, a calibration unit **40** and an impedance readout unit **50**. The calibration unit **40** and an impedance readout unit **50** are implemented, according to an embodiment of the invention, in an analogue domain part **60** of the system. The current generator unit **10** is configured to generate a differential alternate current signal **I1, I2** to an element **20** that presents a certain electrical impedance **Z**, such as, for example, a living being body. By means of electrode sensors connected to that element **20**, analogue sensor signals **S1, S2** are generated and passed through a HPF **30**, which, according to an exemplary embodiment, implements a first order filter with a cut-off frequency that rejects large direct current (DC) offset. According to an exemplary embodiment, the cut-off frequency is lower than the frequency of the stimulation current or input voltage. Then, the calibration

unit **40** is configured to receive the analogue signals **IN1**, **IN2** at the output of the HPF unit **30** and to control and modify those signals for impedance measurement calibration purposes. The output analogue signals **IC1**, **IC2** of the calibration unit **40** are then provided to an analogue impedance readout unit **50**, which is configured to calculate impedance value signals **IMP1**, **IMP2** of the electrical impedance **Z** associated to the subject element **20**. According to an exemplary embodiment, the analogue impedance readout unit **50** is configured to extract a real and an imaginary impedance value associated to the measured subject's electrical impedance **Z**.

[0020] The current generator unit **10**, the high-pass filter (HPF) unit **30** and an impedance readout unit **50** may be implemented as disclosed in patent application EP 2 298 164, but it is understood that there are other design options to implement the functionality of each of those units. The present disclosure focuses on the development of new and inventive calibration unit **40** or circuit for impedance measurement, together with a system and method for impedance measurements which allows compensation of impedance measurement errors introduced by the analogue impedance readout unit **50**.

[0021] Additionally, according to an embodiment of the present invention, the system performs impedance measurements employing a tetra-polar electrode configuration, which means that the current source electrodes are physically separated from the sensing voltage electrodes. Advantageously, this configuration provides higher impedance measurement accuracy than a system for impedance measurements with a bipolar electrode configuration.

[0022] **Figure 2** shows a second exemplary block diagram of a system for impedance measurements according to an embodiment of the invention. The system may comprise the same units as the ones shown in **Figure 1** and additionally an analogue-to-digital converter (ADC) unit **70** which digitizes the impedance signals **IMP1**, **IMP2** and provides a digital version **D1**, **D2** to a digital signal processing (DSP) unit **80**. The solution according to an embodiment of the invention is advantageous due to the fact that the value (or an averaged value) of the impedance signals **IMP1**, **IMP2** can be stored in a memory unit during a calibration phase. Advantageously, by storing the value of the impedance signals **IMP1**, **IMP2** associated to calibration, the need for continuous recalibration of the system is avoided. According to an exemplary embodiment, such memory unit is comprised in the DSP unit **80**. Furthermore, according to an embodiment of the invention, there is provided a calibration unit **40** and a method for calibration of impedance measurements which allows compensation of the impedance measurement errors introduced by the analogue impedance readout unit **50** and the analogue-to-digital converter (ADC) unit **70**.

[0023] **Figure 3** shows a first simplified block diagram of a calibration unit **40** according to an exemplary embodiment of the invention. Schematically, it comprises a

switch matrix **43** connected to a chopper **46**. The switch matrix **43**, according to an embodiment of the invention, comprises six switches **S1** to **S6** controlled by a respective switch control signal **C1** to **C6**. The chopper **46** is controlled by a multiplexer **48**, which provides a first control signal **C11** depending on the value of a selection signal **C12**. The first control signal **C11** of the chopper **46** may be a frequency signal **F1** for modulation purposes when the chopper is in operation (activated) or a voltage signal **VD** when the chopper is deactivated. The chopper also receives a second control signal **C10** which is related to the value of the first control signal **C11**.

[0024] **Figure 4** shows a second exemplary block diagram of a calibration unit **40** according to an embodiment of the invention, which schematically illustrates the relation of the values of the control signals of **Figure 3**. For example, the first, second, fifth and sixth switches **S1**, **S2**, **S5**, **S6** and the multiplexer **48** are controlled by the same first switch control signal **C1'**. The third and fourth switches **S3**, **S4** are controlled by the inverse value **/C1'** of the first switch control signal. The chopper is controlled by the first chopper control signal **CP'** and the inverse value **/CP'** of that signal.

[0025] The chopper **46** may be implemented as disclosed in "A CMOS chopper amplifier", by Christian Enz, IEEE Journal of Solid-State Circuits, Vol. SC-22, no 3, June 1987. According to an embodiment of the invention, the frequency signal **F1'** is the demodulation frequency at 0 degrees as used in the analogue impedance readout unit **50** implemented as disclosed in patent application EP 2 298 164.

[0026] According to an exemplary embodiment, the frequency signal **F1'** may be the same as the frequency of the current **I1**, **I2** injected by the current generator unit **10**.

[0027] **Figure 5A** shows a third exemplary block diagram of a calibration unit **40**, in operation during a calibration phase **PH1**, according to an embodiment of the invention. During the calibration phase **PH1**, the first, second, fifth and sixth switches **S1**, **S2**, **S5**, **S6** are closed and the third and fourth switches **S3**, **S4** are opened so that the analogue calibration unit input signals **IN1**, **IN2** are disconnected from the chopper inputs **IN1'**, **IN2'**. The analogue calibration unit input signals **IN1**, **IN2** are connected to a ground reference, the inputs of the chopper **46** are connected to a voltage reference signal **VR** and the chopper is activated by providing the frequency signal **F1** as the first control signal **C11**.

[0028] Advantageously, according to an embodiment of the invention, during the calibration phase **PH1**, the impedance signals **IMP11**, **IMP21** as shown in **Figure 5B** comprise the offset error of the analogue impedance readout unit **50**. The stored offset error may be the combination of the systematic and random offset of the building blocks of the impedance readout unit. According to another exemplary embodiment, the impedance signals **IMP11**, **IMP21**, during the calibration phase **PH1**, comprise the value of the DC offset and drift due to process,

voltage and temperature variations of the analogue impedance readout unit **50**. According to an exemplary embodiment, and in reference to **Figure 2**, the digital versions **D1**, **D2** of the impedance signals **IMP11**, **IMP21** further comprise, during the calibration phase **PH1**, the offset error of the ADC unit **70**. According to an exemplary embodiment, the value (or an averaged value) of the impedance signals **IMP11**, **IMP21** is, during the calibration phase **PH1**, stored in the memory of the DSP unit **80**.

[0029] Another possible embodiment of the switch matrix **43**, in operation during a calibration phase **PH1**, is shown in **Figure 7A**. According to an exemplary embodiment, the switch matrix **43** does not comprise the first and the second switches **S1**, **S2**. During the calibration phase **PH1**, the fifth and sixth switches **S5**, **S6** are closed and the third and fourth switches **S3**, **S4** are opened so that the analogue calibration unit input signals **IN1**, **IN2** are disconnected from the chopper **46** and the chopper inputs **IN1'**, **IN2'** are connected to a voltage reference signal **VR**.

[0030] **Figures 6A** shows a fourth exemplary block diagram of a calibration unit **40**, in operation during a measurement phase **PH2**, according to an embodiment of the invention. During the measurement phase **PH2**, the first, second, fifth and sixth switches **S1**, **S2**, **S5**, **S6** are opened and the third and fourth switches **S3**, **S4** are closed so that the analogue calibration unit input signals **IN1**, **IN2** are connected to the chopper **46**. The voltage reference signal **VR** is disconnected from the chopper inputs and the chopper is deactivated by providing a voltage signal **VD** as the first control signal **C11**. Since the chopper is deactivated, the calibration unit **40** lets the input signals **IN1**, **IN2** go through to the analogue impedance readout unit **50**, which then measures the voltage value generated on the impedance **Z** by the injected current **I1**, **I2**. During the measurement phase **PH2**, the impedance signals **IMP12**, **IMP22**, as shown in **Figure 6B**, comprise the value of the measured electrical impedance **Z** and the offset error of the analogue impedance readout unit **50**. Furthermore, according to an exemplary embodiment in reference to **Figure 2**, the digital versions **D1**, **D2** of the impedance signals **IMP12**, **IMP22** further comprise, during the measurement phase **PH2**, the offset error of the ADC unit **70**.

[0031] Advantageously, according to an embodiment of the invention, during the measurement phase **PH2**, the value of the impedance signals **IMP11**, **IMP21** obtained during the calibration phase **PH1**, is subtracted from the value of the impedance signals **IMP12**, **IMP22** obtained during the measurement phase **PH2**. Therefore, the system, during the measurement phase **PH2**, provides a value for the measured electrical impedance **Z** that does not contain the offset error of the analogue impedance readout unit **50**. According to another exemplary embodiment, the system, during the measurement phase **PH2**, provides a value for the measured electrical impedance **Z** that does not contain the offset error of both the analogue impedance readout unit **50** and the ADC

unit **70**.

[0032] Advantageously, according to an embodiment of the invention, the accuracy of a DC bio-impedance measurement is increased, particularly for baseline impedance measurements.

[0033] Another possible embodiment of the switch matrix **43**, in operation during a measurement phase **PH2**, is shown in **Figure 7B**. According to an exemplary embodiment, the switch matrix **43** does not comprise the first and the second switches **S1**, **S2**. During the measurement phase **PH2**, the fifth and sixth switches **S5**, **S6** are opened and the third and fourth switches **S3**, **S4** are closed so that the analogue calibration unit input signals **IN1**, **IN2** are connected to the chopper **46** and the voltage reference signal **VR** is disconnected from the chopper inputs.

[0034] **Figure 8** illustrates a flow diagram of a method for impedance measurements according to an embodiment of the invention.

[0035] The method comprises, in a first phase or calibration phase **PH1**, calculating the impedance offset error value of an analogue impedance readout unit **50** (as in the system shown in **Figure 1**). According to an exemplary embodiment, the method further comprises, in a first phase or calibration phase **PH1**, further calculating the offset error of an ADC unit **70**, as in the system shown in **Figure 2**. According to an exemplary embodiment, the method further comprises, in a first phase or calibration phase **PH1**, storing the calculated offset error in a memory unit. According to an exemplary embodiment, the impedance measurement is a bio-impedance measurement and the offset error of the analogue impedance readout unit **50** or the ADC unit **70** comprises a DC bio-impedance offset error.

[0036] The method further comprises, in a second phase or measurement phase **PH2**, measuring the electrical impedance value **Z** of a subject element **20** (as in the system shown in **Figure 1**) and subtracting from that measured electrical impedance value, the impedance offset error value calculated during first phase or calibration phase **PH1**.

[0037] According to an exemplary embodiment, the impedance offset error value and the measured electrical impedance value are voltage values.

[0038] According to an exemplary embodiment, the method for impedance measurements according to the invention is implemented in a system (as in **Figure 1** or **Figure 2**) comprising a calibration unit **40** according to any of the embodiments herein claimed. Additionally, the method for impedance measurements according to the invention may make use of a DSP unit **80**.

[0039] The calibration phase and the measurement phase are performed during determined periods of time, which can be selected by design. The calibration phase may be performed once or repeated at specific steps or events of the impedance measurement.

[0040] **Figure 9** illustrates another exemplary block diagram of a system for impedance measurements accord-

ing to an embodiment of the invention, in which the functioning of the DSP unit **80** is further detailed in relation to the system disclosed in **Figures 1 and 2**. During operation of the system, in a calibration phase **PH1**, the voltage values of the calculated impedance offset error **VoffR**, **VoffI** are stored in a memory. According to an exemplary embodiment, the impedance offset error voltage value is averaged during a certain number of operation cycles. Further during operation of the system, in a measurement phase **PH2**, the stored voltage value of the calculated impedance offset error **VoffR**, **VoffI** is subtracted from the voltage value of the measured impedance and from that resulting voltage value, the actual value of the measured impedance is calculated **R{Z}**, **I{Z}**.

[0041] Further exemplary embodiments are here below described. According to an exemplary embodiment, there is provided a new circuit topology and switch matrix for implementing a new method for impedance measurements. Such solution, according to an exemplary embodiment, advantageously enables to sample the error in the impedance measurement readout so that it can be subtracted from actual impedance measurements.

[0042] According to one exemplary embodiment, the solution proposes an error correction mechanisms that first measures the error in the integrated circuits and then subtracts this error from the measurements. According to one exemplary embodiment there is provided a method for impedance measurements comprising: measuring the error of the readout system, sampling the error and subtracting it from the measurement.

[0043] According to an exemplary embodiment of the present description, the input switch matrix is first connected to a known potential, which enables to measure the offset of the readout chain. This offset is stored on the DSP for error correction. Later the impedance measurement is started where the measurements are made and error is subtracted from the recordings.

[0044] Advantageously, according to an exemplary embodiment of the present description, the error is digitized and stored in memory. Therefore it avoids the need for re-calibration.

[0045] According to an exemplary embodiment of the invention, an off-chip HPF will be integrated to interface with the impedance signal path. The impedance signal path comprises an instrumentation amplifier (TC and TI stage), a programmable gain amplifier (PGA), a SC-LPF, and a channel buffer. A test purpose multiplexed buffer (TMPX) may also be integrated to monitor internal node of the channel. Two impedance readout channels are responsible for extracting the in-phase (IMPR) and quadrature (IMPI) components of the bioimpedance.

[0046] The HPF may implement a first order filter with a cut-off frequency between 0.1 Hz and 50 Hz to reject large DC offset at input.

[0047] The instrumentation amplifier itself consists of a transconductance (TC) stage followed by a transimpedance stage (TI). The instrumentation amplifier (IA)

has single ended topology, and it operates inside choppers to improve low frequency noise performance and CMRR. The next building block in the signal path is a programmable-gain amplifier (PGA). This module allows to be configured with different gain settings (6dB-26dB). A reference PGA signal (900mV) is used for the reference node around which the readout path output will be centered. A first order SC-LPF is cascaded after the PGA. This LPF has fixed the BW of IMP signal path to 10Hz. Finally a channel buffer is implemented.

[0048] The offset of the quadrature impedance readout circuit may affect the accuracy of the DC bio-impedance calculation. To improve DC bio-impedance measurement accuracy, a multi-purpose chopper is allocated at IA input. Before bio-impedance evaluation, the switch can short the TC inputs to measure the systematic offsets presented at the output of IMP-I and IMP-Q. After calibration phase, the TC inputs are connected to a complex bio-impedance to measure actual voltage value generated by the injected current.

[0049] To measure accuracy impedance, an implementation proposes two different modes, a calibration mode and a measurement mode. In the calibration mode, both inputs of the impedance channel are connected to an internal voltage reference and a common mode DC output of (VOUT_DC) can be measured. In the measurement mode, the IA input is connected to external HPF capacitor to measure the bio-impedance RBIO. Based on these two measurements, the bio-impedance can be calculated as follows:

$$R_{BIO} = \frac{V_{OUT} - V_{OUT_DC}}{I_{AMP} \times GAIN_{CHN}}$$

where, IAMP is the amplitude of injection current and GAINCHN is the impedance channel gain.

[0050] According to an exemplary embodiment, two quadrature bio-impedance readout channels are used together with a digitized sinusoidal current generator in order to implement an accurate and wide dynamic range bio-impedance measurement.

[0051] According to an exemplary embodiment, to extract both DC and AC bio-impedance components, a non-inverting DC coupled PGA is used, which amplifies the AC bio-impedance while having unity DC gain. This enables a large dynamic range (82dB) bio-impedance readout, which is important as the DC impedance is in general 100 times larger than the AC one. The offset of the quadrature impedance readout circuit may affect the accuracy of the DC bio-impedance calculation. To improve DC bio-impedance measurement accuracy, a multi-purpose chopper is allocated at IA input. Before bio-impedance evaluation, the switch can short the TC inputs to measure the systematic offsets presented at the output of IMP-I and IMP-Q. These offset values are calibrated

in the DSP to improve the system accuracy to 97% (THD is less than 3%).

Claims

1. A circuit (40) for impedance measurement comprising a switch matrix (43) connected to a chopper (46); wherein the switch matrix (43) comprises a plurality of switches (S1 to S6) and is configured to receive an analogue signal (IN1, IN2); wherein, in operation, during a calibration period (PH1), the circuit (40) is configured to activate the chopper (46) and to control the switch matrix (43) in order to disconnect the received analog signal (IN1, IN2) from the chopper inputs (IN1', IN2') and to connect a voltage reference signal (VR) to the chopper inputs (IN1', IN2'); and wherein, in operation, during a measurement period (PH2), the circuit (40) is configured to deactivate the chopper (46) and to control the switch matrix (43) in order to disconnect the voltage reference signal (VR) from the chopper inputs (IN1', IN2') and to connect the received analog signal (IN1, IN2) to the chopper inputs (IN1', IN2').
2. A system for impedance measurement configured to receive an analogue sensor signal (S1, S2) sensed from an element (20) that presents a certain electrical impedance (Z); the system comprising:
 - a calibration circuit (40) according to claim 1 connected to an analogue impedance readout unit (50) configured to calculate, derived from said analogue sensor signal (S1, S2), an impedance value signal (IMP1, IMP2) of the electrical impedance (Z);
 - wherein, in operation, during the calibration period (PH1), the system is configured to calculate an offset error of the analogue impedance readout unit (50); and
 - wherein, in operation, during the measurement period (PH2), the system is configured to measure impedance value signals (IMP1, IMP2) of the electrical impedance (Z).
3. A system for impedance measurement according to claim 2 further comprising:
 - an ADC unit (70) configured to digitize the impedance signal (IMP1, IMP2) generated by the analogue impedance readout unit (50); and
 - a DSP unit (80) configured to receive a digital version of the impedance signal (D1, D2) and to store it in a memory unit;
 - wherein, in operation, during the calibration period (PH1), the DSP unit is configured to store a value of an offset error related to the analogue
- impedance readout unit (50) and the ADC unit (70); and
- wherein, in operation, during the measurement period (PH2), the DSP unit is configured to calculate an electrical impedance value by subtracting the offset error from the digitized impedance value signal calculated at the analogue impedance readout unit (50).
4. A system for impedance measurement according to claim 3 further comprising:
 - a current generator unit (10) configured to generate a differential alternate current signal (I1, I2) that is injected to an element (20) that presents a certain electrical impedance (Z).
5. A system for impedance measurement according to claim 4 wherein, during the calibration period (PH1), the calibration circuit (40) is configured to activate the chopper (46) by providing a frequency signal (F1) which has the same frequency as the differential alternate current signal (I1, I2) generated by the current generator unit (10).
6. A system for impedance measurement according to any of claims 2 to 5 further comprising a high-pass filter unit (30) configured to adapt the received analogue sensor signal (S1, S2) so as to reject DC offset.
7. A system for impedance measurement according to any of the previous claims, wherein the calculated offset error comprises a DC offset and drift due to process, voltage and temperature variations of the analogue impedance readout unit (50).
8. A system for impedance measurement according to any of the previous claims, wherein the impedance measurement is a bio-impedance measurement.
9. A biopotential signal acquisition system comprising a circuit (40) according to claim 1 or a system for impedance measurement according to any of claims 2 to 8.
10. Electronic device comprising a circuit (40) for impedance measurement according to claim 1.
11. A method for impedance measurement comprising:
 - in a system according to any of claims 2 to 8;
 - calculating, during a calibration period (PH1), an impedance offset error value of an analogue impedance readout unit (50); and
 - calculating, during a measurement period (PH2), an electrical impedance value by subtracting the calculated offset error value from the impedance value signal measured by the ana-

logue impedance readout unit (50).

5

10

15

20

25

30

35

40

45

50

55

Figure 1

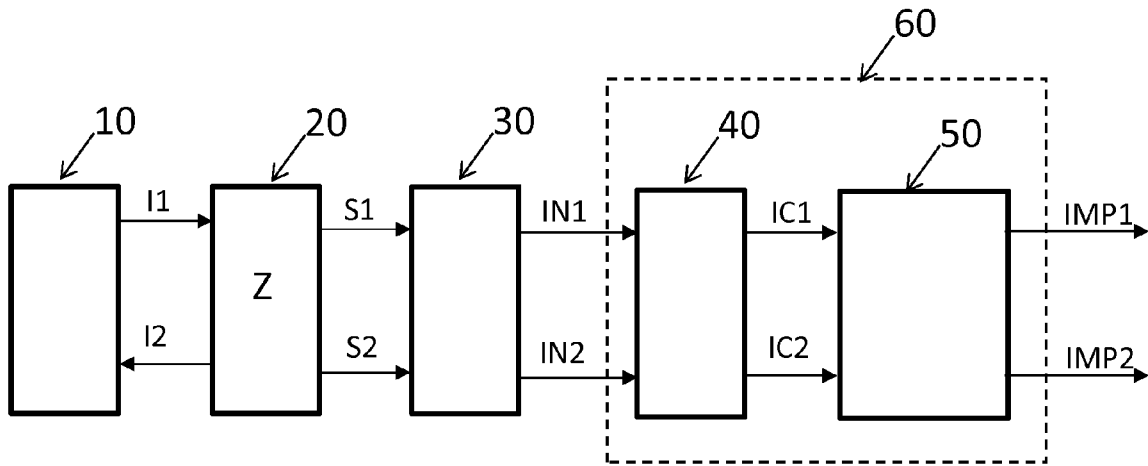


Figure 2

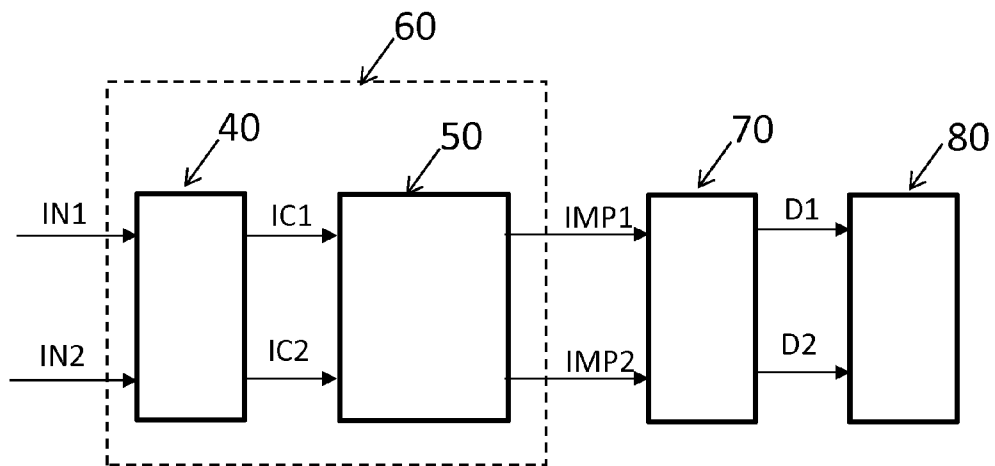


Figure 3

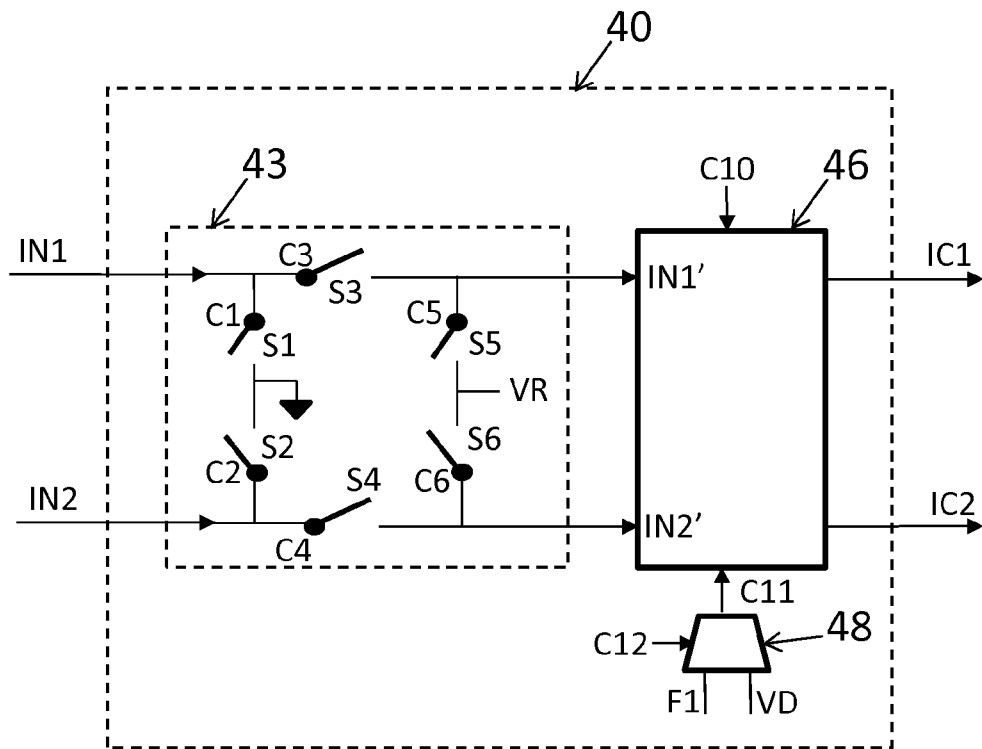


Figure 4

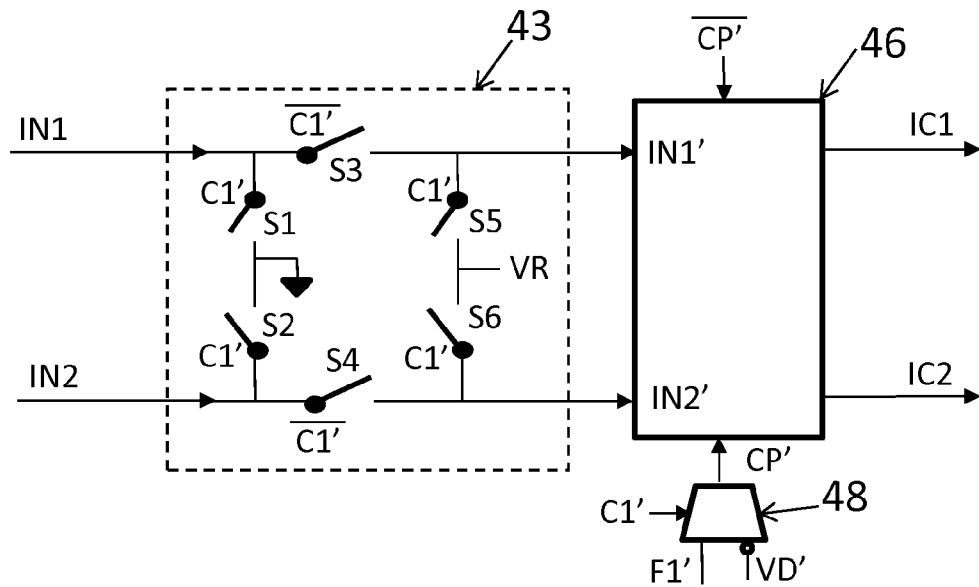


Figure 5A

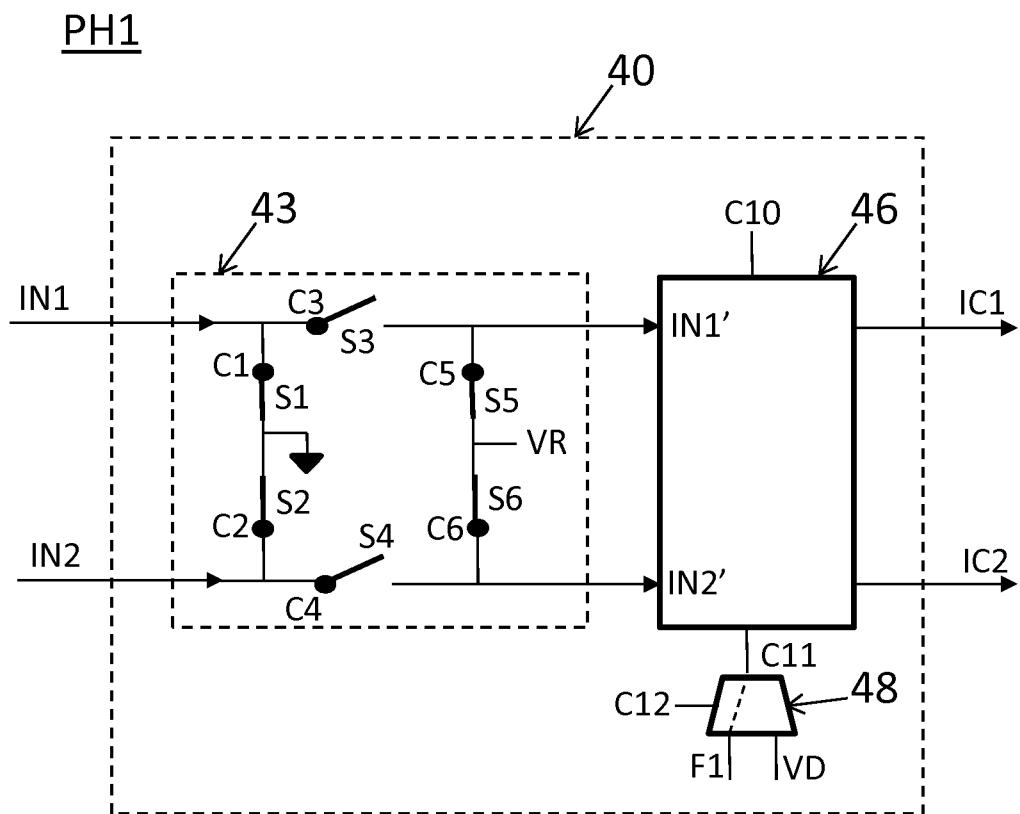


Figure 5B

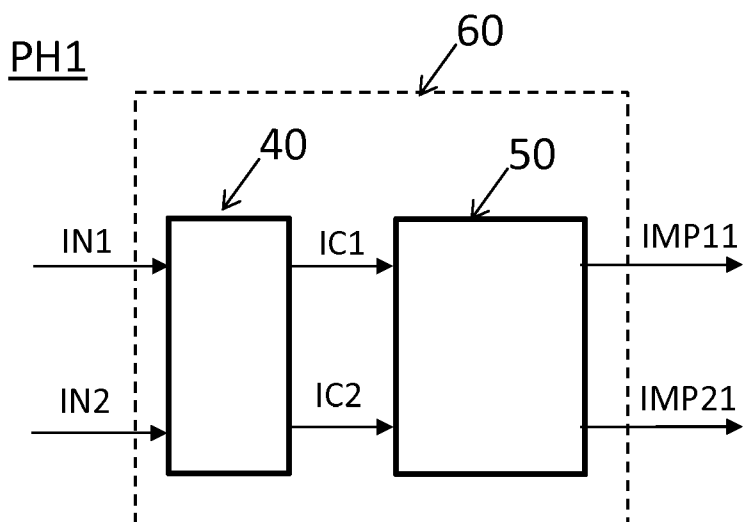


Figure 6A

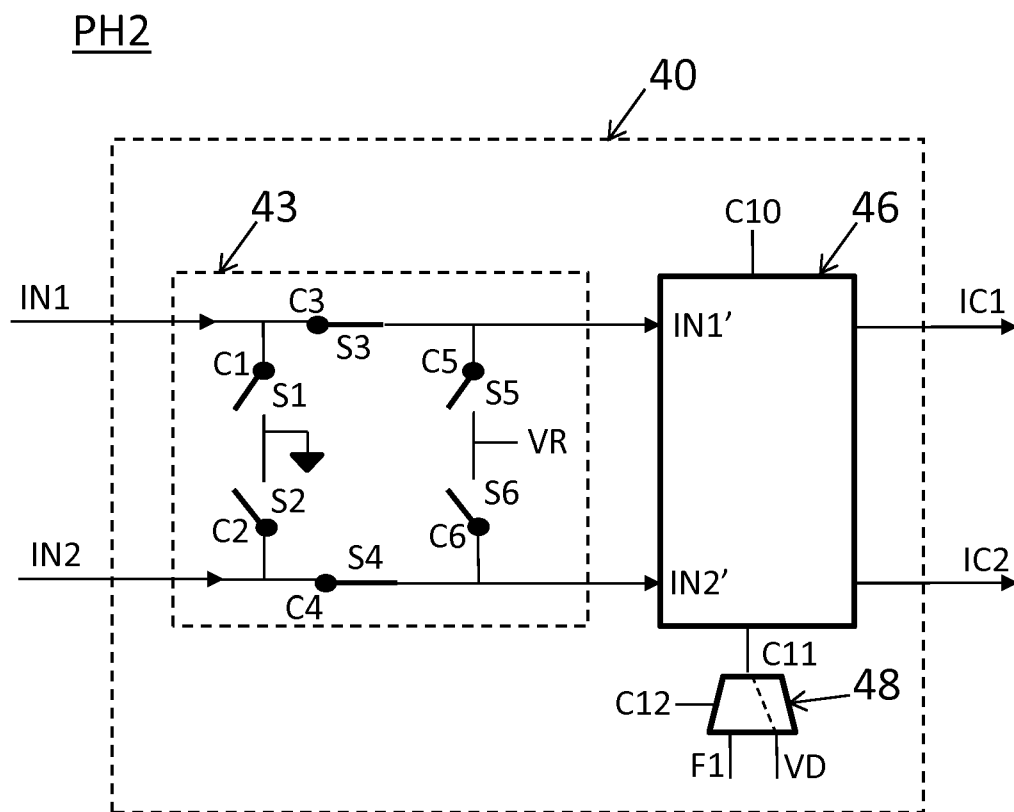


Figure 6B

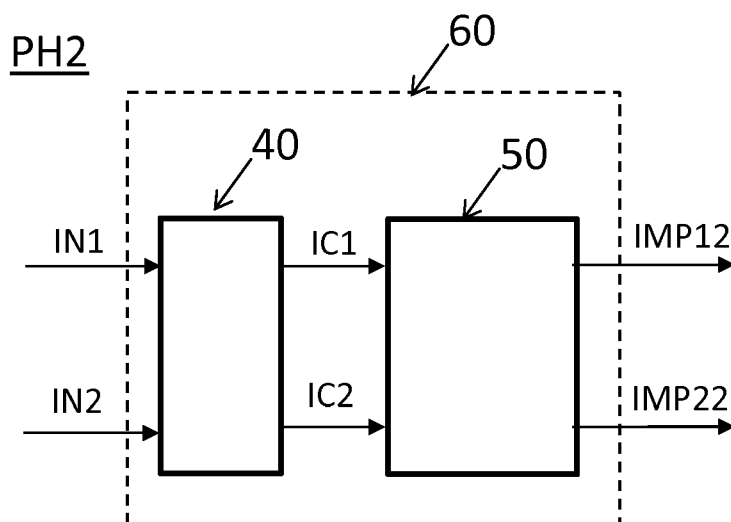


Figure 7A

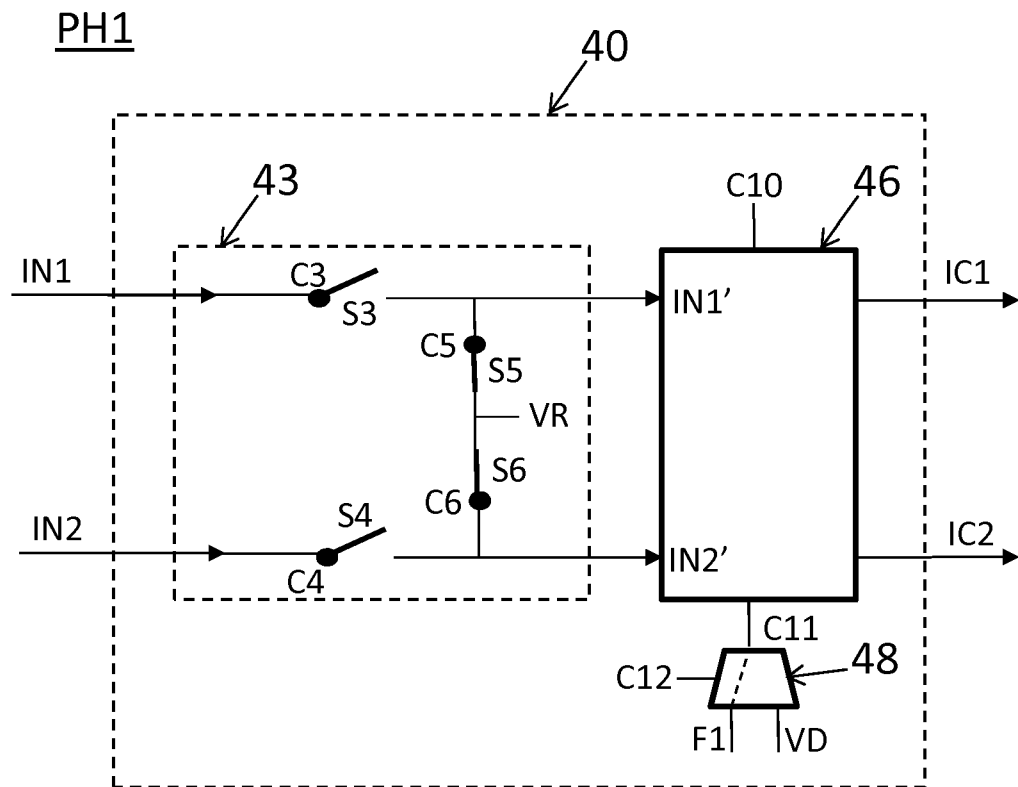


Figure 7B

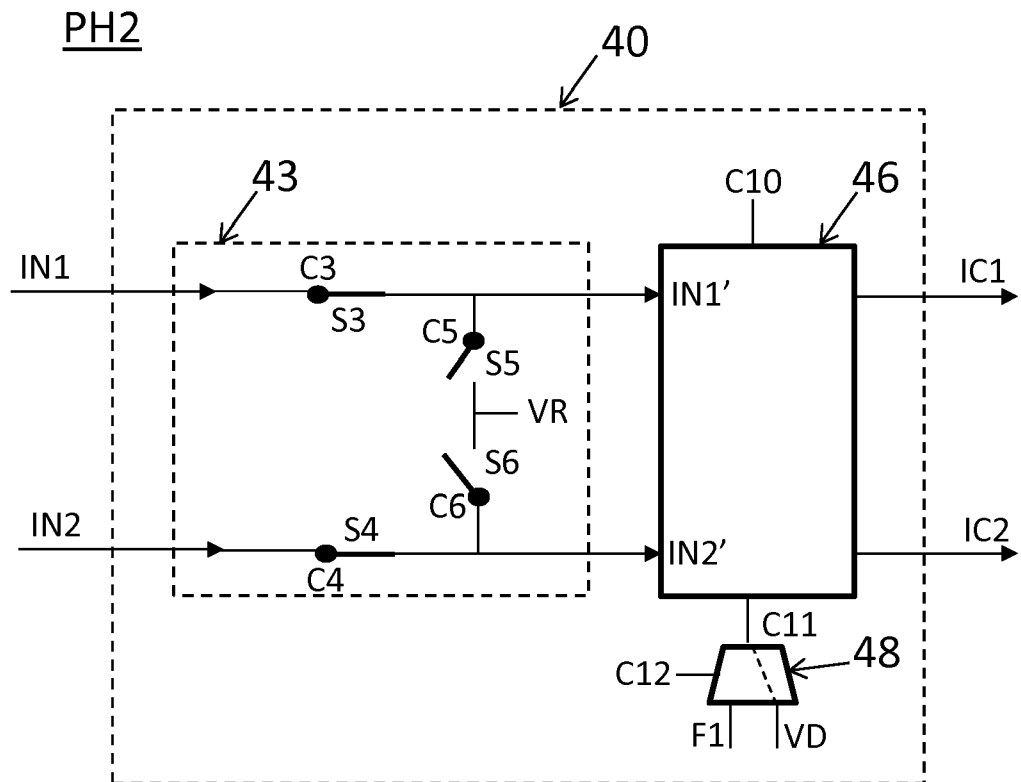


Figure 8

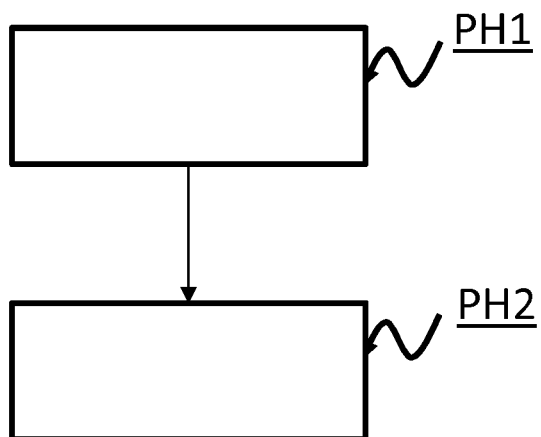
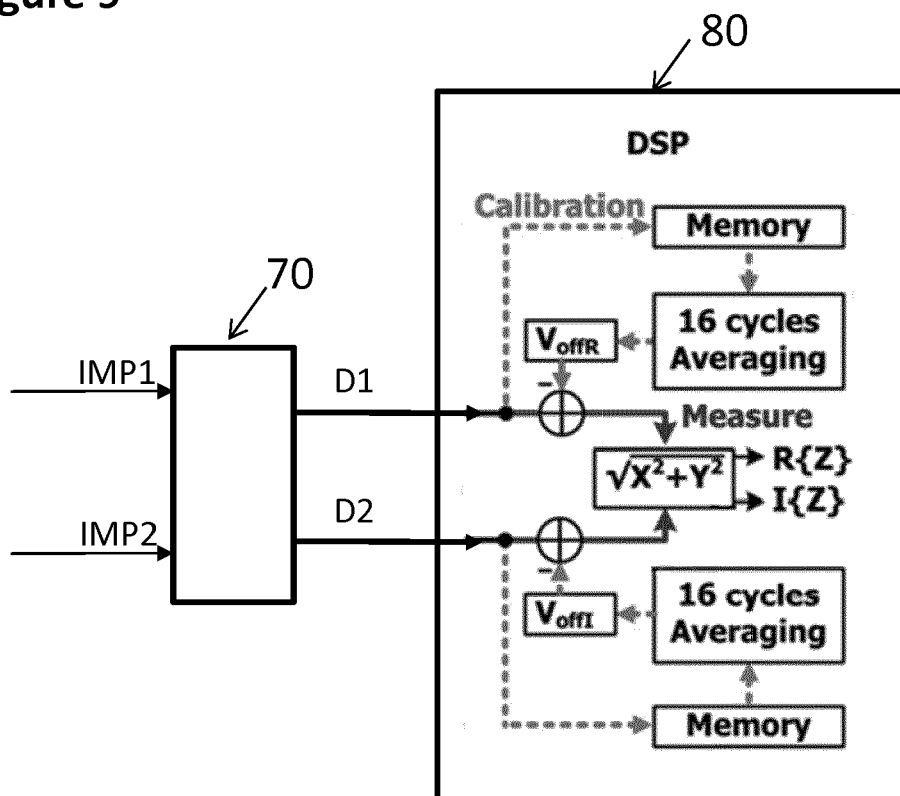


Figure 9





EUROPEAN SEARCH REPORT

 Application Number
 EP 14 15 5380

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 5 467 090 A (BAUMGARTNER RICHARD A [US] ET AL) 14 November 1995 (1995-11-14) * column 1, line 28 - line 32 * * column 2, line 60 - line 63 * * column 14, line 5 - line 14 * * column 20, line 19 - line 61 * * figures 1,3,15 *	1-11	INV. A61B5/04 A61B5/00 G01R35/00 G01R27/14
X,P	YAN LONG ET AL: "A 13 μ A Analog Signal Processing IC for Accurate Recognition of Multiple Intra-Cardiac Signals", IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, IEEE, US, vol. 7, no. 6, 20 January 2014 (2014-01-20), pages 785-795, XP011538076, ISSN: 1932-4545, DOI: 10.1109/TBCAS.2013.2297353 [retrieved on 2014-01-24] * page 790, right-hand column, paragraph 2 - page 791, left-hand column, paragraph 2 * * figure 9 *	1-11	TECHNICAL FIELDS SEARCHED (IPC) A61B G01R
A,D	EP 2 298 164 A2 (IMEC [BE]; STICHTING IMEC NEDERLAND [NL]) 23 March 2011 (2011-03-23) * paragraph [0001] * * paragraph [0036] * * paragraph [0040] * * paragraph [0101] - paragraph [0103] * * figures 3,27 *	1,11	
The present search report has been drawn up for all claims			
Place of search Berlin		Date of completion of the search 16 May 2014	Examiner Völlinger, Martin
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

EPO FORM 1503 03/82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 14 15 5380

5

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

16-05-2014

10

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5467090 A	14-11-1995	EP 0568199 A2	03-11-1993
		JP H06217942 A	09-08-1994
		US 5467090 A	14-11-1995
EP 2298164 A2	23-03-2011	EP 2298164 A2	23-03-2011
		US 2011092834 A1	21-04-2011

15

20

25

30

35

40

45

50

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

55

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- EP 2298164 A [0003] [0020] [0025]

Non-patent literature cited in the description

- **CHRISTIAN ENZ.** A CMOS chopper amplifier. *IEEE Journal of Solid-State Circuits*, June 1987, vol. SC-22 (3 [0025])

专利名称(译)	用于阻抗测量的电路，系统和方法		
公开(公告)号	EP2767230A1	公开(公告)日	2014-08-20
申请号	EP2014155380	申请日	2014-02-17
[标]申请(专利权)人(译)	校际微电子中心		
申请(专利权)人(译)	IMEC		
当前申请(专利权)人(译)	IMEC		
[标]发明人	YAZICIOGLU REFET FIRAT KIM SUNYOUNG		
发明人	YAZICIOGLU, REFET FIRAT KIM, SUNYOUNG		
IPC分类号	A61B5/04 A61B5/00 G01R35/00 G01R27/14		
CPC分类号	A61B5/04004 A61B5/0533 A61B5/0535 A61B5/7225 G01R27/16		
优先权	2013155550 2013-02-15 EP		
其他公开文献	EP2767230B1		
外部链接	Espacenet		

摘要(译)

本发明涉及一种用于阻抗测量的电路 (40)，包括连接到斩波器 (46) 的开关矩阵 (43)。开关矩阵 (43) 包括多个开关 (S1 至 S6)，并被配置为接收模拟信号 (IN1, IN2)。在操作中，在校准时段 (PH1) 期间，电路 (40) 被配置为激活斩波器 (46) 并控制开关矩阵 (43) 以便将所接收的模拟信号 (IN1, IN2) 与斩波器断开。输入 (IN1' ； IN2') 和将电压参考信号 (VR) 连接到斩波器输入 (IN1' ； IN2')。在操作中，在测量周期 (PH2) 期间，电路 (40) 被配置为停用斩波器 (46) 并控制开关矩阵 (43) 以便将电压参考信号 (VR) 与斩波器输入断开 (IN1' ； IN2') 并将接收到的模拟信号 (IN1, IN2) 连接到斩波器输入 (IN1' ； IN2')。本发明还涉及用于阻抗测量的系统和方法。

Figure 3

