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(54) **ENERGY EFFICIENT GREY SCALE DRIVER FOR ELECTROLUMINESCENT DISPLAYS**
ENERGIE-EFFIZIENTER GRAUSTUFEN-TREIBER FÜR ELEKTROLUMINISZENTE ANZEIGEN
PILOTE D'ECHELLE DE GRIS A BON RENDEMENT ENERGIQUE DESTINE A DES ECRANS ELECTROLUMINESCENTS

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Description**FIELD OF THE INVENTION**

5 **[0001]** The present invention relates generally to flat panel displays, and more particularly to a resonant switching panel driving circuit where the panel imposes a variable high capacitive load on the driving circuit and where the driving voltage must be regulated to facilitate gray scale control.

BRIEF DESCRIPTION OF THE DRAWINGS

10 **[0002]** The Background of the Invention and Detailed Description of the Preferred Embodiment are set forth herein below with reference to the following drawings, in which:

15 Fig. 1 is a plan view of an arrangement of rows and columns of pixels on an electroluminescent display, in accordance with the Prior Art;

Fig. 2 is a cross section through a single pixel of the electroluminescent display of Figure 1;

Fig. 3 is an equivalent circuit for the pixel of Figure 2;

Fig. 4 is a simplified circuit schematic of a resonant circuit used in the display driver according to Applicant's earlier filed U.S. Patent Application No. 09/504,472;

20 Figs. 5A - 5C are oscilloscope tracings that show waveforms for the resonant circuit of Figure 4 under different conditions;

Fig. 6 is a simplified schematic of a transformer secondary side portion of a display driver incorporating the elements of the present invention;

Fig. 7 is a block diagram of a driver circuit incorporating the elements of the present invention;

25 Fig. 8 is a detailed circuit diagram of a column driver according to the preferred embodiment of the present invention;

Fig. 9 is a detailed circuit diagram of a row driver according to the preferred embodiment of the present invention;

Fig. 10 is a detailed circuit diagram of a polarity reversing circuit employed at the output of the row driver of Figure 9; and

30 Fig. 11 and Fig. 12 are timing diagrams showing display timing pulses used in the display driver of the present invention.

BACKGROUND OF THE INVENTION

35 **[0003]** Electroluminescent displays are advantageous by virtue of their low operating voltage with respect to cathode ray tubes, their superior image quality, wide viewing angle and fast response time over liquid crystal displays, and their superior gray scale capability and thinner profile than plasma display panels. They do have relatively high power consumption, however, due to the inefficiencies of pixel charging, as discussed in greater detail below. This is the case even though the conversion of electrical energy to light within the pixels is relatively efficient. However, the disadvantage of high power consumption associated with electroluminescent displays can be mitigated if the capacitive energy stored

40 in the electroluminescent pixels is efficiently recovered.

[0004] The present invention relates to energy efficient methods and circuits for driving display panels where the panel imposes a variable capacitive load on the driving circuit and where the driving voltage must be regulated to facilitate gray scale control. The invention is particularly useful for electroluminescent displays where the panel capacitance is high. The panel capacitance is the capacitance as seen on the row and column pins of the display. Electroluminescent display pixels have the characteristic that the pixel luminance is zero if the voltage across the pixel is below a defined threshold voltage, and becomes progressively greater as the voltage is increased beyond the threshold voltage. This property facilitates the use of matrix addressing to generate a video image on the display panel.

45 **[0005]** As shown in Figures 1 and 2, an electroluminescent display has two intersecting sets of parallel electrically conductive address lines called rows (ROW 1, ROW 2, etc.) and columns (COL 1, COL 2, etc.) that are disposed on either side of a phosphor film encapsulated between two dielectric films. A pixel is defined as the intersection point between a row and a column. Thus, Figure 2 is a cross-sectional view through the pixel at the intersection of ROW 4 and COL 4, in Figure 1. Each pixel is illuminated by the application of a voltage across the intersection of row and column. Matrix addressing entails applying a voltage below the threshold voltage to a row while simultaneously applying voltages of the opposite polarity to each column that intersects that row. The opposite polarity voltage augments the row voltage in accordance with the illumination desired on the respective pixels, resulting in generation of one line of the image. An alternate scheme is to apply the maximum pixel voltage to a row and apply column voltages of the same polarity to all columns with a magnitude up to the difference between the maximum voltage and the threshold voltage, in order to decrease the pixel voltages in accordance with the desired image. In either case, once each row is addressed, another

row is addressed in a similar manner until all of the rows have been addressed. Rows not being addressed are left at open circuit. The sequential addressing of all rows constitutes a complete frame. Typically, a new frame is addressed at least about 50 times per second to generate what appears to the human eye as a flicker-free video image.

5 **[0006]** When each row of an electroluminescent display is illuminated, a portion of the energy supplied to the illuminated pixels is dissipated as current flows through the pixel phosphor layer to generate light, but a portion remains stored on the pixel once light emission has ceased. This residual energy remains on the pixel for the duration of the applied voltage pulse, and typically represents a significant fraction of the energy supplied to the pixel.

10 **[0007]** Figure 3 is an equivalent circuit which models the electrical properties of the pixel. The circuit comprises two back-to-back Zener diodes with a series capacitor labeled C_d and a parallel capacitor labeled C_{11} . Physically, the phosphor and dielectric films (Figure 2) are both insulators below the threshold voltage. This is represented in Figure 3 by the situation where one Zener diode is not conducting so that the pixel capacitance is the capacitance of the series combination of the two capacitors C_d and C_{11} . Above the threshold voltage, the phosphor film becomes conductive, corresponding to the situation where both Zener diodes are conducting such that the pixel capacitance is equal to that of the series capacitor only. Thus, the pixel capacitance is dependent on whether the voltage is above or below the threshold voltage. Further, because all of the pixels on the display are coupled to one another through the rows and columns, all of the pixels on the panel may be at least partially charged when a single row is illuminated. The extent of the partial charging of the pixels on non-illuminated rows is highly dependent on the variability of the simultaneous column voltages. In the case where all column voltages are the same, no partial charging of the pixels on non-illuminated rows occurs. In the case where about half of the columns have little or no applied voltage and the remaining half have close to the maximum voltage, the partial charging is most severe. The latter situation arises frequently in presentation of video images. The energy associated with this partial charging is typically much greater than the energy stored in the illuminated row, especially if there are a large number of rows, as in a high-resolution panel. All of the energy stored in non-illuminated rows is potentially recoverable, and may amount to more than 90% of the energy stored in the pixels, particularly for panels with a large number of rows.

25 **[0008]** Another factor contributing to energy consumption is the energy dissipated in the resistance of the driving circuit and the rows and columns during charging of the pixels. This dissipated energy may be comparable in magnitude to the energy stored in the pixels if the pixels are charged at a constant voltage. In this case, there is an initial high current surge as the pixels begin to charge. It is during this period of high current that most of the energy is dissipated since the dissipation power is proportional to the square of the current. Making the current that flows during pixel charging closer to a constant current can reduce the dissipated energy. This has been addressed, for example by C. King in SID International Symposium Lecture Notes 1992, May 18, 1992, Volume 1, Lecture no. 6, through the application of a stepped voltage pulse rather than a single square voltage pulse as is done conventionally in the electroluminescent display art. However, the circuitry required to provide stepped pulses adds to complexity and cost.

30 **[0009]** Sinusoidal driving waveforms have also been employed to reduce resistive energy loss. U.S. Patent 4,574,342 teaches the use of a sinusoidal supply voltage generated using a DC to AC inverter and a resonant tank circuit to drive an electroluminescent display panel. The panel is connected in parallel with the capacitance of the tank circuit. The supply voltage is synchronized with the tank circuit so as to maintain the voltage amplitude in the tank at a constant level independent of the load associated with the panel. The use of the sinusoidal driving voltage eliminates high peak currents associated with constant voltage driving pulses and therefore reduces I^2R losses associated with the peak current, but does not effect recovery of capacitive energy stored in the panel.

35 **[0010]** US Patent 4,707,692 teaches the use of an inductor in parallel with the capacitance of the panel to effect partial energy recovery. This scheme requires a large inductor to achieve a resonance frequency commensurate with the timing constraints inherent in display operation, and does not allow for efficient energy recovery over a wide range of panel capacitance, which, as discussed above is commonly encountered with electroluminescent displays. U.S. Patent 5,559,402 teaches a similar inductor switching scheme by which two small inductors and a capacitor which are external to the panel sequentially release small energy portions to the panel or accept small energy portions from the panel. However, only a portion of the stored energy can be recovered. U.S. Patent 4,349,816 teaches energy recovery by means of incorporating the display panel into a capacitive voltage divider circuit that employs large external capacitors to store recovered energy from the panel. This scheme increases the capacitive load on the driver which, in turn, increases the load current and increases resistive losses. None of these three patents teaches reduction of resistive losses by using sinusoidal drivers.

40 **[0011]** U.S. Patents 4,633,141; 5,027,040; 5,293,098; 5,440,208 and 5,566,064 teach the use of resonant sinusoidal driving voltages to operate an electroluminescent lamp element and recover a portion of the capacitive energy in the lamp element. However, these schemes do not facilitate efficient energy recovery when there is a large random short-term variation in the panel capacitance. In fact, accommodation of such capacitance changes is not a requirement for the operation of electroluminescent lamps where the panel capacitance is fixed, other than to compensate for slow changes due to the aging characteristics of the panel.

55 **[0012]** U.S. Patent 5,315,311 teaches a method of saving power in an electroluminescent display. This method involves

sensing when the power demand from the column drivers is highest in a situation where the pixel voltage is the sum of the row and column voltages, and then reducing the column voltage, and correspondingly increasing the selected row voltage. The method does not facilitate reduction of resistive losses by limiting peak currents, nor does it recover capacitive energy from the panel. Research suggests that the method of this patent degrades the contrast ratio for the display, since any pixels in the selected row that are meant to be off will be somewhat illuminated due to the row voltage being somewhat above the threshold voltage. Thus, this prior art power saving method does not work well in conjunction with gray scale capability.

[0013] According to co-pending U.S. Patent Application No. 09/504,472 (the published PCT equivalent of this application being WO 01/61677) an electroluminescent display driving method and circuit are provided that simultaneously recover and re-use the stored capacitive energy in a display panel and minimize resistive losses attributable to high instantaneous currents. These features improve the energy efficiency of the panel and driver circuit, thereby reducing their combined power consumption. Also, by reducing the rate of heat dissipation in the display panel and driver circuit the panel pixels can be driven at higher voltage and higher refresh rates, thereby increasing brightness. An additional benefit of applicant's prior invention is reduced electromagnetic interference due to the use of a sinusoidal drive voltage rather than a pulse drive voltage. The use of a sinusoidal drive voltage eliminates the high frequency harmonics associated with discrete pulses. The advantages given above are accomplished without the need for expensive high voltage DC/DC converters.

[0014] The energy efficiency of the display panel and driving circuit of U.S. Patent Application No. 09/504,472 is improved through the use of two resonant circuits to generate two sinusoidal voltages, one to power the display rows and one to power the display columns. The row capacitance, as seen on the row pins of the display, forms one element of the resonant circuit for the row driving circuit. The column capacitance, as seen on the column pins of the display, forms one element of the resonant circuit for the column driving circuit.

[0015] The energy in each resonant circuit is periodically transferred back and forth between capacitive elements and inductive elements. The resonant frequency of each of the resonant circuits is tuned so that the period of the oscillations is matched as closely as possible, i.e. synchronized, to the charging of successive panel rows at the scanning frequency of the display.

[0016] When the energy is stored inductively, a switch that connects the row resonant circuit to a particular row is activated so as to direct the energy stored inductively to the appropriate row as the rows are addressed in sequence. The row driving circuit for the rows also includes a polarity reversing circuit that reverses the row voltage on alternate frames in order to extend the service life of the display.

[0017] In a similar manner, the column driving circuit connects the column resonant circuit to all of the columns simultaneously so as to direct energy stored inductively to the columns. The column switches, as is taught in the conventional art, also serve to control the quantity of energy fed to each column in order to effect gray scale control. Typically, the row switches and column switches are packaged as an integrated circuit in sets of 32 or 64 and are respectively called row drivers and column drivers.

[0018] Figure 4 is a simplified schematic of a resonant circuit according to U.S. Patent Application No. 09/504,472. The basic element is a resonant voltage inverter forming a resonant tank that comprises a step down transformer (T), a capacitance corresponding to the panel capacitance (C_p) connected across the secondary winding of the transformer and a further capacitance (C_1) connected across the primary winding of the transformer. The further capacitance may optionally include a further bank of capacitors (C_r) that can be selected to synchronize the resonant frequency with different display scanning frequencies.

[0019] The resonant circuit also comprises two switches (S_1 and S_2) that alternately open and close when the current is zero in order to invert an incoming sinusoidal signal to a unipolar resonant oscillation. An input DC voltage is chopped by switch (S_3) under control of a pulse width modulator (PWM) to control the voltage amplitude of the resonant oscillation. To stabilize the voltage of the oscillations, a signal (FB) is fed back from the primary of the transformer to the PWM to adjust the on-to-off time ratio for the switch (S_3) in response to fluctuations in the voltage on the secondary. This feedback compensates for voltage changes due to variations in the panel impedance resulting, in turn, from changes in the displayed image. The panel impedance is the impedance as seen on the row and column pins of the display.

[0020] To operate efficiently, the resonant frequency of the driving circuit must not vary appreciably so that the resonant frequency remains closely matched to the frequency of row addressing timing pulses. The resonant frequency f is given by equation 1

$$f = 1/(2\pi(LC)^{1/2}) \quad (1)$$

where L is the inductance and C is the capacitance of the tank in the resonant circuit. The resonant circuit must account for the variability in the panel capacitance that contributes to the total tank capacitance. This is accomplished by use of

the step down transformer which reduces the contribution of the panel capacitance (C_p) to the tank capacitance so that the effective tank capacitance C is given by equation 2 where, C_p is the panel capacitance, C_1 is the value of the capacitance across the primary winding of the transformer and n_1 and n_2 are the number of turns respectively on the primary and secondary windings of the transformer.

$$C = (n_2/n_1)^2 C_p + C_1 \quad (2)$$

[0021] Values for the ratio of the number of turns (n_2/n_1) and C_1 are chosen so that the first term in equation 2 is small compared with the second term. Equation 2 is used as a guide in determining appropriate values for the turns-ratio and the primary capacitance for a particular panel, and mutual optimization of these values is then accomplished by examining the voltage waveforms measured at the output of the resonant circuit. Component values are then selected to minimize the deviation from a sinusoidal signal. If the resonant frequency is too high, a waveform exemplified by that shown in Figure 5A will be observed where there is a zero voltage interval between the alternate polarity segments of the waveform. Appropriate adjustments are then made using equations 1 and 2 as a guide. If the resonant frequency is too low, a waveform exemplified by that shown in Figure 5B will be observed, where there is a vertical voltage step crossing zero volts connecting alternate polarity segments of the waveform. If the resonant frequency is well matched to the row addressing frequency, a nearly perfect sinusoidal waveform will be observed, as shown in Figure 5C. However, in practice, fluctuations in the load will result in small frequency variations. Therefore, the DC input switching is usually set so that fluctuations in resonant frequency result in the resonant frequency being equal to or higher than the switching frequency so that deviations from the ideal resonant frequency result in the waveforms shown in Figure 5A. This is to avoid large current transients associated with the abrupt voltage changes at the switching point as shown in Figure 5B. Large transient currents decrease the energy efficiency of the circuit by increasing ohmic loss.

[0022] The known prior art is absent any teaching of voltage regulation of a flat panel display which accommodates variations in load during scanning which occur at a rate faster than the time constant for the feedback circuit to correct, thereby resulting in image artifacts.

[0023] U.S. Patent 5,576,601 (Koenck et al) acknowledges that it is known in the art to apply power to an electroluminescent panel through the secondary output of an autotransformer coupled in series with the electroluminescent panel. The inductance of the autotransformer is configured with respect to the capacitance of the electroluminescent panel to provide a resonant frequency at the desired operating frequency of the electroluminescent panel. However, there is no teaching of any mechanism for accommodating quickly changing load variations during gray scale scanning. A capacitor is provided to prevent the panel from voltage spikes, which is problematic for thin film electroluminescent panels. The present invention relates to thick film panels that are characterized by much higher dielectric breakdown voltages.

[0024] U.S. Patent 3,749,977 (Sliker) relates to drive circuitry for electroluminescent lamps. A transformer with split secondary is disclosed. However, there is no suggestion of providing voltage regulation with a varying load.

[0025] JP 11067447 (Okada) also relates to drive circuitry for electroluminescent lamps, which do not experience fluctuations in load or are in any way concerned with gray scale variation of displays.

[0026] U.S. Patent 4,866,349 (Weber et al) relates to plasma panels and other panels where the drive circuitry is required to provide sustained arc current to provide luminance.

[0027] U.S. Patent 5,517,089 (Ravid) teaches an electroluminescent panel with a transformer. However, there is no suggestion of resonant circuits or gray scale control.

SUMMARY OF THE INVENTION

[0028] According to the present invention, a method and apparatus are provided to regulate the maximum value of the sinusoidal voltage waveform provided to the rows and columns of a flat panel display even though the capacitance of the panel as seen through the rows and columns may vary substantially. Regulation is effected by clamping the voltage to a substantially fixed value when the voltage to the rows or columns exceeds a predetermined value. The predetermined value is chosen to be the peak sinusoidal voltage in the absence of dipping when the panel capacitance as seen through the rows or columns is effectively near its maximum value. This voltage clamping feature facilitates gray scale control by providing a regulated voltage independent of the panel capacitance for any desired input voltage level up to that for maximum display luminance.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0029] According to the present invention in its broadest-aspect, a secondary winding on the step-down transformer

T of Figure 4 is connected to a full wave rectifier with a large storage capacitor connected to its output as shown in Figure 6. The storage capacitor C_S and the panel capacitor C_P are connected in series as shown in Figure 6. The turns ratio of the secondary winding connected to the full wave rectifier and storage capacitor C_S to that of the second secondary winding connected to the panel is at least 1.05:1, preferably at least 1.1:1 and more preferably in the range 1.1:1 to 1.2:1. The turns ratio for the secondary windings of the present invention is substantially larger than the turns ratio of the three turn secondary winding connected to the panel in the energy recovery circuit of Figure 4 (i.e. that of U.S. patent application 09/504,472). The 3-turn winding in that circuit was designed to provide a small DC offset to the voltage input to the row and column drivers to ensure their proper operation. The capacitance of the storage capacitor C_S is very large relative to the panel capacitance C_P . Since the full wave rectifier ensures that the voltage across the storage capacitor always has the same polarity, a large capacitance can be achieved in a small volume through use of an electrolytic capacitor. Other high energy density capacitors such as tantalum or ruthenium oxide super-capacitors may also be used.

[0030] In operation the voltage applied to the panel is clamped at a value that can be arbitrarily set by adjusting feedback to the pulse width modulator (PWM). For a heavy panel load where the panel capacitance C_P is near its maximum value, approximately 90% of the energy is arranged to flow to the secondary winding connected to the panel for charging the panel, and the remaining 10% charges the storage capacitor C_P . For an average load where the panel capacitance has an average value, approximately 50% of the energy is directed to charge the panel and 50% is directed to the storage capacitor C_S . For a light load with the panel capacitance C_P near a minimum approximately 10% of the energy is directed to the panel and 90% to the storage capacitor. Typically these conditions can be met if the voltage at the panel is always positive with a minimum value of about 0.5 volts to ensure proper operation of switching ICs connecting to the rows and columns of the display. Also, the ratio of the capacitance of the storage capacitor to the maximum panel capacitance should be at least about 10:1 and preferably at least about 20:1, and most preferably at least 30:1.

[0031] The internal series resistance of the storage capacitor C_S is chosen to be sufficiently low that voltage fluctuations across the capacitor due to resistive losses and the RC time constant do not exceed the specified regulation tolerance. Also, the turns ratio for the two secondary windings should take into account the forward voltage drop across the diodes in the rectifier that drive the storage capacitor and any resistive loss in the secondary circuits. The forward diode voltage drop can be minimized by selecting Schottky diodes for the rectifier.

[0032] During operation of the circuit according to Figure 6, when a voltage pulse below the clamp voltage is applied to a row or column, energy from the primary winding is transferred mainly through the secondary winding connected across the panel. At the same time, energy from the storage capacitor C_S flows to the panel. When the voltage exceeds the clamp voltage, energy is mainly transferred to both the storage and panel capacitors from the primary winding through the secondary winding connected to the rectifier in such a way that the storage and panel capacitors are charged in parallel. Since the parallel capacitance is dominated by the large capacitance of the storage capacitor C_S , there is only minimal increase in the voltage across the capacitors, and effective voltage regulation is achieved.

[0033] Longer term drift of the voltage across the storage capacitor C_S over many pulses due to random changes in the displayed image can be eliminated by sensing the average voltage over many addressing cycles and providing feedback to the primary circuit, as set forth in U.S. Patent Application 09/504,742. Thus, both short-term voltage fluctuations on the time scale of a single pulse and longer-term voltage fluctuations can be minimized to the extent required to maintain gray scale fidelity.

[0034] A block diagram of a complete display driver is shown in Figure 7. In the diagram HSync refers to timing pulses that initiate addressing of a single row. The HSync pulses are fed to a time delay control circuit 60 where the delay time is set so that the zero current times in the resonant circuit will correspond to the switching times for the rows and columns. The output of circuit 60 is applied to row and column resonant circuits 62 and 64, and the output of circuit 62 is applied to polarity switching circuit 66. The switching times for the polarity switching circuit 66 are controlled by the VSync pulses to control the timing for initiating each complete frame. The outputs of circuits 64 and 66 are clamped as described in greater detail below, and applied to the column and row driver ICs 68 and 70, respectively.

[0035] Returning momentarily to Figure 2, the preferred embodiment for the present invention is optimized for use with an electroluminescent display having a thick film dielectric layer. Thick film electroluminescent displays differ from conventional thin film electroluminescent displays in that one of the two dielectric layers comprises a thick film layer having a high dielectric constant. The second dielectric layer is not required to withstand a dielectric breakdown since the thick layer provides this function, and can be made substantially thinner than the dielectric layers employed in thin film electroluminescent displays. U.S. Patent 5,432,015 teaches methods to construct thick film dielectric layers for these displays. As a result of the nature of the dielectric layers in thick film electroluminescent displays, the values in the equivalent circuit shown in Figure 3 are substantially different than those for thin film electroluminescent displays. In particular, the values for C_d can be significantly larger than they are for thin film electroluminescent displays. This makes the variation in panel capacitance as a function of the applied row and column voltages greater than it is for thin film displays, and provides a greater impetus for the use of the present invention in thick film displays. The ratio of the pixel capacitance above the threshold voltage to that below the threshold voltage is typically about 4:1 but can exceed 10:1. By contrast, for thin film electroluminescent displays this ratio is in the range of about 2:1 to 3:1. Typically the panel

capacitance can range from the nanofarad range to the microfarad range, depending on the size of the display and the voltages applied to the rows and columns.

[0036] A row driver circuit and a column driver circuit have been built according to a successful reduction to practice of the present invention, for an 8.5 inch 240 by 320 pixel quarter VGA format diagonal thick film colour electroluminescent display. Each pixel has independent red, green and blue sub-pixels addressed through separate columns and a common row. The threshold voltage for the prototype display was 150 volts. The panel capacitance for this display measured at an applied voltage of less than 10 volts between a row and the columns with all of the columns at a common potential was 7 nanofarads. The panel capacitance measured at a similar voltage between a row and a column but with half of the remaining columns at a common potential with the selected column and the remaining columns at a voltage of 60 volts with respect to the selected column was 0.4 microfarads, a much larger value.

[0037] Figures 8 and 9 are circuit schematics for the resonant circuits according to a preferred embodiment of the present invention used for columns and rows, respectively. Figure 10 is a circuit schematic of a polarity reversing circuit connected between the row resonant circuit and the row drivers to provide alternating polarity voltage to the row driver high voltage input pins. The input DC voltage to the resonant circuits was 330 volts (rectified off-line from 120/240 volts AC). The output of the polarity reversing circuit is connected to the high voltage input pins of the row driver IC 70 (Figure 7), the output pins of which are connected to the rows of the display. The clock and gate input pins of the row drivers are synchronized using digital circuitry employing field programmable gate arrays (FPGA's) adapted for matrix addressing of electroluminescent displays, as known in the art.

[0038] Figure 11 and Figure 12 shows the timing signal waveforms that are used to control the inventive driver circuit, as shown in Figures 7, 8, 9 and 10. The row addressing frequency for the prototype display was 32 kHz, allowing a refresh rate of 120 Hz for the display.

[0039] With reference to Figure 8, the resonant frequency of the column driving resonant circuit is controlled by the effective inductance seen at the primary of the step-down transformer T2 and by the effective capacitance of the capacitor C42 in parallel with the column capacitance as seen at the primary of T2. There is also a small trimming capacitor C11 in parallel with C42 for fine tuning of the resonant frequency. The turns ratio for the transformer is greater than 5 and the value C_1 of the capacitor C42, with reference to equation 2, is chosen so that C_1 is substantially greater than $(n_2/n_1)^2 C_P$ to minimize the effect of changes in the panel capacitance on the resonant frequency. C9 is a bank of capacitors for tuning the tank circuit, in conjunction with the capacitance of C42, to obtain the desired resonant frequency to match or synchronize with different display scanning frequencies.

[0040] With further reference to Figure 8, the sinusoidal output at the secondary of the transformer T2 is DC shifted by the voltage across the storage capacitor C_s of the clamp circuit so that the instantaneous output voltage is never negative.

[0041] The resonant circuit is driven using the two MOSFETs Q2 and Q3, the switching of which is controlled by the LC DRV signal that is synchronized using an appropriate delay time with the HSync signal thereby causing the row driver ICs to select the addressed row. The delay is adjusted to ensure that switching of the row driver ICs occurs when the drive current is close to zero. The LC DRV signal is generated by the low voltage logic section of the display driver that is typically a field programmable gate array (FPGA) but may be an application specific integrated circuit (ASIC) designed for this purpose. The LC DRV signal is a 50% duty cycle TTL level square wave. The LC DRV signal has two forms: the LC DRV A signal is the complementary of the LC DRV B signal.

[0042] Again with respect to Figure 8, control of the voltage level in the resonant circuit is achieved using the pulse width modulator U1 whose output is routed through the transformer T6 to the gate of the MOSFET Q1. This controls the voltage level in the resonant circuit by chopping the 330 volt input DC voltage. The inductor L2 limits the current to the resonant circuit as it is being energized from the DC voltage and the diode D12 limits voltage excursions at the source of the MOSFET Q1 due to current changes in the inductor. The duty cycle for the pulse width modulator is controlled by a voltage feedback circuit for sensing the voltage at the primary of the transformer T2 to regulate or adjust the resonant circuit voltage. The switching of the pulse width modulator is synchronized with HSync using the TTL signal PWM_SYNC from the low voltage logic section of the display driver.

[0043] With reference to Figure 9, the operation of the row driver circuit for the preferred embodiment is similar to that of the column driver circuit, except that the turns ratio on the transformer T1 as compared to that of the transformer T2 in the column driver circuit is different to reflect the higher row voltages and smaller values of the panel capacitance as seen through the rows, due to the fact that the remaining rows are at open circuit. There are also four more secondary windings on the transformer T1 than there are on T2 to generate floating voltages required for operation of the polarity reversing circuit that alternates the polarity of the rows on successive frames.

[0044] In the preferred embodiment, the output of the row driver circuit feeds into the polarity reversing circuit shown in Figure 10. This provides row voltages having opposite polarity on alternate frames to provide the required ac operation of the electroluminescent display. Six MOSFETs Q4 through Q9 form a set of analogue switches connecting either the positive or the negative sinusoidal drive waveforms generated to the panel rows. The selection of polarity is controlled by FRAME POL, a TTL signal generated by the system logic circuit in the display system. The FRAME POL signal is

synchronized to the vertical synchronization signal VSYNC that initiates scanning of each frame on the display. The FRAME POL signal, together with four floating voltages from T1, generates the control signals (FRAME_POL-1 to FRAME_POL-4) that operate the polarity reversing circuit.

[0045] Although alternate embodiments of the invention have been described herein, it will be understood by those skilled in the art that variations may be made thereto without departing from the scope of the appended claims.

Claims

1. A driving circuit operable to provide regulated power with gray scale image control of an electroluminescent display having pixels arranged in rows and columns using energy recovered from a varying panel capacitance (C_p) of said display, comprising:

a source of electrical energy (VDC); and

a resonant circuit (62, 64) operable to use said panel capacitance (C_p), for receiving said electrical energy and, in response, to generate a sinusoidal voltage to power said display at a resonance frequency which is substantially synchronised to a scanning frequency of said display;

characterised in that the driving circuit further comprises a circuit (U1, U12) operable to clamp said sinusoidal voltage to a substantially fixed value when the voltage to either the rows or columns of said display exceeds a predetermined value, thereby regulating the maximum value of said sinusoidal voltage in the event of variations in said panel capacitance (C_p).

2. The driving circuit of claim 1, wherein said resonant circuit (62, 64) further comprises a step down transformer (T2, T1) operable to reduce the effective panel capacitance (C_p) of said display.

3. The driving circuit of claim 2, wherein said step down transformer (T1, T2) has a primary winding across which a further capacitance (C1; C41, C42) is connected; a first secondary winding across which said panel capacitance (C_p) is connected, wherein the value of said further capacitance (C1; C41, C42) is sufficiently large relative to said panel capacitance (C_p) to maintain substantial synchronisation of said resonance frequency to said scanning frequency; and a further secondary winding connected to a full wave rectifier with a storage capacitor (C_s) connected thereacross and in series with said panel capacitance (C_p) wherein the value of said storage capacitor (C_s) is sufficiently large relative to said panel capacitance (C_p) that (i) for a heavy panel load where the panel capacitance (C_p) is at or near its maximum value most of said electrical energy flows to the first secondary winding for charging the panel and remaining energy charges the storage capacitor (C_s), (ii) for an average load where the panel capacitance has an average value approximately half of the energy flows to the panel and half of the energy flows to the storage capacitor (C_s), and (iii) for a light load where the panel capacitance is at or near a minimum value most of the energy flows to the storage capacitor and remaining energy flows to the panel.

4. The driving circuit of claim 3, wherein the ratio of the capacitance of the storage capacitor (C_s) to the maximum panel capacitance is at least about 10:1.

5. The driving circuit of claim 4, wherein the ratio of the capacitance of the storage capacitor (C_s) to the maximum panel capacitance is at least about 20:1.

6. The driving circuit of claim 5, wherein the ratio of the capacitance of the storage capacitor (C_s) to the maximum panel capacitance is at least about 30:1.

7. The driving circuit of claim 3, wherein said full wave rectifier incorporates Schottky diodes operable to minimise forward diode voltage drop.

8. The driving circuit of claim 3, wherein the turns ratio of the further secondary winding to that of the first secondary winding is at least 1.05:1.

9. The driving circuit of claim 3, wherein the turns ratio of the further secondary winding to that of the first secondary winding is at least 1.1:1.

10. The driving circuit of claim 9, wherein the turns ratio of the further secondary winding to that of the first secondary

winding is in the range 1.1:1 to 1.2:1.

- 5
11. The driving circuit of claim 3, wherein said primary winding has n_1 turns and said secondary winding has n_2 turns such that the value of the further capacitance is substantially larger than $(n_2/n_1)^2$ multiplied with the value of the panel capacitance.
12. The driving circuit of claim 3, further comprising an additional capacitor (C_f ; C9) operable to change said resonance frequency.
- 10
13. The driving circuit of claim 1, wherein the source further comprises voltage means (VDC; DC-IN) operable to generate direct current voltage; and a pulse width modulator (PWM; U1, U12) operable to chop said direct current voltage into pulses of electrical energy.
- 15
14. The driving circuit of claim 1, further comprising a controller operable to control the rate of electrical energy received by said resonant circuit to control fluctuations of said sinusoidal voltage due to a varying impedance of said display and energy usage by said display.
- 20
15. The driving circuit of claim 14, wherein said controller further comprises a feedback circuit operable to sense fluctuations of said sinusoidal voltage using an input from said resonant circuit and in response providing a feedback signal (FB; FB2) to said controller.
- 25
16. The driving circuit of claim 15, wherein said input is from a primary winding of a step down transformer of said resonant circuit.
- 30
17. The driving circuit of claim 16, wherein said sinusoidal voltage is clamped at a predetermined value by adjusting said feedback signal (FB; FB2) to said controller.
- 35
18. A passive matrix display comprising:
- a plurality of rows (ROW 1, ROW 2, ROW 3, ROW 4) adapted to be scanned at a predetermined scanning frequency of said display;
 - a plurality of columns (COL 1, COL 2, COL 3, COL 4) which intersect said rows to form a plurality of pixels **characterised by** a varying panel capacitance (C_p); and
 - a driving circuit as claimed in claim 1.
- 40
19. The passive matrix display of claim 18, wherein said resonant circuit (62, 64) further comprises a step down transformer (T2, T1) operable to reduce the effective panel capacitance (C_p) of said display.
- 45
20. The passive matrix display of claim 19, wherein said step down transformer (T1, T2) has a primary winding across which a further capacitance (C1; C41, C42) is connected; a first secondary winding across which said panel capacitance (C_p) is connected, wherein the value of said further capacitance (C1; C41, C42) is sufficiently large relative to said panel capacitance (C_p) to maintain substantial synchronisation of said resonance frequency to said scanning frequency; and a further secondary winding connected to a full wave rectifier with a storage capacitor (C_s) connected thereacross and in series with said panel capacitance (C_p) wherein the value of said storage capacitor (C_s) is sufficiently large relative to said panel capacitance (C_p) that (i) for a heavy panel load where the panel capacitance (C_p) is at or near its maximum value most of said electrical energy flows to the first secondary winding for charging the panel and remaining energy charges the storage capacitor (C_s), (ii) for an average load where the panel capacitance has an average value approximately half of the energy flows to the panel and half of the energy flows to the storage capacitor (C_s), and (iii) for a light load where the panel capacitance is at or near a minimum value most of the energy flows to the storage capacitor and remaining energy flows to the panel.
- 50
21. The passive matrix display of claim 20, wherein the ratio of the capacitance of the storage capacitor (C_s) to the maximum panel capacitance is at least about 10:1.
- 55
22. The passive matrix display of claim 21, wherein the ratio of the capacitance of the storage capacitor (C_s) to the maximum panel capacitance is at least about 20:1.
23. The passive matrix display of claim 22, wherein the ratio of the capacitance of the storage capacitor (C_s) to the

maximum panel capacitance is at least about 30:1.

24. The passive matrix display of claim 20, wherein said full wave rectifier incorporates Schottky diodes operable to minimise forward diode voltage drop.

25. The passive matrix display of claim 20, wherein the turns ratio of the further secondary winding to that of the first secondary winding is at least 1.05:1.

26. The passive matrix display of claim 20, wherein the turns ratio of the further secondary winding to that of the first secondary winding is at least 1.1:1.

27. The passive matrix display of claim 26, wherein the turns ratio of the further secondary winding to that of the first secondary winding is in the range 1.1:1 to 1.2.:1.

28. The passive matrix display of claim 20, wherein said primary winding has n_1 turns and said secondary winding has n_2 turns such that the value of the further capacitance is substantially greater than $(n_2/n_1)^2$ multiplied with the value of the panel capacitance.

29. The passive matrix display of claim 20, further comprising an additional capacitor (Cf; C9) operable to change said resonance frequency.

30. The passive matrix display of claim 18, wherein the source further comprises voltage means (VDC; DC-IN) operable to generate a direct current voltage; and a pulse width modulator (PWM; U1, U12) operable to chop said direct current voltage into pulses of electrical energy.

31. The passive matrix display of claim 18, further comprising a controller operable to control the rate of electrical energy received by said resonant circuit to control fluctuations of said sinusoidal voltage due to a varying impedance of said display and energy usage by said display.

32. The passive matrix display of claim 31, wherein said controller further comprises a feedback circuit operable to sense fluctuations of said sinusoidal voltage using an input from said resonant circuit and in response providing a feedback signal (FB; FB2) to said controller.

33. The passive matrix display of claim 32, wherein said input is from a primary winding of a step down transformer of said resonant circuit.

34. The passive matrix display of claim 33, wherein said sinusoidal voltage is clamped at a predetermined value by adjusting said feedback signal (FB; FB2) to said controller.

Patentansprüche

1. Treiberschaltung, die derart betrieben werden kann, dass sie eine geregelte Leistung mit Grauskala-Bildsteuerung für einen elektrolumineszenten Bildschirm bereitstellt, bei dem Pixel in Reihen und Spalten angeordnet sind, wobei Energie verwendet wird, die gewonnen wird aus einer variablen Schirmkapazität (C_p) des Bildschirms, umfassend:

eine Quelle für elektrische Energie (VDC); und

eine Resonanzschaltung (62, 64), die derart betrieben werden kann, dass die Schirmkapazität (C_p) genutzt wird, zum Aufnehmen der elektrischen Energie und, als Reaktion darauf, zum Erzeugen einer Sinusspannung, mit der der Bildschirm bei einer Resonanzfrequenz versorgt wird, die im Wesentlichen synchron ist mit einer Abtastfrequenz des Bildschirms;

dadurch gekennzeichnet, dass die Treiberschaltung zudem eine Schaltung (U1, U12) umfasst, die derart betrieben werden kann, dass die Sinusspannung bei einem im Wesentlichen festen Wert festgehalten werden kann, übersteigt die Spannung an entweder die Reihen oder die Spalten des Bildschirms einen zuvor bestimmten Wert, wodurch der Maximalwert der Sinusspannung bei Schwankungen in der Schirmkapazität (C_p) geregelt wird.

2. Treiberschaltung nach Anspruch 1, wobei die Resonanzschaltung (62, 64) zudem einen Abwärtstransformator (T2,

T1) umfasst, der derart betrieben werden kann, dass die wirksame Schirmkapazität (C_p) des Bildschirm verringert wird.

- 5 3. Treiberschaltung nach Anspruch 2, wobei der Abwärtstransformator (T2, T1) Folgendes besitzt: eine Primärwicklung, über die eine weitere Kapazität (C1; C41, C42) angeschlossen ist; eine erste Sekundärwicklung, über die die Schirmkapazität (C_p) angeschlossen ist, wobei der Wert der weiteren Kapazität (C1; C41, C42) verglichen mit der Schirmkapazität (C_p) genügend hoch ist, dass im Wesentlichen eine Synchronisation der Resonanzfrequenz mit der Abtastfrequenz aufrechterhalten wird; und eine weitere Sekundärwicklung, die verbunden ist mit einem Vollwellengleichrichter mit einem darüber angeschlossenen Speicherkondensator (C_s) und in Reihe mit der Schirmkapazität (C_p), wobei der Wert des Speicherkondensators (C_s) verglichen mit der Schirmkapazität (C_p) genügend hoch ist, dass (i) bei einer schweren Schirmbelastung, bei der die Schirmkapazität (C_p) bei oder nahe ihrem Maximalwert ist, der Großteil der elektrischen Energie zu der ersten Sekundärwicklung fließt, so dass der Schirm aufgeladen wird und die Energieladungen des Speicherkondensators (C_s) erhalten bleiben, (ii) bei einer durchschnittlichen Belastung, bei der die Schirmkapazität einen durchschnittlichen Wert aufweist, etwa die Hälfte der Energie zum Schirm fließt und die Hälfte der Energie zum Speicherkondensator (C_s), und (iii) bei einer leichten Belastung, bei der die Schirmkapazität bei oder nahe ihrem Minimalwert ist, der Großteil der Energie zum Speicherkondensator fließt und die restliche Energie zum Schirm.
- 10 4. Treiberschaltung nach Anspruch 3, wobei das Verhältnis der Kapazität des Speicherkondensators (C_s) zur maximalen Schirmkapazität mindestens etwa 10:1 beträgt.
- 15 5. Treiberschaltung nach Anspruch 4, wobei das Verhältnis der Kapazität des Speicherkondensators (C_s) zur maximalen Schirmkapazität mindestens etwa 20:1 beträgt.
- 20 6. Treiberschaltung nach Anspruch 5, wobei das Verhältnis der Kapazität des Speicherkondensators (C_s) zur maximalen Schirmkapazität mindestens etwa 30:1 beträgt.
- 25 7. Treiberschaltung nach Anspruch 3, wobei der Vollwellengleichrichter Schottky-Dioden enthält, die derart betrieben werden können, dass sie den Durchlassdioden-Spannungsabfall minimieren.
- 30 8. Treiberschaltung nach Anspruch 3, wobei das Verhältnis der Windungen der weiteren Sekundärwicklung zu denjenigen der ersten Sekundärwicklung mindestens etwa 1,05:1 beträgt.
- 35 9. Treiberschaltung nach Anspruch 3, wobei das Verhältnis der Windungen der weiteren Sekundärwicklung zu denen der ersten Sekundärwicklung mindestens etwa 1,1:1 beträgt.
- 40 10. Treiberschaltung nach Anspruch 9, wobei das Verhältnis der Windungen der weiteren Sekundärwicklung zu denen der ersten Sekundärwicklung im Bereich von 1,1:1 bis 1,2:1 liegt.
- 45 11. Treiberschaltung nach Anspruch 3, wobei die Primärwicklung n_1 Windungen hat und die zweite Wicklung n_2 Windungen hat, so dass der Wert der weiteren Kapazität im Wesentlichen größer ist als $(n_2/n_1)^2$, multipliziert mit dem Wert der Schirmkapazität.
- 50 12. Treiberschaltung nach Anspruch 3, die zudem einen zusätzlichen Kondensator (C_f ; C9) umfasst, der derart betrieben werden kann, dass sich die Resonanzfrequenz ändert.
- 55 13. Treiberschaltung nach Anspruch 1, wobei die Quelle zudem eine Spannungseinrichtung (VDC; DC-IN) umfasst, die derart betrieben werden kann, dass eine Gleichspannung erzeugt wird; sowie einen Impulsbreitenmodulator (PWM; U1, U12), der derart betrieben werden kann, dass die Gleichspannung in elektrische Energieimpulse zerhackt wird.
14. Treiberschaltung nach Anspruch 1, die zudem einen Regler umfasst, der derart betrieben werden kann, dass er die Rate der elektrischen Energie regelt, die von der Resonanzschaltung aufgenommen wird, so dass Schwankungen der Sinusspannung aufgrund von schwankender Impedanz des Bildschirms und Energieverbrauch durch den Bildschirm geregelt werden.
15. Treiberschaltung nach Anspruch 14, wobei der Regler zudem eine Rückkopplungsschaltung umfasst, die derart betrieben werden kann, dass sie Schwankungen der Sinusspannung unter Verwendung einer Eingabe von der Resonanzschaltung wahrnimmt und als Antwort ein Rückkopplungssignal (FB; FB2) an den Regler liefert.

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16. Treiberschaltung nach Anspruch 15, wobei die Eingabe von einer primären Wicklung eines Abwärtstransformators der Resonanzschaltung stammt.
- 5 17. Treiberschaltung nach Anspruch 16, wobei die Sinusspannung bei einem zuvor festgelegten Wert festgehalten wird, indem das Rückkopplungssignal (FB; FB2) an den Regler eingestellt wird.
- 10 18. Passivmatrix-Bildschirm, umfassend eine Anzahl Reihen (ROW 1, ROW 2, ROW 3, ROW 4), die dafür ausgelegt sind, mit einer festgelegten Abtastfrequenz des Bildschirms abgetastet zu werden; eine Anzahl Spalten (COL 1, COL 2, COL 3, COL 4), die die Reihen schneiden, so dass eine Anzahl Pixel gebildet wird, **gekennzeichnet durch** eine variable Schirmkapazität (C_p); und eine Treiberschaltung nach Anspruch 1.
- 15 19. Passivmatrix-Bildschirm nach Anspruch 18, wobei die Resonanzschaltung (62, 64) zudem einen Abwärtstransformator (T2, T1) umfasst, der derart betrieben werden kann, dass die wirksame Schirmkapazität (C_p) des Bildschirm verringert wird.
- 20 20. Passivmatrix-Bildschirm nach Anspruch 19, wobei der Abwärtstransformator (T2, T1) Folgendes besitzt: eine Primärwicklung, über die eine weitere Kapazität (C1; C41, C42) angeschlossen ist; eine erste Sekundärwicklung, über die die Schirmkapazität (C_p) angeschlossen ist, wobei der Wert der weiteren Kapazität (C1; C41, C42) verglichen mit der Schirmkapazität (C_p) genügend hoch ist, dass im Wesentlichen eine Synchronisation der Resonanzfrequenz mit der Abtastfrequenz aufrechterhalten wird; und eine weitere Sekundärwicklung, die verbunden ist mit einem Vollwellengleichrichter mit einem darüber angeschlossenen Speicherkondensator (C_s) und in Reihe mit der Schirmkapazität (C_p), wobei der Wert des Speicherkondensators (C_s) verglichen mit der Schirmkapazität (C_p) genügend hoch ist, dass (i) bei einer schweren Schirmbelastung, bei der die Schirmkapazität (C_p) bei oder nahe ihrem Maximalwert ist, der Großteil der elektrischen Energie zu der ersten Sekundärwicklung fließt, so dass der Schirm aufgeladen wird und die Energieladungen des Speicherkondensators (C_s) erhalten bleiben, (ii) bei einer durchschnittlichen Belastung, bei der die Schirmkapazität einen durchschnittlichen Wert aufweist, etwa die Hälfte der Energie zum Schirm fließt und die Hälfte der Energie zum Speicherkondensator (C_s), und (iii) bei einer leichten Belastung, bei der die Schirmkapazität bei oder nahe ihrem Minimalwert ist, der Großteil der Energie zum Speicherkondensator fließt und die restliche Energie zum Schirm.
- 25 30 21. Passivmatrix-Bildschirm nach Anspruch 20, wobei das Verhältnis der Kapazität des Speicherkondensators (C_s) zur maximalen Schirmkapazität mindestens etwa 10:1 beträgt.
- 35 22. Passivmatrix-Bildschirm nach Anspruch 21, wobei das Verhältnis der Kapazität des Speicherkondensators (C_s) zur maximalen Schirmkapazität mindestens etwa 20:1 beträgt.
23. Passivmatrix-Bildschirm nach Anspruch 22, wobei das Verhältnis der Kapazität des Speicherkondensators (C_s) zur maximalen Schirmkapazität mindestens etwa 30:1 beträgt.
- 40 24. Passivmatrix-Bildschirm nach Anspruch 20, wobei der Vollwellengleichrichter Schottky-Dioden enthält, die derart betrieben werden können, dass sie den Durchlassdioden-Spannungsabfall minimieren.
25. Passivmatrix-Bildschirm nach Anspruch 20, wobei das Verhältnis der Windungen der weiteren Sekundärwicklung zu denen der ersten Sekundärwicklung mindestens etwa 1,05:1 beträgt.
- 45 26. Passivmatrix-Bildschirm nach Anspruch 20, wobei das Verhältnis der Windungen der weiteren Sekundärwicklung zu denen der ersten Sekundärwicklung mindestens etwa 1,1:1 beträgt.
27. Passivmatrix-Bildschirm nach Anspruch 20, wobei das Verhältnis der Windungen der weiteren Sekundärwicklung zu denjenigen der ersten Sekundärwicklung im Bereich von 1,1:1 bis 1,2:1 liegt.
- 50 28. Passivmatrix-Bildschirm nach Anspruch 26, wobei die Primärwicklung n_1 Windungen hat und die zweite Wicklung n_2 Windungen hat, so dass der Wert der weiteren Kapazität im Wesentlichen größer ist als $(n_2/n_1)^2$, multipliziert mit dem Wert der Schirmkapazität.
- 55 29. Passivmatrix-Bildschirm nach Anspruch 20, die zudem einen zusätzlichen Kondensator (Cf; C9) umfasst, der derart betrieben werden kann, dass sich die Resonanzfrequenz ändert.

30. Passivmatrix-Bildschirm nach Anspruch 18, wobei die Quelle zudem eine Spannungseinrichtung (VDC; DC-IN) umfasst, die derart betrieben werden kann, dass eine Gleichspannung erzeugt wird; sowie einen Impulsbreitenmodulator (PWM; U1, U12), der derart betrieben werden kann, dass die Gleichspannung in elektrische Energieimpulse zerhackt wird.

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31. Passivmatrix-Bildschirm nach Anspruch 18, die zudem einen Regler umfasst, der derart betrieben werden kann, dass er die Rate der elektrischen Energie regelt, die von der Resonanzschaltung aufgenommen wird, so dass Schwankungen der Sinusspannung aufgrund von schwankender Impedanz des Bildschirms und Energieverbrauch durch den Bildschirm geregelt werden.

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32. Passivmatrix-Bildschirm nach Anspruch 31, wobei der Regler zudem eine Rückkopplungsschaltung umfasst, die derart betrieben werden kann, dass sie Schwankungen der Sinusspannung unter Verwendung einer Eingabe von der Resonanzschaltung wahrnimmt und als Antwort ein Rückkopplungssignal (FB; FB2) an den Regler liefert.

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33. Passivmatrix-Bildschirm nach Anspruch 32, wobei die Eingabe von einer primären Wicklung eines Abwärtstransformators der Resonanzschaltung stammt.

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34. Passivmatrix-Bildschirm nach Anspruch 33, wobei die Sinusspannung bei einem zuvor festgelegten Wert festgehalten wird, indem das Rückkopplungssignal (FB; FB2) an den Regler eingestellt wird.

Revendications

25
1. Circuit de commande activable pour fournir une alimentation régulée avec un réglage de l'image à échelle de gris d'un écran électroluminescent dont les pixels sont agencés en rangées et colonnes au moyen de l'énergie récupérée à partir d'une capacité de panneau variable (C_p) dudit écran, comprenant :

30
une source d'énergie électrique (VDC) ; et
un circuit résonant (62, 64) activable pour utiliser ladite capacité de panneau (C_p), destiné à recevoir ladite énergie électrique et, en réponse, pour générer une tension sinusoïdale pour alimenter ledit écran à une fréquence de résonance qui est sensiblement synchronisée sur une fréquence de balayage dudit écran ;

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caractérisé en ce que le circuit de commande comprend en outre un circuit (U1, U12) activable pour caler ladite tension sinusoïdale à une valeur sensiblement fixe lorsque la tension fournie aux rangées ou aux colonnes dudit écran dépasse une valeur prédéterminée, en régulant ainsi la valeur maximale de ladite tension sinusoïdale dans l'éventualité de variations de ladite capacité de panneau (C_p).

40
2. Circuit de commande selon la revendication 1, dans lequel ledit circuit résonant (62, 64) comprend en outre un transformateur abaisseur de tension (T2, T1) activable pour réduire la capacité de panneau (C_p) effective dudit écran.

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3. Circuit de commande selon la revendication 2, dans lequel ledit transformateur abaisseur de tension (T1, T2) possède un enroulement primaire aux bornes duquel une capacité supplémentaire (C_1 ; C41, C42) est connectée ; un premier enroulement secondaire aux bornes duquel ladite capacité de panneau (C_p) est connectée, la valeur de ladite capacité supplémentaire (C_1 ; C41, C42) étant suffisamment grande par rapport à ladite capacité de panneau (C_p) pour maintenir une synchronisation substantielle de ladite fréquence de résonance sur ladite fréquence de balayage ; et un enroulement secondaire supplémentaire connecté à un redresseur double alternance avec un condensateur de stockage (C_s) connecté à ses bornes et en série avec ladite capacité de panneau (C_p), la valeur dudit condensateur de stockage (C_s) étant suffisamment grande par rapport à ladite capacité de panneau (C_p) pour que (i) pour une charge de panneau élevée où la capacité de panneau (C_p) est à sa valeur maximale ou proche de celle-ci, la majeure partie de ladite énergie électrique passe au premier enroulement secondaire pour charger le panneau et l'énergie restante charge le condensateur de stockage (C_s), (ii) pour une charge moyenne où la capacité de panneau a une valeur moyenne, approximativement la moitié de l'énergie passe au panneau et la moitié de l'énergie passe au condensateur de stockage (C_s), et (iii) pour une charge faible où la capacité de panneau est à une valeur minimale ou proche de celle-ci, la majeure partie de l'énergie passe au condensateur de stockage et l'énergie restante passe au panneau.

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4. Circuit de commande selon la revendication 3, dans lequel le rapport entre la capacité du condensateur de stockage (C_s) et la capacité de panneau maximale est au moins d'environ 10:1.

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5. Circuit de commande selon la revendication 4, dans lequel le rapport entre la capacité du condensateur de stockage (C_s) et la capacité de panneau maximale est au moins d'environ 20:1.
- 5 6. Circuit de commande selon la revendication 5, dans lequel le rapport entre la capacité du condensateur de stockage (C_s) et la capacité de panneau maximale est au moins d'environ 30:1.
7. Circuit de commande selon la revendication 3, dans lequel ledit redresseur double alternance comporte des diodes Schottky activables pour minimiser la chute de tension directe des diodes.
- 10 8. Circuit de commande selon la revendication 3, dans lequel le rapport de spires entre l'enroulement secondaire supplémentaire et le premier enroulement secondaire est d'au moins 1,05:1.
9. Circuit de commande selon la revendication 3, dans lequel le rapport de spires entre l'enroulement secondaire supplémentaire et le premier enroulement secondaire est d'au moins 1,1:1.
- 15 10. Circuit de commande selon la revendication 9, dans lequel le rapport de spires entre l'enroulement secondaire supplémentaire et le premier enroulement secondaire se trouve dans la plage de 1,1:1 à 1,2:1.
11. Circuit de commande selon la revendication 3, dans lequel ledit enroulement primaire possède n_1 spires et ledit enroulement secondaire possède n_2 spires de sorte que la valeur de la capacité supplémentaire est sensiblement supérieure à $(n_2/n_1)^2$ multiplié par la valeur de la capacité de panneau.
- 20 12. Circuit de commande selon la revendication 3, comprenant en outre un condensateur additionnel (C_f ; C9) activable pour modifier ladite fréquence de résonance.
- 25 13. Circuit de commande selon la revendication 1, dans lequel la source comprend en outre des moyens de tension (VDC ; DC-IN) activables pour générer une tension de courant continu ; et un modulateur d'impulsions en largeur (PWM ; U1, U12) activable pour hacher ladite tension de courant continu en impulsions d'énergie électrique.
- 30 14. Circuit de commande selon la revendication 1, comprenant en outre un régulateur activable pour réguler le taux d'énergie électrique reçu par ledit circuit résonant pour réguler les fluctuations de ladite tension sinusoïdale dues à une impédance variable dudit écran et l'utilisation d'énergie par ledit écran.
- 35 15. Circuit de commande selon la revendication 14, dans lequel ledit régulateur comprend en outre un circuit de réaction activable pour capter les fluctuations de ladite tension sinusoïdale au moyen d'une entrée provenant dudit circuit résonant et fournissant en réponse un signal de réaction (FB ; FB2) audit régulateur.
- 40 16. Circuit de commande selon la revendication 15, dans lequel ladite entrée provient d'un enroulement primaire d'un transformateur abaisseur de tension dudit circuit résonant.
- 45 17. Circuit de commande selon la revendication 16, dans lequel ladite tension sinusoïdale est calée à une valeur prédéterminée en ajustant ledit signal de réaction (FB ; FB2) audit régulateur.
18. Ecran à matrice passive comprenant :
- 50 une pluralité de rangées (ROW 1, ROW 2, ROW 3, ROW 4) adaptées pour être balayées à une fréquence de balayage prédéterminée dudit écran ;
une pluralité de colonnes (COL 1, COL 2, COL 3, COL 4) qui croisent lesdites rangées pour former une pluralité de pixels **caractérisés par** une capacité de panneau variable (C_p) ;
et
un circuit de commande selon la revendication 1.
- 55 19. Ecran à matrice passive selon la revendication 18, dans lequel ledit circuit résonant (62, 64) comprend en outre un transformateur abaisseur de tension (T2, T1) activable pour réduire la capacité de panneau (C_p) effective dudit écran.
20. Ecran à matrice passive selon la revendication 19, dans lequel ledit transformateur abaisseur de tension (T1, T2) possède un enroulement primaire aux bornes duquel une capacité supplémentaire (C1 ; C41, C42) est connectée ; un premier enroulement secondaire aux bornes duquel ladite capacité de panneau (C_p) est connectée, la valeur

de ladite capacité supplémentaire (C_1 ; C_{41} , C_{42}) étant suffisamment grande par rapport à ladite capacité de panneau (C_p) pour maintenir une synchronisation sensible de ladite fréquence de résonance sur ladite fréquence de balayage ; et un enroulement secondaire supplémentaire connecté à un redresseur double alternance avec un condensateur de stockage (C_s) connecté à ses bornes et en série avec ladite capacité de panneau (C_p), la valeur dudit condensateur de stockage (C_s) étant suffisamment grande par rapport à ladite capacité de panneau (C_p) pour que (i) pour une charge de panneau élevée où la capacité de panneau (C_p) est à sa valeur maximale ou proche de celle-ci, la majeure partie de ladite énergie électrique passe au premier enroulement secondaire pour charger le panneau et l'énergie restante charge le condensateur de stockage (C_s), (ii) pour une charge moyenne où la capacité de panneau a une valeur moyenne, approximativement la moitié de l'énergie passe au panneau et la moitié de l'énergie passe au condensateur de stockage (C_s), et (iii) pour une charge faible où la capacité de panneau est à une valeur minimale ou proche de celle-ci, la majeure partie de l'énergie passe au condensateur de stockage et l'énergie restante passe au panneau.

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21. Ecran à matrice passive selon la revendication 20, dans lequel le rapport entre la capacité du condensateur de stockage (C_s) et la capacité de panneau maximale est au moins d'environ 10:1.
 22. Ecran à matrice passive selon la revendication 21, dans lequel le rapport entre la capacité du condensateur de stockage (C_s) et la capacité de panneau maximale est au moins d'environ 20:1.
 23. Ecran à matrice passive selon la revendication 22, dans lequel le rapport entre la capacité du condensateur de stockage (C_s) et la capacité de panneau maximale est au moins d'environ 30:1.
 24. Ecran à matrice passive selon la revendication 20, dans lequel ledit redresseur double alternance comporte des diodes Schottky activables pour minimiser la chute de tension directe des diodes.
 25. Ecran à matrice passive selon la revendication 20, dans lequel le rapport de spires entre l'enroulement secondaire supplémentaire et le premier enroulement secondaire est d'au moins 1,05:1.
 26. Ecran à matrice passive selon la revendication 20, dans lequel le rapport de spires entre l'enroulement secondaire supplémentaire et le premier enroulement secondaire est d'au moins 1,1:1.
 27. Ecran à matrice passive selon la revendication 26, dans lequel le rapport de spires entre l'enroulement secondaire supplémentaire et le premier enroulement secondaire se trouve dans la plage de 1,1:1 à 1,2:1.
 28. Ecran à matrice passive selon la revendication 20, dans lequel ledit enroulement primaire possède n_1 spires et ledit enroulement secondaire possède n_2 spires de sorte que la valeur de la capacité supplémentaire est sensiblement supérieure à $(n_2/n_1)^2$ multiplié par la valeur de la capacité de panneau.
 29. Ecran à matrice passive selon la revendication 20, comprenant en outre un condensateur additionnel (C_f ; C_9) activable pour modifier ladite fréquence de résonance.
 30. Ecran à matrice passive selon la revendication 18, dans lequel la source comprend en outre des moyens de tension (VDC ; DC-IN) activables pour générer une tension de courant continu; et un modulateur d'impulsions en largeur (PWM ; U1, U12) activable pour hacher ladite tension de courant continu en impulsions d'énergie électrique.
 31. Ecran à matrice passive selon la revendication 18, comprenant en outre un régulateur activable pour réguler le taux d'énergie électrique reçu par ledit circuit résonant pour réguler les fluctuations de ladite tension sinusoïdale dues à une impédance variable dudit écran et l'utilisation d'énergie par ledit écran.
 32. Ecran à matrice passive selon la revendication 31, dans lequel ledit régulateur comprend en outre un circuit de rétroaction activable pour capter les fluctuations de ladite tension sinusoïdale au moyen d'une entrée provenant dudit circuit résonant et fournissant en réponse un signal de réaction (FB ; FB2) audit régulateur.
 33. Ecran à matrice passive selon la revendication 32, dans lequel ladite entrée provient d'un enroulement primaire d'un transformateur abaisseur de tension dudit circuit résonant.
 34. Ecran à matrice passive selon la revendication 33, dans lequel ladite tension sinusoïdale est calée à une valeur prédéterminée en ajustant ledit signal de réaction (FB ; FB2) audit régulateur.

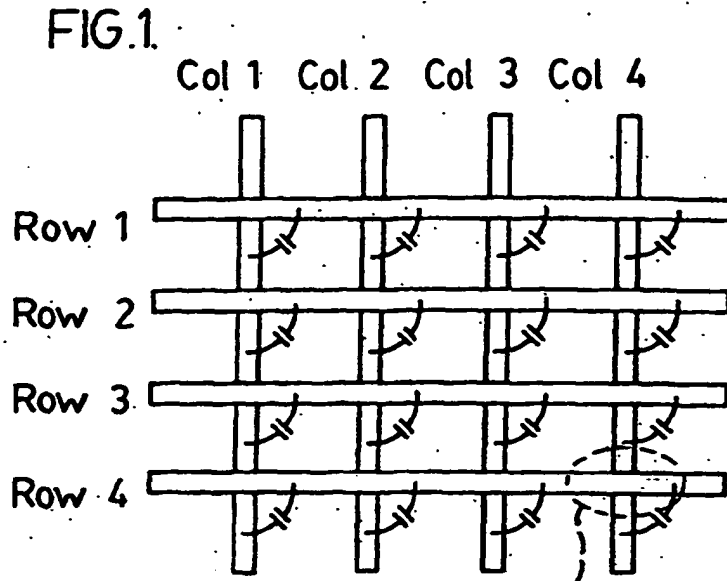
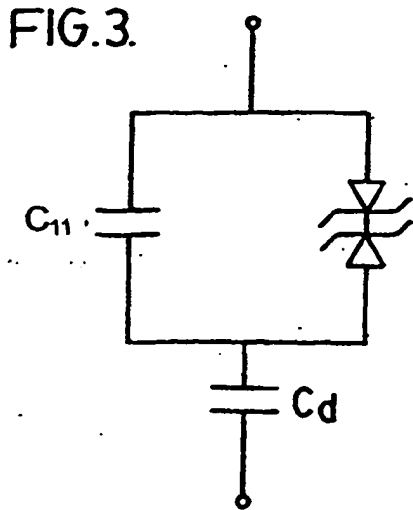
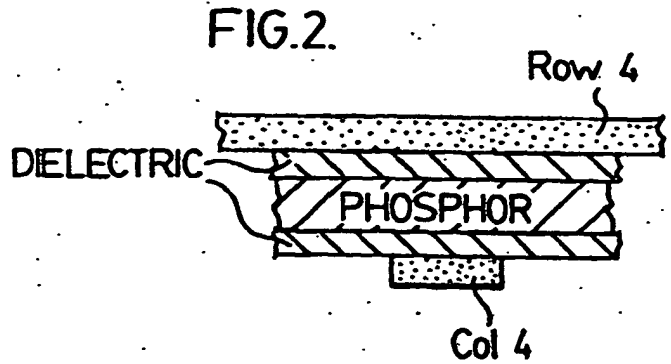


FIG. 2



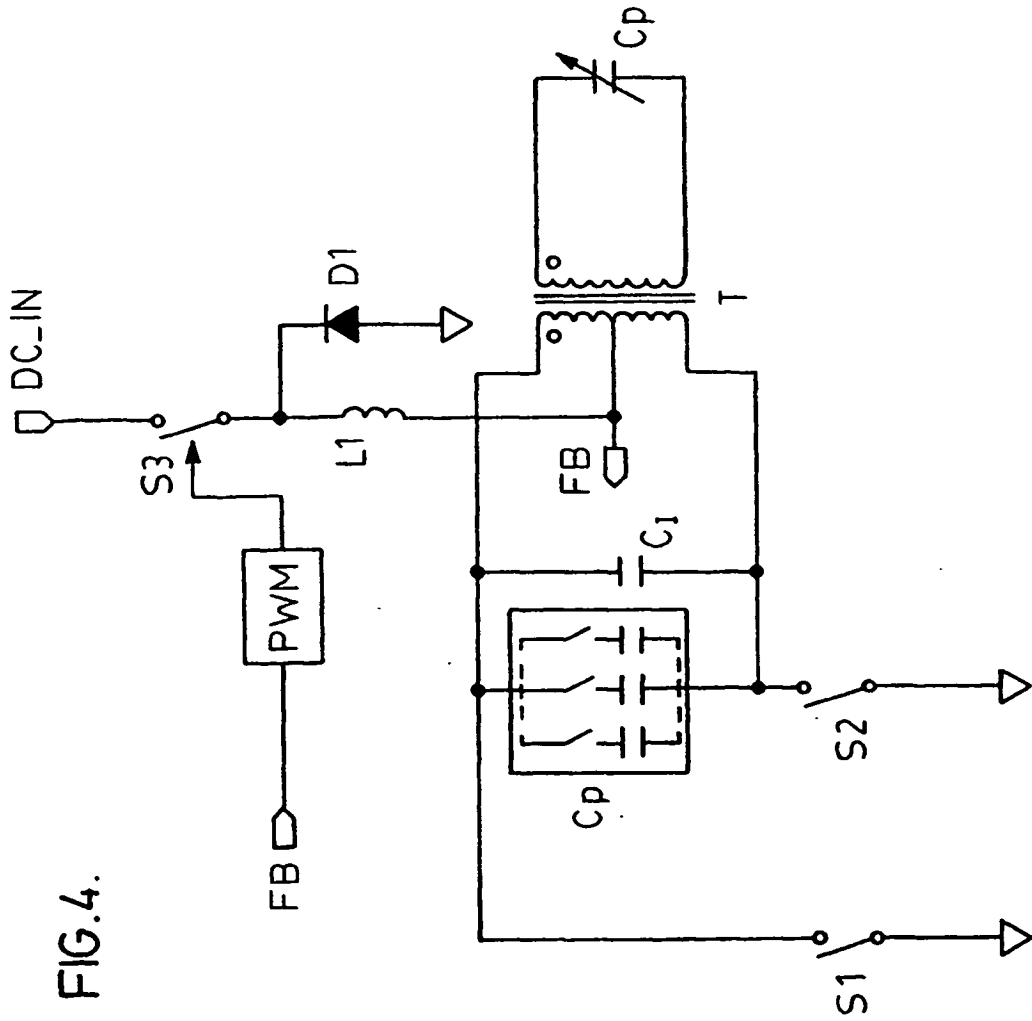


FIG. 4.

FIG.5a.

Waveform distortion due to resonant frequency too high

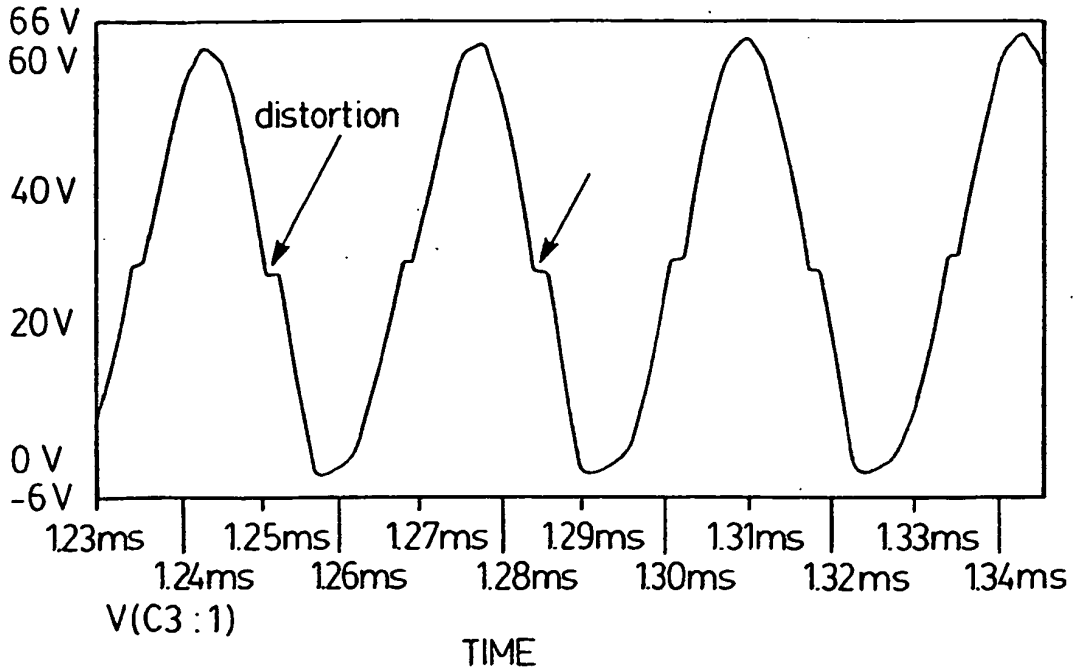


FIG.5b.

Waveform distortion due to resonant frequency too low

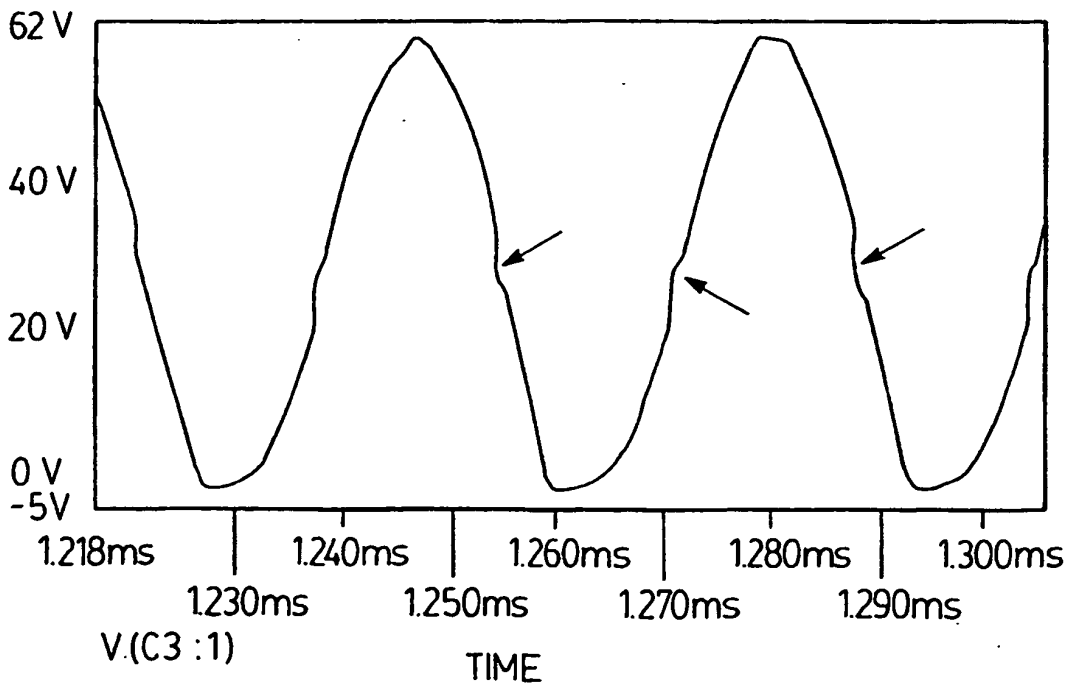


FIG. 5c.

Row drive polarity switch output showing +ve and -ve display cycle (6 lines per frame shown)

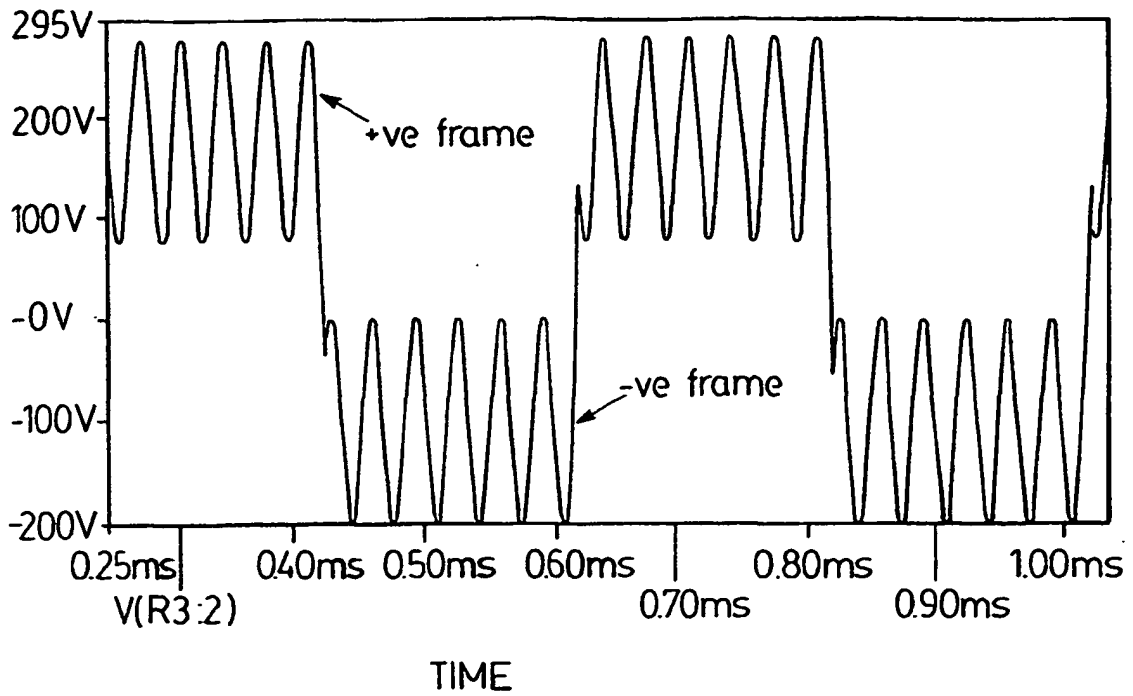


FIG. 6.

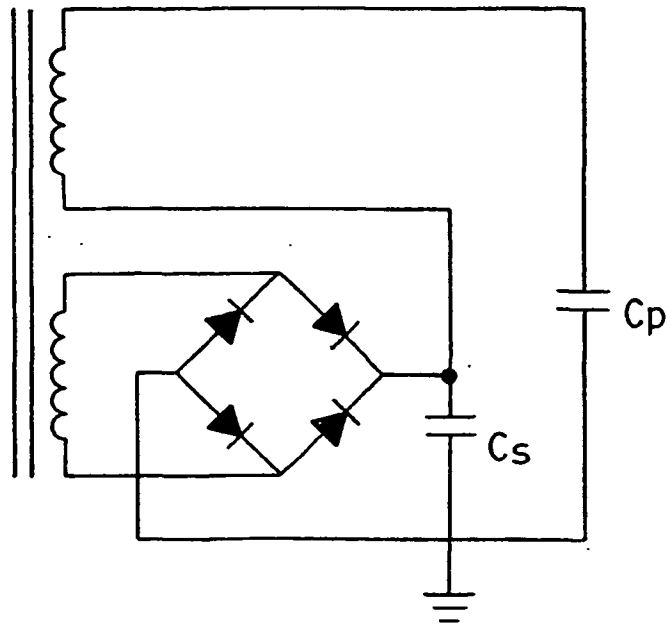


FIG. 7.

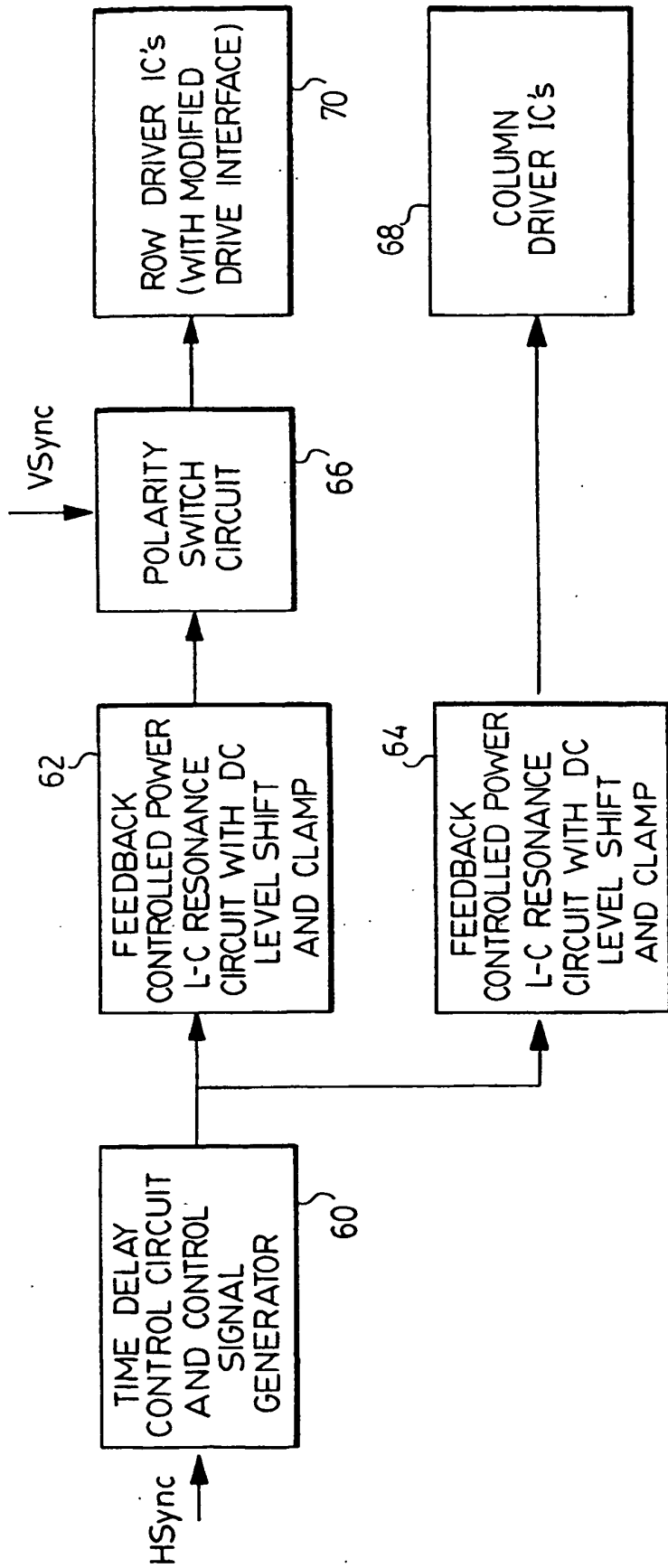


FIG. 8.

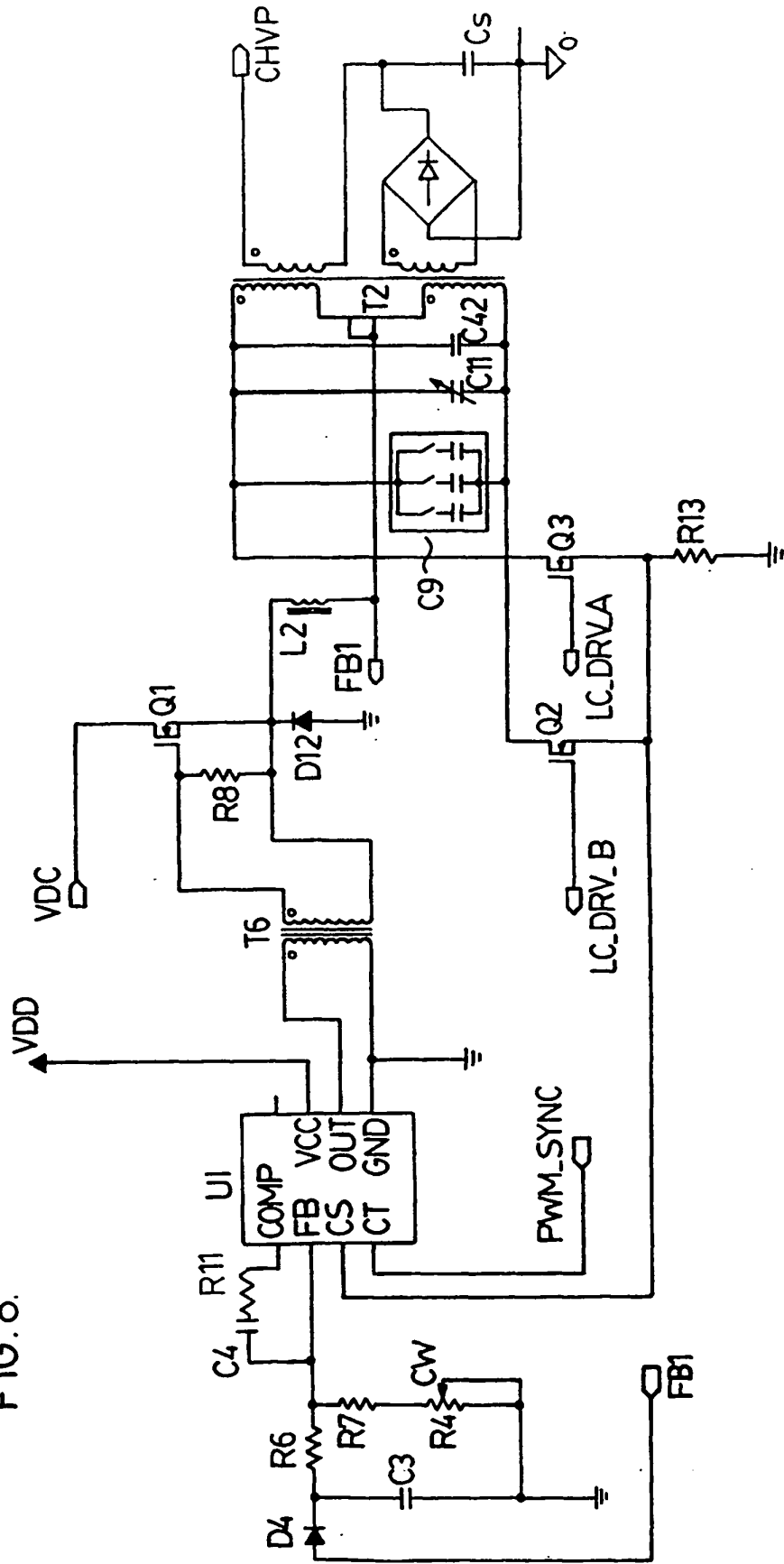
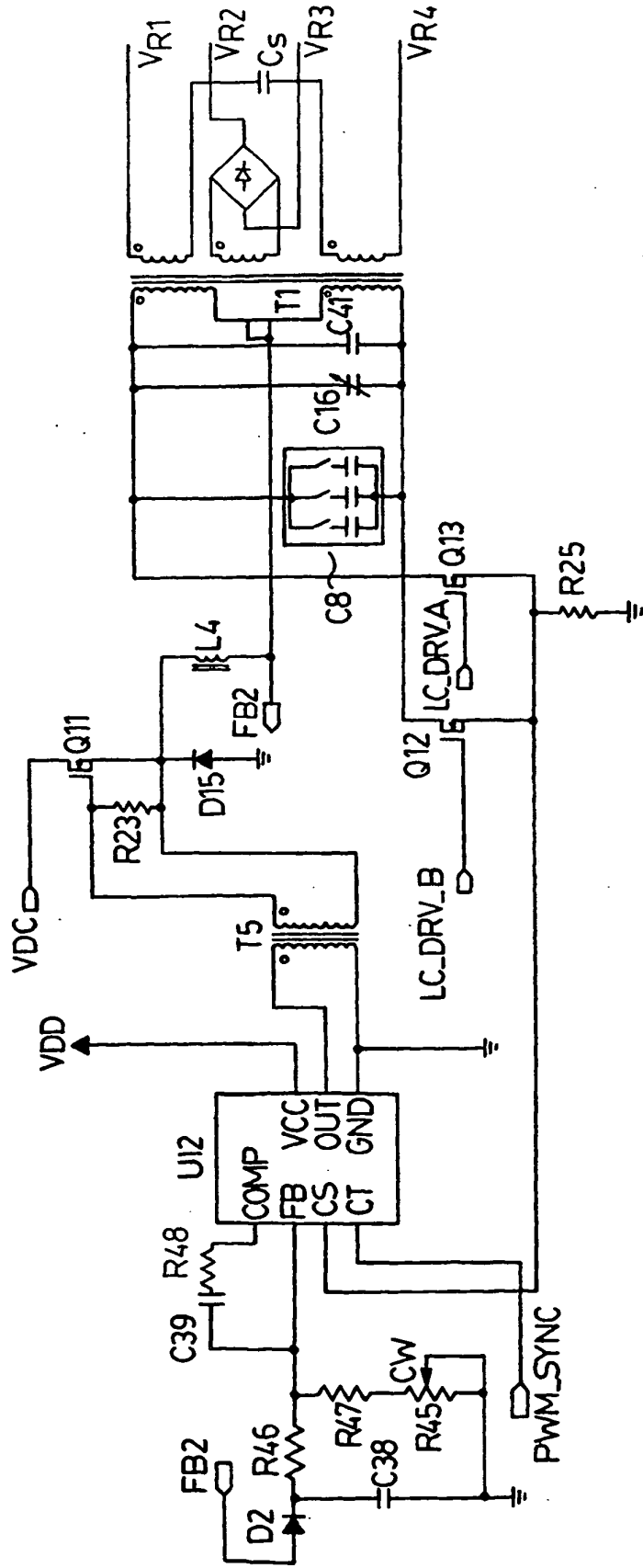


FIG. 9.



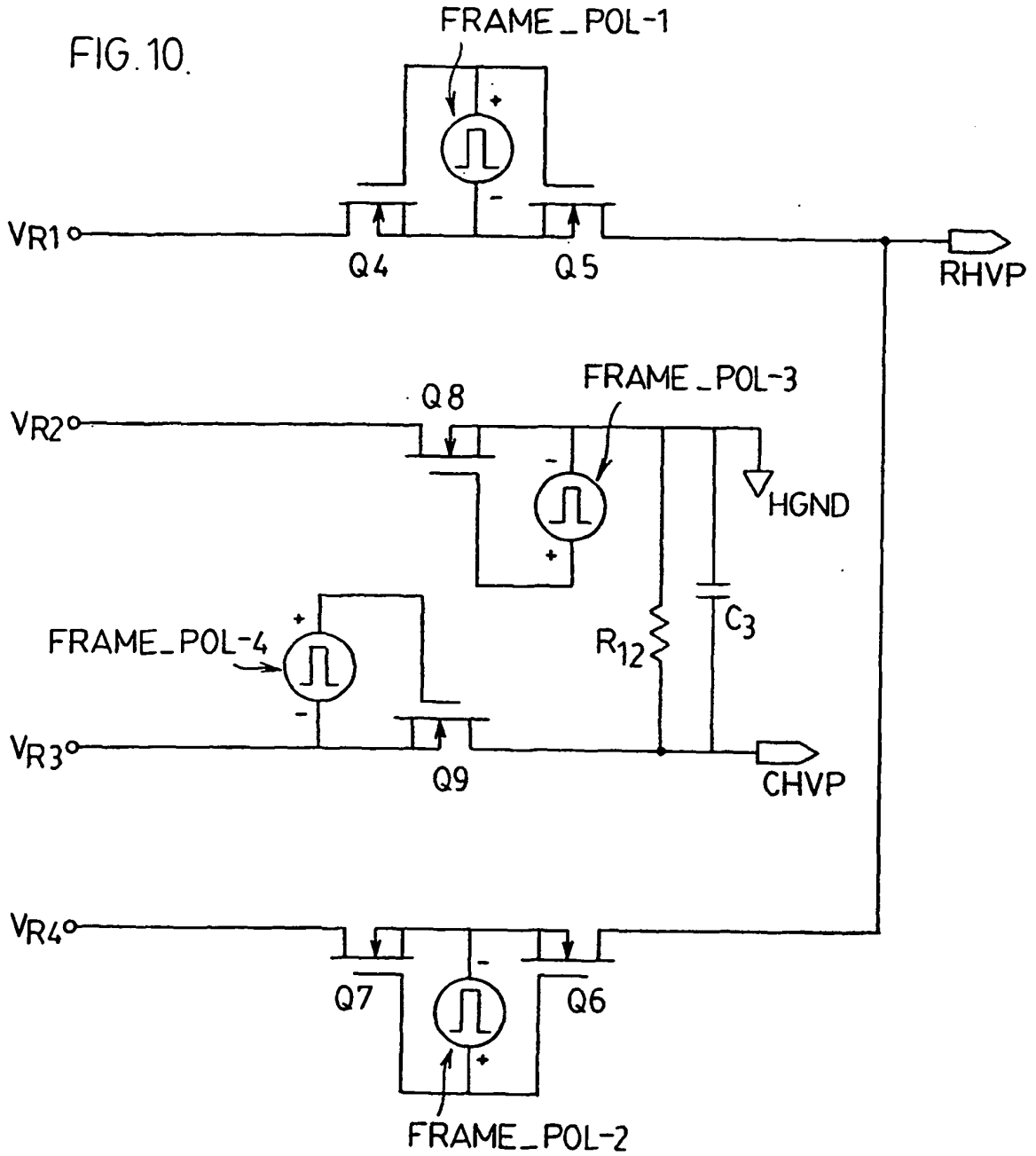


FIG. 11

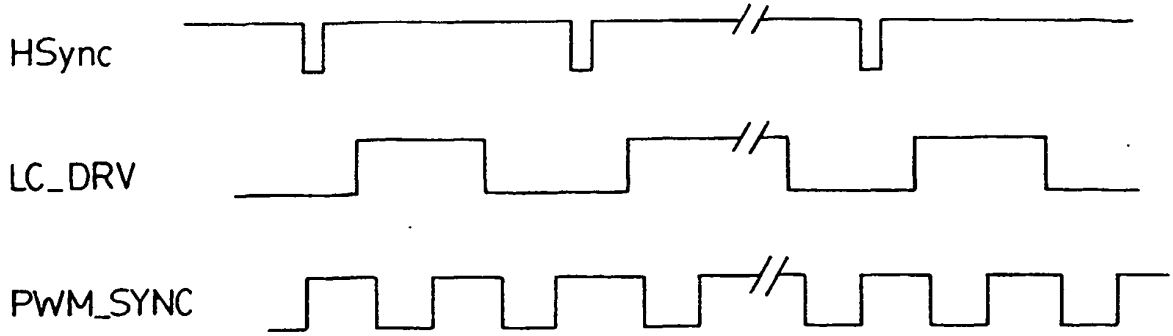
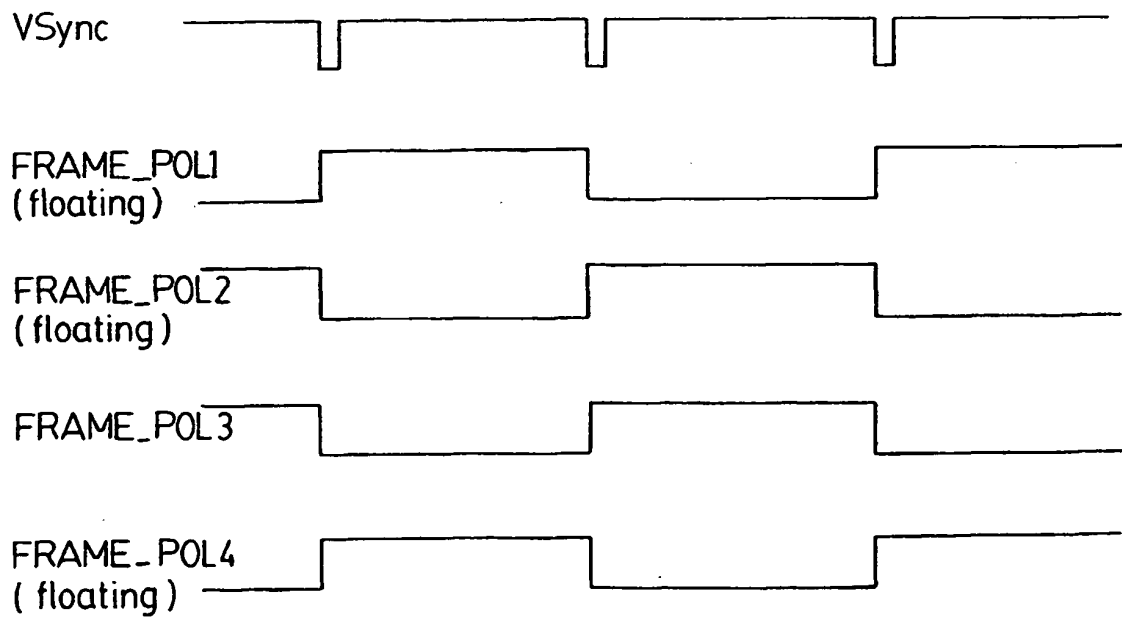


FIG. 12



专利名称(译)	用于电致发光显示器的节能灰度驱动器		
公开(公告)号	EP1459283B1	公开(公告)日	2007-03-28
申请号	EP2002787298	申请日	2002-12-23
[标]申请(专利权)人(译)	伊菲雷技术公司		
申请(专利权)人(译)	IFIRE TECHNOLOGY INC.		
当前申请(专利权)人(译)	IFIRE科技股份有限公司.		
[标]发明人	CHENG CHUN FAI		
发明人	CHENG, CHUN-FAI		
IPC分类号	G09G3/30 G09G3/20		
CPC分类号	G09G3/30 G09G2330/023		
优先权	10/036002 2001-12-26 US		
其他公开文献	EP1459283A1		
外部链接	Espacenet		

摘要(译)

驱动电路包括谐振电路，该谐振电路能够有效地恢复存储在像素行上的电容能量，并在寻址行时将其传送到另一行像素。谐振电路包括降压变压器，跨越初级绕组的电容器，连接的显示板的行或列与次级绕组和输入电压和FET开关，以驱动谐振电路与控制寻址的定时脉冲同步显示器。本发明的改进是附加的次级绕组，其连接到整流器和DC存储电容器，其与面板的列行串联连接。附加电路有助于将驱动器电压钳位到恒定水平，而不管由于负载阻抗的波动引起的负载变化。

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$