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(54) **Data drive circuit for current writing type active matrix organic luminescent display panel**

Datentreiberschaltung für eine stromgesteuerte organische Elektrolumineszenzanzeige mit einer aktiven Matrix

Circuit de commande de données pour panneau d'affichage organique électroluminescent, commandé par courant, à matrice active

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(56) References cited:  
**EP-A- 1 039 440 EP-A- 1 130 781**  
**EP-A- 1 282 103 US-A- 6 091 203**  
**US-A- 6 097 359 US-B1- 6 323 631**

**EP 1 327 972 B1**

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**Description**

[0001] This application claims the benefit of the Korean Application No. P 2002-1175, filed on January 9, 2002.

5 **BACKGROUND OF THE INVENTION**

**Field of the Invention**

10 [0002] The present invention relates to a data drive circuit for a current writing type AMOEL display panel.

**Background of the Related Art**

15 [0003] In general, there are two kinds of AMOEL (Active Matrix Organic ElectroLuminescent) pixel structures; a voltage writing type pixel structure and a current writing type pixel structure. The AMOEL display panel of the current writing type pixel structure is sensitive to noises, such as variation of a threshold voltage, and an irregular voltage rise at an earth line.

[0004] FIG. 1 illustrates a related art circuit of a voltage writing type pixel structure of two positive elements.

20 [0005] Referring to FIG. 1, there is a charge storage capacitor Cstg having both a drive transistor Q1 for direct driving of an organic electroluminescent (OEL) and a positive power source  $V_{DD}$  connected thereto. The drive transistor Q1 has one side connected to an anode of the OEL. There is a switching transistor Q2 having a gate connected to a scanline for switching the OEL under the control of a signal from the scanline. The switching transistor Q2 has a source connected to a dataline, a drain connected to a gate of the drive transistor Q1. The charge storage capacitor Cstg is connected both to the positive power source  $V_{DD}$  and the gate of the drive transistor Q1. As shown in FIG. 1, the drive transistor Q1 and the switching transistor Q2 are PMOS (P type Metal Oxide Semiconductor).

25 [0006] The operation of the circuit in FIG. 1 will be explained.

[0007] A data voltage having a gray scale adjusted is provided from the dataline both to the charge storage capacitor Cstg and the gate of the drive transistor Q1 through the switching transistor Q2. When the switching transistor Q2 is closed in response to the scanline signal, a data voltage of the gray scale of each pixel is written on the charge storage capacitor Cstg through the dataline. The written data voltage is used as a control voltage for fixing a current level of the drive transistor Q1. The current by the control voltage is provided to the OEL through the drive transistor Q1. The AMOEL panel has lots of pixels, wherein, if voltage-current characteristics of the drive transistors Q1 between the pixels are not uniform, currents to the OELs in the pixels are not uniform, even if the voltages written on the charge storage capacitors Cstg are the same, which results in a non-uniform display, i.e., non-uniform luminance, on the AMOEL display panel, that is one of disadvantages of the voltage writing type.

35 [0008] FIG. 2 illustrates a circuit of a related art pixel of the current writing type. Different from the voltage writing type shown in FIG. 1, a current level of the gray scale is written on the drive transistor P1, directly.

[0009] Referring to FIG. 2, if a data drive circuit for providing a write current  $I_{data}$  is operable uniformly, the organic EL panel can display uniformly, even if the voltage-current characteristics of the drive transistors P1 of the pixels are not uniform. However, FIG. 2 illustrates a data drive circuit for only one pixel, actually. That is, a part for providing the writing current is present, not as only one circuit in the data drive circuit part, but for every dataline, or a few datalines. Therefore, if there are errors among the circuits that provide the writing currents, the pixels of the current writing type can not make the best use of their advantages, such that the organic EL panel fails to have uniform display characteristics.

40 [0010] For solving the problem of FIG. 2, a circuit illustrated in FIG. 3 may be used. FIG. 3 illustrates a circuit for mirroring a reference current source  $I_{REF}$  for providing desired current sources. In this case, one reference current source is employed in the data drive circuit. However, referring to FIG. 3, if one reference current source is mirrored to all the datalines, the reference current source can not exactly be mirrored, if a distance between transistors that act as mirrors is too far from the reference current source.

45 [0011] Referring to FIG. 4, as another method, a circuit for correcting the reference current source  $I_{REF}$  can be employed. In a case of this circuit, current source devices, such as transistors, and charge storage capacitors may be used for making calibration periods equal for the datalines. However, a current leakage between a gate and a source of the charge storage transistor causes voltage variations on the datalines, and non-uniform output currents between the datalines. EP1,039,440, discusses data drive circuitry for a display panel, according to the preamble of claim 1.

55 **SUMMARY OF THE INVENTION**

[0012] Accordingly, the present invention is directed to a data drive circuit for an AMOEL display panel having a current writing type pixel structure that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0013] An object of the present invention is to provide a data drive circuit for an AMOEL display panel having a current writing type pixel structure, in which a difference between output current levels is minimized in channels for making uniform driving of an AMOEL panel having a current writing type pixel structure.

[0014] Another object of the present invention is to provide a data drive circuit for a current writing type AMOEL display panel, which can make uniform and accurate display of a data on an AMOEL display channel according to a size of a current flowing through the AMOEL display panel.

[0015] Further object of the present invention is to provide a data drive circuit for a TFT-AMOEL or single crystalline AMOEL display panel having a current writing type pixel structure.

[0016] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0017] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the data drive circuit for a current writing type AMOEL display panel including a plurality of current output channels, and a plurality of channel current generating circuits on respective current output channels for minimizing a difference of current levels occurred between the current output channels, each inclusive of one pair of PMOS transistors having the same widths and lengths and a common gate terminal, a first bias circuit connected to the common gate terminal of the pair of PMOS transistors for prevention of floating of the common gate terminal, a first NMOS transistor for receiving an output current from the pair of PMOS transistors, n (n=1, 2, 3, ----) second NMOS transistors connected to a gate terminal of the first NMOS transistor, each for forming a current mirror with the first NMOS transistor for mirroring the output current from the pair of the PMOS transistors, and n PMOS transistors respectively connected to the n second NMOS transistors in series, wherein outputs of the n PMOS transistors are connected in parallel.

[0018] Preferably, the pair of PMOS transistors have the same widths and lengths.

[0019] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0020] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention:

[0021] In the drawings:

- FIG. 1 illustrates a related art data drive circuit for a voltage writing type display panel with two positive elements;
- FIG. 2 illustrates a related art data drive circuit for a current writing type display panel;
- FIG. 3 illustrates a related art data drive circuit for a current writing type display panel having a method for mirroring a reference current source applied thereto;
- FIG. 4 illustrates a related art data drive circuit for a current writing type display panel having a method for correcting by using a reference current source applied thereto;
- FIG. 5A illustrates a data drive circuit for a current writing type AMOEL display panel in accordance with a preferred embodiment of the present invention; and
- FIG. 5B illustrates a detailed circuit of each of the channel current generating circuits in FIG. 5A.

#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[0022] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings FIGS. 5A and 5B. FIG. 5A illustrates a block diagram of a data drive circuit for a current writing type AMOEL display panel in accordance with a preferred embodiment of the present invention.

[0023] Referring to FIG. 5A, the data drive circuit includes a plurality of current output channels  $I_{out1}$ ,  $I_{out2}$ , ----,  $I_{outk}$ , and a plurality of channel current generating circuits at respective current output channel positions for minimizing differences of current levels occurred between the current output channels  $I_{out1}$ ,  $I_{out2}$ , ----,  $I_{outk}$ .

[0024] Referring to FIG. 5B, the channel current generating circuit includes one pair of PMOS transistors Q1 and Q2 having the same width and length and a common gate terminal, a bias circuit 10 connected to the common gate terminal of the pair of the PMOS transistors Q1 and Q2 for prevention of floating of the common gate terminal, a first NMOS transistor M1 for receiving a current from the pair of PMOS transistors Q1 and Q2, n second NMOS transistors M2, M3, ----,  $M_{n+1}$  each having a gate terminal in common with the gate terminal of the first NMOS transistor M1, to form a current mirror circuit with the first NMOS transistor M1 for mirroring an current  $I_{Q2}$  from the pair of the PMOS transistors

Q1 and Q2, and n second PMOS transistors D1, D2, ----, Dn respectively connected to output sides of the n second NMOS transistors M2, M3, ----, Mn+1 having outputs connected in parallel to form one of the current output channels Iout1, Iout2, ----, Ioutk.

[0025] Referring to FIG. 5B, one of the pair of PMOS transistors Q1 and Q2 has a body and a source connected to each other connected to a first external bias  $V_{Bias1}$ , and the common gate terminal of the pair of the PMOS transistors is connected to the external bias circuit 10 for prevention of floating. The external bias circuit includes three NMOS transistors connected between the common gate terminal and the ground having a second external bias  $V_{Bias2}$  used as a common gate voltage.

[0026] In the meantime, each of the n PMOS transistors D1, D2, ----, Dn receives an one bit external digital gate signal for controlling a current to a relevant NMOS transistor M. Currents from the second PMOS transistors D1, D2, ----, Dn are added together in parallel and provided as one driving current to one of the current output channels. The driving current is regulated to have a current level of a binary form by combination of n-bit digital signals to the n PMOS transistors D1, D2, ----, Dn. The width and length of each of the n second NMOS transistors M2, M3, ----, Mn+1 is fixed so that a current thereto is to be a  $2^a$  ( $a=0, 1, \dots$ ) times of a current  $I_{Q2}$  from the pair of PMOS transistors.

[0027] As explained, according to the embodiment, a current, having small variation, proportional to square of a difference of threshold voltages of the PMOS transistors Q1 and Q2 is generated by using the pair of the PMOS transistors Q1 and Q2, and mirrored by n current mirror circuits of n+1 NMOS transistors M1, M2, ----, Mn+1. An output current from each of the current mirror circuits are adjusted by a relevant second PMOS transistor 'D' and added together in parallel. The added value is a current value of one channel. Each of the channel current values obtained thus minimizes a difference of levels of the driving currents between channels, and makes uniform operation of the AMOEL display panel.

[0028] Moreover, referring to FIG. 5B, even if voltages induced at the output channels are different due to differences of effective ground resistances in view of respective output channels, voltage rises at the output channels caused by the differences of ground resistances give no great influence to the output currents of the channels, because the current  $I_{Q2}$  generated at the pair of the PMOS transistors Q1 and Q2 is mirrored by the n current mirror circuits of the n+1 NMOS transistors M1, M2, ----, Mn+1. The effect of the voltage rise at the ground line is offset.

[0029] When the data drive circuit has many channels, required very long ground line the channels have in common, the effective resistances of the ground lines between the channels distanced far away from each other are different. If the ground resistances between the channels are different, voltages induced at the ground lines are different. However, referring to FIG. 5B, the current  $I_{Q2}$  from the pair of the PMOS transistors Q1 and Q2 is very small compared to the drive currents of the channels which are output currents of current mirror circuits of the n+1 second NMOS transistors M1, M2, M3, ----, Mn+1, the voltage drop caused by the current  $I_{Q2}$  from pair of the PMOS transistors Q1 and Q2 can be neglected.

[0030] Moreover, the output current from one channel generated by the pair of PMOS transistors Q1 and Q2 are used after being mirrored by the mirror circuits of the NMOS transistors, the voltage rise caused by the difference of ground resistances give no influence to the output current from the channel. Thus, deviations of current levels between channels having different effective ground voltages can be reduced to a small value.

[0031] The level of the output current Iout from the channel is fixed by controlling the output currents from the current mirror circuits mirrored a current  $I_{Q2}$  of the first NMOS transistor M1 with the n PMOS transistors D1, D2, ----, Dn. The n second PMOS transistors D1, D2, ----, Dn control output currents from the current mirror circuits with external n-bit digital signals used as gate signals. The n PMOS transistors D1, D2, ----, Dn which use the n-bit digital signals as their gate signals are connected to the n second NMOS transistors M2, M3, ----, Mn+1 in series. Each of the NMOS transistors M2, M3, ----, Mn+1 has a width and a length of  $2^n$  current levels by combination of the n-bits, so as to be one of the  $2^a$  times ( $a=0, 1, 2, \dots$ ) of the current  $I_{Q2}$  from the pair of the PMOS transistors Q1 and Q2.

[0032] The current  $I_{Q2}$  to the first NMOS transistor M1 is generated by the pair of the PMOS transistors Q1 and Q2 having the same width and length with the first NMOS transistor M1. The common gate of the pair of the PMOS transistors Q1 and Q2 has the variable resistance connected thereto. The external bias circuit 10 is connected to the common gate of the pair of the PMOS transistors Q1 and Q2. The source and body of the PMOS transistor Q1 are connected to each other, which are in turn connected to the first external bias current source  $V_{Bias1}$ . The source of the PMOS transistor Q2 is connected to the positive power source  $V_{DD}$ .

[0033] The current  $I_{Q2}$  from the PMOS transistor Q2 is can be calculated by the following equations (1) and (2).

$$|I_{Q1}| = K1 (V_{Bias1} - V_X - |V_{th1}|)^2 \text{-----}$$

$$\text{-----} \quad (1)$$

Where,

$$V_X = V_{Bias1} - |V_{th1}| - \sqrt{(|I_{Q1}|/K1)},$$

5 , and

$$\begin{aligned} |I_{Q2}| &= K2 (V_{DD} - V_X - |V_{th2}|)^2 \\ &= K2 (V_{DD} - V_{Bias1} + |V_{th1}| - |V_{th2}| + \sqrt{(|I_{Q1}|/K1)})^2 \end{aligned}$$

----- (2)

15 where,

$$K1 = \mu_p C \sigma_x (W1/L1),$$

20

$$K2 = \mu_p C \sigma_x (W2/L2).$$

25 **[0034]** Referring to equation (2), if the positive power source voltage  $V_{DD}$ , the first external bias power source  $V_{Bias1}$  and  $\sqrt{(|I_{Q1}|/K1)}$  are constant, the current  $I_{Q2}$  from the PMOS transistor Q2 is proportional to square of a difference of the threshold voltages of the pair of PMOS transistors Q1 and Q2.

30 **[0035]** This implies that, if the PMOS transistors Q1 and Q2 are close in view of design, the pair of PMOS transistors Q1 and Q2 provide a uniform source current  $I_{Q2}$  even if the threshold voltages of the PMOS transistors Q1 and Q2 on respective channels vary when a distance between the current output channels are far.

35 **[0036]** That is, since the pair of PMOS transistors Q1 and Q2 are close in view of a layout, an output from the pair of the PMOS transistors, i.e., a base current  $I_{Q2}$  from the pair of the PMOS transistors Q1 and Q2 has a current value of a small deviation proportional to square of a difference of the threshold voltages of the pair of the PMOS transistors Q1 and Q2, thereby providing comparatively uniform current value.

40 **[0037]** Moreover, if the pair of the PMOS transistors Q1 and Q2 are far apart, the base current  $I_{Q2}$  from the pair of the PMOS transistors Q1 and Q2 is a current of a great deviation proportional to square of a difference of the threshold voltages  $V_{th1}$  and  $V_{th2}$  of the pair of the PMOS transistors Q1 and Q2.

**[0038]** As explained, since the uniform current  $I_{Q2}$  obtained thus passes through the n current mirror circuits of n+1 NMOS transistors positioned close to the pair of PMOS transistors Q1 and Q2, and a parallel sum of the current mirror circuits is used as an output current Iout from one uniform channel of the data drive circuit.

**[0039]** Moreover, the data drive circuit of the embodiment compensates a difference of ground voltages of channels by the following principle even if the difference is occurred.

45 **[0040]** As explained, in a case there are many number of current output channels in the data drive circuit, it is required that a common ground line of the channels is very long depending on positions of the channels. The far away channels have different effective resistance of the ground lines.

**[0041]** For an example, if two far away channels have different effective ground resistances, voltages induced at the ground lines are also different depending on the channels.

50 **[0042]** Since the level of the current  $I_{Q2}$  from the pair of the PMOS transistors for one channel in the data drive circuit is so low compared to the channel output current Iout enough to neglect a voltage drop of the positive power source voltage  $V_{DD}$  caused by the current  $I_{Q2}$  of the pair of the PMOS transistors Q1 and Q2, the voltage rise at the ground line caused by the channel output current Iout acts as a cause to differ the channel output current in a case a current source of NMOS transistors is used simply.

55 **[0043]** The current  $I_{Q2}$  from the pair of the PMOS transistors Q1 and Q2 is used, with the current  $I_{Q2}$  mirrored to the current mirror circuit of the n+1 NMOS transistors M1, M2, ---, Mn+1, the voltage rise at the ground resistance does not affect to the channel output current Iout.

[0044] As has been explained, the data drive circuit for a current writing type AMOEL display panel of the present invention has the following advantages.

[0045] By using a pair of transistors having a width and a length, a current of a small deviation proportional to square of a difference of threshold voltages of the transistors is provided. Accordingly, different from the related art case when a current of a great deviation proportional to square of a difference of the threshold voltages is used, a difference of output current levels can be prevented between current output channels independent from each other and spaced far.

[0046] [0045] It will be apparent to those skilled in the art that various modifications and variations can be made in the data drive circuit for a current writing type AMOEL display panel of the present invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims.

## Claims

1. A data drive circuit for a current writing type AMOEL display panel comprising:

a plurality of current output channels ( $I_{out}$ ); and  
a plurality of channel current generating circuits on respective current output channels **characterized in that**  
each channel current generating circuit includes:

a first pair of PMOS transistors ( $Q_1, Q_2$ ) having the same widths and lengths and a common gate terminal,  
a first bias circuit (10) connected to the common gate terminal of the first pair of PMOS transistors ( $Q_1, Q_2$ ),  
providing a means for preventing floating of the common gate terminal,

a first NMOS transistor ( $M_1$ ) for receiving an output current from the pair of PMOS transistors ( $Q_1, Q_2$ ),  
 $n$  (=1, 2, 3, ---) second NMOS transistors ( $M_2-M_{n+1}$ ), connected to a gate terminal of the first NMOS transistor,  
each for forming a current mirror with the first NMOS transistor for mirroring the output current from the pair  
of the PMOS transistors and  $n$  PMOS transistors ( $D_1-D_n$ ) respectively connected to the  $n$  second NMOS  
transistors ( $M_2-M_{n+1}$ ) in series, wherein outputs of the  $n$  PMOS transistors ( $D_1-D_n$ ) are connected in parallel.

2. The data drive circuit as claimed in claim 1, wherein, of the first pair of the PMOS transistors ( $Q_1, Q_2$ ), a first PMOS transistor ( $Q_1$ ) has a body and a source connected together, which is in turn connected a first external bias circuit (10), and a second PMOS transistor ( $Q_2$ ) has a body and a source connected together, which is in turn connected to a positive voltage power source ( $V_{DD}$ ).

3. The data drive circuit as claimed in claim 1 or 2, wherein the bias circuit (10) includes;  
at least one NMOS transistor connected between the common gate and the ground in series, and  
a second external bias ( $V_{BIAS2}$ ) used as a common gate voltage of the gates of the NMOS transistors.

4. The data drive circuit as claimed in at least one of claims 1 to 3, wherein the  $n$  PMOS transistors ( $D_1-D_n$ ) control currents to the  $n$  second NMOS transistors ( $M_2-M_{n+1}$ ) in response to external  $n$  bit digital signals received as respective gate signals, to forward as respective channel currents.

5. The data drive circuit as claimed in claim 4, wherein the respective channel currents are regulated to have a binary form of desired current levels by combination of the  $n$ -bit digital signals received at the  $n$  PMOS transistors ( $D_1-D_n$ ).

6. The data drive circuit as claimed in at least one of claims 1 to 5, wherein the  $n$  second NMOS transistors ( $M_2-M_{n+1}$ ) have widths and lengths fixed such that currents to the  $n$  second NMOS transistors ( $M_2-M_{n+1}$ ) are  $2^a$  ( $a=0, 1, 2, \dots$ ) times of the output current from the pair of the PMOS transistors ( $Q_1, Q_2$ ).

## Patentansprüche

1. Datentreiberschaltung für eine AMOEL Anzeigetafel des Stromschreibenden Typs, umfassend:

- mehrere Stromausgangskanäle ( $I_{out}$ ); und
- mehrere Kanalstrom-Erzeugungsschaltungen auf entsprechenden Stromausgangskanälen,

**dadurch gekennzeichnet, dass** jede Kanalstrom-Erzeugungsschaltung umfasst:

## EP 1 327 972 B1

- ein erstes Paar von PMOS-Transistoren ( $Q_1, Q_2$ ), die die gleichen Breiten und Längen und einen gemeinsamen Gate-Anschluss aufweisen;
  - eine erste Vorspannungsschaltung (10), die mit dem gemeinsamen Gate-Anschluss des ersten Paares von PMOS-Transistoren ( $Q_1, Q_2$ ) verbunden ist, wodurch Mittel für das Verhindern einer Potentialfreiheit ("Floating") des gemeinsamen Gate-Anschlusses bereitgestellt sind,
  - einen ersten NMOS-Transistor ( $M_1$ ) für das Empfangen eines Ausgangsstroms von dem Paar der PMOS-Transistoren ( $Q_1, Q_2$ ),
  - $n$  ( $=1, 2, 3, \dots$ ) zweite NMOS-Transistoren ( $M_2-M_{n+1}$ ), die mit einem Gate-Anschluss des ersten NMOS-Transistors verbunden sind, wobei jeder einen Stromspiegel mit dem ersten NMOS-Transistor bildet, um den Ausgangsstrom des Paares von PMOS-Transistoren zu spiegeln, und
  - $n$  PMOS-Transistoren ( $D_1-D_n$ ), die entsprechend mit den  $n$  zweiten NMOS-Transistoren ( $M_2-M_{n+1}$ ) in Reihe verbunden sind, wobei Ausgänge der  $n$  PMOS-Transistoren ( $D_1-D_n$ ) parallel verbunden sind.
2. Datentreiberschaltung nach Anspruch 1, wobei bei einem ersten PMOS-Transistor ( $Q_1$ ) des ersten Paares von PMOS-Transistoren ( $Q_1, Q_2$ ) ein Körper und eine Source verbunden sind, die wiederum mit einer ersten externen Vorspannungsschaltung (10) verbunden ist, und bei einem zweiten PMOS-Transistor ( $Q_2$ ) ein Körper und eine Source verbunden sind, die wiederum mit einer positiven Spannungsquelle ( $V_{DD}$ ) verbunden ist.
3. Datentreiberschaltung nach Anspruch 1 oder 2, wobei die Vorspannungsschaltung (10) umfasst:
- wenigstens einen NMOS-Transistor, der zwischen dem gemeinsamen Gate und dem Erdpotential in Reihe verbunden ist, und
  - eine zweite externe Vorspannung ( $V_{BIAS 2}$ ), die als eine gemeinsame Gate-Spannung der Gates der NMOS-Transistoren verwendet wird.
4. Datentreiberschaltung nach einem der Ansprüche 1 bis 3, wobei die  $n$  PMOS-Transistoren ( $D_1-D_n$ ) Ströme an die  $n$  zweiten NMOS-Transistoren ( $M_2-M_{n+1}$ ) entsprechend einem externen  $n$ -Bit Digitalsignal steuern, das als entsprechendes Gate-Signal empfangen wird, um diese als entsprechende Kanalströme weiterzuleiten.
5. Datentreiberschaltung nach Anspruch 4, wobei die entsprechenden Kanalströme so geregelt werden, dass sie eine binäre Gestalt eines gewünschten Strompegels durch eine Kombination des an den  $n$  PMOS-Transistoren ( $D_1-D_n$ ) empfangenen  $n$ -Bit Digitalsignals aufweisen.
6. Datentreiberschaltung nach einem der Ansprüche 1 bis 5, wobei die  $n$  zweiten NMOS-Transistoren ( $M_2-M_{n+1}$ ) feste Breiten und Längen aufweisen, so dass die Ströme zu den  $n$  zweiten NMOS-Transistoren ( $M_2-M_{n+1}$ ) das  $2^a$  ( $a=0, 1, 2, \dots$ )-fache des Ausgangsstroms des Paares von PMOS-Transistoren ( $Q_1, Q_2$ ) sind.

### Revendications

1. Circuit de commande de données pour un panneau d'affichage organique électroluminescent à matrice active, du type commandé par courant, comprenant :
- une pluralité de canaux de sortie de courant ( $I_{out}$ ) ; et
  - une pluralité de circuits de génération de courants de canaux sur des canaux de sortie de courant respectifs, **caractérisé en ce que** chaque circuit de génération de courant inclut :
    - une première paire de transistors PMOS ( $Q_1, Q_2$ ) ayant les mêmes largeurs et les mêmes longueurs et une borne de grille commune,
    - un premier circuit de polarisation (10) connecté à la borne de grille commune de la première paire de transistors PMOS ( $Q_1, Q_2$ ), constituant un moyen pour empêcher un flottage de la borne de grille commune,
    - un premier transistor NMOS ( $M_1$ ) pour recevoir un courant de sortie de la paire de transistors PMOS ( $Q_1, Q_2$ ),
    - $n$  ( $= 1, 2, 3, \dots$ ) seconds transistors NMOS ( $M_2 - M_{n+1}$ ), connectés à une borne de grille du premier transistor NMOS, chacun pour former un courant symétrique avec le premier transistor NMOS, pour fournir une valeur symétrique du courant de sortie de la paire de transistors PMOS, et  $n$  transistors PMOS ( $D_1 - D_n$ ) respectivement connectés aux  $n$  seconds transistors NMOS ( $M_2 - M_{n+1}$ ) en série, dans lequel les sorties des  $n$  transistors PMOS ( $D_1 - D_n$ ) sont connectées en parallèle.

## EP 1 327 972 B1

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2. Circuit de commande de données selon la revendication 1, dans lequel, parmi la première paire de transistors PMOS ( $Q_1$ ,  $Q_2$ ), un premier transistor PMOS ( $Q_1$ ) comprend un corps et une source connectés ensemble, laquelle est à son tour connectée à un premier circuit de polarisation externe (10), et un second transistor PMOS ( $Q_2$ ) comprend un corps et une source connectés ensemble, laquelle est à son tour connectée à une source de puissance à voltage positif ( $V_{DD}$ ).
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3. Circuit de commande de données selon la revendication 1 ou 2, dans lequel le circuit de polarisation (10) inclut :
- au moins un transistor NMOS connecté entre la grille commune et la terre en série, et  
une seconde polarisation externe ( $V_{BIAS2}$ ) utilisée à titre de voltage de grille commune des grilles des transistors NMOS.
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4. Circuit de commande de données selon l'une au moins des revendications 1 à 3, dans lequel les  $n$  transistors PMOS ( $D_1 - D_n$ ) commandent des courants vers les  $n$  transistors NMOS ( $M_2 - M_{n+1}$ ) en réponse à des signaux externes numériques à  $n$  bits reçus à titre de signaux de grille respectifs, pour les envoyer à titre de courants de canaux respectifs.
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5. Circuit de commande de données selon la revendication 4, dans lequel les courants de canaux respectifs sont régulés pour présenter une forme binaire avec des niveaux de courants désirés par combinaison des signaux numériques à  $n$  bits reçus aux  $n$  transistors PMOS ( $D_1 - D_n$ ).
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6. Circuit de commande de données selon l'une au moins des revendications 1 à 5, dans lequel les  $n$  seconds transistors NMOS ( $M_2 - M_{n+1}$ ) ont des largeurs et des longueurs fixées de telle façon que les courants vers les  $n$  seconds transistors NMOS ( $M_2 - M_{n+1}$ ) sont  $2^a$  ( $a = 0, 1, 2, \dots$ ) fois le courant de sortie provenant de la paire de transistors PMOS ( $Q_1, Q_2$ ).

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FIG.1  
Prior Art

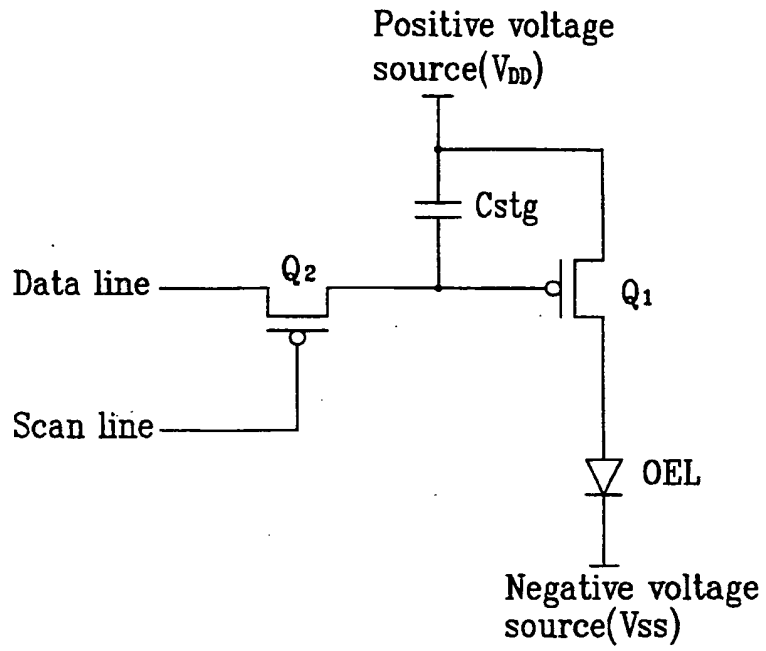


FIG.2  
Prior Art

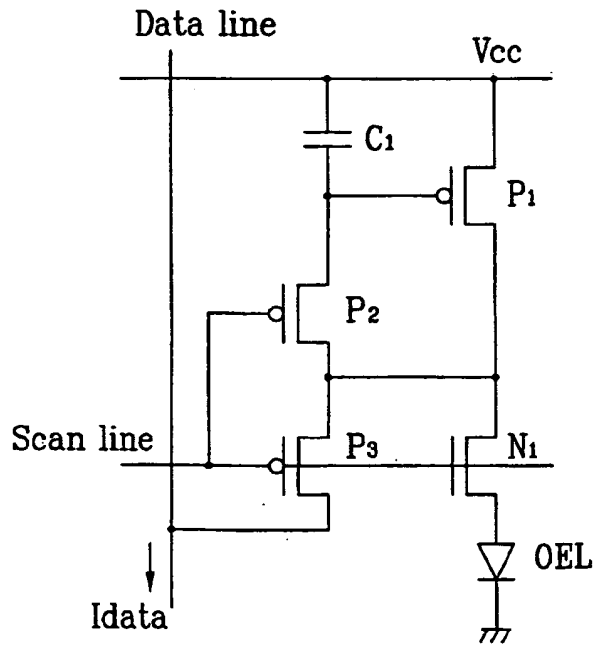


FIG. 3  
Prior Art

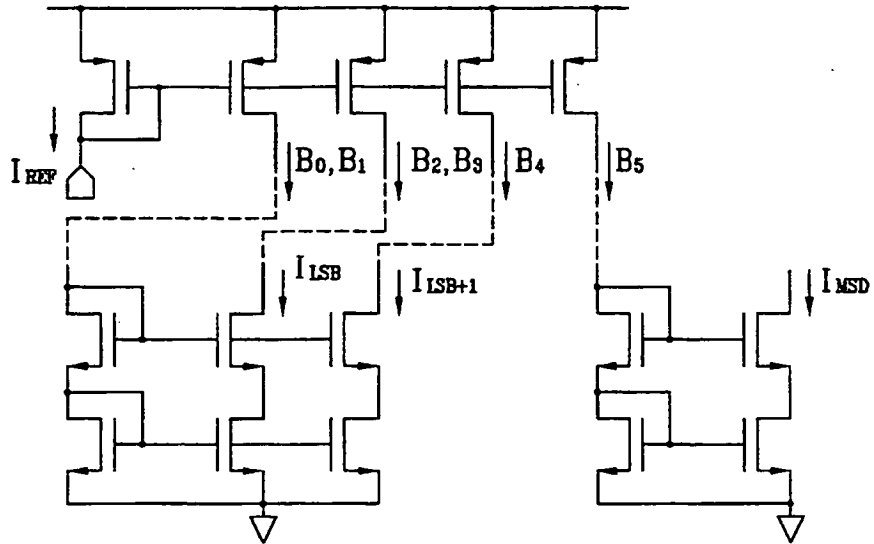


FIG. 4  
Prior Art

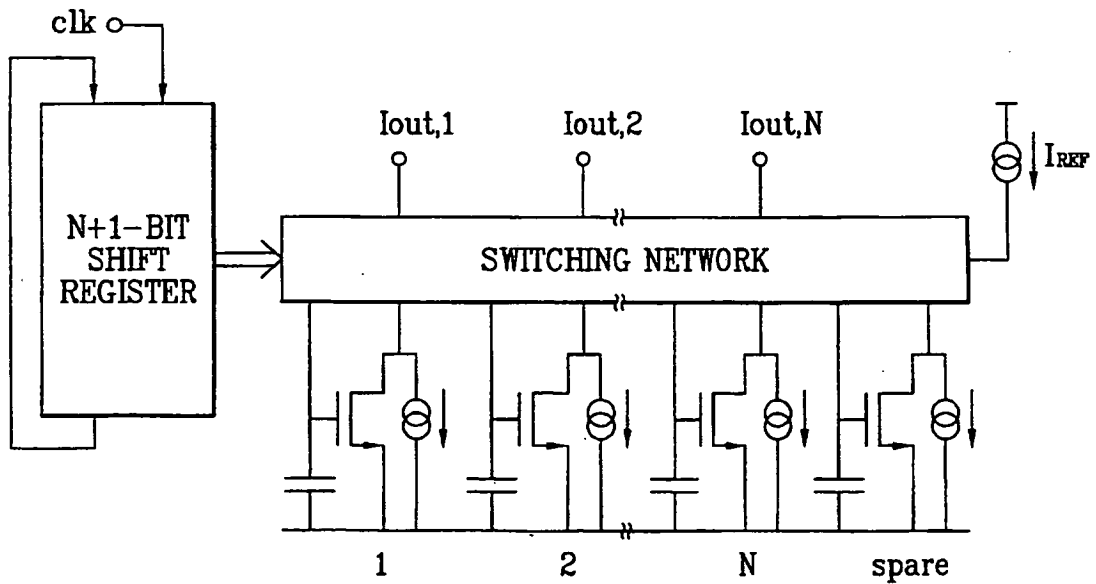


FIG. 5A

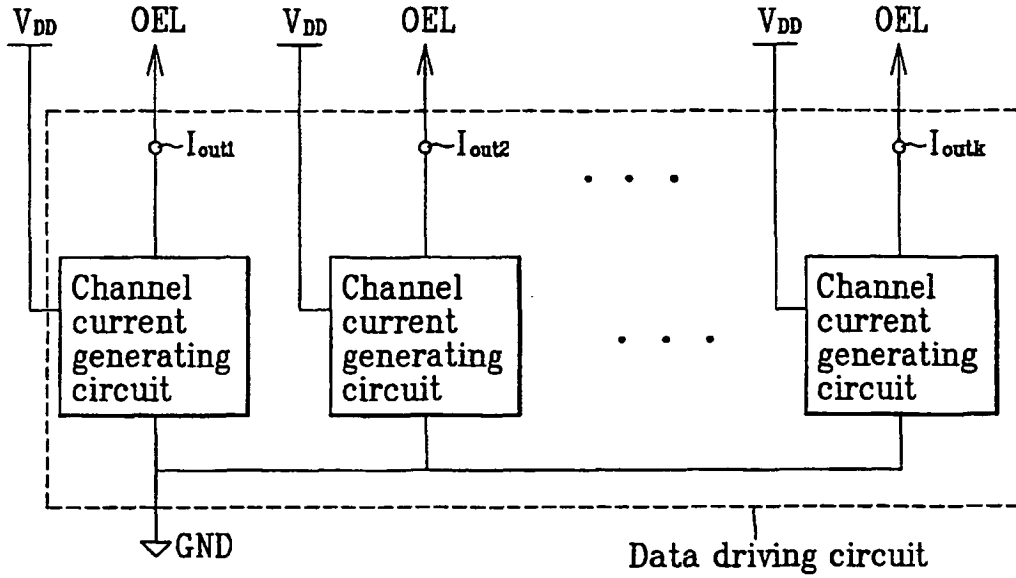
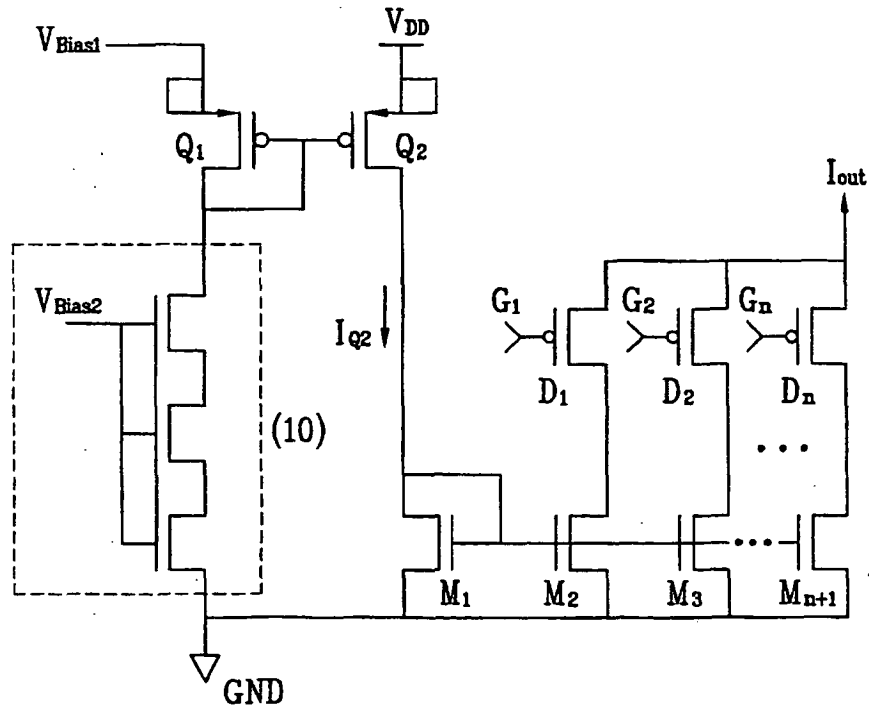


FIG. 5B



**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

- EP 1039440 A [0011]

专利名称(译)	用于电流写入型有源矩阵有机发光显示板的数据驱动电路		
公开(公告)号	<a href="#">EP1327972B1</a>	公开(公告)日	2012-03-07
申请号	EP2003000091	申请日	2003-01-08
申请(专利权)人(译)	LG电子株式会社.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KIM HAK SOO NA YOUNG SUN KWAN OH KYOUNG		
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IPC分类号	G09G3/32 H01L51/50 G09G3/20 G09G3/30 H03F3/343		
CPC分类号	G09G3/3283 G09G3/325 G09G2310/027		
优先权	1020020001175 2002-01-09 KR		
其他公开文献	EP1327972A2 EP1327972A3		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

用于电流写入型AMOEL显示面板的数据驱动电路，包括多个电流输出通道，以及在各个电流输出通道上的多个通道电流产生电路，用于最小化在电流输出通道之间发生的电流水平的差异，每个电流输出通道包括一个晶体管对，用于产生与一对晶体管的阈值电压的差的平方成比例的小偏差的电流的电流产生部分，以及用于镜像电流的电流镜部分，并且将镜像电流转发为通道的通道电流，从而最小化输出通道之间发生的电流水平的差异，并均匀地驱动AMOEL显示面板。

$$I_{out} = K(V_{bias} - V_{th})^2$$