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(54) **Wiring and Sealing Scheme for an Active Matrix Electroluminescent Display Device**

Dichtungs- und Verdrahtungsanordnung für ein elektrolumineszentes Anzeigesystem des Aktivmatrix-Typs

Arrangement de câblage et d'étanchéité pour un système d'affichage électroluminescent à matrice active

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- **PATENT ABSTRACTS OF JAPAN vol. 1999, no. 05, 31 May 1999 (1999-05-31) -& JP 11 052394 A (NEC KAGOSHIMA LTD), 26 February 1999 (1999-02-26)**
- **PATENT ABSTRACTS OF JAPAN vol. 1999, no. 04, 30 April 1999 (1999-04-30) -& JP 11 024588 A (KYOCERA CORP), 29 January 1999 (1999-01-29)**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a display device having a sealing structure. Specifically, the invention relates to an active matrix display device using a semiconductor element (an element formed of a semiconductor thin film) and to electronic equipment employing the active matrix display device as its display unit.

2. Description of the Related Art

[0002] An electro-optical device such as an EL display device having an EL element has lately been attracting attention as a flat display.

[0003] The EL element has a structure in which an EL layer is sandwiched between a pair of electrodes (an anode and a cathode). The EL layer generally takes a laminate structure. A typical example of the laminate structure is the one proposed by Tang et al. of Eastman Kodak Company, and consists of a hole transportation layer, a light emitting layer and an electron transportation layer. This structure has so high a light emission efficiency that it is employed in almost all of EL display devices that are under development at present.

[0004] Other examples of the EL layer laminate structure include a structure consisting of a hole injection layer, a hole transportation layer, a light emitting layer, and an electron transportation layer which are layered in this order on an anode, and a structure consisting of a hole injection layer, a hole transportation layer, a light emitting layer, an electron transportation layer, and an electron injection layer which are layered in this order on an anode. The light emitting layer may be doped with a fluorescent pigment or the like.

[0005] In this specification, all of the layers provided between a cathode and an anode are collectively called an EL layer. Accordingly the hole injection layer, a hole transportation layer, a light emitting layer, an electron transportation layer, an electron injection layer, etc. mentioned above are all included in the EL layer.

[0006] A given voltage is applied to the EL layer structured as above from the pair of electrodes, whereby recombination of carriers takes place in the light emitting layer to emit light. An EL element emitting light is referred to herein as EL element being driven. The EL element in this specification refers to a light emitting element composed of an anode, an EL layer, and a cathode.

[0007] The EL element in this specification refers to both a light emitting element that utilizes light emission from a singlet exciton (fluorescence) and a light emitting element that utilizes light emission from a triplet exciton (phosphorescence).

[0008] An active matrix structure is given as one of structures for EL display devices.

[0009] Fig. 9 shows an example of the structure of a pixel portion in an active matrix EL display device. In the active matrix EL display device, each pixel has thin film transistors (hereinafter referred to as TFTs). Each pixel has a switching TFT 901 whose gate electrode is connected to one of gate signal lines (G1 to Gy) for inputting a selection signal from a gate signal line driving circuit. The switching TFT 901 in each pixel has a source region and a drain region one of which is connected to one of source signal lines (S1 to Sx) for inputting a signal from a source signal line driving circuit and the other of which is connected to a gate electrode of an EL driving TFT 902 and to one of electrodes of a capacitor 903 that is provided in each pixel. The other electrode of the capacitor 903 is connected to one of power supply lines (V1 to Vx). The EL driving TFT 902 provided in each pixel has a source region and a drain region one of which is connected to one of the power supply lines (V1 to Vx) and the other of which is connected to an EL element 904 that is provided in each pixel.

[0010] When the gate signal line driving circuit selects the gate signal line G1 and inputs a signal, the switching TFT 901 that is connected to the gate signal line G1 is turned ON. If the source signal line driving circuit inputs a signal to the source signal lines Si to Sx at this point, the EL driving TFT 902 is turned ON in every pixel to which the signal is inputted. Thus a current flows into the EL element 904 from its associated power supply line (one of V1 to Vx), causing the EL element 904 to emit light. This operation is repeated for all of the gate signal lines G1 to Gy to display an image.

[0011] The EL element 904 has an anode, a cathode, and an EL layer that is provided between the anode and the cathode. If the anode of the EL element 904 is connected to the source region or the drain region of the EL driving TFT 902, the anode of the EL element 904 serves as a pixel electrode whereas the cathode thereof serves as an opposite electrode. On the other hand, if the cathode of the EL element 904 is connected to the source region or the drain region of the EL driving TFT 902, the cathode of the EL element 904 serves as the pixel electrode whereas the anode thereof serves as the opposite electrode.

[0012] The electric potential of the opposite electrode is called herein as an opposite electric potential. A power supply for giving the opposite electric potential to the opposite electrode is called an opposite power supply. The electric potential difference between the electric potential of the pixel electrode and the electric potential of the opposite electrode corresponds to an EL driving voltage, which is applied to the EL layer.

[0013] An organic EL layer has a problem of being degraded by moisture or oxygen. For that reason, it is common to seal the device after the EL layer is formed by a UV-curable resin in a nitrogen atmosphere instead of exposing the device to the air. Figs. 4A and 4B show an example of sealing the EL display device.

[0014] Fig. 4A is a top view of the EL display device.

A pixel portion 402 having EL elements, a gate signal line driving circuit 403, and a source signal line driving circuit 404 are formed on an insulating substrate 41. A sealing member 401 is formed on the insulating substrate 41 so as to surround the pixel portion 402, the gate signal line driving circuit 403 and the source signal line driving circuit 404. At this point, an opening (not shown) is formed as an inlet for injecting a filer 43 later. Then a spacer (not shown) is sprayed to bond a covering member 42. After the sealing member 401 is cured by irradiation of ultraviolet rays, the filler 43 is filled in a region enclosed with the covering member 42 and the sealing member 401. The inlet for the filler 43 is then sealed by an end-sealing material (not shown).

[0015] Fig. 4B is a sectional view taken along the line A-A' in Fig. 4A.

[0016] In order to simplify the illustration, components shown in Fig. 4B are limited to a TFT 413 constituting the gate signal line driving circuit 403, and an EL driving TFT 414 and an EL element 417 which constitute the pixel portion 402. The insulating substrate 41 is referred to as pixel substrate. The EL element 417 is composed of a pixel electrode 407, an EL layer 416, and an opposite electrode 408. The covering member 42 is set in place by the sealing member 401. The filler 43 is sealed in a space between the pixel substrate 41 and the covering member 42. A hygroscopic substance (not shown) is added to the filler 43. In this way, degradation of the EL element 417 due to moisture is avoided.

[0017] Denoted by 406 is a gate insulating film for the TFT 413 and for the EL driving TFT 414, and 415 denotes an interlayer insulating film.

[0018] A signal to be inputted to the pixel portion 402, the gate signal line driving circuit 403, and the source signal line driving circuit 404 is inputted through wiring lines 412 (412a to 412c) from an FPC (flexible printed circuit) substrate 410 (see Fig. 4A). The wiring lines 412 run between the pixel substrate 41 and the sealing member 401 to connect the FPC substrate 410 with the driving circuits. The FPC substrate 410 is connected at an external input terminal 409 to the wiring lines 412 through an anisotropic conductive film (not shown).

[0019] Any EL display device has to seal its EL element by bonding a pixel substrate to a covering member using a sealing member in order to prevent degradation of the EL element.

[0020] Unlike the pixel portion, portions where the sealing member and the driving circuits are formed do not display an image. In conventional display devices, these portions that are not used to display an image occupy a great proportion to hinder the display devices from reducing their sizes.

[0021] US 6,011,607 concerns an active matrix display with sealing material and discloses all the features in the preamble of claim 1.

[0022] WO 98143130 discloses a liquid crystal device, an electro optic device and a projection display device using the same. This disclosure describes that on the data side driving circuit section, a sealing layer is formed so that it overlaps a sampling signal input wiring pattern and an image signal sampling wiring pattern. Thus, the area outside the seating layer can be expanded to provide a larger area where a circuit can be formed.

[0023] JP 11052394 discloses a liquid crystal display device and its production. This disclosure solves the problem to prevent the occurrence of curing defect of a UV curing resin seal in the overlap part of the extraction wiring, sealing part and CF black of a TFT liquid crystal display device. The problem is solved by using a transparent electrode for the extraction wiring of the TFT substrate.

[0024] EP 0932137 discloses a display device in which parasitic capacitance associated with data lines in driving circuits is prevented using a blank layer whose primary purpose is to define areas on the substrate in which an organic semiconductor film is formed.

[0025] EP 0950917 discloses an electro optical device and an electronic apparatus wherein image signal lines extend on the substrate at both sides of a data line driving circuit and are electrically shielded from such as clock signal lines by shielding lines formed on the substrate and maintained at a constant voltage.

[0026] JP 11024588 discloses a display device that solves the problem to reduce the cost of manufacturing by quickening processing cycle and by preventing peelings of anisotropic conductive films. In this liquid crystal display device, a large number of transparent electrodes constituting a display part are made to extend on the non display area of a scanning side substrate.

SUMMARY OF THE INVENTION

[0027] The present invention has been made in view of the above and an object of the present invention is therefore to reduce the area of portions other than a pixel portion in a display device.

[0028] To attain the object, wiring lines are formed in a portion of a pixel substrate which is covered with a sealing member. The width of each of the wiring lines is set to a width that allows the sealing member on the wiring lines to be sufficiently exposed to ultraviolet rays when the sealing member is irradiated with ultraviolet rays through the wiring lines.

[0029] The area where the wiring lines around the pixel portion and the driving circuits occupy and the area where the sealing member occupies are thus reduced in the display device, whereby the display device can be made smaller.

[0030] The structure of the present invention will be described hereinbelow.

[0031] According to the present invention, there is provided a display device as set forth in claim 1.

[0032] Preferred embodiments are defined in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] In the accompanying drawings:

Figs. 1A and 1B are a top view of an EL display device according to the present invention and a sectional view thereof, respectively;
Figs. 2A and 2B are a top view of an EL display device according to the present invention and a sectional view thereof, respectively;
Figs. 3A and 3B are diagrams showing the configuration of wiring lines for a display device according to the present invention;
Figs. 4A and 4B are a top view of a conventional EL display device and a sectional view thereof, respectively;
Figs. 5A and 5B are wiring diagrams of power supply lines in a display device according to the present invention;
Figs. 6A and 6B are a top view of a liquid crystal display device and a sectional view thereof, respectively;
Figs. 7A and 7B are a top view of a liquid crystal display device and a sectional view thereof, respectively;
Figs. 8A to 8E are diagrams showing electronic equipment that employs a display device of the present invention;
Fig. 9 is a diagram showing the structure of a pixel portion in an EL display device; and
Fig. 10 is a diagram showing the structure of a pixel portion in a liquid crystal display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0034] An embodiment mode of the present invention will be described with reference to Figs. 1A and 1B.

[0035] The description given here is about an EL display device with wiring lines formed in a portion of a pixel substrate which is covered with a sealing member. In this specification, the portion of the pixel substrate which is covered with the sealing member is called a sealed region.

[0036] Fig. 1A shows a top view of an EL display device according to the present invention. On a pixel substrate 701, a pixel portion 711, a gate signal line driving circuit 702, and a source signal line driving circuit 703 are formed. A sealing member 704 is formed surrounding the pixel portion and the driving circuits, so that a covering member 705 is bonded by the sealing member. FPC substrates 706 are connected to the top face of the pixel substrate 701 by external input terminals 707. Wiring lines 708 are a plurality of wiring lines such as signal lines and power supply lines, which receive signals from the FPC substrates 706 through the external input terminals 707 to transmit the signals to the gate signal line driving circuit 702. Wiring lines 709 are a plurality of wiring lines such as signal lines and power supply lines, which receive signals from the FPC substrates 706 through the external input terminals 707 to transmit the signals to the source signal line driving circuit 703. Wiring lines 710 (wiring lines 710a and wiring lines 710b) are a plurality of wiring lines such as power supply lines, which receive signals from the FPC substrates 706 through the external input terminals 707 to transmit the signals to the pixel portion 711. The wiring lines 708 to 710 are formed in the sealed region.

[0037] Fig. 1B is a sectional view taken along the line A-A' in Fig. 1A.

[0038] In order to simplify the illustration, components shown in Fig. 1B are limited to a TFT 712 as an element constituting the gate signal line driving circuit 702, and an EL driving TFT 713 and an EL element 721 as elements that constitute the pixel portion 711. Either a source region of the EL driving TFT 713 or a drain region thereof is connected to a pixel electrode 714 of the EL element 721 in order to control a current flowing into the EL element 721. Denoted by 716 in Fig. 1B is an interlayer insulating film, 715, an EL layer, 717, an insulating film, 718, an opposite electrode, 719, a filler, and 720, a gate insulating film. The interlayer insulating film 716 is formed of an inorganic material here.

[0039] The wiring lines 708 and the wiring lines 710a and 710b are formed from the same material that is used to form source wiring lines and drain wiring lines of the TFT 712 and of the EL driving TFT 713.

[0040] Of the wiring lines 708 to 710, explanations of the wiring lines 709 are omitted because the wiring lines 709 are formed in the same way as the wiring lines 708 and the wiring lines 710a and 710b.

[0041] The sealing member 704 is often formed from a UV-curable material. A material often used for the covering member 705 is a material having a light-shielding property. Therefore the sealing member 704 cannot be exposed and cured when the sealing member 704 is irradiated with ultraviolet rays from the covering member 705 side. Thus the irradiation of ultraviolet rays has to be made from the pixel substrate 701 side through the wiring lines 708 and the wiring lines 710a and 710b to expose the sealing member 704.

[0042] Of the wiring lines 708 and the wiring lines 710a and 710b, wiring lines having a narrower width are used as video signal lines and pulse lines. On the other hand, power supply lines for supplying current to power supply lines for the pixel portion and power supply lines for the source signal line driving circuit and the gate signal line driving circuit have to be wiring lines having a width greater than the video signal lines and the pulse lines because a voltage inputted to these power supply lines is larger than a voltage inputted to the video signal lines and the pulse lines.

[0043] However, wiring lines having a large width is an obstacle when irradiating the sealing member with ultraviolet rays through the wiring lines, for the sealing member under the shade of the wiring lines is not irradiated

with a sufficient amount of ultraviolet rays. Then there is a possibility is that the sealing member is not cured satisfactorily.

[0044] The present invention therefore provides wiring lines having the following configuration. A schematic diagram of the configuration is shown in Fig. 3A. Fig. 3A corresponds to an enlarged view of a part of the sealed region in Figs. 1A and 1B, and the part is denoted by 666.

[0045] Fig. 3A focuses on one power supply line 777 out of the wiring lines (first wiring lines) 710b. The power supply line 777 is composed of wiring lines (second wiring lines) A1 to A6 connected in parallel to one another. Now, a description is given to the case where the sealing member 704 is irradiated with ultraviolet rays through the wiring line 777 configured as above.

[0046] Although the one power supply line 777 here is composed of six wiring lines A1 to A6 connected in parallel to one another, the present invention is not limited thereto. To generalize, one wiring line may be composed of n (n is a natural number equal to or greater than 2) wiring lines (second wiring lines) A1 to An connected in parallel to one another.

[0047] Fig. 3B is a sectional view taken along the line A-A' in Fig. 3A. In Figs. 3A and 3B, the same reference symbols denote the same components.

[0048] When the irradiation of ultraviolet rays is made from the pixel substrate side in Fig. 3B, portions of the sealing member on the wiring lines A1 to A6, which are denoted by 660, are shaded. However, if a width L of each wiring line is sufficiently small and a spacing S between two wiring lines is large enough, the ultraviolet rays irradiated reach the shaded portions 660. Though portions 600 right on the wiring lines are not exposed to the ultraviolet rays, the portions 600 are small enough as compared with the case where the width of a wiring line is large and, overall, the sealing member can be exposed sufficiently.

[0049] Specifically, the width L of each of the wiring lines A1 to A6 is 100 μm to 200 μm whereas the spacing S between adjacent lines in the wiring lines A1 to A6 is 50 μm to 150 μm, and L/S is within 0.7 to 1.5. If wiring lines configured as above are used, the sealing member on these wiring lines is sufficiently exposed to ultraviolet rays through the wiring lines, so that the sealing member is cured satisfactorily.

[0050] More desirably, the width L of each of the wiring lines A1 to A6 is equal to or less than 150 μm whereas the spacing L between adjacent lines in the wiring lines A1 to A6 is equal to or more than 100 μm, and L/S is 1.5 or less. In this case, the sealing member on the wiring lines can be cured enough.

[0051] Although the one power line 777 is focused out of the wiring lines 710b in Figs. 3A and 3B, a similar configuration can be applied to the other wiring lines formed in the sealed region which can cause a trouble if their width is set improperly.

[0052] Thus the wiring lines can be formed in the sealed region. This reduces the area of the regions other than the pixel portion, thereby making it possible to reduce the display device in size.

[0053] Embodiments of the present invention will be described below.

Embodiment 1

[0054] This embodiment gives a description with reference to Figs. 2A and 2B on an active matrix EL display device having a structure different from the one shown in Embodiment Mode. Components identical with those in Figs. 1A and 1B are denoted by the same reference symbols.

[0055] Fig. 2A is a top view of an EL display device according to the present invention. On a pixel substrate 701, a pixel portion 711, a gate signal line driving circuit 702, and a source signal line driving circuit 703 are formed. A sealing member 704 is formed surrounding the pixel portion and the driving circuits, so that a covering member 705 is bonded by the sealing member. FPC substrates 706 are connected to the top face of the pixel substrate 701 by external input terminals 707. Wiring lines 708 are a plurality of wiring lines such as signal lines and power supply lines, which receive signals from the FPC substrates 706 through the external input terminals 707 to transmit the signals to the gate signal line driving circuit 702. Wiring lines 709 are a plurality of wiring lines such as signal lines and power supply lines, which receive signals from the FPC substrates 706 through the external input terminals 707 to transmit the signals to the source signal line driving circuit 703. Wiring lines 710a and wiring lines 710b are a plurality of wiring lines such as power supply lines, which receive signals from the FPC substrates 706 through the external input terminals 707 to transmit the signals to the pixel portion 711. The wiring lines 708 to 710 are formed in the sealed region.

[0056] Fig. 2B is a sectional view taken along the line A-A' in Fig. 2A.

[0057] In order to simplify the illustration, components shown in Fig. 2B are limited to a TFT 712 as an element constituting the gate signal line driving circuit 702, and an EL driving TFT 713 and an EL element 721 as elements that constitute the pixel portion 711. Either a source region of the EL driving TFT 713 or a drain region thereof is connected to a pixel electrode 714 of the EL element 721 in order to control a current flowing into the EL element 721. Denoted by 716 in Fig. 2B is an interlayer insulating film, 715, an EL layer, 717, an insulating film, 718, an opposite electrode, 719, a filler, and 720, a gate insulating film. The interlayer insulating film 716 is formed of an organic material here.

[0058] The wiring lines 708 and the wiring lines 710a and 710b are formed from the same material that is used to form source wiring lines and drain wiring lines of the TFT 712 and of the EL driving TFT 713.

[0059] Of the wiring lines 708 to 710, explanations of the wiring lines 709 are omitted because the wiring lines 709 are formed in the same way as the wiring line 708

and the wiring lines 710a and 710b.

[0060] The interlayer insulating film 716 is formed of an organic material, and adhesion is poor between the organic material and the wiring lines 708 and the wiring lines 710a and 710b if they are formed directly on the organic material. Forming the wiring lines directly on the organic material also has a problem of degrading the wiring lines 708 and the wiring lines 710a and 710b, for impurities are introduced from the organic material to the material used to form the wiring lines 708 and the wiring lines 710a and 710b. For that reason, the wiring lines 708 and the wiring lines 710a and 710b have to be formed after removing the interlayer insulating film 716 formed of an organic material.

[0061] The step of removing the interlayer insulating film 716 from a part where the wiring lines 708 and the wiring lines 710a and 710b are to be formed can be carried out when source wiring lines and drain wiring lines of the TFT 712 and the pixel TFT 713 are formed and contact holes reaching source regions of the TFTs 712 and 713 are formed.

[0062] The sealing member 704 is often formed from a UV-curable material. A material often used for the covering member 705 is a material having a light-shielding property. Therefore the sealing member 704 cannot be cured when the sealing member 704 is irradiated with ultraviolet rays from the covering member side. Thus the irradiation of ultraviolet rays has to be made from the pixel substrate 701 side through the wiring lines 708 and the wiring lines 710a and 710b to cure the sealing member 704. However, if a wide wiring line is used for the wiring lines 708 and the wiring lines 710a and 710b, portions of the sealing member 704 which are shaded by the wiring lines cannot receive a sufficient amount of ultraviolet irradiation. Then the possibility is that the sealing member 704 is not cured satisfactorily.

[0063] Accordingly, this embodiment does not use a single wide wiring line for the wiring lines 708 and the wiring lines 710a and 710b. Employed instead are a plurality of wiring lines connected in parallel to one another as shown in Figs. 3A and 3B.

[0064] Specifically, the width L of each of the plural wiring lines is 100 μm to 200 μm whereas the spacing S between adjacent lines in the plural wiring lines is 50 μm to 150 μm, and the ratio of the width L of each of the plural wiring lines to the spacing S between adjacent lines in the plural wiring lines, namely, L/S is within 0.7 to 1.5. If wiring lines configured as above are used, the sealing member on these wiring lines is sufficiently exposed to ultraviolet rays through the wiring lines, so that the sealing member is cured satisfactorily.

[0065] More desirably, the width L of each of the plural wiring lines is equal to or less than 150 μm whereas the spacing S between adjacent lines in the plural wiring lines is equal to or more than 100 μm, and L/S is 1.5 or less. In this case, the sealing member on the wiring lines can be cured enough.

[0066] Thus the wiring lines can be formed in the sealed region. This reduces the area of the regions other than the pixel portion, thereby making it possible to reduce the display device in size.

Embodiment 2

[0067] This embodiment describes a wiring example of power supply lines for supplying current to power supply lines for a pixel portion of an active matrix EL display device.

[0068] Reference is again made to Fig. 1A. A current for driving the EL element 721 flows through the power supply lines of the wiring lines 710a and 710b to be inputted to the power supply lines for the pixel portion 711. The power supply lines for the pixel portion 711 are supplied with current from two sources, namely, from the power supply lines of the wiring lines 710a and from the power supply lines of the wiring lines 710b.

[0069] On the other hand, in the conventional EL display device shown in Figs. 4A and 4B, the power supply lines for the pixel portion 402 is supplied with current from one source, namely, from the power supply lines of the wiring lines 412a. Following is the reason why the pixel portion of the active matrix EL display device according to the present invention is supplied with current at two points in the pixel portion.

[0070] Figs. 5A and 5B schematically illustrate wiring examples for the power supply lines. Shown in Fig. 5A is a case where one external input terminal connected to one FPC substrate is provided to supply current to the pixel portion at one point in the pixel portion. Fig. 5B shows a case where an external input terminal is divided into two each connected to an FPC substrate (a first FPC substrate and a second FPC substrate) and provided in different places to supply current to the pixel portion at two points in the pixel portion. Shown as the power supply lines are anode lines connected to the anodes of the EL elements and cathode lines connected to the cathodes thereof. In Fig. 5A, one external input terminal 707 is provided. In Fig. 5B, on the other hand, the external input terminal 707 is divided into two so that two parts are provided in different places (near one end of a longer side of the substrate and near the other end of the longer side of the substrate) and a set of anode lines and cathode lines connects one part with the pixel portion while the other set of anode lines and cathode lines connects the other part with the pixel portion.

[0071] In Fig. 5A, the power supply lines on the far side of the input port of the anode lines and the cathode lines have an wiring resistance increased in accordance with a length R1. With the wiring resistance increased, the electric potential declines and hence the voltage applied to the EL elements by the power supply lines is lowered, thereby inviting reduction in image quality.

[0072] On the other hand, in Fig. 5B, there are an input port 1 of the anode lines and the cathode lines and an input port 2 that is provided apart from the input port 1. The power supply lines are thus receive current both from

the input port 1 and from the input port 2. This prevents voltage reduction due to increase in wiring resistance, whereby degradation of image quality can be controlled.

[0073] When the external input terminal is divided to be provided in two places as in Fig. 5B, the distance between two external input terminal parts is set to equal to or more than half the length of the longer side of the substrate on which the pixel portion is formed. This enhances the effect of controlling the degradation of image quality caused by voltage reduction due to the increase in wiring resistance.

[0074] The external input terminal may be provided in one place without dividing it if an increase in wiring resistance is ignorable, or does not matter.

[0075] This embodiment can be carried out in combination with Embodiment Mode or Embodiment 1.

[0076] A liquid crystal display device is described adopting the method of forming wiring lines in a sealed region.

[0077] The liquid crystal display device is driven by the active matrix method, for example.

[0078] First, the structure of a pixel portion in the active matrix liquid crystal display device is shown in Fig. 10. In the active matrix liquid crystal display device, each pixel has TFTs. Each pixel has a pixel TFT 1002 whose gate electrode is connected to one of gate signal lines (G1 to Gy) for receiving a selection signal from a gate signal line driving circuit. The pixel TFT 1002 in each pixel has a source region and a drain region one of which is connected to one of source signal lines (S1 to Sx) for receiving a signal from a source signal line driving circuit and the other of which is connected to one of electrodes of a capacitor storage 1001 and to one of two electrodes sandwiching a liquid crystal 1003.

[0079] When a signal is inputted to the gate signal line G1, the signal is inputted to the gate electrode of every pixel TFT 1002 that is connected to the gate signal line G1 to turn these pixel TFTs ON. If a signal is inputted from the source signal lines (S1 to Sx) to a pixel whose pixel TFT 1002 is turned ON, an electric charge is held in the capacitor storage 1001. With the electric charge held in the capacitor storage, a voltage is applied to the electrodes sandwiching the liquid crystal 1003. The applied voltage is used to control the orientation of liquid crystal molecules, thereby controlling the amount of transmitting light. This operation is repeated for all of the gate signal lines (G1 to Gy) to display an image.

[0080] Next, sealing of the liquid crystal in the active matrix liquid crystal display device will be described.

[0081] The liquid crystal display device displays an image by controlling the orientation of liquid crystal through application of voltage to the two electrodes sandwiching the liquid crystal. In order to keep the liquid crystal sandwiched between the electrodes, the liquid crystal has to be sealed in a space between two insulating substrates which respectively have electrodes and which are adhered to each other by a sealing member in a manner that makes their electrodes face each other.

[0082] Figs. 6A and 6B show in schematic diagrams the two substrates of the liquid crystal display device with the liquid crystal sealed therebetween.

[0083] Fig. 6A is a top view of the liquid crystal display device. An epoxy resin is used for a sealing member 301. An orientation film (not shown) is formed on a substrate 31 and subjected to rubbing treatment. On the substrate 31, the sealing member 301 is formed surrounding a pixel portion 302, a gate signal line driving circuit 303, and a source signal line driving circuit 304. At this point, an opening (not shown) is formed in a part of the sealing member 301 as an inlet for injecting the liquid crystal later. Then a spacer (not shown) is sprayed and the substrate 31 is bonded to another substrate 32.

[0084] The diameter of the spacer determines the distance between the substrate 31 and the substrate 32. After the distance is fixed, the substrate 31 is adhered to the substrate 32 by curing the sealing member 301 with irradiation of ultraviolet rays through the substrate 31 or the substrate 32, or heating.

[0085] When the sealing member 301 is cured by heating in order to bond the substrate 31 to the substrate 32, the heat treatment has to be performed while pressurizing. This method causes the substrate 31 and the substrate 32 to thermally expand and the displacement in bonding the substrates is a serious problem. Thermal curing also takes a longer time. Therefore, the sealing member is often cured by irradiation of ultraviolet rays rather than thermally cured.

[0086] Thereafter, a liquid crystal 33 is injected from the liquid crystal inlet, which is closed by an end-sealing material (not shown) so that the liquid crystal 33 does not leak to the exterior thereof. The end-sealing material is a UV-curable material, not a thermally curable material. This is because the liquid crystal 33 is degraded if the device is heated after the liquid crystal 33 is injected.

[0087] The sealing member 301 and the end-sealing material also serve to block the passage of substances that contaminate the liquid crystal, such as moisture containing ions.

[0088] Described next are wiring lines for transmitting signals to be inputted respectively to the source signal line driving circuit and the gate signal line driving circuit.

[0089] Video signals or other signals from the external are inputted to the gate signal line driving circuit 303 and the source signal line driving circuit 304 to constitute signals that are to be inputted to the pixel portion 302. The signals to be inputted to the gate signal line driving circuit 303 and the source signal line driving circuit 304 from the external are inputted by an FPC substrate 310 bonded to an external input terminal 309 that is placed on the pixel substrate 31. The FPC substrate 310 is connected at the external input terminal 309 through an anisotropic conductive film (not shown) to wiring lines 312 that are formed on the pixel substrate. The wiring lines 312 (312a, 312b, and 312c) run in the sealing member 301 to be connected to the gate signal line driving circuit 303 and the source signal line driving circuit 304.

[0090] The wiring lines 312a are wiring lines that receive signals from the FPC substrate 310 through the external input terminal 309 to transmit the signals to the gate signal line driving circuit 303. The wiring lines 312b are wiring lines that receive signals from the FPC substrate 310 through the external input terminal 309 to transmit the signals to the source signal line driving circuit 304. The wiring lines 312a and 312b are formed in a part of the pixel substrate 31 which is covered by the sealing member 301 (the sealed region).

[0091] Fig. 6B is a sectional view taken along the line B-B' in Fig. 6A. The same components are denoted by the same reference symbols in Figs. 6A and 6B.

[0092] In order to simplify the illustration, components shown in Fig. 6B are limited to a TFT 114 constituting the gate signal line driving circuit 303, and a pixel TFT 314 constituting the pixel portion 302. The substrate 31 on which the TFTs constituting the pixel portion and the driving circuits are formed is referred to as pixel substrate. An electrode 307 set on the pixel substrate is referred to as pixel electrode. The other substrate, 32, is called an opposite substrate. An electrode 308 set on the opposite substrate side is called an opposite electrode. The voltage applied to the pixel electrode 307 and the opposite electrode 308 is controlled to display an image.

[0093] Denoted by 306 in Fig. 6B is a gate insulating film of each of the TFT 114 and the pixel TFT 314. Reference symbol 315 denotes an interlayer insulating film and 112 denotes a light-shielding layer. The orientation film is not shown in Fig. 6B.

[0094] The pixel TFT 314 has a source region and a drain region one of which is connected to the pixel electrode 307 to control the voltage applied to the pixel electrode 307. The interlayer insulating film 315 is formed of an inorganic material here.

[0095] The wiring lines 312 are formed from the same material that is used to form source wiring lines and drain wiring lines of the TFT 114 and of the pixel TFT 314.

[0096] Assuming that the sealing member 301 is formed from a UV-curable material, the sealing member 301 cannot be cured when the sealing member 301 is irradiated with ultraviolet rays from the opposite substrate 32 side because of the light-shielding layer 112. Thus the irradiation of ultraviolet rays has to be made from the pixel substrate 31 side through the wiring lines 312a to cure the sealing member 301. However, if a wide wiring line is used for the wiring lines 312a, portions of the sealing member 301 which are shaded by the wiring lines cannot receive a sufficient amount of ultraviolet irradiation. Then the possibility is that the sealing member 301 is not cured satisfactorily.

[0097] Accordingly, this display does not use a single wide wiring line for the wiring lines 312a. Employed instead are a plurality of wiring lines connected in parallel to one another as shown in Figs. 3A and 3B.

[0098] Specifically, the width L of each of the plural wiring lines is 100 μm to 200 μm whereas the spacing S between adjacent lines in the plural wiring lines is 50 μm to 150 μm, and the ratio of the width L of each of the plural wiring lines to the spacing S between adjacent lines in the plural wiring lines, namely, L/S, is within 0.7 to 1.5. If wiring lines configured as above are used, the sealing member on these wiring lines is sufficiently exposed to ultraviolet rays through the wiring lines, so that the sealing member is cured satisfactorily.

[0099] More desirably, the width L of each of the plural wiring lines is equal to or less than 150 μm whereas the spacing S between adjacent lines in the plural wiring lines is equal to or more than 100 μm, and L/S is 1.5 or less. In this case, the sealing member on the wiring lines can be cured enough.

[0100] If the light-shielding layer 112 is formed on the pixel substrate 31 side, the irradiation of ultraviolet rays has to be made from the opposite substrate 32 side to cure the sealing member 301. In this case, the wiring lines 312a do not block the ultraviolet rays irradiated, and hence a wide wiring line may be used as 312a.

[0101] Thus the wiring lines can be formed in the sealed region. This reduces the area of the regions other than the pixel portion, thereby making it possible to reduce the display device in size.

[0102] A second display device is illustrated in Figs. 7A and 7B. This second display device has a structure different from the one described in the first LCD device. Components in Figs. 7A and 7B that are identical with those in Figs. 6A and 6B are denoted by the same reference symbols.

[0103] Fig. 7A is a top view of the second liquid crystal display device. On a pixel substrate 31, a pixel portion 302, a gate signal line driving circuit 303, and a source signal line driving circuit 304 are formed. A sealing member 301 is formed surrounding the pixel portion and the driving circuits, so that an opposite substrate 32 is bonded to the substrate 31 and a liquid crystal 33 is sealed therebetween. An FPC substrate 310 is connected to the top face of the pixel substrate 31 by an external input terminal 309. Wiring lines 312a are wiring lines that receive signals from the FPC substrate 310 through the external input terminal 309 to transmit the signals to the gate signal line driving circuit 303. Wiring lines 312b are wiring lines that receive signals from the FPC substrate 310 through the external input terminal 309 to transmit the signals to the source signal line driving circuit 304. The wiring lines 312a and 312b are formed in the sealed region.

[0104] Fig. 7B is a sectional view taken along the line B-B' in Fig. 7A. The same components are denoted by the same reference symbols in Figs. 7A and 7B.

[0105] In order to simplify the illustration, components shown in Fig. 7B are limited to a TFT 114 as an element constituting the gate signal line driving circuit 303, and a pixel TFT 314 as an element constituting the pixel portion 302. The pixel TFT 314 has a source region and a drain region one of which is connected to a pixel electrode 307 to control the voltage applied to the pixel electrode 307.

[0106] The wiring lines 312 are formed from the same

material that is used to form source wiring lines and drain wiring lines of the TFT 114 and of the pixel TFT 314. An interlayer insulating film 315 is formed of an organic material here.

[0107] The interlayer insulating film 315 is formed of an organic material, and adhesion is poor between the organic material and the wiring lines 312 if they are formed directly on the organic material. Forming the wiring lines directly on the organic material also has a problem of degrading the wiring lines 312, for impurities are introduced from the organic material to the material used to form the wiring lines 312. For that reason, the wiring lines 312 have to be formed after removing the interlayer insulating film 315 formed of an organic material.

[0108] The step of removing the interlayer insulating film 315 from a part where the wiring lines 312a are to be formed can be carried out when the source wiring lines and the drain wiring lines of the TFr 114 and the pixel TFT 314 are formed and contact holes reaching source regions or drain regions of the TFTs 114 and 314 are formed.

[0109] Assuming that the sealing member 301 is formed from a UV-curable material, the sealing member 301 cannot be cured when the sealing member 301 is irradiated with ultraviolet rays from the opposite substrate 32 side because of the light-shielding layer 112. Thus the irradiation of ultraviolet rays has to be made from the pixel substrate 31 side through the wiring lines 312a to cure the sealing member 301. However, if a wide wiring line is used for the wiring lines 312a, portions of the sealing member 301 which are shaded by the wiring lines cannot receive a sufficient amount of ultraviolet irradiation. Then the possibility is that the sealing member 301 is not cured satisfactorily.

[0110] Accordingly, this display does not use a single wide wiring line for the wiring lines 312a. Employed instead are a plurality of wiring lines connected in parallel to one another as shown in Figs. 3A and 3B.

[0111] Specifically, the width L of each of the plural wiring lines is 100 μm to 200 μm whereas the spacing S between adjacent lines in the plural wiring lines is 50 μm to 150 μm, and the ratio of the width L of each of the plural wiring lines to the spacing S between adjacent lines in the plural wiring lines, namely, L/S, is within 0.7 to 1.5. If wiring lines configured as above are used, the sealing member on these wiring lines is sufficiently exposed to ultraviolet rays through the wiring lines, so that the sealing member is cured satisfactorily.

[0112] More desirably, the width L of each of the plural wiring lines is equal to or less than 150 μm whereas the spacing S between adjacent lines in the plural wiring lines is equal to or more than 100 μm, and L/S is 1.5 or less. In this case, the sealing member on the wiring lines can be cured enough.

[0113] If the light-shielding layer 112 is formed on the pixel substrate 31 side, the irradiation of ultraviolet rays has to be made from the opposite substrate 32 side to cure the sealing member 301. In this case, the wiring lines 312a do not block the ultraviolet rays irradiated, and hence a wide wiring line may be used as 312a.

[0114] Thus the wiring lines can be formed in the sealed region. This reduces the area of the regions other than the pixel portion, thereby making it possible to reduce the display device in size.

Embodiment 3

[0115] The electronic equipments, which incorporate the electronic display device manufactured by applying the present invention as the display medium, are explained below.

[0116] Such electronic equipments include a video camera, a digital camera, a head mounted display (goggle type display), a game machine, a car navigation system, a personal computer, a portable information terminal (a mobile computer, a portable telephone, an electronic book and the like) and the like. Examples of those are shown in Fig. 8.

[0117] Fig. 8A shows a personal computer, which contains a main body 2001, a casing 2002, a display portion 2003, a keyboard 2004 and the like. The display device of the present invention can be used in the display portion 2003 of the personal computer.

[0118] Fig. 8B shows a video camera, which contains a main body 2101, a display portion 2102, a sound input portion 2103, operation switches 2104, a battery 2105, an image receiving portion 2106 and the like. The display device of the present invention can be used in the display portion 2102 of the video camera.

[0119] Fig. 8C shows a portion (right side) of a head mounted type display device, which contains a main body 2301, a signal cable 2302, a head fixing band 2303, a screen monitor 2304, an optical system 2305, a display portion 2306 and the like. The display device of the present invention can be used in the display portion 2306 of the head mounted type display device,

[0120] Fig. 8D shows an image playback device equipped with a recording medium (specifically, a DVD playback device), which contains a main body 2401, a recording medium (such as a CD, an LD or a DVD) 2402, operation switches 2403, a display portion (a) 2404, a display portion (b) 2405 and the like. The display portion (a) is mainly used for displaying image information. The display portion (b) is mainly used for displaying character Information. The display device of the present invention can be used in the display portions (a) and (b) of the image playback device equipped with the recording medium. Note that the present invention can be applied to devices such as a CD playback device and a game machine as the image playback device equipped with the recording medium.

[0121] Fig. 8E shows a mobile computer, which contains a main body 2501, a camera portion 2502, an image receiving portion 2503, operation switches 2504, a display portion 2505 and the like. The display device of the present invention can be used in the display portion 2505

of the mobile computer.

[0122] The application range for the display as claimed is extremely wide, as shown above, and it is possible to apply the display as claimed to electronic equipments in all fields. Further, the electronic equipments of this embodiment can be realized using the constitution in which Embodiments 1 to 2 are freely combined.

[0123] In display devices such as EL display devices and liquid crystal display devices, portions that do not display an image, including the periphery of driving circuits where wiring lines are formed and a portion where the sealing member is formed, take up a large area to hinder the display devices from reducing their sizes.

[0124] With the structures described above, the present invention is capable of forming wiring lines in the portion where the sealing member is formed instead of the periphery of the driving circuits. Thus the invention can provide a small-sized display device.

Claims

1. A display device comprising:

pixels that each have an electroluminescent element (721) and are arranged over a substrate (701);
a driver circuit (702, 703) for Inputting a signal to said pixels and arranged over said substrate (701):
a covering member (705) having a light-shielding property; and
a seating member (704) comprising an uttra-viotet-curable material, said sealing member (704) surrounding said pixels and said driver circuit (702,703),
wherein:

said substrate (701) is adhered to said covering member (705) with said sealing member (704) sandwiched therebetween to seal said electroluminescent elements (721),
characterized in that
first wiring lines (708, 709) for inputting an external signal to said driver circuit (702, 703) are arranged to run along at least one side of said sealing member (704) and between said sealing member (704) and said substrate (701),
said first wiring lines (708, 709) each comprise further wiring lines (777, A1,...A6) connected in parallel to one another;
the width of each of said further wiring lines (777, A1,...A6) is given as L, the space between adjacent ones of the further wiring lines (777, A1,...A6) is given as S, and the ratio of L to S is within 0.7 to 1.5,
wherein the width of each of said plural further wiring lines (777, A1,...6) connected in parallel to one another, given as L, is 100μm to 200μm, and
wherein the space between adjacent lines in said plural further wiring lines (777, A1, ...A6) connected in parallel to one another, given as S, is 50μm to 150μm.

2. A display device according to claim 1, wherein said sealing member (704) is in contact with an inorganic layer (716) arranged over said substrate (701).

3. A display device according to claim 1, wherein said first wiring lines (708, 709) are made from the same material that is used for source wiring lines and drain wiring lines of Thin Film Transistors (712, 713) for said pixels and for said driving circuit (702, 703).

4. A video camera comprising a display device according to any one of claims 1 to 3.

Patentansprüche

1. Anzeigevorrichtung, die umfasst:

Pixel, die je ein elektrolumineszentes Element (721) haben und über einem Substrat (701) angeordnet sind;
eine Treiberschaltung (702, 703) zum Eingeben eines Signals zu den Pixeln, die über dem Substrat (701) angeordnet ist;
einen Deckteil (705), der die Eigenschaft hat, Licht zu blockieren; und
einen Dichtungsteil (704), der ein UV-härtendes Material umfasst und der die Pixel und die Treiberschaltung (702, 703) umgibt,
wobei:

das Substrat (701) an das Deckteil (705) geklebt ist, mit dem Dichtungsteil (704) dazwischen, um die elektrolumineszenten Elemente (721) abzudichten,
dadurch gekennzeichnet, dass
erste Verdrahtungsleitungen (708, 709) zum Eingeben eines externen Signals zu der Treiberschaltung (702, 703) so angeordnet sind, dass sie entlang zumindest einer Seite des Dichtungsteils (704) und zwischen dem Dichtungsteil (704) und dem Substrat (701) laufen,
die ersten Verdrahtungsleitungen (708, 709) jeweils zusätzliche Verdrahtungsleitungen (777, A1,...A6) umfassen, die parallel zueinander angeschlossen sind;
die Breite jedes der zusätzlichen Verdrahtungsleitungen (777, A1,...A6) als L vorgegeben ist, der Abstand zwischen angren-

zenden Leitungen in den zusätzlichen Verdrahtungsleitungen (777, A1,...A6) als S vorgegeben ist, und das Verhältnis von L zu S im Bereich 0,7 bis 1,5 liegt,
wobei die als L vorgegebene Breite jeder der Vielzahl von zusätzlichen Verdrahtungsleitungen (777, A1,...A6), die parallel zueinander angeschlossen sind, 100 μm bis 200 μm beträgt, und
wobei der als S vorgegebene Abstand zwischen angrenzenden Leitungen der Vielzahl von zusätzlichen Verdrahtungsleitungen (777, A1,...A6), die parallel zueinander angeschlossen sind, 50 μm bis 150 μm beträgt.

2. Anzeigevorrichtung nach Anspruch 1, wobei der Dichtungsteil (704) mit einer anorganischen Schicht (716), die über dem Substrat (701) angeordnet ist, in Kontakt ist.

3. Anzeigevorrichtung nach Anspruch 1, wobei die ersten Verdrahtungsleitungen (708, 709) aus dem gleichen Material wie Source-Verdrahtungsleitungen und Drain-Verdrahtungsleitungen der Dünnschichttransistoren (712, 713) für die Pixel und für die Treiberschaltung (702, 703) ausgebildet sind.

4. Videokamera, die eine Anzeigevorrichtung nach einem der Ansprüche 1 bis 3 umfasst.

Revendications

1. Dispositif d'affichage comprenant :

des pixels comportant chacun un élément électroluminescent (721) et agencés au-dessus d'un substrat (701) ;
un circuit de commande (702, 703) pour entrer un signal dans lesdits pixels et agencé au-dessus dudit substrat (701) ;
un élément de recouvrement (705) ayant une propriété de masquage de la lumière ; et
un élément d'étanchéité (704) comprenant un matériau pouvant être traité par ultraviolet, ledit élément d'étanchéité (704) entourant lesdits pixels et ledit circuit de commande (702, 703),
dans lequel on colle ledit substrat (701) sur ledit élément de recouvrement (705) avec ledit élément d'étanchéité (704) intercalé entre eux pour sceller lesdits éléments électroluminescents (721),
caractérisé en ce que
des premières lignes de câblage (708, 709) pour entrer un signal extérieur dans ledit circuit de commande (702, 703) sont agencées de manière à s'étendre au moins le long d'une face dudit élément d'étanchéité (704) et entre ledit élément d'étanchéité (704) et ledit substrat (701),
lesdites premières lignes de câblage (708, 709) comprennent chacune d'autres lignes de câblage (777, A1, ..., A6) connectées en parallèle entre elles ;
la largeur de chacune desdites autres lignes de câblage (777, A1, ..., A6) est donnée par L, l'espace entre des lignes adjacentes parmi les autres lignes de câblage (777, A1, ..., A6) est donné par S et le rapport entre L et S est compris entre 0,7 et 1,5,
dans lequel la largeur de chaque ligne desdites plusieurs autres lignes de câblage (777, A1, ..., A6) connectées en parallèle entre elles, donnée par L, est de 100 μm à 200 μm, et
dans lequel l'espace entre des lignes adjacentes parmi lesdites plusieurs autres lignes de câblage (777, A1, ..., A6) connectées en parallèles entre elles, donnée par S, est de 50 μm à 150 μm.

2. Dispositif d'affichage selon la revendication 1, dans lequel ledit élément d'étanchéité (704) est en contact avec une couche inorganique (716) agencée au-dessus dudit substrat (701).

3. Dispositif d'affichage selon la revendication 1, dans lequel lesdites premières lignes de câblage (708, 709) sont faites du même matériau que celui qui est utilisé pour les lignes de câblage de source et les lignes de câblage de drain de transistors à couches minces (712, 713) pour lesdits pixels et pour ledit circuit de commande (702, 703).

4. Caméra vidéo comprenant un dispositif d'affichage selon l'une quelconque des revendications 1 à 3.

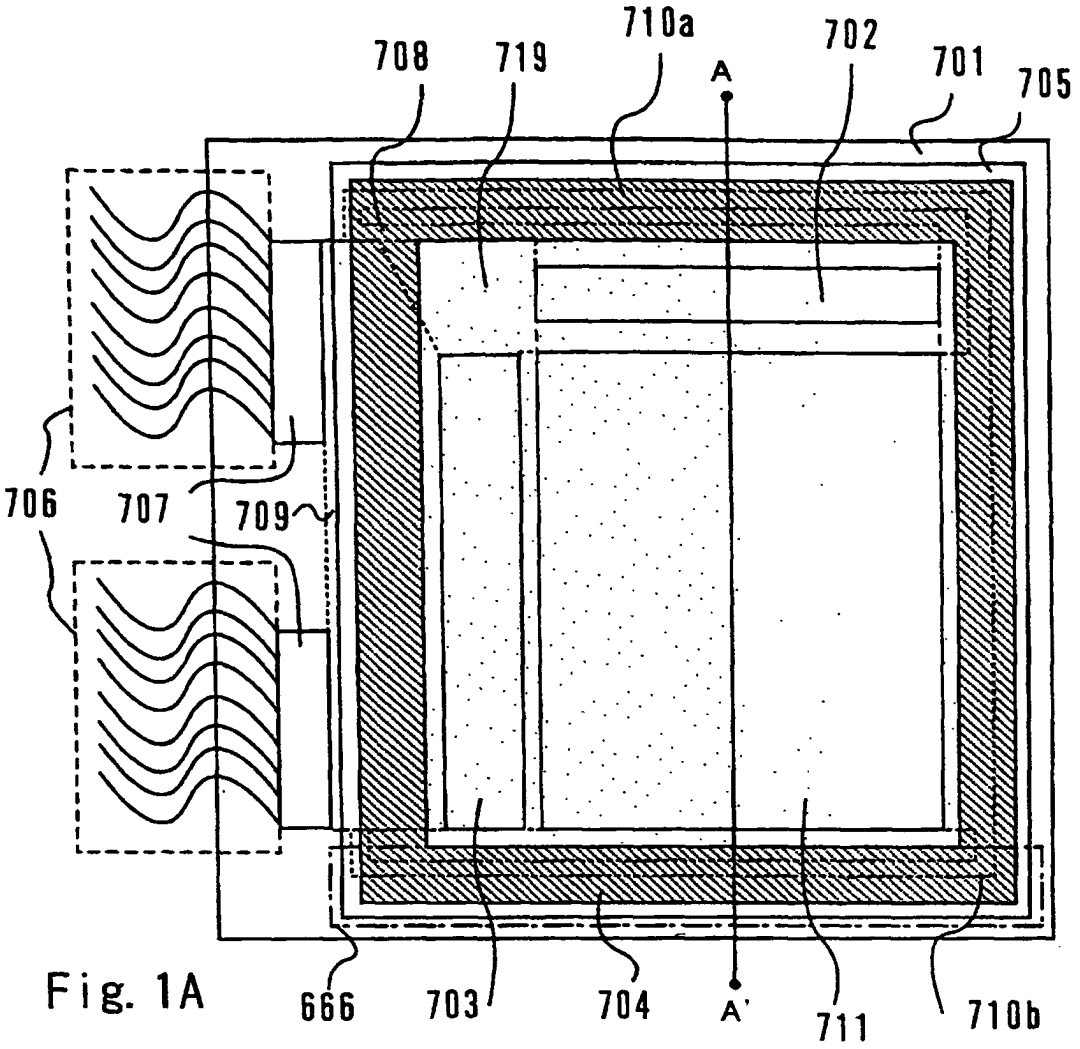

710a
708
719
A
702
701
705
706
707
709
666
703
704
A'
711
710b

Fig. 1A

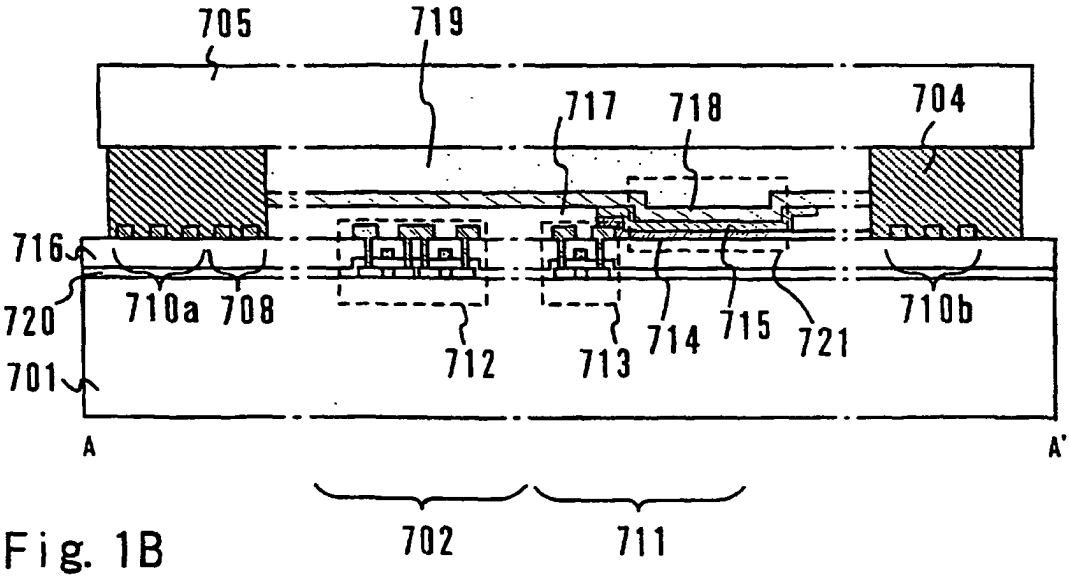

705
719
717
718
704
716
720
710a
708
712
713
714
715
721
710b
701
A
A'
702
711

Fig. 1B

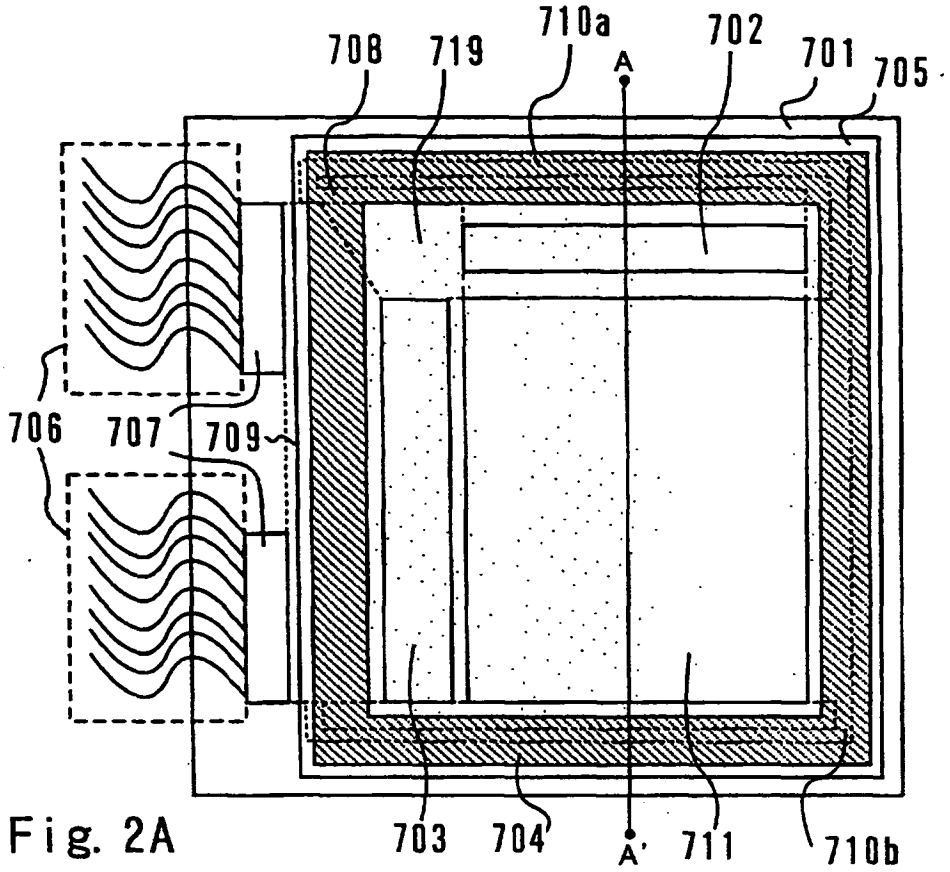

708
719
710a
A
702
701
705
706
707
709
703
704
A'
711
710b

Fig. 2A

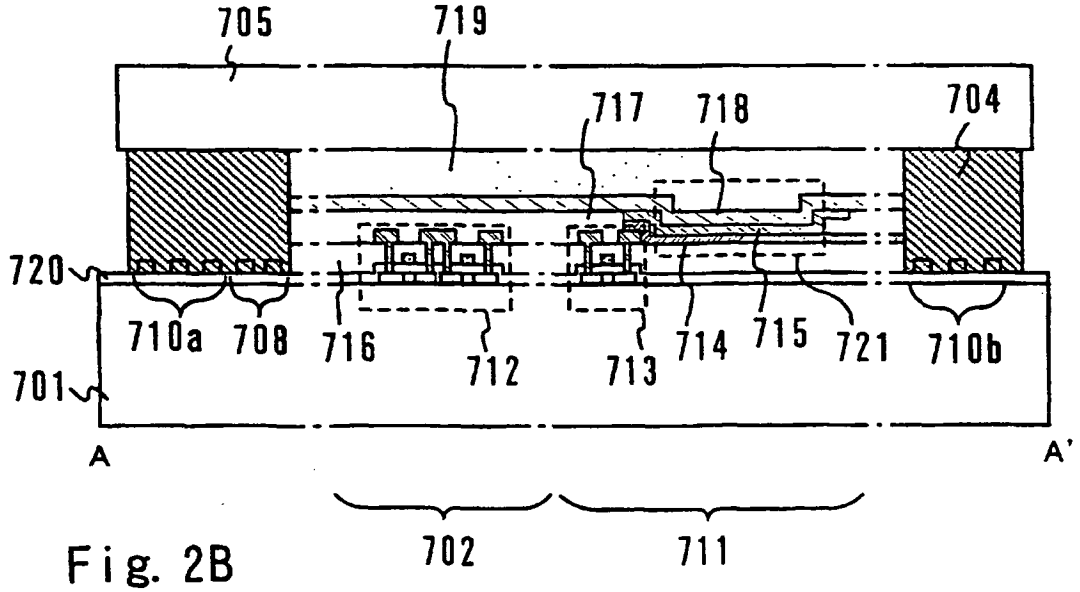

705
719
717
718
704
720
710a
708
716
712
713
714
715
721
710b
701
A
A'
702
711

Fig. 2B

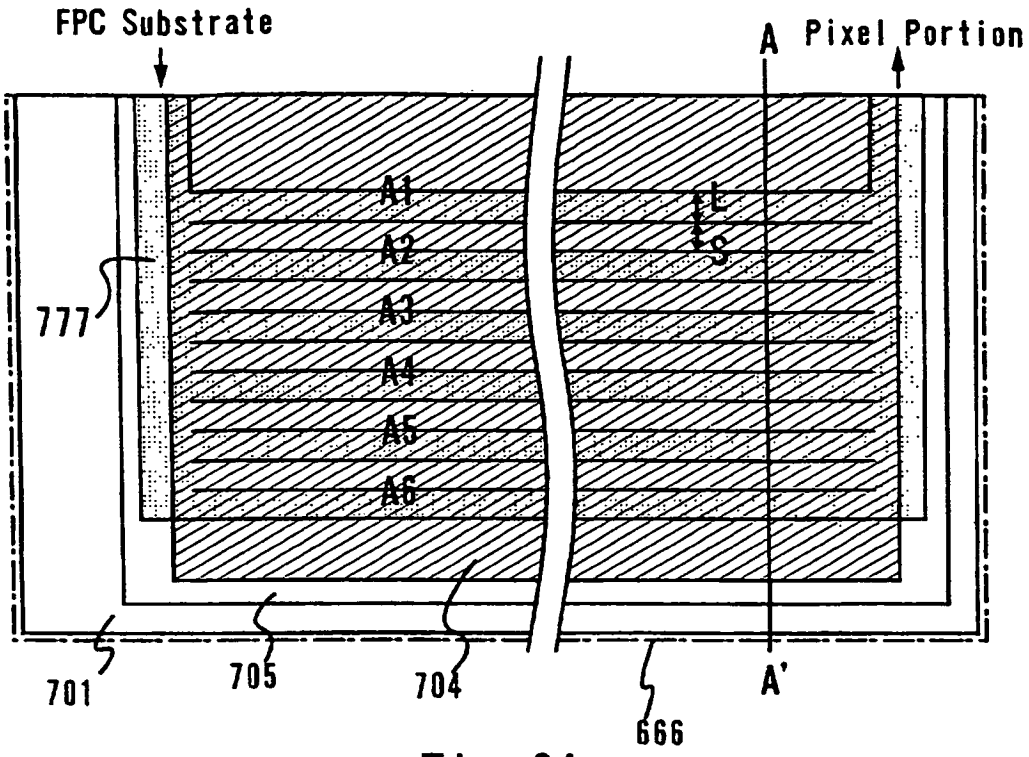

FPC Substrate
A Pixel Portion
A1
A2
A3
A4
A5
A6
L
S
777
701
705
704
666
A'

Fig. 3A

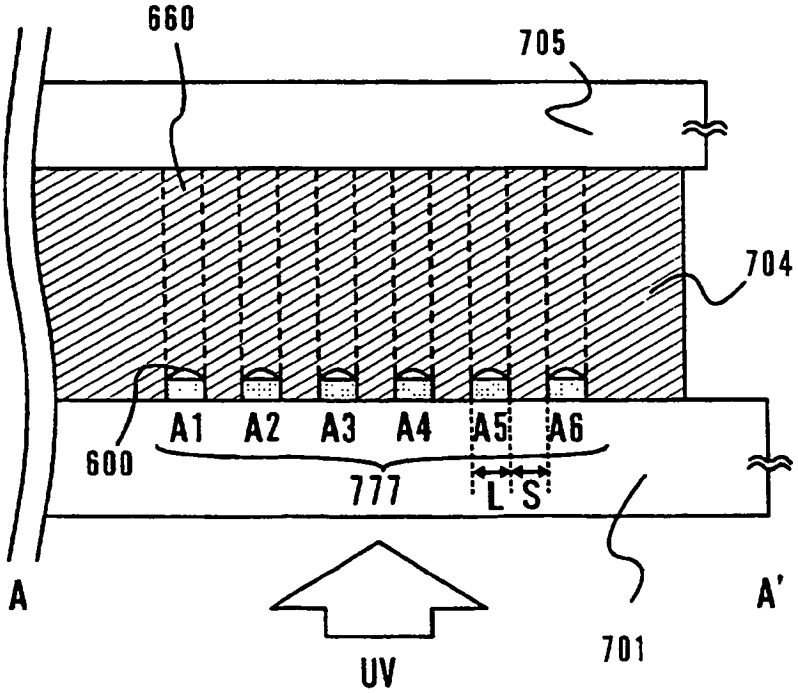

660
705
704
A1
A2
A3
A4
A5
A6
600
777
L
S
A
A'
UV
701

Fig. 3B

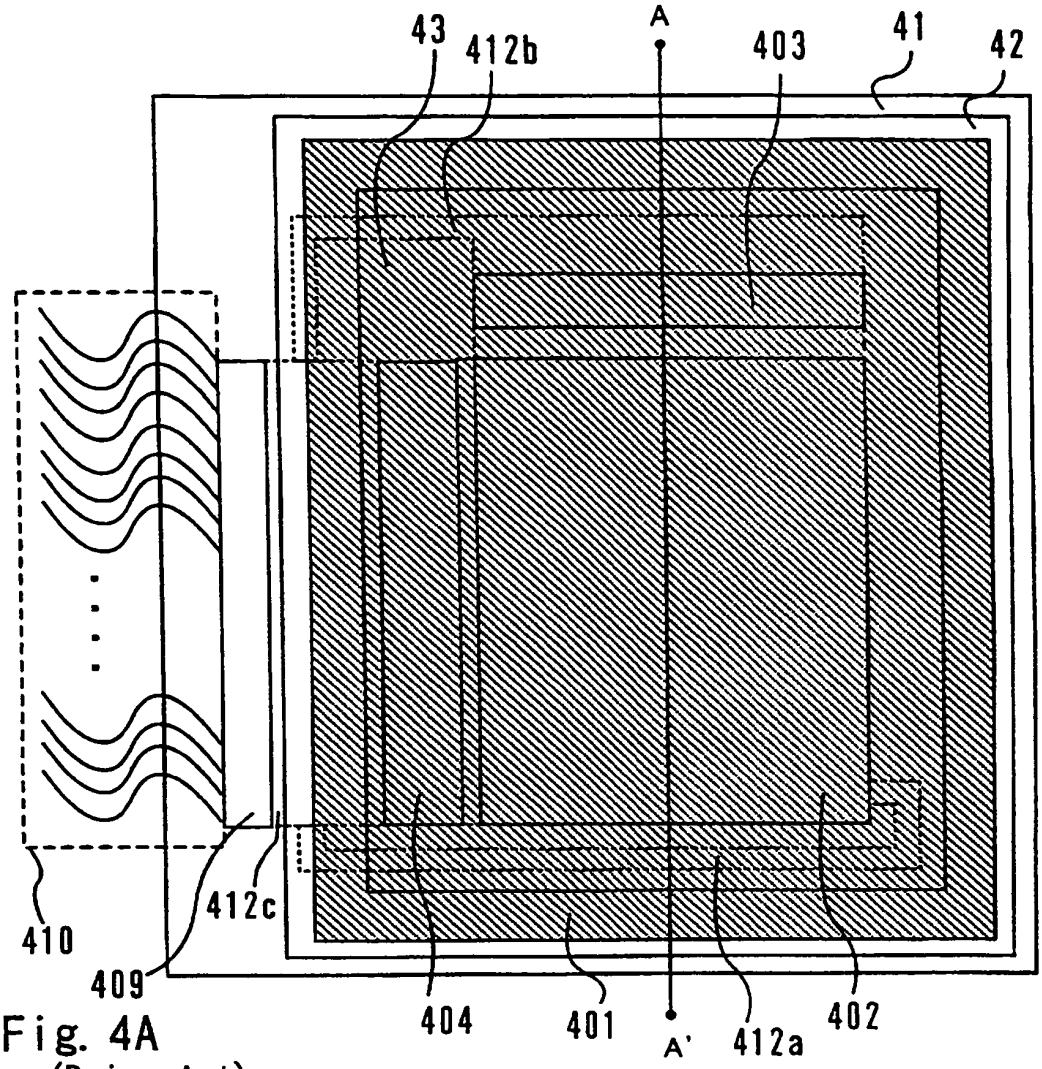


Fig. 4A
(Prior Art)

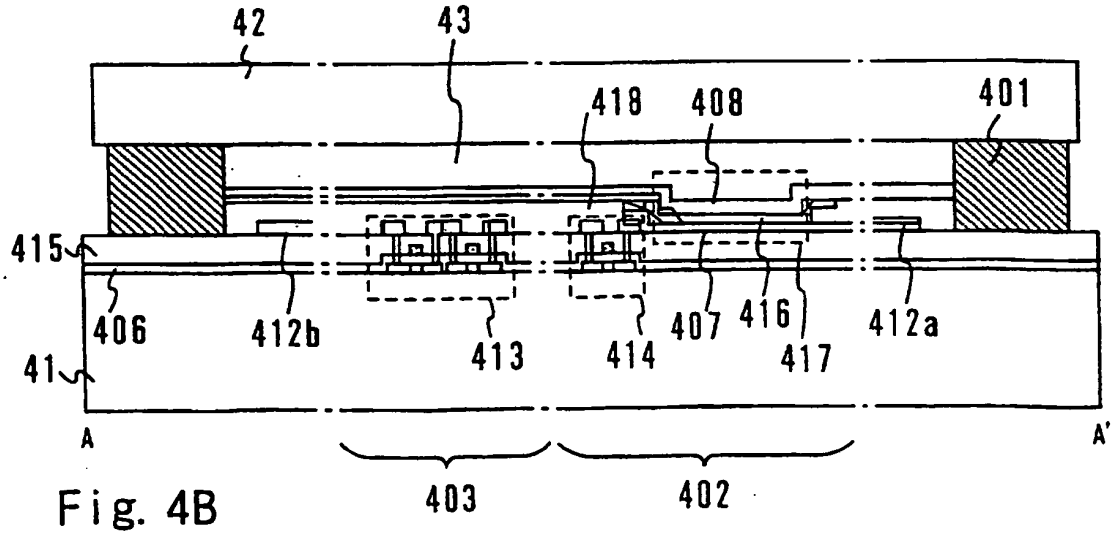


Fig. 4B
(Prior Art)

Fig. 5A

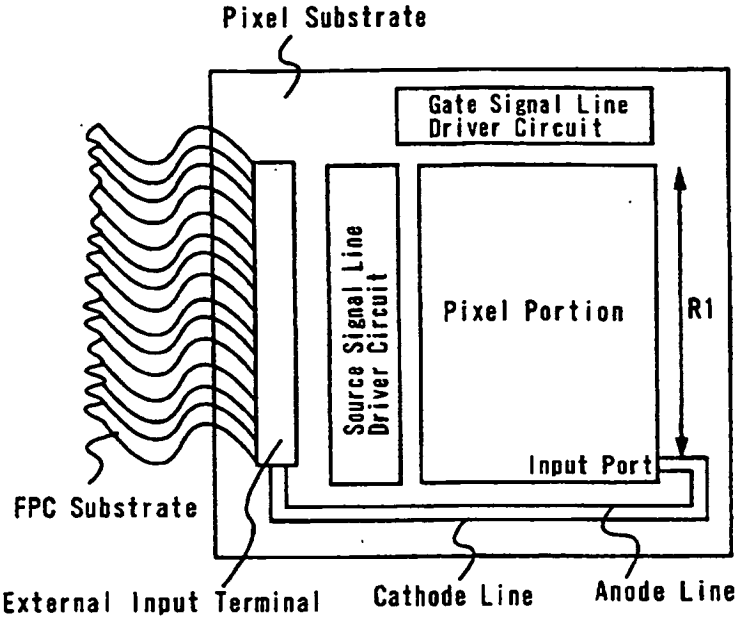
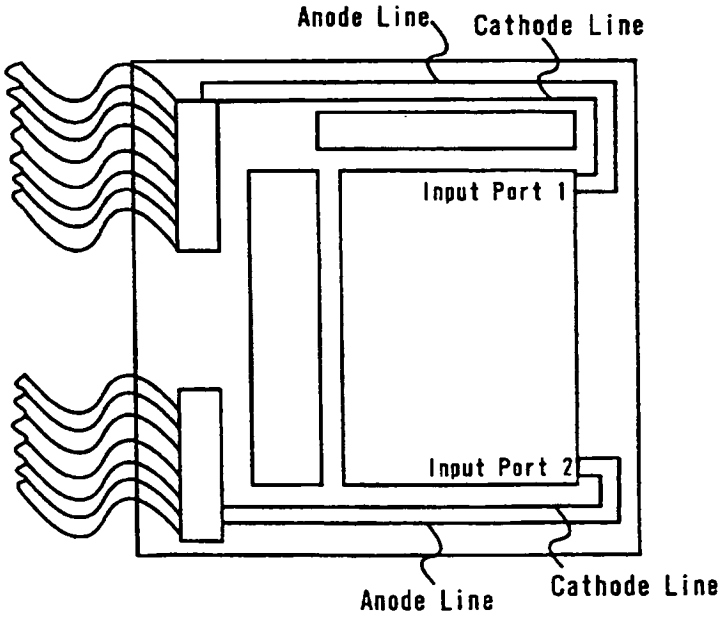

Pixel Substrate
Gate Signal Line Driver Circuit
Source Signal Line Driver Circuit
Pixel Portion
R1
Input Port
FPC Substrate
External Input Terminal
Cathode Line
Anode Line

Fig. 5B


Anode Line
Cathode Line
Input Port 1
Input Port 2
Anode Line
Cathode Line

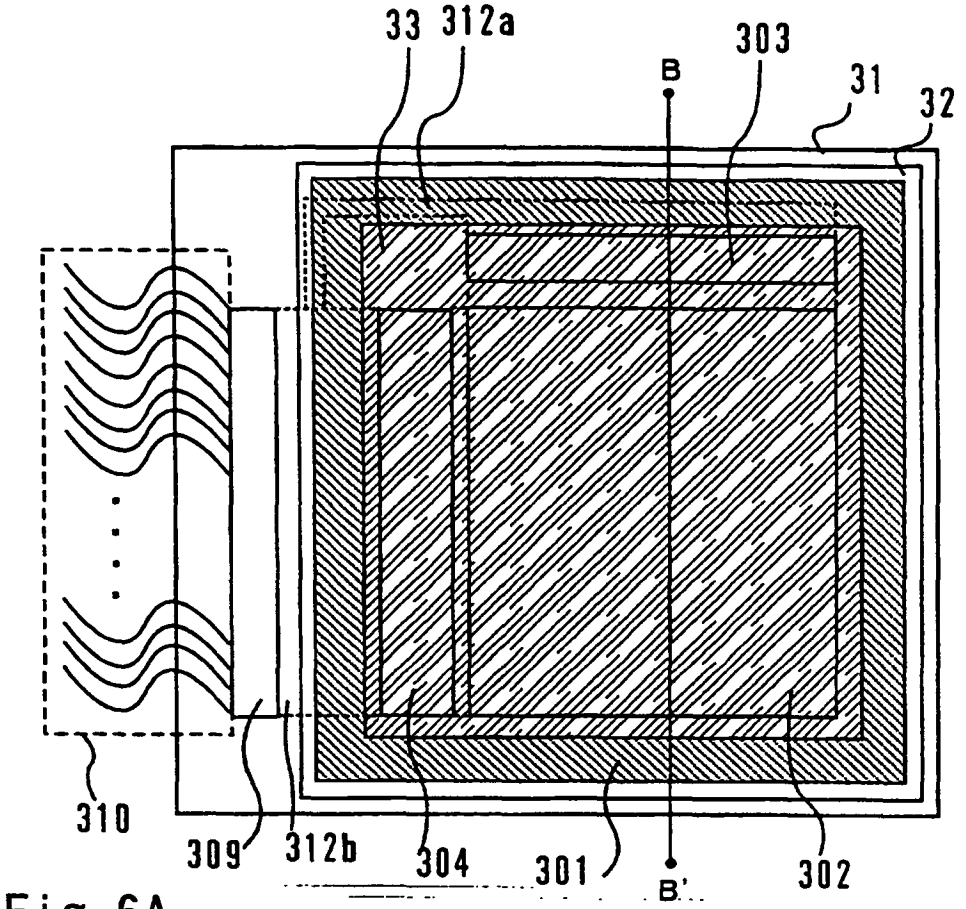

33
312a
303
B
31
32
310
309
312b
304
301
B'
302

Fig. 6A

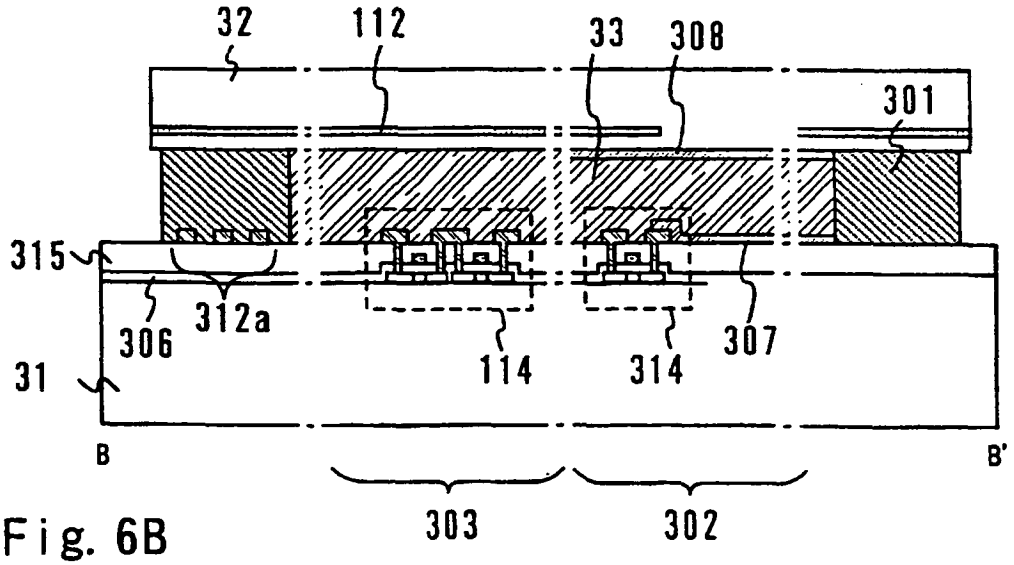

32
112
33
308
301
315
306
312a
114
314
307
31
B
B'
303
302

Fig. 6B

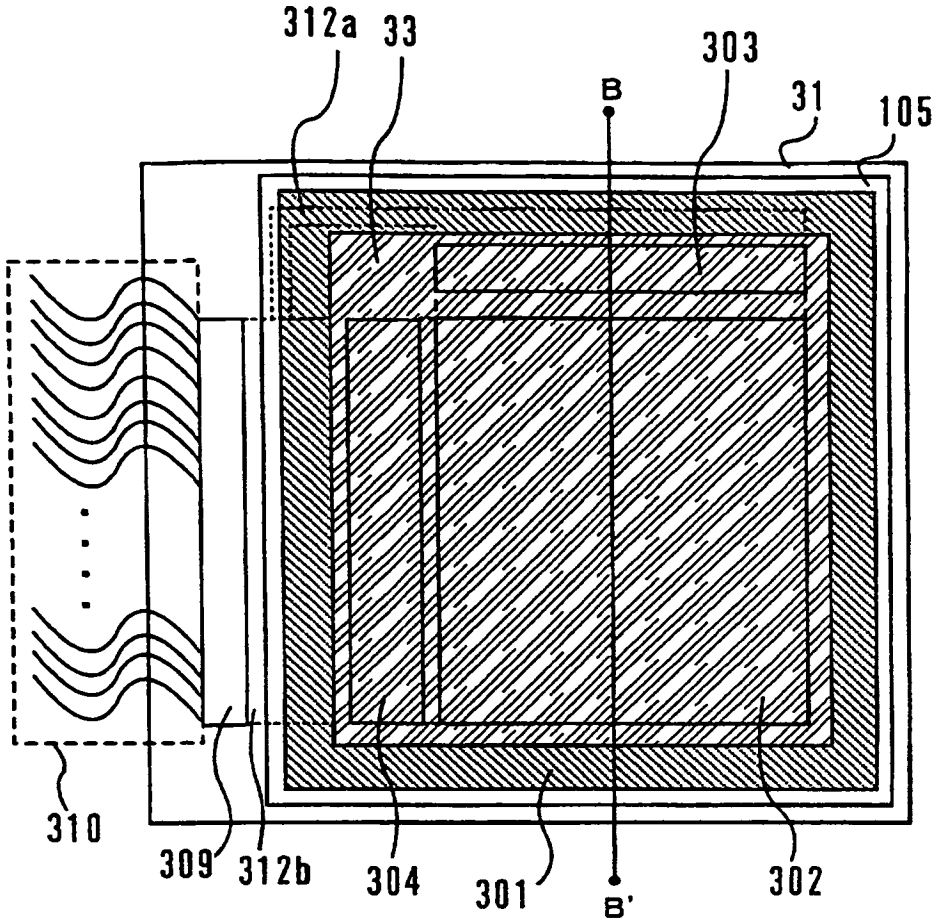

312a
33
303
B
31
105
310
309
312b
304
301
B'
302

Fig. 7A

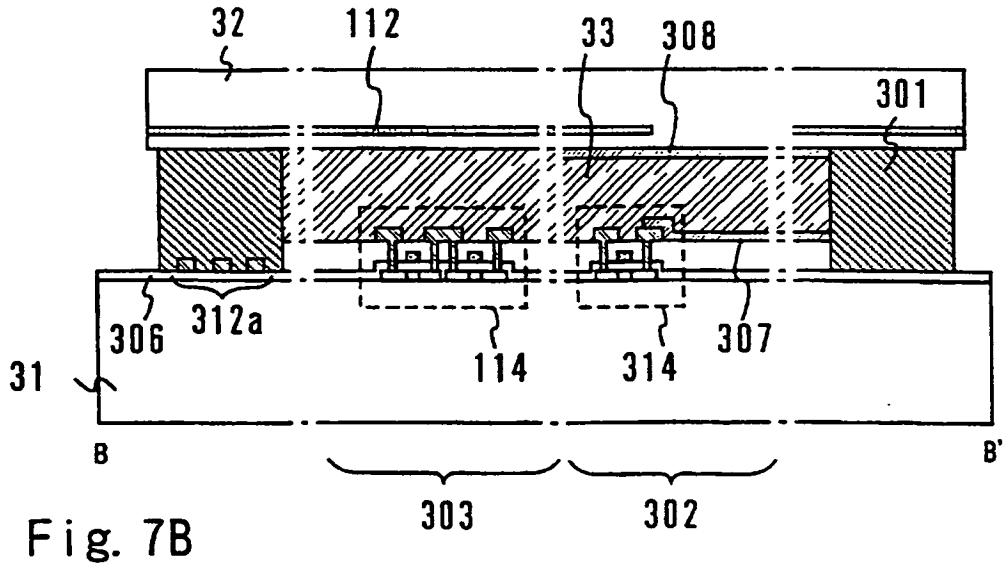

32
112
33
308
301
306
312a
114
314
307
31
B
B'
303
302

Fig. 7B

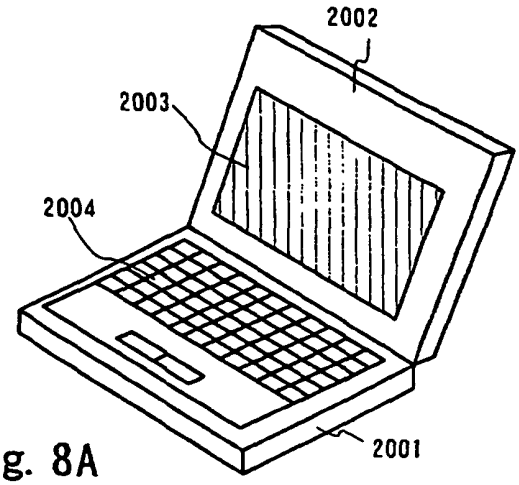


Fig. 8A

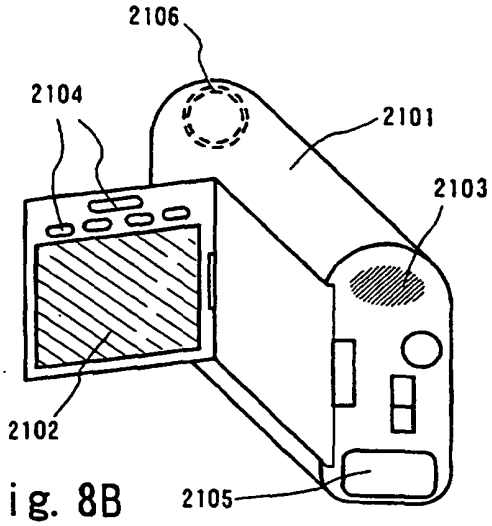


Fig. 8B

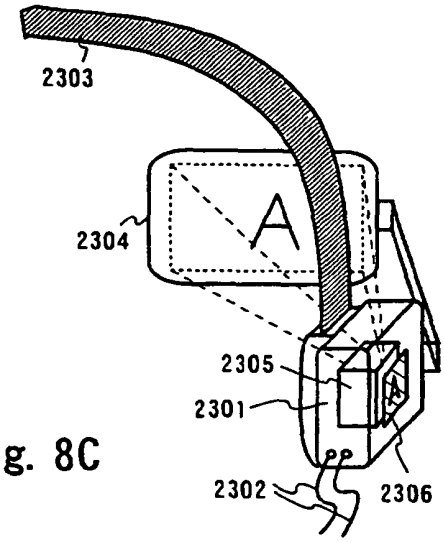


Fig. 8C

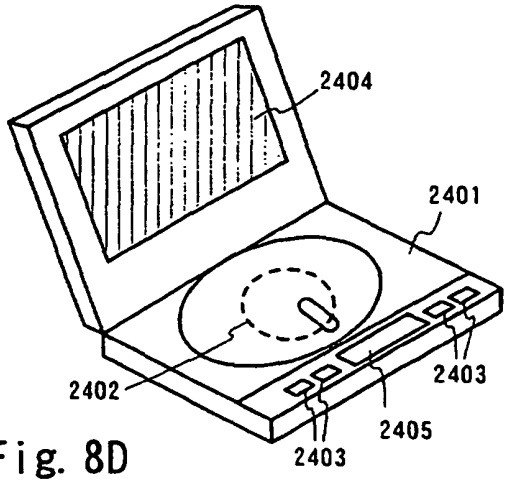


Fig. 8D

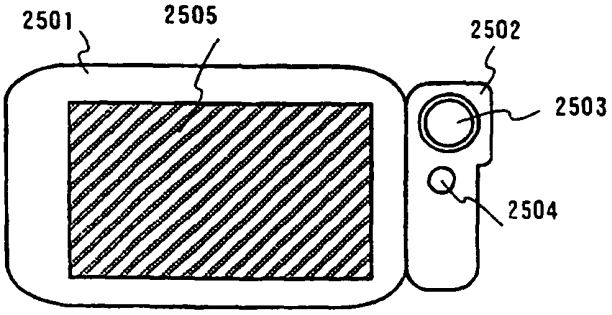


Fig. 8E

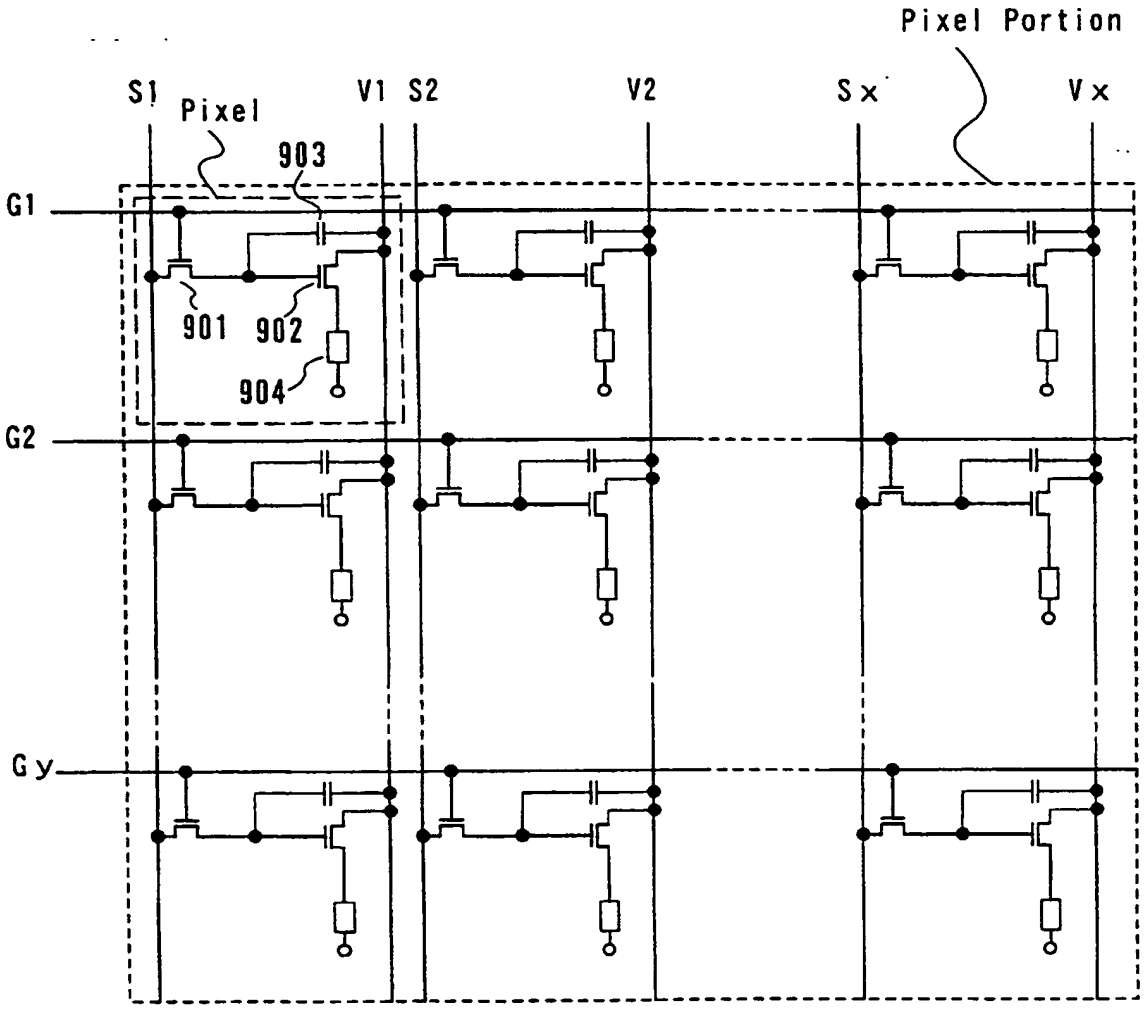


Fig. 9

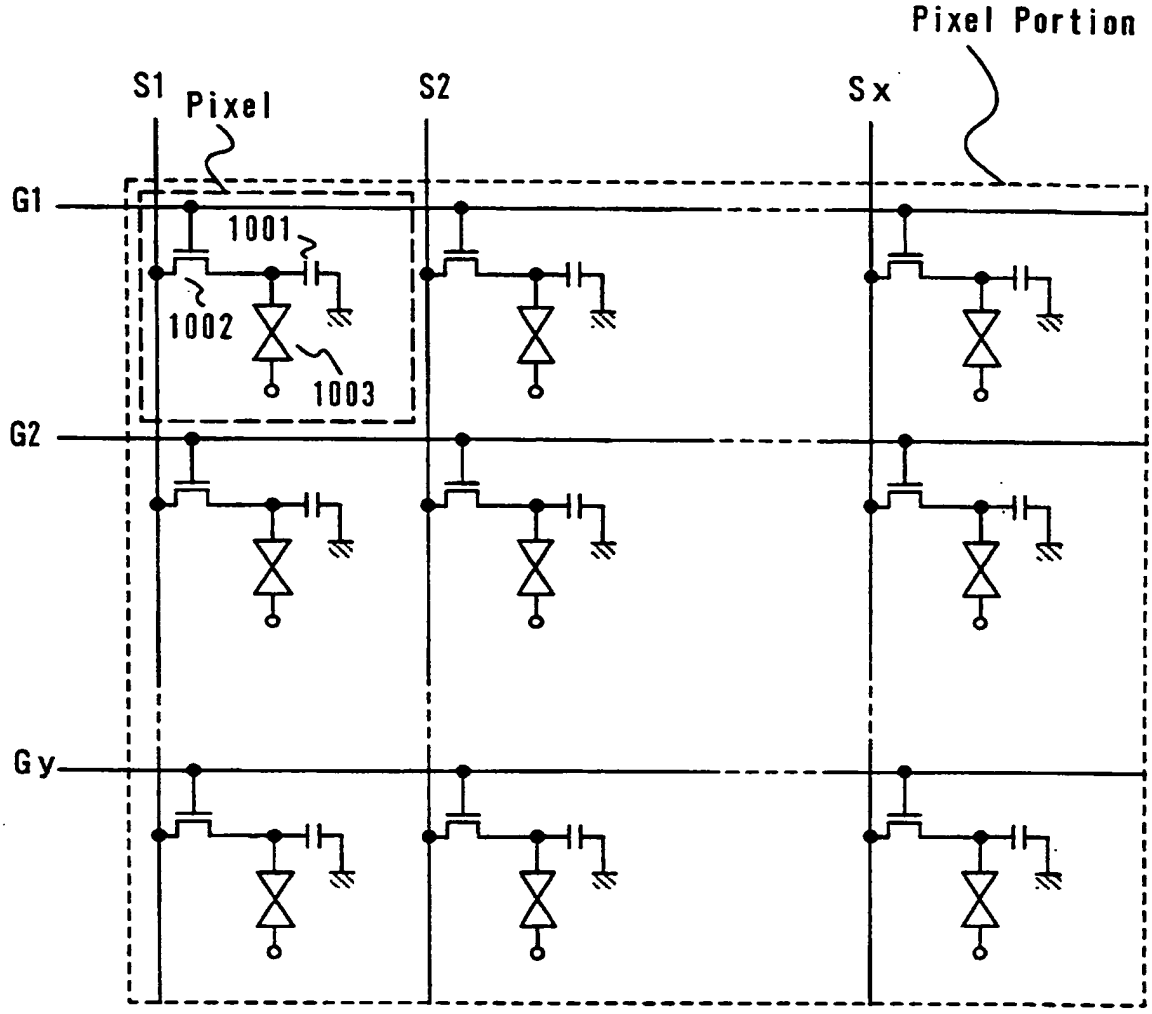


Fig. 10

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	有源矩阵电致发光显示装置的布线和密封方案		
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CPC分类号	G02F1/13454 G02F1/1339 G02F1/1345 G02F1/13452 H01L27/3276 H01L51/524 H01L51/5246		
代理机构(译)	GRÜNECKER，KINKELDEY，STOCKMAIR & SCHWANHÄUSSER		
优先权	2000223488 2000-07-25 JP		
其他公开文献	EP1176457A2 EP1176457A3		
外部链接	Espacenet		

摘要(译)

显示装置的尺寸减小。在用密封构件覆盖的像素基板的一部分中形成布线。每个布线的宽度设定为当密封构件通过布线照射紫外线时允许布线上的密封构件充分暴露于紫外线的宽度。代替使用一条宽布线，每条宽度小的多条布线彼此并联连接。因此，在显示装置中减小了像素部分和驱动电路周围的布线区域和密封构件占据的区域，从而可以使显示装置更小。

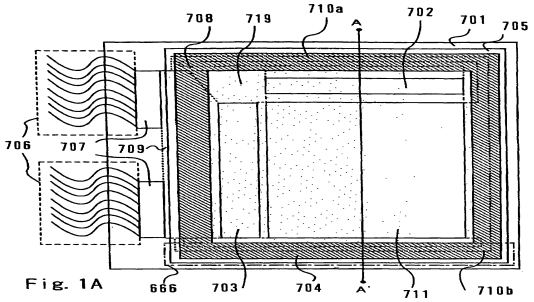

Fig. 1A

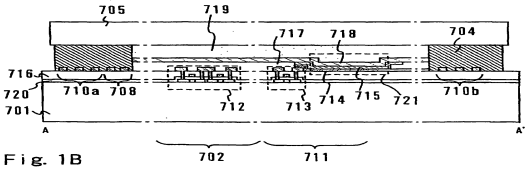

Fig. 1B