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(54) **DISPLAY DEVICE WITH CHIPLET DRIVERS**

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to display devices having a substrate with distributed, independent chiplets for controlling a pixel array.

BACKGROUND OF THE INVENTION

[0002] Flat-panel display devices are widely used in conjunction with computing devices, in portable devices, and for entertainment devices such as televisions. Such displays typically employ a plurality of pixels distributed over a substrate to display images. Each pixel incorporates several, differently colored light-emitting elements commonly referred to as sub-pixels, typically emitting red, green, and blue light, to represent each image element. As used herein, pixels can refer to a single light-emitting element or a group of differently colored light-emitting elements. A variety of flat-panel display technologies are known, for example plasma displays, liquid crystal displays, and light-emitting diode (LED) displays.

[0003] Light emitting diodes (LEDs) incorporating thin films of light-emitting materials forming light-emitting elements have many advantages in a flat-panel display device and are useful in optical systems. U.S. Patent No. 6,384,529 2 to Tang et al. shows an organic LED (OLED) color display that includes an array of organic LED light-emitting elements. Alternatively, inorganic materials can be employed and can include phosphorescent crystals or quantum dots in a polycrystalline semiconductor matrix. Other thin films of organic or inorganic materials can also be employed to control charge injection, transport, or blocking to the light-emitting-thin-film materials, and are known in the art. The materials are placed upon a substrate between electrodes, with an encapsulating cover layer or plate. Light is emitted from a pixel when current passes through the light-emitting material. The frequency of the emitted light is dependent on the nature of the material used. In such a display, light can be emitted through the substrate (a bottom emitter) or through the encapsulating cover (a top emitter), or both.

[0004] LED devices can include a patterned light-emissive layer wherein different materials are employed in the pattern to emit different colors of light when current passes through the materials. Alternatively, one can employ a single emissive layer, for example, a white-light emitter, together with color filters for forming a full-color display, as is taught in U.S. Patent No. 6,987,355 by Cok. It is also known to employ a white sub-pixel that does not include a color filter, for example, as taught in U.S. Patent No. 6,919,681 by Cok et al. This and other disclosures teach a design employing an unpatterned white emitter together with a four-color pixel including red, green, and blue color filters and sub-pixels and an unfiltered white sub-pixel to improve the efficiency of the device (see, e.g. U.S. Patent No. 7,230,594 to Miller, et al).

[0005] Two different methods for controlling the pixels in a flat-panel display device are generally known: active-matrix control and passive-matrix control. In a passive-matrix device, the substrate does not include any active electronic elements (e.g. transistors). An array of row electrodes and an orthogonal array of column electrodes in a separate layer are formed over the substrate; the intersections where the row and column electrodes overlap form the electrodes of a light-emitting diode. External driver chips then sequentially supply current to each row (or column) while the orthogonal column (or row) supplies a suitable voltage to illuminate each light-emitting diode in the row (or column). Therefore, a passive-matrix design employs 2n connections to produce n^2 separately controllable light-emitting elements. However, a passive-matrix drive device is limited in the number of rows (or columns) that can be included in the device since the sequential nature of the row (or column) driving creates flicker. If too many rows are included, the flicker can become perceptible. Moreover, the currents necessary to drive an entire row (or column) in a display can be problematic and the power required for the non-imaging pre-charge and discharge steps of PM driving become dominant as the area of the PM display grows. These two problems limit the physical size of a passive-matrix display.

[0006] In an active-matrix device, active control elements are formed of thin-films of semiconductor material, for example amorphous or poly-crystalline silicon, distributed over the flat-panel substrate. Typically, each sub-pixel is controlled by one control element and each control element includes at least one transistor. For example, in a simple active-matrix organic light-emitting (OLED) display, each control element includes two transistors (a select transistor and a drive transistor) and one capacitor for storing a charge specifying the luminance of the sub-pixel. Each light-emitting element typically employs an independent control electrode and a common electrode. Control of the light-emitting elements is typically provided through a data signal line, a select signal line, a power connection and a ground connection. Active-matrix elements are not necessarily limited to displays and can be distributed over a substrate and employed in other applications requiring spatially distributed control. The same number of external control lines (except for power and ground) can be employed in an active-matrix device as in a passive-matrix device. However, in an active-matrix device, each light-emitting element has a separate driving connection from a control circuit and is active even when not selected for data deposition so that flicker is eliminated.

[0007] One common, prior-art method of forming active-matrix control elements typically deposits thin films of semi-

conductor materials, such as silicon, onto a glass substrate and then forms the semiconductor materials into transistors and capacitors through photolithographic processes. The thin-film silicon can be either amorphous or polycrystalline. Thin-film transistors (TFTs) made from amorphous or polycrystalline silicon are relatively large and have lower performance compared to conventional transistors made in crystalline silicon wafers. Moreover, such thin-film devices typically exhibit local or large-area non-uniformity across the glass substrate that results in non-uniformity in the electrical performance and visual appearance of display employing such materials.

[0008] Employing an alternative control technique, Matsumura et al., in U.S. Patent Application Publication No. 2006/0055864, describe crystalline silicon substrates used for driving LCD displays. The application describes a method for selectively transferring and affixing pixel-control devices made from first semiconductor substrates onto a second planar display substrate. Wiring interconnections within the pixel-control device and connections from busses and control electrodes to the pixel-control device are shown.

[0009] Since a conventional passive-matrix display design is limited in size and number of light-emitting elements, and an active-matrix design using TFTs has lower electrical performance, there is a need for improved control for display devices employing LEDs that overcomes these problems.

[0010] Patent application DE 199 50 839 A1 discloses an embodiment of an OLED display based on a passive-matrix scheme. The display is subdivided in four electrically independent arrays, each of which is controlled by a single control chip. The control chip is connected to each of a plurality of column conductors and row conductors. Address lines are necessary for connecting the control chip with the conductors.

[0011] Patent publication US 6,370,019 B1 discloses a display comprising a plurality of tiles each comprising pixels. Each tile comprises a circuit board with an integrated circuit controlling pixels through conductive traces coupled to vias that extend through the circuit board. The diameter of the vias is less than the spacing of any pixel. This publication discloses how to use an active matrix scheme and also discloses column electrodes and row electrodes.

[0012] Patent application EP 1 187 212 A2 discloses a display apparatus which includes a panel substrate operating as a display screen, plural display devices arranged in a matrix on the panel substrate, and a drive circuit substrate having a drive circuit for driving each display device. Each drive circuit substrate comprises a drive circuit IC, picture signal/power supply terminals, a data line terminal, and scan light terminal. The data line and the scan line terminals are associated with respect to driving lines arranged in a matrix and are used for outputting driving current corresponding to driving signals to the organic EL devices.

SUMMARY OF THE INVENTION

[0013] In accordance with the present invention, there is provided a display device according to claim 1. Preferred embodiments of the display device are recited in the dependent claims.

[0014] The present invention has the advantage that, by providing a display device with chiplet drivers having row and column electrode connections, the number of connection pads and the size and number of chiplets are reduced. In an embodiment of the present invention, a plurality of arrays provides reduced flicker and power requirements. Another advantage of the present invention is that, by providing large spaces on the display substrate for wiring, larger wires can be employed at lower cost and with higher electrical performance. A further advantage is that the monocrystalline silicon chiplets have high mobility and uniformity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

FIG. 1A is a cross sectional view of a chiplet taken along the lines 1A- 1A of FIG. 2 having two connections to the bottom electrode of a light-emitting diode according to an embodiment of the present invention;

FIG. 1B is a cross sectional view of a chiplet taken along the lines 1B- 1B of FIG. 2 having two connections to the top electrode of a light-emitting diode according to an embodiment of the present invention;

FIG. 2 is a plan schematic view of a diagonally oriented chiplet having connection pads according to an embodiment of the present invention;

FIGS. 3A and 3B are schematics of a display device having row and column electrodes and a diagonally oriented chiplet according to an embodiment of the present invention;

FIG. 4 is a schematic of a display device having row and column electrodes and three diagonally oriented chiplets according to an embodiment of the present invention;

FIG. 5 is a schematic of a display device having a pixel array divided into mutually exclusive sub-arrays and two diagonally oriented chiplets according to an embodiment of the present invention;

FIG. 6 is a schematic of a display device having a pixel array and three diagonally oriented chiplets with an alternative distribution according to an alternative embodiment of the present invention;

FIG. 7 is a schematic of a display device having row and column electrodes connected with vias to chiplet connection pads according to an example useful for understanding the present invention;

FIG. 8 is a schematic of a display device having multiple chiplets and a buss routed to avoid the chiplet devices according to another example useful for understanding the present invention;

FIG. 9 is a schematic of a display device having multiple chiplets connected by a buss according to another example useful for understanding the present invention;

FIG. 10A is a cross section of a chiplet having different connection pads according to another embodiment of the present invention;

FIG. 10B is a top view of FIG. 10A in an embodiment of the present invention;

FIG. 11 is a schematic of multiple two-dimensional pixel arrays according to an embodiment of the present invention;

FIG. 12A is an illustration of multiple chiplets and busses located in a serpentine fashion over a substrate, according to an example;

FIG. 12B is a top view of a chiplet having connections useful for understanding the illustration of FIG. 12A; and

FIG. 13 is a larger-scale illustration of multiple chiplets and busses located in a serpentine fashion over a substrate, according to an example.

[0016] Because the various layers and elements in the drawings have greatly different sizes, the drawings are not to scale.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Referring to FIG. 3A, in one embodiment, the present invention includes a display device including a substrate 10, a first layer having an array of row electrodes 16 formed in rows across the substrate 10 in a first direction and a second layer having an array of column electrodes 12 formed in columns across the substrate 10 in a second direction different from the first direction and wherein the first and second electrodes overlap to form pixel locations 30. Referring also to FIG. 1A, one or more layers 14 of light-emitting material are formed between the row and column electrodes 16, 12. Light-emitting diodes 15 are pixels 30 that form a two-dimensional array 32 of pixels in the pixel locations and emit light when a current is passed through the light-emitting layer 14 from the row and column electrodes 16, 12. A plurality of chiplets 20 are located over the substrate 10, the number of chiplets 20 being less than the number of pixels 30, each chiplet 20 exclusively controlling a subset of row electrodes 16 and a subset of column electrodes 12 so that the pixels are controlled to display an image. Each chiplet has a substrate 28 that is independent and separate from the display device substrate 10. In this disclosure, a pixel, sub-pixel, and light-emitting element all refer to a light-emitting diode 15. Each chiplet 20 can include circuitry 22 for controlling the pixels 30 to which the chiplet 20 is connected through connection pads 24. The circuitry 22 can include storage elements 26 that store a value representing a desired luminance for each pixel 30 to which the chiplet 20 is connected in a subset row or column, the chiplet 20 using such value to control the row electrodes 16 or column electrodes 12 connected to the pixel 30, to activate the pixel 30 to emit light. For example, if a chiplet 20 is connected to a subset of 8 rows and 8 columns, eight storage elements 26 can be employed to store luminance information for eight rows or columns. Each time a new row or column is activated, a new subset of luminance information can be supplied to the chiplet 20. In one embodiment of the present invention, two storage elements 26 can be employed for each subset row or column, so that luminance information can be stored in one of the storage elements 26 while the other storage element 26 is employed to display luminance information. In yet another embodiment of the present invention, one or two storage elements 26 can be employed for each light-emitting element 30 to which the chiplet 20 is connected.

[0018] A planarization layer 18 can be employed to form a smooth surface over which the row and column electrodes

16, 12, and the light-emitting layer 14 can be formed. As shown in FIG. 1A, the connection pads 24 of the chiplet 20 can connect to the bottom electrode of the light-emitting diode 15, here shown as the column electrode 12 and indicated with cross section line 1A-1A' in FIG. 2. Alternatively, as shown in FIG. 1B, the connection pads 24 of the chiplet 20 can connect to the top electrode of the light-emitting diode, here shown as the row electrode 16 and indicated with cross section line 1B-1B' in FIG. 2. In this way, the connection pads of chiplet 20 can connect to either row electrodes 16 or column electrodes 12. In FIG. 2 the connection pads 24 of chiplet 20 are distinguished as column connection pads 24A connected to column electrodes 16 and row connection pads 24B connected to row electrodes 16. Hence, in one embodiment of the present invention, the chiplets 20 have two rows (25A and 25B in FIG. 10B) of connection pads 24, one row of connection pads 24A connected to corresponding row electrodes 16 and the other row of connection pads 24B connected to corresponding column electrodes 12. As shown in FIG. 3, however, the row and column electrode pads 24A and 24B are laid out on the substrate 10 to avoid electrical shorts between the row and column electrodes 16, 12, by providing enough space between the column connection pads 24A and the row electrodes 16 and by providing enough space between the row connection pads 24B and the column electrodes 12. FIG. 3A is a simplified figure drawn for illustrative purposes. In an exemplary embodiment shown in FIG. 3B, the column connection pad 24A (not shown) can be covered with the row electrode 16 to increase the overlapping area defining the pixel 30, thereby increasing the aperture ratio of the display device and the lifetime of the display. Depending on the tolerances of the manufacturing process used to construct a display device of the present invention, the column electrodes 12 can be increased in size so long as there is not an electrical short between the column electrodes 12 and the row connection pads 24B and row electrodes 16.

[0019] Referring to FIG. 4, an embodiment of a display device of the present invention can include multiple chiplets (20A, 20B, 20C) distributed over the two-dimensional pixel array 32 formed by the intersections of row and column electrodes 16, 12. (Note that the chiplets are located behind the electrodes so that the electrodes can connect to the connection pads as in FIG. 1A and 1B but the chiplets are shown in front of the electrodes for clarity of illustration in FIGS. 4, 6, and 11.) Each chiplet 20 is connected to a mutually exclusive subset of row electrodes 16 and column electrodes 12. As shown in FIG. 4, chiplet 20A is connected to the top 6 row electrodes 16 in the two-dimensional pixel array 32 and the leftmost 6 column electrodes 12. Chiplet 20B is connected to the central 6 row electrodes 16 in the two-dimensional pixel array 32 and the central 6 column electrodes 12. Chiplet 20C is connected to the bottom 6 row electrodes 16 in the pixel array 32 and the rightmost 6 column electrodes 12. Hence, the pixel array 32 has 18 by 18 or 324 elements controlled by three chiplets 20 with 12 connection pads each. A careful examination of FIG. 4 shows that each chiplet 20 controls a separate group of row and column electrodes 16, 12.

[0020] FIG. 5 is a more detailed illustration having only two chiplets 20A and 20B. Chiplet 20A is connected to row electrodes 16A and column electrodes 12A. Chiplet 20B is connected to row electrodes 16B and column electrodes 12B. Therefore, chiplet 20A controls a first pixel subset 32A and chiplet 20B controls a first pixel subset 32D. Chiplet 20A controls only the column electrodes 12A for a second pixel subset 32C of the pixels 30 in the pixel array 32, and controls only the row electrodes 16A for a third pixel subset 32B of the pixels 30 in the pixel array 32. Similarly, chiplet 20B controls only the column electrodes 12B for a second pixel subset 32B of the pixels 30 in the pixel array 32, and controls only the row electrodes 16B for a third pixel subset 32C of the pixels 30 in the pixel array 32. The pixel subsets 32A, 32B, 32C, 32D are mutually exclusive. Hence, chiplet 20A has complete control over the pixels 30 in pixel subset 32A, since chiplet 20A controls both the row electrodes 16A and the column electrodes 12A necessary to control the pixels 30 in the pixel subset 32A. Similarly, chiplet 20B has complete control over the pixels 30 in pixel subset 32D, since chiplet 20B controls both the row electrodes 16B and the column electrodes 12B necessary to control the pixels 30 in the pixel subset 32D. Therefore, row electrodes 16A and 16B are electrically independent, and column electrodes 12A and 12B are electrically independent. However, both chiplet 20A and chiplet 20B acting in concert control the pixels 30 in pixel subsets 32B and 32C. This control is provided by circuitry 22 in the chiplets 20. Since pixel subsets 32A and 32D are completely controlled, they are referred to as directly driven pixel arrays, whereas pixel subsets 32B and 32C are referred to as indirectly driven pixel arrays.

[0021] The present invention provides reduced costs over the prior art. For example, if a conventional, active-matrix backplane were employed to drive the 324 pixels 30 of FIG. 4, a relatively low-performance and expensive thin-film semiconductor backplane would be necessary. The present invention instead employs a few high-performance, inexpensive chiplets to drive the pixels 30.

[0022] A large variety of chiplet layouts can be employed in various embodiments of the present invention. As shown in FIGS. 3A, 3B, 4, and 5, the chiplets 20 are located on a diagonal 13 of the pixel array 32. Adjacent chiplets 20 control adjacent second subsets of column electrodes and adjacent chiplets control adjacent third subsets of row electrodes. As intended herein, a diagonal is a line that is slanted or oblique with respect to either the row electrodes or the column electrodes or both. However, it is not necessary that the chiplets 20 be arranged in a single diagonal line. Referring to FIG. 6 and compared to FIG. 4, the duplets 20 are located on a plurality of spaced-apart diagonals. Chiplet 20A controls the topmost 6 row electrodes and leftmost 6 column electrodes (as in FIG. 4). However, chiplet 20B controls the rightmost 6 column electrodes and the central 6 row electrodes. Chiplet 20C controls the central 6 column electrodes and the

bottom 6 row electrodes. This alternative arrangement is useful because it separates and provides more space for the chiplets 20. In particular, if the circuitry in the chiplets takes significant space within the chiplet so that, for example the chiplets 20 have a display connection portion 21A at one end of the chiplet 20 and a control circuitry connection portion 21B at the other end of the chiplet 20, a chiplet 20 arrangement that spaces the chiplets farther apart is useful. In an alternative design of an example (see FIGS. 12A, 12B, and 13), a display connection portion 21A can be located at each end of the chiplet 20 and a control circuitry connection portion 21B in the middle of the chiplet 20.

[0023] In a further example, the chiplets are not laid out on diagonal lines of the pixel array 32. Although diagonal arrangements are useful for minimizing interconnection lengths, they require careful alignment with respect to the connection pads 24 and row and column electrodes 16, 12. Moreover, the spacing of the row and column electrodes 16, 12 can cause the chiplets 20 to be larger than necessary, as illustrated in FIGS. 3A, 3B, 4, 5, and 6, for example. Referring to FIG. 7, in an example useful for understanding the present invention, the chiplets 20 can be aligned in any orientation with respect to the pixel array 32 and substrate 10, including aligning an edge of a chiplet 20 with a row or column electrode 16 or 12. The chiplet can have a long dimension DI and a short dimension D2, and the long dimension D1 can be parallel to the first direction or the second direction (FIG. 10B) of the row or column electrodes, respectively.

[0024] Indeed, different chiplets 20 can be differently aligned. As shown in FIG. 7, a long dimension of a chiplet 20 is aligned with row electrodes 16. Connection pads 24 are connected with wiring to the column electrodes 12 and row electrodes 16. Vias 50 can be employed to connect from one wiring layer to another and are formed between, for example, the row electrodes 16 to avoid electrical shorts with the column electrodes 12. Since considerable wiring 52 can be necessary to electrically connect the connection pads 24 to the row and column electrodes 16, 12, a top emitter configuration can be preferred, in which the top electrode (e.g. 16 in FIG. 1A and 1B) is transparent and the bottom electrode (e.g. 12 in FIG. 1A and 1B) can be reflective. The substrate 10 can also be opaque.

[0025] Referring to FIG. 8 in another example useful for understanding the present invention, the chiplets 20 can be connected to an external controller 40 through a buss 42. The buss 42 can be a serial, parallel, or point-to-point buss and can be digital or analog. A serial buss, shown in FIG. 9, is one in which data is retransmitted from one chiplet to the next on an electrically separate electrical connection. A parallel buss, shown in FIG. 8, is one in which data is simultaneously broadcast to all of the chiplets on an electrically common electrical connection. The buss 42 is connected to the chiplets to provide signals, such as power, ground, data, or select signals. More than one buss 42 can be employed. The chiplets 20 can have a pixel connection portion 21A at one end of the chiplet 20 and a circuitry portion 21B connected to a buss 42 at the other end. Referring to FIGS. 10A and 10B, each chiplet can have a first group of connection pads 24 connected to the row and column electrodes and second group of connection pads 25 connected to the control buss, wherein the first and second groups of connection pads are spatially separated. As shown in FIGS. 10A and 10B, each chiplet also can have a third group of connection pads 25 in the center of the chiplet connected to a control buss; the first, second, and third groups of connection pads are spatially separated.

[0026] Alternatively, no separate chiplet portions can be employed. Referring to FIGS. 10A, 10B, additional connection pads 25 for connecting to a buss 42 can also be provided in the chiplet 20 and can be located at a circuitry portion of a chiplet or at either end of the long dimension D1 of a chiplet 20, or in the center of the chiplet 20. Internal chiplet connections 44 can be employed to route buss connections from one end of a chiplet 20 to another end.

[0027] Referring back to FIG. 8, a chiplet arrangement corresponding to that shown in FIG. 5 is illustrated. This arrangement has the advantage of providing areas on the device substrate 10 that are not occupied with chiplets 10 and that can then be used for routing busses 42. For example, as shown in FIG. 8, pixel subsets 32A, 32D, 32E, and 32H forming pixel connection areas that are at least partially occupied with duplets 20A, 20B, 20C, and 20D, respectively. In contrast, buss connection areas 32B, 32C, 32F, and 32G form buss connection areas that can be employed for routing buss 42 wires. Hence, in some examples, the busses can have a serpentine path.

[0028] FIG. 8 illustrates an example useful for understanding in which the buss 42 is connected in parallel in common to all of the chiplets 20A, 20B, 20C, and 20D. In an alternative example shown in FIG. 9, serial buss 42 connections can be routed through chiplets 20A, 20B, 20C, and 20D.

[0029] Referring to FIG. 11 in a further embodiment of the present invention, a plurality of two-dimensional pixel arrays 32 of pixels can be located over a common substrate 10, each two-dimensional pixel array 32 having a separate set of row electrodes 16, column electrodes 12, and chiplets 20. Hence, the structure described above can be replicated on a larger substrate 10. Each two-dimensional array structure can operate independently to reduce electrode impedance, precharge and discharge power consumption, and flicker. The structures can be connected to a common buss 42 system. Thus, in one embodiment of the present invention, a display device can include a substrate; a first layer having a plurality of arrays of row electrodes formed in rows across the substrate in a first direction and a second layer having a corresponding plurality of arrays of column electrodes formed in columns across the substrate in a second direction different from the first direction wherein the first and second electrodes overlap to form pixel locations; one or more layers of light-emitting material formed between the row and column electrodes to form two-dimensional arrays of pixels, the pixels being located in the pixel locations; and a plurality of chiplets for each array located over the substrate, the number of chiplets in each array being less than the number of pixels in the corresponding array, each array chiplet exclusively

controlling a subset of row electrodes and a subset of column electrodes for the corresponding array.

[0030] FIG. 12A illustrates an example in which the chiplets 20 are located in the indirectly driven pixel arrays with the control circuitry connection portion 21B of the chiplet directly under the buss wiring. The chiplet 20 has two display connection portions 21A, one on each end of the chiplet 20. Each display connection portion 21 A is connected by wires to the vertical electrodes and to the horizontal electrodes in the adjacent directly driven pixel arrays. The directly driven blocks of pixels shown as shaded in FIG 12A form a checkerboard pattern on the display, and the wiring buss forms a serpentine pattern as it is formed across the control circuitry connection portions 21 B of the chiplets 20 located in the indirectly driven pixel arrays.

[0031] FIG. 12B illustrates the detailed wiring connections of the display connection portion 21 A of the chiplet 20 to the vertical and horizontal electrodes. This figure illustrates the simple case of 6 horizontal and 6 vertical electrodes in the directly driven pixel array. Connections on wires to the vertical electrodes are shown with shaded squares, whereas connection on wires to the horizontal electrodes are shown with open squares. A similar design will work with any number of horizontal and vertical connections.

[0032] FIG. 12A and FIG 12B show that the electrode connection wires can be patterned to leave a wide area for the control and power bus wiring 42, thus both types of wires can be constructed in the same metal layer, reducing the cost of the display compared to designs that require 2 or more wiring layers. Thus, a control buss can be located in a third layer separate from the first and second layers used for the row and column electrodes.

[0033] An additional advantage of this design is that the wires can be patterned using low-cost methods since there is ample area available for the wiring. For example, systems developed for printed-circuit board fabrication use low-cost photo-masks and proximity exposure tools capable of making 25 um lines and 25 um spaces. These are much lower cost than TFT photo-masks and TFT stepper exposure tools. This results in a back-plane fabrication process requiring less capital expense, less operating expense, and reduced TAC time.

[0034] Referring to FIG. 10B, the connection pads have center-to-center pitch 23 spacing the connection pads apart on the chiplets. Vias (FIG. 1B) form openings that expose the connection pads to which the control buss can be connected in a first portion that extends through the openings to the connection pads. The control busses can have a separate second portion having a width greater than the pitch of the connection pads, thereby enabling buss wires with a greater width and improved conductivity.

[0035] In some cases the physical length of the chiplet can be constrained, such as by the limits of the chiplet transfer system, or due to the number of electrical conductors that can be formed inside the chiplet. In such cases, the length of the display connection portion of the chiplets can be reduced to half, and a second serpentine line of chiplets added. This is shown in FIG 13. In this example the indirectly controlled area has been increased (shown as unshaded areas), providing more room for the control and power bus wiring, enabling processing by even less precise and lower cost methods.

[0036] Referring to FIG. 11, in operation, controller 40 receives and processes an information signal according to the needs of the display device and transmits the processed signal through one or more busses 42 to each chiplet 20 in the device. The processed signal includes luminance information for each light-emitting pixel 30 corresponding to the chiplet 20. The luminance information can be stored in a storage element 26 corresponding to each light-emitting pixel 30. The chiplets then sequentially activate the row and column electrodes to which they are connected. When both the row and column electrode for a pixel is activated, current can flow through the pixel defined by the row and column electrode to emit light. Typically, an entire row or column of electrodes within a pixel array are activated simultaneously be activating all of the column electrodes and one row electrode at once. The column electrodes are controlled to provide the individual luminance desired for each pixel in the row. Then a second row is selected and the process repeats until all of the rows are activated and all of the pixels emit light. The process can then repeat. Note that some of the pixels are controlled by one chiplet and some require two chiplets acting in concert. Note that the designation of "row" and "column" is arbitrary and the functions of row and column electrodes can be reversed.

[0037] Although the sequential activation of separate rows (or columns) in a display device can induce flicker, employing multiple, independently controlled pixel arrays 32 reduces the number of rows or columns in each separately controlled pixel array 32. Since the pixel groups 32 are simultaneously activated, flicker can be greatly reduced. Moreover, because the group row electrodes 16 and group column electrodes 12 are connected only within a pixel array 32, the group row electrodes 16 and group column electrodes 12 are short, reducing the electrode capacitance and resistance and the need for high-power driving circuitry in the chiplet 20. Hence, the portion of time that each pixel row emits light is increased, flicker is decreased, and current densities decreased at a desired luminance.

[0038] The busses 42 can supply a variety of signals, including timing (e.g. clock) signals, data signals, select signals, power connections, or ground connections. The signals can be analog or digital, for example digital addresses or data values. Analog data values can be supplied as charge. The storage elements 26 can be digital (for example including flip-flops) or analog (for example including capacitors for storing charge).

[0039] In various embodiments of the present invention, the chiplets 20 distributed over the substrate 10 can be identical. However, a unique identifying value, i.e. an ID, can be associated with each chiplet 20. The ID can be assigned

before or, preferably, after the chiplet 20 is located over the substrate 10 and the ID can reflect the relative position of the chiplet 20 on the substrate 10, that is, the ID can be an address. For example, the ID can be assigned by passing a count signal from one chiplet 20 to the next in a row or column. Separate row or column ID values can be used.

[0040] The controller 40 can be implemented as a chiplet and affixed to the substrate 10. The controller 40 can be located on the periphery of the substrate 10, or can be external to the substrate 10 and include a conventional integrated circuit.

According to various embodiments of the present invention, the chiplets 20 can be constructed in a variety of ways, for example with one or two rows of connection pads 24 along a long dimension of a chiplet 20. The interconnection busses 42 or wires 52 can be formed from various materials and can use various methods for deposition on the device substrate. For example, the interconnection busses 42 or wires 52 can be metal, either evaporated or sputtered, for example aluminum or aluminum alloys. Alternatively, the interconnection busses 52 or wires 52 can be made of cured conductive inks or metal oxides. In one cost-advantaged embodiment, the interconnection busses 42 or wires 52, or both, are formed in a single layer.

[0041] The present invention is particularly useful for multi-pixel device embodiments employing a large device substrate, e.g. glass, plastic, or foil, with a plurality of chiplets 20 arranged in a regular arrangement over the device substrate 10. Each chiplet 20 can control a plurality of pixels 30 formed over the device substrate 10 according to the circuitry in the chiplet 20 and in response to control signals. Individual pixel groups or multiple pixel groups can be located on tiled elements, which can be assembled to form the entire display.

[0042] According to the present invention, chiplets 20 provide distributed pixel control elements over a substrate 10. A chiplet 20 is a relatively small integrated circuit compared to the device substrate 10 and includes a circuit 22 including wires, connection pads, passive components such as resistors or capacitors, or active components such as transistors or diodes, formed on an independent substrate 28. Chiplets 20 are separately manufactured from the display substrate 10 and then applied to the display substrate 10. The chiplets 20 are preferably manufactured using silicon or silicon on insulator (SOI) wafers using known processes for fabricating semiconductor devices. Each chiplet 20 is then separated prior to attachment to the device substrate 10. The crystalline base of each chiplet 20 can therefore be considered a substrate 28 separate from the device substrate 10 and over which the chiplet's circuitry 22 is disposed. The plurality of chiplets 20 therefore has a corresponding plurality of substrates 28 separate from the device substrate 10 and each other. In particular, the independent substrates 28 are separate from the substrate 10 on which the pixels 30 are formed and the areas of the independent, chiplet substrates 28, taken together, are smaller than the device substrate 10. Chiplets 20 can have a crystalline substrate 28 to provide higher performance active components than are found in, for example, thin-film amorphous or polycrystalline silicon devices. Chiplets 20 can have a thickness preferably of 100 um or less, and more preferably 20 um or less. This facilitates formation of the adhesive and planarization material 18 over the chiplet 20 that can then be applied using conventional spin-coating techniques. According to one embodiment of the present invention, chiplets 20 formed on crystalline silicon substrate are arranged in a geometric array and adhered to a device substrate (e.g. 10) with adhesion or planarization materials. Connection pads 24 on the surface of the chiplets 20 are employed to connect each chiplet 20 to signal wires, power busses and row or column electrodes (16, 12) to drive pixels 30. Chiplets 20 can control at least four pixels 30.

[0043] Since the chiplets 20 are formed in a semiconductor substrate, the circuitry of the chiplet can be formed using modern lithography tools. With such tools, feature sizes of 0.5 microns or less are readily available. For example, modern semiconductor fabrication lines can achieve line widths of 90 nm or 45 nm and can be employed in making the chiplets of the present invention. The chiplet 20, however, also requires connection pads 24 for making electrical connection to the wiring layer provided over the chiplets once assembled onto the display substrate 10. The connection pads 24 are sized based on the feature size of the lithography tools used on the display substrate 10 (for example 5 um) and the alignment of the chiplets 20 to the wiring layer (for example +/- 5um). Therefore, the connection pads 24 can be, for example, 15 um wide with 5 um spaces between the pads. This means that the pads will generally be significantly larger than the transistor circuitry formed in the chiplet 20.

[0044] The pads can generally be formed in a metallization layer on the chiplet over the transistors. It is desirable to make the chiplet with as small a surface area as possible to enable a low manufacturing cost. Therefore, the size and number of the connection pads and not the transistors will generally limit the size of the chiplet.

By employing chiplets with independent substrates (e.g. including crystalline silicon) having circuitry with higher performance than circuits formed directly on the substrate (e.g. amorphous or polycrystalline silicon), a device with higher performance is provided. Since crystalline silicon has not only higher performance but much smaller active elements (e.g. transistors), the circuitry size is much reduced so that the chiplet size is determined by the number and spacing of connection pads necessary to control and power the device. A useful chiplet can also be formed using micro-electro-mechanical (MEMS) structures, for example as described in "A novel use of MEMS switches in driving AMOLED", by Yoon, Lee, Yang, and Jang, Digest of Technical Papers of the Society for Information Display, 2008, 3.4, p. 13.

[0045] The device substrate 10 can include glass and the wiring layers made of evaporated or sputtered metal, e.g. aluminum or silver, formed over a planarization layer (e.g. resin) patterned with photolithographic techniques known in

the art. The chiplets 20 can be formed using conventional techniques well established in the integrated circuit industry.

[0046] The present invention can be employed in devices having a multi-pixel infrastructure. In particular, the present invention can be practiced with LED devices, either organic or inorganic, and is particularly useful in information-display devices. In a preferred embodiment, the present invention is employed in a flat-panel OLED device composed of small-molecule or polymeric OLEDs as disclosed in, but not limited to U.S. Patent No. 4,769,292 to Tang et al., and U.S. Patent No. 5,061,569 to VanSlyke et al. Inorganic devices, for example, employing quantum dots formed in a polycrystalline semiconductor matrix (for example, as taught in U.S. Patent Application Publication No. 2007/0057263 by Kahen), and employing organic or inorganic charge-control layers, or hybrid organic/inorganic devices can be employed. Many combinations and variations of organic or inorganic light-emitting displays can be used to fabricate such a device, including active-matrix displays having either a top- or a bottom-emitter architecture.

PARTS LIST

[0047]

D1	long dimension
D2	short dimension
10	substrate
12	column electrode
12A, 12B	column electrode group
13	diagonal
14	light-emissive material
15	light-emitting diode
16	row electrode
16A, 16B	row electrode group
18	planarization layer
20	chiplet
20A, 20B, 20C, 20D	chiplet
21A	display connection portion
21B	control circuit connection portion
22	circuitry
23	connection pad pitch
24	connection pad
24A	column connection pad
24B	row connection pad
25	buss connection pad
25A, 25B	row of connection pads
26	storage element
28	chiplet substrate
30	pixel
32	two-dimensional pixel array
32A, 32B, 32C, 32D, 32E, 32F, 32G, 32H	pixel subsets
40	controller
42	buss
44	internal chiplet connection
50	via
52	wire

Claims

1. A display device, comprising:

(a) a substrate (10);

(b) a first layer having an array of row electrodes (16) formed in rows across the substrate (10) in a first direction and a second layer having an array of column electrodes (12) formed in columns across the substrate (10) in a second direction different from the first direction wherein the row and column electrodes (12, 16) overlap to form pixel locations;

(c) one or more layers (14) of light-emitting material formed between the row and column electrodes (12, 16) to form a two-dimensional array of pixels (32), the pixels (30) being located in the pixel locations; and
(d) a plurality of chiplets (20) located over the substrate (10) on a diagonal of the pixel array or on a plurality of spaced-apart diagonals of the pixel array, the number of chiplets (20) being less than the number of pixels (30), each chiplet (20) being configured to exclusively control a subset of row electrodes (16) and a subset of column electrodes (12), whereby the pixels (30) are configured to be controlled to display an image,

characterized in that
each chiplet (20) is diagonally oriented with respect to the row and column electrodes (12, 16) and has two rows of connection pads (24), wherein one row of connection pads (24B) is connected to the corresponding row electrodes (16) and one row of connection pads (24A) is connected to the corresponding column electrodes (12).

2. The display device of claim 1, wherein each chiplet (20) has a storage element (26) for at least each pixel (30) to which it is connected in a subset row or column, the storage element (26) storing a value representing a desired luminance for each pixel (30) and the chiplet (20) using such value to control the row electrodes (16) or column electrodes (12) connected to the pixel (30).

3. The display device of claim 1, wherein a first chiplet (20A) of the plurality of chiplets (20) controls the column electrodes (12) for a first subset of pixels and a second chiplet (20B) of the plurality of chiplets (20) controls the row electrodes (16) for the first subset of pixels.

4. The display device of claim 3, wherein the first chiplet (20A) is configured to control both the column electrodes (12) for a second subset of pixels different from the first subset and the row electrodes (16) for the second subset of pixels.

5. The display device of claim 1, further comprising a controller (40) configured for controlling signals transmitted to the chiplets (20) through one or more busses (42).

6. The display device of claim 1, including one or more serial or parallel buss connections electrically connected to each chiplet.

7. The display device of claim 6, wherein a buss (42) is configured to provide a power or ground electrical connection or a buss (42) is configured to transmit a data signal or a control signal.

8. The display device of claim 1, further including a control buss (42), wherein each chiplet (20) has a first group of connection pads connected to the row and column electrodes (12, 16) and a second group of connection pads connected to the control buss, wherein the first and second groups of connection pads are spatially separated.

9. The display device of claim 8, wherein each chiplet (20) has a third group of connection pads connected to the control buss, and wherein the first, second, and third groups of connection pads are spatially separated.

10. The display device of claim 8, wherein each chiplet (20) further includes a third group of connection pads connected to the row and column electrodes (12, 16), and wherein the first, second, and third groups of connection pads are spatially separated.

11. The display device of claim 1, further including a third layer separate from the first and second layers and a control buss located in the third layer.

12. The display device of claim 11, further comprising spaced-apart connection pads having a pitch formed on the chiplets and openings formed to expose the connection pads and wherein the control buss has a first portion that extends through the openings to the connection pads, and a separate second portion having a width greater than the pitch of the connection pads.

Patentansprüche

1. Anzeigevorrichtung, umfassend:

(a) ein Substrat (10);

(b) eine erste Schicht mit einem Feld von Zeilenelektroden (16), die in Zeilen über das Substrat (10) in einer ersten Richtung gebildet sind und eine zweite Schicht mit einem Feld von Spaltenelektroden (12), die in Spalten über das Substrat (10) in einer von der ersten Richtung verschiedenen zweiten Richtung gebildet sind, wobei sich die Zeilen- und Spaltenelektroden (12, 16) überlappen, um Pixelorte zu bilden;

(c) eine oder mehrere Schichten (14) lichtemittierenden Materials, die zwischen den Zeilen- und Spaltenelektroden (12, 16) gebildet sind, um ein zweidimensionales Feld von Pixeln (32) zu bilden, wobei sich die Pixel (30) in den Pixelorten befinden; und

(d) eine Vielzahl von Chiplets (20), die sich über dem Substrat (10) auf einer Diagonale des Pixelfelds oder auf einer Vielzahl von voneinander beanstandeten Diagonalen des Pixelfelds befinden, wobei die Anzahl der Chiplets (20) kleiner ist als die Anzahl der Pixel (30), wobei jedes Chiplet (20) dazu eingerichtet ist, eine Untermenge von Zeilenelektroden (16) und eine Untermenge von Spaltenelektroden (12) exklusiv zu steuern, wobei die Pixel (30) dazu eingerichtet sind, gesteuert zu werden, um ein Bild anzuzeigen,

dadurch gekennzeichnet, dass

jedes Chiplet (20) bezüglich der Zeilen- und Spaltenelektroden (12, 16) diagonal ausgerichtet ist und zwei Reihen von Anschlusspads (24) aufweist, wobei eine Reihe der Anschlusspads (24B) mit den entsprechenden Zeilenelektroden (16) verbunden ist und eine Reihe der Anschlusspads (24A) mit den entsprechenden Spaltenelektroden (12) verbunden ist.

2. Anzeigevorrichtung nach Anspruch 1, bei der jedes Chiplet (20) ein Speicherelement (26) für mindestens jeden Pixel (30) aufweist, mit dem es in einer Untermengenzeile oder -spalte verbunden ist, wobei das Speicherelement (26) einen Wert speichert, der eine gewünschte Leuchtstärke für jeden Pixel (30) repräsentiert, und wobei das Chiplet (20) einen solchen Wert verwendet, um die mit dem Pixel (30) verbundenen Zeilenelektroden (16) oder Spaltenelektroden (12) zu steuern.

3. Anzeigevorrichtung nach Anspruch 1, bei der ein erstes Chiplet (20A) der Vielzahl von Chiplets (20) die Spaltenelektroden (12) für eine erste Untermenge von Pixeln steuert und ein zweites Chiplet (20B) der Vielzahl von Chiplets (20) die Zeilenelektroden (16) für die erste Untermenge von Pixeln steuert.

4. Anzeigevorrichtung nach Anspruch 3, bei der das erste Chiplet (20A) dazu eingerichtet ist, sowohl die Spaltenelektroden (12) für eine zweite Untermenge von Pixeln, die von der ersten Untermenge verschieden ist, als auch die Zeilenelektroden (16) für die zweite Untermenge von Pixeln zu steuern.

5. Anzeigevorrichtung nach Anspruch 1, ferner umfassend eine Steuereinheit (40), die zum Steuern von Signalen eingerichtet ist, die zu den Chiplets (20) durch einen oder mehrere Busse (42) übertragen werden.

6. Anzeigevorrichtung nach Anspruch 1, umfassend eine oder mehrere serielle oder parallele Busverbindungen, die elektrisch mit jedem Chiplet verbunden sind.

7. Anzeigevorrichtung nach Anspruch 6, bei der ein Bus (42) dazu eingerichtet ist, eine elektrische Strom- oder Masseverbindung bereitzustellen, oder ein Bus (42) dazu eingerichtet ist, ein Datensignal oder ein Steuersignal zu übertragen.

8. Anzeigevorrichtung nach Anspruch 1, ferner umfassend einen Steuerbus (42), wobei jedes Chiplet (20) eine erste Gruppe von Anschlusspads, die mit den Zeilen- und Spaltenelektroden (12, 16) verbunden sind, und eine zweite Gruppe von Anschlusspads aufweist, die mit dem Steuerbus verbunden sind, wobei die erste und zweite Gruppe von Anschlusspads räumlich voneinander getrennt sind.

9. Anzeigevorrichtung nach Anspruch 8, bei der jedes Chiplet (20) eine dritte Gruppe von Anschlusspads aufweist, die mit dem Steuerbus verbunden sind, und wobei die erste, zweite und dritte Gruppe von Anschlusspads räumlich voneinander getrennt sind.

10. Anzeigevorrichtung nach Anspruch 8, bei der jedes Chiplet (20) ferner eine dritte Gruppe von Anschlusspads umfasst, die mit den Zeilen- und Spaltenelektroden (12, 16) verbunden sind, und wobei die erste, zweite und dritte Gruppe von Anschlusspads räumlich voneinander getrennt sind.

11. Anzeigevorrichtung nach Anspruch 1, ferner umfassend eine von der ersten und zweiten Schicht getrennte dritte Schicht und einen sich in der dritten Schicht befindenden Steuerbus.

12. Anzeigevorrichtung nach Anspruch 11, ferner umfassend voneinander beanstandete Anschlusspads mit einem auf den Chiplets gebildeten Zwischenraum und mit Öffnungen, die die Anschlusspads freilegen, und wobei der Steuerbus einen ersten Abschnitt, der sich durch die Öffnungen zu den Anschlusspads erstreckt, und einen getrennten zweiten Abschnitt aufweist, der eine größere Breite hat als der Zwischenraum der Anschlusspads.

Revendications

1. Dispositif d'affichage, comprenant :

(a) un substrat (10) ;
(b) une première couche ayant une matrice d'électrodes de rangée (16) formées en rangées au travers du substrat (10) dans un premier sens et une deuxième couche ayant une matrice d'électrodes de colonne (12) formées en colonnes au travers du substrat (10) dans un deuxième sens différent du premier sens dans lequel les électrodes de rangée et de colonne (12, 16) se chevauchent pour former des emplacements de pixels ;
(c) une ou plusieurs couche(s) (14) d'une matière électroluminescente formée(s) entre les électrodes de rangée et de colonne (12, 16) pour former une matrice bidimensionnelle (32) de pixels, les pixels (30) étant situés dans les emplacements de pixels ; et
(d) une pluralité de micropuces (20) situées par-dessus le substrat (10) sur une diagonale de la matrice de pixels ou sur une pluralité de diagonales espacées de la matrice de pixels, le nombre de micropuces (20) étant inférieur au nombre de pixels (30), chaque micropuce (20) étant configurée pour contrôler exclusivement un sous-ensemble d'électrodes de rangée (16) et un sous-ensemble d'électrodes de colonne (12), d'où il résulte que les pixels (30) sont configurés pour être contrôlés pour afficher une image,

caractérisé en ce que
chaque micropuce (20) est orientée diagonalement par rapport aux électrodes de rangée et de colonne (12, 16) et a deux rangées de plots de connexion (24), dans lequel une rangée de plots de connexion (24B) est connectée aux électrodes de rangée (16) correspondantes et une rangée de plots de connexion (24A) est connectée aux électrodes de colonne (12) correspondantes.

2. Dispositif d'affichage selon la revendication 1, dans lequel chaque micropuce (20) a un élément de stockage (26) pour au moins chaque pixel (30) auquel elle est connectée dans une rangée ou une colonne de sous-ensemble, l'élément de stockage (26) stockant une valeur représentant une luminance désirée pour chaque pixel (30) et la micropuce (20) utilisant une telle valeur pour contrôler les électrodes de rangée (16) ou les électrodes de colonne (12) connectées au pixel (30).

3. Dispositif d'affichage selon la revendication 1, dans lequel une première micropuce (20A) de la pluralité de micropuces (20) contrôle les électrodes de colonne (12) pour un premier sous-ensemble de pixels et une deuxième micropuce (20B) de la pluralité de micropuces (20) contrôle les électrodes de rangée (16) pour le premier sous-ensemble de pixels.

4. Dispositif d'affichage selon la revendication 3, dans lequel la première micropuce (20A) est configurée pour contrôler à la fois les électrodes de colonne (12) pour un deuxième sous-ensemble de pixels différent du premier sous-ensemble et les électrodes de rangée (16) pour le deuxième sous-ensemble de pixels.

5. Dispositif d'affichage selon la revendication 1, comprenant en outre un contrôleur (40) configuré pour contrôler des signaux transmis aux micropuces (20) par l'intermédiaire d'un ou plusieurs bus (42).

6. Dispositif d'affichage selon la revendication 1, incluant une ou plusieurs connexion(s) de bus en série ou en parallèle électriquement connectée(s) à chaque micropuce.

7. Dispositif d'affichage selon la revendication 6, dans lequel un bus (42) est configuré pour fournir une connexion électrique d'alimentation ou de terre, ou bien un bus (42) est configuré pour transmettre un signal de données ou un signal de contrôle.

8. Dispositif d'affichage selon la revendication 1, incluant en outre un bus (42) de contrôle, dans lequel chaque micropuce (20) a un premier groupe de plots de connexion connectés aux électrodes de rangée et de colonne (12, 16) et un deuxième groupe de plots de connexion connectés au bus de contrôle, dans lequel les premier et deuxième

groupes de plots de connexion sont spatialement séparés.

9. Dispositif d'affichage selon la revendication 8, dans lequel chaque micropuce (20) a un troisième groupe de plots de connexion connectés au bus de contrôle, et dans lequel les premier, deuxième et troisième groupes de plots de connexion sont spatialement séparés.

10. Dispositif d'affichage selon la revendication 8, dans lequel chaque micropuce (20) inclut en outre un troisième groupe de plots de connexion connectés aux électrodes de rangée et de colonne (12, 16), et dans lequel les premier, deuxième et troisième groupes de plots de connexion sont spatialement séparés.

11. Dispositif d'affichage selon la revendication 1, incluant en outre une troisième couche séparée des première et deuxième couches et un bus de contrôle situé dans la troisième couche.

12. Dispositif d'affichage selon la revendication 11, comprenant en outre des plots de connexion espacés ayant un pas formé sur les micropuces et des ouvertures formées de façon à exposer les plots de connexion et dans lequel le bus de contrôle a une première partie qui s'étend à travers les ouvertures jusqu'aux plots de connexion, et une deuxième partie séparée ayant une largeur supérieure au pas des plots de connexion.

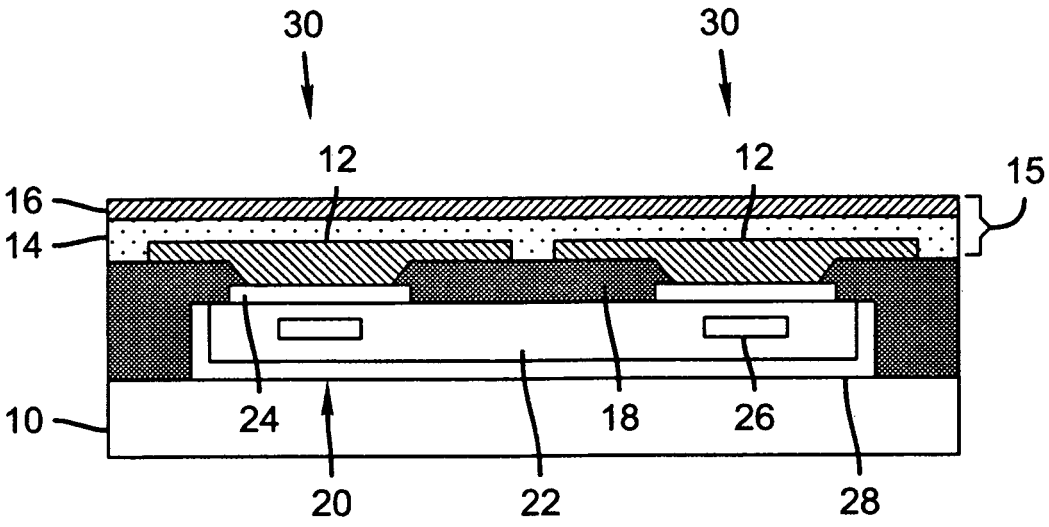
30
30
12
12
15
16
14
10
24
18
26
20
22
28

FIG. 1A

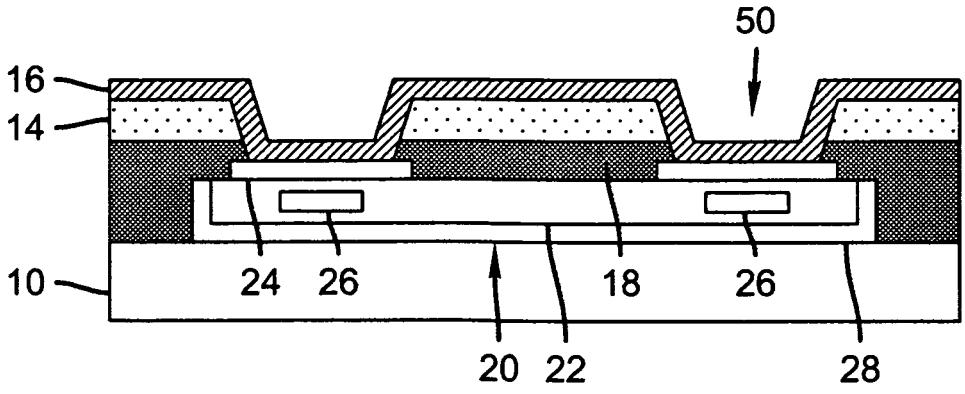
50
16
14
10
24
26
18
26
20
22
28

FIG. 1B

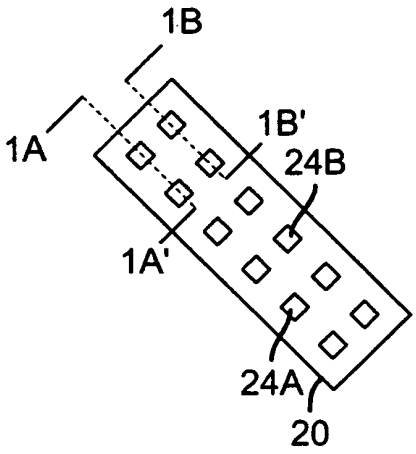

FIG. 2

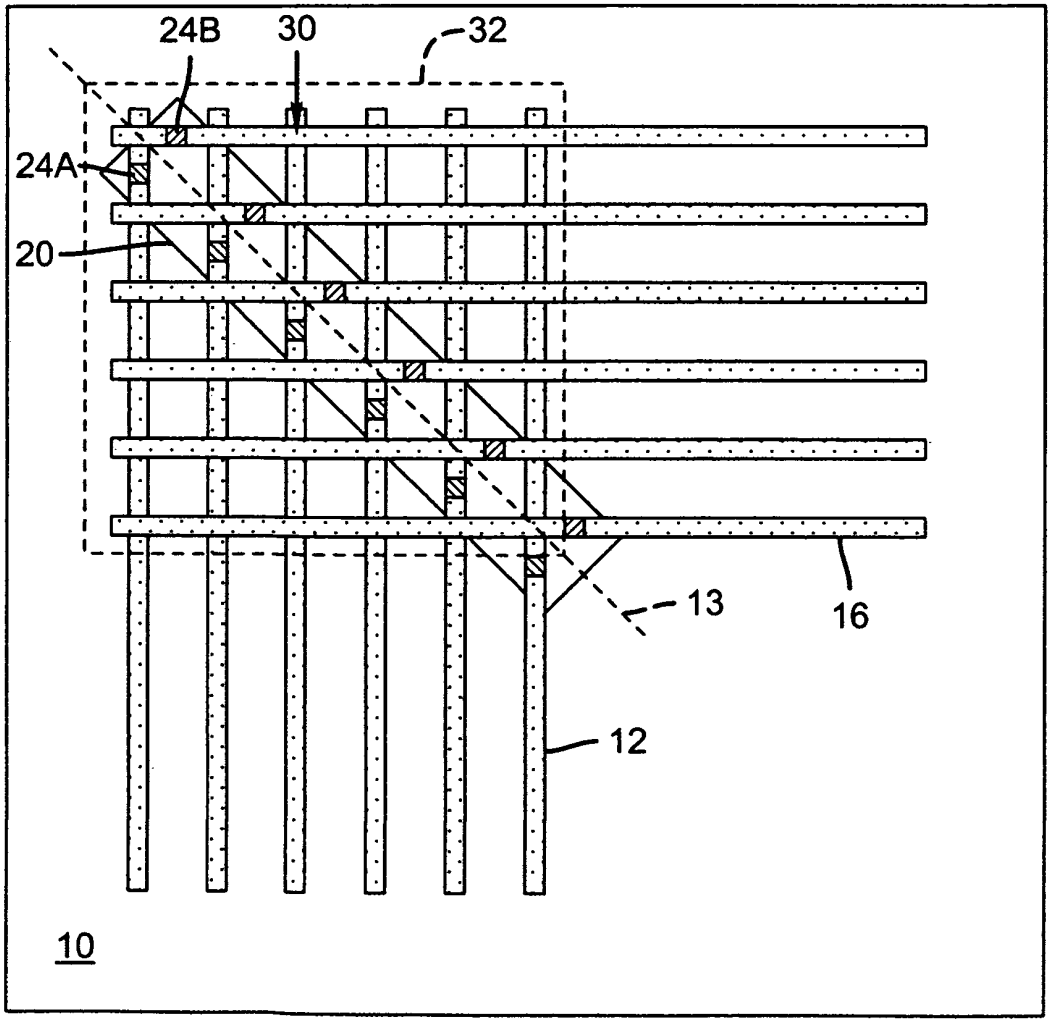

FIG. 3A

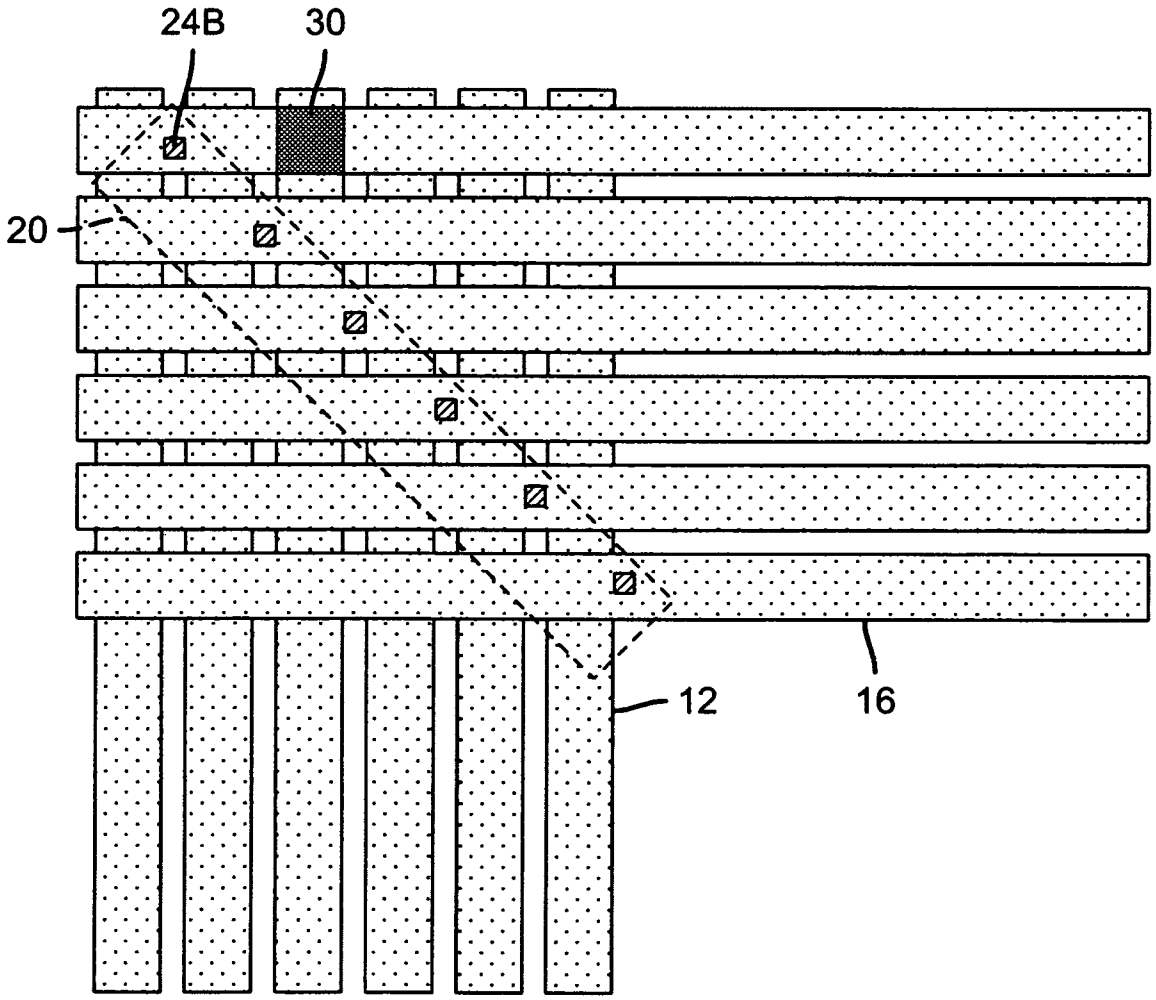

FIG. 3B

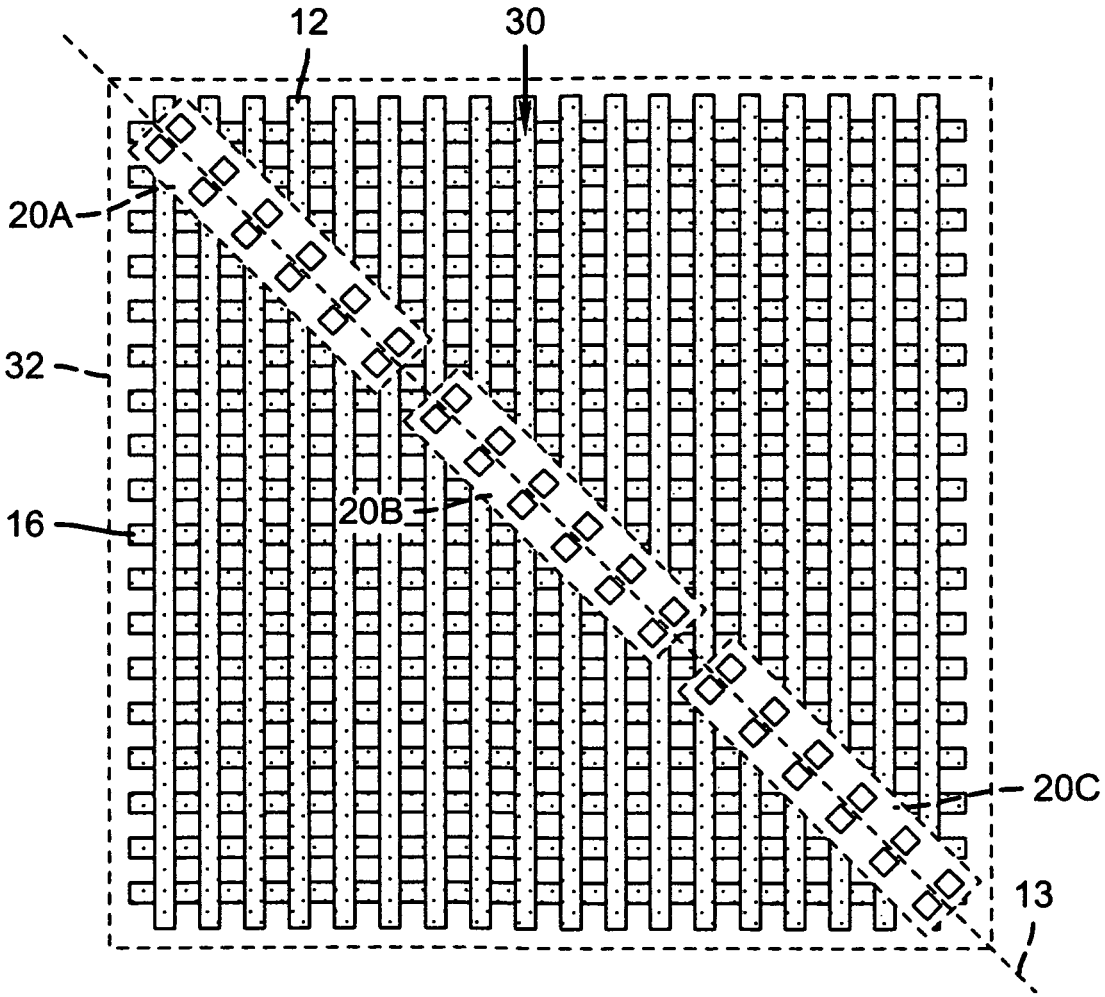

FIG. 4

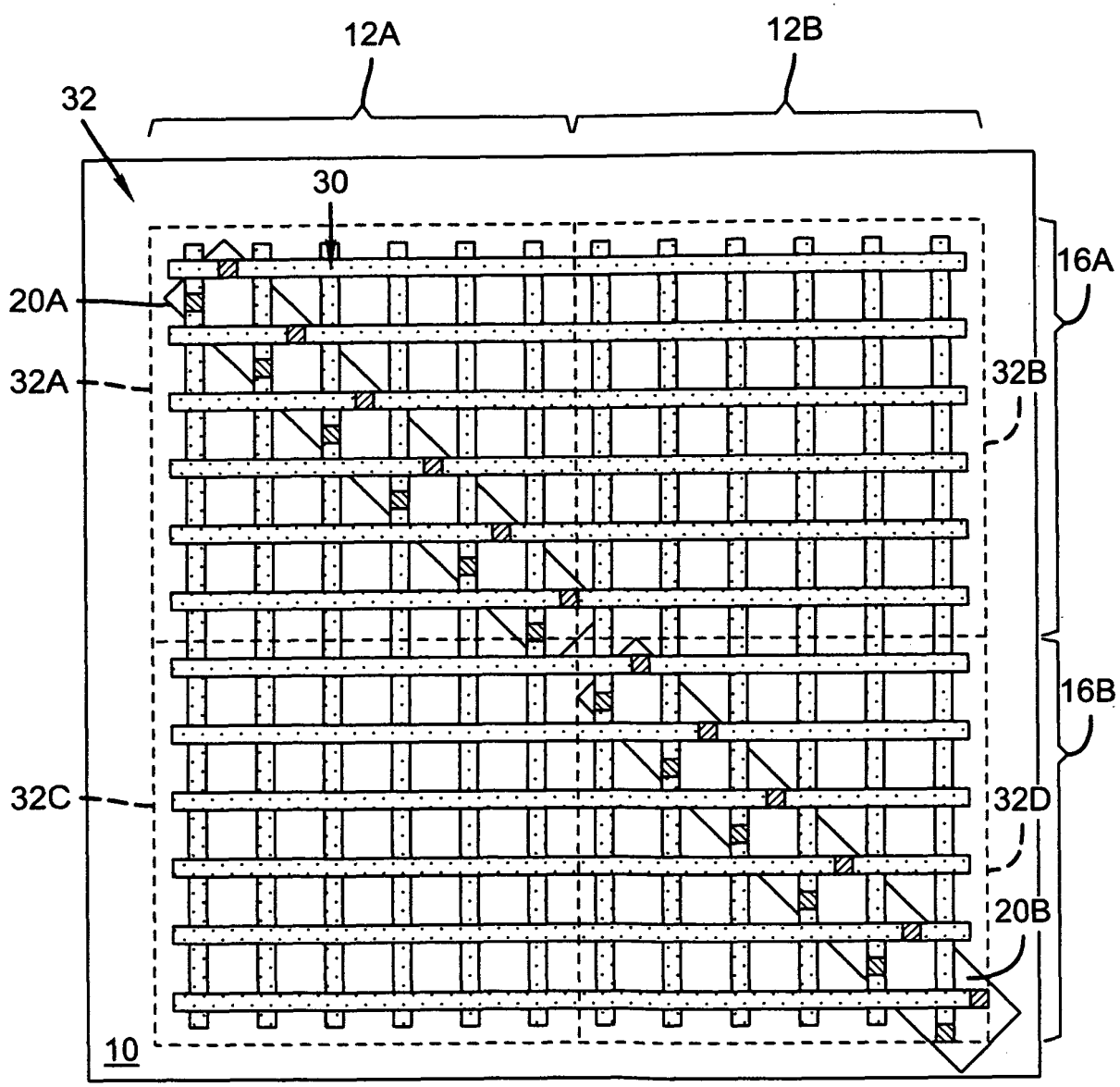

FIG. 5

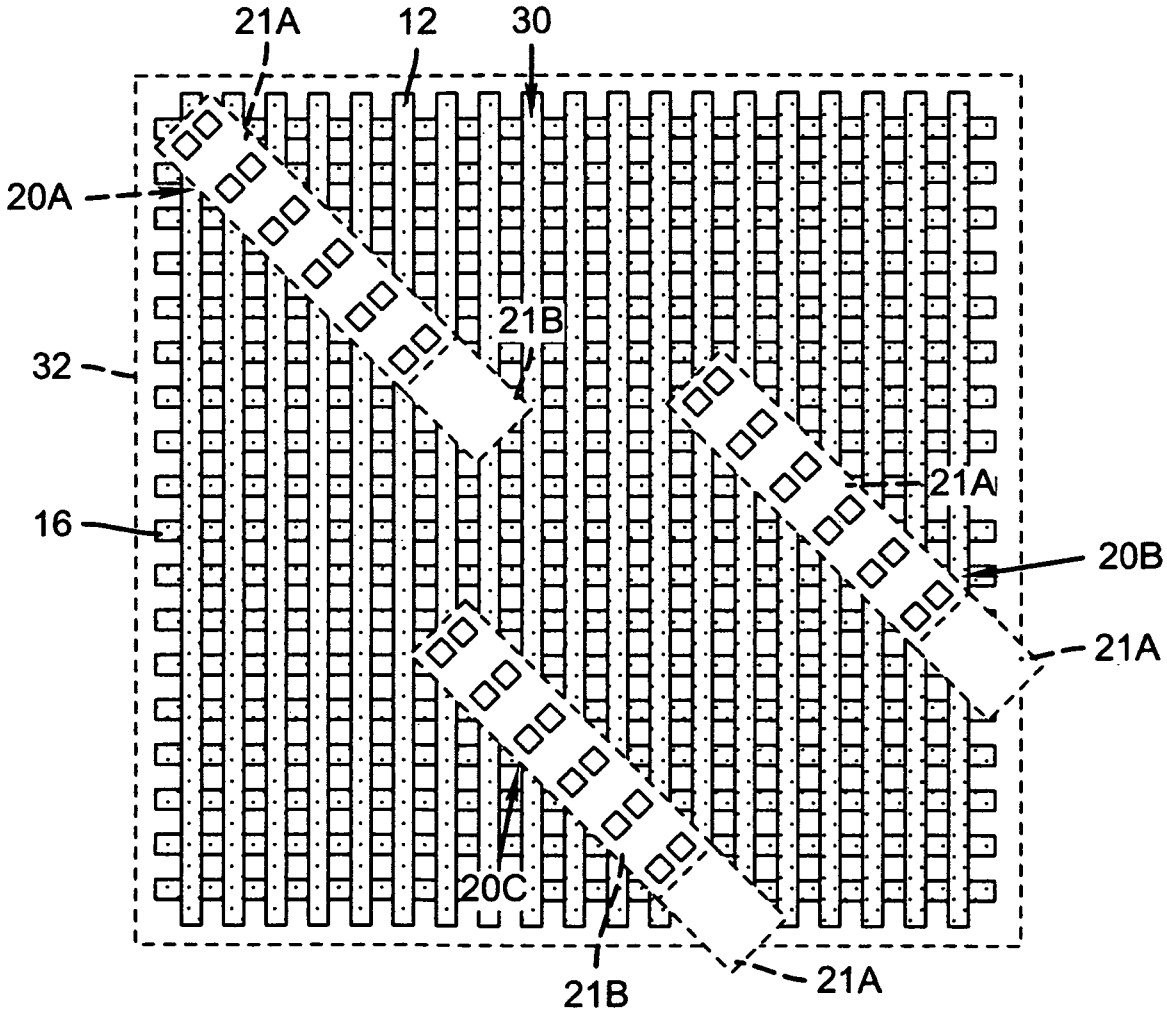

FIG. 6

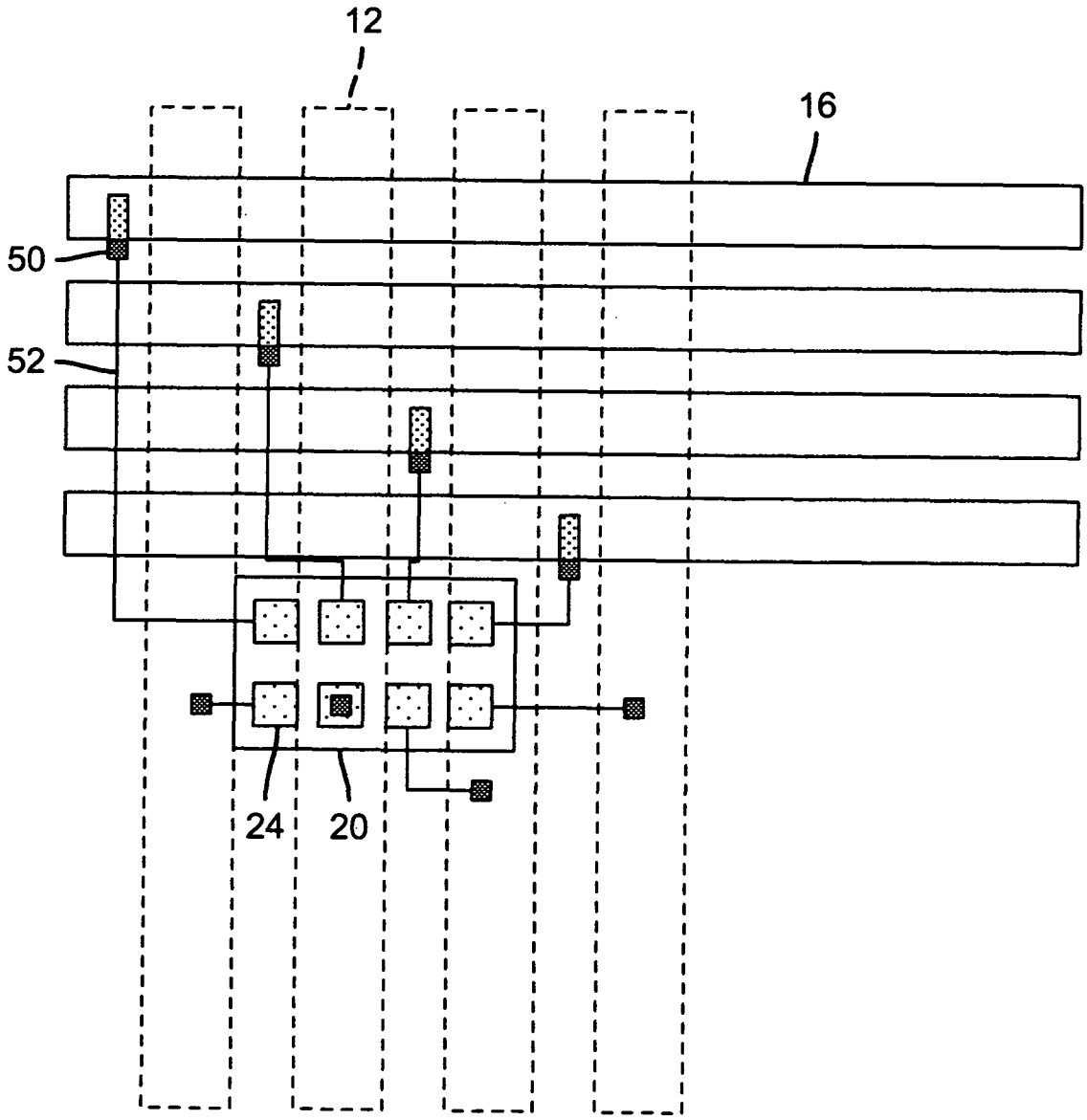

FIG. 7

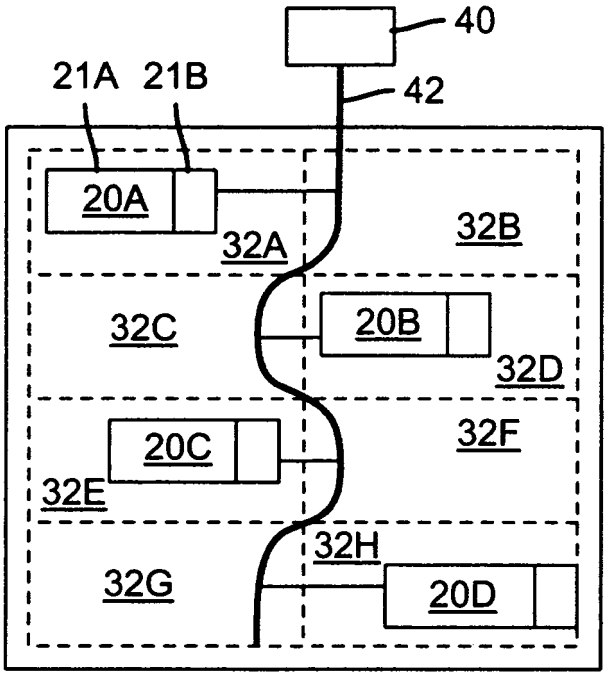
40
21A
21B
42
20A
32A
32B
32C
20B
32D
32F
20C
32E
32H
32G
20D

FIG. 8

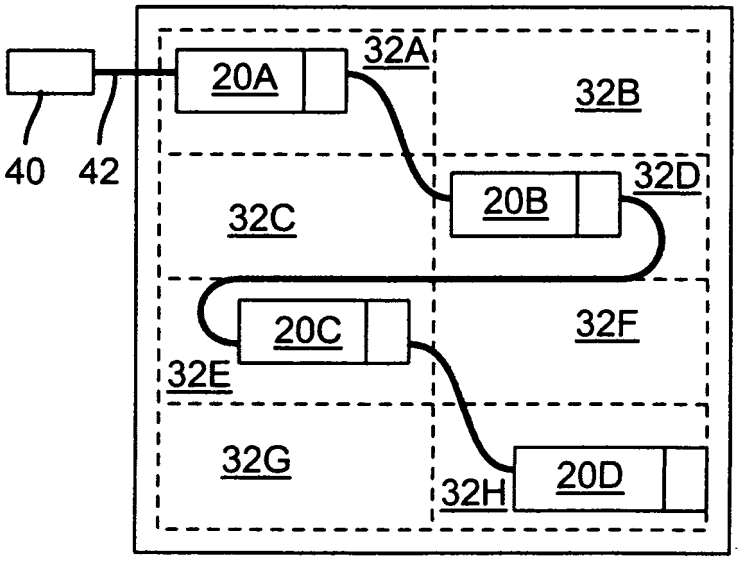
40
42
20A
32A
32B
32C
20B
32D
20C
32F
32E
32G
32H
20D

FIG. 9

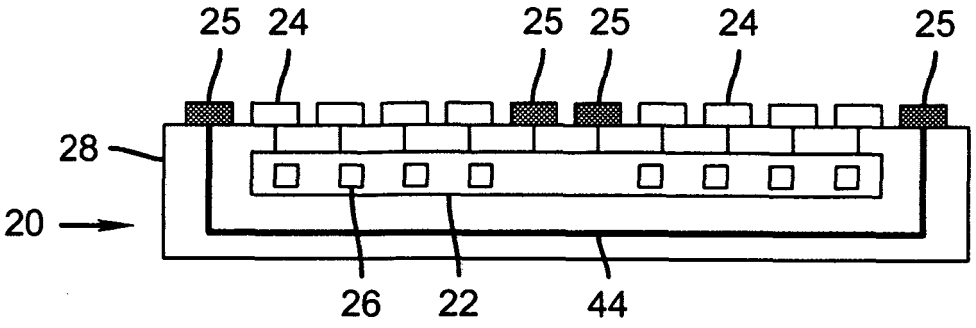

FIG. 10A

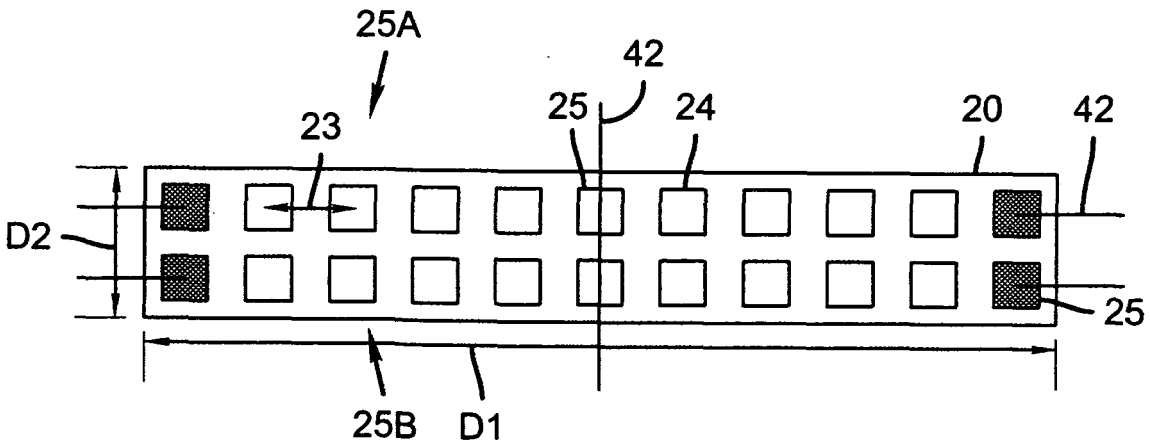

FIG. 10B

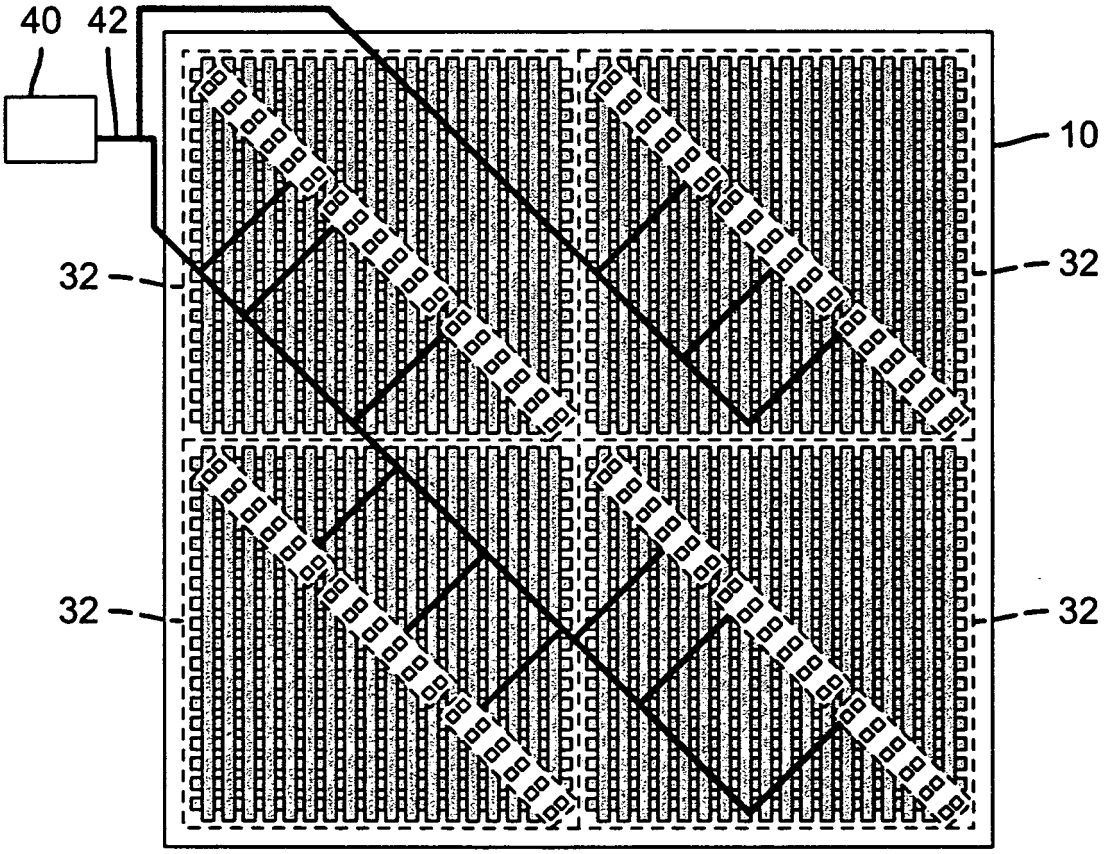

FIG. 11

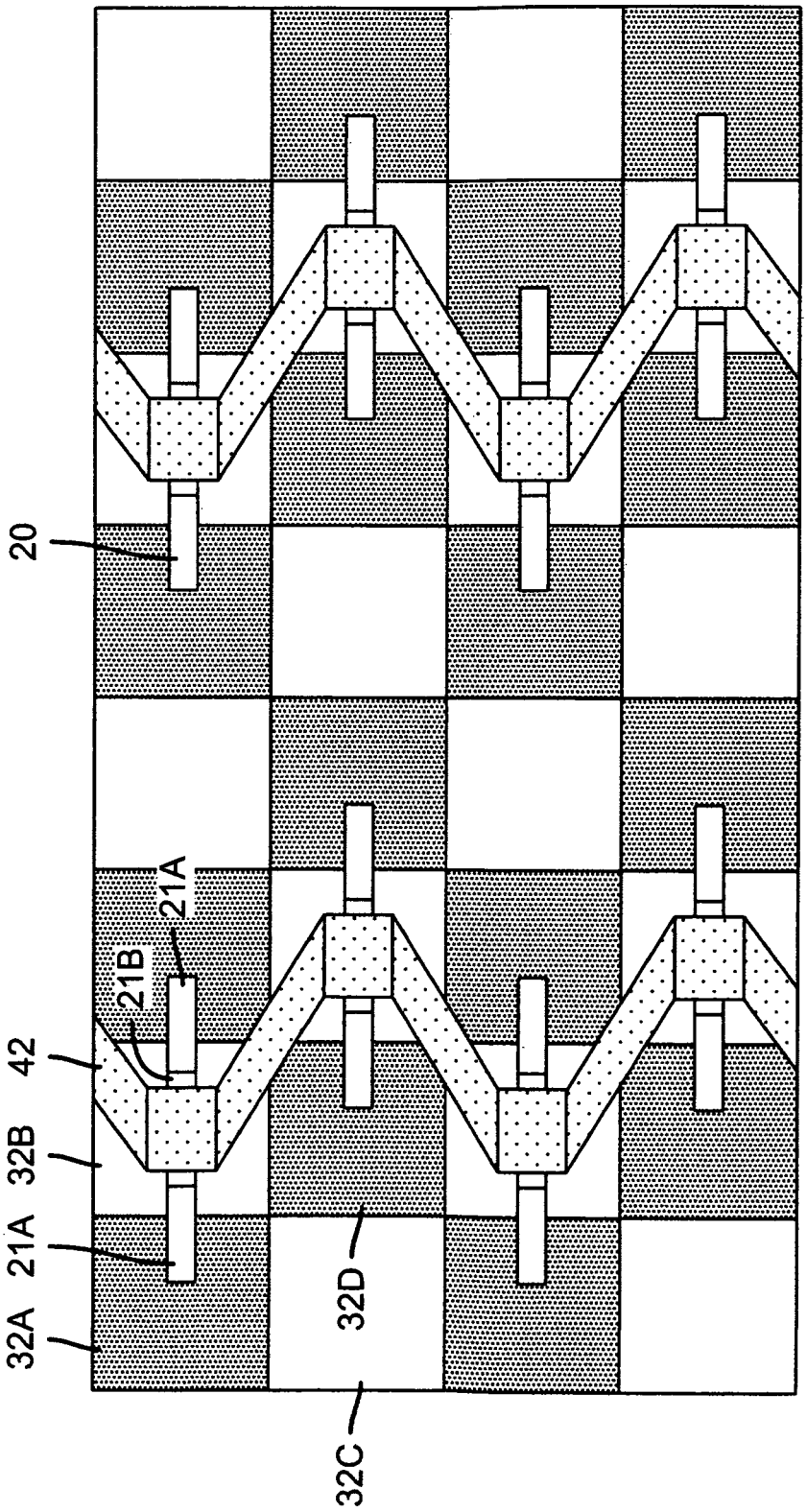

FIG. 12A

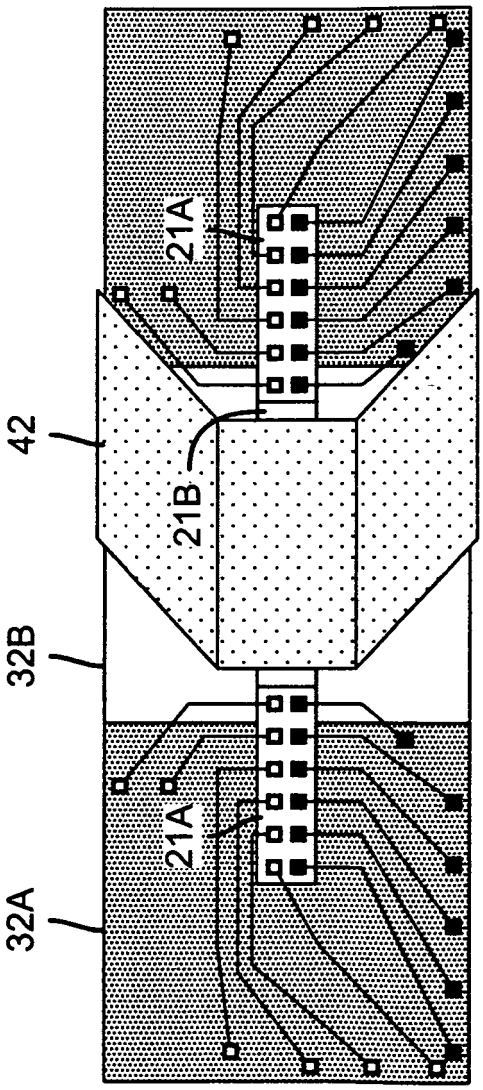

FIG. 12B

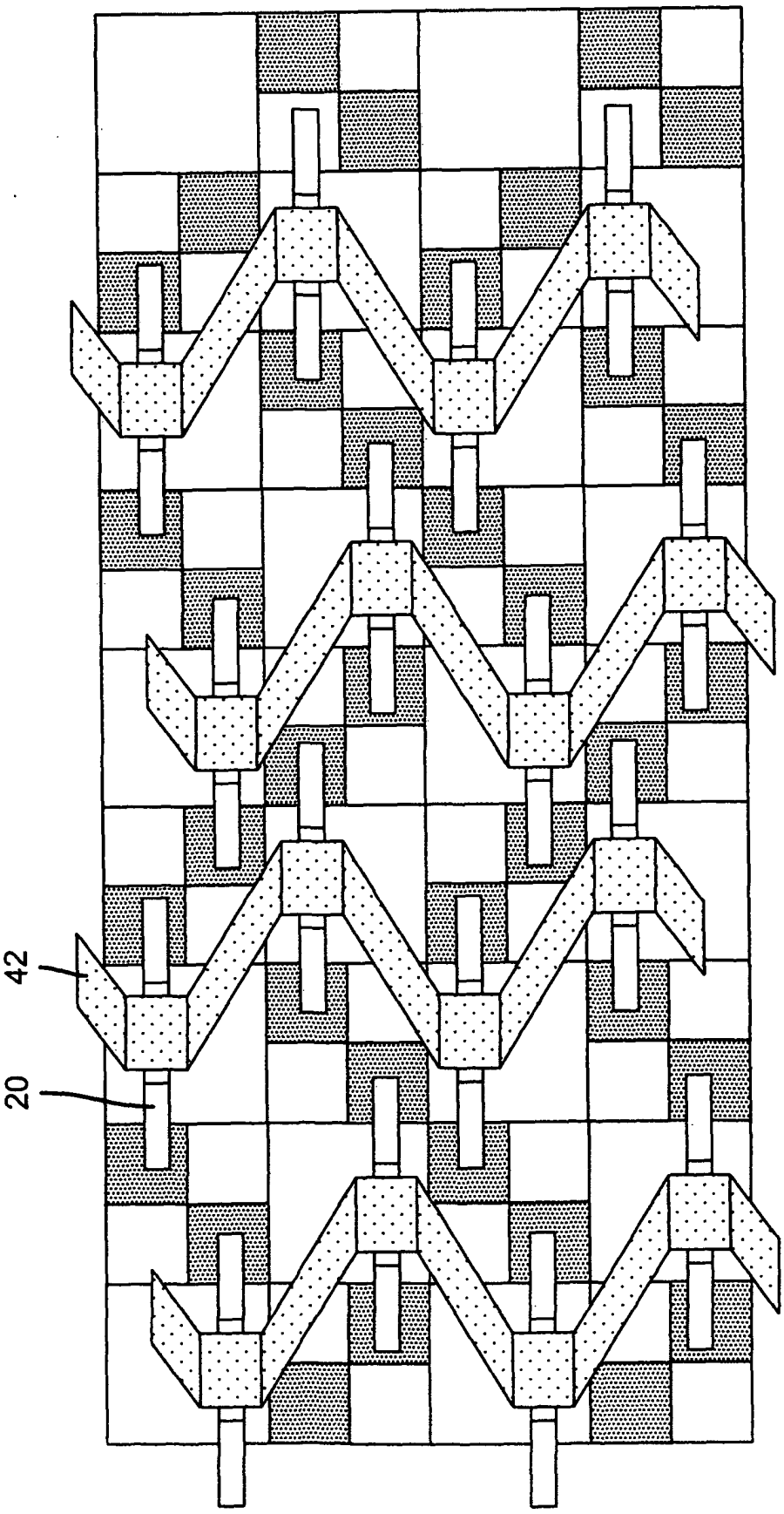

FIG. 13

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	具有小芯片驱动器的显示设备		
公开(公告)号	EP2399253B1	公开(公告)日	2016-08-10
申请号	EP2010704296	申请日	2010-02-12
[标]申请(专利权)人(译)	全球OLED TECH		
申请(专利权)人(译)	全球OLED科技有限责任公司		
当前申请(专利权)人(译)	全球OLED科技有限责任公司		
[标]发明人	COK RONALD S HAMER JOHN W		
发明人	COK, RONALD, S. HAMER, JOHN, W.		
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优先权	12/372906 2009-02-18 US		
其他公开文献	EP2399253A1		
外部链接	Espacenet		

摘要(译)

一种显示装置，包括基板;具有在第一方向上横跨基板成行形成的行电极阵列的第一层和具有在不同于第一方向的第二方向上跨越基板的列形成的列电极阵列的第二层，其中行和列电极重叠以形成像素位置;在行和列电极之间形成一层或多层发光材料以形成二维像素阵列，像素位于像素位置;位于衬底上方的多个小芯片，小芯片的数量小于像素的数量，每个小芯片专门控制行电极的子集和列电极的子集，由此控制像素以显示图像。

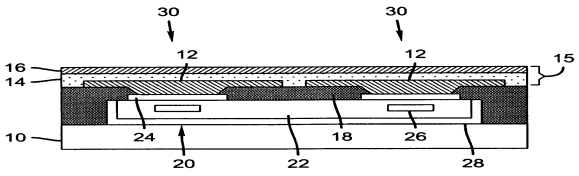

FIG. 1A

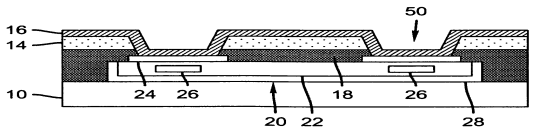

FIG. 1B