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(54) METHOD AND SYSTEM FOR DRIVING LIGHT EMITTING DISPLAY

VERFAHREN UND SYSTEM ZUR ANSTEUERUNG EINER LICHTEMITTIERENDEN ANZEIGE

PROCÉDÉ ET SYSTÈME PERMETTANT DE COMMANDER UN AFFICHAGE ÉLECTROLUMINESCENT

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Description

FIELD OF INVENTION

[0001] The present invention relates to a display system, more specifically to a method and system for driving light emitting displays.

BACKGROUND OF THE INVENTION

[0002] A display device having a plurality of pixels (or subpixels) arranged in a matrix has been widely used in various applications. Such a display device includes a panel having the pixels and peripheral circuits for controlling the panels. Typically, the pixels are defined by the intersections of scan lines and data lines, and the peripheral circuits include a gate driver for scanning the scan lines and a source driver for supplying image data to the data lines. The source driver may include gamma corrections for controlling gray scale of each pixel. In order to display a frame, the source driver and the gate driver respectively provide a data signal and a scan signal to the corresponding data line and the corresponding scan line. As a result, each pixel will display a predetermined brightness and color.

[0003] In recent years, the matrix display has been widely employed in small electronic devices, such as handheld devices, cellular phones, personal digital assistants (PDAs), and cameras. However, the conversional scheme and structure of the source driver and the gate driver demands the large number of elements (e.g., resistors, switchers, and operational amplifiers), resulting that the layout area of the peripheral circuits is still large and expensive.

[0004] Patent application US 2002/080108 describes a gate line driving circuit and driving method for driving gate control lines G_1...G_N, which are evenly divided into L groups. The driving circuit comprises a gate line control logic circuit, a first level shifter module, a second level shifter module and a multiplexer. The multiplexer is used to connect driving lines D_1...D_K to the gate control lines of the selected group, and connect the gate control lines of unselected groups to a predetermined power line. The driving method consists in, at the start, orderly selecting a group in a time frame so that the gate control lines of the selected group are connected to the driving lines D_1...D_K. Next, scanning and driving the K driving lines D_1...D_K of the selected group in a time slot. All the gate control lines of the unselected are connected to a power line VEE.

[0005] Published international patent application WO 2008/057369 A1 describes a data driver, for sequentially supplying image data of each pixel to a display panel having pixels arranged in a matrix layout, for every line, includes a frame memory for storing pixel data having multiple-bits per single pixel in single screen segments; and a structure for converting from multiple-bit pixel data for a single line segment read out in single line units from the frame memory, into single bit pixel data corresponding to a subframe, in single frame units, wherein pixel data for a single line that has been converted to single-bit data by the conversion structure is output simultaneously for a single line.

[0006] Therefore there is a need to provide a display driver that can reduce a driver die area and thus cost, without reducing the driver performance.

SUMMARY OF THE INVENTION

[0007] It is an object of the invention to provide a method and system that obviates or mitigates at least one of the disadvantages of existing systems.

[0008] This object is achieved by the present invention as claimed in the independent claims.

[0009] According to an example, there is provided a display system, which includes: a driver for operating a panel having a plurality of pixels arranged by a plurality of first lines and at least one second line, the driver having: a driver output unit for providing to the panel a single driver output for activating the plurality of first lines, the single driver output being demultiplexed on the panel to activate each first line.

[0010] According to an example, there is provided a display system, which includes: a driver for operating a panel having a plurality of pixels arranged by a plurality of data lines and at least one scan line, the driver having: a shift register unit including a plurality of shift registers; a latch and shift register unit including a plurality of latch and shift circuits for the plurality of shift registers, each storing an image signal from the corresponding shift register or shifting the image signal to a next latch and shift circuit; and a decoder unit including at least one decoder coupled to one of the latch and shift circuits, for decoding the image signal latched in the one of the latch and shift circuit to provide a driver output.

[0011] According to an example, there is provided a display system, which includes: a driver for operating a panel having a plurality of pixels, the driver having: a plurality of multiplexers for a plurality of offset gamma curve sections, each offset gamma curve section having a first range less than a second range of a main gamma curve, at least one of offset gamma curve sections being offset by a predetermined voltage from a corresponding section of the main gamma curve; a plurality of decoders for the plurality of multiplexers; and an output buffer for providing a driver output based on the output from the decoder and the predetermined voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

Figure 1A illustrates a gate driver and a panel for a

display system;

Figure 1B illustrates an example of the gate driver and the panel of Figure 1A;

Figure 2 illustrates a timing chart for operating the display system of Figures 1A-1B;

Figure 3A illustrates another example of a gate driver and a panel for a display system;

Figure 3B illustrates an example of the gate driver and the panel of Figure 3A;

Figure 4 illustrates a timing chart for operating the display system of Figures 3A-3B;

Figure 5 illustrates an example of a source driver and a panel for a display system;

Figure 6 illustrates an example of operation for the display system having RGB pixel structure;

Figure 7 illustrates a further example of a source driver and a panel for a display system;

Figure 8 illustrates a further example of a source driver and a panel for a display system having RGBW pixel structure;

Figure 9 illustrates an example of subpixel configuration for RGBW pixel stricture;

Figure 10 illustrates a further example of a source driver, external gamma and a panel for a display system;

Figure 11 illustrates a further example of a source driver and a panel for a display system;

Figure 12 illustrates a further example of a source driver and a panel for a display system;

Figure 13 illustrates a source driver for a conventional display system;

Figure 14 illustrates a further example of a source driver for a display system;

Figure 15 illustrates a further example of a source driver for a display system;

Figure 16A illustrate an example of a gamma curve and 16B illustrate an example of a segmented offset gamma curve;

Figure 17 illustrates an example of a display system having the gate driver of Figure 1A or 3A;

Figure 18 illustrates an example of a display system having the source driver of Figures 5-12; and

Figure 19 illustrates an example of a display system having the source driver of Figures 14-15.

DETAILED DESCRIPTION

[0013] One or more currently preferred embodiments have been described by way of example. It will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

[0014] Embodiments in this disclosure are described using a panel having pixels that are coupled to at least first line and at least one second line (e.g., scan lines and data lines) and being operated by a driver. The driver may be a driver IC having a plurality of pins, e.g., source driver ICs, gate driver ICs. The panel may be, for example, but not limited to, a LCD or LED panel. The panel may be a color panel or a monochrome panel.

[0015] In the description below, the terms "source driver" and "data driver" are used interchangeably, and the terms "gate driver" and "address driver" are used interchangeably. In the description below, the terms "row", "scan line" and "address line" may be used interchangeably. In the description below, the terms "column", "data line" and "source line" may be used interchangeably. In the description below, the terms "pixel" and "subpixel" may be used interchangeably.

[0016] Referring to Figures 1A-1B, there is illustrated a system 100 having a gate driver 102 and a panel 110 having pixels arranged in rows and columns. The system 100 includes a mechanism for multiplexing (muxing) gate driver outputs based on frequency reduction. In Figure 1A, "fv" represents the vertical frequency of the display (or row frequency), and "M" is the number of muxing blocks. In Figure 1B, "Cell #i" represents an address cell 106, and "SEL k" (k=(i-1)*M+1, (i-1)*M+2, ..., (i-1)*M+M+1, i*M) represents a row or a scan line coupled to the row of the panel 110. A pixel in the row is selected by the scan line. The address cell 106 may be a logic or a flip-flop in a shift register chain to output a gate output.

[0017] The gate driver 102 includes a driver output unit 104 having at least one address cell 106 (Cell #i). The address cell 106 provides a single gate driver output 108 which is shared by M rows. An individual gate driver output 108 from the gate driver 102 is active for M rows. On the panel side 110, a demultiplexer 112 ("1:M Demuxs" in Figure 1A) is employed for M rows. The input of the demultiplexer 112 is coupled to the gate driver output 108, and the outputs of the demultiplexer 112 are coupled to M rows. In this example, the demultiplexer 112 is coupled to scan lines SEL (i-1)*M+1, SEL (i-1)*M+2, ..., and SEL i*M. The activated gate driver output 108 from the address cell 106 (Cell #i) is assigned to each individual row in sequence, via the demultiplexer 112.

[0018] The demultiplexer 112 is implemented using,

for example, thin film transistors, on the panel 110. The demultiplexer 112 includes a plurality of switch blocks for activating M rows. In Figure 1B, switches 116 (SET #1, SET #2, ..., SET #M) are shown as an example of the components of the demultiplexer 112. The switch block 116 (SET #k: k=1, 2, ..., M) is employed for the scan line SEL (i-1)*M+k. Each switch block 116 includes a pair of switches, one being capable of connecting the gate driver output 108 to the corresponding scan line and the other being capable of connecting VGL to the corresponding scan line. VGL may be a ground level voltage. Each scan line SEL (i-1)*M+k turns to be on the VGL level or the activated gate driver output 108 via the corresponding switch block 116 (SET #k). Each switch block 116 (SET #k) is controlled by the corresponding control signal CTRL (k). In Figure 3B, the scan line SEL (i-1)*M+k is selected (becomes active) by the control signal CTRL (k). By operating the demultiplexer 112 with the control signals CTRL (1)-CTRL (M), the number of the gate driver outputs and address cells is reduced by a factor of M.

[0019] In Figure 1B, one address cell 116 is shown as an element of the driver output unit 104; however, the number of the address cells may vary. In Figure 1B, M rows (scan lines) are shown; however, the panel 110 may include a plurality of groups of rows where the ith group has M rows and is operated by the ith address cell (Cell #i). One of ordinary skill in the art would appreciate that the gate driver 102 and the panel 110 may include components not shown in the Figures 1A-1B.

[0020] Referring to Figures 1A, 1B and 2, the operation of a display having the gate driver 102 and the panel 110 is described. Each of the controlling signals CTRL (1) - CTRL (M) for controlling the demultiplexing on the panel 110 works at the normal gate frequency. When the display programming reaches the row SEL (i-1)*M+1, the control signal CTRL (1) for that row is high, resulting that the address cell 106 for the ith block (Cell #i) of rows is connected to SEL (i-1)*M+1. Thus, that row SEL (i-1)*M+1 is selected and the image data can be written in the pixels of the row.

[0021] After the programming of the row SEL (i-1)*M+1, the next control signal CTRL (2) is high, resulting that the next row SEL (i-1)*M+2 becomes active. This continues till the entire display is programmed (end of a frame).

[0022] If a row is not active, the control signal related to that row is low or the address cell related to that row is not active. Thus, the row is connected to VGL which will disconnect the pixels in that row from the gate driver 102.

[0023] Referring to Figures 3A-3B, there is illustrated a system 130 having a gate driver 132 and a panel 140 having pixels arranged in rows and columns. The system 130 has a mechanism for reducing the number of gate driver outputs and reducing the operation frequency of demultiplexing control signals on the panel side. In Figure 3A, "fv" represents the vertical frequency of the display (or row frequency). In Figure 3B, "Cell #j" (j=i, i+1, i+2, i+3) represents an address cell, and "SEL k" (k=i, i+1, i+2, i+3) represents a row or a scan line coupled to the row of the panel 140. A pixel in the row is selected by the scan line. The address cell may be a logic or a flip-flop in a shift register chain to output a gate output.

[0024] In the system 130, gate driver output signals are multiplexed on the gate driver 132 side, and the outputs from the gate driver 132 are demultiplexed on the panel 140 side.

[0025] The gate driver 132 includes a driver output unit 133 having a plurality of multiplexers for a plurality of address cells. Each address cell provides a gate driver signal, and each multiplexer multiplexing the gate driver signals and outputs a single gate driver output. In Figure 3B, four address cells 138a-138d (Cell #i, Cell #i+1, Cell #i+2, and Cell #i+3) are shown as an example of the address cells in the gate driver 132. In Figure 3B, two multiplexers 134a and 134b are shown as an example of multiplexing the gate driver signals. The multiplexers 134a and 134b are controlled by a control signal iCTRL. The multiplexer 134a is coupled to the address cells 138a and 138c (Cell #i and Cell #i+2) and outputs a gate output signal 136a that corresponds to either address cell 138a or 138c (Cell #i or Cell #i+2). The multiplexer 134b is coupled to the address cells 138b and 138d (Cell #i+1 and Cell #i+3) and outputs a gate output signal 136b that corresponds to either address cell 138b or 138d (Cell #i+1 or Cell #i+3).

[0026] The panel 140 includes a multiplexer 142 ("1:M Demuxs" in Figure 3A) coupling to the gate driver outputs and a plurality of rows. The demultiplexer 142 is implemented using, for example, thin film transistors, on the panel 140. The demultiplexer 142 includes a plurality of switch group blocks, each coupling to the gate driver multiplexers. In Figure 3B, two switch group blocks 146a and 146b (SET #1 and SET #2) are shown as an example of the components of the demultiplexer 142. On the panel side 140, the activated gate driver outputs 136a and 136b are assigned of the switch group blocks 146a and 146b.

[0027] Each switch group block in the panel 140 includes a plurality of switch blocks 148. In Figure 3B, each of the switch group blocks 146a and 146b includes two switch blocks 148, one being capable of coupling one gate driver output 136a to one scan line and the other being capable of coupling the other gate driver output 136b to the other scan line. The switch block 148 includes a pair of switches, one being capable of coupling the gate driver output to the corresponding scan line and the other being capable of coupling VGL to the corresponding scan line. VGL may be a ground level voltage. The switch block 148 in the switch group block (SET #k: k=1, 2, ...) is controlled by the corresponding control signal CTRL (k). Each scan line turns to be on the VGL level or the corresponding activated gate driver output 136a or 136b via the corresponding switch block 148. In Figure 3B, the scan lines SEL (i) and SEL (i+1) are selected (become active) by the control signal CTRL (1), and the scan lines SEL (i+2) and SEL (i+3) are selected (become active) by

the control signal CTRL (2).

[0028] In Figure 3B, the multiplexing (muxing) and demultiplexing (demuxing) operations are executed for two rows, however, the multiplexing and demultiplexing operations may be executed for more than two rows. In Figure 3B, four address cells are shown as an element of the driver output unit 133; however, the number of the address cells is not limited to four and may vary. In Figure 3B, rows (scan lines) are divided into two groups, each having two rows; however, the number of groups and the number of rows in each group are not limited to two and may vary. One of ordinary skill in the art would appreciate that the gate driver 132 and the panel 140 may include components not shown in the Figures 3A-3B.

[0029] In this structure, the physical multiplexing is used at the gate driver side 132. As a result, the number of address cells remains the same while the number of gate driver outputs is reduced by a factor of multiplexing blocks. The number of rows in each set (SET #k) can be increased for further reduction in output of the gate driver and the frequency of the control signals. Since multiple gate driver outputs can be active, the operation frequency of the demultiplexing control signals is reduced.

[0030] Referring to Figures 3A, 3B and 4, the operation of a display having the gate driver 132 and the panel 140 is described. When the display programming reaches the rows SEL (i) and SEL (i+1), the control signal CTRL (1) for those rows is high (150), resulting that the gate driver output 136a is coupled to the row SEL (i) and the gate driver output 136b is coupled to the row SEL (i+1). At this period (150), the control signal iCTRL is in one state (e.g., low). The gate driver output 136a corresponds to the output from the address cell 138a (Cell #i) and the gate driver output 136b corresponds to the output from the address cell 138b (Cell #i+1). The image data can be written in the pixels of the selected rows SEL (i) and SEL (i+1).

[0031] After the programming of the rows SEL (i) and SEL (i+1), the next control signal CTRL (2) is high (152), resulting that the next rows SEL (i+2) and SEL (i+3) become active. At this period (152), the control signal iCTRL is in the other state (e.g., high). The gate driver output 136a corresponds to the output from the address cell 138c (Cell #i+2) and the gate driver output 136b corresponds to the output from the address cell 138d (Cell #i+3). The image data can be written in the pixels of the selected rows SEL (i+2) and SEL (i+3). This continues till the entire display is programmed (end of a frame).

[0032] If a row is not active, the control signal related to that row is low or the address cell related to that row is not active. Thus, the row is connected to VGL which will disconnect the pixels in that row from the gate driver 132.

[0033] Referring to Figure 5, there is illustrated a system 160 having a source driver 162 and a panel 180 having subpixels for RGB. Most of light emitting displays employ different gammas (or gamma corrections) for different subpixels, which use different decoders for different outputs. In the system 160, gammas (gamma corrections, gamma voltages) are multiplexed on the source driver 162 side. In the description, the terms "gamma", "gamma correction" and "gamma voltages" may be used interchangeably. One of ordinary skill in the art would appreciate that the source driver 162 and the panel 180 may include components not shown in Figure 5.

[0034] The source driver 162 includes a driver output unit 164 having a CMOS multiplexer 166 and a CMOS digital to analog converter (DAC) 170. The multiplexer 166 multiplexes a Red gamma correction 168a, a Green gamma correction 168b and a Blue gamma correction 168c. The DAC 170 includes a decoder. In the description, the terms "DAC" and "DAC decoder" may be used interchangeably.

[0035] Each of the gamma corrections 168a, 168b and 168c provides a reference voltage to the DAC 170. The reference voltage is selected based on the dynamic range of the DAC decoder 170. The reference voltage at the gamma correction block may be generated using, for example, resistors, or be stored using, for example, registers.

[0036] The output from the multiplexer 166 is provided to the DAC 170. The multiple gammas share one decoder in the DAC 170. The DAC decoder 170 operates on an output from a multiplexer 172. The multiplexer 172 multiplexes a Red register (reg) 174a for storing image data for Red, a Green register (reg) 174b for storing image data for Green, and a Blue register (reg) 174c for storing image data for Blue. The CMOS DAC 170 provides a single source driver output 174.

[0037] A demultiplexer 182 is employed on the panel 180 side to demultiplex the driver output 174 from the source driver 162. The demultiplexer 182 is implemented using, for example, thin film transistors, on the panel 180. The outputs from the demultiplexer 182 are couples to three data lines. The driver output 174 is demultiplexed 182 on the panel 180 side and goes to different subpixels (i.e., Red subpixel, Blue subpixel and Green subpixel).

[0038] In the system 160, the output of the source driver 162 is multiplexed to reduce the number of driver pins and demultiplexed at the panel 180. To further improve the size of the driver area, the multiplexing is executed at few stage earlier at the gamma selection and DAC inputs. For example, when, the Red pixels are being programmed at the panel 180, the Red data (Red register 174a) and the red gamma 168a are assigned to the DAC 170.

[0039] The multiplexers 166 and 172 may be controlled by a color selection control signal ColorSel. The demultiplexer 182 may be controlled by the control signal ColorSel or a control signal associated with the multiplexing control signal ColorSel.

[0040] As shown in Figure 6, the Red pixels, Green pixels and Blue pixels may be programmed sequentially. It will be appreciated by one of ordinary skill in the art that the programming sequence is not limited to that of Figure 6, and is changeable by using the color selection control signal.

[0041] Generally, the output range of the voltage required for the light emitting displays is high and thus source drivers are to be a rail-to-rail design for the power. Currently, this results in using multiple CMOS decoders, leading to a larger area source driver. Referring to Figure 7, there is illustrated a system 190 having a source driver 192 and a panel 220 having subpixels for RGB. In this system 190, multiple gammas (gamma corrections, gamma voltages) are multiplexed and a DAC is divided into separate NMOS and PMOS components, resulting in that the source driver 192 area is reduced. One of ordinary skill in the art would appreciate that the source driver 192 and the panel 220 may include components not shown in Figure 7.

[0042] The source driver 192 includes gamma corrections for Red, Blue and Green, each providing a reference voltage to a DAC decoder. The reference voltage is selected based on the dynamic range of the decoder. The reference voltage may be generated using, for example, resistors, or be stored using, for example, registers. Each gamma correction has a high voltage level gamma correction (high voltage level of gamma corrections) and a low voltage level gamma correction (low voltage level of gamma corrections). The high voltage level of gamma corrections is a level from a predefined reference voltage to the high point of the driver output, and the low voltage level of gamma corrections is a level from the predetermined reference voltage to the beginning of the gamma voltage. The predetermined reference voltage may be at the middle for the driver output range. For example, if the driver range is 10V, the predetermined reference voltage is 5V; the high voltage level of gamma corrections is 5 to 10V; and the low voltage level of gamma corrections is 0 to 5V.

[0043] The source driver 192 includes a driver output unit 194 having a PMOS multiplexer 196 for the high voltage level of gamma corrections, and a NMOS multiplexer 200 for the low voltage level of gamma corrections. In Figure 7, the multiplexer 196 multiplexes a high Red gamma correction 198a, a high Green gamma correction 198b and a high Blue gamma correction 198c, and the multiplexer 200 multiplexes a low Red gamma correction 202a, a low Green gamma correction 202b and a low Blue gamma correction 202c.

[0044] The driver output unit 194 includes a DAC that is divided into separate components: a PMOS component 204 ("PMOS DAC" in Figure 7) and a NMOS component 206 ("NMOS DAC" in Figure 7). The PMOS component 202 includes a PMOS decoder and receives the output from the multiplexer 196. The NMOS component 206 includes a NMOS decoder and receives the output from the multiplexer 200. The reference voltage from the gamma correction is selected based on the dynamic range of the NMOS and PMOS decoders in the components 204 and 206. The PMOS and NMOS decoders in the components 204 and 206 operate on an output from a multiplexer 208 for multiplexing a Red register 210a, a Green register 210b, and a Blue register 210c. The registers 210a, 210b and 210c correspond to the resisters 174a, 174b and 174c of Figure 5, respectively. The multiplexers 196, 200 and 208 are controlled by a color selection control signal ColorSel.

[0045] The driver output unit 194 includes a CMOS multiplexer 212 for multiplexing the outputs from the PMOS and NMOS components 204 and 206. The multiplexer 212 is operated by an output from a multiplexer 214. The multiplexer 214 multiplexes bit signals R[j], G[i], and B[k], based on the color selection control signal ColorSel. R[j] (G[i], B[k]) is a bit that defines when to use which part of the gamma for Red (Green, Blue). The bit R[j] (G[i], B[k]) is generated based on the Red register 210a (210b, 210c) and predefined data about the gamma curve for Red (Green, Blue), e.g., gamma values. The multiplexer 212 outputs a single source driver output 216.

[0046] When the bit signal R[j] is active and the other signals are not active, the source driver 192 outputs the driver output 216 based on either the high Red gamma correction or the low Red gamma correction.

[0047] A demultiplexer 222 is employed on the panel 220 side to demultiplex the source driver output 216. The demultiplexer 222 corresponds to the demultiplexer 182 of Figure 5. The demultiplexer 222 is implemented using, for example, thin film transistors, on the panel 220. The outputs from the demultiplexer 222 are couples to three data lines. The demultiplexer 222 may be controlled by the control signal ColorSel or a control signal associated with the multiplexing control signal ColorSel. Based on the output from the demultiplexer 222, one of three data lines is active. The driver output 216 is demultiplexed 222 on the panel 220 side and goes to different subpixels (i.e., Red subpixel, Blue subpixel, Green subpixel).

[0048] Based on the image data, one of the low gamma correction and the high gamma correction is selected. For example, if the high voltage level of gamma corrections is 5 to 10V, the low voltage level of gamma corrections is 0 to 5V, and the image data requires 6 V, the high end of gamma correction will be selected.

[0049] Based on the color selection control signal ColorSel, the Red pixels, Green pixels and Blue pixels may be programmed sequentially, similar to that of Figure 6. It will be appreciated by one of ordinary skill in the art that the programming sequence is not limited to that of Figure 6, and is changeable by using the color selection control signal.

[0050] Instead of using a CMOS decoder that has twice as many transistors as a PMOS or NMOS decoder for the entire range the output voltage, the PMOS decoder 204 is used for the higher range and the NOMS decoder 206 for the lower range of the voltage. Thus, the area will be reduced by using twice less transistors.

[0051] Referring to Figure 8, there is illustrated a system 230 having a source driver 232 and a panel 270 having subpixels. The system 230 is applied to quad RGBW pixel structure. Multiple gamma corrections for White, Green, Blue and Red are multiplexed in the source driver 232. In the source driver 232, four different gamma

corrections are generated (White, Green Blue and Low) for each of high voltage level and low voltage level. One of ordinary skill in the art would appreciate that the source driver 232 and the panel 270 may include components not shown in Figure 8.

[0052] The source driver 232 includes gamma corrections for White, Green, Blue and Red, each providing a reference voltage to a DAC decoder. The gamma correction may be generated using, for example, resistors, or be stored using, for example, registers. Each gamma correction has a high voltage level gamma correction (high voltage level of gamma corrections) and a low voltage level gamma correction (low voltage level of gamma corrections). As described above, the high voltage level of gamma corrections is a level from the reference voltage to the reference voltage to the high point of the driver output, and the low voltage level of gamma corrections is a level from the reference voltage to the beginning of the gamma voltage.

[0053] The source driver 232 includes a driver output unit 270 having PMOS multiplexers 240a and 240b for high voltage level of gamma corrections, and NMOS multiplexers 244a and 244b for low voltage level of gamma corrections. The multiplexer 240a multiplexes a high White gamma correction 242a and a high Green gamma correction 242b, and the multiplexer 240b multiplexes a high Blue gamma correction 242c and a high RED gamma correction 242d. The multiplexer 244a multiplexes a low White gamma correction 246a and a low Green gamma correction 246b, and the multiplexer 244b multiplexes a low Blue gamma correction 246c and a low RED gamma correction 246d.

[0054] The driver output unit 270 includes a PMOS multiplexer 248 for multiplexing the outputs from the PMOS multiplexers 240a and 240b, and a NMOS multiplexer 250 for multiplexing the outputs from the NMOS multiplexers 244a and 244b. Based on the image data and a color selection, one of the low gamma correction and the high gamma correction for the selected color is selected.

[0055] The driver output unit 270 includes a DAC that is divided into separate components; a PMOS component 252 ("PMOS DAC" in Figure 8) for the high voltage level of the gamma corrections and a NMOS component 254 ("NMOS DAC" in Figure 8) for the low voltage level of the gamma corrections. The PMOS component 252 includes a PMOS decoder and receives the output from the multiplexer 248. The NMOS component 254 includes a NMOS decoder and receives the output from the multiplexer 250. The reference voltage from the gamma correction is selected based on the dynamic range of the NMOS and PMOS decoders in the components 252 and 254.

[0056] The PMOS and NMOS decoders in the components 252 and 254 operate on an output from a multiplexer 256 for multiplexing a White/Blue register 258a and a Green/Red register 258b. The White/Blue register 258a stores image data for White/Blue. The Green/Red register 258b stores image data for Green/Red. In the RGBW structure, each data line carries data for two different colors. In this example, one data line carries data for White and Blue, and the other data line carries data for Green and Red. In one row, a data line is connected, for example, to White pixels (Green pixels) while during the next row it is connected to Blue pixels (Red pixels). As a result, the register 258a used for White and Blue data is shared, and the register 258b used for Green and Red is shared.

[0057] The driver output unit 270 includes a CMOS multiplexer 260 for multiplexing the outputs from the PMOS and NMOS decoders in the components 252 and 254. The multiplexer 260 is operated by a multiplexer 262 for multiplexing bit signals G/R[i] and W/B[k]. W/B[k] (G/R[j]) is a bit that defines when to use which part of the gamma for White or Blue (Green or Red). The bit W/B[k (G/R[j]) is generated based on the White/Blue register 258a (Green/Red register 258b) and predefined gamma values for White and Blue (Green and Red). The multiplexer 260 provides a source driver output 264.

[0058] When the bit signal W/B[k] is active, the source driver 192 outputs the source driver output 264 based on the high White gamma correction, the low White gamma correction, the high Blue gamma correction, the low White gamma correction or the low Blue gamma correction.

[0059] A demultiplexer 272 is employed in the panel 270 side to demultiplex the driver output 264 from the source driver 232. The demultiplexer 272 is implemented using, for example, thin film transistors, on the panel 270. The outputs from the demultiplexer 272 are couples to two data lines 274 and 276. The demultiplexer 272 is controlled by a control signal associated with the color selection. Based on the output from the demultiplexer 272, one of two data lines 274 and 276 is active. The driver output 264 is demultiplexed 272 on the panel 270 side and goes to different subpixels (i.e., White subpixel, Blue subpixel, Green subpixel, Red subpixel).

[0060] In the source driver 232, one PMOS decoder 254 is used for the higher range and one NOMS decoder 254 for the lower range of the voltage. Thus, the area will be reduced by using twice less transistors than a CMOS decoder.

[0061] In the panel 270, instead of having four Red subpixel, Green subpixel, Blue subpixel, and White subpixel side by side, they are configured in a quad arrangement where two subpixels for two colors are in one row and the other two colors are in the other row. In this example, one data line 274 carries data for White and Blue subpixels 278a and 278b, and the other data line 276 carries data for Green and Red subpixels 278c and 278d, as shown in Figure 9. The subpixels are divided into two rows and two columns. Thus the source driver provides data for two subpixels at a time.

[0062] Referring to Figure 10, there is illustrated a system 280 having a source driver 282, a panel 320 having pixels, and external gamma buffer area 290. The system

280 is applied to RGB pixel structure. Multiple gamma corrections for Red, Green and Blue are multiplexed in the external buffer area 290. The external gamma buffer area 290 is located external to the source driver area 282 (e.g., external to the source driver IC). The gamma voltages are generated externally and applied to the source driver 282 through buffers in the external gamma buffer area 290. On the display side 320, a demultiplexing is used to provide data for each color. One of ordinary skill in the art would appreciate that the source driver 282, the external gamma buffer area 290 and the panel 320 may include components not shown in Figure 10.

[0063] A PMOS multiplexer 292 is employed in the external gamma buffer area 290 for high voltage level of gamma corrections, and a NMOS multiplexer 294 is employed in the external gamma buffer area 290 for low voltage level of gamma corrections. The multiplexer 292 multiplexes a high Red gamma correction 296a, a high Green gamma correction 296b and a high Blue gamma correction 296c, and the multiplexer 294 multiplexes a low Red gamma correction 298a, a low Green gamma correction 298b and a low Blue gamma correction 298c. The gamma corrections 296a, 296b and 296c correspond to the gamma corrections 198a, 198b and 198c of Figure 7, respectively and are located outside the source driver 282. The gamma corrections 298a, 298b and 298c correspond to the gamma corrections 202a, 202b and 202c of Figure 7, respectively and are located outside the source driver 282. The PMOS and NMOS multiplexers 292 and 294 correspond to the multiplexers 196 and 200 of Figure 7, respectively and are located outside the source driver 282. The outputs from the PMOS and NMOS multiplexers 292 and 294 are provided to the source driver 282.

[0064] The source driver 282 includes a driver output unit 284. The driver output unit 284 includes a DAC that is divided into separate components: a PMOS component 300 ("PMOS DAC" in Figure 10) and a NMOS component 302 ("NMOS DAC" in Figure 10). The PMOS and NMOS components 300 and 302 correspond to the PMOS and NMOS components 204 and 206 of Figure 7, respectively. The PMOS component 300 includes a PMOS decoder and receives the output from the multiplexer 292. The NMOS component 302 includes a NMOS decoder and receives the output from the multiplexer 294. The PMOS and NMOS decoders in the components 300 and 302 operate on an output from a multiplexer 304 for multiplexing a Red register 306a, Green register 306b and Blue register 306c. The resisters 306a, 306b and 306b correspond to the registers 210a, 210b and 210c of Figure 7, respectively.

[0065] The driver output unit 284 includes a CMOS multiplexer 308 for multiplexing the outputs from the PMOS and NMOS components 300 and 302. The multiplexer 308 is operated by a multiplexer 310 for multiplexing bit signals R[j], G[i] and B[k]. The multiplexers 308 and 310 correspond to the multiplexers 212 and 214 of Figure 7, respectively. The multiplexer 308 outputs a single source driver output 316.

[0066] A demultiplexer 322 is employed on the panel 320 side to demultiplex the driver output 264 from the source driver 282. The demultiplexer 322 corresponds to the demultiplexer 182 of Figure 5. The demultiplexer 322 is implemented using, for example, thin film transistors, on the panel 320. The outputs from the demultiplexer 322 are couples to three data lines. The demultiplexer 322 is controlled by a control signal associated with the color selection. Based on the output from the demultiplexer 322, one of three data lines is active. The driver output 316 is demultiplexed 322 on the panel 320 side and goes to different subpixels (i.e., Red subpixel, Blue subpixel, Green subpixel).

[0067] In this example, the PMOS decoder component 300 is used for the higher range and the NOMS decoder component 302 for the lower range of the voltage. Thus, the source area will be reduced by using twice less transistors than that of a CMOS decoder. In addition, the gammas are multiplexed and provided from the outside of the source driver 282 area, thus the number of inputs required for the gamma correction is reduced as well.

[0068] For small displays, the gamma correction is internally programmable. The data for gamma correction is stored in internal registers. To reduce the number of gamma registers, DAC resistive ladders and DAC decoders, the gamma registers are multiplexed, as shown in Figure 11. For programming each color, the corresponding gamma color is assigned to the gamma block. Referring to Figure 11, there is illustrated a system 330 having a source driver 332 and a panel 360 having pixels. The system is applied to quad RGB pixel structure. Multiple gamma corrections for Red, Green and Blue are multiplexed in the source driver 332. One of ordinary skill in the art would appreciate that the source driver 332 and the panel 360 may include components not shown in Figure 11.

[0069] The source driver 332 includes a driver output unit 334 having a multiplexer 340 for multiplexing a Red gamma register 342a, a Green gamma register 342b and a Blue gamma register 342c, each for storing the corresponding gamma correction data. The gamma correction is internally programmed (configurable), and the data for the gamma correction is stored in the resister. The driver output unit 334 includes a gamma circuit 344 for generating the gamma voltage based on its input signals from the multiplexer 340 (i.e., data from the gamma resister 342a, 342b, 342c). The gamma circuit 344 may be, for example, but not limited to, a digital potentiometer or a DAC.

[0070] The driver output unit 334 includes a CMOS DAC 346 that has a decoder and receives the output from the gamma correction 344. The DAC decoder in the DAC 346 operates on an output from a multiplexer 348 for multiplexing a Red register 350a, a Green register 350b and a Blue register 350c. The registers 350a, 350b and 350c correspond to the resisters 174a, 174b and 174c of Figure 5, respectively. The driver output 348 from the

DAC decoder 346 is demultiplexed at a demultiplexer 362 in the panel 360 and goes to different subpixels (e.g., Red subpixel, Green subpixel and Blue subpixel). The demultiplexer 362 is implemented using, for example, thin film transistors, on the panel 360.

[0071] For further improving the source driver area, the DAC is divided into NMOS and PMOS decoders as shown in Figure 12. Referring to Figure 12, there is illustrated a system 370 having a source driver 372 and a panel 420 having pixels. The system 370 is applied to RGB pixel structure. Multiple gamma corrections for Red, Green and Blue are multiplexed in the source driver 372. One of ordinary skill in the art would appreciate that the source driver 372 and the panel 420 may include components not shown in Figure 12.

[0072] The source driver 372 includes a driver output unit 374 having a multiplexer 380 for multiplexing a Red gamma register 382a, a Green gamma register 382b and a Blue gamma register 382c. The gamma registers 382a, 382b and 382c correspond to the gamma resisters 342a, 342b and 342c of Figure 11, respectively. The driver output unit 374 includes a high gamma circuit 384 and a low gamma circuit 386. The high gamma circuit 384 generates a high gamma voltage based on its input signals from the multiplexer 380 (i.e., data from the gamma resister 382a, 382b, 382c). The low gamma circuit 386 generates a low gamma voltage based on its input signals from the multiplexer 380 (i.e., data from the gamma resister 382a, 382b, 382c). Each of the gamma circuits 384 and 386 may be, for example, but not limited to, a digital potentiometer or a DAC.

[0073] The driver output unit 374 includes PMOS and NMOS components 390 and 392. The PMOS component 390 includes a PMOS decoder and is provided for the high gamma 384. The NMOS component 392 includes a NMOA decoder and is provided for the low gamma 386. The PMOS and NMOS components 390 and 392 correspond to the PMOS and NMOS components 204 and 206 of Figure 7. The PMOS and NMOS decoders in the components 390 and 392 operate on an output from a multiplexer 394 for multiplexing a Red register 396a, a Green register 396b and a Blue register 396c. The registers 396a, 396b and 396c correspond to the resisters 174a, 174b and 174c of Figure 5 (210a, 210b and 210c of Figure 7), respectively.

[0074] The driver output unit 374 includes a CMOS multiplexer 400 for multiplexing the outputs from the PMOS and NMOS decoders in the components 390 and 392. The multiplexer 400 is operated by a multiplexer 402 for multiplexing bit signals R[j], G[i] and B[k]. The bit signals R[j], G[i] and B[k] correspond to the bit signals R[j], G[i] and B[k] of Figure 8. The multiplexer 400 outputs a source driver output 404.

[0075] A demultiplexer 422 is employed on the panel 420 side to demultiplex the driver output 404 from the source driver 372. The demultiplexer 422 corresponds to the demultiplexer 182 of Figure 5. The demultiplexer 422 is implemented using, for example, thin film transistors, on the panel 420. The outputs from the demultiplexer 422 are couples to three data lines. The demultiplexer 422 is controlled by a control signal associated with the color selection. Based on the output from the demultiplexer 422, one of three data lines is active. The driver output 404 is demultiplexed 422 on the panel 420 side and goes to different subpixels (i.e., Red subpixel, Blue subpixel, Green subpixel).

[0076] To develop muxing in a source driver, data for each color is multiplexed as shown in Figure 13. Figure 13 illustrates a source driver 450 for scanning a panel for a conventional display system. The source driver 450 includes a shift register unit 452 and a latch unit 456. The shift register unit 452 includes a plurality of shift registers 454a-454d, and receives a latch signal. The latch unit 456 includes a plurality of latch circuits 458a-458d that are employed for the shift registers 454a-454b, respectively. Each latch circuit 458a, 458b, 458c, 458d latches a digital image signal in response to the latch signal from the corresponding shift register. The outputs from three latch circuits 458a, 458b and 458c are multiplexed by a multiplexer 460 to output R, G, B image signals. The data for each color is multiplexed 460. A DAC 462 includes a decoder for decoding the output from the multiplexer 460 to output analog image signals.

[0077] To further reduce the source area, the latch unit 456 is replaced with shift registers as shown in Figure 14. Referring to Figure 14, there is illustrated a source driver 480 for a display system. The source driver 480 includes a first stage shift register unit 482, a second stage latch and shift unit 486, and a DAC unit. The multiplexer 460 of Figure 13 is not implemented in the source driver 480 side. The shift register unit 482 includes a plurality of shift registers, and each receives a latch signal. The latch and shift unit 486 includes a plurality of latch and shift registers that are employed for the shift registers in the shift register unit 482, respectively. In Figure 14, four shift registers 484a-484d are shown as an example of the components of the shift register unit 482. In Figure 14, four latch and shift registers 488a-488d are shown as an example of the components of the latch and shift unit 486. In Figure 14, one DAC 490 is shown as an element of the DAC unit. The DAC 490 has a decoder. The DAC 490 is coupled to the latch and shift register 488c, which decodes its input and outputs a source driver output 492.

[0078] It will be appreciated by one of ordinary skill in the art that the number of the shift registers and the number of the latch and shift registers are not limited to four and may vary. It will be appreciated by one of ordinary skill in the art that the source driver 480 may include components not illustrated in Figure 14. It will be appreciated by one of ordinary skill in the art that the DAC unit of the source driver 480 may include more than one DAC. In one example, the DAC unit includes a plurality of DACs connected in M intervals.

[0079] Each latch and shift register in the second stage latch and shift unit 486 can copy its input signal and keep

it intact till the next activation signal. The input signal to the latch and shift register may come from the corresponding first stage shift register or the previous latch and shift register in the chain. As a result, the latch and shift register can store the data for a row from the first stage shift register or it can shift its own data to the next units. For example, the latch and shift register 488a latches a digital image signal in response to an activation signal from the corresponding shift register 484a. The latched signal is shifted to the next latch and shift register 488b.

[0080] After the input signal for a row is stored in the shift register unit 482, the second stage latch unit 486 is activated and copies the signals from the shift register unit 482. After that, the second stage latch unit 486 shifts the data one by one to the DACs connected in M intervals connect to the latch unit where M defines the muxing order.

[0081] After the first color data is programmed, the latch data is shifted by the number of required bits so that the second data is stored in the latch 488c connected to the DAC 490. This operation is executed for other colors as well until all the colors are programmed. This implementation results in a simpler routing and smaller die area. It will be appreciated by one of ordinary skill in the art that a panel side may have a demultiplexer for demultiplexing the source driver 480 output associated with the M multiplexing operation. It will be appreciated by one of ordinary skill in the art that the source driver 480 is applicable to monochrome displays.

[0082] Referring to Figure 15, there is illustrated a source driver 500 for a display system. To develop DAC decoders, high voltage fabrication process is used, which results in large die area. Instead of a having one gamma curve that covers the entire output voltage rage (e.g. 0 to 15), the source driver 500 uses a plurality of smaller offset gamma curve segments (sections) at lower voltage range, which are extracted from different part of the complete gamma curve.

[0083] The source driver 500 includes a gamma block 502 for changing the color (gray scale) mapping for a display, a resistive ladder 504 for generating reference voltages, and an overlapping multiplexer block 506 for the offset gamma curve sections.

[0084] The overlapping multiplexer block 506 includes a plurality of multiplexers, each for multiplexing reference voltages for different colors. In Figure 15, three multiplexers 508a, 508b and 508c are shown as an example of components of the overlapping multiplexer block 506. The adjacent multiplexer covers different range of the output voltage, having the beginning and the end of the range. However, the end of one range in one multiplexer and the beginning of the other range in the adjacent multiplexer overlap each other. The overlapping provides flexibility in achieving different gamma curve. The same inputs are being used for both multiplexers.

[0085] The source driver 500 includes a DAC decoder section that is segmented into a plurality of low voltage decoders for the offset gamma curve sections. In Figure 15, the three low voltage decoders 510a, 510b and 510c are shown as the elements of the DAC decoder, each operating at low voltage. The two adjacent decoders share a small portion of their dynamic range. A programmable decoder 512 defines the border of each decoder 510a-510c according to the gamma curves. This allows for having different gamma curves for different applications.

[0086] In Figure 16A, an example of a main gamma curve is illustrated. The main gamma curve 530 of Figure 16A has a range from 0 to 10V. In Figure 16B, the main gamma curve 530 of Figure 16A is segmented into a plurality of offset gamma curve sections 540, 542 and 544. Each offset gamma curve section has a shape corresponding to that of the same section of the main gamma curve 530, and has a voltage range 0 to 5V. The gamma curve section 542 is offset by -5V. The gamma curve section 542 is offset by -10V. Using the offset gamma curve sections, the internal circuits associated with the gamma corrections are offset to lower voltage. The gamma curve section may be internally programmed or input from an external area or device. The display system may include a module for programming/defining offset gamma curve sections. This module may be integrated or operate in conjunction with the programmable decoder 512.

[0087] Referring to Figures 15 and 16B, the multiplexer 508a is allocated for one offset gamma curve section (e.g., 540 of Figure 16B) and the low voltage decoder 510a uses that offset gamma curve section. The multiplexer 508b is allocated for another offset gamma curve section (e.g., 542 of Figure 16B) and the low voltage decoder 510b uses that offset gamma curve section. The multiplexer 508c is allocated for the other offset gamma curve section (e.g., 544 of Figure 16B) and the low voltage decoder 510c uses that offset gamma curve section. The low voltage decoders 510a, 510b and 510c are programmable.

[0088] The source driver 500 includes an output buffer 516. The output buffer 516 outputs a source driver output 520 based on the output from the decoder and the offset voltage.

[0089] Based on the pixel circuit data, one offset gamma curve section with its corresponding decoder is being selected. Then the data is passed to the output buffer 516. In order to create the required voltage, the created voltage is being shifted up at the output buffer 516. If a voltage is selected from the second gamma curve section 542 of Figure 16B, it will be offset by 5 V at the output buffer 516 to cover for the original offset.

[0090] Each segment is in its own well so that the body bias can be adjusted accordingly. The decoder can be implemented in low voltage process, leading to smaller die area (over three times saving).

[0091] Referring to Figure 17, there is illustrated an example of a display system 600. The system 600 includes a controller 602, a source driver IC 604, a gate

driver IC 606, and a panel 608. The gate driver 606 may include the gate driver 102 of Figures 1A-1B or the gate driver 132 of Figures 3A-3B. The panel 608 includes a pixel array having a plurality of pixels (or subpixels) 610 and a demultiplexer 612. The demultiplexer 612 may include the demultiplexer 112 of Figures 1A-1B or the demultiplexer 142 of Figures 3A-3B. The controller 602 controls the source driver 604 and the gate driver 606. The controller 602 also generates control signals 614 to operate the demultiplexer 612, which may correspond to the control signals CTRL(k) of Figures 1A or 3A. The demultiplexer 612 is implemented using, for example, thin film transistors, on the panel 608.

[0092] Referring to Figure 18, there is illustrated an example of a display system 630. The system 530 includes a controller 632, a source driver IC 634, a gate driver IC 636, and a panel 638. The source driver 632 may include the source driver 162 of Figure 5, 192 of Figure 7, 232 of Figure 8, 282 of Figure 10, 332 of Figure 11 or 372 of Figure 12. The panel 638 includes a pixel array having a plurality of pixels (or subpixels) 610 and a demultiplexer 642. The demultiplexer 642 may include the demultiplexer 182 of Figure 5, 222 of Figure 7, 272 of Figure 8, 322 of Figure 10, 362 of Figure 11 or 422 of Figure 12. The controller 632 controls the source driver 634 and the gate driver 636. The controller 632 also generates control signals 644 to operate the demultiplexer 632. The demultiplexer 642 is implemented using, for example, thin film transistors, on the panel 638. The system 630 may includes the external gamma 290 of Figure 10.

[0093] Referring to Figure 19, there is illustrated an example of a display system 660 having the source driver elements of Figure 14 or Figure 15. The system 660 includes a controller 662, a source driver IC 664, a gate driver IC 666, and a panel 668. The panel 668 includes a pixel array having a plurality of pixels (or subpixels) 610. The controller 662 controls the source driver 664 and the gate driver 666. The controller 662 controls, for example, the shift register unit 482 and the latch and shift unit 486 of Figure 14 or the overlapping multiplexer block 506 and the low voltage decoders 510a-510b of Figure 15.

[0094] In the above example, the gate drivers and the source drivers are described separately. However, one of ordinary skill in the art would appreciate that any of the gate drivers of Figures 1A and 3B can be used with the source drivers of Figures 6-15.

Claims

1. A display system, comprising:

a panel (140) comprising:

a plurality of scan lines;
at least one data line;
a plurality of pixels arranged by the plurality of scan lines and the at least one data line, wherein the plurality of scan lines correspond to a plurality of rows and the at least one data line corresponds to at least one column; and
a demultiplexer (142) having a plurality of switch blocks (146a, 146b) adapted to activate the plurality of scan lines by demultiplexing an input signal (136a, 136b) in accordance with a control signal (CTRL(1), CTRL(2)); and

a gate driver (132) adapted to operate the panel (140), the gate driver (132) comprising:

a plurality of address cells (138a-138d) each outputting a respective gate driver signal; and
a driver output unit (133) adapted to provide to the panel (140) a single driver output (136a, 136b) for activating the plurality of scan lines, the single driver output being connected to the demultiplexer (142) on the panel (140), wherein the single driver output is demultiplexed on the panel to activate each of the plurality of scan lines;

characterized in that

the driver output unit (133) comprises:

a multiplexer (134a, 134b) adapted to multiplex the plurality of gate driver signals generated by the respective address cells (138a - 138d) such that the signal output by the single driver output (136a, 136b) corresponds to one of the plurality of gate driver signals;
wherein the multiplexer (134a, 134b) is controlled by a multiplexing control signal (iCTRL) that is associated with said control signal (CTRL(1), CTRL(2)) for controlling the demultiplexing of the single driver output (136a, 136b) on the panel (140); and
each switch block (146a, 146b) of the demultiplexer is adapted to receive an output from the multiplexer (134a, 134b).

2. A method of operating the display system of claim 1, the method further comprising:

providing from the gate driver (132) to the panel (140) a signal from the single driver output (136a, 136b); and
demultiplexing the signal provided by the single

driver output to activate the plurality of scan lines;
characterized by:

multiplexing the plurality of gate driver signals from the address cells (138a-138d) such that the signal output by the single driver output (136a, 136b) corresponds to one of the plurality of gate driver signals; and
controlling the multiplexing by a multiplexing control signal (iCTRL) that is associated with the control signal (CTRL(1), CTRL(2)) for controlling the demultiplexing of the single driver output on the panel.

Patentansprüche

1. Anzeigesystem, das umfasst:

ein Panel (140), das umfasst:

eine Vielzahl von Abtastungsleitungen,
wenigstens eine Datenleitung,
eine Vielzahl von Pixeln, die durch die Vielzahl von Abtastungsleitungen und die wenigstens eine Datenleitung angeordnet werden, wobei die Vielzahl von Abtastungsleitungen einer Vielzahl von Reihen entsprechen und die wenigstens eine Datenleitung wenigstens einer Spalte entspricht, und
einen Demultiplexer (142), der eine Vielzahl von Schaltblöcken (146a, 146b) aufweist, die ausgebildet sind zum Aktivieren der Vielzahl von Abtastungsleitungen durch das Demultiplexen eines Eingangssignals (136a, 136b) gemäß einem Steuersignal (CTRL(1), CTRL(2)), und

einen Gate-Treiber (132), der ausgebildet ist zum Betreiben des Panels (140), wobei der Gate-Treiber (132) umfasst:

eine Vielzahl von Adresszellen (138a-138d), die jeweils ein entsprechendes Gate-Treibersignal ausgeben, und
eine Treiberausgabeeinheit (133), die ausgebildet ist zum Vorsehen, zu dem Panel (140), einer einzelnen Treiberausgabe (136a, 136b) für das Aktivieren der Vielzahl von Abtastungsleitungen, wobei die einzelne Treiberausgabe mit dem Demultiplexer (142) an dem Panel (140) verbunden wird, wobei die einzelne Treiberausgabe an dem Panel gedemultiplext wird, um jede aus der Vielzahl von Abtastungsleitungen zu aktivieren,

dadurch gekennzeichnet, dass
die Treiberausgabeeinheit (133) umfasst:

einen Multiplexer (134a, 134b), der ausgebildet ist zum Multiplexen der Vielzahl von Gate-Treibersignalen, die durch die entsprechenden Adresszellen (138a-138d) erzeugt werden, sodass das durch die einzelne Treiberausgabe (136a, 136b) ausgegebene Signal einem aus der Vielzahl von Gate-Treibersignalen entspricht,
wobei der Multiplexer (134a, 134b) durch ein mit dem Steuersignal (CTRL(1), CTRL(2)) assoziiertes Multiplexing-Steuersignal (iCTRL) gesteuert wird, um das Demultiplexen der einzelnen Treiberausgabe (136a, 136b) an dem Panel (140) zu steuern, und
jeder Schaltblock (146a, 146b) des Demultiplexers ausgebildet ist zum Empfangen einer Ausgabe von dem Multiplexer (134a, 134b).

2. Verfahren zum Betreiben des Anzeigesystems von Anspruch 1, wobei das Verfahren umfasst:

Vorsehen, von dem Gate-Treiber (132) zu dem Panel (140), eines Signals von der einzelnen Treiberausgabe (136a, 136b), und
Demultiplexen des durch die einzelne Treiberausgabe vorgesehenen Signals, um die Vielzahl von Abtastungsleitungen zu aktivieren,

gekennzeichnet durch:

Multiplexen der Vielzahl von Gate-Treibersignalen von den Adresszellen (138a-138d) derart, dass das durch die einzelne Treiberausgabe (136a, 136b) ausgegebene Signal einem aus der Vielzahl von Gate-Treibersignalen entspricht, und
Steuern des Multiplexens durch ein mit dem Steuersignal (CTRL(1), CTRL(2)) assoziiertes Multiplexing-Steuersignal (iCTRL), um das Demultiplexen der einzelnen Treiberausgabe an dem Panel zu steuern.

Revendications

1. Système d'affichage comprenant :

un panneau (140) comprenant :

une pluralité de lignes de balayage,
au moins une ligne de données,
une pluralité de pixels organisés par la pluralité de lignes de balayage et par la ou les

lignes de données, la pluralité de lignes de balayage correspondant à une pluralité de rangées et la ou les lignes de données correspondant à au moins une colonne, et
un démultiplexeur (142) comportant une pluralité de blocs de commutation (146a, 146b) conçus pour activer la pluralité de lignes de balayage en démultiplexant un signal d'entrée (136a, 136b) en fonction d'un signal de commande (CTRL(1), CTRL(2)), et

un circuit d'attaque de portes (132) conçu pour opérer le panneau (140), le circuit d'attaque de portes (132) comprenant :

une pluralité de cellules d'adressage (138a à 138d) délivrant chacune en sortie un signal respectif d'attaque de porte, et
une unité de sortie d'attaque (133) conçue pour fournir au panneau (140) une sortie unique d'attaque (136a, 136b) permettant d'activer la pluralité de lignes de balayage, la sortie unique d'attaque étant reliée au démultiplexeur (142) sur le panneau (140), la sortie unique d'attaque étant démultiplexée sur le panneau pour activer chacune de la pluralité de lignes de balayage,

caractérisé en ce que
l'unité de sortie d'attaque (133) comprend :

un multiplexeur (134a, 134b) conçu pour multiplexer la pluralité de signaux d'attaque de portes générés par les cellules d'adressage (138a à 138d) respectives de sorte à ce que le signal délivré en sortie par la sortie unique d'attaque (136a, 136b) corresponde à l'un de la pluralité de signaux d'attaque de portes,
dans lequel le multiplexeur (134a, 134b) est commandé par un signal de commande de multiplexage (iCTRL) qui est associé au dit signal de commande (CTRL(1), CTRL(2)) afin de commander le démultiplexage de la sortie unique d'attaque (136a, 136b) sur le panneau (140), et
chaque bloc de commutation (146a, 146b) du démultiplexeur est conçu pour recevoir une sortie provenant du multiplexeur (134a, 134b).

2. Procédé de mise en oeuvre du système d'affichage de la revendication 1, le procédé comprenant en outre :

la délivrance, en provenance du circuit d'attaque de portes (132) vers le panneau (140), d'un signal provenant de la sortie unique d'attaque (136a, 136b), et
le démultiplexage du signal délivré par la sortie unique d'attaque pour activer la pluralité de lignes de balayage,

caractérisé par :

le multiplexage de la pluralité de signaux d'attaque de portes à partir des cellules d'adressage (138a à 138d) de sorte à ce que le signal délivré en sortie par la sortie unique d'attaque (136a, 136b) corresponde à l'un de la pluralité de signaux d'attaque de portes, et
la commande du multiplexage par un signal de commande de multiplexage (iCTRL) qui est associé au signal de commande (CTRL(1), CTRL(2)) pour commander le démultiplexage de la sortie unique d'attaque sur le panneau.

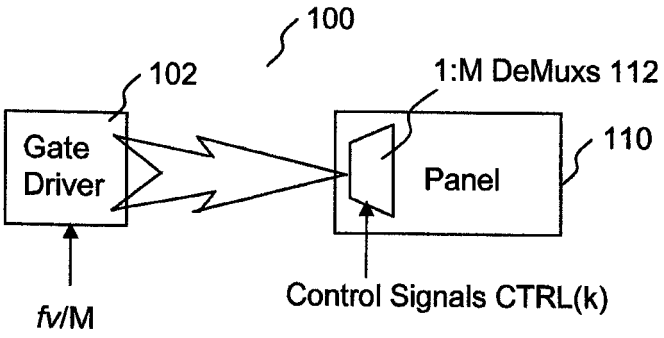
100
102
1:M DeMuxs 112
Gate Driver
Panel
110
fv/M
Control Signals CTRL(k)

FIG. 1A

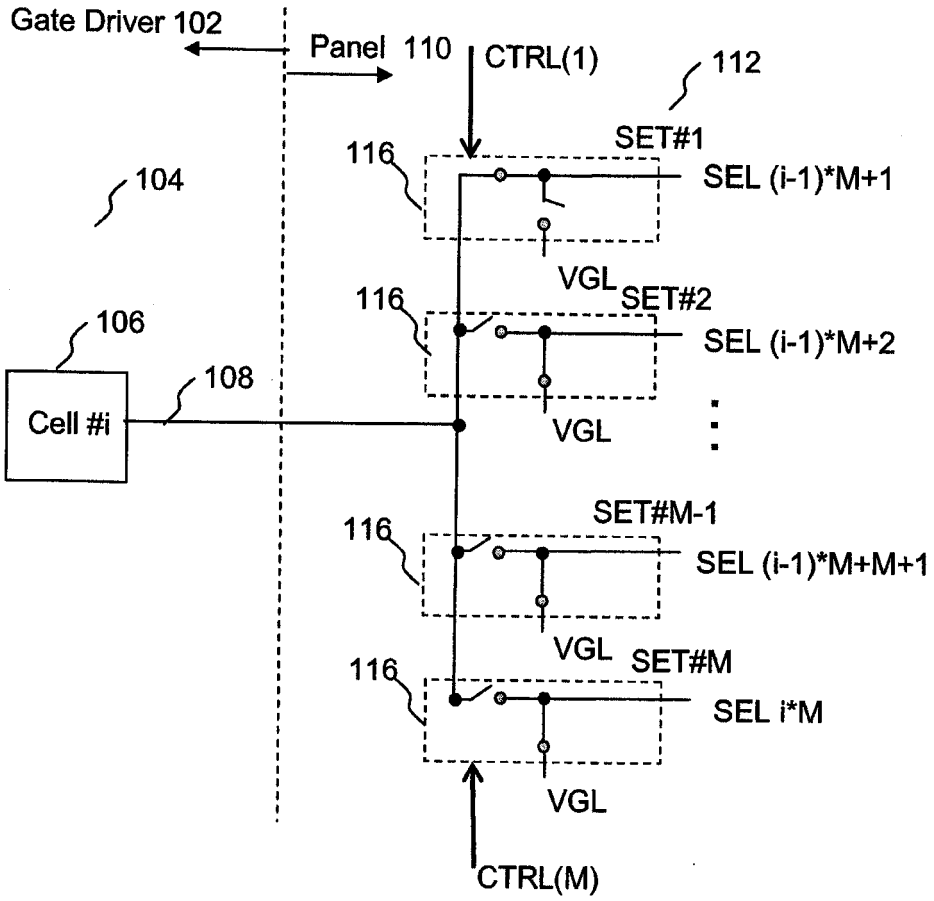
Gate Driver 102
Panel 110
CTRL(1)
112
SET#1
116
104
SEL (i-1)*M+1
VGL
SET#2
116
106
SEL (i-1)*M+2
108
Cell #i
VGL
SET#M-1
116
SEL (i-1)*M+M+1
VGL
SET#M
116
SEL i*M
VGL
CTRL(M)

FIG. 1B

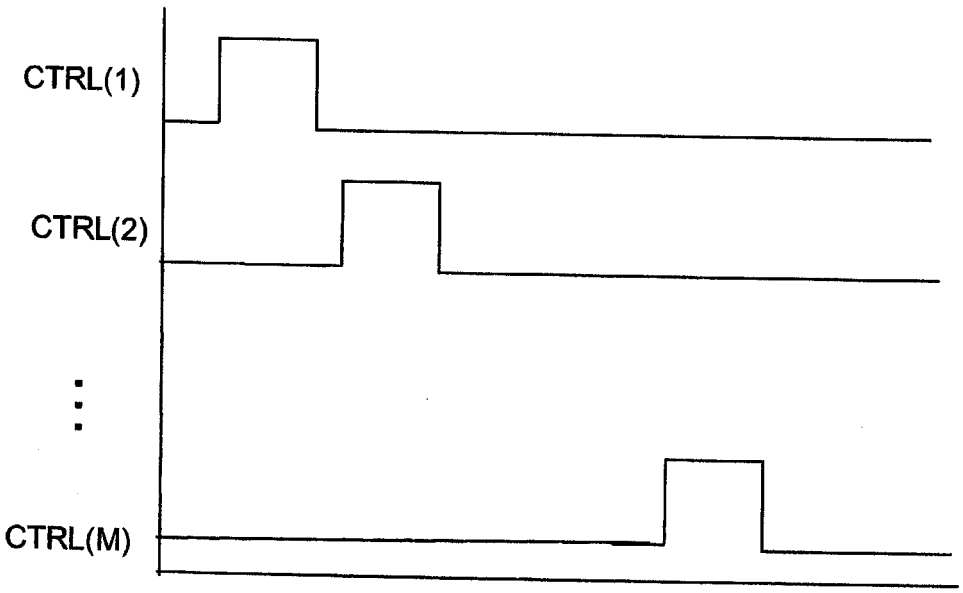

FIG. 2

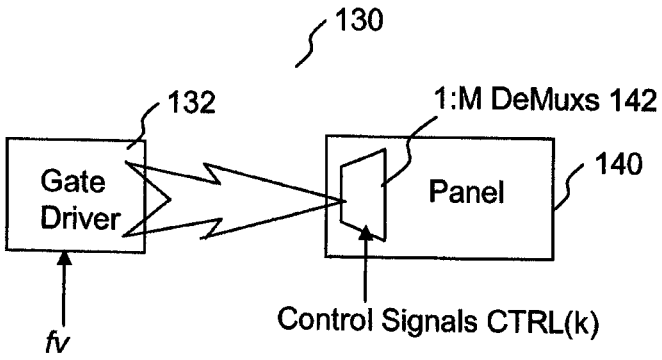
130
132
1:M DeMuxs 142
Gate Driver
Panel
140
fv
Control Signals CTRL(k)

FIG. 3A

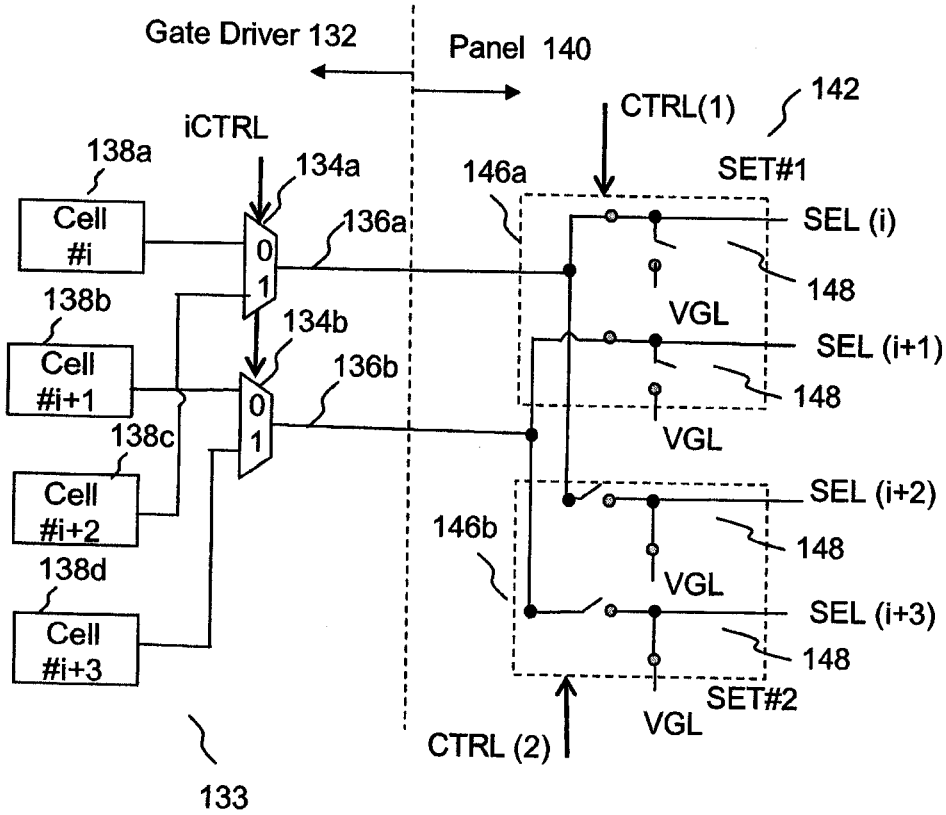
Gate Driver 132
Panel 140
CTRL(1)
142
iCTRL
138a
134a
146a
SET#1
Cell #i
136a
SEL (i)
148
VGL
138b
134b
SEL (i+1)
Cell #i+1
136b
148
VGL
138c
SEL (i+2)
Cell #i+2
146b
148
VGL
138d
SEL (i+3)
Cell #i+3
148
SET#2
VGL
CTRL (2)
133

FIG. 3B

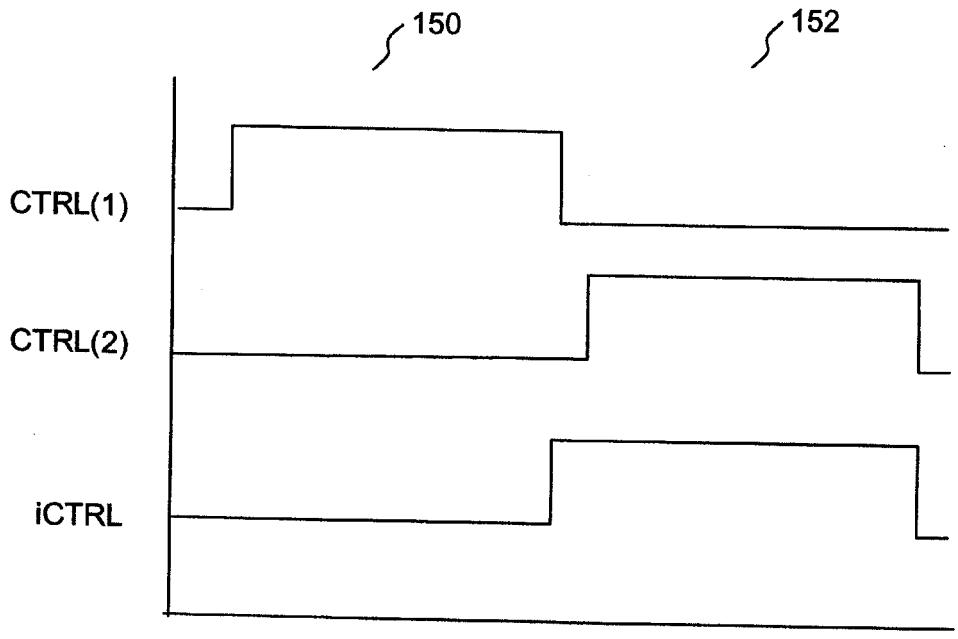

FIG. 4

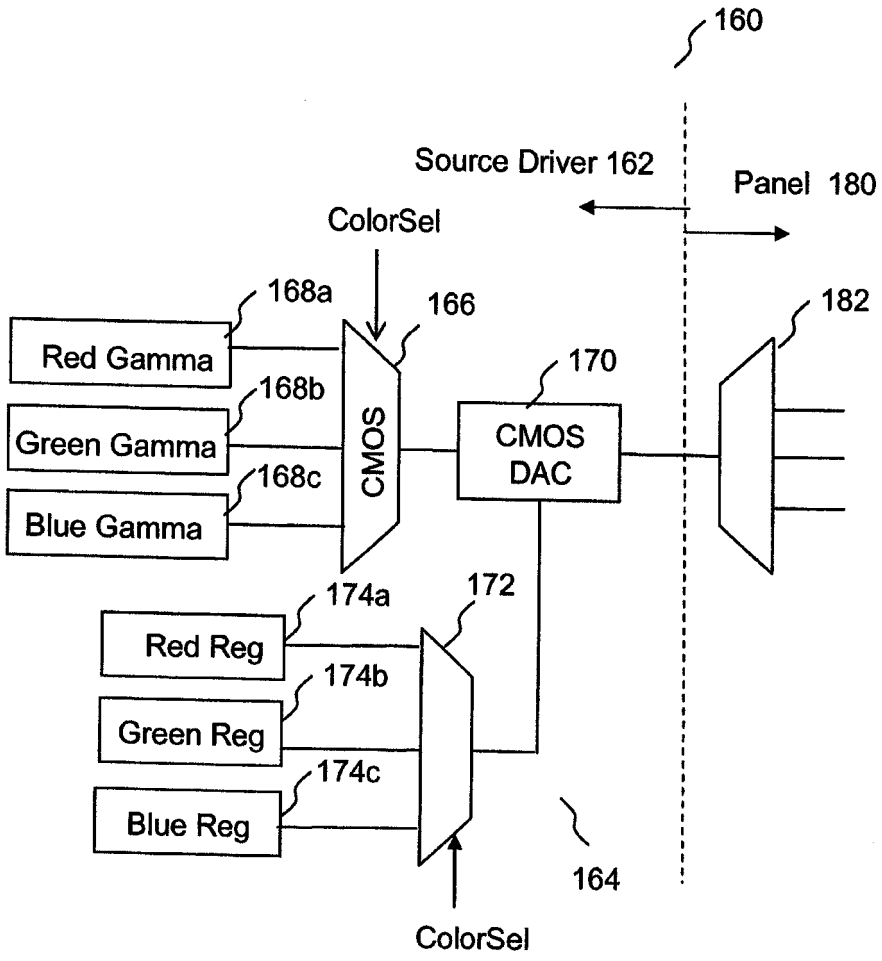
160
Source Driver 162
Panel 180
ColorSel
168a
166
182
Red Gamma
170
168b
Green Gamma
CMOS
CMOS DAC
168c
Blue Gamma
174a
172
Red Reg
174b
Green Reg
174c
Blue Reg
164
ColorSel

FIG. 5

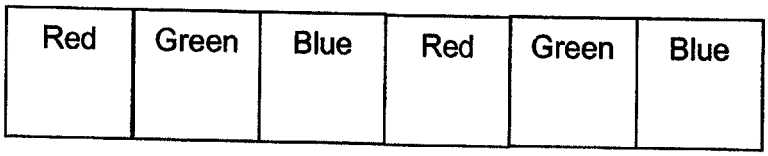

FIG. 6

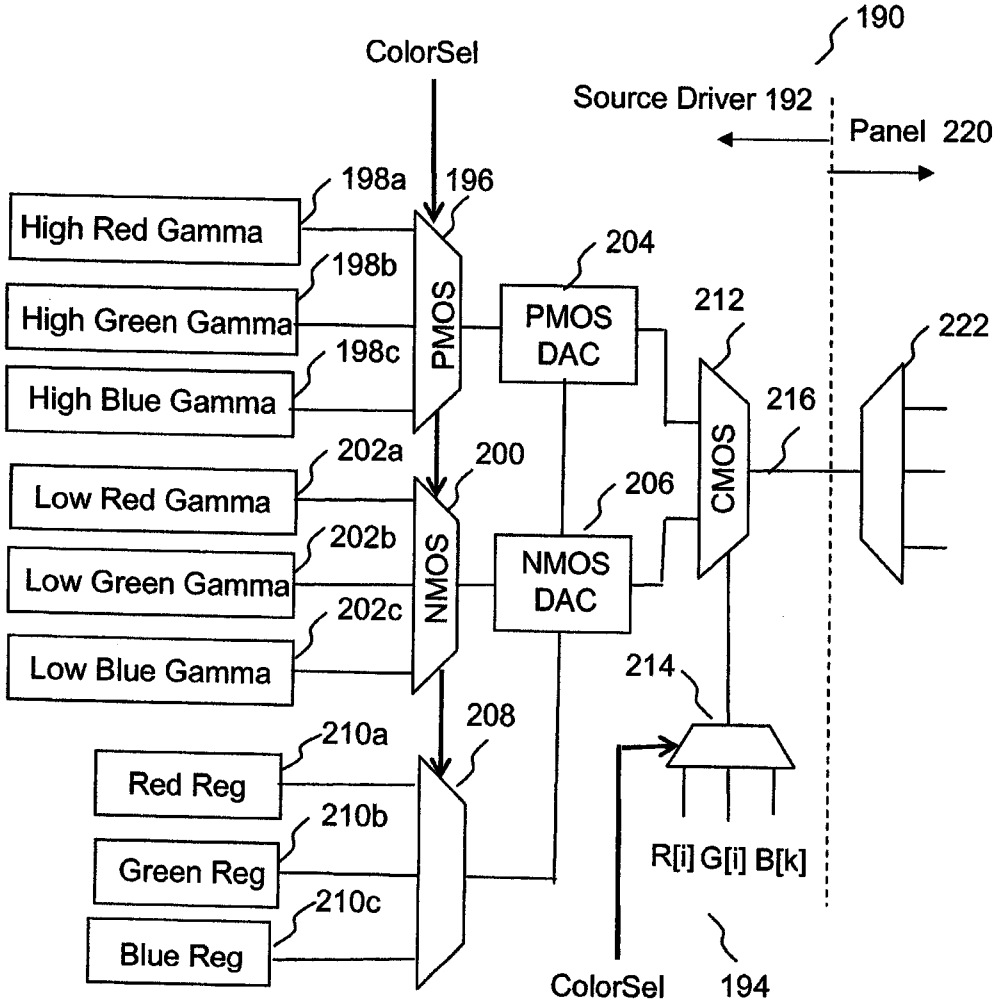
ColorSel
190
Source Driver 192
Panel 220
198a
196
High Red Gamma
198b
High Green Gamma
198c
High Blue Gamma
PMOS
204
PMOS DAC
212
222
216
CMOS
202a
200
Low Red Gamma
206
202b
Low Green Gamma
NMOS
NMOS DAC
202c
Low Blue Gamma
214
208
210a
Red Reg
210b
Green Reg
210c
Blue Reg
R[i] G[i] B[k]
ColorSel
194

FIG. 7

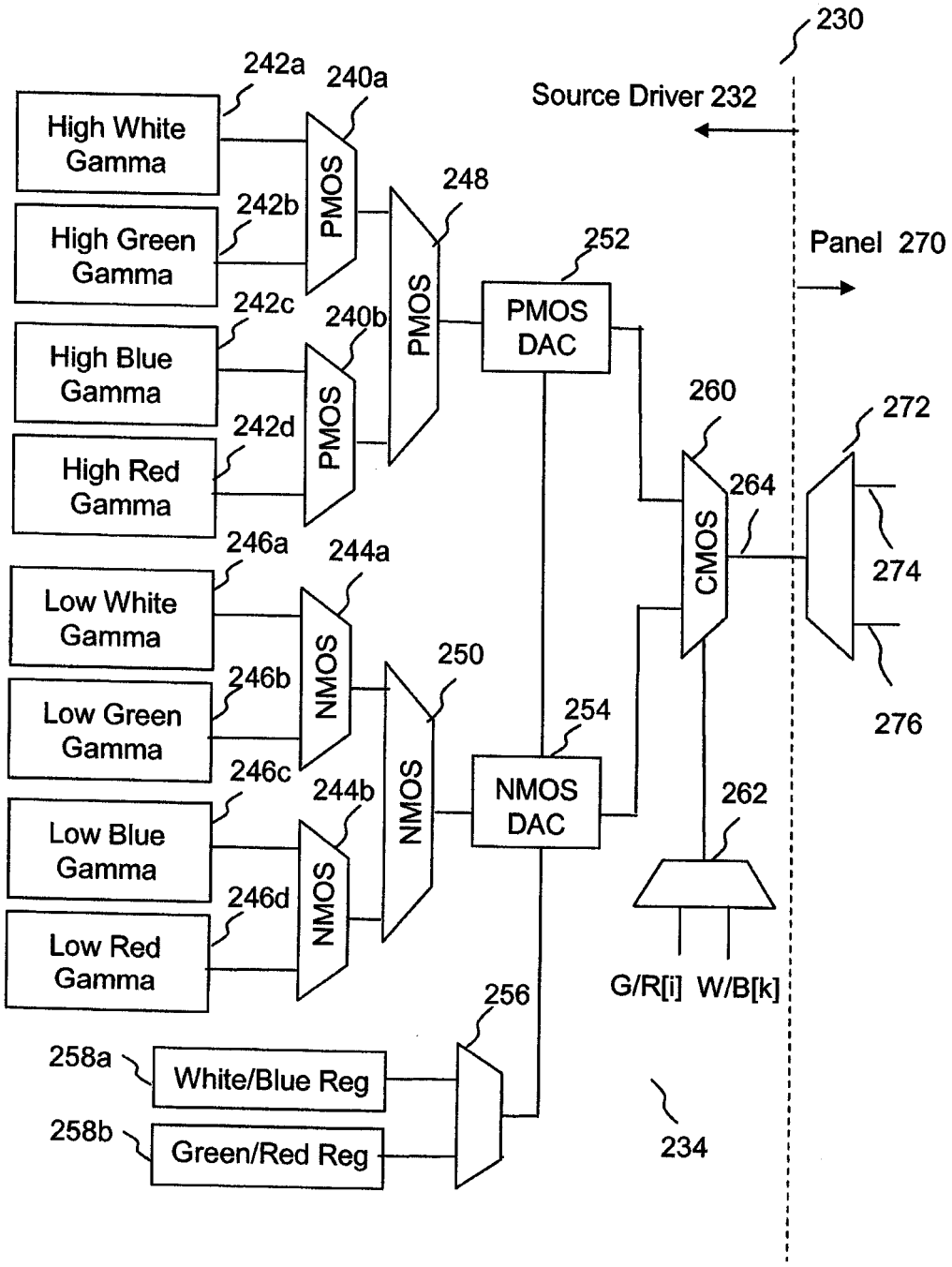
230
Source Driver 232
Panel 270
242a
240a
High White Gamma
242b
High Green Gamma
242c
240b
High Blue Gamma
242d
High Red Gamma
PMOS
PMOS
PMOS
248
252
PMOS DAC
260
CMOS
264
272
274
276
246a
244a
Low White Gamma
246b
Low Green Gamma
246c
244b
Low Blue Gamma
246d
Low Red Gamma
NMOS
NMOS
NMOS
250
254
NMOS DAC
262
G/R[i] W/B[k]
256
258a
White/Blue Reg
258b
Green/Red Reg
234

FIG. 8

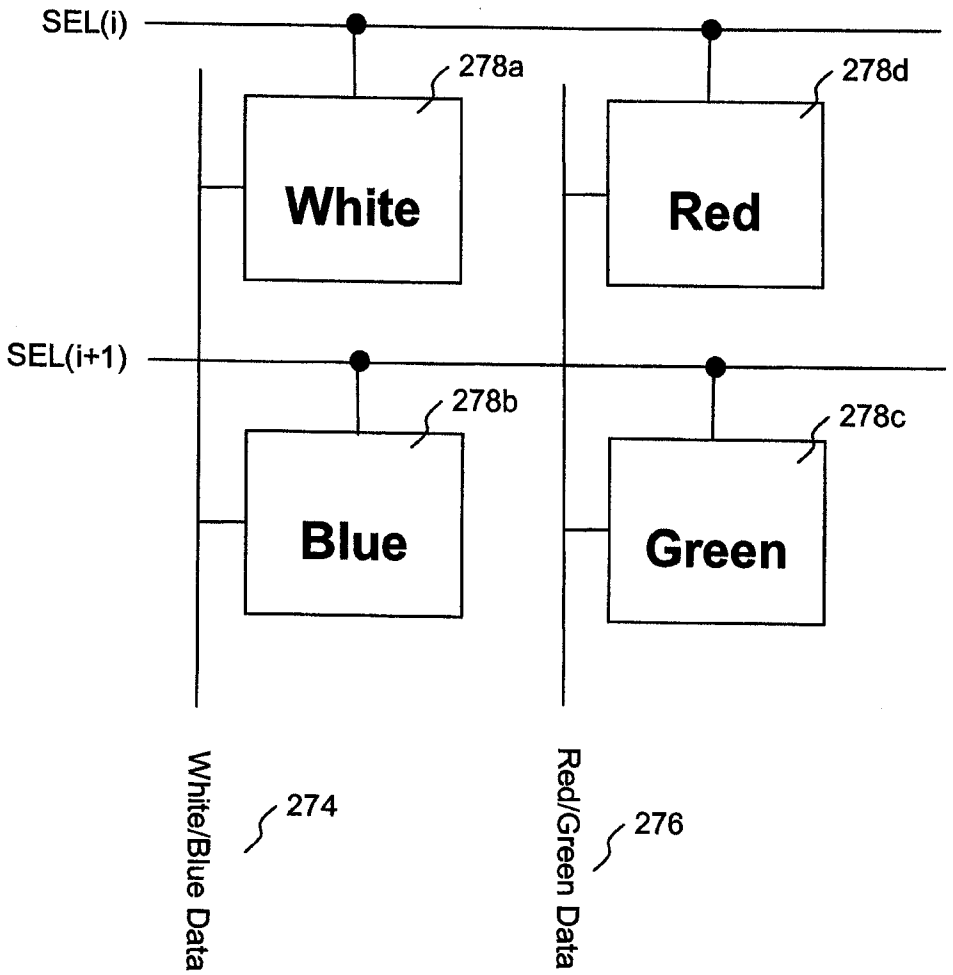
SEL(i)
SEL(i+1)
278a
278d
278b
278c
White
Red
Blue
Green
White/Blue Data
Red/Green Data
274
276

FIG. 9

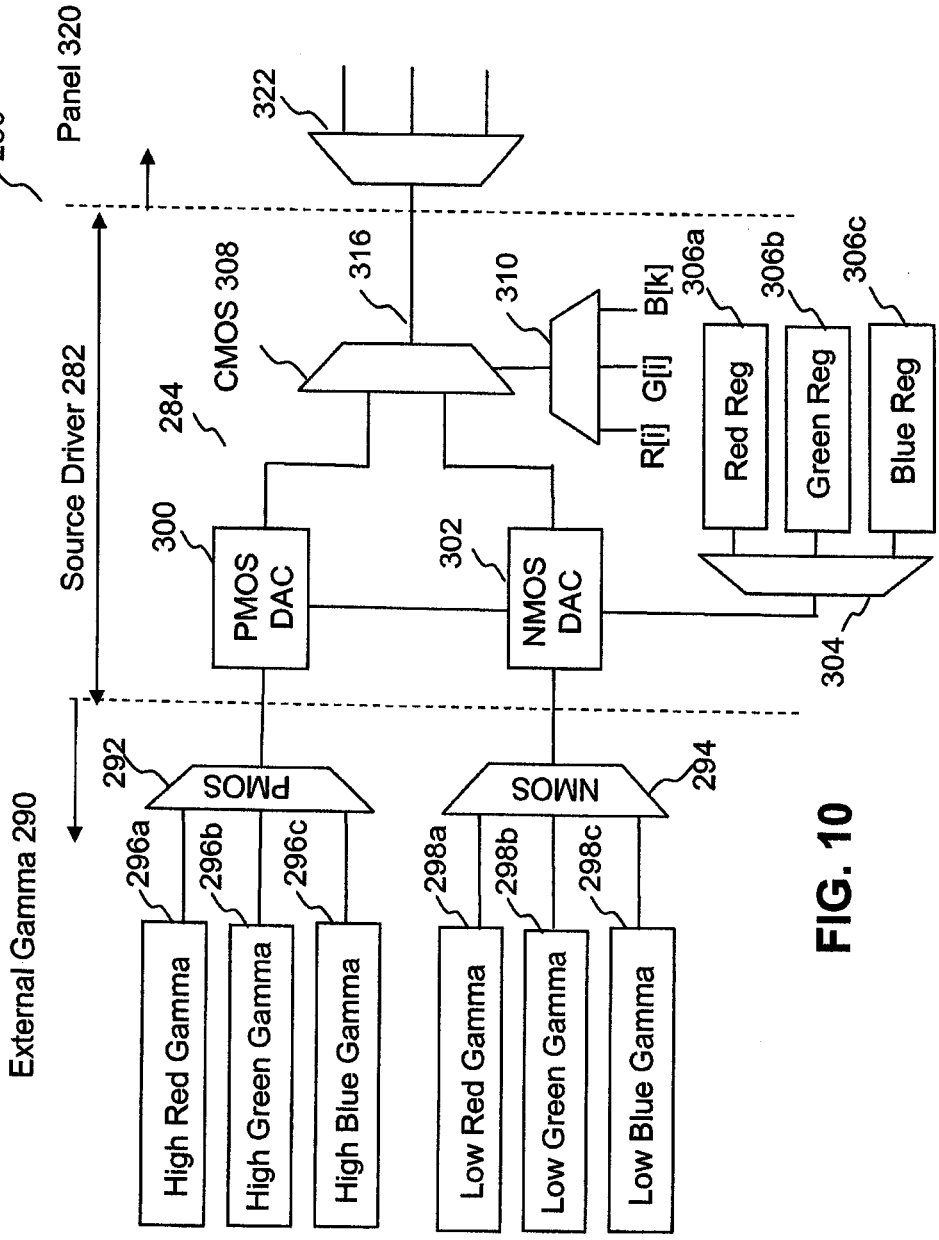
280
Panel 320
322
316
310
CMOS 308
284
Source Driver 282
B[k]
G[i]
R[i]
306a
306b
306c
Red Reg
Green Reg
Blue Reg
300
PMOS DAC
302
NMOS DAC
304
292
PMOS
NMOS
294
External Gamma 290
296a
296b
296c
298a
298b
298c
High Red Gamma
High Green Gamma
High Blue Gamma
Low Red Gamma
Low Green Gamma
Low Blue Gamma

FIG. 10

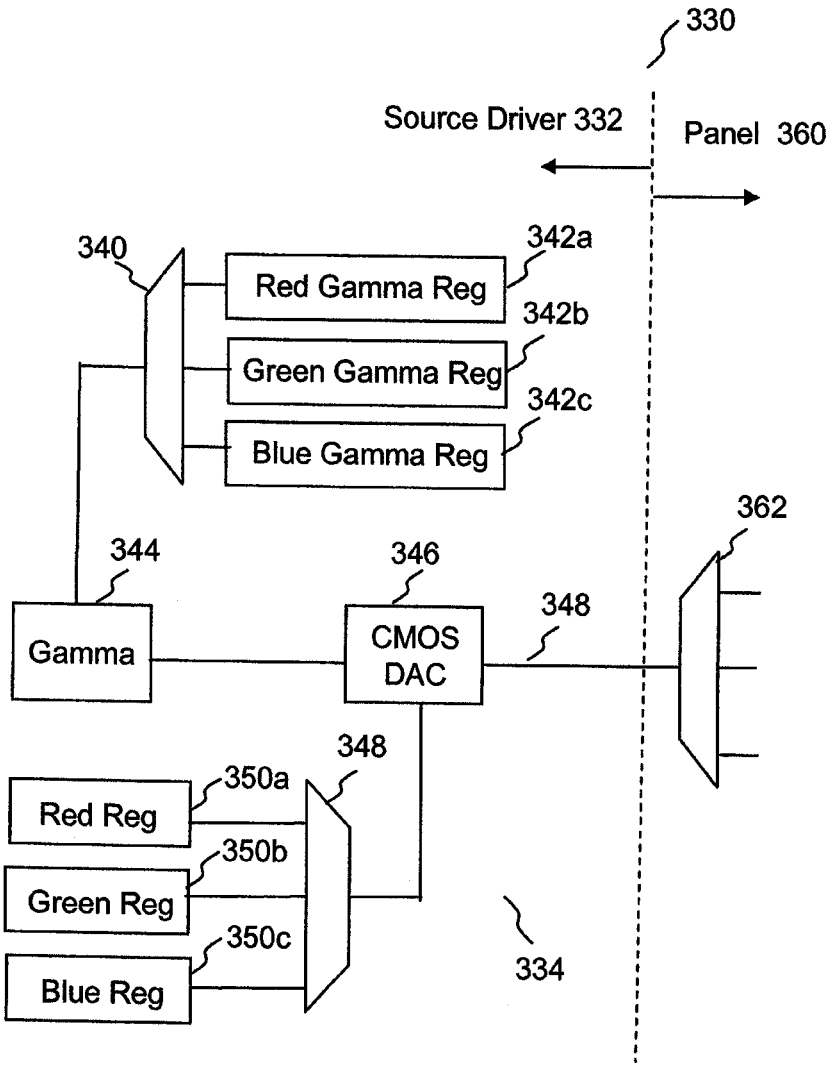
330
Source Driver 332
Panel 360
340
342a
Red Gamma Reg
342b
Green Gamma Reg
342c
Blue Gamma Reg
362
344
346
348
Gamma
CMOS DAC
348
350a
Red Reg
350b
Green Reg
350c
Blue Reg
334

FIG. 11

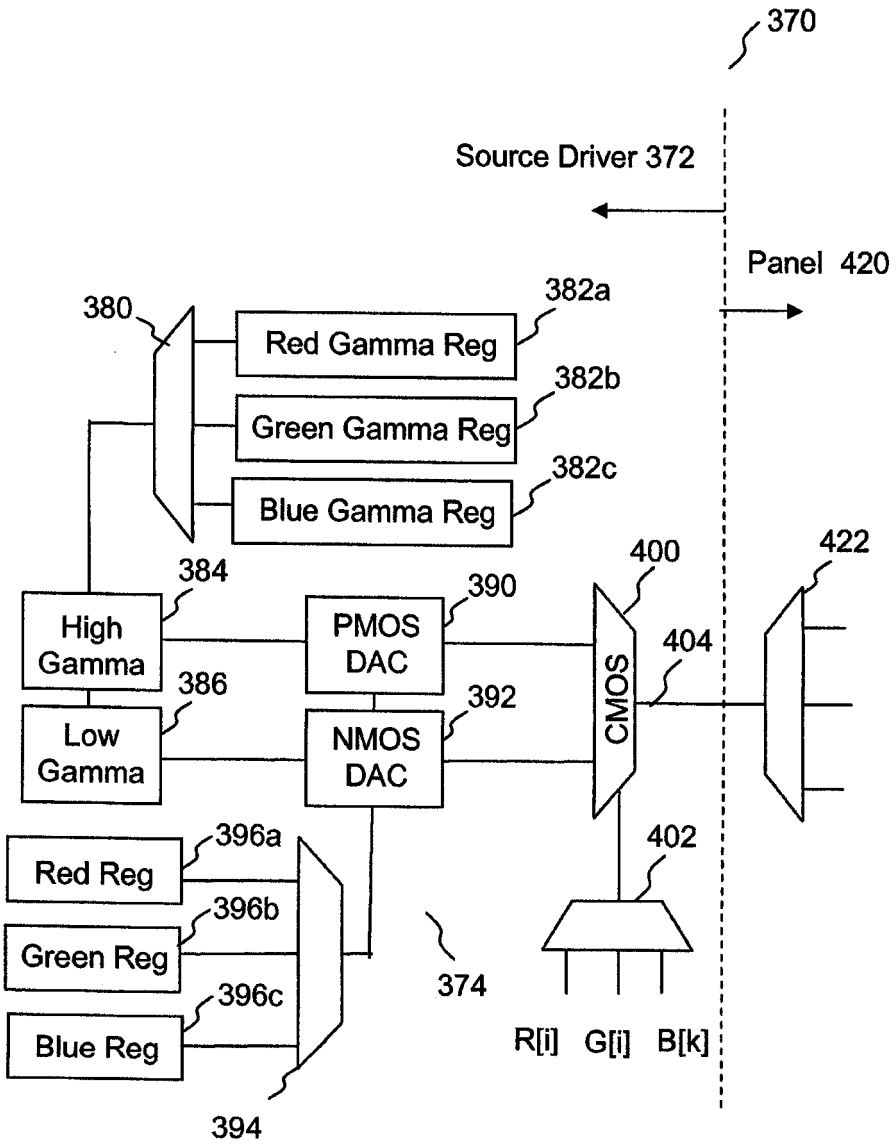
370
Source Driver 372
Panel 420
380
382a
Red Gamma Reg
382b
Green Gamma Reg
382c
Blue Gamma Reg
384
High Gamma
386
Low Gamma
390
PMOS DAC
392
NMOS DAC
400
CMOS
404
422
396a
Red Reg
396b
Green Reg
396c
Blue Reg
394
374
402
R[i] G[i] B[k]

FIG. 12

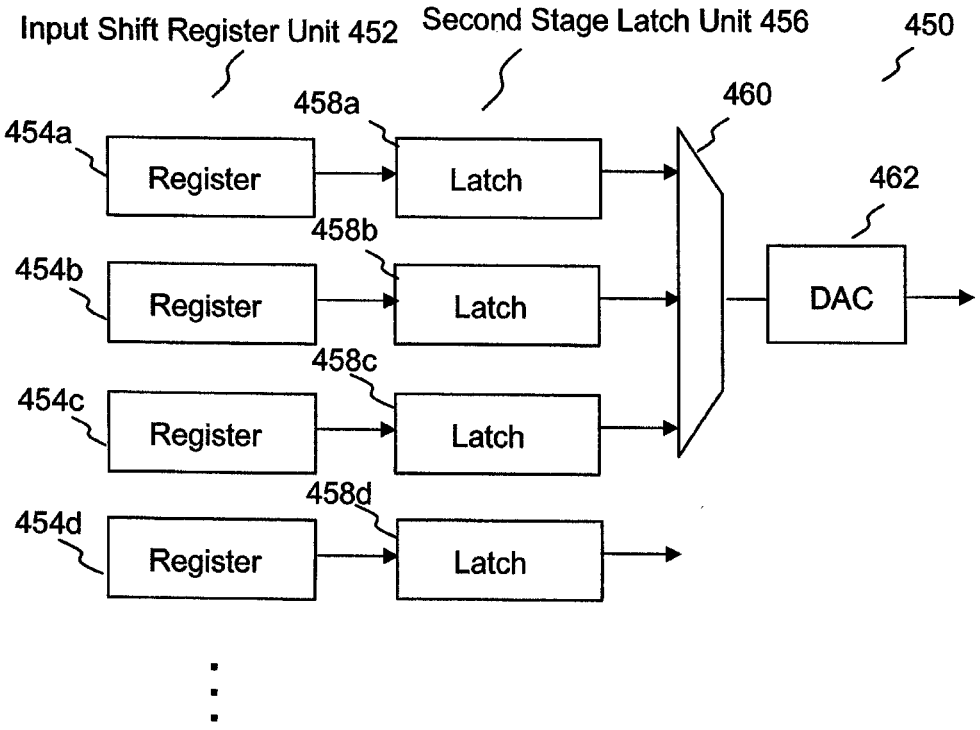

FIG. 13 (Prior Art)

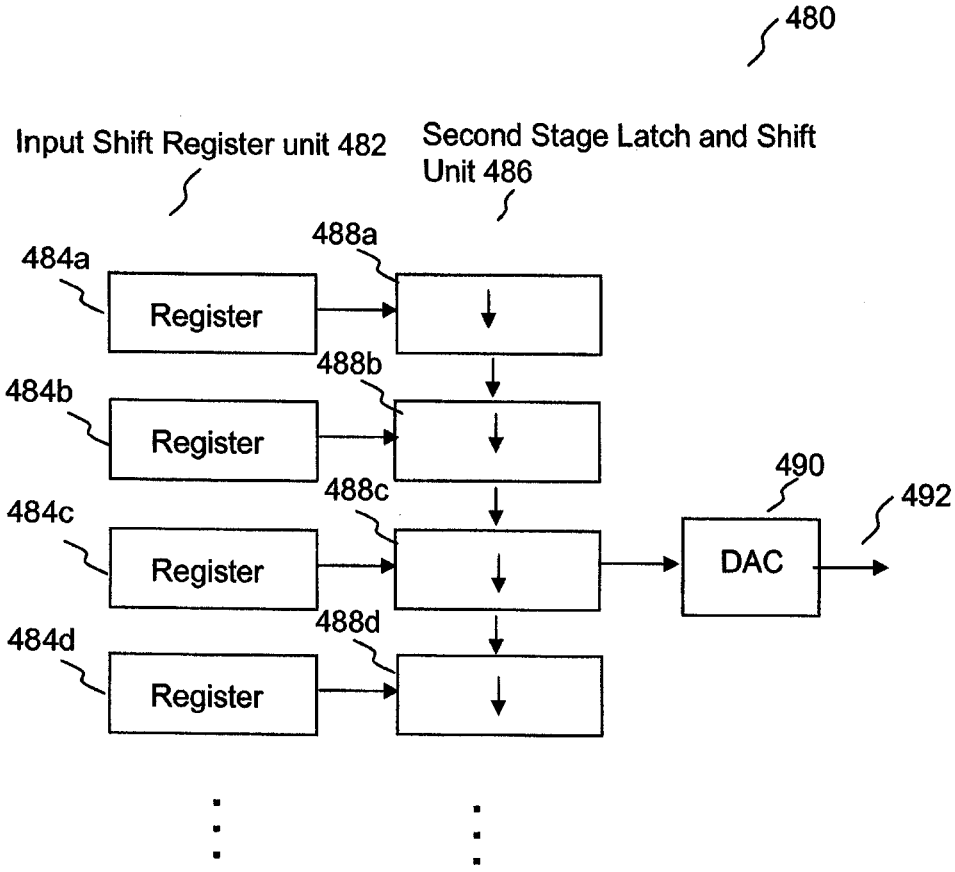
480
Input Shift Register unit 482
Second Stage Latch and Shift Unit 486
484a
Register
488a
484b
Register
488b
484c
Register
488c
484d
Register
488d
490
DAC
492

FIG. 14

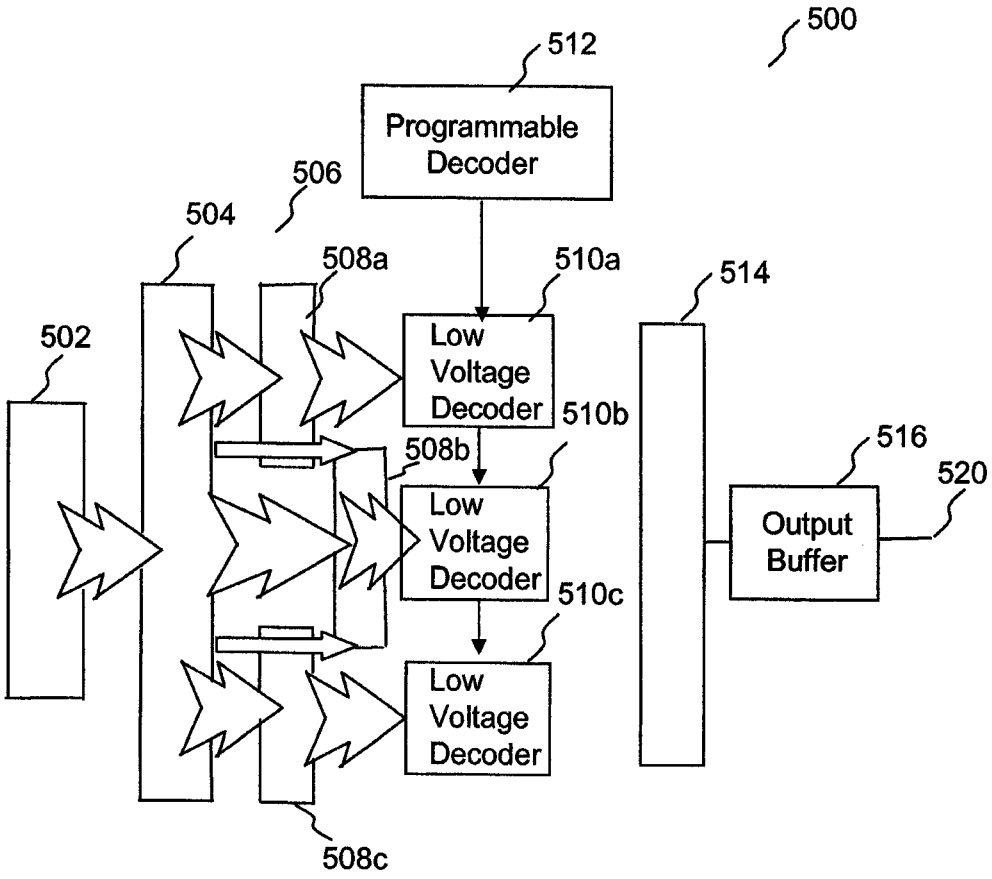
500
512
Programmable Decoder
506
504
508a
510a
514
502
Low Voltage Decoder
510b
508b
516
520
Low Voltage Decoder
Output Buffer
510c
Low Voltage Decoder
508c

FIG. 15

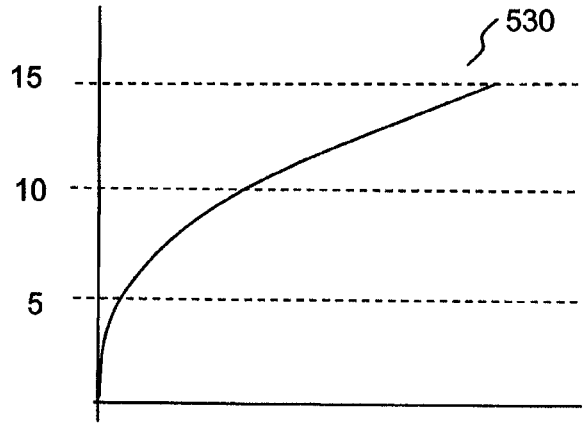

FIG. 16A

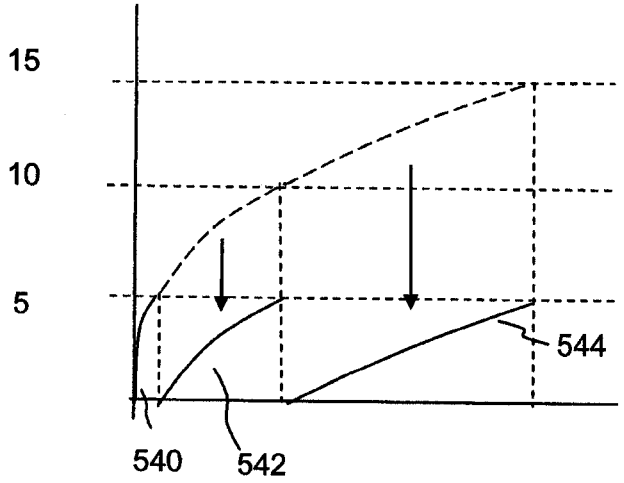

FIG. 16B

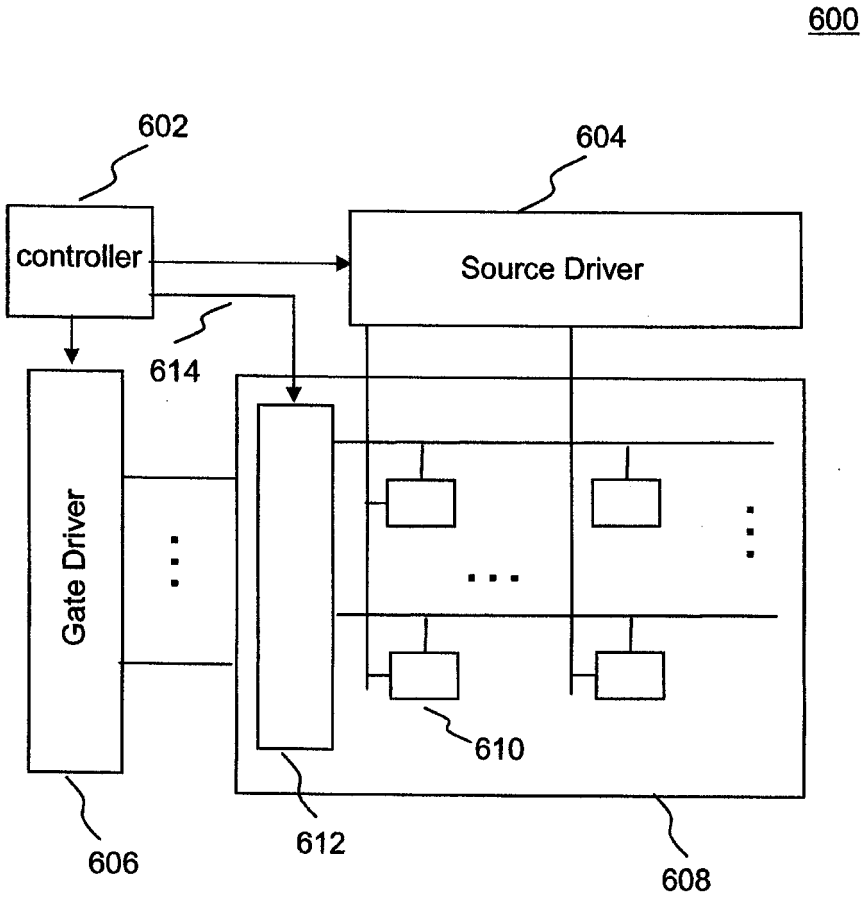
600
602
604
controller
Source Driver
614
Gate Driver
610
606
612
608

FIG. 17

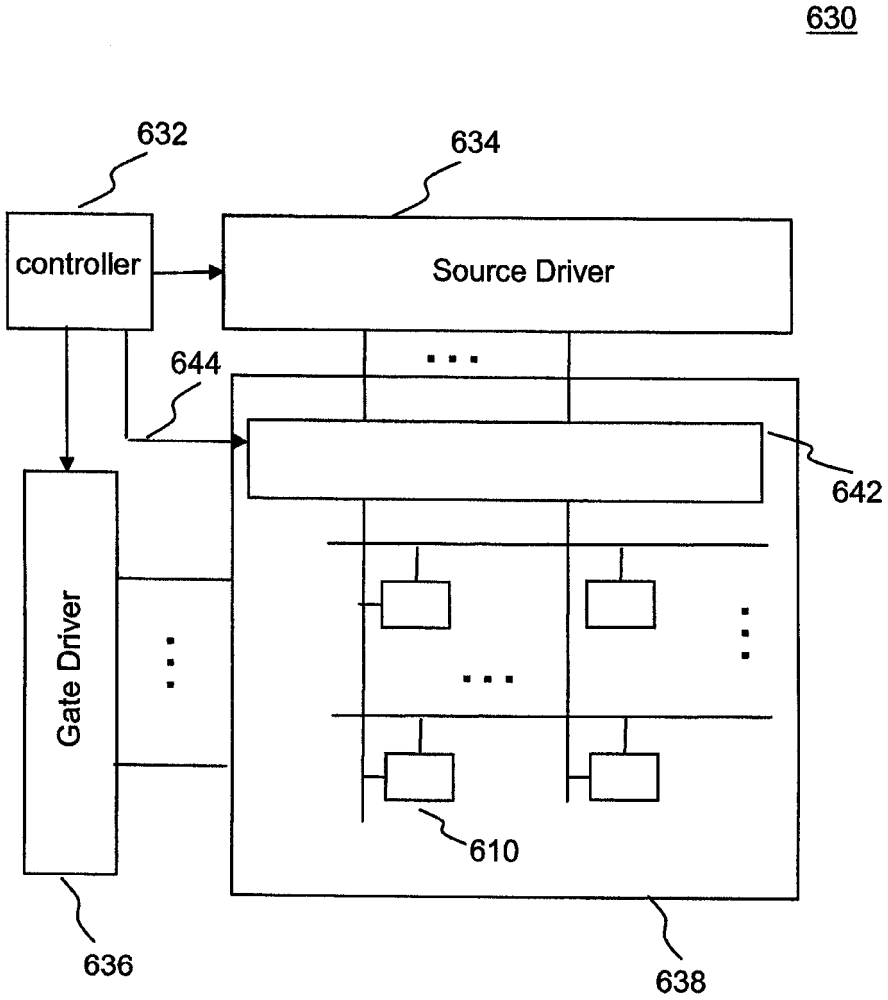
630
632
634
controller
Source Driver
644
642
Gate Driver
610
636
638

FIG. 18

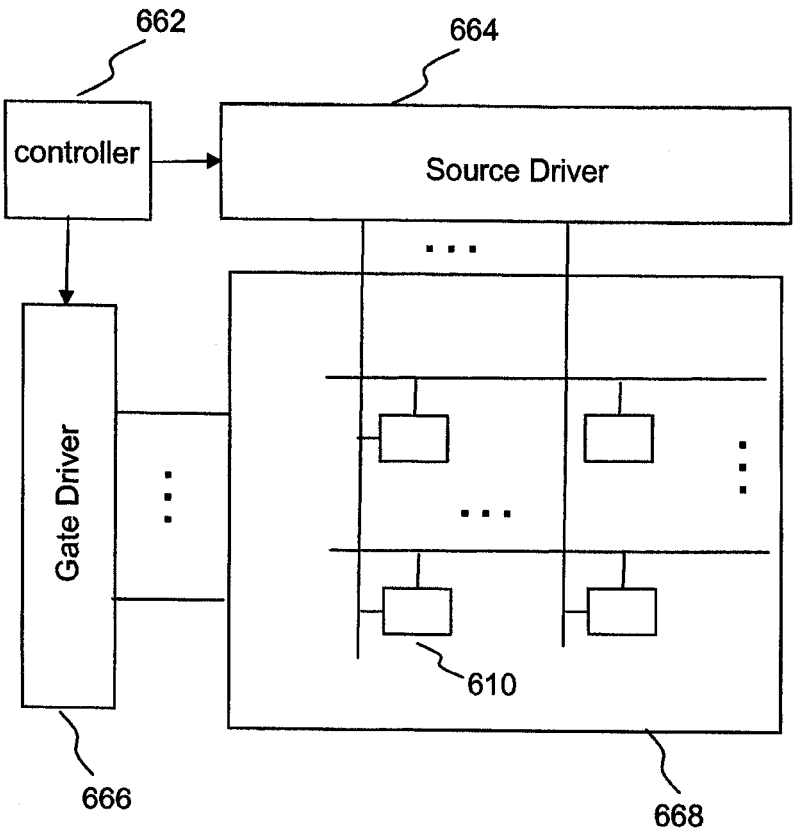
660
662
664
controller
Source Driver
Gate Driver
610
666
668

FIG. 19

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2002080108 A **[0004]**
- WO 2008057369 A1 **[0005]**

专利名称(译)	用于驱动发光显示器的方法和系统		
公开(公告)号	EP2313881A4	公开(公告)日	2011-09-07
申请号	EP2009802309	申请日	2009-07-28
[标]申请(专利权)人(译)	IGNIS INNOVATION INC		
申请(专利权)人(译)	IGNIS INNOVATION公司		
当前申请(专利权)人(译)	IGNIS INNOVATION公司		
[标]发明人	CHAJI G REZA LI KONGNING GUPTA VASUDHA NATHAN AROKIA		
发明人	CHAJI, G. REZA LI, KONGNING GUPTA, VASUDHA NATHAN, AROKIA		
IPC分类号	G09G3/20 G09G3/32 G09G3/36		
CPC分类号	G09G3/3696 G09G3/20 G09G3/3266 G09G3/3275 G09G3/3677 G09G3/3688 G09G2300/0452 G09G2310/0218 G09G2310/0267 G09G2310/027 G09G2310/0286 G09G2310/0294 G09G2310/0297 G09G2320/0276 G09G2320/0673		
优先权	2637343 2008-07-29 CA		
其他公开文献	EP2313881B1 EP2313881A1		
外部链接	Espacenet		

摘要(译)

一种显示系统，包括用于操作面板的驱动器，所述面板具有由多个第一线和至少一个第二线布置的多个像素。所述驱动器包括驱动器输出单元，用于向所述面板提供用于激活所述多个第一驱动器的单个驱动器输出。在单独的线路上，单个驱动器输出在面板上被多路分解以激活每个第一线路。