(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 610 293 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
06.08.2008 Bulletin 2008/32

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **05105436.9**

(22) Date of filing: **21.06.2005**

(54) **Light emitting display and driving device and method thereof**

Lichtemittierende Anzeige und Steuergerät und Steuerverfahren dafür

Dispositif d'affichage électroluminescent et dispositif et méthode de commande pour celui-ci

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU MC NL PL PT RO SE SI SK TR

(30) Priority: **25.06.2004 KR 2004048152**
25.06.2004 KR 2004048153
25.06.2004 KR 2004048154

(43) Date of publication of application:
28.12.2005 Bulletin 2005/52

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Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

Technical Field

[0001] The present invention relates to a light emitting display, a driving device thereof, and a driving method thereof. More specifically, the present invention relates to a light emitting display using an organic light emitting diode (OLED), and a driving method thereof.

Related Art

[0002] In general, an OLED display electrically excites a phosphorous organic compound to emit light, and it voltage-drives or current-drives a plurality of organic emitting cells to display images. The organic emitting cell includes an anode, an organic thin film, and a cathode layer. A method for driving the organic emission cells can be classified as a passive matrix method or as an active matrix method using thin film transistors (TFTs). The passive matrix method provides anodes and cathodes that cross (or cross over) each other, in which method a line to drive the organic emission cells is selected. The active matrix method provides TFTs that access respective pixel electrodes, and a pixel is driven according to a voltage maintained by a capacitance of a capacitor accessed by a gate of a TFT. Depending on the formats of the signals applied to capacitors for establishing the voltage, the active matrix method can be categorized as a voltage programming method or a current programming method.

[0003] The pixel circuit of the voltage programming method has a difficulty in obtaining high gray scales because of deviations of the threshold voltage V_{TH} and carrier mobility, the deviations being caused by non-uniformity in the manufacturing process. For example, in order to represent 8-bit (*i.e.*, 256) gray scales in the case of driving thin film transistors by a voltage of 3V (volts), it is required to apply the voltage to the gate of the thin film transistor with an interval less than a voltage of 12 mV (=3V/256). If the deviation of the threshold voltage of the thin film transistor caused by the non-uniformity in the manufacturing process is 100 mV, it is difficult to represent high gray scales.

[0004] However, the pixel circuit of the current programming method achieves uniform display characteristics when the driving transistor in each pixel has non-uniform voltage-current characteristics, provided that a current source for supplying the current to the pixel circuit is uniform throughout the whole panel.

[0005] However, the pixel circuit of the current programming method involves a long data programming time because of a parasitic capacitance component provided on the data line. In particular, the time for programming the data on the current pixel line is influenced by the voltage state of the data line according to the data of a previous pixel line, and in particular, the data programming time is further lengthened when the data line is charged with a voltage which is very different from the target voltage (the voltage corresponding to the current data). This phenomenon becomes an even greater factor as the gray level becomes lower (near black).

[0006] Document US6417830 discloses a row driver for an active matrix LCD with two shift registers and an OR circuit. Each scan line receives a short precharge pulse and later a long data loading pulse. Simultaneous precharging of plural rows is mentioned. However, it is not disclosed how these pulses may be generated without requiring a shift clock period lower than the horizontal period.

[0007] Document EP1424674 discloses an active matrix organic light emitting display in which each scan line is selected plural times (n-line simultaneous current precharging) for precharging and once for loading of the data value. This is implemented using a standard shift register.

[0008] Document EP1061497 discloses a row driver for an active matrix organic light emitting display which comprises two shift registers and combination logic. Each scan line is selected once to load data and later again to erase the data.

SUMMARY OF THE INVENTION

[0009] It is an aspect of the present invention to reduce the data programming time in a light emitting display based on the current driving method. It is a further aspect of the present invention to reduce the clock frequencies required in a driving device for a light emitting display based on the current driving method.

[0010] The present invention provides a driving device for a light emitting display which includes a plurality of scan lines for transferring a plurality of selection signals, the driving device comprising: a first driver for outputting a plurality of first signals to a plurality of outputs, each first signal having a first integer multiple of first pulses and being shifted by a first period with respect to the preceding first signal; a second driver for outputting a plurality of second signals to a plurality of outputs, each second signal having a plurality of second pulses corresponding to the first pulses shifted by a second period; a third driver for outputting a plurality of third signals to a plurality of outputs in response to the first signals and the second signals, each third signal having a second integer multiple of third pulses and being shifted by the first period with respect to the preceding third signal; a fourth driver for outputting a plurality of fourth signals to a plurality of outputs, each fourth signal having a fourth pulse and being shifted by a third period with respect to the preceding fourth signal; and a fifth driver for outputting the plurality of selection signals in response to the third signals and the fourth signals, each selection signal having a third integer multiple of fifth pulses, each third pulse corresponding to at least one fifth pulse, and having a sixth pulse corresponding to the fourth pulse. The second integer multiple is greater than the first integer multiple,

and the third pulses are shorter than the first pulses.

[0011] The second period may have a width the same as a width of a third pulse. A width between two adjacent first pulses in a plurality of the first pulses may be the same as a width of a first pulse. The second period may have a width shorter than the width of a first pulse. The first integer may correspond to twice the second integer.

[0012] The first driver, the second driver and the fourth driver may respectively comprise a shift register. A cycle of a clock used in the fourth driver may correspond to twice a cycle of a clock used in the first driver and the second driver. Alternatively, a cycle of a clock used in the fourth driver may be the same as a cycle of a clock used in the first driver and the second driver.

[0013] The present invention also provides a light emitting display comprising a display area and a driving device as described above. The display area comprises a plurality of data lines for transferring a data signal, a plurality of scan lines arranged in a direction which crosses a direction of the data lines, and a plurality of pixels respectively coupled to the data lines and the scan lines.

[0014] Each pixel may comprise at least one switch for transferring a data signal from one of the data lines in response to a low level in the selection signal applied to one of the scan lines; a capacitor for charging to a voltage corresponding to the data signal transferred; a transistor for outputting a current according to the voltage charged on the capacitor; and a light emitting element for emitting light according to a magnitude of the current outputted by the transistor.

[0015] The present invention further provides a method for driving a light emitting display which includes a plurality of scan lines for transferring a plurality of selection signals, the method comprising the steps of: outputting a plurality of first signals to a plurality of outputs, each first signal having a first integer multiple of first pulses and being shifted by a first period with respect to the preceding first signal; outputting a plurality of second signals to a plurality of outputs, each second signal having a plurality of second pulses corresponding to the first pulses shifted by a second period; outputting a plurality of third signals to a plurality of outputs in response to the first signals and the second signals, each third signal having a second integer multiple of third pulses and being shifted by the first period with respect to the preceding third signal; outputting a plurality of fourth signals to a plurality of outputs, each fourth signal having a fourth pulse and being shifted by a third period with respect to the preceding fourth signal; and outputting the plurality of selection signals in response to the third signals and the fourth signals, each selection signal having a third integer multiple of fifth pulses corresponding to at least one of the second integer multiple of third pulses, and having a sixth pulse corresponding to the fourth pulse. The second integer multiple is greater than the first integer multiple, and the third pulses are shorter than the first pulses.

[0016] The second period may have a width the same as a width of a third pulse. A width between two adjacent first pulses in a plurality of the first pulses may be the same as a width of a first pulse. The second period may have a width shorter than the width of a first pulse. The first integer may correspond to twice the second integer.

[0017] The step of outputting the plurality of first signals, the step of outputting the plurality of second signals and the step of outputting the plurality of fourth signals may respectively be performed using a shift register. A cycle of a clock used in the step of outputting the plurality of fourth signals may correspond to twice a cycle of a clock used in the step of outputting the plurality of first signals and the step of outputting the plurality of second signals. Alternatively, a cycle of a clock used in the step of outputting the plurality of fourth signals may be the same as a cycle of a clock used in the step of outputting the plurality of first signals and the step of outputting the plurality of second signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings, in which like reference symbols indicate the same or similar components, wherein:

[0019] FIG. 1 is a graph illustrating variations of data programming times versus gray levels to be written in a light emitting display device;

[0020] FIG. 2 is a simplified plan view of a light emitting display according to a first exemplary embodiment of the present invention;

[0021] FIG. 3 is a simplified circuit diagram of a pixel circuit in a light emitting display according to the first exemplary embodiment of the present invention;

[0022] FIG. 4 is a driving timing diagram of a light emitting display according to the first exemplary embodiment of the present invention;

[0023] FIG. 5A shows a current supply state in the precharging stage;

[0024] FIG. 5B shows a current supply state in the data programming stage;

[0025] FIG. 6 shows a scan driver in a light emitting display according to a first comparative example;

[0026] FIG. 7 is a signal timing diagram of a scan driver according to a second comparative example;

[0027] FIG. 8A is a simplified circuit diagram of a first shift register in the scan driver of FIG. 6;

[0028] FIG. 8B is a simplified diagram of a flip-flop used in the shift register in FIG. 8A;

[0029] FIG. 9 is a timing diagram for an output signal of the flip-flop and an output signal of a NOR gate used in the shift register in FIG. 8A;

[0030] FIG. 10 is a simplified circuit diagram of a second shift register in the scan driver of FIG. 6;

[0031] FIG. 11 is a simplified circuit diagram of a first

shift register in the scan driver according to the second comparative example;

[0032] FIG. 12 is a signal timing diagram of the scan driver according to the second comparative example;

[0033] FIGs. 13A and 13B show respective simplified diagrams of the flip-flops used in the shift register of FIG. 11;

[0034] FIG. 14 shows a scan driver according to a second exemplary embodiment of the present invention;

[0035] FIG. 15 is a signal timing diagram of the scan driver according to the second exemplary embodiment of the present invention;

[0036] FIG. 16 is a simplified circuit diagram of a first shift register in the scan driver of FIG. 14;

[0037] FIG. 17 is a simplified circuit diagram of a first shift register in the scan driver according to a third exemplary embodiment of the present invention;

[0038] FIG. 18 is a signal timing diagram of the scan driver according to the third exemplary embodiment of the present invention;

[0039] FIG. 19 shows a scan driver according to a third comparative example;

[0040] FIG. 20 is a signal timing diagram of the scan driver according to the third comparative example;

[0041] FIG. 21 is a simplified circuit diagram of a first shift register in the scan driver of FIG. 19;

[0042] FIG. 22 is a signal timing diagram of a scan driver according to a fourth comparative example;

[0043] FIG. 23 is a simplified circuit diagram of a first shift register in a scan driver according to an fifth comparative example;

[0044] FIG. 24 is a signal timing diagram of the scan driver according to the fifth comparative example; and

[0045] FIG. 25 is a signal timing diagram of a scan driver according to a sixth comparative example.

DETAILED DESCRIPTION OF THE INVENTION

[0046] FIG. 1 is a graph illustrating variations of data programming times versus gray levels to be written in a light emitting display device.

[0047] The time t1 to t7 in FIG. 1 represents the data programming times, and the gray lines (*e.g.*, gray 00 through gray 63) on the right of the graph indicate gray levels of the data programmed to the pixel circuit coupled to the previous pixel line.

[0048] For example, when the gray level of the data programmed to the pixel circuit coupled to the previous pixel line is "8" and the gray level of the data to be programmed to the pixel circuit coupled to the current pixel line is 8 (*i.e.,* a point where a curve meets the horizontal axis), the time needed for data programming is almost "0" since there is no difference between the voltage state of the data line and the target voltage.

[0049] By contrast, the time needed for data programming increases as the difference between the voltage state of the data line and the target voltage increases because the gray level of the data to be currently programmed becomes further away from the gray level of 8.

[0050] Also, the time needed for data programming is inversely proportional to the magnitude of the data current for driving the data line. As such, when the gray level is to be lowered, the data current for driving the data line is reduced, and hence, the data programming time is increased. That is, as can be derived from FIG. 1, when the gray level is lowered (e.g., to near the black level), the data voltage is changed so that is has a large voltage range with a low driving current, and the data programming time is increased.

[0051] In the following detailed description, only certain exemplary embodiments of the present invention and comparative examples are shown and described, simply by way of illustration. As those skilled in the art will realize, the described embodiments may be modified in various different ways, all without departing from the scope of the present invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

[0052] In the context of the present application, to couple one thing to another refers to directly couple a first thing to a second thing, or to couple a first thing to a second thing with a third thing provided therebetween. In addition, to clarify the present invention as shown in the drawings, certain components which are not described in the specification may be omitted, and like reference numerals indicate like components.

[0053] Hereinafter, a light emitting display and a driving method thereof according to exemplary embodiments of the present invention and comparative examples will be described in detail with reference to drawings. In exemplary embodiments of the present invention, the light emitting display is described as an organic light emitting diode (OLED). However, the present invention should not be limited to the OLED display.

[0054] First, a light emitting display according to a first exemplary embodiment of the present invention is described in detail with reference to FIG. 2, which is a simplified plan view of a light emitting display according to a first exemplary embodiment of the present invention.

[0055] As shown in FIG. 2, the light emitting display according to the first exemplary embodiment includes display panel 100, data driver 200, scan driver 300, emission control driver 400, and precharge unit 500.

[0056] Display panel 100 includes a plurality of data lines Y_1 to Y_n arranged in a column direction, a plurality of selection scan lines X_1 to X_m and a plurality of emitting scan lines Z_1 to Z_m arranged in a row direction, and a plurality of pixel circuits 110. The selection scan lines X_1 to X_m transmit selection signals for selecting pixels, and the emitting scan lines Z_1 to Z_m transmit emit signals for controlling an emit period of an organic light emitting element (or OLED). Pixel circuits 110 are formed at pixel areas defined by data lines Y_1 to Y_n and selection scan lines X_1 to X_m.

[0057] Data driver 200 applies a data current I_{data} to the data lines Y_1 to Y_n. Furthermore, data driver 200

applies a precharge current NI_{data} to the data lines Y_1 to Y_n, the precharge current NI_{data} being N times the data current I_{data}. Thus, data driver 200 includes a first current source for generating the data current I_{data} and a second current source for generating the precharge current NI_{data}. The precharge current NI_{data} can be generated from the data current I_{data} by a current mirror circuit or the like. The methods for generating the precharge current are well known to a person of ordinary skill in the art, and thus a detailed description of the method for generating the precharge current is not given. However, data driver 200 can alternatively supply the precharge current NI_{data} and the data current I_{data} to the data lines according to a control signal applied from an external controller (not shown).

[0058] Scan driver 300 sequentially applies the selection signals to the selection scan lines X_1 to X_m so as to select pixel circuits 110. Emit control driver 400 sequentially applies the emit signals to the emitting scan lines Z_1 to Z_m so as to control light emission of the pixel circuits 110.

[0059] Scan driver 300, emit control driver 400 and/or data driver 200 can be electronically coupled to the display panel 100, or can be installed as a chip by means of a tape carrier package (TCP) attached and electronically coupled to display panel 100. They can also be installed as a chip on a flexible printed circuit (FPC) or as a film attached and electronically coupled to display panel 100. In addition, they can be directly installed on a glass substrate of the display panel, or they can also be replaced by a driving circuit on the same layer as that of signal lines, data lines, and thin film transistors (TFTs).

[0060] In the first exemplary embodiment of the present invention, the precharge current NI_{data} corresponding to N times the data current I_{data} is applied to a data line Y_j, before the data current I_{data} is applied to a pixel circuit 110 coupled to the data line Y_j and a selection scan line X_i. Then, when the precharge current NI_{data} is applied to the data line Y_j, a low level selection signal is applied to the pixel circuit 110 coupled to the selection scan line X_i and to N-1 selection scan lines X_{i+1} ~X_{i+N-1} of the pixel circuit 110 adjacent to the pixel circuit in the column direction. Then, only the selection signal applied to the selection scan line X_i is maintained at a low level, and the data current I_{data} is applied to a data line Y_j. As such, the data line Y_j is quickly precharged by the precharge current NI_{data}, which is larger than the data current I_{data}, and then the data current I_{data} is applied to the data line Y_j. Thus, a voltage corresponding to the data current I_{data} is quickly supplied to and charges the pixel circuit 110.

[0061] Hereinafter, referring to FIGs. 3, 4, 5A, and 5B, the operation of the light emitting display according to the first exemplary embodiment of the present invention will be described in detail. For ease of description, N is assumed to be 5, that is, the precharge current is assumed to be 5 times that of the data current.

[0062] First, pixel circuit 110 of the light emitting display according to the first exemplary embodiment of the present invention is described in detail with reference to FIG. 3.

[0063] FIG. 3 is a simplified circuit diagram of a pixel circuit in a light emitting display according to the first exemplary embodiment of the present invention. FIG. 3 shows the pixel circuit coupled to the jth data line Y_j, the ith selection scan line X_i, and emitting scan line Z_i.

[0064] As shown, pixel circuit 110 according to the first exemplary embodiment of the present invention includes organic light emitting element OLED, transistors T1, T2, T3 and T4, and capacitor C. Transistors T1, T2, T3, and T4 are shown as PMOS transistors in FIG. 3, but transistor types of the present invention are not restricted to PMOS transistors. The transistors can be TFTs which have a gate electrode, a drain electrode, and a source electrode formed on the glass substrate of display panel 100 as a control electrode and two main electrodes, respectively.

[0065] In detail, the three electrodes (or terminals) of transistor T1 are respectively coupled to the selection scan line X_i, data line Y_j, and the gate of transistor T3. Transistor T1 transmits the data current I_{data} provided by data line Y_j to the gate of transistor T3 in response to the selection signal provided by selection scan line X_i. The source of transistor T3 is coupled to the supply voltage VDD, and capacitor C is coupled between the gate and source of transistor T3. Transistor T2 is coupled between the drain of transistor T3 and data lines Y_j, and transistors T1 and T2 diode-connect transistor T3 in response to the selection signal provided by selection scan lines X_i. Transistors T1 and T2 may be directly connected between the gate and drain of transistor T3.

[0066] At this point, data current I_{data} is applied to data line Y_i, and selection signal (select[1] in FIG. 4) provided by selection scan line X_i is converted to low level. Transistors T1 and T2 are turned on, and transistor T3 is diode-connected. Then, data current I_{data} is applied to and charges capacitor C, the gate voltage potential of transistor T3 is lowered, and current flows from the source to the drain of transistor T3. When the voltage charge on capacitor C is increased, and the drain current of transistor T3 increases so as to be the same as data current I_{data}, the charge on capacitor C is stopped, and the voltage charge on capacitor C is stabilized. Thus, a voltage corresponding to data current I_{data} provided by data line Y_j is charged on capacitor C.

[0067] Next, the selection signal (select [1] in FIG. 4) provided by the selection scan line X_i is converted to a high level, and the emit signal (emit[1] in FIG. 4) provided by the emitting scan line Z_i is converted to a low level. Then, transistors T1 and T2 are turned off, transistor T4 coupled between transistor T3 and the organic light emitting element OLED is turned on, and the current provided by transistor T3 is transferred to the organic light emitting element OLED. The cathode of the organic light emitting element OLED is coupled to a voltage source VSS which is lower than a supply voltage VDD, and the organic light

emitting element OLED emits light in response to the current supplied via transistor T4. The current I_{OLED} transmitted to the organic light emitting element OLED can be given in Equation 1 according to the voltage charged on capacitor C connected to transistor T3.

Equation 1

$$I_{OLED} = \frac{\beta}{2}(V_{GS} - V_{TH})^2 = I_{data}$$

where V_{GS} is the voltage between the gate and the source of transistor T3, VTH is a threshold voltage at transistor T3, and β is a constant.

[0068] Next, referring to FIGs. 4, 5A, and 5B, the operation of the light emitting display according to the first exemplary embodiment of the present invention will be further described in detail.

[0069] FIG. 4 is a driving timing diagram of a light emitting display according to the first exemplary embodiment of the present invention; FIG. 5A shows a current supply state in the precharging stage; and FIG. 5B shows a current supply state in the data programming stage. In FIGs. 5A and 5B, five pixel circuits coupled to the first selection scan line thru the fifth selection scan line X_1 to X_5 and the five emitting scan lines Z_1 to Z_5 are shown for convenience. In FIG. 4, and in FIGs. 5A and 5B, select[i] indicates a selection signal applied to the selection scan line X_i, and emit[i] indicates an emit signal applied to the emitting scan line Z_i. Reference numerals X_i and Z_i corresponding to the selection scan lines and the emitting scan lines are omitted.

[0070] As shown in FIG. 4, when the data is programmed in the pixel circuit coupled to the first selection scan line X_1, low level selection signals select[1] to select [5] are supplied to the first thru fifth selection scan lines X_1 to X_5, respectively. At the same time, data driver 200 applies the precharge current $5I_{data}$ to the data line Y_j so as to perform a precharge operation during a precharge period Tp.

[0071] Transistors T1 and T2 of the pixel circuits 110 coupled to the selection scan lines X_1 to X_5 are turned on in response to the low level selection signals select [1] to select[5], and thus transistor T3 assumes a diode-connected state. As such, as shown in FIG. 5A, the precharge current $5I_{data}$ flows on the data line Y_j. At this point, when the ratio W/L (hereinafter, transistor size) of the channel width W and channel length L of transistors T3 in the five pixel circuits are the same, 1/5 of the precharge current $5I_{data}$ provided by the data line Y_j is respectively supplied to the five pixel circuits. That is, the data current is supplied to each of the five pixel circuits. Then, the voltage V_{GS} of Equation 1 is charged on capacitor C. That is, the precharge voltage from the gate voltage V_G to the gate-source voltage V_{GS} is applied to the data lines Y_j. However, when the precharge period Tp is short, the precharge voltage may not achieve a suitable voltage which should be applied to the data lines Y_j by the data current I_{data}. However, the precharge voltage $5I_{data}$ is larger than the data current I_{data}, and thus a voltage corresponding to the data current I_{data} can be applied to the data line Y_j even though the precharge period Tp is short.

[0072] Next, as shown in FIG. 4, the selection signal select[1] applied to the first selection scan line X_1 is maintained at a low level, but the other selection signals select [2] to select[5] are changed to the high level. At the same time, data driver 200 applies the data current, the 1/5 of the precharge current $5I_{data}$, to the data line Y_j. Then, as shown in FIG. 5B, transistors T1 and T2 coupled to the first selection scan line X_1 are turned on, and the data current I_{data} is transmitted to transistor T3. Thus, a voltage corresponding to the data current I_{data} is charged on capacitor C of the pixel circuit coupled to the first selection scan lineX_1 so as to perform the data programming operation. At this point, the precharge voltage (the voltage corresponding to the data current I_{data}) has been applied to the data line Y_j by the previous precharge operation, and thus a voltage corresponding to the data current I_{data} can be quickly charged on capacitor C.

[0073] Then, when the data programming operation is completed, the selection signal select[1] is turned to a high level, and transistor T4 is turned on by the low level of the emit signal emit[1] applied by the emitting scan line Z_1. Then, the current I_{OLED} provided by transistor T3 is supplied to the organic light emitting element OLED through transistor T4, and the organic light emitting element OLED emits light corresponding to the current I_{OLED}.

[0074] As such, when the emit operation of the pixel circuit coupled to the first selection scan line X_1 is performed, the low levels of selection signals select[2] to select[6] are applied to selection scan lines X2 to X6, respectively. The precharge current $5I_{data}$ equal to 5 times the data current I_{data}, and corresponding to the pixel circuit coupled to the selection scan line X2, is applied to the data line Y_j so as to perform a precharge operation on the pixel circuit coupled to the second selection scan line X2. Then, the selection signals select[3] to select[6] are converted to a high level after the precharge operation, and a data current I_{data} corresponding to the pixel circuit coupled to the selection scan line X2 is applied to the data line Y_j so as to perform the data programming operation on the pixel circuit coupled to the second selection scan line X2.

[0075] As such, in the first exemplary embodiment of the present invention, before data is programmed in a pixel circuit coupled to an ith selection scan line X_i, a precharge current NI_{data} corresponding to 5 times the data current I_{data} is applied to the pixel circuit when the selection signal is applied to the ith to (i+-1)th selection scan lines X_i to X_{i+N-1}. Then, if the sizes of transistors T3 in pixel circuits arranged in the column direction are the

same, a current corresponding to 1/N of the precharge current NI_{data} is supplied to N pixel circuits coupled to the ith to (i+-1)th selection scan lines X_i to X_{i+N-1} so as to perform a precharge operation. Next, when the selection signal of the ith selection scan line X_i is maintained at a low level, the selection signals of the (i+1)th to (i+-1)th selection scan lines X_i to X_{i+N-1} turn to a high level, while the data current I_{data} is applied to the data line Y_j so as to perform the data programming operation.

[0076] As such, the first exemplary embodiment of the present invention can program data in the pixel circuit by precharging a data line by means of a precharge current which is larger than the data current before the data is programmed. The data programming can be achieved in a predetermined period of time.

[0077] Hereinafter, with respect to the selection signal select[i] of FIG. 4, "precharge pulse" means a pulse that is of a low level only during a precharge period, and "selection pulse" means a pulse that is of a low level during a precharge period and a data programming period. Then, as shown in FIG. 4, a selection signal select[i] applied to the selection scan line X_i has one selection pulse and at least one precharge pulse per cycle. In the selection signal select[i], the interval of start time points of two adjacent precharge pulses is the same as the interval of starting points of a selection pulse and a precharge pulse adjacent to the selection pulse. Furthermore, the selection signal select[i] has a number of precharge pulses corresponding to the number of pixels used in the precharge, excluding the pixel to which data is programmed. In addition, the precharge period Tp is the same as the width of the precharge pulse.

[0078] Hereinafter, a driver for generating the above driving waveform is described in detail with reference to FIG. 6 thru FIG. 25.

[0079] In the exemplary embodiments of the present invention and comparative examples, a selection signal is generated by combining an output signal from a shift register for generating a precharge pulse and an output signal from a shift register for generating a selection pulse. Hereinafter, a particular shift register for generating the precharge pulse is described in detail.

[0080] Furthermore, in exemplary embodiments of the present invention and comparative examples, the number of selection scan lines X_1 to X_m is m, and a selection signal select[i] with four precharge pulses is described, if not particularly mentioned to the contrary. That is, four neighboring pixel circuits are used in the precharge of a pixel circuit for data programming.

[0081] FIG. 6 shows a scan driver in a light emitting display according to a first comparative example, and FIG. 7 is a signal timing diagram of a scan driver according to a second comparative example.

[0082] As shown in FIG. 6, scan driver 300 of the first comparative example includes two shift registers 310 and 320, and m NOR gates NOR11 to NOR1m.

[0083] As shown in FIG. 6 and FIG. 7, shift register 310 receives clock signal VCLK11 and a starting signal VSP11, shifts output signals out11[1] to out11[4m-3] by half of a cycle of clock signal VCLK11, and sequentially provides the shifted output signals. The output signal out11[i] has four high level pulses in one cycle. The width of the high level pulse is the same as the half clock cycle of clock signal VCLK11, and the cycle of the high level pulse is twice the clock cycle of clock signal VCLK11. At this point, the precharge period Tp is determined by the width of the high level pulse. In addition, the (4i-3)th output signal out11[4i-3] of the output signals out11[1] to out11 [4m-3] becomes an input signal scan11[i] of the ith NOR gate NOR_{1i}, i being an integer from 1 to m.

[0084] Shift register 320 receives clock signal VCLK12 and starting signal VSP12, shifts output signals scan12 [1] to scan12[m] having one high level pulse by a half of a clock cycle of clock signal VCLK12, and sequentially provides the shifted output signals. The width of the high level pulse of the output signal scan12[i] is the same as the half clock cycle of clock signal VCLK12, and the clock cycle of clock signal VCLK12 is four times the clock cycle of clock signal VCLK11. A start time point of the high level pulse in the output signal scan12[i] is half of a clock cycle of clock signal VCLK12 away from a start time point of the last high level pulse in the output signal scan11[i].

[0085] NOR gate NOR_{1i} performs a NOR operation on the output signal scan11[i] of shift register 310 and the output signal scan12[i] of shift register 320, and outputs the selection signal select[i]. The output signal select[i] of NOR gate NOR_{1i} has a low level by virtue of the NOR operation when at least one of two output signals scan11 [i] and scan12[i] has a high level. Thus, the output signal select[i] has four low level pulses (precharge pulse) and then one low level pulse (selection pulse) in one cycle as shown in FIG. 7. Thus, as shown in FIG. 4 and FIG. 7, the selection signal select[i] applied to the selection scan line X_i can be generated as the output signal of the NOR gate NOR_{1i}.

[0086] Next, shift registers 310 and 320 for generating the output signals out11[i], scan11[i], and scan 12[i] explained in FIG. 6 and FIG. 7 are described with reference to FIGs. 8A to 13B.

[0087] FIG. 8A is a simplified circuit diagram of a first shift register in the scan drive of FIG. 6, FIG. 8B is a simplified diagram of a flip-flop used in the shift register in FIG. 8A, and FIG. 9 is a timing diagram for an output signal of the flip-flop and an output signal of a NOR gate used in the shift register in FIG. 8A. More specifically, FIG. 8A is a simplified circuit diagram of shift register 310 in the scan driver of FIG. 6; FIG. 8B is a simplified diagram of a flip-flop used in the shift register in FIG. 8A; and FIG. 9 is a timing diagram for an output signal of the flip-flop and an output signal of the NOR gate used in the shift register of FIG. 8A. In FIGs. 8A and 8B, VCLK11b indicates an inverted clock signal VCLK11. However, VCLK11b is omitted in the signal timing diagram of FIG. 7 and FIG. 9.

[0088] As shown in FIG. 8A, shift register 310 includes (4m-2) flip-flops FF_{11} to $FF_{1(4m-2)}$ and (4m-3) NOR gates

NOR_{21} to $NOR_{2(4m-3)}$. The output signals of each NOR gate NOR_{2k} become the output signals out11[k] of shift register 310, k being an integer from 1 to (4m-3).

[0089] In FIG. 8A, the input signal of the first flip-flop FF_{11} is the start signal VSP11 of FIG. 7 and FIG. 9, and the output signal SR_k of the kth flip-flop FF_{1k} is the input signal of the (k+1)th flip-flop $FF_{1(k+1)}$. The kth NOR gate NOR2k performs a NOR operation on the output signal SR_{1k} of the kth flip-flop FF_{1k} and the output signal $SR_{1(R+1)}$ of the (k+1)th flip-flop $FF_{1(R+1)}$ so as to generate the input signal out11[k].

[0090] The flip-flop FF_{1k} outputs input signal in as it is inputted when clock clk is at a high level, but the flip-flop FF_{1k} latches the input signal in inputted when the clock clk was at a high level, and outputs the resultant signal. Furthermore, the clock clk is inverted in the two adjacent flip-flops FF_{1k} and $FF_{1(k+1)}$, and output signal $SR_{1(R+1)}$ of the flip-flop $FF_{1(k+1)}$ is the output signal SR_{1k} of the flip-flop FF_{1k} shifted by half of a clock cycle of clock signal VCLK1. That is, the clock signals VCLK11 and VCLK11 b are inputted to the two flip-flops FF_{1k} and $FF_{1(k+1)}$ in the opposite direction.

[0091] In detail, in FIG.8A, the flip-flop FF_{1k} which is located at an odd-numbered position in the column direction receives the clocks VCLK11 and VCLK11b as inner clocks clk and clkb, respectively. The flip-flop FF_{1k} which is located at an even-numbered position in the column direction receives the clocks VCLK11 and VCLK11 b as inner clocks clkb and clk, respectively. The starting signal VSP11, which is an input signal in of flip-flop FF_{11}, has four low level pulses in one cycle. The low level pulse corresponds to a high level of the clock VCLK11 per two clocks VCLK11 of the interval. Then, the flip-flops FF_{11} to $FF_{1(4m-2)}$ can shift output signals SR_1 to SR_{4m-2} having four low level pulses per cycle by half of a clock cycle of clock VCLK11, and sequentially output the output signals.

[0092] The kth NOR gate NOR2k performs a NOR operation on output signals SR_k and SR_{k+1} of the flip-flops FF_{1k} and $FF_{1(k+1)}$, respectively, and thus the kth NOR gate NOR2k outputs a high level pulse when both output signals SR_k and SR_{k+1} are at a low level. The output signal SR_{k+1} is the output signal SR_k shifted by half of a clock cycle of clock VCLK11. Thus, as shown in FIG. 9, the output signal out11[k] of the NOR gate NOR2k has a high level pulse in half of a cycle of clock VCLK11. The output signal out11[k+1] of NOR gate $NOR_{2(k+1)}$ is the output signal out11[k] of NOR gate NOR2k shifted by half of a clock cycle of clock VCLK11. The (4i-3)th output signal out11[4i-3] of output signals out11[1] to out11[4m-3] of NOR gates NOR21 to NOR2(4m-3) is selected as a final output signal scan11[i] of shift register 310, i being an integer from 1 to m.

[0093] Next, referring to FIG. 8B, one example of flip-flop FF_{1k} used in shift register 310 of FIG. 8A is described.

[0094] As shown in FIG. 8B, the flip-flop FF_{1k} includes clock inverter 311a located at the input terminal, inverter 311b forming a latch, and clock inverter 311c. When clock clk is at a high level, clock inverter 311 a inverts the input signal in and outputs the resultant signal, while inverter 311b inverts the output signal of clock inverter 311a and outputs the resultant signal. When clock clk is at a low level, the output of clock inverter 311a is cut off, the output of inverter 311b is inputted to clock inverter 311c, and the output of clock inverter 311c is inputted to inverter 311b to form a latch. Then, the output signal of inverter 311b becomes the output signal of the flip-flop FF_{1k}. As such, the flip-flop FF_{1k} outputs the input signal in, as it is inputted when clock clk is at a high level, and the flip-flop FF_{1k} latches the input signal in, inputted when the clock clk was at a high level, and outputs the resultant signal.

[0095] Next, the construction and operation of shift register 320 of FIG. 6 is described with reference to FIG. 10, which is a simplified circuit diagram of a second shift register in the scan driver of FIG. 6. FIG. 10 shows a simplified circuit diagram of shift register 320. In FIG.10, VCLK12b indicates an inverted signal of clock VCLK12. However, VCLK11b is omitted in the signal timing diagram of the FIG. 7.

[0096] As shown in FIG. 7, shift register 320 shifts a high level pulse by half of a clock cycle of clock VCLK12 and outputs the resultant signal, as does shift register 310. The high level pulse has a width of half of a clock cycle of clock VCLK12. Thus, a shift register having the same function as the shift register 310 can be used. Hereinafter, the difference between the two shift registers 310 and 320 is described. As shown in FIG. 7, the clock cycle of clock VCLK12 is four times the clock cycle of clock VCLK11.

[0097] As shown in FIG. 10, shift register 320 has the same construction as the shift register 310, excluding the number of flip-flops and NOR gates, as well as the start signal and clock used.

[0098] In detail, shift register 320 includes (m+1) flip-flops FF_{21} to $FF_{2(m+1)}$, and m NOR gates NOR_{31} to NOR_{3m}. An output signal of each NOR gate NOR_{3i} becomes the output signal scan12[i] of shift register 320, i being an integer from 1 to m. An input signal of a first flip-flop FF_{21} is a starting signal VSP12 of FIG. 7, and an output signal of the ith flip-flop FF_{1i} becomes the input signal of the (i+1)th flip-flop $FF_{2(i+1)}$. The ith NOR gate NOR_{3i} performs a NOR operation on the output signal of the ith flip-flop FF_{2i} and the output signal of (i+1)th flip-flop FF2(i+1), and outputs the resultant signal scan12[i].

[0099] The flip-flop FF_{2i} which is located at an odd-numbered position in the column direction in FIG. 10 receives the clocks VCLK12 and VCLK12b as inner clocks clk and clkb, respectively. The flip-flop FF_{2i} which is located at an even-numbered position in the column direction receives the inverted clocks VCLK12 and VCLK12b as inner clocks clk and clkb, respectively. The starting signal VSP12 is established so as to have one low-level pulse when the clock VCLK12 is at a high level. Furthermore, a start time point of the high level pulse in the output signal scan12[i] is established so as to be half of a clock cycle of clock VCLK12 away from a start time point of

the last high level pulse in the output signal scan11[i] of shift register 310. As such, shift register 320 shifts output signals scan12[1] to scan12[m] by half of a clock cycle of clock VCLK12 and outputs the resultant signal. The output signals scan12[1] to scan12[m] have a high level pulse, the cycle of which is half of a clock cycle of clock VCLK12.

[0100] The ith NOR gate NOR_{1i} of scan driver 300 performs a NOR operation on the ith final output signal scan11[i] and the ith output signal scan12[i] of shift register 320, and outputs the resultant signal. Thus, the selection signal select[i] may include four precharge pulses and a selection pulse.

[0101] As such, in FIG. 6 thru FIG. 10, the width of the selection pulse is four times the width of a precharge pulse. However, scan driver 300 of FIG. 6 thru FIG. 10 may generate selection signals having different precharge pulse widths.

[0102] As mentioned above, the width of the precharge pulse is determined by the output of the flip-flop FF_{1k}, and thus a low level pulse of the output signal SR_k of the flip-flop FF_{1k} is assumed to have the narrowest width so as to lower the frequency of the clock VCLK11. That is, the width of the low level pulse of the output signal SR_k of the flip-flop FF_{1k} is assumed to be the same as the width of one clock cycle VCLK11.

[0103] Under the above assumption, a cycle of a low level pulse of the output signal SR_k of the flip-flop FF_{1k} is always n times the width, n being an integer of more than 2. Then, a cycle of a high level pulse in the output signal out11[k] of the NOR gate NOR2k becomes 2n times the width (that is, an even number of times more than 4). Thus, the width of the precharge pulse in the output signal scan11[i] is always 1/2n times the cycle. When a clock cycle of clock VCLK12 is 2n times a clock cycle of clock VCLK11, the width of selection pulse can be 2n times the width of the precharge pulse, and the interval by which the selection pulse is shifted may be the same as the cycle of the precharge pulse. The output signal out11[k] of shift register 310 is shifted by half of a clock cycle of clock VCLK11 and is outputted. Thus, the total [2n×i-(2n-1)]th output signal out[2nxi-(2n-1)] is selected as the final output signal scan11[i] of shift register 310.

[0104] Next, a comparative example wherein the width of a selection pulse may be an even number of times, or less than at most 3 times, the width of a precharge pulse is described in detail with reference to FIG. 11 and FIG. 12.

[0105] FIG. 11 is a simplified circuit diagram of a first shift register in the scan driver according to the second comparative example, and FIG. 12 is a signal timing diagram of the scan driver according to the second comparative example. More specifically, FIG. 11 shows a simplified circuit diagram of shift register 310' according to a second comparative example, and FIG. 12 shows a signal timing diagram of a scan driver according to the second comparative example. In FIG.11, VCLK11b' indicates an inverted signal of clock VCLK11'. However, VCLK11b' is omitted in the signal timing diagram of FIG. 12. Furthermore, for ease of description, a cycle of the precharge pulse is three times the width in the second comparative example. The construction and operation of shift register 320 and NOR gates NOR_{11} to NOR_{1m} may be the same as those in the first comparative example, and thus the descriptions for those are omitted here.

[0106] As shown in FIG. 11, shift register 310' includes (3m-2) flip-flops FF_{31} to $FF_{3(3m-2)}$. Output signals of each of the flip-flops FF_{31} to $FF_{3(3m-2)}$ become the output signals out11 [1]' to out11 [3m-2]' of shift register 310'.

[0107] The flip-flop FF_{3k} receives the clock signals VCLK11' and VCLK11b' as inner clocks clk and clkb, respectively. The flip-flop FF_{3k} receives an input signal when clock clk is at a low level, while the flip-flop FF_{3k} outputs an input signal latched in a previous clock clk cycle. The flip-flop FF_{3k} latches the signal inputted at a low level, and outputs the resultant signal when clock clk is at a high level. As a result, the flip-flop FF_{3k} delays the signal inputted at a low level of clock clk by half of a clock cycle of clock clk, and outputs the resultant signal during one clock cycle of clock clk.

[0108] As shown in FIG. 12, the output signal out11[1]' of the flip-flop FF31 has four high level pulses per cycle. The width of the high level pulse is the same as a clock cycle of clock VCLK11', and the cycle is three times the width. A start signal VSP11', which is an input signal in of the flip-flop FF31, has three high level pulses per cycle. This high level pulse corresponds to a low level of clock VCLK11' per three clocks VCLK11'. Then, the flip-flop FF_{3k} shifts the output signal out11[k]' having four high level pulses per cycle by one clock cycle of clock VCLK11', and sequentially outputs the resultant signals. The (3i-2)th output signal out11[3i-2]' of output signals out11[k]' of the flip-flop FF_{3k} is selected as the final output signal scan11[i]', i being an integer from 1 to m.

[0109] As such, when the width of the high level pulse is established to be one clock cycle of clock VCLK11' in the output signal scan11[i]' of shift register 310', a cycle of the high level pulse can be established to be more than twice the width of the high level pulse (three times in FIG. 12). Since the high level pulse corresponds to a precharge pulse in the output signal scan11[i]', the width Tp of the precharge pulse is always 1/n times (1/3 times in FIG. 11) the cycle, n being an integer of more than 2. When a clock cycle of clock VCLK12 of the shift register 320 is established to be 2n times (six times in FIG. 11) the clock VCLK11' of shift register 310', the width of the selection pulse may be n times (three times in FIG. 11) the width of the precharge pulse, while the selection pulse may be shifted by an interval of the cycle of the precharge pulse.

[0110] When a cycle of the high level pulse is n times the width in output signal out11[k]' of shift register 310', a total of [nxm-(n-1)] output signals out11[k]' are required in shift register 310'. The [nxi-(n-1)]th output signal out1 [nxi-(n-1)]' of the latter output signals becomes the final

output signal scan11[i] of shift register 310'.

[0111] As such, when the cycle of the precharge pulse is established to be an odd number of times or less than 3 times the width, shift register 310' can be used according to the second comparative example. Shift register 310', according to the second comparative example, can be used when the cycle of the precharge pulse is an even number of times of more than four times the width. However, its construction becomes complicated and the frequency of the clock VCLK11' is increased in comparison with shift register 310 as described in the first comparative example.

[0112] Next, one example of a flip-flop used in the shift register of FIG. 11 is described with reference to FIGs. 13A and 13B.

[0113] FIGs. 13A and 13B show respective simplified diagrams of the flip-flops used in the shift register of FIG. 11. The flip-flop FF_{3k} of FIG. 13A and FIG. 13B is formed as a master/slave type of latch. Clocks VCLK11' an d VCLK11 b' are inputted to inner clocks clk and clkb, respectively, of the flip-flop FF_{3k}.

[0114] As shown in FIG. 13A, in master latch 313, PMOS transistor 313a located in the input terminal transfers the input signal in to inverter 313b in response to a low level of one clock cycle of clock clk, and inverter 313b inverts the output signal of PMOS transistor 313a and outputs the resultant signal as an output signal of master latch 313. Furthermore, inverter 313c inverts the output signal of inverter 313b, and outputs the resultant signal. PMOS transistor 313d transfers the output signal of inverter 313c to inverter 313b in response to a low level of the clock clk, that is, a high level of one clock cycle clkb. In other words, master latch 313 inverts the input signal inputted during a low level of the clock clk, and outputs the resultant signal during one clock cycle of clock clk.

[0115] Next, in slave latch 314, PMOS transistor 314a located at the input terminal transfers the output signal of master latch 313 to inverter 314b in response to a low level of an inverted clock clkb, and inverter 314b inverts the output signal of PMOS transistor 314a and outputs the resultant signal as an output signal of slave latch 314. Furthermore, inverter 314c inverts the output signal of inverter 314b and outputs the resultant signal, and PMOS transistor 314d transfers the output signal of inverter 314c to inverter 314b in response to a low level of the clock clk. That is, slave latch 314 inverts the output signal of master latch 313 during a high level of the clock clk, and outputs the resultant signal during one clock cycle of clock VCLK1.

[0116] Therefore, the flip-flop FF_{3k} of FIG. 13A may delay the input signal inputted during a low level of the clock VCLK11' by half of a clock cycle of clock VCLK11', and outputs the resultant signal during one clock cycle of clock VCLK11'.

[0117] In contrast with FIG. 13A, a master and a slave of the flip-flop FF_{3k} may be formed with the same construction as the flip-flop of FIG. 8B, as shown in FIG. 13B. At this time, master latch 315 uses the clocks clk and clkb in a method contrasted with the flip-flop in FIG. 8B, and slave latch 316 uses the clocks clk and clkb in the same method as the flip-flop in FIG. 8B.

[0118] Master latch 315 outputs the input signal in inputted during a low level of the clock clk during one clock cycle, and slave latch 316 outputs the output signal of master latch 315 during a high level of the clock clk during one clock cycle of clock clk. Thus, the flip-flop FF_{3k} of FIG. 13B delays the input signal in during a low level of the clock VCLK11' by half of a clock cycle of clock VCLK11', and outputs the resultant signal during one clock cycle of clock VCLK11'.

[0119] As explained above, scan drivers 300 according to the first and second comparative examples shift a first output signal having a high level pulse corresponding to the precharge pulse by an interval corresponding to the width of the high level pulse, and sequentially output the resultant signal. Scan drivers 300 select a signal shifted by a predetermined interval corresponding to the cycle of the high level pulse of the first output signals, and use the signal as the precharge pulse.

[0120] FIG. 14 shows a scan driver according to a second exemplary embodiment of the present invention, and FIG. 15 is a signal timing diagram of the scan driver according to the second exemplary embodiment of the present invention.

[0121] As shown in FIG. 14, scan driver 300' according to the second exemplary embodiment includes: three shift registers 330, 340, and 350; a plurality of XOR gates XOR_{11} to XOR1m; and a plurality of NOR gates NOR41 to NOR4m.

[0122] As shown in FIG. 14 and FIG. 15, shift register 330 receives a clock signal VCLK21 and a starting signal VSP21, shifts output signals out21[1] to out21[m] by one clock cycle of clock VCLK21, and sequentially outputs the resultant signal. The output signal out21[i] includes two high level pulses in one cycle. In the high level pulse, its width is the same as a period Tc1 of the clock VCLK21, and its period is twice the period Tc1 of the clock VCLK21, i being an integer from 1 to m.

[0123] Shift register 330 receives a clock signal VCLK22 and a starting signal VSP22, and shifts output signals out22[1] to out22[m] by one cycle of clock VCLK22, and sequentially outputs the resultant signal. The clock VCLK22 has the same cycle Tc1 as the clock VCLK21, and is the signal for the clock VCLK21 to be shifted by the precharge period Tp. The output signal out22[i] also has two high level pulses in one cycle. The width of the high level pulse is the same as the clock cycle of clock VCLK22, and the cycle of the high level pulse is twice the clock cycle of clock VCLK22, i being an integer from 1 to m. The output signal out22[i] of shift register 340 is the signal for the output signal out21[i] of shift register 330 to be shifted by the precharge period Tp.

[0124] Each XOR gate XOR_{1i} performs an XOR operation on the output signal out21[i] of shift register 330 and the output signal out22[i] of shift register 340, and outputs the resultant output signal scan21[i]. The output

signal scan21[i] assumes a high level when one of the two output signals out21[i] and out22[i] is at a high level by virtue of the XOR operation. Since the output signal out22[i] is the signal for the output signal out21[i] to be shifted by the precharge period Tp, the output signal scan21[i] has four high level pulses in one cycle when the precharge period Tp is shorter than one clock cycle of clock VCLK21. The output signal scan21[i+1] of the XOR gate XOR1(i+1) becomes a signal for the previous output signal scan21[i] to be shifted by one clock cycle of clock VCLK21, and three of four high level pulses of the output signal scan21[i+1] correspond to the high level pulses of the output signal scan21[i].

[0125] Shift register 350, like shift register 320 of FIG. 6, receives a clock signal VCLK23 and a starting signal VSP23, shifts the output signals scan22[1] to scan22[m] having the high level pulse by half of a clock cycle of clock VCLK23, and sequentially outputs the resultant signals. The clock cycle of clock VCLK23 is twice the clock cycle of clock VCLK21. The start time point of the high level pulse in the output signal scan22[i] is half of a clock cycle of clock VCLK21 away from a start time point of the last high level pulse in the output signal scan21[i].

[0126] NOR gate NOR4i performs a NOR operation on the two output signals scan21[i] and scan22[i], and outputs a selection signal select[i] as does NOR gate NOR_{1i} of FIG. 6. The width and cycle of the precharge pulse are the same as the width and cycle, respectively, of the high level pulse of the output signal scan21[i], and the width of the selection pulse is the same as the width of the high level pulse of the selection signal scan2[i]. Thus, as shown in FIG. 4 and FIG. 15, the selection signal select[i] applied to a selection scan line X_i can be generated from the output signal of NOR gate NOR_{4i}.

[0127] Next, shift registers 330, 340, and 350 for generating the output signals out21[i], out22[i], and scan22[i], respectively, explained in FIG. 14 and FIG. 15, are described in detail with reference to FIG. 16.

[0128] FIG. 16 is a simplified circuit diagram of a first shift register in the scan driver of FIG. 14. More specifically, FIG. 16 is a simplified circuit diagram of the shift register 330 of FIG. 14. VCLK21b indicates an inverted version of clock signal VCLK21 in FIG. 16. Shift registers 330 and 340 have the same types of output signals, and thus they may have the same construction or shift register. Thus, hereinafter, the shift register 330 is mainly described.

[0129] As shown in FIG. 16, shift register 330 of FIG. 16 includes m flip-flops FF_{41} to FF_{4m}, and the output signal of each flip-flop FF_{4i} become the output signal out21[i] of shift register 330, i being an integer from 1 to m.

[0130] In FIG. 16, an input signal of a first flip-flop FF_{41} is the starting signal VSP21 of FIG. 15, and an input signal in of the (i+1)th flip-flop $FF_{4(i+1)}$ is the output signal out21[i] of the ith flip-flop FF_{4i}. The flip-flop FF_{4i} receives the clock signal VCLK21 and VCLK21b as inner clocks clk and clkb, respectively. The flip-flop FF_{4i} delays the signals inputted during a low level of the clock clk by half of a clock cycle of clock clk and outputs the resultant signal, as do the flip-flops described in FIGs. 11, 13A, and 13B.

[0131] As shown in FIG. 15, the output signal out21[i] of the flip-flop FF4i has two high level pulses in one cycle, the width of the high level pulse is the same as the clock cycle VCLK21, and the cycle of the high level pulse is twice the clock cycle of clock VCLK21. The starting signal VSP21 and the input signal in of the flip-flop FF_{41} have two high level pulses in one cycle, and the high level pulses correspond to the low level of the clock VCLK21 per two clock intervals of clock VCLK21. The flip-flops FF_{41} to FF_{4m} shift the output signals out21[1] to out21[m] having two high level pulses by one clock cycle of clock VCLK21, and sequentially output the resultant signal.

[0132] Further, shift register 340 has the same construction as shift register 330, the clock signal VCLK22 and the starting signal VSP22 are signals that represent the clock signal VCLK21 and the starting signal VSP21, respectively, shifted by the precharge period (Tp), and they are inputted to shift register 340. Then, as shown in FIG. 15, shift register 340 sequentially outputs the signal out22[i] such that the output signal out21[i] is shifted by the precharge period (Tp).

[0133] As shown in FIG. 7 and FIG. 14, the output signal scan22[i] of shift register 350 is the same as the output signal scan12[i] of shift register 320 in FIG. 10. Thus, when the clock signal VCLK23 and a starting signal VSP23 of FIG. 14 are inputted to shift register 320 in FIG. 10, the output signal scan22[i] of shift register 350 can be generated.

[0134] Furthermore, other numbers of precharge pulses, in addition to four, may be generated by applying scan driver 300' of the second exemplary embodiment.

[0135] For example, when the precharge pulse is 2n, n high level pulses may be generated in the output signals out21[i] and out22[i] of shift registers 330 and 340, and the cycle of the high level pulse may be twice the width. In particular, when the precharge pulses are two, scan driver 300' can be embodied by the shift register 320 of FIG. 10. Hereinafter, such an exemplary embodiment is described with reference to FIG. 17 and FIG. 18.

[0136] FIG. 17 is a simplified circuit diagram of a first shift register in the scan driver according to a third exemplary embodiment of the present invention, and FIG. 18 is a signal timing diagram of the scan driver according to the third exemplary embodiment of the present invention. In FIG. 17 and FIG. 18, out21[i]', VCLK21' and VSP21' indicate an output signal, a clock signal and a starting signal, respectively, of shift register 330', and out22[i]', VCLK22', and VSP22' indicate an output signal, a clock signal and a starting signal, respectively, of shift register 340, i being an integer from 1 to m.

[0137] As shown in FIG. 17, shift register 330' includes flip-flops FF_{51} to $FF_{5(m+1)}$ and m NOR gates NOR_{51} to NOR_{5m}. The flip-flops FF_{51} to $FF_{5(m+1)}$ and m NOR gates NOR_{51} to NOR_{5m} are substantially the same as flip-flops FF_{31} to $FF_{3(m+1)}$ and m NOR gates NOR_{31} to NOR_{3m} of

FIG. 10, and thus descriptions thereof are omitted. Furthermore, shift register 340' has the same construction as shift register 330', and VCLK22' and VSP22' are inputted as clock and starting signals, respectively.

[0138] The clocks VCLK21' and VCLK22' inputted to shift registers 330' and 340' have the same cycle as the clock VCLK23 of shift register 350. The starting signals VSP21' and VSP22' of shift registers 330 and 340 have a low level pulse, while the clocks VCLK21' and VCLK22' are at a high level.

[0139] As shown in FIG. 18, the output signals out21[i]' and out22[i]' having high level pulses are shifted by half of a clock cycle of clock VCLK23. The width of the high level pulse corresponds to half of a clock cycle of clock VCLK23. The construction and operation of the scan driver can be easily understood from the above descriptions, and thus the detailed description is omitted.

[0140] As such, the construction of a scan driver can be simplified by using the shift register of FIG. 10 as shift registers 330', 340' and 350 of the scan driver. Furthermore, the clock cycles of clocks VCLK21' and VCLK22' are longer than the clock cycle of FIG. 15, and thus the frequency can be reduced.

[0141] As mentioned above, scan driver 300' according to the second and third exemplary embodiments of the present invention sequentially outputs a first output signal having high level pulses. The number of the high level pulses is one-half the number of the precharge pulses, or a larger number than one-half the number of the precharge pulses by 1. The cycle of the high level pulse is twice the width. Scan driver 300' sequentially outputs a second output signal for the first output signal to be shifted by the precharge period, and generates a pulse corresponding to the precharge pulse, while the first output signal and the second output signal have different levels from each other.

[0142] FIG. 19 shows a scan driver according to a third comparative example, and FIG. 20 is a signal timing diagram of the scan driver according to the third comparative example.

[0143] As shown in FIG. 19, scan driver 300" according to the third comparative example includes two shift registers 360 and 370, and a plurality of NOR gates NOR_{61} to NOR_{6m} and NOR_{71} to NOR_{7m}.

[0144] As shown in FIG. 18 and FIG. 19, shift register 360 receives a clock signal VCLK31 and a starting signal VSP31, and shifts the output signals out31[1] to out31[m] by half of a clock cycle of clock VCLK31, and sequentially outputs the resultant signal. The output signal out31[i] has one low-level pulse in one cycle, and the width of the low-level pulse is twice the clock cycle of clock VCLK31, i being an integer from 1 to m.

[0145] NOR gate NOR_{5i} performs a NOR operation on a precharge control signal PC and the output signal out31[i] of shift register 360, and outputs the output signal scan31[i]. As shown in FIG. 20, the precharge control signal PC has a low-level pulse in a predetermined cycle. The width Tp of the low-level pulse is the same as the precharge period, and the cycle of the precharge control signal PC corresponds to half of a clock cycle of clock VCLK31. As such, the width of the low-level pulse of the output signal out31[i] becomes four times the cycle of the precharge control signal PC, and the four low-level pulses of the precharge control signal PC correspond to the output signal out31[i].

[0146] NOR gate NOR6i outputs a high-level pulse when both the precharge control signal PC and the output signal out31[i] are at a low level, and thus the output signal scan31[i] of the NOR gate NOR6i has four high-level pulses in one cycle. The width and cycle of the high-level pulse are the same as the width and cycle, respectively, of the precharge control signal PC, and the precharge pulse may be generated by the high-level pulse. Furthermore, an output signal out31[i+1] is the signal for the output signal out31[i] to be shifted by half of a clock cycle of clock VCLK31, and thus the output signal scan31[i+1] of NOR gate $NOR_{6(i+1)}$ is the signal for the output signal scan31[i] to be shifted by half of a clock cycle of clock VCLK31. That is, the three pulses of four high-level pulses of the output signal scan31[i+1] correspond to the high-level pulse of the output signal scan31[i].

[0147] Shift register 370 receives a clock signal VCLK32 and a starting signal VSP32, shifts the output signals scan32[1] to scan32[m] by half of a clock cycle of clock VCLK31, and sequentially outputs the resultant signal. The output signals scan32[i] to scan32[m] have one high-level pulse in one cycle. The width of the high-level pulse of the output signal scan32[i] is ½ times the clock cycle of clock VCLK32, and the cycle of the clock VCLK32 is the same as that of the clock VCLK31. The start time point of the high-level pulse in the output signal scan32[i] is half of a clock cycle of clock VCLK32 away from a start time point of the last high-level pulse in the output signal scan31[i].

[0148] NOR gate NOR7i performs a NOR operation on an output signal scan32[i] of shift register 360 and an output signal scan 31[i] of NOR gate NOR6i, and outputs a selection signal select[i]. The width and cycle of the precharge pulse are the same as the width and cycle, respectively, of the high-level pulse of the output signal scan31[i], and the width of the selection pulse is the same as the width of the high-level pulse of the output signal scan31[i].

[0149] Next, shift registers 360 and 370 for generating the output signals out31[i] and scan32[i] described in FIG. 19 and 20 are described in detail with reference to FIG. 21 to FIG. 25.

[0150] FIG. 21 is a simplified circuit diagram of a first shift register in the scan drive of FIG. 19. In FIG. 21, VCLK31b indicates an inverted version of a clock signal VCLK31, but VCLK31b is not shown in the signal timing diagram of the FIG. 20.

[0151] As shown in FIG. 21, shift register 360 includes m flip-flops FF61 to FF6m, and output signals of each flip-flop FF6i become an output signal out31[i] of shift register 360, i being an integer from 1 to m. In FIG. 20,

an input signal of a first flip-flop FF_{61} is the start signal VSP31 of FIG. 19, and an output signal out31[i] of the ith flip-flop FF_{6i} becomes an input signal of the (i+1)th flip-flop $FF_{6(i+1)}$.

[0152] The flip-flop FF_{6i} outputs an input signal in as it is inputted when a clock clk is at a high level, but the flip-flop FF_{6i} latches the input signal in inputted when the clock clk was at a high level, and outputs the resultant signal as does the flip-flop of FIGs. 8A and 8B. Furthermore, the clock clk is inverted between two adjacent flip-flops FF_{6i} and $FF_{6(i+1)}$, as does the shift register of FIG. 8A.

[0153] In FIG. 20, the flip-flop FF_{6i} which is located at an odd-numbered position in the column direction receives clocks VCLK31 and VCLK31b as inner clocks clk and clkb, respectively. The flip-flop FF_{6i} which is located at an even-numbered position in the column direction receives clocks VCLK31 and VCLK31b as inner clocks clk and clkb, respectively. The starting signal VSP31, which is the input signal in of flip-flop FF61, has a low level pulse in two clock cycles when the clock VCLK31 is at a high level. Then, the flip-flops FF_{61} to FF_{6m} can shift output signals out31[1] to out31[m] having low-level pulses in two clock cycles of clock VCLK31 by half of a clock cycle of clock VCLK31, and sequentially output the resultant signals.

[0154] Furthermore, as shown in FIG. 7 and FIG. 20, the output signal scan32[i] of shift register 370 is the same as the output signal scan12[i] of shift register 320 of FIG. 10. Thus, when the clock signal VCLK32 and the starting signal VSP32 are inputted to shift register 320 of FIG. 10, the output signal scan32[i] of shift register 370 can be generated.

[0155] As such, scan driver 300" described in FIG. 19 to FIG. 21 can generate the selection signal select[i] shown in FIG. 4. Although the selection signal has four precharge pulses in FIG. 19 to FIG. 21, scan driver 300" of FIG. 19 to FIG. 21 can generate a selection signal having other numbers of precharge pulses.

[0156] For example, for 2n precharge pulses, the width of the high-level pulse is established to be twice the cycle of the precharge control signal PC in the output signal out31[i] of shift register 360. Then, the output signals scan31[i] of NOR gate NOR5i have 2n high-level pulses.

[0157] Scan driver 300" of FIG. 19 can be applied to generate odd-numbered precharge pulses in addition to even-numbered precharge pulses. Hereinafter, the case of generating an odd number of precharge pulses is described with reference to FIG. 22, which is a signal timing diagram of a scan driver according to the fourth comparative example, specifically, the scan driver 300" thereof.

[0158] The signal timing of FIG. 22 is the same as the signal timing of FIG. 20, excluding the timing of the starting signal VSP32', the signal clock VCLK32', and the output signal 32[i]'.

[0159] In detail, the start time point of the last high level pulse of the output signal scan31[i] of NOR gate NOR_{6i} is established so as to correspond to the start time point of the high-level pulse of the output signal scan32[i]' of shift register 370. The last high-level pulse of the output signal scan31[i] of NOR gate NOR_{6i} is subjected to a NOR operation with the high-level pulse of the output signal scan32[i]' of shift register 370, and thus an odd number of precharge pulses can be generated.

[0160] As such, the method described in FIG. 21 can be applied to the first and second comparative examples and the second and third exemplary embodiments. That is, in the first and second comparative examples and the second and third exemplary embodiments, the start time points of the last high-level pulse of the output signals scan11[i], scan11[i]', scan21[i] are established to correspond to the start time points of the high-level pulse of the output signals scan12[i], scan12[i]', and scan22[i]. Then, the number of precharge pulses can be made less than the number of high-level pulses by 1 in the selection signal select[i].

[0161] Shift register 360 having half of a clock cycle shift function is applied in FIG. 19 to FIG. 22. However, shift register 360' having a one clock cycle shift function can also be applied. Hereinafter, such a comparative example is described in detail with reference to FIG. 23 and FIG. 24.

[0162] FIG. 23 is a simplified circuit diagram of a first shift register in a scan driver according to a fifth comparative example, and FIG. 24 is a signal timing diagram of the scan driver according to the fifth comparative example.

[0163] As shown in FIG. 23, shift register 360' includes m flip-flops FF_{71} to FF_{7m}, and the output signal of the flip-flop FF_{7i} becomes the output signal out31[i]' of shift register 360', i being an integer from 1 to m.

[0164] The flip-flop FF_{7i} receives the clock signals VCLK31 and VCLK31b as inner clocks clk and clkb, respectively. The flip-flop FF_{7i} delays a signal inputted at a low level of clock clk by half of a clock cycle of clock clk and outputs the resultant signal during one clock cycle of clock clk, as do the flip-flops described in FIGs. 13A and 13B. Thus, the flip-flops FF_{71} to FF_{7m} can shift the output signals out31[1]' to out31[m]' by one clock cycle of clock VCLK331', and sequentially output the resultant signal as shown in FIG. 24.

[0165] However, the flip-flop FF_{7i} shifts the output signal by one clock cycle of clock VCLK31', and thus the clock cycle of clock VCLK31' is one-half of the clock cycle of clock VCLK32, while the clock cycle of clock VCLK31' is the same as the cycle of the precharge control signal PC, apart from FIG. 19. Furthermore, the output signal out31[i]' has a low-level pulse, the width of which is four times the cycle of the precharge control signal PC, and thus the width of the low-level pulse of the output signal out31[i]' is the same as four times the clock cycle of clock VCLK31'. The starting signal VSP31', the input signal in of the flip-flop FF_{71}, is converted to a high-level signal after the clock VCLK31' has low levels during the four cycles of clock VCLK31'. Then, the flip-flops FF_{71} to FF_{7m} shift the output signals out31[i] to out31[m]' having the

low-level pulse during four clock cycles of clock VCLK31' by one cycle of clock VCLK31', and sequentially output the resultant signal. Thus, the output signal scan31[i]' having four high-level pulses can be outputted, as shown in FIG. 24.

[0166] In the scan driver described in FIG. 23 and FIG. 24, when the high-level pulse of the output signal scan32 [i] of shift register 370' is established so as to correspond to the last-high level pulse of the output signal scan31[i] ' of NOR gate NOR6i, an odd number of precharge pulses can be generated. Furthermore, in the scan driver, the number of high-level pulses of the output signal scan31 [i]' of NOR gate NOR6i can be established so as to be an odd number. That is, the width of the low-level pulse of the output signal out31[i] of shift register 360' can be established so as to be an odd number multiple of the cycle of the precharge control signal PC, that is, an odd number multiple of the clock cycle of clock VCLK31'.

[0167] Furthermore, an emit signal emit[i] of FIG. 4 can be generated by using scan driver 300 described in FIG. 23 and FIG. 24. Hereinafter, such a comparative example is described with reference to FIG. 25.

[0168] FIG. 25 is a signal timing diagram of a scan driver according to a sixth comparative example.

[0169] As shown in FIG. 25, shift register 370 outputs an output signal scan32[i]', such that a start time point of a high-level pulse in the output signal scan32[i]' corresponds to a start time point of the last high-level pulse in the output signal scan31[i]' of NOR gate NOR_{6i}. As such, a period in which the output signal scan31[i]' of NOR gate NOR_{6i} is a high-level pulse, and a period in which the output signal scan32[i]' of shift register 370 is a high-level pulse, are included in a period in which the output signal out31[i]' of shift register 360' is a low-level pulse. That is, while the selection signal select[i] has the selection pulse and the precharge pulse, the output signal out31[i]' of shift register 360' is at a low level. Thus, an inverted signal of the output signal of shift register 360' can be used as the emit signal emit[i].

[0170] As such, scan driver 300" according to the third to fifth comparative examples uses a precharge control signal in which a first pulse having a width corresponding to the precharge pulse is repeated a predetermined number of cycles. In the precharge control signal, the first pulses corresponding to the number of precharge pulses are selected to generate the precharge pulse. In this respect, scan driver 300' selects the first pulse by using a second pulse, the width of which includes the first pulses corresponding to the number of the precharge pulses.

[0171] In the first to third exemplary embodiments of the present invention, the selection signal outputted from the scan driver is directly applied to the selection scan line. However, the selection signal outputted from the scan driver may be applied to the selection scan line through a buffer formed between the scan driver and the display area. Furthermore, a level shifter may be formed between the scan driver and the display area so as to modify levels of the selection signal and the emit signal.

[0172] According to the present invention, the time for charging the data line can be reduced, and thus quick data programming and a correct gray expression can be achieved.

[0173] While this invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications included within the scope of the appended claims.

Claims

1. A driving device (300') for a light emitting display which includes a plurality of scan lines (X1, X2, ..., Xm) for transferring a plurality of selection signals (select [1], select [2], ..., select [m]), the driving device (300') comprising:

a first driver (330) for outputting a plurality of first signals (out21 [1], out21 [2], ..., out21 [m]) to a plurality of outputs, each first signal (out21 [1], out21 [2], ..., out21 [m]) having a first integer multiple of first pulses and being shifted by a first period (Tcl) with respect to the preceding first signal (out21 [1], out21 [2], ..., out21 [m]);

a second driver (340) for outputting a plurality of second signals (out22 [1], out22 [2], ..., out22 [m]) to a plurality of outputs, each second signal (out22 [1], out22 [2], ..., out22 [m]) having a plurality of second pulses corresponding to the first pulses shifted by a second period (Tp);

a third driver (XOR_{11}, XOR_{12}, ..., XOR_{1m}) for outputting a plurality of third signals (scan21 [1], scan21 [2], ..., scan21 [m]) to a plurality of outputs in response to the first signals (out21 [1], out21 [2], ..., out21 [m]) and the second signals (out22 [1], out22 [2], ..., out22 [m]), each third signal (scan21 [1], scan21 [2], ..., scan21 [m]) having a second integer multiple of third pulses and being shifted by the first period (Tcl) with respect to the preceding third signal (scan21 [1], scan21 [2], ..., scan21 [m]);

a fourth driver (350) for outputting a plurality of fourth signals (scan22 [1], scan22 [2], ..., scan22 [m]) to a plurality of outputs, each fourth signal (scan22 [1], scan22 [2], ... , scan22 [m]) having a fourth pulse and being shifted by a third period with respect to the preceding fourth signal (scan22 [1], scan22 [2], ..., scan22 [m]); and

a fifth driver (NOR_{41}, NOR_{42}, ..., NOR_{4m}) for outputting the plurality of selection signals (select [1], select [2], ..., select [m]) in response to the third signals (scan21 [1], scan21 [2], ..., scan21 [m]) and the fourth signals (scan22 [1], scan22 [2], ..., scan22 [m]), each selection signal (select

[1], select [2], ..., select [m]) having a third integer multiple of fifth pulses, each third pulse corresponding to at least one fifth pulse, and having a sixth pulse corresponding to the fourth pulse, wherein the second integer multiple is greater than the first integer multiple and
wherein the third pulses are shorter than the first pulses.

2. The driving device (300') of claim 1, wherein the second period (Tp) has a width the same as a width of a third pulse.

3. The driving device (300') of claim 2, wherein a width between two adjacent first pulses in a plurality of the first pulses is the same as a width of a first pulse.

4. The driving device (300') of claim 3, wherein the second period (Tp) has a width shorter than the width of a first pulse.

5. The driving device (300') of claim 2, wherein the first integer corresponds to twice the second integer.

6. The driving device (300') of claim 2 or 5, wherein the first driver (330), the second driver (340) and the fourth driver (350) respectively comprise a shift register, and a cycle of a clock used in the fourth driver (350) corresponds to twice a cycle of a clock used in the first driver (330) and the second driver (340).

7. The driving device (300') of claim 2 or 5, wherein the first driver (330), the second driver (340) and the fourth driver (350) respectively comprise a shift register, and a cycle of a clock used in the fourth driver (350) is the same as a cycle of a clock used in the first driver (330) and the second driver (340).

8. A light emitting display, comprising:

a display area comprising a plurality of data lines (Y1, Y2, ..., Yn) for transferring a data signal, a plurality of scan lines (X1, X2, ..., Xm) arranged in a direction which crosses a direction of the data lines (Y1, Y2, ..., Yn), and a plurality of pixels (110) respectively coupled to the data lines (Y1, Y2, ..., Yn) and the scan lines (X1, X2, ..., Xm); and
a driving device (300') according to one of the preceding claims.

9. The light emitting display of claim 8, wherein each pixel (110) comprises:

at least one switch (T1, T2) for transferring a data signal from one of the data lines (Y1, Y2, ..., Yn) in response to a low level in the selection signal (select [1], select [2], ..., select [m]) applied to one of the scan lines (X1, X2, ..., Xm);
a capacitor (C) for charging to a voltage corresponding to the data signal transferred;
a transistor (T3) for outputting a current according to the voltage charged on the capacitor (C); and
a light emitting element (OLED) for emitting light according to a magnitude of the current outputted by the transistor (T3).

10. A method for driving a light emitting display which includes a plurality of scan lines (X1, X2, ..., Xm) for transferring a plurality of selection signals (select [1], select [2], ..., select [m]), the method comprising the steps of:

outputting a plurality of first signals (out21 [1], out21 [2], ..., out21 [m]) to a plurality of outputs, each first signal (out21 [1], out21 [2], ..., out21 [m]) having a first integer multiple of first pulses and being shifted by a first period (Tcl) with respect to the preceding first signal (out21 [1], out21 [2], ..., out21 [m]);
outputting a plurality of second signals (out22 [1], out22 [2], ..., out22 [m]) to a plurality of outputs, each second signal (out22 [1], out22 [2], ..., out22 [m]) having a plurality of second pulses corresponding to the first pulses shifted by a second period (Tp);
outputting a plurality of third signals (scan21 [1], scan21 [2], ..., scan21 [m]) to a plurality of outputs in response to the first signals (out21 [1], out21 [2], ..., out21 [m]) and the second signals (out22 [1], out22 [2], ..., out22 [m]), each third signal (scan21 [1], scan21 [2], ..., scan21 [m]) having a second integer multiple of third pulses and being shifted by the first period (Tcl) with respect to the preceding third signal (scan21 [1], scan21 [2], ..., scan21 [m]);
outputting a plurality of fourth signals (scan22 [1], scan22 [2], ..., scan22 [m]) to a plurality of outputs, each fourth signal (scan22 [1], scan22 [2], ..., scan22 [m]) having a fourth pulse and being shifted by a third period with respect to the preceding fourth signal (scan22 [1], scan22 [2], ..., scan22 [m]); and
outputting the plurality of selection signals (select [1], select [2], ..., select [m]) in response to the third signals (scan21 [1], scan21 [2], ..., scan21 [m]) and the fourth signals (scan22 [1], scan22 [2], ..., scan22 [m]), each selection signal (select [1], select [2], ..., select [m]) having a third integer multiple of fifth pulses corresponding to at least one of the second integer multiple of third pulses, and having a sixth pulse corresponding to the fourth pulse,
wherein the second integer multiple is greater than the first integer multiple and

wherein the third pulses are shorter than the first pulses.

11. The method of claim 10, wherein the second period (Tp) has a width the same as a width of a third pulse.

12. The method of claim 11, wherein a width between two adjacent first pulses in a plurality of the first pulses is the same as a width of a first pulse.

13. The method of claim 12, wherein the second period (Tp) has a width shorter than the width of a first pulse.

14. The method of claim 11, wherein the first integer corresponds to twice the second integer.

15. The method of claim 11 or 14, wherein the step of outputting the plurality of first signals, the step of outputting the plurality of second signals and the step of outputting the plurality of fourth signals are respectively performed using a shift register, and a cycle of a clock used in the step of outputting the plurality of fourth signals corresponds to twice a cycle of a clock used in the step of outputting the plurality of first signals and the step of outputting the plurality of second signals.

16. The method of claim 11 or 14, wherein the step of outputting the plurality of first signals, the step of outputting the plurality of second signals and the step of outputting the plurality of fourth signals are respectively performed using a shift register, and a cycle of a clock used in the step of outputting the plurality of fourth signals is the same as a cycle of a clock used in the step of outputting the plurality of first signals and the step of outputting the plurality of second signals.

Patentansprüche

1. Ein Steuergerät (300') für eine lichtemittierende Anzeige, die eine Vielzahl von Ansteuerleitungen (X1, X2, ..., Xm) zur Übertragung einer Vielzahl von Selektierungssignalen (select [1], select [2], ..., select [m]), aufweist, wobei das Steuergerät (300') aufweist:

einen ersten Treiber (330) zur Ausgabe einer Vielzahl erster Signale (out21 [1], out21 [2], ..., out21 [m]) an eine Vielzahl von Ausgängen, wobei jedes erste Signal (out21 [1], out21 [2], ..., out21 [m]) ein erstes ganzzahliges Vielfaches erster Pulse aufweist und bezüglich des vorausgehenden ersten Signals (out21 [1], out21 [2], ..., out21 [m]) um ein erstes Intervall (Tcl) verschoben ist;
einen zweiten Treiber (340) zur Ausgabe einer Vielzahl zweiter Signale (out22 [1], out22 [2], ..., out22 [m]) an eine Vielzahl von Ausgängen, wobei jedes zweite Signal (out22 [1], out22 [2], ..., out22 [m]) eine Vielzahl zweiter Pulse aufweist, die den ersten Pulsen entsprechen, welche um ein zweites Intervall (Tp) verschoben sind;
einen dritten Treiber (XOR_{11}, XOR_{12}, ..., XOR_{1m}) zur Ausgabe einer Vielzahl dritter Signale (scan21 [1], scan 21 [2], ..., scan 21 [m]) an eine Vielzahl von Ausgängen in Reaktion auf die ersten Signale (out21 [1], out21 [2], ..., out21 [m]) und die zweiten Signale (out22 [1], out22 [2], ..., out22 [m]), wobei jedes dritte Signal (scan21 [1], scan 21 [2], ..., scan 21 [m]) ein zweites ganzzahliges Vielfaches dritter Pulse aufweist und bezüglich des vorausgehenden dritten Signals (scan 21 [1], scan 21 [2], ..., scan21 [m]) um das erste Intervall (Tcl) verschoben ist;
einen vierten Treiber (350) zur Ausgabe einer Vielzahl vierter Signale (scan22 [1], scan 22 [2], ..., scan 22 [m]) an eine Vielzahl von Ausgängen, wobei jedes vierte Signal (scan22 [1], scan 22 [2], ..., scan 22 [m]) einen vierten Puls aufweist und bezüglich des vorausgehenden vierten Signals (scan22 [1], scan 22 [2], ..., scan 22 [m]) um ein drittes Intervall verschoben ist; und
einen fünften Treiber (NOR_{41}, NOR_{42}, ..., NOR_{4m}) zur Ausgabe der Vielzahl von Selektierungssignalen (select [1], select [2], ..., select [m]) in Reaktion auf die dritten Signale (scan21 [1], scan21 [2], ..., scan21 [m]) und die vierten Signale (scan22 [1], scan 22 [2], ..., scan 22 [m]), wobei jedes Selektierungssignal (select [1], select [2], ..., select [m]) ein drittes ganzzahliges Vielfaches fünfter Pulse aufweist, wobei jeder dritte Puls zumindest einem fünften Puls entspricht, und wobei jedes Selektierungssignal (select [1], select [2], ..., select [m]) einen sechsten Puls aufweist, der dem vierten Puls entspricht,
wobei das zweite ganzzahlige Vielfache größer als das erste ganzzahlige Vielfache ist und
wobei die dritten Pulse kürzer als die ersten Pulse sind.

2. Steuergerät (300') nach Anspruch 1, wobei das zweite Intervall (Tp) eine Breite aufweist, die gleich einer Breite eines dritten Pulses ist.

3. Steuergerät (300') nach Anspruch 2, wobei eine Breite zwischen zwei benachbarten ersten Pulsen in einer Vielzahl der ersten Pulse gleich einer Breite eines ersten Pulses ist.

4. Steuergerät (300') nach Anspruch 3, wobei das zweite Intervall (Tp) eine Breite aufweist, die kürzer als

die Breite eines ersten Pulses ist.

5. Steuergerät (300') nach Anspruch 2, wobei die erste ganze Zahl dem Doppelten der zweiten ganzen Zahl entspricht.

6. Steuergerät (300') nach Anspruch 2 oder 5, wobei der erste Treiber (330), der zweite Treiber (340) und der vierte Treiber (350) jeweils ein Schieberegister aufweisen, und wobei ein Zyklus eines Taktes, der im vierten Treiber (350) verwendet wird, dem Doppelten eines Zyklus eines Taktes, der im ersten Treiber (330) und im zweiten Treiber (340) verwendet wird, entspricht.

7. Steuergerät (300') nach Anspruch 2 oder 5, wobei der erste Treiber (330), der zweite Treiber (340) und der vierte Treiber (350) jeweils ein Schieberegister aufweisen, und wobei ein Zyklus eines Taktes, der im vierten Treiber (350) verwendet wird, gleich einem Zyklus eines Taktes, der im ersten Treiber (330) und im zweiten Treiber (340) verwendet wird, ist.

8. Lichtemittierende Anzeige, aufweisend:

einen Anzeigebereich, der eine Vielzahl von Datenleitungen (Y1, Y2, ..., Yn) zur Übertragung eines Datensignals, eine Vielzahl von Ansteuerleitungen (X1, X2, ..., Xm), die in einer Richtung, welche eine Richtung der Datenleitungen (Y1, Y2, ..., Yn) kreuzt, angeordnet sind, und eine Vielzahl von Pixeln (110), die jeweils an die Datenleitungen (Y1, Y2, ..., Yn) und die Ansteuerleitungen (X1, X2, ..., Xm) angekoppelt sind, aufweist; und
ein Steuergerät (300') nach einem der vorhergehenden Ansprüche.

9. Lichtemittierende Anzeige nach Anspruch 8, wobei jeder Pixel (110) aufweist: zumindest einen Schalter (T1, T2) zur Übertragung eines Datensignals von einer der Datenleitungen (Y1, Y2, ..., Yn) in Reaktion auf ein niedriges Level in dem an einer der Ansteuerleitungen (X1, X2, ..., Xm) anliegenden Selektierungssignal (select [1], select [2], ..., select [m]);
einen Kondensator (C), der mit einer Spannung entsprechend dem übertragenen Datensignal aufgeladen wird;
einen Transistor (T3), der einen Strom gemäß der im Kondensator (C) geladenen Spannung ausgibt; und
ein lichtemittierendes Element (OLED), welches Licht gemäß einem Betrag des von dem Transistor (T3) ausgegebenen Stromes emittiert.

10. Verfahren zur Steuerung einer lichtemittierenden Anzeige, die eine Vielzahl von Ansteuerleitungen (X1, X2, ..., Xm) zur Übertragung einer Vielzahl von Selektierungssignalen (select [1], select [2], ..., select [m]) aufweist, wobei das Verfahren die folgenden Schritte aufweist:

Ausgabe einer Vielzahl erster Signale (out21 [1], out21 [2], ..., out21 [m]) an eine Vielzahl von Ausgängen, wobei jedes erste Signal (out21 [1], out21 [2], ..., out21 [m]) ein erstes ganzzahliges Vielfaches erster Pulse aufweist und bezüglich des vorausgehenden ersten Signals (out21 [1], out21 [2], ..., out21 [m]) um ein erstes Intervall (Tcl) verschoben ist;
Ausgabe einer Vielzahl zweiter Signale (out22 [1], out22 [2], ..., out22 [m]) an eine Vielzahl von Ausgängen, wobei jedes zweite Signal (out22 [1], out22 [2], ..., out22 [m]) eine Vielzahl zweiter Pulse aufweist, die den ersten Pulsen entsprechen, welche um ein zweites Intervall (Tp) verschoben sind;
Ausgabe einer Vielzahl dritter Signale (scan21 [1], scan 21 [2], ..., scan 21 [m]) an eine Vielzahl von Ausgängen in Reaktion auf die ersten Signale (out21 [1], out21 [2], ..., out21 [m]) und die zweiten Signale (out22 [1], out22 [2], ..., out22 [m]), wobei jedes dritte Signal (scan21 [1], scan 21 [2], ..., scan 21 [m]) ein zweites ganzzahliges Vielfaches dritter Pulse aufweist und bezüglich des vorausgehenden dritten Signals (scan 21 [1], scan 21 [2], ..., scan21 [m]) um das erste Intervall (Tcl) verschoben ist; und
Ausgabe einer Vielzahl vierter Signale (scan22 [1], scan 22 [2], ..., scan 22 [m]) an eine Vielzahl von Ausgängen, wobei jedes vierte Signal (scan22 [1], scan 22 [2], ..., scan 22 [m]) einen vierten Puls aufweist und bezüglich des vorausgehenden vierten Signals (scan22 [1], scan 22 [2], ..., scan 22 [m]) um ein drittes Intervall verschoben ist; und
Ausgabe der Vielzahl von Selektierungssignalen (select [1], select [2], ..., select [m]) in Reaktion auf die dritten Signale (scan21 [1], scan21 [2], ..., scan21 [m]) und die vierten Signale (scan22 [1], scan 22 [2], ..., scan 22 [m]), wobei jedes Selektierungssignal (select [1], select [2], ..., select [m]) ein drittes ganzzahliges Vielfaches fünfter Pulse aufweist, das zumindest einem des zweiten ganzzahligen Vielfachen dritter Pulse entspricht, und wobei jedes Selektierungssignal (select [1], select [2], ..., select [m]) einen sechsten Puls, der dem vierten Puls entspricht, aufweist,
wobei das zweite ganzzahlige Vielfache größer als das erste ganzzahlige Vielfache ist und
wobei die dritten Pulse kürzer als die ersten Pulse sind.

11. Verfahren nach Anspruch 10, wobei das zweite Intervall (Tp) eine Breite aufweist, die gleich einer Brei-

te eines dritten Pulses ist.

12. Verfahren nach Anspruch 11, wobei eine Breite zwischen zwei benachbarten ersten Pulsen in einer Vielzahl der ersten Pulse gleich einer Breite eines ersten Pulses ist.

13. Verfahren nach Anspruch 12, wobei das zweite Intervall (Tp) eine Breite aufweist, die kürzer als die Breite eines ersten Pulses ist.

14. Verfahren nach Anspruch 11, wobei die erste ganze Zahl dem Doppelten der zweiten ganzen Zahl entspricht.

15. Verfahren nach Anspruch 11 oder 14, wobei der Schritt der Ausgabe der Vielzahl erster Signale, der Schritt der Ausgabe der Vielzahl zweiter Signale und der Schritt der Ausgabe der Vielzahl vierter Signale jeweils mittels eines Schieberegisters durchgeführt werden, und wobei ein Zyklus eines Taktes, der beim Schritt der Ausgabe der Vielzahl vierter Signale verwendet wird, dem Doppelten eines Zyklus eines Taktes, der beim Schritt der Ausgabe der Vielzahl erster Signale und beim Schritt der Ausgabe der Vielzahl zweiter Signale verwendet wird, entspricht.

16. Verfahren nach Anspruch 11 oder 14, wobei der Schritt der Ausgabe der Vielzahl erster Signale, der Schritt der Ausgabe der Vielzahl zweiter Signale und der Schritt der Ausgabe der Vielzahl vierter Signale jeweils mittels eines Schieberegisters durchgeführt werden, und wobei ein Zyklus eines Taktes, der beim Schritt der Ausgabe der Vielzahl vierter Signale verwendet wird, gleich einem Zyklus eines Taktes, der beim Schritt der Ausgabe der Vielzahl erster Signale und beim Schritt der Ausgabe der Vielzahl zweiter Signale verwendet wird, ist.

Revendications

1. Dispositif d'attaque (300') pour un afficheur à émission de lumière qui comprend de multiples lignes de balayage (X1, X2, ..., Xm) pour le transfert de multiples signaux de sélection (select[1], select[2], ..., select[m]), le dispositif d'attaque (300') comportant :

un premier élément d'attaque (330) destiné à délivrer en sortie de multiples premiers signaux (out21 [1], out21 [2], ..., out21 [m]) à de multiples sorties, chaque premier signal (out21 [1], out21 [2], ..., out21 [m]) ayant un premier multiple entier de premières impulsions et étant décalé d'une première période (Tcl) par rapport au premier signal précédent (out21 [1], out21 [2], ..., out21 [m]) ;
un second élément d'attaque (340) destiné à délivrer en sortie de multiples seconds signaux (out22 [1], out22 [2], ..., out22 [m]) à de multiples sorties, chaque second signal (out22 [1], out22 [2], ..., out22 [m]) ayant de multiples secondes impulsions correspondant aux premières impulsions décalées d'une seconde période (Tp) ;
un troisième élément d'attaque (XOR_{11}, XOR_{12}, ..., XOR_{1m}) destiné à délivrer en sortie de multiples troisièmes signaux (scan21 [1], scan21 [2], ..., scan21 [m]) à de multiples sorties en réponse aux premiers signaux (out21 [1], out21 [2], ..., out21 [m]) et aux seconds signaux (out22 [1], out22 [2], ..., out22 [m]), chaque troisième signal (scan21 [1], scan21 [2], ..., scan21 [m]) ayant un second multiple entier de troisièmes impulsions et étant décalé de la première période (Tcl) par rapport au troisième signal précédent (scan21 [1], scan21 [2], ..., scan21 [m]) ;
un quatrième élément d'attaque (350) destiné à délivrer en sortie de multiples quatrièmes signaux (scan22 [1], scan22 [2], ..., scan22 [m]) à de multiples sorties, chaque quatrième signal (scan22 [1], scan22 [2], ..., scan22 [m]) ayant une quatrième impulsion et étant décalé d'une troisième période par rapport au quatrième signal précédent (scan22 [1], scan22 [2], ..., scan22 [m]) ; et
un cinquième élément d'attaque (NOR_{41}, NOF_{42}, ..., NOR_{4m})destiné à délivrer en sortie les multiples signaux de sélection (select [1], selec [2], ..., select [m]) en réponse aux troisièmes signaux (scan21 [1], scan21 [2], ..., scan21 [m]) et aux quatrièmes signaux (scan22 [1], scan22 [2], ..., scan22 [m]), chaque signal de sélection (select [1], select [2], ..., select [m]) ayant un troisième multiple entier de cinquièmes impulsions, chaque troisième impulsion correspondant à au moins une cinquième impulsion et ayant une sixième impulsion correspondant à la quatrième impulsion,
dans lequel le deuxième multiple entier est plus grand que le premier multiple entier, et
dans lequel les troisièmes impulsions sont plus courtes que les premières impulsions.

2. Dispositif d'attaque (300') selon la revendication 1, dans lequel la seconde période (Tp) a une largeur égale à la largeur d'une troisième impulsion.

3. Dispositif d'attaque (300') selon la revendication 2, dans lequel une largeur comprise entre deux premières impulsions adjacentes parmi de multiples premières impulsions est égale à la largeur d'une première impulsion.

4. Dispositif d'attaque (300') selon la revendication 3, dans lequel la seconde période (Tp) a une largeur plus courte que la largeur d'une première impulsion.

5. Dispositif d'attaque (300') selon la revendication 2, dans lequel le premier entier correspond au double du deuxième entier.

6. Dispositif d'attaque (300') selon la revendication 2 ou 5, dans lequel le premier élément d'attaque (330), le deuxième élément d'attaque (340) et le quatrième élément d'attaque (350) comprennent respectivement un registre à décalage, et un cycle d'une horloge utilisée dans le quatrième élément d'attaque (350) correspond au double d'un cycle d'une horloge utilisée dans le premier élément d'attaque (330) et dans le deuxième élément d'attaque (340).

7. Dispositif d'attaque (300') selon la revendication 2 ou 5, dans lequel le premier élément d'attaque (330), le deuxième élément d'attaque (340) et le quatrième élément d'attaque (350) comprennent respectivement un registre à décalage, et un cycle d'une horloge utilisée dans le quatrième élément d'attaque (350) est égal à un cycle d'une horloge utilisée dans le premier élément d'attaque (330) et dans le deuxième élément d'attaque (340).

8. Dispositif d'affichage émettant de la lumière, comportant :

une zone d'affichage comportant de multiples lignes de données (Y1, Y2, ..., Yn) pour transférer un signal de données, de multiples lignes de balayage (X1, X2, ..., Xm) agencées dans une direction qui croise une direction des lignes dedonnées(Y1,Y2, ..., Yn), et de multiples pixels (110) reliés respectivement aux lignes de données (Y1, Y2, ..., Yn) et aux lignes de balayage (X1, X2,..., Xm) ; et
un dispositif d'attaque (300') selon l'une des revendications précédentes.

9. Dispositif d'affichage émettant de la lumière selon la revendication 8, dans lequel chaque pixel (110) comporte :

au moins un commutateur (T1, T2) destiné à transférer un signal de données de l'une des lignes de données (Y1, Y2, ..., Yn) en réponse à un niveau bas dans le signal de sélection (select [1], selec [2], ..., select [m]) appliqué à l'une des lignes de balayage (X1, X2, ..., Xm) ;
un condensateur (C) destiné à charger une tension correspondant au signal de données transféré ;
un transistor (T3) destiné à délivrer en sortie un courant conforme à la tension chargée sur le condensateur (C) ; et
un élément d'émission de lumière (OLED) destiné à émettre de la lumière conformément à l'intensité du courant délivré en sortie par le transistor (T3).

10. Procédé pour attaquer un dispositif d'affichage émettant de la lumière qui comprend de multiples lignes de balayage (X1,X2, ...,Xm)pour transférer de multiples signaux de sélection (select[1],select [2], ...,select[m]), le procédé comprenant les étapes qui consistent :

à délivrer en sortie de multiples premiers signaux (out21 [1], out21 [2], ..., out21 [m]) à de multiples sorties, chaque premier signal (out21 [1], out21 [2], ..., out21 [m]) ayant un premier multiple entier de premières impulsions et étant décalé d'une première période (Tcl) par rapport au premier signal précédent (out21 [1], out21 [2], ..., out21 [m]) ;
à délivrer en sortie de multiples seconds signaux (out22 [1], out22 [2], ..., out22 [m]) à de multiples sorties, chaque second signal (out22 [1], out22 [2], ..., out22 [m]) ayant de multiples secondes impulsions correspondant aux premières impulsions décalées d'une seconde période (Tp) ;
à délivrer en sortie de multiples troisièmes signaux (scan21 [1], scan21 [2], ..., scan21 [m]) à de multiples sorties en réponse aux premiers signaux (out21 [1], out21 [2], ..., out21 [m]) et aux deuxièmes signaux (out22 [1], out22 [2], ..., out22 [m]), chaque troisième (signal scan21 [1], scan21 [2], ..., scan21 [m]) ayant un deuxième multiple entier de troisièmes impulsions et étant décalé de la première période (Tcl) par rapport au troisième signal précédent (scan21 [1], scan21 [2], ..., scan21 [m]) ;
à délivrer en sortie de multiples quatrièmes signaux (scan22 [1], scan22 [2], ..., scan22 [m]) à de multiples sorties, chaque quatrième signal (scan22 [1], scan22 [2], ..., scan22 [m]) ayant une quatrième impulsion et étant décalé d'une troisième période par rapport au quatrième signal précédent (scan22 [1], scan22 [2], ..., scan22 [m]) ; et
à délivrer en sortie les multiples signaux de sélection (select [1], select [2], ..., select [m]) en réponse aux troisièmes signaux (scan21 [1], scan21 [2], ...,scan21 [m]) et aux quatrièmes signaux (scan22 [1],scan22[2], ...,scan22[m]), chaque signal de sélection (select[1],select [2], ...,select[m]) ayant un troisième multiple entier de cinquièmes impulsions correspondant à au moins l'un du deuxième multiple entier de troisièmes impulsions, et ayant une sixième impulsion correspondant à la quatrième impulsion, dans lequel le deuxième multiple entier est plus grand que le premier multiple entier, et
dans lequel les troisièmes impulsions sont plus courtes que les premières impulsions.

11. Procédé selon la revendication 10, dans lequel la seconde période (Tp) a une largeur égale à la largeur d'une troisième impulsion.

12. Procédé selon la revendication 11, dans lequel une largeur comprise entre deux premières impulsions adjacentes parmi plusieurs des premières impulsions est égale à la largeur d'une première impulsion.

13. Procédé selon la revendication 12, dans lequel la seconde période (Tp) a une largeur plus courte que la largeur d'une première impulsion.

14. Procédé selon la revendication 11, dans lequel le premier entier correspond au double du deuxième entier.

15. Procédé selon la revendication 11 ou 14, dans lequel l'étape consistant à délivrer en sortie les multiples premiers signaux, l'étape consistant à délivrer en sortie les multiples deuxièmes signaux et l'étape consistant à délivrer en sortie les multiples quatrièmes signaux sont exécutées respectivement en utilisant un registre à décalage, et un cycle d'une horloge utilisée dans l'étape consistant à délivrer en sortie les multiples quatrièmes signaux correspond au double d'un cycle d'une horloge utilisée dans l'étape consistant à délivrer en sortie les multiples premiers signaux et dans l'étape consistant à délivrer en sortie les multiples deuxièmes signaux.

16. Procédé selon la revendication 11 ou 14, dans lequel l'étape consistant à délivrer en sortie les multiples premiers signaux, l'étape consistant à délivrer en sortie les multiples deuxièmes signaux et l'étape consistant à délivrer en sortie les multiples quatrièmes signaux sont exécutées respectivement en utilisant un registre à décalage, et un cycle d'une horloge utilisée dans l'étape consistant à délivrer en sortie les multiples quatrièmes signaux est égal à un cycle d'une horloge utilisée dans l'étape consistant à délivrer en sortie les multiples premiers signaux et l'étape consistant à délivrer en sortie les multiples deuxièmes signaux.

FIG.1

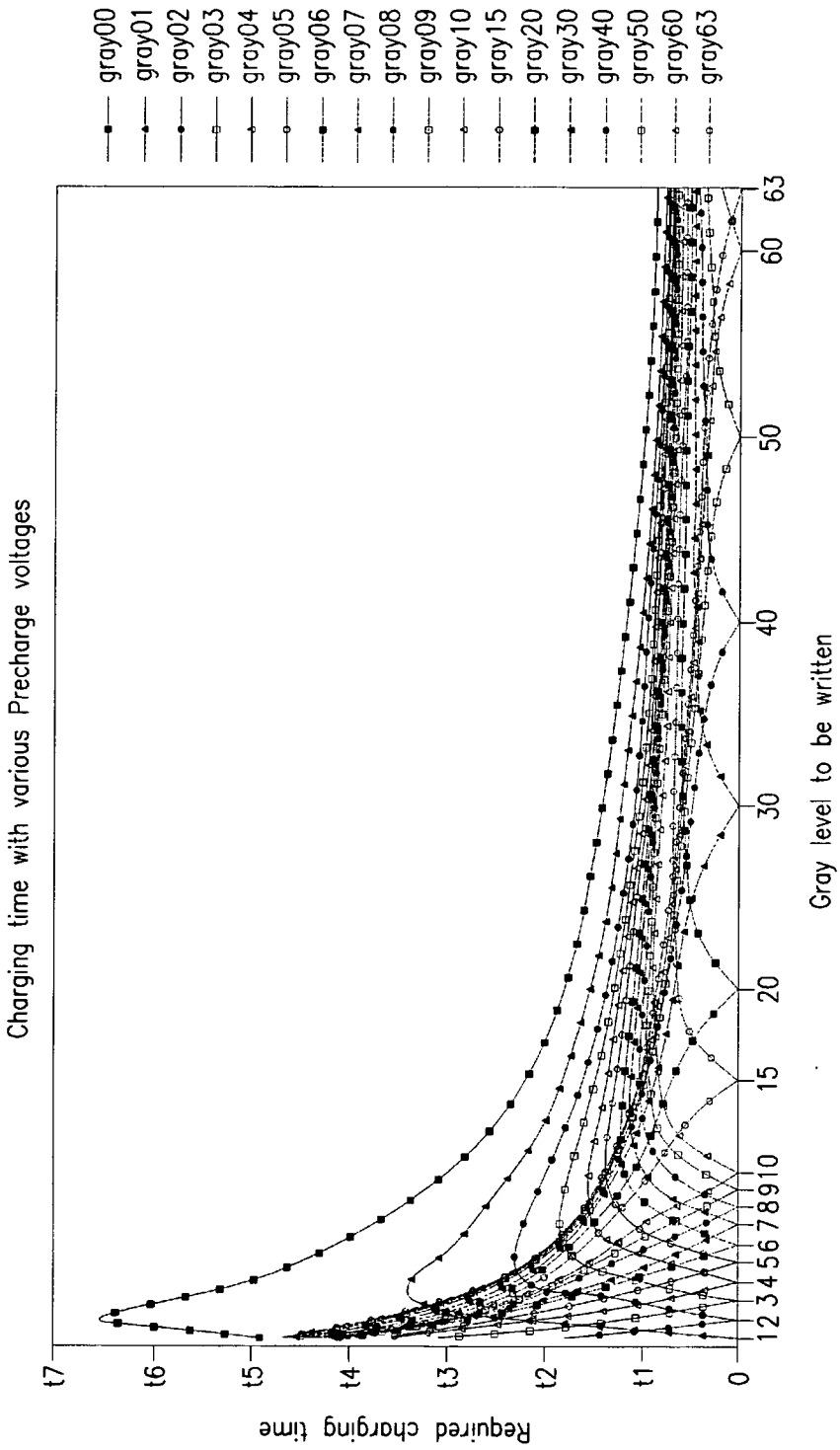

Charging time with various Precharge voltages
gray00
gray01
gray02
gray03
gray04
gray05
gray06
gray07
gray08
gray09
gray10
gray15
gray20
gray30
gray40
gray50
gray60
gray63
Required charging time
t7
t6
t5
t4
t3
t2
t1
0
1 2 3 4 5 6 7 8 9 10
15
20
30
40
50
60
63
Gray level to be written

FIG.2

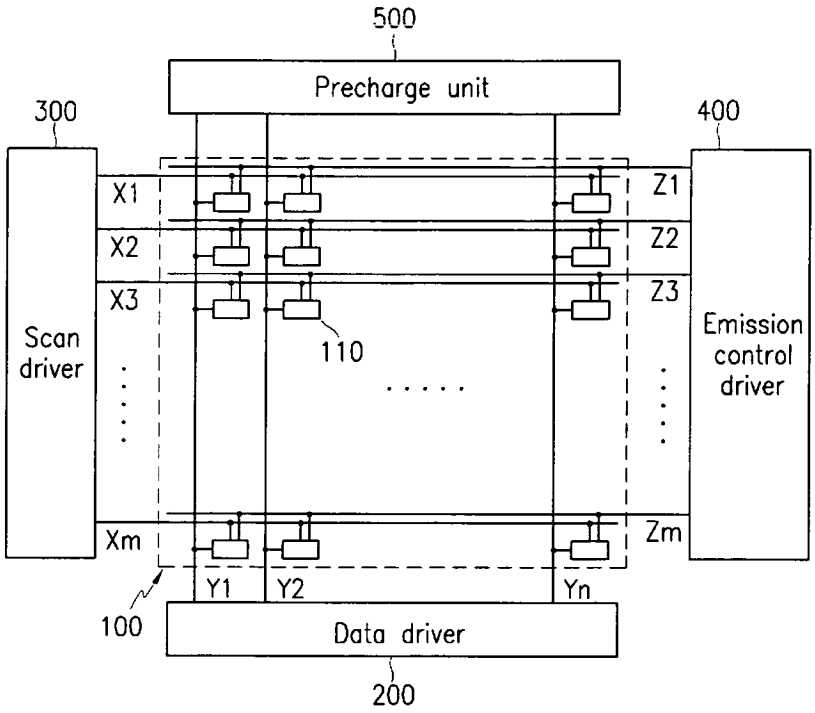

500
Precharge unit
300
400
X1
X2
X3
Xm
Z1
Z2
Z3
Zm
Scan driver
Emission control driver
110
Y1
Y2
Yn
100
Data driver
200

FIG.3

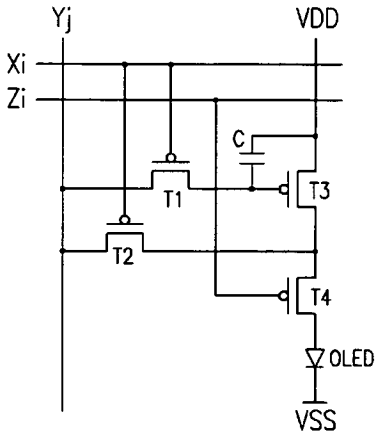

Yj
VDD
Xi
Zi
C
T1
T2
T3
T4
OLED
VSS

FIG.4

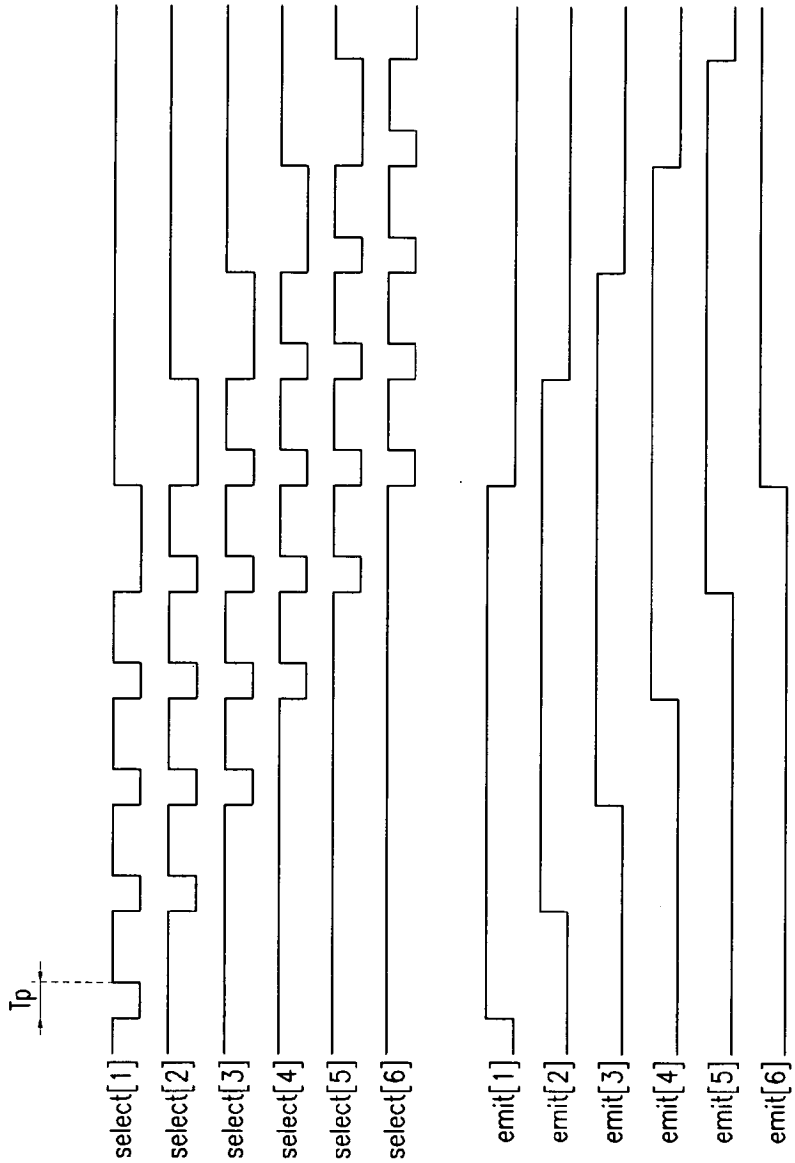

Tp
select[1]
select[2]
select[3]
select[4]
select[5]
select[6]
emit[1]
emit[2]
emit[3]
emit[4]
emit[5]
emit[6]

FIG.5A

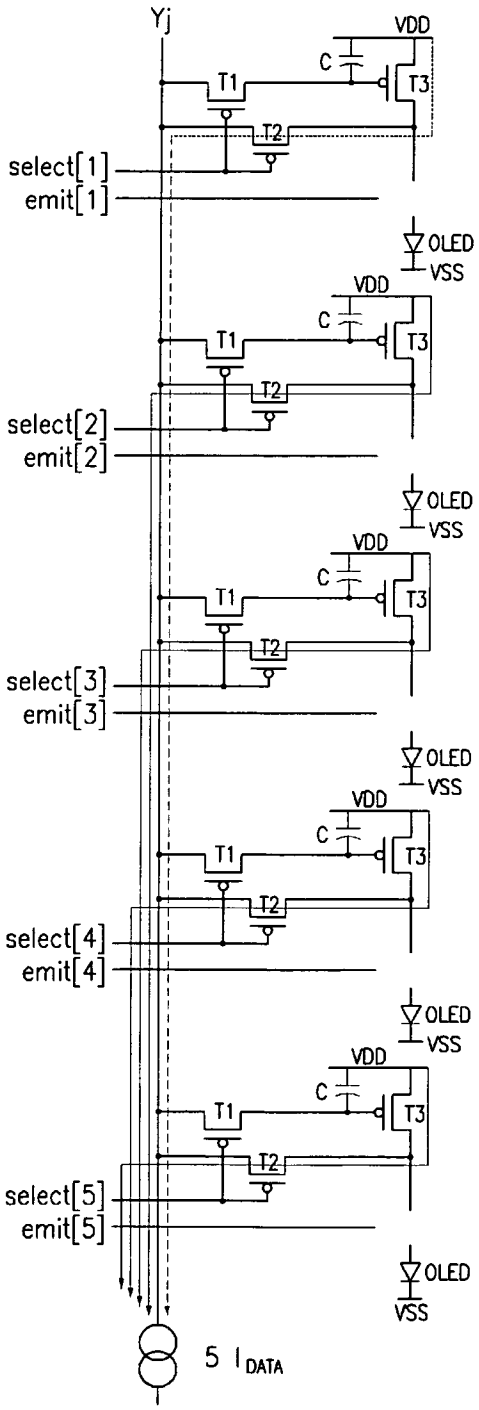

Yj
VDD
C
T1
T3
T2
select[1]
emit[1]
OLED
VSS
select[2]
emit[2]
select[3]
emit[3]
select[4]
emit[4]
select[5]
emit[5]
5 I DATA

FIG.5B

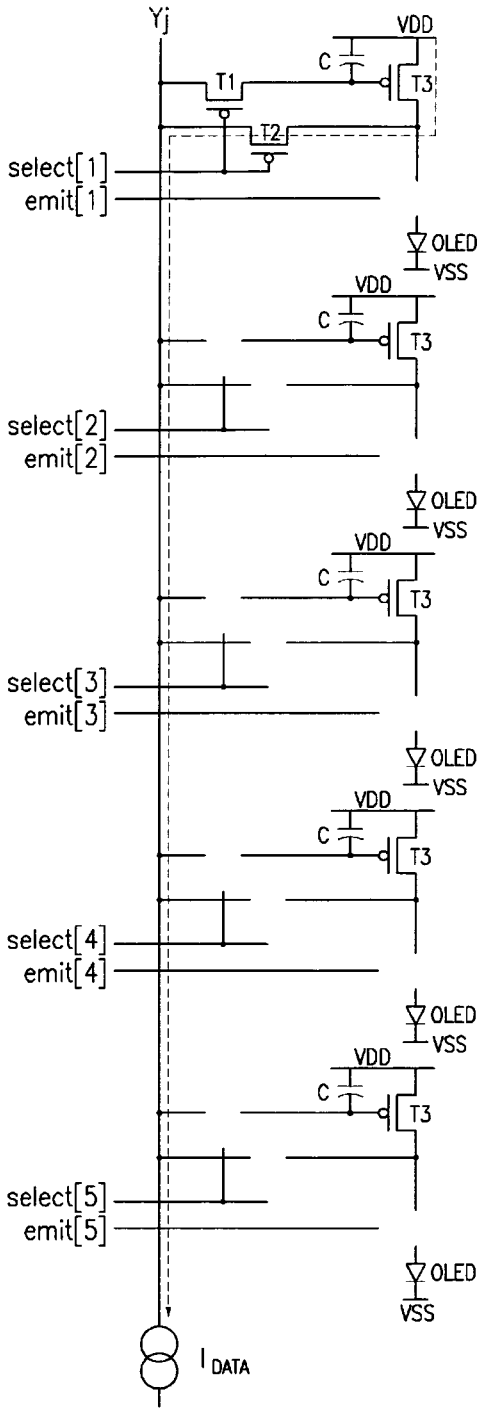

Yj
VDD
C
T1
T3
T2
select[1]
emit[1]
OLED
VSS
VDD
C
T3
select[2]
emit[2]
OLED
VSS
VDD
C
T3
select[3]
emit[3]
OLED
VSS
VDD
C
T3
select[4]
emit[4]
OLED
VSS
VDD
C
T3
select[5]
emit[5]
OLED
VSS
I DATA

FIG.6

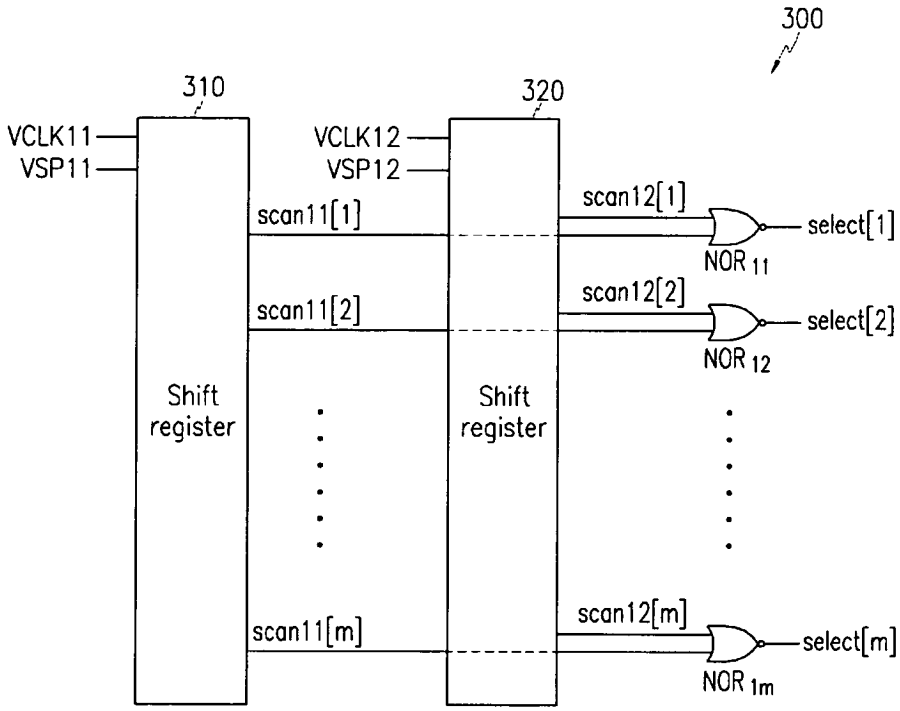

300
310
320
VCLK11
VSP11
VCLK12
VSP12
scan11[1]
scan11[2]
scan11[m]
scan12[1]
scan12[2]
scan12[m]
Shift register
Shift register
NOR 11
NOR 12
NOR 1m
select[1]
select[2]
select[m]

FIG.7

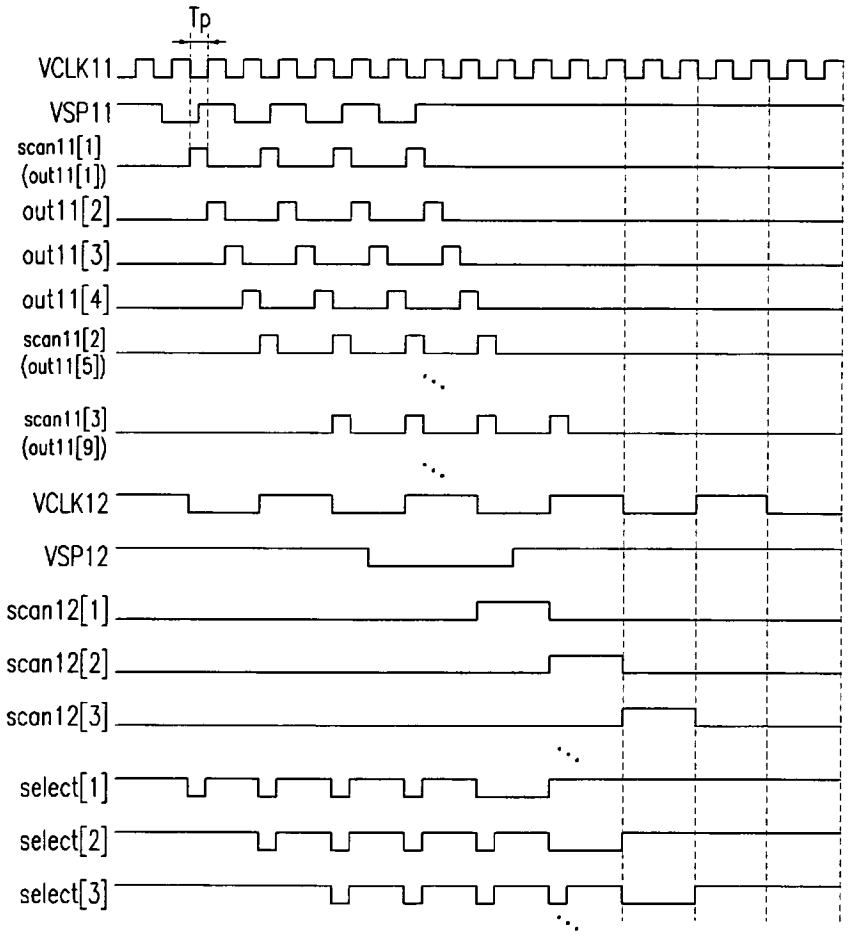

Tp
VCLK11
VSP11
scan11[1]
(out11[1])
out11[2]
out11[3]
out11[4]
scan11[2]
(out11[5])
scan11[3]
(out11[9])
VCLK12
VSP12
scan12[1]
scan12[2]
scan12[3]
select[1]
select[2]
select[3]

FIG.8A

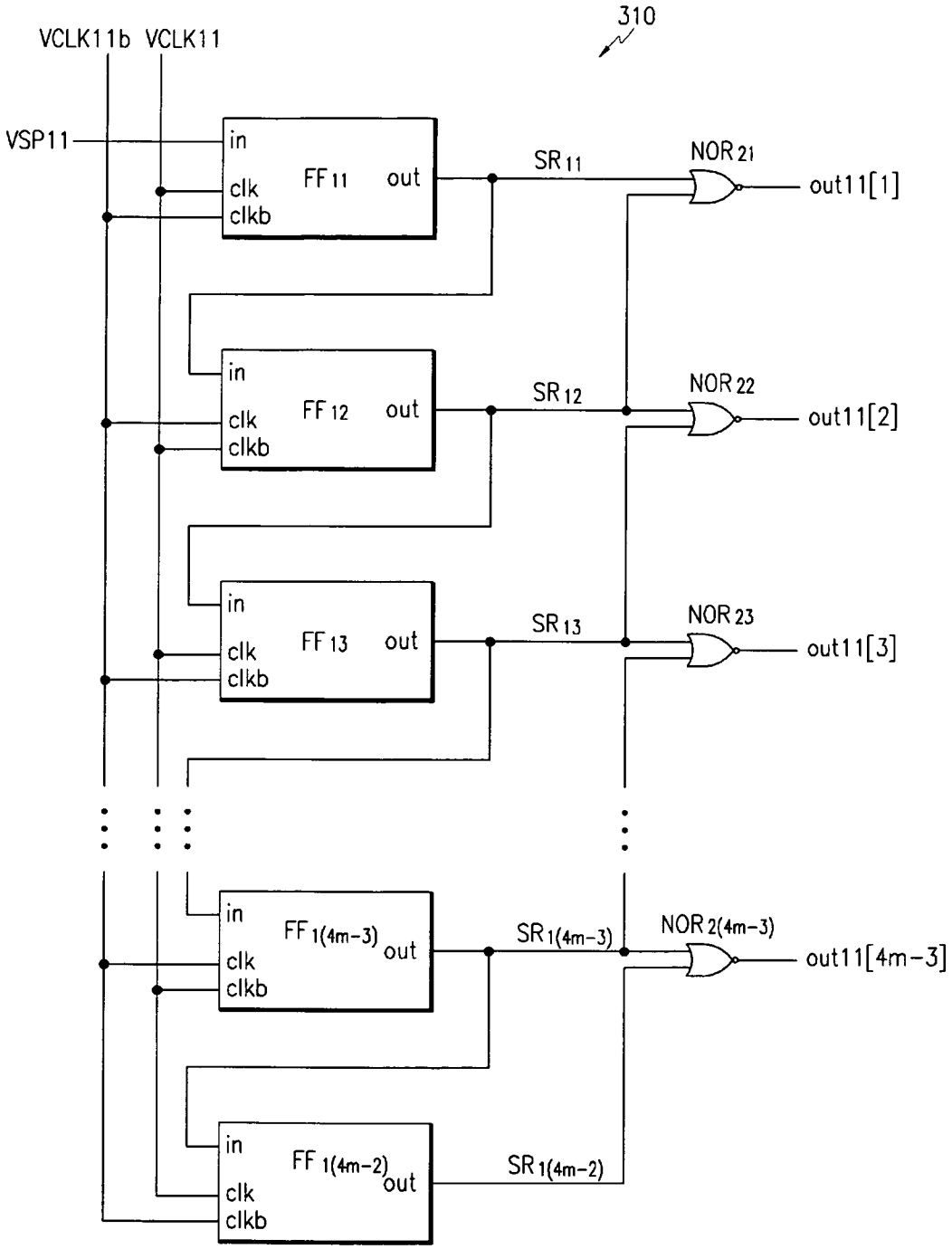

310
VCLK11b
VCLK11
VSP11
in
clk
clkb
FF11
out
SR11
NOR21
out11[1]
FF12
SR12
NOR22
out11[2]
FF13
SR13
NOR23
out11[3]
FF1(4m-3)
SR1(4m-3)
NOR2(4m-3)
out11[4m-3]
FF1(4m-2)
SR1(4m-2)

FIG.8B

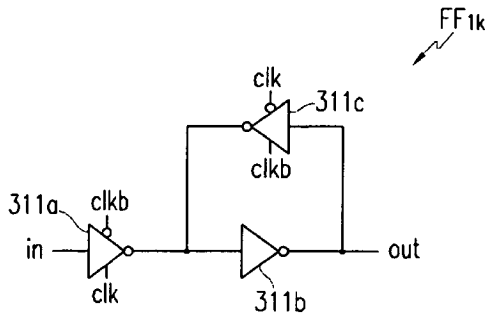

FF1k
clk
311c
clkb
311a
clkb
in
out
clk
311b

FIG.9

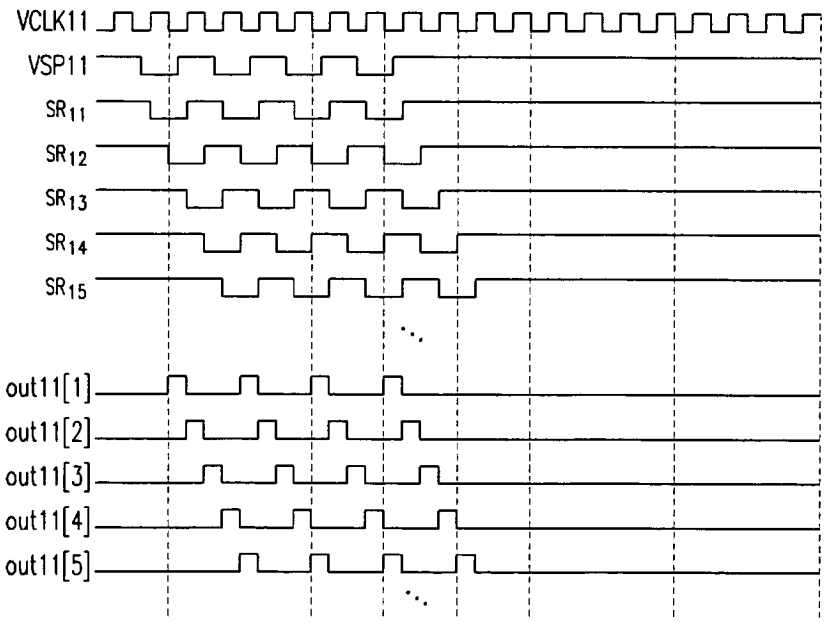

VCLK11
VSP11
SR11
SR12
SR13
SR14
SR15
out11[1]
out11[2]
out11[3]
out11[4]
out11[5]

FIG.10

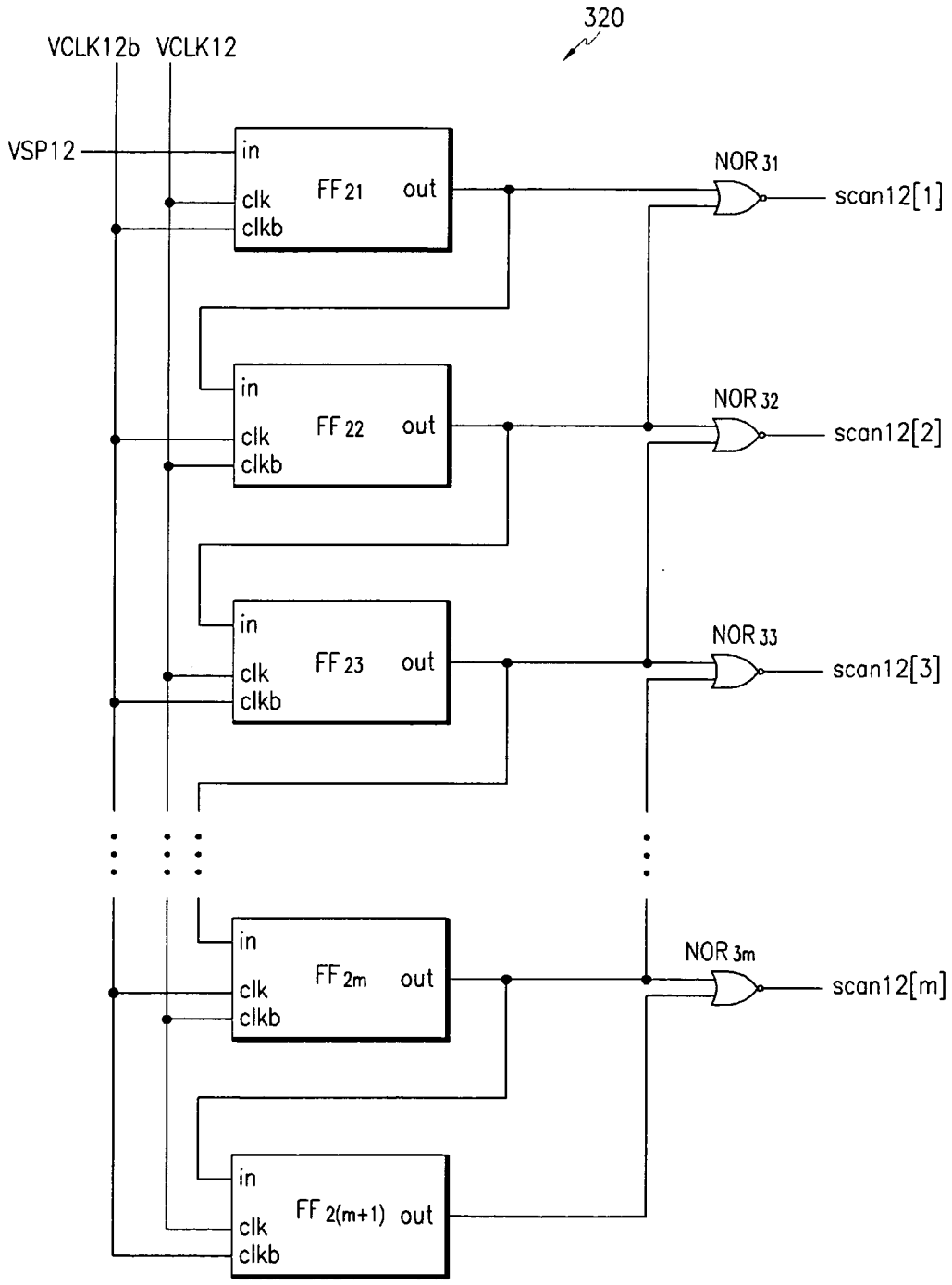

320
VCLK12b
VCLK12
VSP12
in
clk
clkb
FF 21
out
NOR 31
scan12[1]
FF 22
NOR 32
scan12[2]
FF 23
NOR 33
scan12[3]
FF 2m
NOR 3m
scan12[m]
FF 2(m+1)

FIG.11

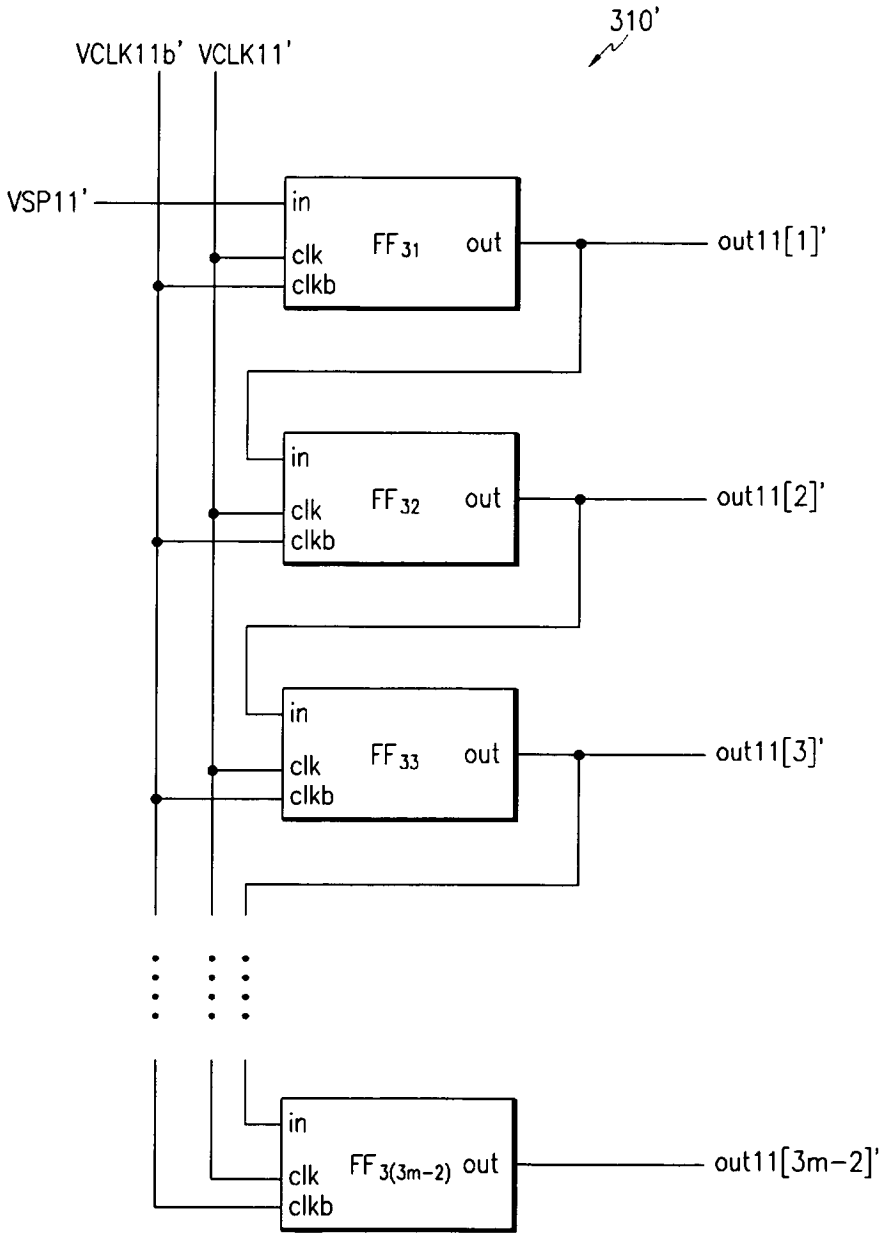

310'
VCLK11b'
VCLK11'
VSP11'
in
clk
clkb
FF31
out
out11[1]'
FF32
out11[2]'
FF33
out11[3]'
FF3(3m-2)
out11[3m-2]'

FIG.12

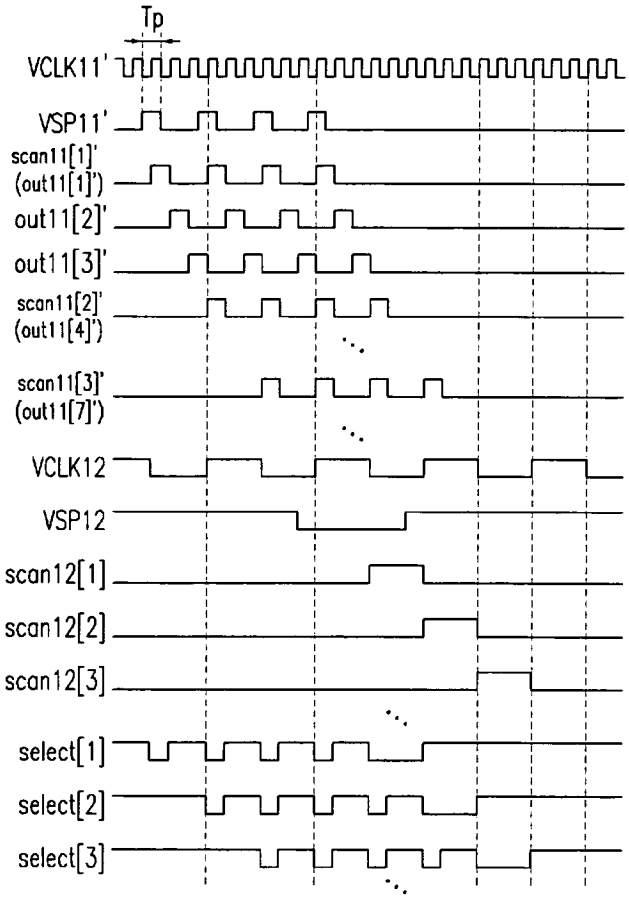

Tp
VCLK11'
VSP11'
scan11[1]'
(out11[1]')
out11[2]'
out11[3]'
scan11[2]'
(out11[4]')
scan11[3]'
(out11[7]')
VCLK12
VSP12
scan12[1]
scan12[2]
scan12[3]
select[1]
select[2]
select[3]

FIG.13A

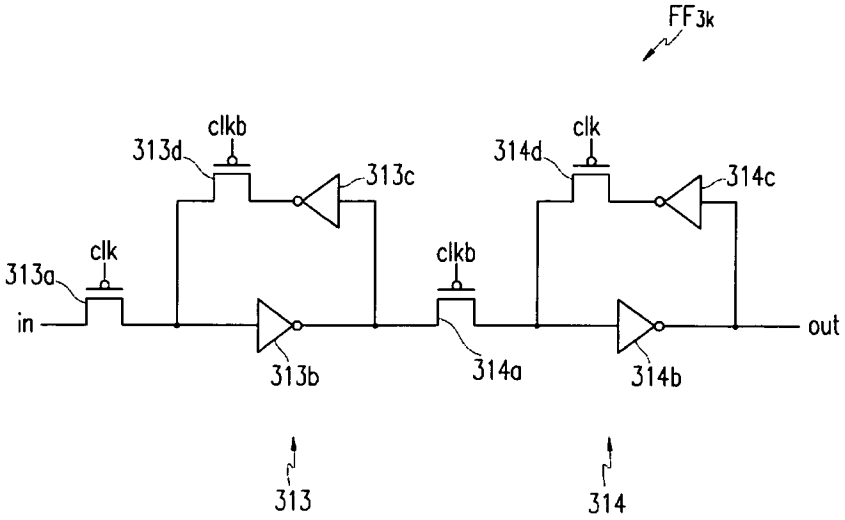


FIG.13B

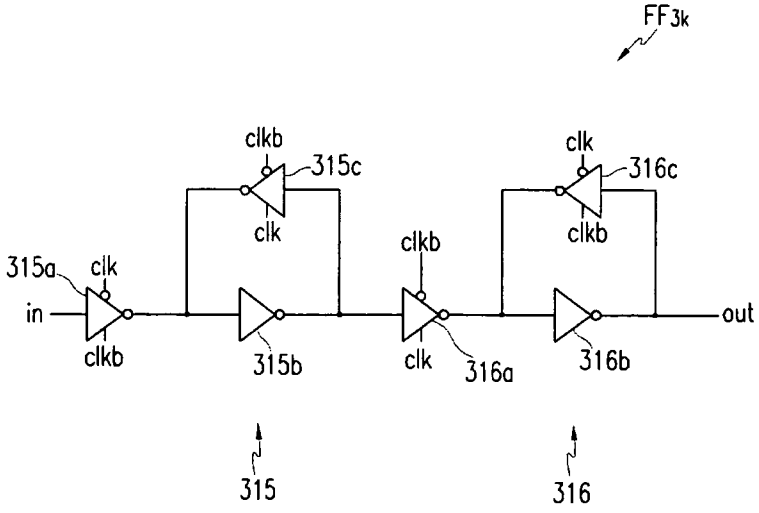


FIG.14

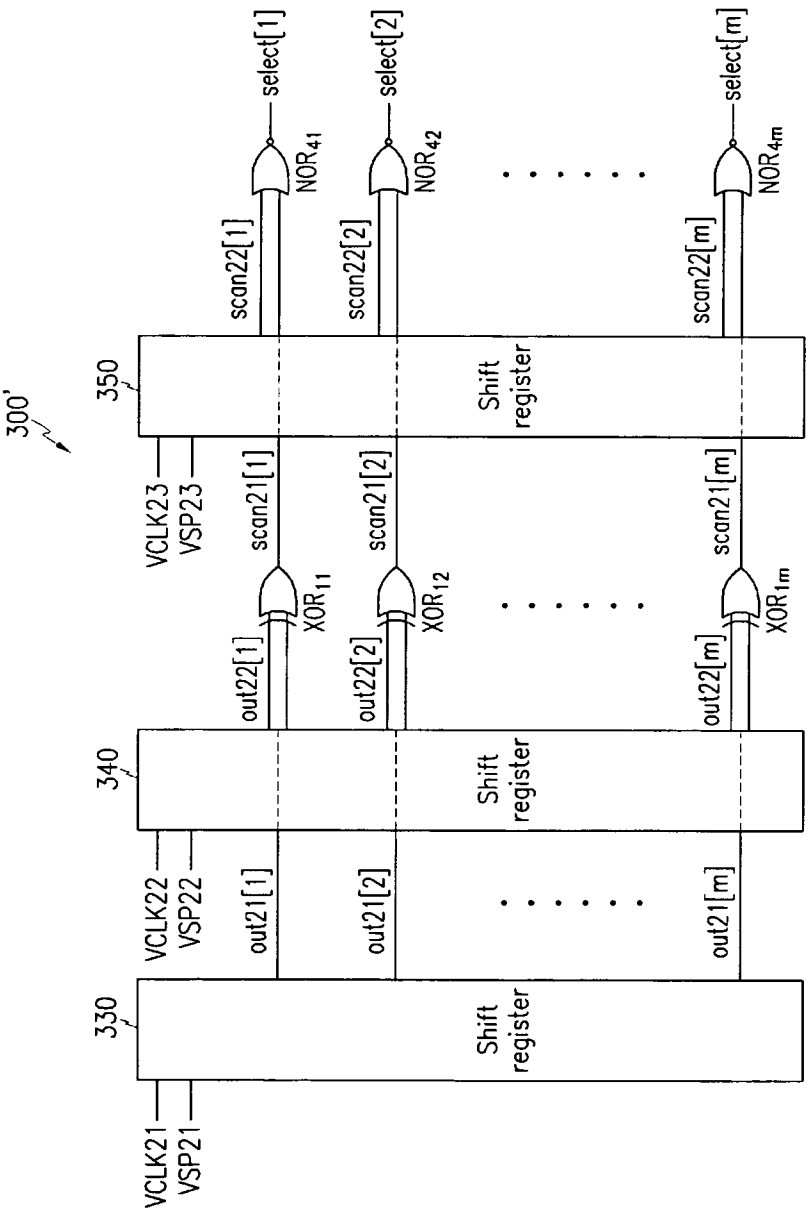

300'
330
340
350
Shift register
Shift register
Shift register
VCLK21
VSP21
VCLK22
VSP22
VCLK23
VSP23
out21[1]
out21[2]
out21[m]
out22[1]
out22[2]
out22[m]
scan21[1]
scan21[2]
scan21[m]
scan22[1]
scan22[2]
scan22[m]
XOR11
XOR12
XOR1m
NOR41
NOR42
NOR4m
select[1]
select[2]
select[m]

FIG.15

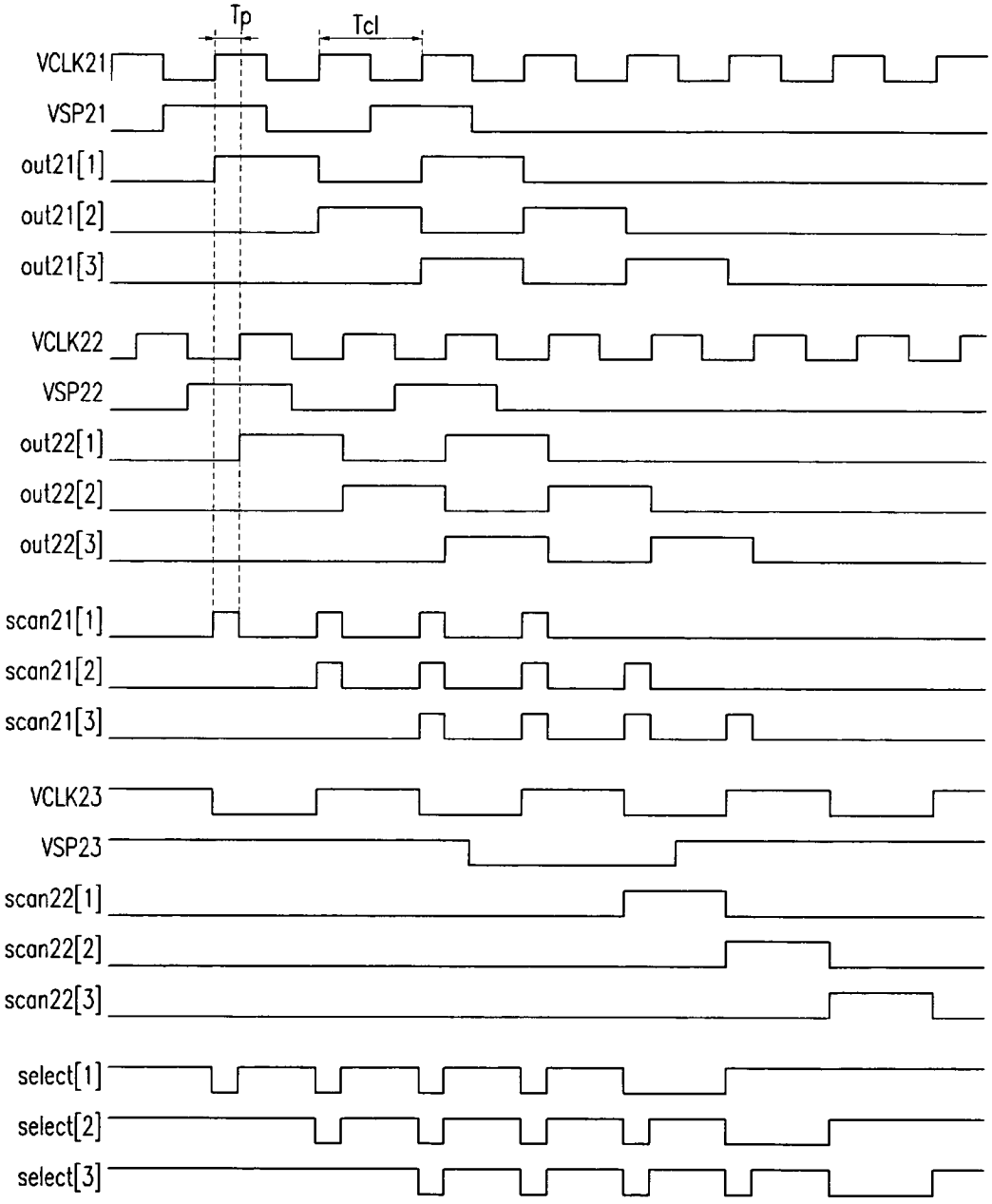

Tp
Tcl
VCLK21
VSP21
out21[1]
out21[2]
out21[3]
VCLK22
VSP22
out22[1]
out22[2]
out22[3]
scan21[1]
scan21[2]
scan21[3]
VCLK23
VSP23
scan22[1]
scan22[2]
scan22[3]
select[1]
select[2]
select[3]

FIG.16

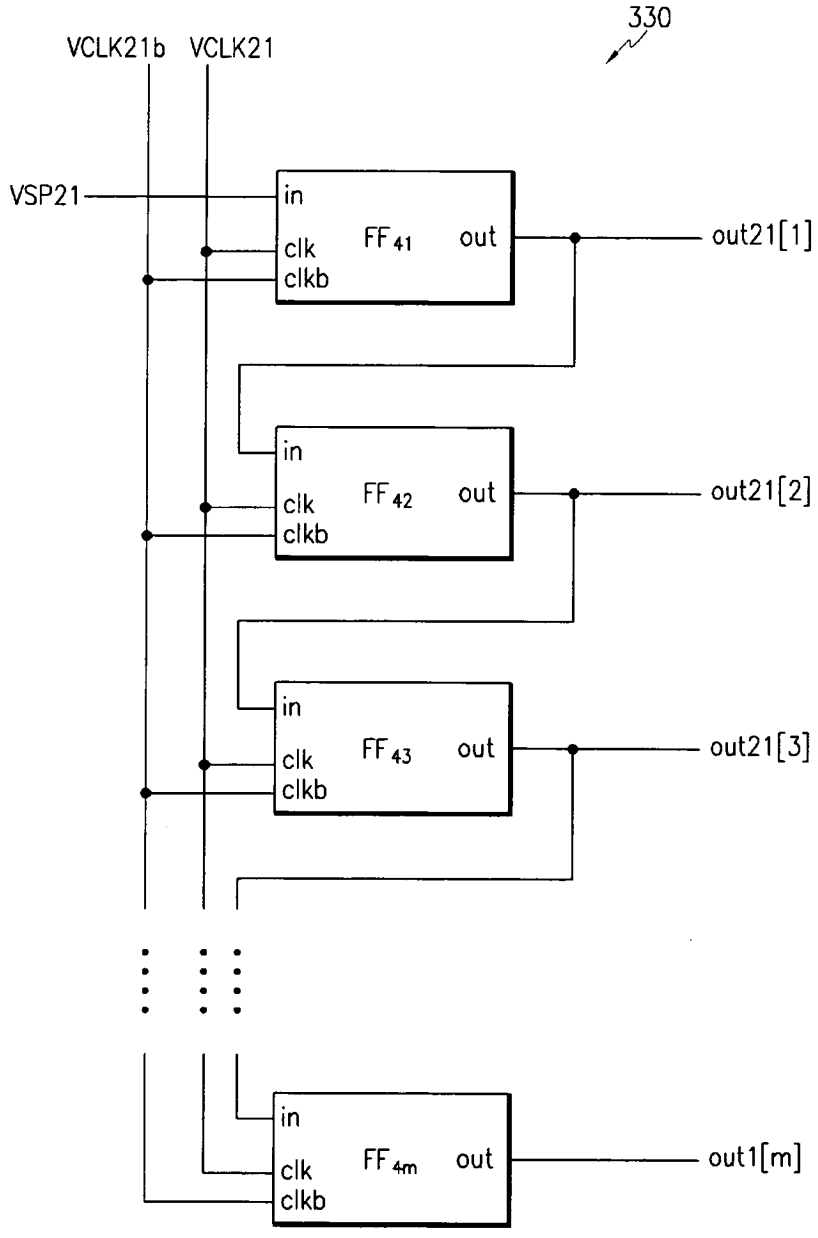

330
VCLK21b
VCLK21
VSP21
in
clk
clkb
FF41
out
out21[1]
FF42
out21[2]
FF43
out21[3]
FF4m
out1[m]

FIG.17

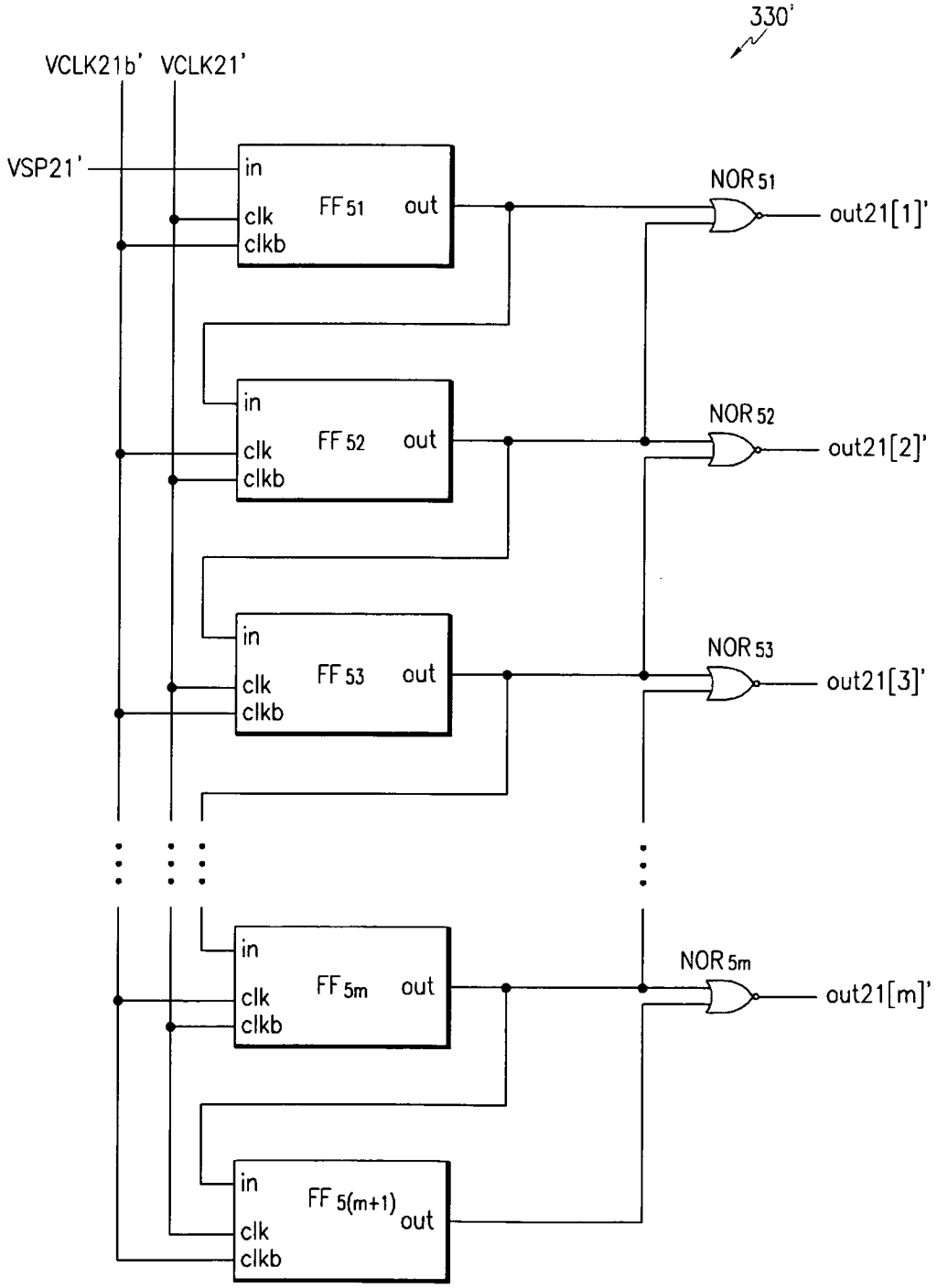

330'
VCLK21b'
VCLK21'
VSP21'
in
clk
clkb
FF 51
out
NOR 51
out21[1]'
FF 52
NOR 52
out21[2]'
FF 53
NOR 53
out21[3]'
FF 5m
NOR 5m
out21[m]'
FF 5(m+1)

FIG.18

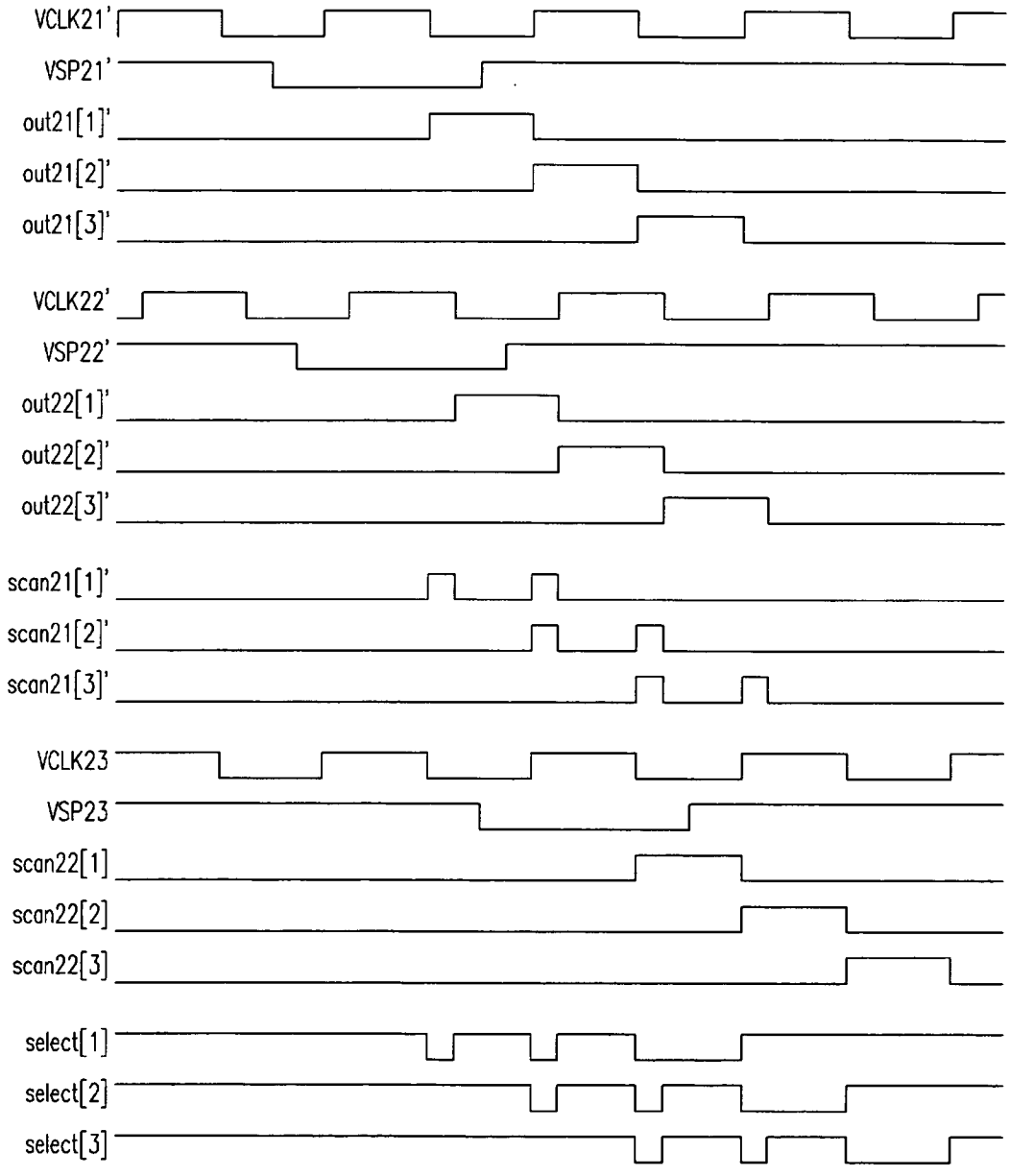

VCLK21'
VSP21'
out21[1]'
out21[2]'
out21[3]'
VCLK22'
VSP22'
out22[1]'
out22[2]'
out22[3]'
scan21[1]'
scan21[2]'
scan21[3]'
VCLK23
VSP23
scan22[1]
scan22[2]
scan22[3]
select[1]
select[2]
select[3]

FIG.19

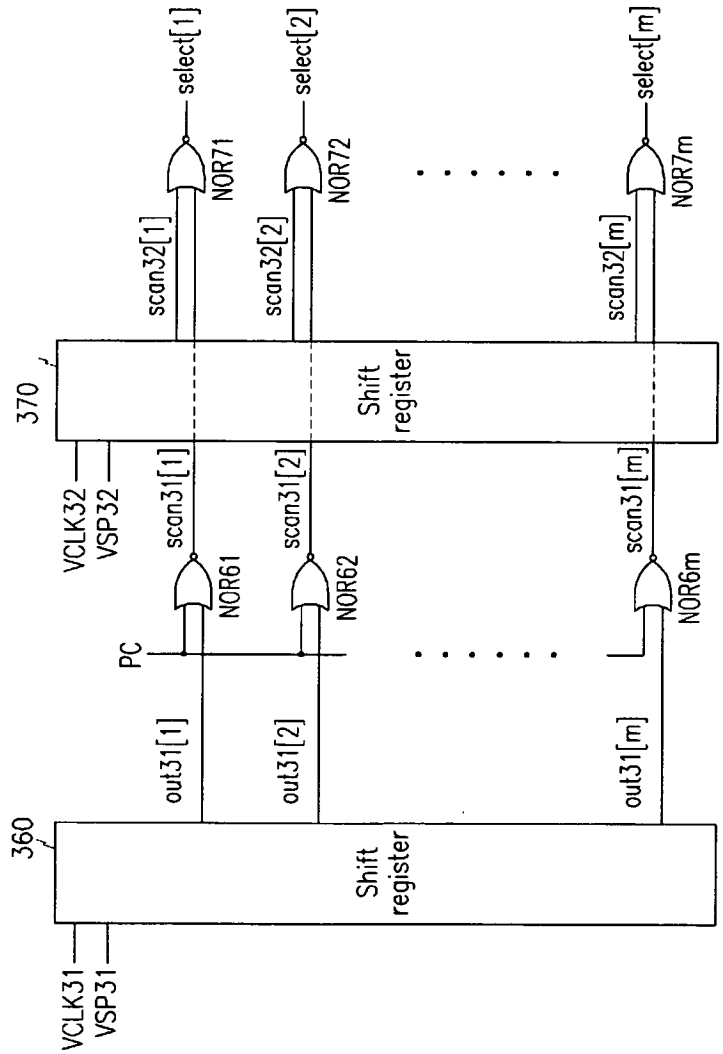

330"
select[1]
select[2]
select[m]
NOR71
NOR72
NOR7m
scan32[1]
scan32[2]
scan32[m]
370
Shift register
VCLK32
VSP32
scan31[1]
scan31[2]
scan31[m]
NOR61
NOR62
NOR6m
PC
out31[1]
out31[2]
out31[m]
360
Shift register
VCLK31
VSP31

FIG.20

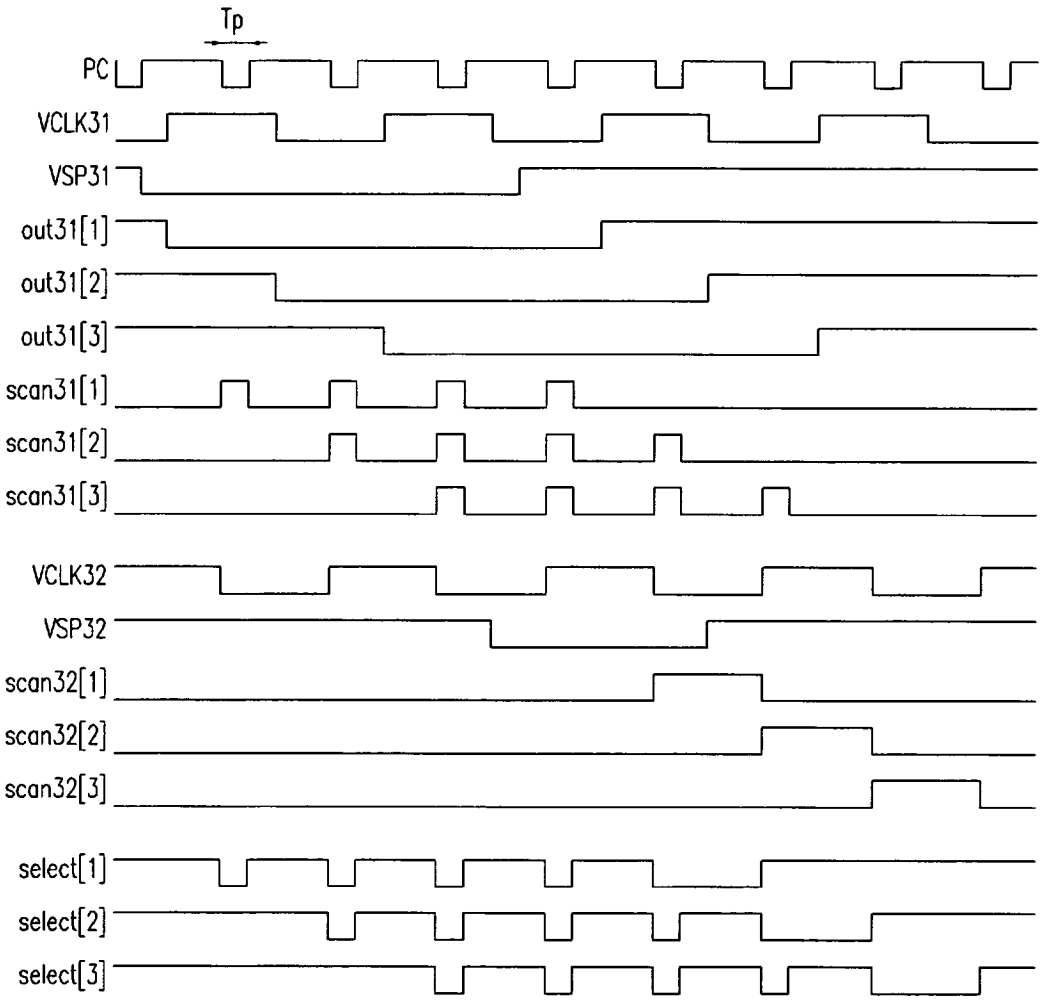

Tp
PC
VCLK31
VSP31
out31[1]
out31[2]
out31[3]
scan31[1]
scan31[2]
scan31[3]
VCLK32
VSP32
scan32[1]
scan32[2]
scan32[3]
select[1]
select[2]
select[3]

FIG.21

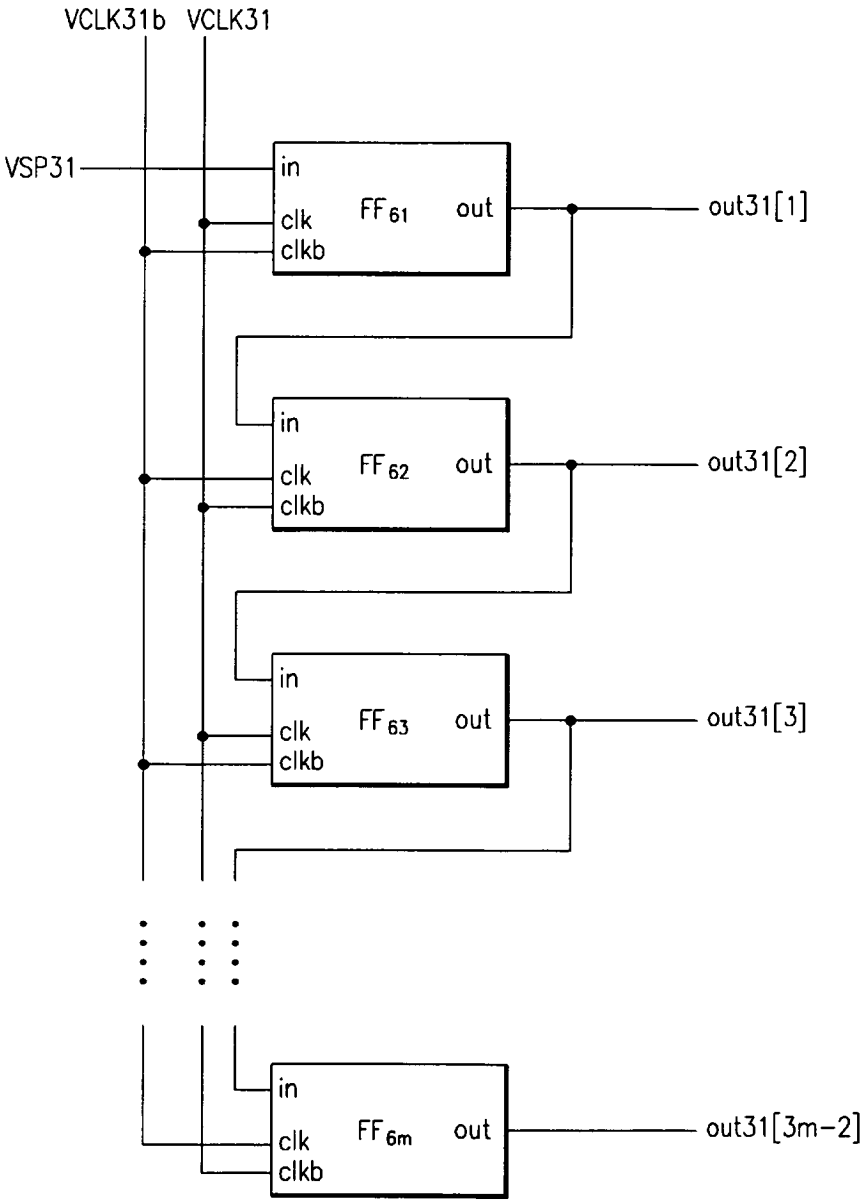

VCLK31b
VCLK31
VSP31
in
clk
clkb
FF61
out
out31[1]
FF62
out31[2]
FF63
out31[3]
FF6m
out31[3m-2]

FIG.22

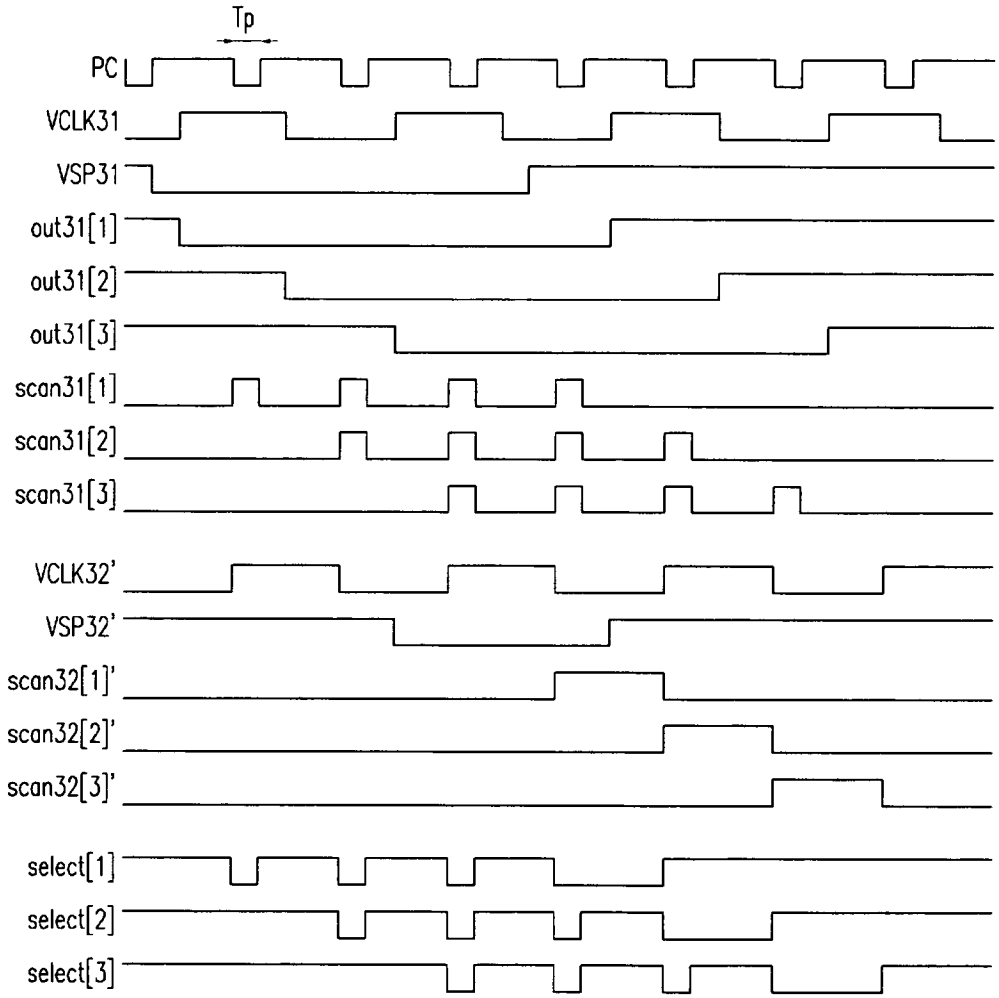

Tp
PC
VCLK31
VSP31
out31[1]
out31[2]
out31[3]
scan31[1]
scan31[2]
scan31[3]
VCLK32'
VSP32'
scan32[1]'
scan32[2]'
scan32[3]'
select[1]
select[2]
select[3]

FIG.23

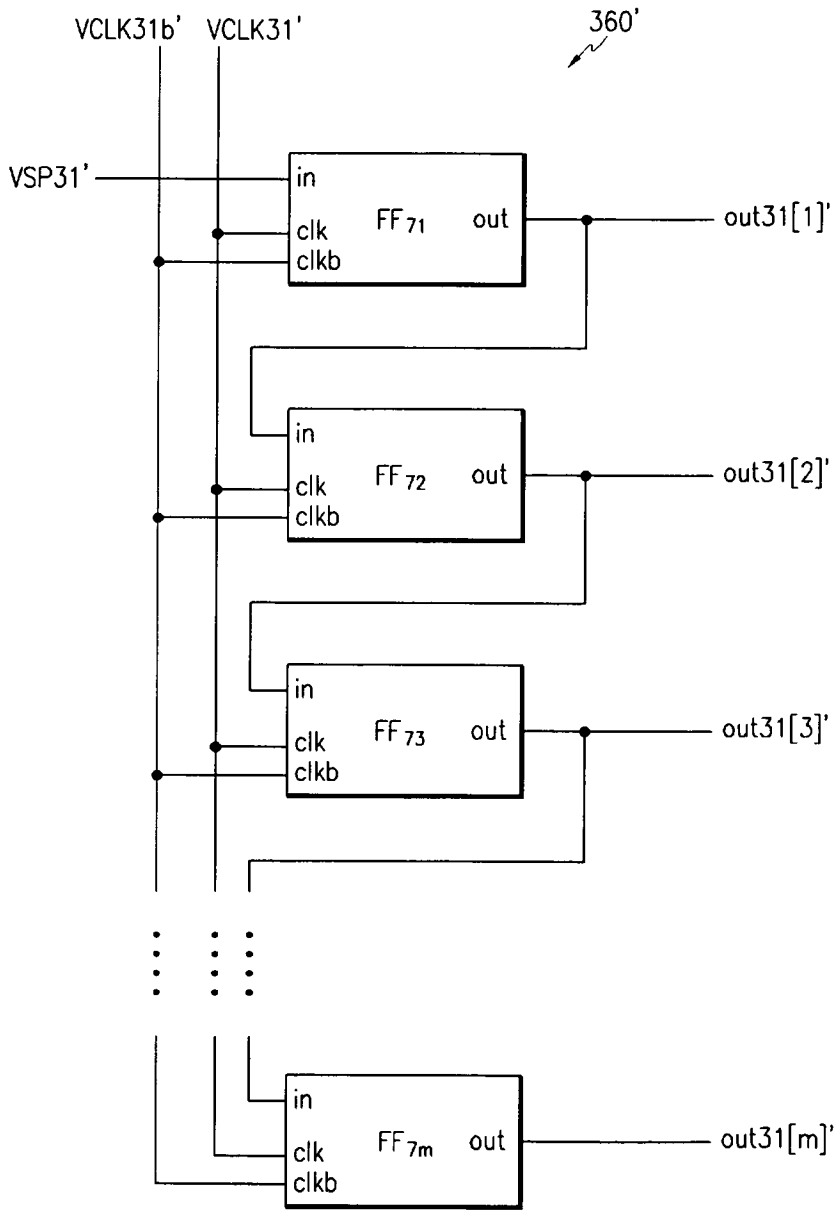

VCLK31b'
VCLK31'
360'
VSP31'
in
clk
clkb
FF71
out
out31[1]'
FF72
out31[2]'
FF73
out31[3]'
FF7m
out31[m]'

FIG.24

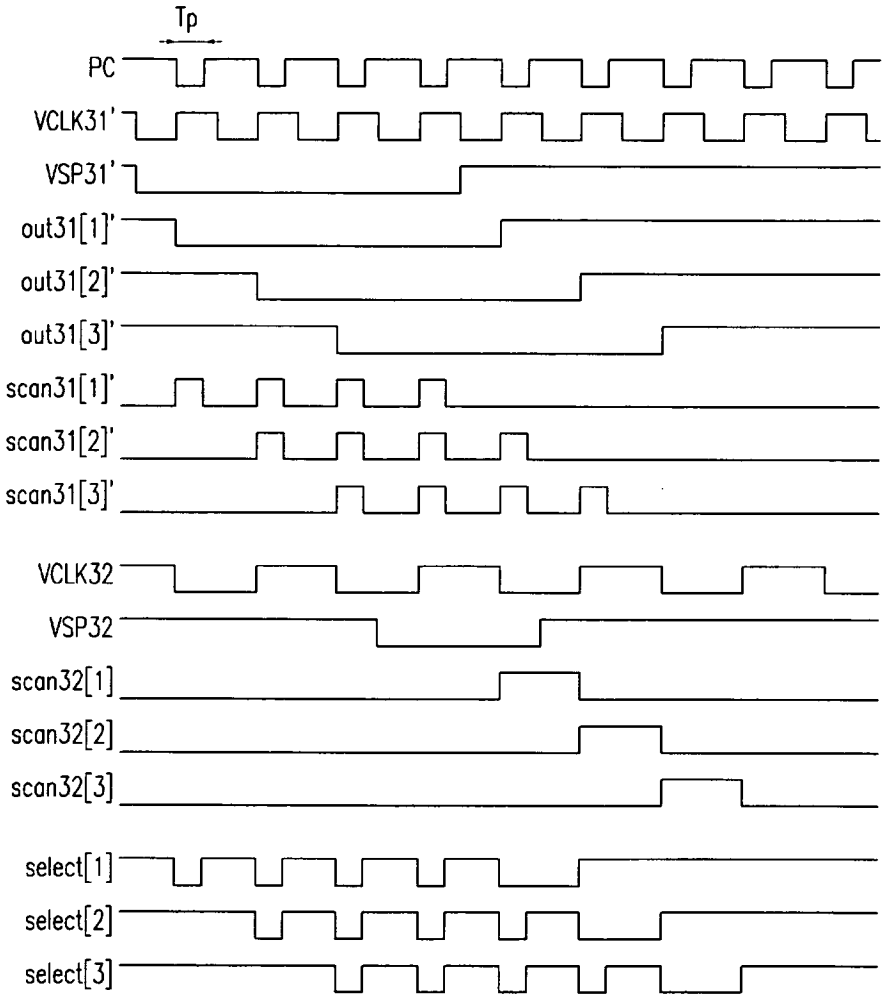
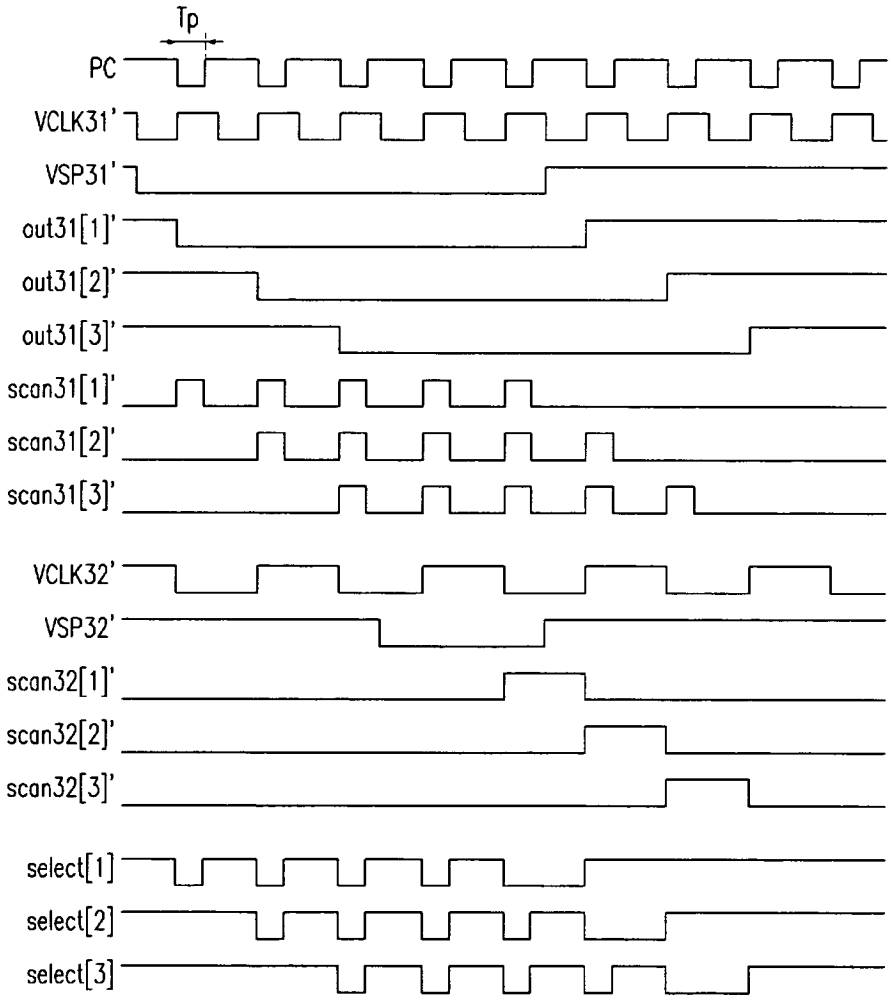

Tp
PC
VCLK31'
VSP31'
out31[1]'
out31[2]'
out31[3]'
scan31[1]'
scan31[2]'
scan31[3]'
VCLK32
VSP32
scan32[1]
scan32[2]
scan32[3]
select[1]
select[2]
select[3]

FIG.25


Tp
PC
VCLK31'
VSP31'
out31[1]'
out31[2]'
out31[3]'
scan31[1]'
scan31[2]'
scan31[3]'
VCLK32'
VSP32'
scan32[1]'
scan32[2]'
scan32[3]'
select[1]
select[2]
select[3]

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 6417830 B **[0006]**
- EP 1424674 A **[0007]**
- EP 1061497 A **[0008]**

专利名称(译)	发光显示器及其驱动装置和方法		
公开(公告)号	EP1610293B1	公开(公告)日	2008-08-06
申请号	EP2005105436	申请日	2005-06-21
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IPC分类号	G09G3/32 G09G3/20 G09G3/30 G11C19/00		
CPC分类号	G09G3/325 G09G3/3266 G09G2300/0842 G09G2300/0861 G09G2310/0251 G11C19/00 G11C19/28		
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优先权	1020040048154 2004-06-25 KR 1020040048152 2004-06-25 KR 1020040048153 2004-06-25 KR		
其他公开文献	EP1610293A3 EP1610293A2		
外部链接	Espacenet		

摘要(译)

一种用于发光显示器的驱动装置，包括用于传输选择信号的多条扫描线，包括：第一驱动器，用于将具有第一整数倍的第一脉冲的第一信号移位第一周期，并依次输出第一驱动器信号;第二驱动器，用于将具有第二脉冲的第二信号移位第二周期，并顺序输出第二信号;第三驱动器，用于响应于第一信号和顺序输出具有与第一脉冲的第一整数倍中的至少一个相对应的第三整数倍的第二整数倍的选择信号，以及与第二脉冲相对应的第四脉冲。第二个信号。

Equation 1

$$I_{OLED} = \frac{\beta}{2}(V_{GS} - V_{TH})^2 = I_{data}$$