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Description

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Korea Patent Application No. 2003-84746, filed on November 26, 2003.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to a flat panel display and, more particularly, to an active matrix organic light emitting device capable of avoiding a defective element and improving picture quality by reducing a taper angle of a substrate surface.

2. Background of the Invention

[0003] In general, pixels in an active matrix organic light emitting device (AMOLED) are arranged on the substrate in a matrix form. Each pixel includes an electroluminescence (EL) element, where an anode electrode, an organic film layer and a cathode electrode are stacked, and a thin film transistor (TFT) as an active element connected to the EL element and for driving the EL element.

[0004] FIG. 1A shows a cross-sectional view of a conventional bottom-emitting OLED. Referring to FIG. 1A, a semiconductor layer 110 has a buffer layer 105 formed on an insulating substrate 100 and source and drain regions 111 and 115 formed on the buffer layer 105. A gate 125 is formed on a gate insulating layer 120, and source and drain electrodes 141 and 145 are formed on an inter-layer insulating layer 130 through contact holes 131 and 135, to be connected to the source and drain region 111 and 115, respectively. As a result, the TFT is fabricated. Wiring 147, such as a data line or a power supply line, is formed on the inter-layer insulating layer 130.

[0005] An anode electrode 170, as a lower electrode connected to the drain electrode 145 through a via hole 155, is formed on a passivation layer 150, and an organic film layer 185 and a cathode electrode 190, as an upper electrode, are formed on the substrate, thereby fabricating the organic EL element.

[0006] FIG. 1B shows a detailed cross-sectional view of the red on R pixel EL element within an emission region of an R pixel in the OLED of FIG. 1A. A method for fabricating the EL diode is described in detail below, with reference to FIG. 1B. A cleaning process is performed after forming the anode electrode 170 connected to the drain electrode of the TFT through the via hole 155. A 60nm thick hole injecting layer 185a is then formed with CuPc on the substrate using a vacuum deposition method, and a 30nm thick hole transporting layer 185b is formed with NPB on the hole injecting layer 185a. A 20nm thick Alq+DCM is deposited on the hole transporting layer 185b to form a red color emission layer 185c. A 20nm thick Alq3 is formed on the red color emission layer 185c to form an electron transporting layer 185d, thereby forming the organic film layer 185. Finally, a LiF/Al, as the cathode electrode 190, is deposited by a thermal evaporation method. Although not shown in the figure, a hole blocking layer may be formed between the red color emission layer 185c and the electron transporting layer 185d, or an electron injecting layer may be formed on the electron transporting layer 185d.

[0007] After forming the organic film layer 185 and the cathode electrode 190 on the anode electrode 170, as shown in FIG. 1B, a sealant (not shown) is applied on the insulating substrate 100, and an encapsulating substrate is bonded to the insulating substrate to prevent external oxygen and moisture from being introduced inside, thereby fabricating the conventional OLED.

[0008] The conventional OLED having the above mentioned structure may have pinhole defects occurring near a stepped portion of the anode electrode 170, near the via hole 155 and near the contact holes 141 and 145, and/or short-circuit defects between the anode and cathode electrodes. Furthermore, portions where the organic emission layer is not deposited or not uniformly deposited may be thinner than other portions near the stepped portion of the anode electrode and near the contact holes and via holes. When a high voltage is applied between the anode and cathode electrodes, a current density may focus on the portion where the organic emission layer is not deposited or is thinly deposited, so that one or more spherical dark spot may occur. As a result, the emission region may decrease and the picture quality may deteriorate due to the occurrence of the dark spot.

[0009] Oxygen and/or moisture may be more easily introduced through a portion where the cathode electrode is not densely formed. When a high voltage is applied between the anode and cathode electrodes, a current density is focused on the portion where the cathode electrode is not densely formed, and a void occurs in the cathode electrode due to an electromigration. Heat may occur due to increased resistance from an external oxygen inflow. As a result, a spherical dark spot may occur in the portion as time passes.

[0010] To prevent defects, such as a short-circuit or the dark spot, a contact hole or via hole may be formed having

a small taper angle. However, there has been a limit in reducing the taper angle of the contact hole or via hole due to difficulties in design of a high resolution flat panel display.

[0011] U.S. Patent Number 5,684,365 discloses a technique that limits a taper angle of a passivation layer at an edge of an opening for exposing some portions of the anode electrode. FIG. 2 illustrates a cross-sectional view of a conventional bottom-emitting OLED. Referring to FIG. 2, a buffer layer 205 is formed on an insulating substrate 200, and a semiconductor layer 210 having source and drain regions 211 and 215 is formed on the buffer layer 205. A gate 225 is formed on a gate insulating layer 220, and source and drain electrodes 241 and 245 are formed to be connected to the source and drain regions 211 and 215, respectively, through contact holes 231 and 235 on an inter-layer insulating layer 230. In this case, an anode electrode 270, as a lower electrode to be connected to the drain electrode 245, is formed on the inter-layer insulating layer 230.

[0012] After depositing a passivation layer 250, at a thickness of 0.5 to 1.0 μm formed of an insulating layer, such as an silicon nitride layer, on a substrate, the passivation 250 is etched to form an opening 275 exposing some portions of the anode electrode 270. In this case, the passivation layer 250 is formed to have a taper angle of 10 to 30° with respect to the anode electrode at an edge of the opening 275. An organic film layer 285 and a cathode electrode 290 as an upper electrode are then formed on the substrate. The organic film layer 285 has at least one of a hole injecting layer, a hole transporting layer, an R, G, or B emission layer, a hole barrier layer, an electron transporting layer, or an electron injecting layer, as shown in FIG. 1B.

[0013] U.S. Patent Number 6,246,179 discloses a technique that uses an organic insulating layer having a planarizing function to prevent defects from occurring near a via hole or a contact hole and at a stepped portion. FIG. 3 shows a cross-sectional view of the OLED having a conventional top-emitting structure. Referring to FIG. 3, a buffer layer 305 is formed on an insulating substrate 300, and a semiconductor 310, having source and drain regions 311 and 315, is then formed on the buffer layer 305. A gate 325 is formed on a gate insulating layer 320, and source and drain electrodes 341 and 345 are connected to the source and drain regions 311 and 315, respectively, through contact holes 331 and 335 on an inter-layer insulating layer 330. In this case, wiring 347, such as a data line or a power supply line, is formed at the same time the source and drain electrodes 341 and 345 are formed on the inter-layer insulating layer 330.

[0014] A planarization layer 360 is formed on a passivation layer 350, and an anode electrode, as a lower electrode, is connected to one electrode, for example, to the drain electrode 345 between the source and drain regions 341 and 345 through the via hole 355 on the planarization layer 360. A pixel defining layer 365, having an opening 375 for exposing some portions of an anode electrode 370, is formed, and an organic film layer 385 and a cathode electrode 390 as an upper electrode are formed on the pixel defining layer 365 and the anode 370. The organic film layer 385 has at least one of a hole injecting layer, a hole transporting layer, a R, G, or B emission layer, a hole blocking layer, an electron transporting layer and an electron injecting layer, as shown in FIG. 1B.

[0015] As in the above mentioned conventional OLED, a taper angle of the passivation layer connected to the anode electrode within the opening is limited to between 10° to 30°, or a taper angle of the pixel defining layer is limited to between 20° to 80°, thereby preventing defects in the organic emission layer. In addition, the problem of the stepped portion may be solved by using the planarization layer, thereby preventing the defect of the organic emission layer.

[0016] U.S. Patent application 2002/113248 A1 and European patent applications 1 331 667 A2 and 1 058 311 A2 deal with a flat panel display comprising a lower layer formed on an insulating substrate and having a first step and a first taper angle with respect to a surface of the substrate and an upper layer formed on the insulating substrate for reducing the taper angle of the lower layer, wherein the upper layer has a second taper angle smaller than the first taper angle of the lower layer.

[0017] European patent application 1 315 209 A2 discloses a flat panel display, comprising an insulating substrate, a lower layer formed on the insulating substrate and having a first step and a first taper angle with respect to a surface of the substrate, and an upper layer formed on the insulating substrate. Furthermore, EP 1 063 704 A and US 2003/0047736 A1 are directed to light emitting devices comprising an organic emission layer.

[0018] However, in the high-resolution OLED, there has been a limit to reducing the taper angle of the passivation layer or the pixel defining layer due to difficulties in the design process. Furthermore, the reliability of the element depends on a taper angle between the pixel defining layer and the anode electrode. When the taper angle is large, the organic emission layer and the cathode electrode easily deteriorate at the edge of the opening. When the taper angle is small, there has been a limit to reducing the taper angle and thickness of the pixel defining layer due to problems of parasitic capacitance and a stepped portion caused by the wiring.

[0019] In addition, since the cathode electrode deposited on the entire surface of the substrate is not densely formed near the contact hole, near the via hole and at the stepped portion, as described above, dark spot may occur, or a pinhole or short-circuit defect may occur near the contact hole, near the via hole and at the stepped portion.

SUMMARY OF THE INVENTION

[0020] The present invention provides an OLED capable of preventing pinhole and short-circuit defects in a contact

hole and a via hole.

[0021] The present invention provides an OLED capable of improving a picture quality by reducing or preventing a pattern defect of an organic EL layer.

[0022] The present invention provides an OLED capable of reducing or preventing inflow of oxygen or moisture by densely forming a cathode electrode.

[0023] The present invention provides an OLED capable of reducing or preventing a dark spot from being occurred in an emission region of a pixel.

[0024] In the embodiment of the present invention, a flat panel display according to claim 1 includes an insulating substrate, a thin film transistor formed on the insulating substrate, the thin film transistor includes a semiconductor layer having source and drain regions, a first insulating layer having contact holes for exposing some portions of the source and drain regions, and source and drain electrodes connected to the source and drain regions through the contact holes, a second insulating layer formed on the insulating substrate and having a via hole for exposing one of the source and drain electrodes, an EL element formed on the second insulating layer to be connected to one electrode of the thin film transistor through the via hole and having a lower electrode, an organic film layer comprising at least an organic emission layer and an upper electrode, and a taper reducing layer formed on the lower electrode, on the second insulating layer and on the source and drain electrodes. The taper reducing layer is a conductive organic layer having a charge transporting capability, and the edge of the lower electrode is covered by the taper reducing layer. The taper reducing layer is formed between the lower electrode and the emission layer, and a taper angle of the taper reducing layer in a position corresponding to the contact hole in which the other one of the source and drain electrodes which is not connected with the electroluminesence element is formed has a first taper angle smaller than a taper angle of the corresponding contact hole, a taper angle of the taper reducing layer in a position corresponding to the via hole has a second taper angle smaller than a taper angle of the via hole, and a taper angle of the taper reducing layer at an edge of the lower electrode has a third taper angle smaller than a taper angle of the edge of the lower electrode, wherein the taper angle of the contact hole in which the other one of the source and drain electrodes which is not connected with the electroluminesence element is formed, the taper angle of the via hole and the taper angle at an edge of the lower electrode are planarized by the taper reducing layer, and wherein the first, second, and third taper angles are greater than zero degrees.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing in detail preferred embodiments thereof with reference to the attached drawings.

FIG. 1A illustrates a cross-sectional view of a conventional OLED.

FIG. 1B illustrates a cross-sectional view of an emission region of one pixel in the OLED shown in FIG. 1A.

FIG. 2 illustrates a cross-sectional view of a conventional OLED having a passivation layer where the edge is tapered.

FIG. 3 illustrates a cross-sectional view of a conventional OLED having a pixel defining layer.

FIG. 4 illustrates a cross-sectional view of an OLED employing a taper reducing layer according to an embodiment of the present invention.

FIG. 5A illustrates a taper angle and number of defects in an OLED that has employed a taper reducing layer according to an embodiment of the present invention.

FIG. 5B illustrates a relationship between the taper angle and the thickness of the taper reducing layer in the OLED shown in FIG. 3.

FIG. 6A illustrates a cross-sectional view of a bottom-emitting AMOLED in accordance with the embodiment of the present invention.

FIG. 6B illustrates a cross-sectional view of the emission region of one pixel in the bottom-emitting AMOLED shown in FIG. 6A.

FIG. 6C illustrates a cross-sectional view of the emission region of one pixel in the bottom-emitting AMOLED shown in FIG. 6A.

FIG. 7A illustrates the reduced taper angle by the taper reducing layer in the AMOLED shown in FIG. 6A.

FIG. 7B illustrates a pixel that the dark spot is not occurred in the AMOLED shown in FIG. 6A.

FIG. 7C illustrates that defects occur in the pixel when the taper reducing layer is not employed in the conventional bottom-emitting OLED.

FIG. 8 illustrates a cross-sectional view of a bottom-emitting AMOLED having a pixel defining layer in accordance with an embodiment which is not part of the present invention.

FIG. 9A illustrates that the taper angle is reduced by the taper reducing layer in the AMOLED shown in FIG. 8.

FIG. 9B illustrates a pixel that the dark spot is not occurred in the AMOLED shown in FIG. 8.

FIG. 9C illustrates a pixel where dark spots occur in an OLED having a conventional pixel defining layer.

FIG. 10 illustrates a cross-sectional view of a top-emitting AMOLED in accordance with another embodiment which

is not part of the present invention.

FIG. 11 illustrates a cross-sectional view of a top-emitting AMOLED having a pixel defining layer in accordance with a further embodiment which is not part of the present invention.

FIG. 12 illustrates a cross-sectional view of an AMOLED in accordance with yet another embodiment which is not part of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments are shown, not all of them according to the invention. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention as claimed to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout the specification.

[0027] FIG. 4 illustrates a cross-sectional view of an OLED having a taper angle reduced by a taper reducing layer of the present invention. Referring to FIG. 4, an insulating substrate 40 has a lower layer 41 having an opening 42 for exposing a portion of the insulating substrate 40. The lower layer 41 has a predetermined taper angle with respect to an upper surface of the substrate at an edge of the opening 42. Furthermore, the lower layer 41 has a predetermined step d0 with respect to the upper surface of the substrate.

[0028] A taper reducing layer 43 having a taper angle $\theta 2$ is formed on the lower layer 41 and the opening 42. The deposition thickness of the taper reducing layer 43 may depend on the step of the substrate surface where the taper reducing layer is deposited. In other words, the taper reducing layer deposited on a portion where the substrate surface has a high step is deposited thinner than the taper reducing layer deposited on a portion where the substrate surface has a low step. Thus, the taper reducing layer 43 has a thickness of d2 on the lower layer having the step d0, and has a thickness of d3, thicker than d2 on the opening 42, for exposing the substrate. Since the thickness of the taper reducing layer 43 depends on the step of the substrate surface, the taper reducing layer 43 has a taper angle smaller than the taper angle at the lower layer 41. As a result, the taper reducing layer 43 has a taper angle $\theta 2$ smaller than the taper angle $\theta 1$ of the lower layer 41.

[0029] In the OLED of an embodiment of the present invention, when the lower layer 41 is an insulating layer, such as an inter-layer insulating layer and a gate insulating layer, the opening 42 is a contact hole and exposes some portions of the source and drain regions. Thus, the taper angle of the contact hole becomes $\theta 1$, and the step formed by the contact hole in the insulating layer, with respect to the substrate surface, is d0.

[0030] When the lower layer 41 is a passivation layer, the opening 42 is a via hole and exposes a portion of the source and drain electrodes. Thus, the taper angle of the via hole becomes $\theta 1$, and the step formed by the via hole in the passivation layer with respect to the substrate surface is d0. When the lower layer 41 is a pixel defining which is not according to the invention, the opening 42 exposes a portion of a pixel electrode. Thus, the taper angle of the pixel defining layer at the edge of the opening becomes $\theta 1$, and the step formed by the opening in the pixel defining layer with respect to the substrate surface is d0.

[0031] When the taper reducing layer 43 is formed within the contact hole, via hole, or opening of the pixel defining layer, a conductive layer is formed over and below the taper reducing layer 43, so that the taper reducing layer 43 is formed of a conductive material. An organic layer that has a charge transporting capability and may be coated by a wet coating method is used for the taper reducing layer 43. The taper reducing layer 43 may consist of at least one organic layer selected from a polymer organic layer, a small-molecule organic layer or similar material. The small-molecule organic layer for the taper reducing layer may be selected from carbazole-based, arylamine-based, hydrazone-based, stilbene-based, oxadiazole-based and starburst-based derivatives, and the polymer organic layer is selected from PEDOT, PANI, carbazole-based, arylamine-based, perylene-based, pyrrole-based and oxadiazole-based derivatives or similar materials.

[0032] In the above mentioned OLED, the principle that the taper angle is reduced by the taper reducing layer is as follows. The lower layer 41 has an opening 42, such as the contact hole, via hole, or not according to the invention, the region of the pixel defining layer, a step of d0 and a taper angle of $\theta 1$ with respect to the substrate surface, and a linear slope of $\tan\theta 1$. The taper reducing layer 43 has a thickness of d2 on the lower layer 41 and d3 on the opening 42, a taper angle of $\theta 2$, and a linear slope of $\tan \theta 2$ with respect to the substrate surface. In addition, the minimum thickness of the taper reducing layer required to planarize the substrate surface, *i.e.,* the minimum thickness of the taper reducing layer 43 required to have its taper angle $\theta 2$ of zero degree with respect to the substrate surface, is d1.

[0033] Thus, the taper angle planarized by the taper reducing layer 43 becomes $\theta 2$, which is the taper angle of the taper reducing layer 43 in the opening 42. The taper angle before it is planarized is $\theta 1$, which is the taper angle of the lower layer 41 in the opening 42. When a straight line having a slope of $\tan \theta 1$, formed by the taper angle $\theta 1$ of the lower layer 41, is assumed to be L1 and a straight line having a slope of $\tan \theta 2$, formed by the taper angle $\theta 2$ of the taper

reducing layer 43, is assumed to be L2, where L1 and L2 may be expressed as the equation 1 below. In this case, a point where the substrate surface and the straight line L1 meet, *i.e.,* an edge portion of the opening 42, is an origin O, where a longitudinal direction of the substrate is an x axis, and a height direction of the substrate is a y axis.

$$L1 : y1 = \tan \Theta 1x$$

$$L2 : y2 = \tan \Theta 2 \ x + \ d3 \ \text{---------- (1)}$$

[0034] The straight line L1 passes the d0 at the position x0 of the x axis direction, and the straight line L2 passes the d0 + d2 at a position x0 of the x axis direction. In addition, the lines L1 and L2 pass d1 at the position x1 of the x axis direction.

[0035] Thus, when functions y1 and y2 are substituted with values of the x and y axis directions in the equation 1, the result is as follows.

$$L1 : d0 = \tan \Theta 1x0$$

$$L2 : d0 + d2 = \tan \Theta 2x0 + d3$$

[0036] Thus, d0 + d2 may be expressed as the equation 2 below.

$$d0 + d2 = (\tan \Theta 2/\tan \Theta 1)d0 + d3 \text{ ----------(2)}$$

[0037] In addition,

$$L1 : d1 = \tan \Theta 1x1$$

$$L2 : d1 = \tan \Theta 2x1 + d3$$

[0038] Therefore, d1 may be expressed as the equation 3 below.

$$d1 = (\tan \Theta 2/\tan \Theta 1)d1 + d3 \text{ ----------(3)}$$

[0039] From the equations 2 and 3, a relationship equation with respect to the taper angle θ2 of the taper reducing layer 43 is obtained from the equation 4 below. Thickness d2 and thickness d3 of the taper reducing layer 43 to be deposited on the lower layer 41 and the opening 42, respectively, are obtained from equations 5 and 6 below. The thickness d2 of a portion of the taper reducing layer 43 formed on the lower layer 41 may linearly increase until the thickness d1 - d0, that is, the thickness when the substrate surface is planarized from the surface of the lower layer 41. The thickness d3 of a portion where the taper reducing layer 43 is formed in the opening 42 may linearly increase until the thickness d1, namely, the thickness when the substrate surface is planarized from the surface of the opening 42. The minimum thickness d1 required to planarize the substrate surface may vary in accordance with the planarizing capability of the organic layer used for the taper reducing layer, and may be varied and experimentally obtained in accordance with viscosity and volatility of a solution, variables of a coating process, and the like.

$$\tan \Theta 2 = (1 - d2/(d1 - d0))\tan \Theta 1 \text{ ----------(4)}$$

$$d2 = (d1 - d0)(1 - \tan \Theta 2/\tan \Theta 1) = (d1 - d0)(1 - \alpha) \text{ ------(5)}$$

$$d3 = d1(1 - \tan \Theta 2/\tan \Theta 1) = d1(1 - \alpha) \text{ ----------(6)}$$

[0040] In the above equations, α is a rate of a planarizing degree for the substrate surface when the taper reducing layer is formed on the substrate with respect to the planarizing degree of the substrate surface when the lower layer by itself is formed on the substrate. The value is defined as a relative flatness, and is expressed as $\alpha = \tan\theta 2/\tan\theta 1$.

[0041] For example, the lower layer 41 is an insulating layer having a via hole as the opening 42 and has a thickness of 600nm and a taper angle $\theta 1$ of 75° in the via hole. When the minimum thickness d1 is experimentally assumed to be 800nm to entirely planarize the via hole, the angle $\theta 2$ with which the substrate surface is planarized by the taper reducing layer 43 and the thickness d3 of the taper reducing layer 43 in the via hole are calculated as described below from the equations 4 and 6 above, to have the taper reducing layer 43 with 100nm in thickness to be deposited on the lower layer 41.

$$\tan\Theta 2 = (1 - \ 100/200)\tan 75 \ = 0.5 * 3.73 = 1.87$$

[0042] The taper angle $\theta 2$ of the taper reducing layer 43 in the via hole is as follows.
$\theta 2 = \tan^{-1}(1.87) = 62°$.

[0043] In addition, the thickness d3 of the taper reducing layer 43 in the via hole is as follows.

$$d3 = d1(1 - \tan\Theta 2/\tan\Theta 1) = d1 * d2/(d1 - d0) = \ 800 * 100/200 = 400$$

[0044] Thus, when the taper angle of the via hole is 75°and the thickness of the taper reducing layer 43 formed on the lower layer 41 is 100nm, the thickness d3 of the taper reducing layer 43 formed in the via hole becomes 400nm.

[0045] In the meantime, when the taper reducing layer 43 is deposited to have the angle planarized by the taper reducing layer 43, namely, the taper angle $\theta 2$ of the taper reducing layer 43 in the via hole to be below 40°or less, the thickness d2 of the taper reducing layer formed on the lower layer 41 and the thickness d3 of the taper reducing layer formed in the via hole are obtained as follows from the equations 5 and 6.

$$d2 = \ 200 \ (1 - \tan 40/\tan 75) = \ 200 \ (1 - 0.23) = \ 154$$

$$d3 = \ 800 \ (1 - \tan 40/\tan 75) = 800 \ (1 - 0.23) = \ 616$$

[0046] In other words, when the taper reducing layer 43 in the via hole is formed to have the taper angle $\theta 2$ of 40°, it may be arithmetically seen that the taper reducing layer 43 is formed with 154nm on the lower layer 41 and with 616nm in the via hole.

[0047] FIG. 5A shows the number of defects in accordance with the taper angle of the via hole or contact hole. Referring to FIG. 5A, the smaller the taper angle of the via hole or the contact hole becomes, the fewer defects in the element. It may be seen that when the taper angle of the contact hole or via hole is 60° or less, an initial defect becomes significantly reduced, thereby enabling fabrication of a more reliable element. In this case, the initial defect may include a defect such as a dark pixel that occurred before driving the OLED. When the taper angle of the via hole or contact hole is 60°, the thickness d2 of a portion where the taper reducing layer 43 is formed on the lower layer 41 becomes 100nm and the thickness d3 of a portion where the taper reducing layer 43 is formed in the opening becomes 400nm, from the equations 5 and 6.

[0048] FIG. 5B shows a relationship between the taper angle $\theta 2$ and the thickness d3 of the taper reducing layer formed in the opening when the lower layer 41 formed on the substrate has a predetermined taper angle $\theta 1$ and a step d1. Referring to FIG. 5B, when the 600nm thick lower layer 41 has a taper angle of 75°and the taper reducing layer 43 is formed with a thickness d1 of at least 800nm to planarize the substrate surface, the taper angle $\theta 2$ of the opening should be 40°or less when a pixel defining layer exists, and the taper angle $\theta 2$ of the contact hole or via hole should be 60°or less when a pixel defining layer does not exist, in order to fabricate a reliable element.

[0049] To reduce the taper angle of the taper reducing layer as an organic layer having a planarizing characteristic, as well as to prevent light emitting characteristic from deteriorating in accordance with usage of the taper reducing layer, a high increase in driving voltage should be avoided when the taper reducing layer 43 is formed with a thickness d2 of about 100nm to about 200nm on the lower layer 41.

[0050] Thus, the taper reducing layer used in an exemplary embodiment of the present invention preferably has a planarizing characteristic, a charge transporting capability for transporting a hole or an electron, and a proper HOMO (highest occupied molecular orbital) and LUMO (lowest unfilled molecular orbital), so that it does not increase the driving voltage of the element due to an increased deposition thickness of the taper reducing layer.

[0051] In the case of a typical bottom-emitting or top-emitting OLED, where the taper reducing layer is formed below

the emission layer and over the anode electrode, an organic layer having a hole transporting capability may be used, with an HOMO of 4.5eV or more, and charge mobility of 10^{-8} cm^2/Vs or more for the taper reducing layer. In the case of an inverted-type OLED, where the taper reducing layer is formed over the cathode electrode and below the emission layer, an organic layer having an electron transporting capability may be used, with an LUMO of 3.5eV or less, and charge mobility of 10^{-8} cm^2/Vs or more for the taper reducing layer.

[0052] Referring to FIG. 4, the taper reducing layer is employed to an insulating layer having an opening to reduce a taper angle. However, the taper angle may be reduced by the taper reducing layer even in a stepped portion of the deposition layer, so that element defects may be prevented.

[0053] FIG. 6A shows a cross-sectional view of a bottom-emitting OLED having a taper reducing layer in accordance with an embodiment of the present invention. Referring to FIG. 6A, a buffer layer 405 is formed on an insulating substrate 400, and a semiconductor layer 410, having source and drain regions 411 and 415, is formed on the buffer layer 405. A gate 425 is formed on a gate insulating layer 420, and source and drain electrodes 441 and 445 are connected to the source and drain regions 411 and 415 through contact holes 431 and 435 on an inter-layer insulating layer 430. Wiring 447, such as a data line or a power supply line, is formed at the same time the source and drain electrodes 441 and 445 are formed on the inter-layer insulating layer 430. The contact holes 431 and 435 have a taper angle of 75°and a depth of 500nm.

[0054] An anode electrode 470, as a lower electrode connected to one of the source and drain electrodes 441 and 445, for example, to the drain electrode 445 through the via hole 455, is formed on a passivation layer 450. The via hole 455 may have a taper angle of 85°and a depth of 500nm, and the anode electrode 470 may have a thickness of 100nm. After forming the anode electrode 470, a cleaning process is performed. A taper reducing layer 480, an organic film layer 485 and a cathode electrode 490 may be sequentially formed on the substrate.

[0055] FIG. 6B illustrates a cross-sectional view of an emission region of an R pixel in an OLED in accordance with an embodiment of the present invention. Referring to FIG. 6B, the taper reducing layer 480 is formed on the anode electrode 470, and an emission layer 485c is formed on the taper reducing layer 480.

[0056] By way of an exemplary embodiment, a polymer organic layer having a hole transporting capability, such as, for example, PEDOT is formed with a thickness of 100nm on the anode electrode 470 by a spin coating method, and an annealing process is performed by using a hot plate for 5 minutes at 20nm, thereby forming the taper reducing layer 480. In this case, the deposition thickness of the taper reducing layer 480 is determined by its taper angle, the depths and taper angles of the contact hole and via hole below the taper reducing layer, the thickness of the pixel electrode and a taper angle at an edge of the pixel electrode.

[0057] Using a vacuum deposition method, a 60nm thick CuPc, as the hole injecting layer 485a, and a 30nm thick NPB, as the hole transporting layer 485b, are sequentially formed on the taper reducing layer 480. A 20nm thick Alq+DCM, as the red color emission layer 485c, is deposited on the hole transporting layer 485b, and a 20nm thick Alq_3, as the electron transporting layer 485d, is formed on the red emission layer 485c, thereby forming the organic film layer 485. In the present embodiment, a hole blocking layer between the red color emission layer 485c and the electron transporting layer 485d, and an electron injecting layer on the electron transporting layer 485d may be formed. Finally, LiF/Al, as the cathode electrode 490, is deposited by a thermal evaporation method.

[0058] After forming the organic film layer 485 and the cathode electrode 490, as shown in FIG. 6B, a sealant (not shown in the figures) is applied on the insulating substrate 400 to prevent external oxygen and moisture from being introduced inside. An encapsulating substrate is bonded thereon, thereby fabricating the OLED.

[0059] FIG. 6C illustrates another cross-sectional view of the emission region of the R pixel in the OLED in accordance with an embodiment of the present invention. Referring to FIG. 6C, the taper reducing layer 480 is formed between the emission layer 485c and the hole transporting layer 485b of the organic film layer 485.

[0060] The anode electrode 470 is formed on the insulating layer 400, and the hole injecting layer 485a and the hole transporting layer 485b of the organic film layer 485 are sequentially formed on the anode electrode 470. The taper reducing layer 480 is formed on the hole transporting layer 485b, the R emission layer 485c and the electron transporting layer 485d, as the organic emission layer 485 are sequentially formed on the taper reducing layer 480. The cathode electrode 490 is formed on the electron transporting layer 485d.

[0061] The taper reducing layer 480 may be formed just on the anode electrode 470 and below the emission layer 485c, as shown in FIGs. 6B and 6C, and at the same time, may be formed only between the anode electrode 470 and the emission layer 485c of the organic film layer 485. The organic film layer 485 has at least one of a hole injecting layer, a hole transporting layer, an emission layer, a hole blocking layer, an electron transporting layer and/or an electron injecting layer.

[0062] In the first exemplary embodiment, according to the invention, the contact hole and via hole have taper angles (θ41, θ42) of 75°and 85°, respectively, before forming the taper reducing layer 480. The taper angle is reduced with respect to the substrate surface after the taper reducing layer 480 is formed, so that the taper angles (θ43, θ44) of the contact hole and via hole are 60°or less. The anode electrode has an edge taper angle θ47 and the taper reducing layer 480 may reduce the edge taper angle θ45 to 40°. In addition, the taper angle θ46 may be reduced near the contact hole,

and via hole and near the wiring 447 in accordance with formation of the taper reducing layer.

[0063] The deposition thickness of the taper reducing layer 480 is determined by the taper angle of the taper reducing layer, the depths and taper angles of the contact hole and via hole below the taper reducing layer, the thickness of the pixel electrode and the taper angle at an edge of the pixel electrode. When the taper reducing layer is deposited to have the taper angles of the contact hole or via hole of 60°or less, from FIG. 4 and equations 4 to 6, the deposition thickness of the taper reducing layer is determined by the taper angle of the contact hole and the thickness of the insulating layer, such as the inter-layer insulating layer and the gate insulating layer where the contact hole is formed, and further determined by the taper angle of the via hole and the thickness of the insulating layer, such as the passivation layer where the via hole is formed. In the meantime, when the taper reducing layer is deposited to have the taper angle at an edge of the pixel electrode of 40°or less, the deposition thickness of the taper reducing layer is determined by the taper angle at an edge of the pixel electrode and the thickness of the pixel electrode, from FIG. 4a and equations 4 to 6.

[0064] FIG. 7A illustrates a SEM picture near the via hole in the OLED in accordance with the first exemplary embodiment of the present invention. Referring to FIG. 7A, a portion with a thickness d73 where the taper reducing layer is formed on the anode electrode within the via hole is deposited thicker than a portion with a thickness d72 where the taper reducing layer is formed on the anode electrode over an insulating layer having a stepped portion, so that the taper angle in the via hole is reduced to 50°. FIG. 7B illustrates a microscope picture for representing whether edge defects occur in the emission region when the OLED of the first exemplary embodiment is driven. Referring to FIG. 7B, when the substrate surface is planarized by the taper reducing layer, so that the taper angle is reduced at an edge of the pixel, defects may be reduced or eliminated at an edge of the emission region. FIG. 7C illustrates a microscope picture for representing whether the edge defects occur at an edge of the emission region when the OLED having the same structure as shown in Figs. 1A and 1B is driven. Referring to FIG. 7C, it may be seen that dark spots may occur at an edge of the emission region when the taper reducing layer is not used. In this case, a numerical reference 71 indicates the dark spot near the via hole, and 72 indicates the dark spot near the contact hole.

[0065] FIG. 8 illustrates a cross-sectional view of a bottom-emitting OLED in accordance with an exemplary embodiment which is not part of the present invention. Referring to FIG. 8, a buffer layer 505 is formed on an insulating substrate 500, and a semiconductor layer 510 having source and drain regions 511 and 515 is formed on the buffer layer 505. A gate 525 is formed on a gate insulating layer 520, and source and drain electrodes 541 and 545 are formed on an inter-layer insulating layer 530 through contact holes 531 and 535. In this case, a data line 547 is formed at the same time when the source and drain electrodes 541 and 545 are formed on the inter-layer insulating layer 530.

[0066] An anode electrode 570 as a lower electrode connected to one of the source and drain electrodes 541 and 545, such as, for example, to the drain electrode 545 through the via hole 555, is formed on the passivation layer 550. After depositing a 500nm thick pixel defining layer 565 over the entire substrate, this pixel defining layer is etched to have a taper angle $\theta 51$ of 60°to form an opening 575. After forming the pixel defining layer 565, an organic layer, such as PEDOT, coated by a wet coating method and having a hole transporting capability, is deposited on the substrate, so that a taper reducing layer 580 is formed. In this case, the taper reducing layer 580 may have a taper angle $\theta 51$ of the opening 575 of 40°or less, and the deposition thickness of the taper reducing layer 580 is determined by the taper angle of the taper reducing layer 580, thickness of the pixel defining layer 585 and the taper angle of the opening 575.

[0067] After depositing the organic film layer 585 on the taper reducing layer 580, such as in the first embodiment of FIG. 6A, and depositing LiF/Al for the cathode electrode 590 on the organic film layer 585 by the thermal evaporation method, an encapsulating substrate (not shown) is then bonded to fabricate the OLED in accordance with this exemplary embodiment not forming part of the present invention.

[0068] FIG. 9A illustrates a SEM picture near an emission region of an OLED in accordance with the exemplary embodiment shown in figure 8. Referring to FIG. 9A, it may be seen that the taper angle at an edge of the opening is reduced to 40° as the taper reducing layer is formed. FIG. 9B illustrates a microscope picture of an edge of the emission region when the OLED employing the taper reducing layer in accordance with the exemplary embodiment, shown in figure 8, is driven. Referring to FIG. 9B, it may be seen that defects, such as a dark spot at an edge of the emission region, may be reduced or eliminated by forming the taper reducing layer on the pixel defining layer. FIG. 9C illustrates a microscope picture at an edge of the emission region when the OLED, having the pixel defining layer and employing a conventional taper reducing layer, is driven. Referring to FIG. 9C, it may be seen that dark spots occur if the taper angle at an edge of the opening is large even when the pixel defining layer is used.

[0069] FIG. 10 illustrates a cross-sectional view of a top-emitting OLED in accordance with another exemplary embodiment which is not part of the present invention. Referring to FIG. 10, a buffer layer 605 is formed on an insulating layer 600, and a semiconductor layer 610 having source and drain regions 611 and 615 is formed on the buffer layer 605. A gate 625 is formed on a gate insulating layer 620, and source and drain electrodes 641 and 645 are formed on an inter-layer insulating layer 630 through contact holes 631 and 635. In this case, wiring 647, such as a data line or a power supply line, is formed when the source and drain electrodes 641 and 645 are formed on the inter-layer insulating layer 630.

[0070] A planarization layer 660 is formed on a passivation layer 650, and an anode electrode 670 as a lower electrode

connected to one of the source and drain electrodes 641 and 645, such as, for example, to the drain electrode 645 through the via hole 655, is formed on the planarization layer 660. PEDOT as an organic layer that may be coated by a wet coating method and has a hole transporting capability is deposited on the substrate, may be used so that the taper reducing layer 680 is formed. In this case, the taper reducing layer 680 may have the taper angle of the via hole of 60°or less, and the deposition thickness of the taper reducing layer 680 is determined by the taper angle of the taper reducing layer, thickness of the planarization layer 660 and the taper angle of the via hole.

[0071] After forming an organic film layer 685 and a cathode electrode 690 as an upper electrode on the taper reducing layer 680, such as in the first exemplary embodiment, an encapsulating substrate (not shown in the figure) is then used to fabricate the OLED in accordance with this exemplary embodiment, not forming part of the invention.

[0072] FIG. 11 illustrates a cross-sectional view of a top-emitting OLED in accordance with a further exemplary embodiment which is not part of the invention. Referring to FIG. 11, a buffer layer 705 is formed on an insulating substrate 700, and a semiconductor layer 710 having source and drain regions 711 and 715 is formed on the buffer layer 705. A gate 725 is formed on a gate insulating layer 720, and source and drain electrodes 741 and 745 are formed on an inter-layer insulating layer 730 through contact holes 731 and 735. In this case, wiring 747 such as a data line or a power supply line, is formed when the source and drain electrodes 741 and 745 are formed on the inter-layer insulating layer 730.

[0073] A planarization layer 760 is formed on a passivation layer 750, and an anode electrode 770 as a lower electrode connected to one of the source and drain electrodes 741 and 745, such as, for example, to the drain electrode 745 through the via hole 755, is formed on the planarization layer 760. A pixel defining layer 765, having an opening 775 for exposing a portion of the anode electrode 770, is then formed. PEDOT, as an organic layer that may be coated by a wet coating method and has a hole transporting capability, may be deposited on the substrate, so that the taper reducing layer 780 is formed. In this case, taper reducing layer 780 may have the taper angle of the opening 775 of 40°or less, and the deposition thickness of the taper reducing layer 780 is determined by the taper angle of the taper reducing layer, the thickness of the pixel defining layer and the taper angle of the pixel defining layer. After forming a cathode electrode 790 for an upper electrode and an organic film layer 785 on the taper reducing layer 780, such as in the first exemplary embodiment, an encapsulating substrate (not shown in the figure) is used to fabricate the OLED in accordance with this exemplary embodiment not forming part of the invention.

[0074] FIG. 12 illustrates a cross-sectional view of a bottom-emitting OLED in accordance with yet another exemplary embodiment which is not part of the present invention. Referring to FIG. 12, a buffer layer 805 is formed on an insulating substrate 800, and a semiconductor layer 810 having source and drain regions 811 and 815 is formed on the buffer layer 805. A gate 825 is formed on a gate insulating layer 820, and source and drain electrodes 841 and 845 are formed through contact holes 831 and 835 on an inter-layer insulating layer 830. In this case, an anode electrode 870 is formed to be connected to one of the source and drain electrodes 841 and 845, such as, for example, to the drain electrode 845 on the inter-layer insulating layer 830.

[0075] A passivation layer 850 having an opening 855 for exposing a portion of the anode electrode 870 is formed on the substrate. A taper reducing layer 880 formed of a conductive organic layer that may be coated by a wet coating method, such as, for example, PEDOT, is formed on the opening 855 and the passivation layer 850. The taper reducing layer 880 may have a taper angle in the opening of 40°or less, and the thickness of the taper reducing layer 880 is determined by the taper angle of the taper reducing layer 880, the thickness of the passivation layer 850 and the taper angle of the opening. After forming a cathode electrode 890 for an upper electrode and an organic film layer 885 on the taper reducing layer 880, such as in the first exemplary embodiment, an encapsulating substrate (not shown in the figure) is bonded to fabricate the OLED in accordance with this embodiment not forming part of the invention.

[0076] In the embodiment of the present invention, the organic film layer has the hole injecting layer, the hole transporting layer, the R, G, or B organic emission layer and the electron transporting layer. However, it may have at least one of the hole injecting layer, the hole transporting layer, the R, G, or B organic emission layer, the hole blocking layer, the electron transporting layer and/or the electron injecting layer.

[0077] In the embodiment of the present invention, top and bottom-emitting OLEDs, where the organic emission layer is deposited on the anode electrode, use the organic layer having a hole transporting capability for the taper reducing layer. However, it is also possible to use the organic layer having the electron transporting capability for the taper reducing layer in the inverted-type OLED, where the organic emission layer is deposited on the cathode electrode.

[0078] In addition, the taper reducing layer is shown to be formed between the anode electrode and the organic emission layer in the embodiment of the present invention. However, it is possible to form the taper reducing layer on any layer existing between the emission layer of the organic film layer and the anode electrode in the top and bottom-emitting OLEDs. It is also possible to form it on any layer existing between the emission layer of the organic film layer and the cathode electrode in the inverted-type OLED.

[0079] In addition, the method for reducing the taper angle of the substrate surface by using the taper reducing layer of the present invention may use various methods, such as, for example, but not limited to, a deposition method, an inkjet method and a laser-induced thermal imaging for forming the organic emission layer.

[0080] As mentioned above, by forming the organic film layer capable of reducing the taper angle between the organic

emission layer and the lower electrode in accordance with the embodiment of the present invention, defects near the contact hole and via hole and at a stepped portion of the lower electrode and defects of the organic emission layer may be prevented, and reliability and the yield may also be improved.

Claims

1. A flat panel display, comprising:

an insulating substrate (400);
a thin film transistor formed on the insulating substrate (400), the thin film transistor including a semiconductor layer (410) having source and drain regions (411, 415), a first insulating layer (430) having contact holes (431, 435) for exposing a portion of the source and drain regions (411, 415) and source and drain electrodes (441, 445) connected to the source and drain regions (411, 415) through the contact holes (431, 435);
a second insulating layer (450) formed on the insulating substrate (400) and having a via hole (455) for exposing one of the source and drain electrodes (441, 445);
an electroluminesence element formed on the second insulating layer (450) and connected to one electrode of the thin film transistor through the via hole (455), and having a lower electrode (470), an organic film layer (485) comprising at least an organic emission layer (485c), and an upper electrode (490); and
a taper reducing layer (480) formed on the lower electrode (470), on the second insulating layer (450) and on the source and drain electrodes (441, 445),
wherein the taper reducing layer (480) is a conductive organic layer having a charge transporting capability, and wherein the edge of the lower electrode (470) is covered by the taper reducing layer (480),
characterized in that
the taper reducing layer (480) is formed between the lower electrode (470) and the organic emission layer (485c), and
a taper angle of the taper reducing layer (480) in a position corresponding to the contact hole in which the other one of the source and drain electrodes (441, 445) which is not connected with the electroluminesence element is formed has a first taper angle (θ43) smaller than a taper angle of the corresponding contact hole, a taper angle of the taper reducing layer (480) in a position corresponding to the via hole (θ44) has a second taper angle smaller than a taper angle of the via hole, and a taper angle of the taper reducing layer (480) at an edge of the lower electrode (470) has a third taper angle (θ45) smaller than a taper angle of the edge of the lower electrode (470),
wherein the taper angle of the contact hole in which the other one of the source and drain electrodes (441, 445) which is not connected with the electroluminesence element is formed, the taper angle of the via hole and the taper angle at an edge of the lower electrode are planarized by the taper reducing layer (480), and wherein the first, second, and third taper angles (θ43, θ44, θ45) are greater than zero degrees.

2. The flat panel display of claim 1, wherein the organic film layer (485) further includes at least one selected from a group consisting of a hole injecting layer, a hole transporting layer, a hole blocking layer, an electron transporting layer and an electron injecting layer.

3. The flat panel display of one of claims 1 and 2, wherein the taper reducing layer (480) consists of at least one selected from the group consisting of a small-molecule organic layer selected from carbazole-based, arylamine-based, hydrazone-based, stilbene-based, oxadiazole-based and starburst-based derivatives, and a polymer organic layer selected from PEDOT, PANI, carbazole-based, arylamine-based, perylene-based, pyrrole-based and oxadiazole-based derivatives.

4. The flat panel display of claim 1, wherein the first, second, and third taper angles (θ43, θ44, θ45) are 60°or less, 60°or less and 40°or less, respectively.

5. The flat panel display of claim 1, wherein the lower electrode (470) is a transparent electrode, the upper electrode (490) is a reflective electrode, and light emitted from the emission layer (485) is directed toward the insulating substrate (400),
and the taper reducing layer (480) has a hole transporting capability, a highest occupied molecular orbital of at least 4.5eV and a charge mobility of at least 10^{-8} cm^2/Vs when the lower electrode (470) is an anode electrode, and has an electron transporting capability, a lowest unoccupied molecular orbital of at least 3.5eV and a charge mobility of at least 10^{-8} cm^2/Vswhen the lower electrode (470) is a cathode electrode.

Patentansprüche

1. Eine flache Anzeigetafel, aufweisend:

ein Isoliersubstrat (400);
einen Dünnfilmtransistor, der auf dem Isoliersubstrat (400) ausgebildet ist, wobei der Dünnfilmtransistor eine Halbleiterschicht (410), die Source- und Drain-Bereiche (411, 415) aufweist, eine erste Isolierschicht (430), die Kontaktlöcher (431, 435) zum Freilegen eines Abschnitts der Source- und Drain-Bereiche (411, 415) aufweist, und Source- und Drain-Elektroden (441, 445), die durch die Kontaktlöcher (431, 435) mit den Source- und Drain-Bereichen (411, 415) verbunden sind, aufweist;
eine zweite Isolierschicht (450), die auf dem Isoliersubstrat (400) ausgebildet ist und ein Durchgangsloch (455) zum Freilegen einer der Source- und Drain-Elektrode (441, 445) aufweist;
ein Elektrolumineszenz-Element, das auf der zweiten Isolierschicht (450) ausgebildet ist und durch das Durchgangsloch (455) mit einer Elektrode des Dünnfilmtransistors verbunden ist und eine untere Elektrode (470), eine organische Filmschicht (485), die zumindest eine organische Emissionsschicht (485c) aufweist, und eine obere Elektrode (490) aufweist; und
eine Konizitätsverringerungsschicht (480), die auf der unteren Elektrode (470), auf der zweiten Isolierschicht (450) und auf der Source- und Drain-Elektrode (441, 445) ausgebildet ist,
wobei die Konizitätsverringerungsschicht (480) eine leitende organische Schicht, die eine Ladungstransportfähigkeit aufweist, ist, und wobei der Rand der unteren Elektrode (470) von der Konizitätsverringerungsschicht (480) bedeckt wird,
dadurch gekennzeichnet, dass
die Konizitätsverringerungsschicht (480) zwischen der unteren Elektrode (470) und der organischen Emissionsschicht (485c) ausgebildet ist, und
ein Kegelwinkel der Konizitätsverringerungsschicht (480) in einer Position entsprechend dem Kontaktloch, in dem die andere der Source- und Drain-Elektrode (441, 445), die nicht mit dem Elektrolumineszenz-Element verbunden ist, ausgebildet ist, einen ersten Kegelwinkel (θ43), der kleiner ist als ein Kegelwinkel des entsprechenden Kontaktlochs, aufweist, ein Kegelwinkel der Konizitätsverringerungsschicht (480) in einer Position entsprechend dem Durchgangsloch (θ44) einen zweiten Kegelwinkel, der kleiner ist als ein Kegelwinkel des Durchgangsloch, aufweist, und ein Kegelwinkel der Konizitätsverringerungsschicht (480) an einem Rand der unteren Elektrode (470) einen dritten Kegelwinkel (θ45), der kleiner ist als ein Kegelwinkel des Randes der unteren Elektrode (470), aufweist,
wobei der Kegelwinkel des Kontaktlochs, in dem die andere der Source- und Drain-Elektrode (441, 445), die nicht mit dem Elektrolumineszenz-Element verbunden ist, ausgebildet ist, der Kegelwinkel des Durchgangslochs und der Kegelwinkel an einem Rand der unteren Elektrode durch die Konizitätsverringerungsschicht (480) planarisiert werden, und wobei der erste, zweite und dritte Kegelwinkel (θ43, θ44, θ45) größer als null Grad sind.

2. Die flache Anzeigetafel nach Anspruch 1, wobei die organische Filmschicht (485) ferner zumindest eine ausgewählt aus einer Gruppe bestehend aus einer Lochinjektionsschicht, einer Lochtransportschicht, einer Lochblockierschicht, einer Elektronentransportschicht und einer Elektroneninj ektionsschicht aufweist.

3. Die flache Anzeigetafel nach einem der Ansprüche 1 und 2, wobei die Konizitätsverringerungsschicht (480) aus zumindest einer ausgewählt aus der Gruppe bestehend aus einer organischen Kleinmolekülschicht ausgewählt aus Derivaten auf Carbazolbasis, auf Arylaminbasis, auf Hydrazonbasis, auf Stilbenbasis, auf Oxadiazolbasis und auf Starburstbasis, und aus einer organischen Polymerschicht ausgewählt aus Derivaten von PEDOT, PANI, auf Carbazolbasis, auf Arylaminbasis, auf Perylenbasis, auf Pyrrolbasis und auf Oxadiazolbasis besteht.

4. Die flache Anzeigetafel nach Anspruch 1, wobei der erste, zweite und dritte Kegelwinkel (θ43, θ44, θ45) jeweils 60° oder weniger, 60° oder weniger und 40° oder weniger betragen.

5. Die flache Anzeigetafel nach Anspruch 1, wobei die untere Elektrode (470) eine transparente Elektrode ist, die obere Elektrode (490) eine reflektierende Elektrode ist und Licht, das von der Emissionsschicht (485) emittiert wird, zum Isoliersubstrat (400) hin gelenkt wird,
und wobei die Konizitätsverringerungsschicht (480) eine Lochtransportfähigkeit, ein höchstes besetztes molekulares Orbital von zumindest 4,5 eV und eine Ladungsmobilität von zumindest 10^{-8} cm^2/Vsaufweist, wenn die untere Elektrode (470) eine Anodenelektrode ist, und eine Elektronentransportfähigkeit, ein niedrigstes unbesetztes molekulares Orbital von zumindest 3,5 eV und eine Ladungsmobilität von zumindest 10^{-8} cm^2/Vsaufweist, wenn die untere Elektrode (470) eine Kathodenelektrode ist.

Revendications

1. Un panneau d'affichage plat, comprenant :

un substrat isolant (400) ;
un transistor à film mince formé sur le substrat isolant (400), le transistor à film mince comprenant une couche semi-conductrice (410) ayant des régions source et drain (411, 415), une première couche isolante (430) ayant des trous de contact (431, 435) pour exposer une partie des régions source et drain (411, 415), et des électrodes source et drain (441, 445) reliées aux régions source et drain (411, 514) par les trous de contact (431, 435) ;
une deuxième couche isolante (450) formée sur le substrat isolant (400) et ayant un trou traversant (455) pour exposer l'une des électrodes source et drain (441,445) ;
un élément électroluminescent formé sur la deuxième couche isolante (450) et relié à une électrode du transistor à film mince par le trou traversant (455) et ayant une électrode inférieure (470), une couche de film organique (485) comprenant au moins une couche d'émission organique (485c), et une électrode supérieure (490) ; et
une couche de réduction de conicité (480) formée sur l'électrode inférieure (470), sur la deuxième couche isolante (450) et sur les électrodes source et drain (441,445),
la couche de réduction de conicité (480) étant une couche organique conductrice ayant une capacité de transport de charge, et le bord de l'électrode inférieure (470) étant couvert par la couche de réduction de conicité (480),
caractérisé en ce que
la couche de réduction de conicité (480) est formée entre l'électrode inférieure (470) et la couche d'émission organique (485c), et
un angle conique de la couche de réduction de conicité (480) se trouvant dans une position correspondant au trou de contact dans lequel est formée l'autre des électrodes source et drain (441, 445) qui n'est pas reliée à l'élément électroluminescent a un premier angle conique (θ43) inférieur à un angle conique du trou de contact correspondant, un angle conique de la couche de réduction de conicité (480) se trouvant dans une position correspondant au trou traversant (θ44) a un deuxième angle conique inférieur à un angle conique du trou traversant, et un angle conique de la couche de réduction de conicité (480) se trouvant à un bord de l'électrode inférieure (470) a un troisième angle conique (θ45) inférieur à un angle conique du bord de l'électrode inférieure (470),
l'angle conique du trou de contact dans lequel est formée l'autre des électrodes source et drain (441, 445) qui n'est pas reliée à l'élément électroluminescent, l'angle conique du trou traversant et l'angle conique se trouvant à un bord de l'électrode inférieure sont planarisés par la couche de réduction de conicité (480), et les premier, deuxième et troisième angles coniques (θ43, θ44, θ45) sont supérieurs à zéro degrés.

2. Le panneau d'affichage plat selon la revendication 1, dans lequel la couche de film organique (485) comprend en outre au moins une couche sélectionnée dans un groupe constitué d'une couche d'injection de trous, une couche de transport de trous, une couche de blocage de trous, une couche de transport d'électrons et une couche d'injection d'électrons.

3. Le panneau d'affichage plat selon l'une des revendications 1 et 2, dans lequel la couche de réduction de conicité (480) est au moins une couche sélectionnée dans le groupe constitué d'une couche organique à petites molécules sélectionnée parmi les dérivés à base de carbazole, à base d'arylamine, à base d'hydrazone, à base de stilbène, à base d'oxadiazole et à base de starburst, et une couche de polymère organique sélectionnée parmi les dérivés de PEDOT, PANI, à base de carbazole, à base d'arylamine, à base de pérylène, à base de pyrrole et à base d'oxadiazole.

4. Le panneau d'affichage plat selon la revendication 1, dans lequel les premier, deuxième et troisième angles coniques (θ43, θ44, θ45) sont respectivement de 60° ou moins, de 60° ou moins et de 40° ou moins.

5. Le panneau d'affichage plat selon la revendication 1, dans lequel l'électrode inférieure (470) est une électrode transparente, l'électrode supérieure (490) est une électrode réfléchissante, et de la lumière émise par la couche d'émission (485) est dirigée vers le substrat isolant (400),
et dans lequel la couche de réduction conique (480) a une capacité de transport de trous, une orbitale moléculaire occupée la plus élevée d'au moins 4,5 eV et une mobilité de charge d'au moins 10^{-8} cm^2/Vssi l'électrode inférieure (470) est une électrode d'anode, et a une capacité de transport d'électrons, une orbitale moléculaire inoccupée la plus basse d'au moins 3,5 eV et une mobilité de charge d'au moins 10^{-8} cm^2/Vssi l'électrode inférieure (470) est une électrode de cathode.

FIG. 1a

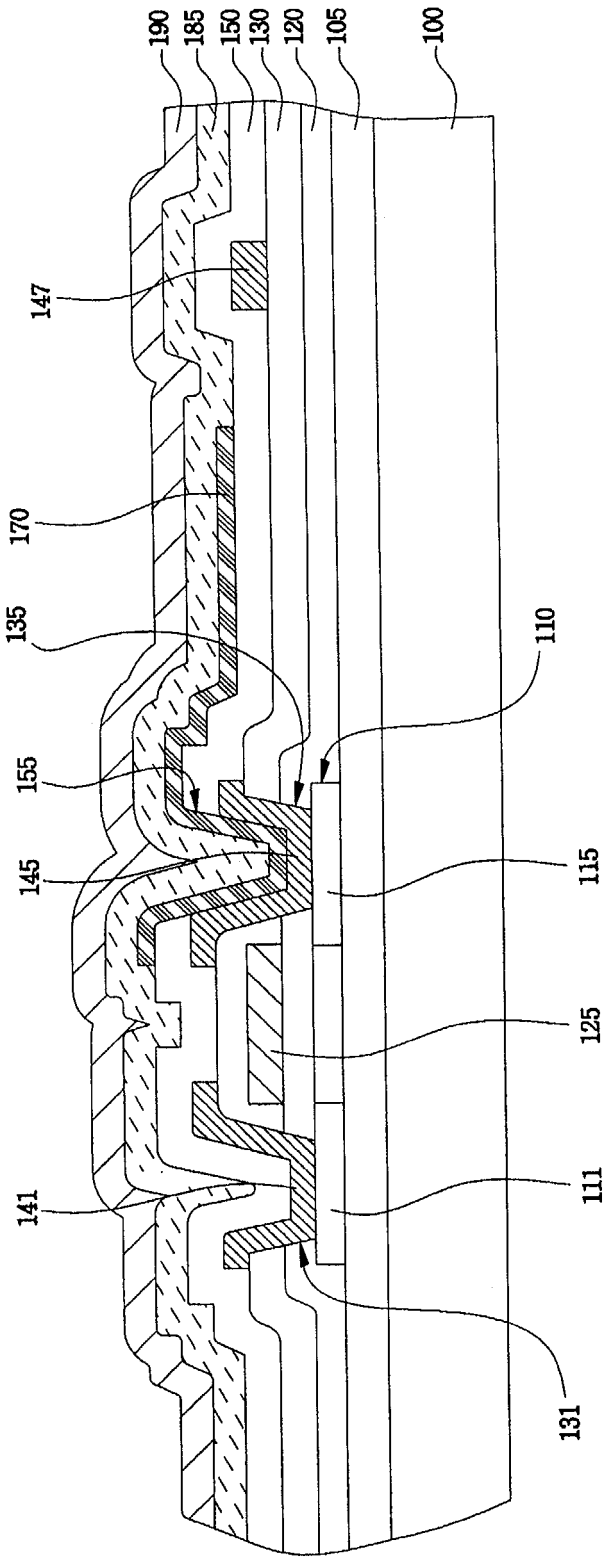
190
185
150
130
120
105
100
147
170
135
155
145
110
115
125
111
141
131

FIG. 1b

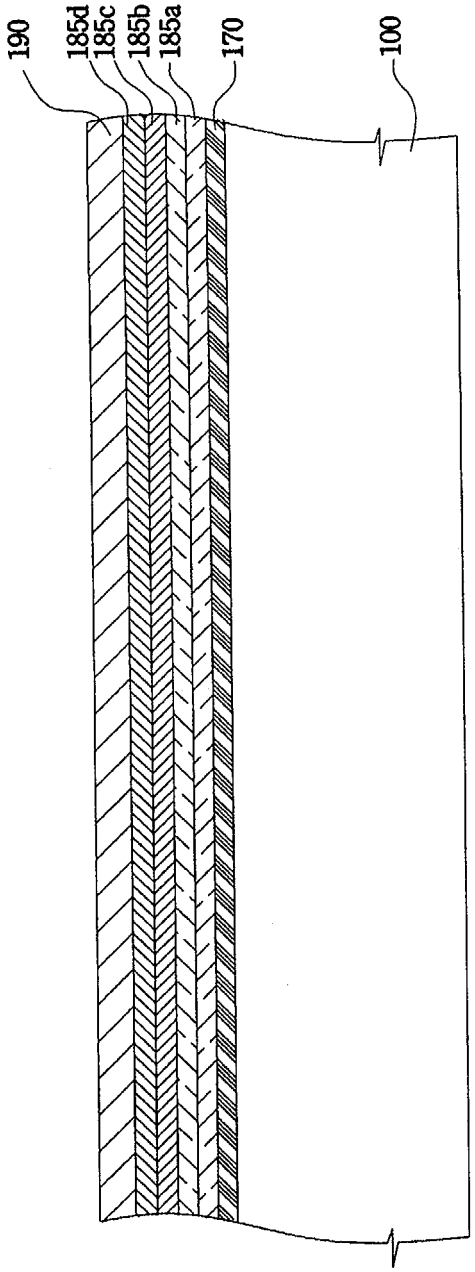

FIG. 2

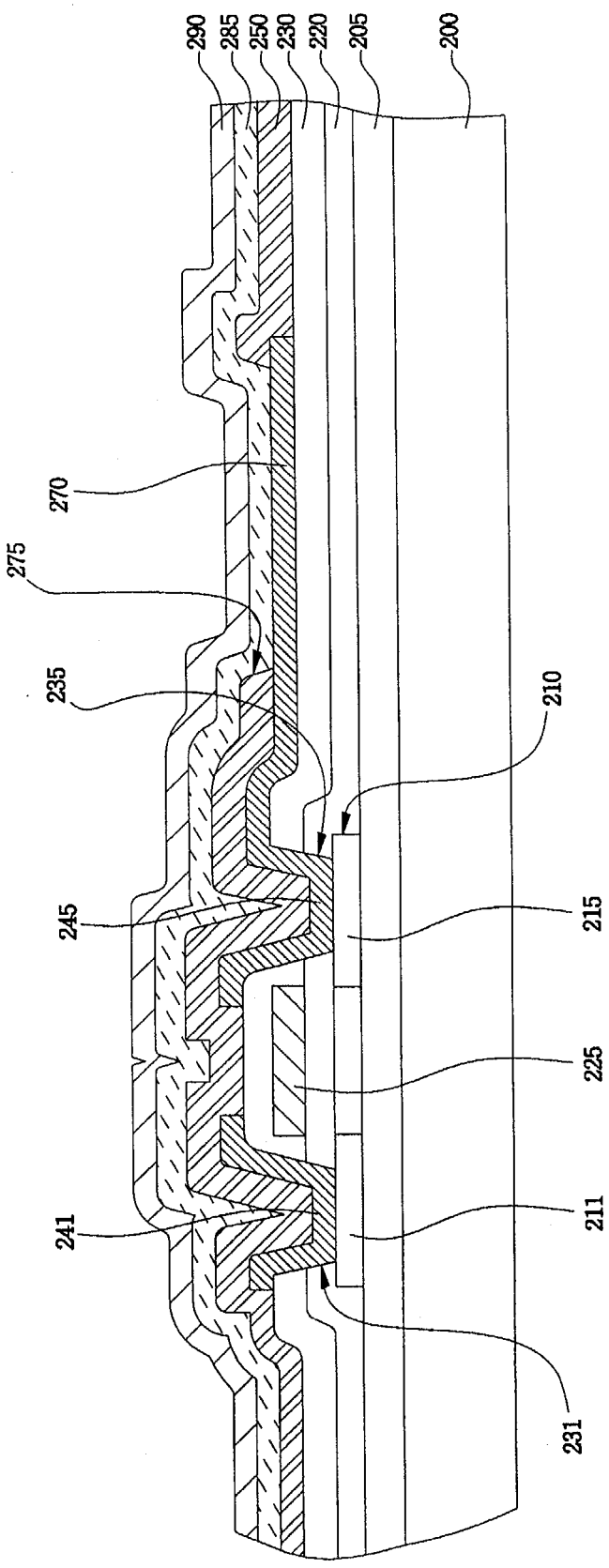
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FIG. 3

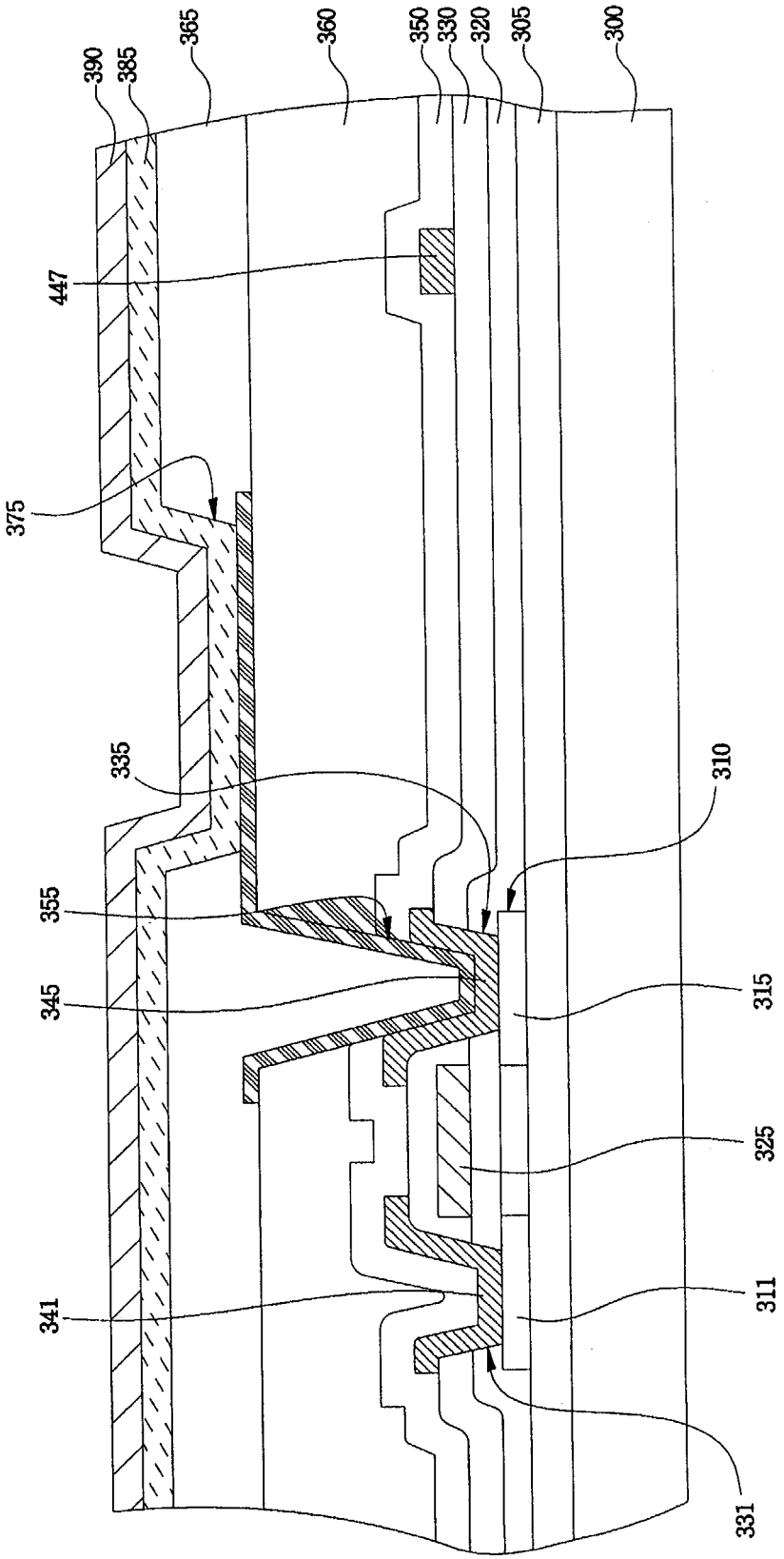
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FIG. 4

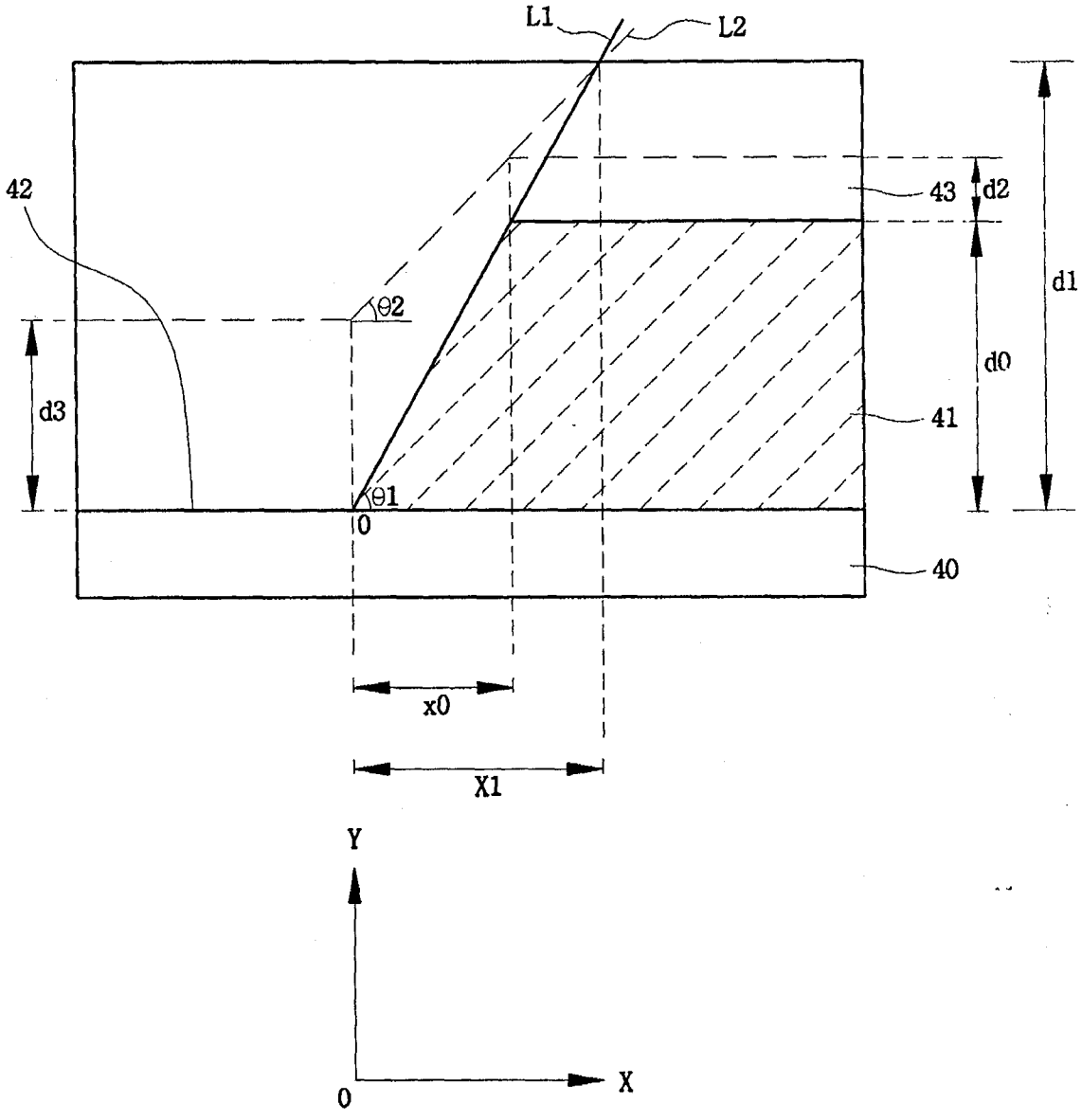


FIG. 5a

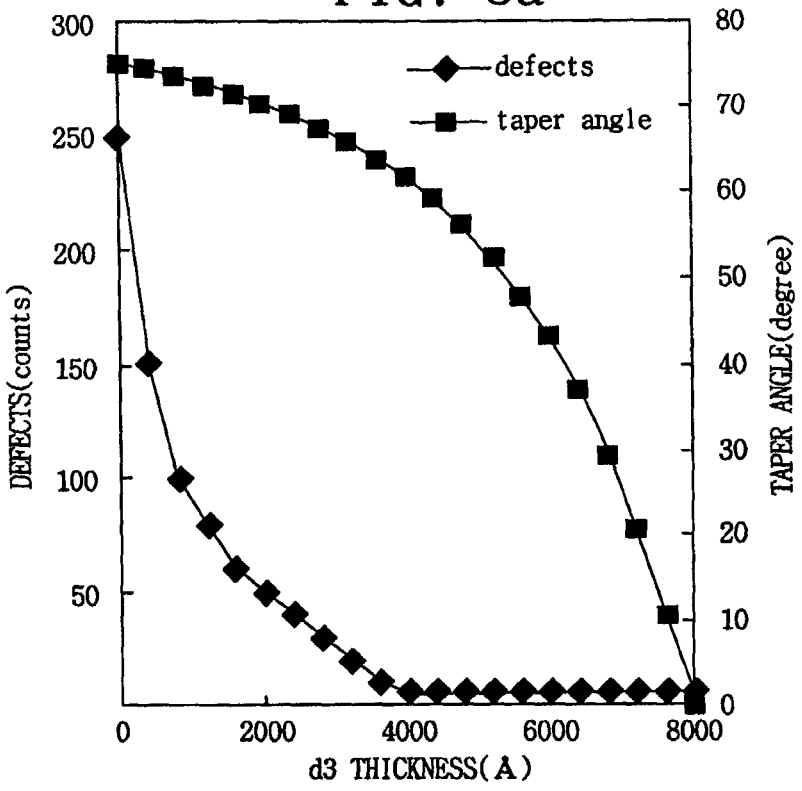
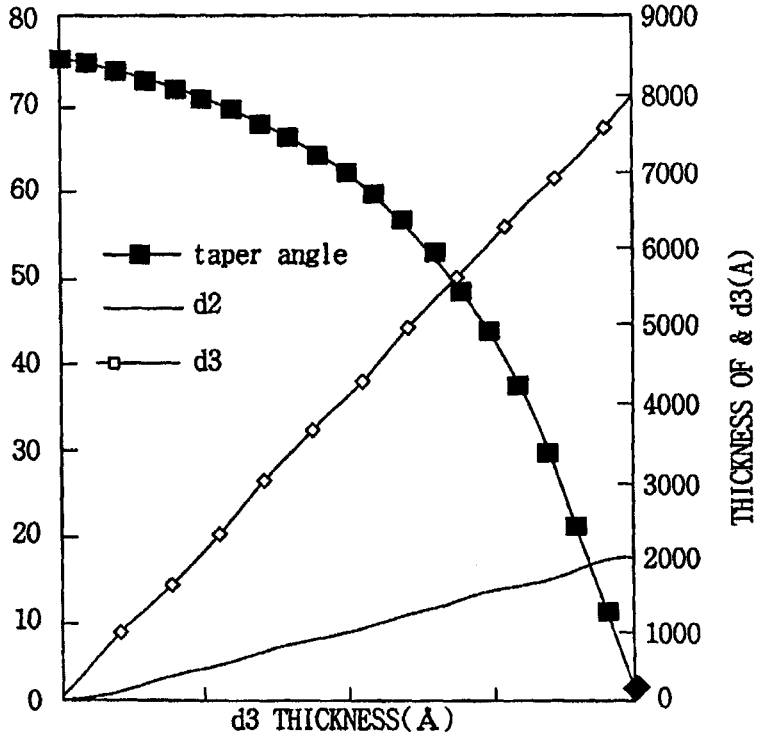

defects
taper angle
DEFECTS(counts)
TAPER ANGLE(degree)
d3 THICKNESS(A)
300
250
200
150
100
50
80
70
60
50
40
30
20
10
0
0
2000
4000
6000
8000

FIG. 5b


taper angle
d2
d3
THICKNESS OF & d3(A)
d3 THICKNESS(A)
80
70
60
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20
10
0
9000
8000
7000
6000
5000
4000
3000
2000
1000
0

FIG. 6a

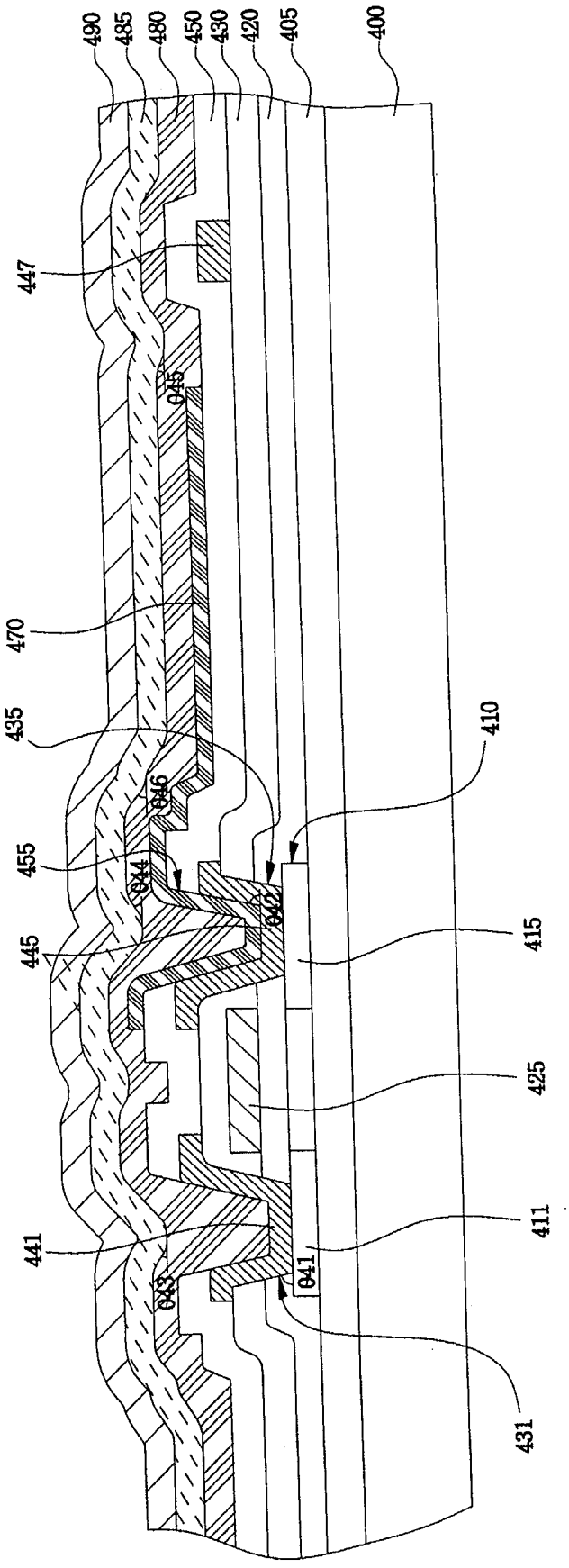
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FIG. 6b

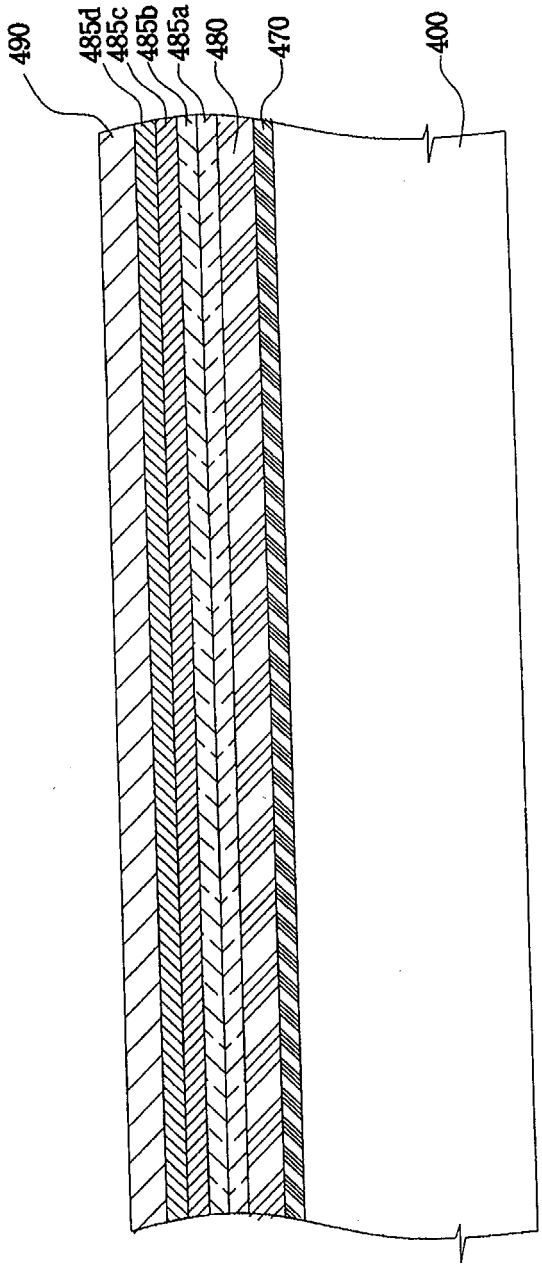

FIG. 6c

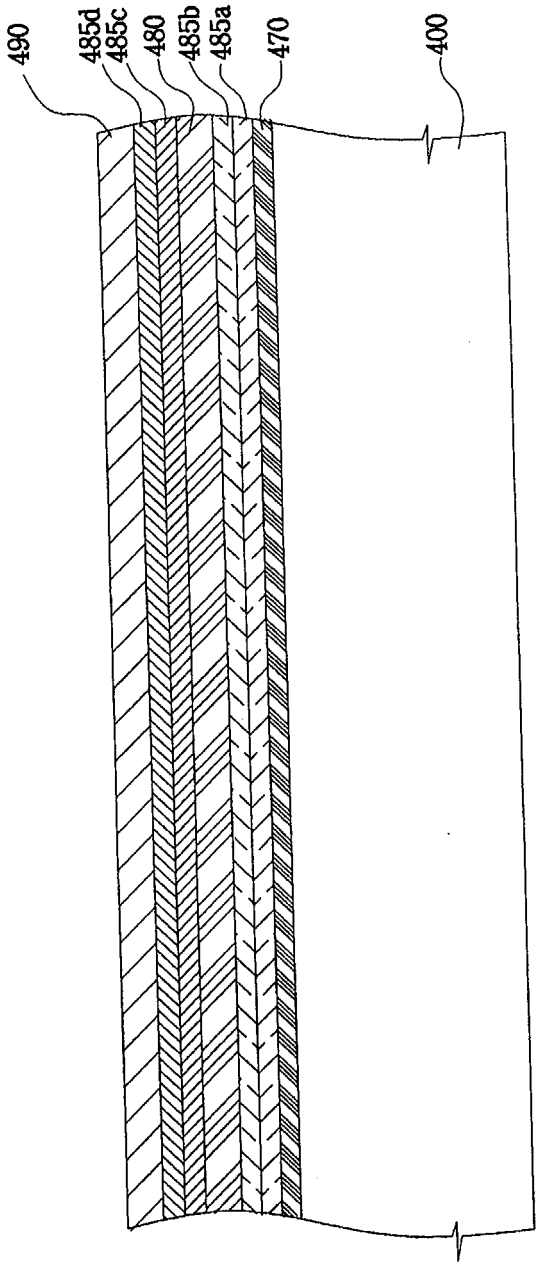

FIG. 7a

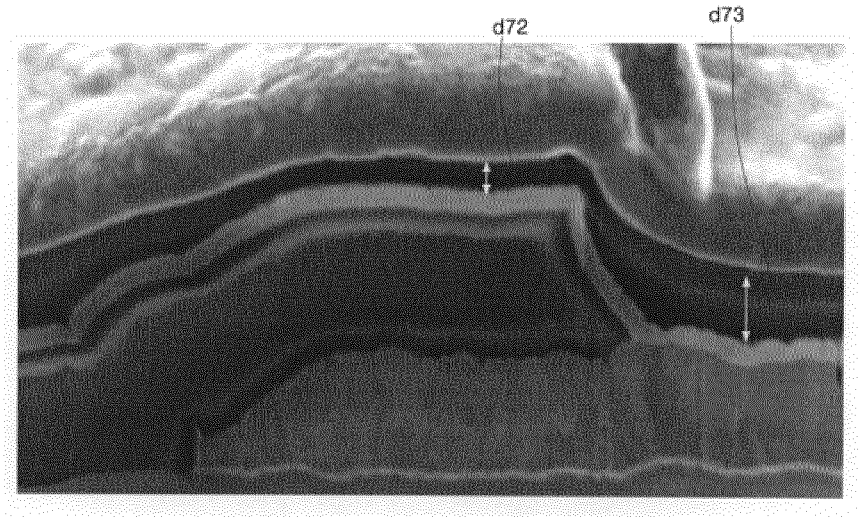

FIG. 7b

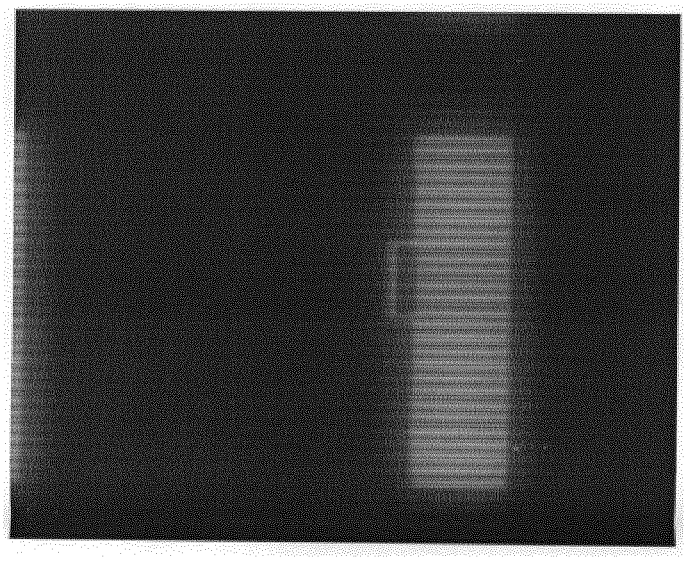

FIG. 7c

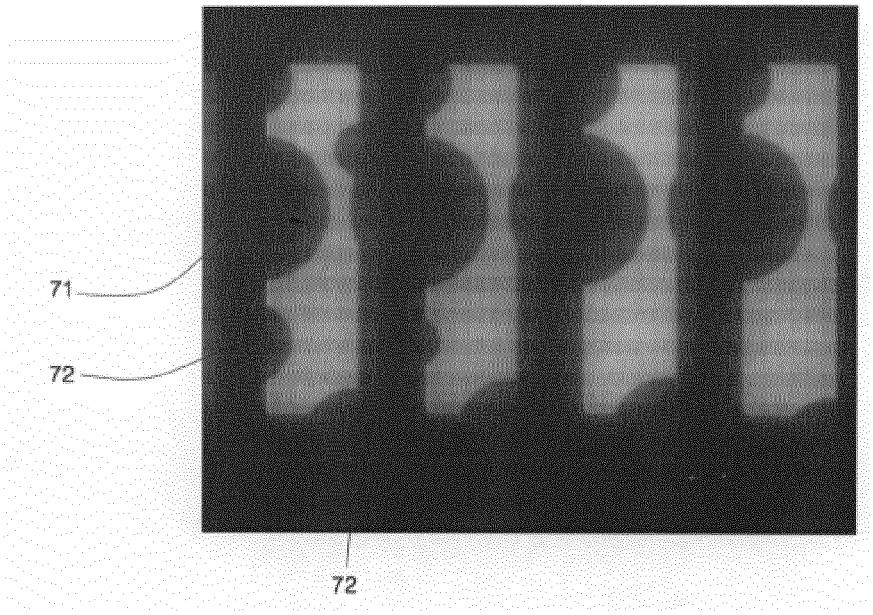

FIG. 8

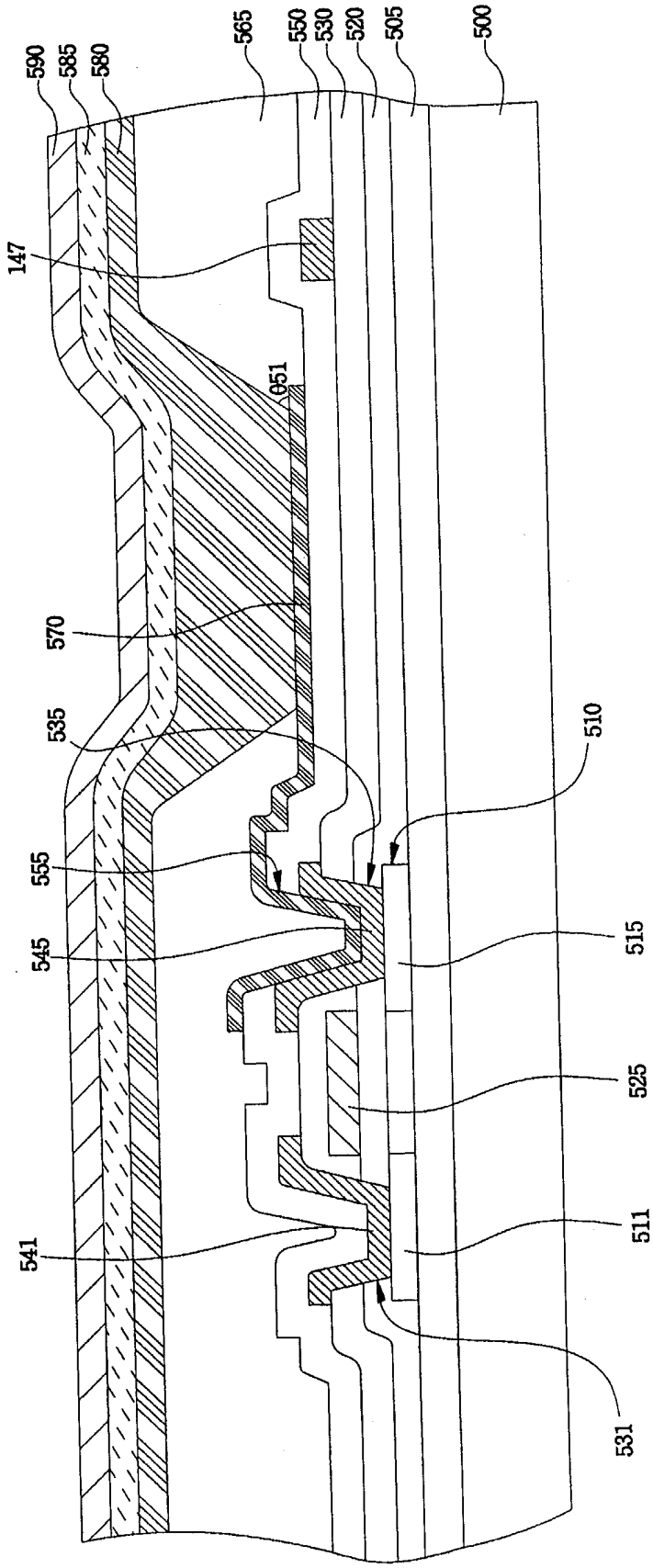
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FIG. 9a

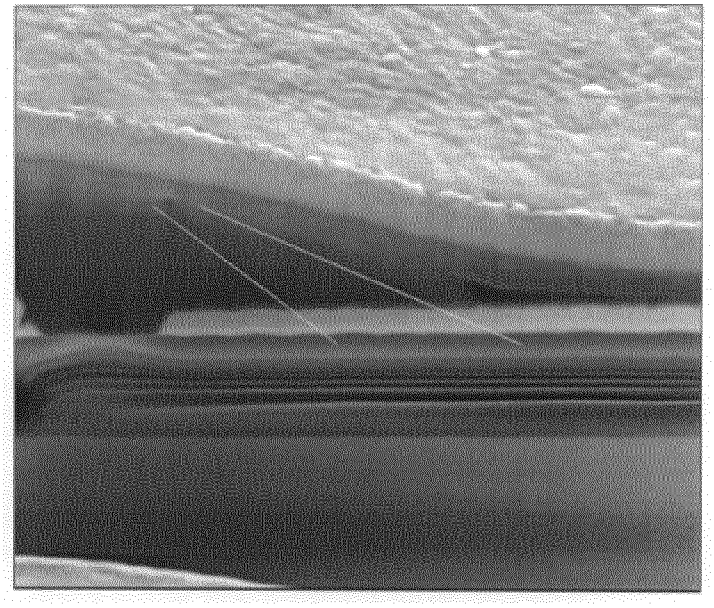


FIG. 9b

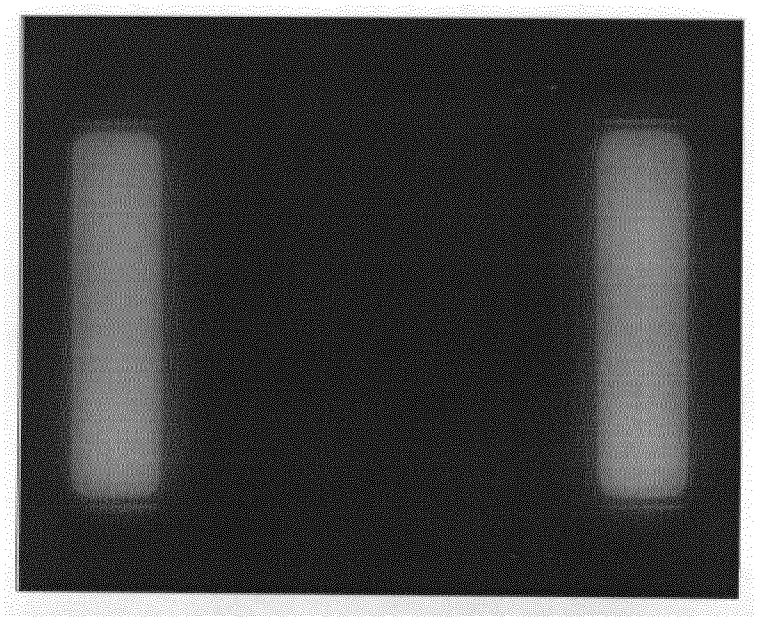


FIG. 9c

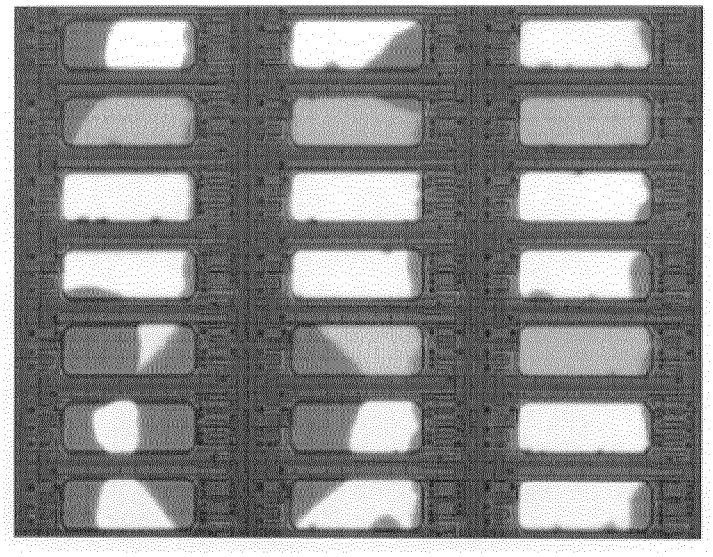
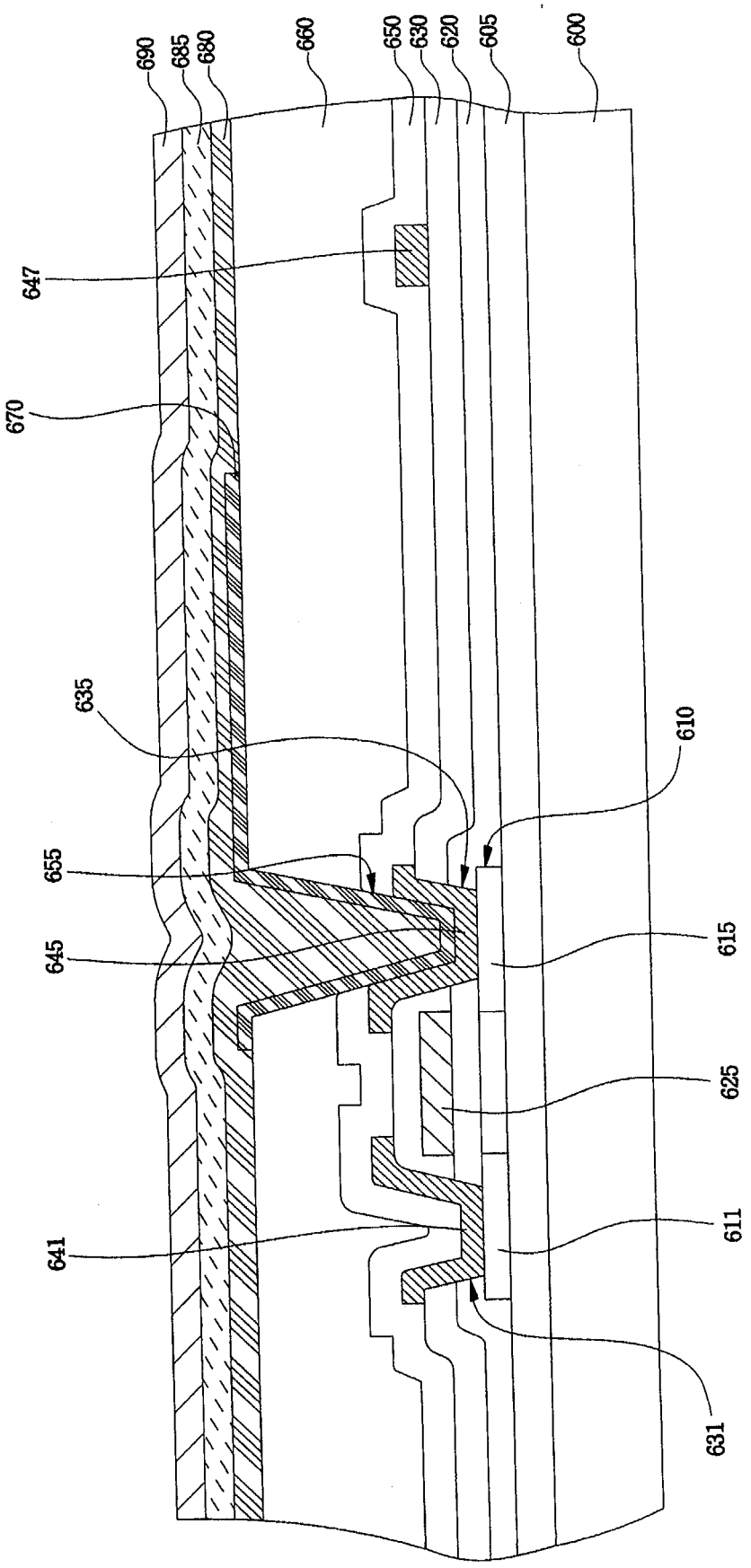


FIG. 10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631

FIG. 11

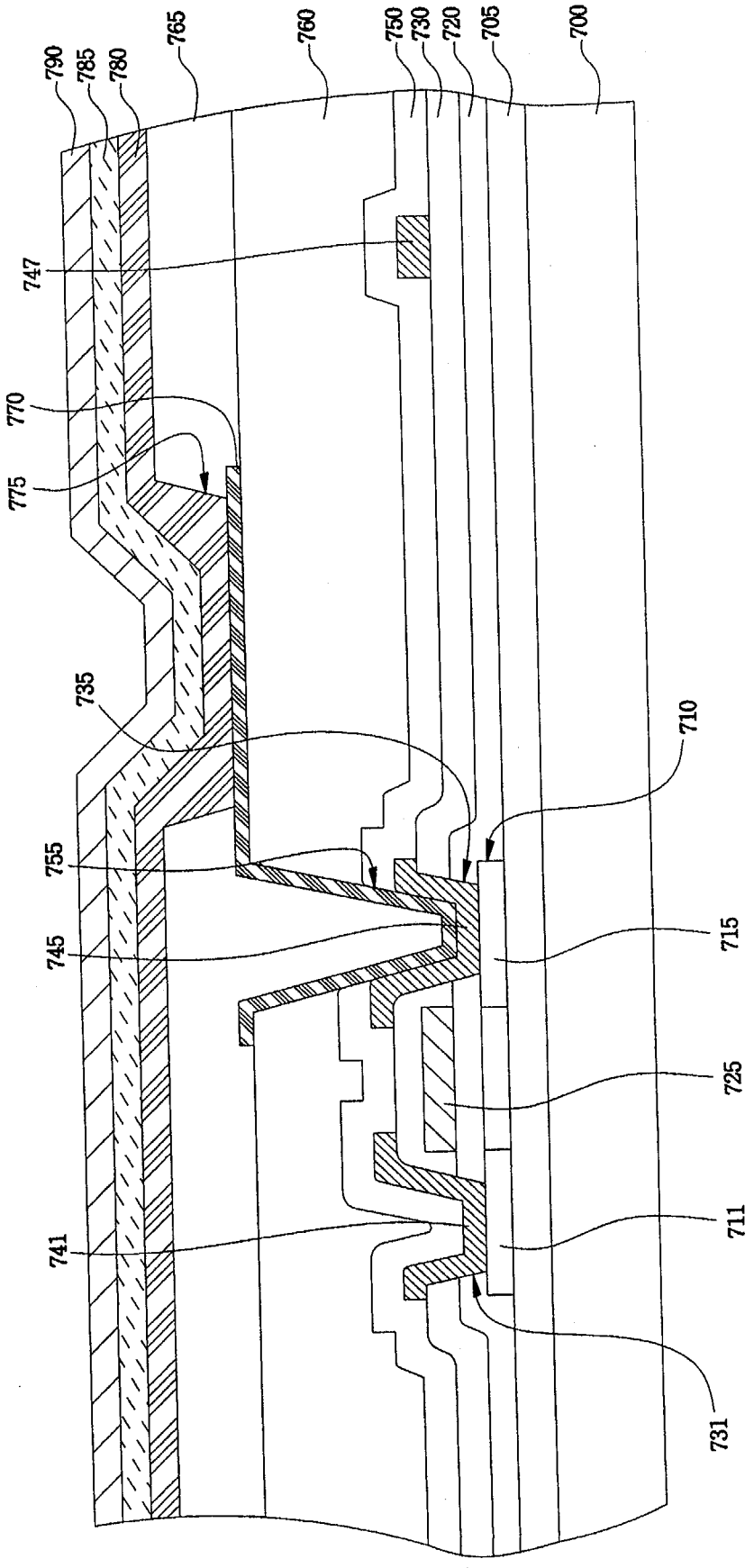
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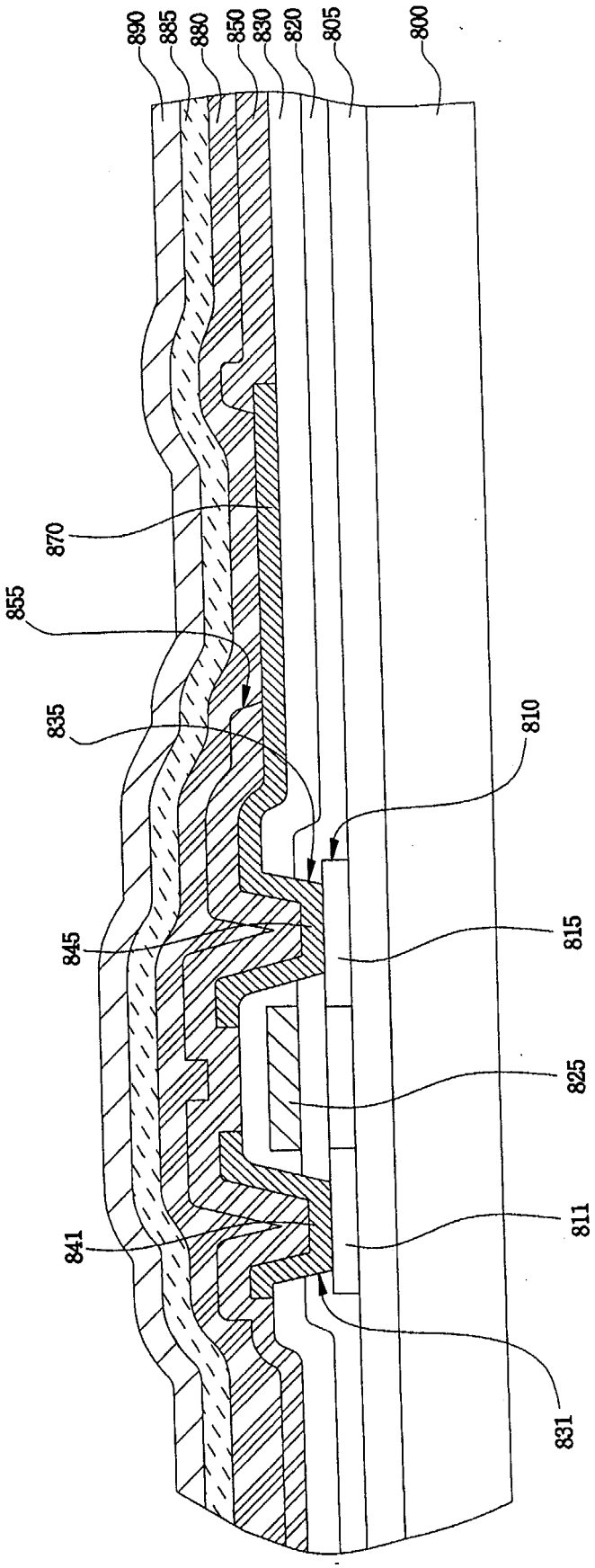
FIG. 12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841
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REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	平板显示器		
公开(公告)号	EP1536471B1	公开(公告)日	2019-10-02
申请号	EP2004090398	申请日	2004-10-18
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
发明人	KIM, MU-HYUNG, C/O SAMSUNG SDI CO., LTD. CHIN, BYUNG-DOO, C/O SAMSUNG SDI CO., LTD. WON, SONG-MYUNG, C/O SAMSUNG SDI CO., LTD. LEE, SEONG-TAEK, C/O SAMSUNG SDI CO., LTD.		
IPC分类号	H01L27/32 H05B33/22 C09K11/06 G09F9/30 H01L27/00 H01L51/50 H01L51/52 H05B33/00 H05B33/02 H05B33/12 H05B33/14 H05B33/20		
优先权	1020030084746 2003-11-26 KR		
其他公开文献	EP1536471A2 EP1536471A3		
外部链接	Espacenet		

摘要(译)

本发明公开了一种用于通过减小基板表面的锥角来防止元件缺陷并改善画面质量的有机发光装置。本发明的平板显示器包括：绝缘基板；形成在绝缘基板上并且相对于基板表面具有第一台阶和第一锥角的下层；以及形成在绝缘基板上的上层，用于减小下层的锥角。上层的第二锥角小于下层的第一锥角。上层是可以通过湿涂法施加的导电层，具有电荷传输能力，并且选自包括咔唑基，芳基胺基，基的小分子有机层中的至少一层。 ，基于二苯乙烯的，基于恶二唑的，基于星爆的衍生物，以及包括PEDOT，PANI，咔唑，芳基胺，per，吡咯，恶二唑的衍生物的聚合物有机层。