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(54) GATE ON ARRAY DRIVER UNIT, GATE ON ARRAY DRIVER CIRCUIT, AND DISPLAY DEVICE

GATE-ON-ARRAY-TREIBEREINHEIT, GATE-ON-ARRAY-TREIBERSCHALTUNG UND ANZEIGEVORRICHTUNG

UNITÉ DE COMMANDE DE GRILLE SUR RÉSEAU, CIRCUIT DE COMMANDE DE GRILLE SUR RÉSEAU ET DISPOSITIF D'AFFICHAGE

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to the field of organic light-emitting display, and more particularly relates to an array substrate row driving unit, array substrate row driving circuit and a display device.

BACKGROUND

[0002] The organic light-emitting diode (OLED) has been increasingly used in high - performance display due to its advantages of high brightness, wide viewing angle and rapid response speed, etc. With the increase of its display size, the conventional passive matrix organic light-emitting diode display (Passive Matrix OLED display) requires a shorter driving time of a single pixel, which needs to increase the transient current, thus increasing the power consumption. At the same time, the application of a large current will cause the voltage drop on the ITO (pixel electrode) line to be excessively large and the working voltage of OLED to be too high, thereby reducing its efficiency. The active matrix organic light-emitting diode display (Active Matrix OLED display) inputs OLED current by progressive scanning via switch transistors, which can solve these problems very well.

[0003] The array substrate row driving circuit (Gate on Array) integrates the gate switch circuit on an array substrate, thus achieving a high-degree integration of the driving circuit, reducing costs both by saving material and reducing process steps.

[0004] As to AMOLED (active matrix organic light - emitting diode) display, not only the generation of a row strobe signal is required to control the ON/OFF state of the pixels connected to the gate line, but also a control over the ON/OFF state of the organic light-emitting display diode is required. The state control signal of the organic light-emitting display diodes for an AMOLED display backplane constituted of the P-type transistors is a positive level signal to ensure that an OLED component is in an OFF state during the process of writing display data into the pixel units, while after the display data have been written into the pixel units, the OLED component turns on and emits light so as to ensure that the displaying image will not flicker due to the unstable state of the pixel circuit when the data are being written.

[0005] EP 1 843 317 A1 discloses a scan driving circuit for a OLED display with a first scan driver including a plurality of first units, the first units receiving an input signal or an output voltage of a previous first unit and first and second clock signals to output a scan signal, and a second scan driver having a plurality of second units, the second units receiving a plurality of scan signals output from respective ones of the first units, and at least one of the first and second clock signals, and outputting an emission control signal.

[0006] US 2011/012823 A1 discloses a liquid crystal display and a shift register device thereof, which shift register device includes a plurality of shift registers connected in series.

[0007] US 2006/001637 A1 discloses a display device including a display panel having gate lines, data lines, display members, and switching members; a timing controller configured to output image data, gate control signals, and data control signals; a shift register configured to sequentially output gate signals to the gate lines based on the gate control signals; and a data drive circuit configured to output data signals to the data lines based on the data control signals, wherein the shift register includes stages corresponding to the gate lines, each of the stages outputting a first clock signal as the gate signal to a corresponding gate line in response to the gate signal of an adjacent stage, inactivating the gate line in response to a second clock signal. An inactive state of the gate line may be maintained in correspondence with the first clock signal.

SUMMARY

[0008] It is an object of the present invention to provide an array substrate row driving unit, array substrate line driving circuit and a display device, which may ensure that an OLED component is in an OFF state during the process of writing display data into the pixel units, while after the display data have been written into the pixel units, the OLED component is turned on and emits light so as to ensure that the displaying image does not flicker due to the unstable state of the pixel circuit when the data are being written.

[0009] The object is solved by the features of the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010]

Figure 1 is a structure diagram of an array substrate row driving unit of a first embodiment of the present invention;

Figure 2 is a circuit diagram of an array substrate row driving unit of a second embodiment of the present invention;

Figure 3 is a timing chart of the respective signals of the array substrate row driving unit of the second embodiment of the present invention at work;

Figure 4 is a circuit diagram of an array substrate row driving unit of a third embodiment of the present invention;

Figure 5 is a timing chart of the respective signals of the array substrate row driving unit of the third embodiment of the present invention at work; and

Figure 6 is a circuit diagram of an array substrate row driving circuit of an embodiment of the present invention.

DETAILED DESCRIPTION

[0011] Compared to AMLCD (Active Matrix Liquid Crystal Display), AMOLED (active matrix organic light-emitting diode) is usually implemented in a low-temperature polysilicon circuit with greater mobility due to its need for an increased driving current. To compensate for the threshold voltage drift problem present in the polysilicon TFT (thin film transistor), the pixel circuit of the AMOLED often requires a corresponding compensative structure, so the structure of the pixel circuit of the AMOLED is more complex, and correspondingly needs to occupy a larger circuit layout area.

[0012] An embodiment of the present invention provides an array substrate row driving circuit, which has a simple structure and stable performance, for the active matrix organic light-emitting display, and the array substrate row driving circuit comprises a plurality of cascading array substrate row driving units manufactured on the array substrate of a liquid crystal through an array film-forming process. Each array substrate row driving unit contains 8 thin film transistors and 2 capacitors. The array substrate row driving unit is divided into two stages, a first stage being used for generating a the conventional gate line strobe signal, a second stage being used for accordingly generating a control signal to control the switching of the organic light-emitting diode. The array substrate row driving circuit according to an embodiment of present invention has a simple and compact structure, which reduces the circuit layout area, and is the best choice to achieve high resolution AMOLED display.

[0013] As shown in Figure 1, the array substrate row driving unit according to a first embodiment of present invention includes a gate driving module 11 and an emission control module 12, wherein,

[0014] the gate driving module 11 being connected to the emission control module 12, for generating a gate driving signal;

[0015] the emission control module being is used for generating an emission control signal for controlling the switching of OLED under control of the gate driving signal, the gate driving signal having an opposite phase to that of the emission control signal.

[0016] In the array substrate row driving unit according to the first embodiment of the present invention, the emission control module 12 generates an emission control signal that has an opposite phase to that of the gate drive signal, so that OLED component is in an OFF state during the process of writing the display data into the pixel units, while OLED component turns on and emits light after the display data have been written into the pixel units, therefore ensuring that the displaying image will not flicker due to the unstable state of the pixel circuit when the data is written.

[0017] As shown in Figure 2, it shows a circuit diagram of an array substrate row driving unit according to a second embodiment of the present invention. The array substrate row driving unit according to the second embodiment of the present invention is based on that of the first embodiment of the present invention. In the array substrate row driving unit according to the second embodiment of the present invention ,

[0018] the gate driving module including a first thin film transistor T1, a second thin film transistor T2, a third thin film transistor T3, a fourth thin film transistor T4 and a first bootstrap capacitor C1, wherein,

[0019] the first thin film transistor T1, having a gate connected to the output for the gate driving signal of the previous-stage array substrate row driving unit, a source connected to a drain of the second thin film transistor T2, and a drain connected to the low-level output of the driving power supply;

[0020] the second thin film transistor T2, having gate connected to the output for the gate driving signal of next-stage array substrate row driving unit, and a source connected to the high-level output of the driving power supply;

[0021] the third thin film transistor T3, having a gate connected to the source of the first thin film transistor T1, a source connected to a drain of the fourth thin film transistor T4, and a drain connected to the input for a first clock signal;

[0022] the fourth thin film transistor T4, having a gate connected to the input for a second clock signal, and a source connected to the high-level output of the driving power supply;

[0023] the first bootstrap capacitor C1 being connected between the gate and source of the third thin film transistor T3;

[0024] the first thin film transistor T1, the second thin film transistor T2, the third thin film transistor T3 and the fourth thin film transistor T4 being p-type thin film transistors.

[0025] the emission control module comprising a fifth thin film transistor T5, a sixth fifth thin film transistor T6, a seventh thin film transistor T7, an eighth thin film transistor T8 and a second bootstrap capacitor C2, wherein,

[0026] the fifth thin film transistor T5, having a gate connected to the output for the gate driving signal of next-stage array substrate row driving unit, a source connected to the drain of the sixth thin film transistor T6, and a drain connected to the low-level output of the driving power supply;

[0027] the sixth thin film transistor T6, having a gate connected to the drain of the fourth thin film transistor T4, and a source connected to the high-level output of the driving power supply;

[0028] the seventh thin film transistor T7, having a gate connected to the source of the fifth thin film transistor T5, a source connected to a drain of the eighth thin film transistor T8, and a drain connected to the low-level output of the driving power supply;

[0029] the eighth thin film transistor T8, having a gate connected to the gate of the sixth thin film transistor T6, and a source connected to the high-level output of the driving power supply;

[0030] the second bootstrap capacitor C2 being connected between the gate and source of the seventh thin film transistor T7;

[0031] the fifth thin film transistor T5, the sixth thin film transistor T6, the seventh thin film transistor T7 and the eighth thin film transistor T8 being p-type thin film transistors;

[0032] the gate of the first thin film transistor T1 being the input of the array substrate row driving unit according to the second embodiment of present invention, the gate of the second thin film transistor T2 being the reset terminal of the array substrate row driving unit according to the second embodiment of present invention, the source of the third thin film transistor T3 being the output for the gate driving signal of the array substrate row driving unit according to the second embodiment of present invention, the source of the seventh thin film transistor T7 being an output for the emission control signal of the array substrate row driving unit according to the second embodiment of present invention.

[0033] Wherein output voltage of the low-level output of the driving power supply is VGL, and output voltage of the high-level output of the driving power supply is VGH. A first clock signal CLK1 is input into the first clock signal input, and a second clock signal CLK2 is input into the second clock signal input. The output signal of the output for the gate driving signal of the previous-stage array substrate row driving unit is G[n-1], that of the present-stage array substrate row driving unit is G[n], and that of the next-stage array substrate row driving unit is G[n+1]. The output signal of the output for the emission control signal of the present-stage array substrate row driving unit is EMISSION[n]. The point N1 is a node connected to the gate of the third thin film transistor T3, and the point N2 is a node connected to the gate of the seventh thin film transistor T7.

[0034] The array substrate row driving unit according to the second embodiment of the present invention is controlled by the first clock signal CLK1 and the second clock signal CLK2. The output signal of the output for the gate driving signal of the previous-stage array substrate row driving unit G[n-1] serves as the input signal of the present-stage array substrate row driving unit, and the output signal of the output for the gate driving signal of the next-stage array substrate row driving unit G[n+1] serves as the reset signal of the present-stage array substrate row driving unit.

[0035] As shown in Fig. 3, the work process of the array substrate row driving unit according to the second embodiment of the present invention is divided into input sampling phase t1, signal output phase t2 and reset phase T3.

[0036] During the input sampling phase t1, G[n-1] is low and T1 is turned on, while G[n+1] is high and T2 is turned off, so in this case the potential at point N1 is correspondingly pulled down to VGL+|Vthp|. At this time CLK2 is low, T4 is turned off, and G[n] is high, so at this time C1 is being charged, and the input signal is sampled. At this time, G[n] and G [n+1] are both high, ensuring the working state of each transistor included in the control module will not change.

[0037] During the signal output phase t2, G[n-1] and G[n+1] are both high, and the potential at point N1 is maintained a VGL+|Vthp| by C1, which is a low-level, so T3 is turned on. At the same time, CLK2 is high, T4 is turned off and G[n] is low, so T6 and T8 are turned on. At this time, EMISSION[n] is high, used for lighting the organic light-emitting diode components.

[0038] During the reset phase t3, G [n -1] is high, ensuring that transistors T1 and T3 are turned off; CLK2 is low and T4 is turned on, so G[n] is pulled up to a high level; G[N] is high, ensuring that T6 and T8 are turned off, while G[n+1] is low, and the voltage at point N1 is pulled up again by turning on T2; T5 is turned on at the same time, and the potential at point N2 is pulled down to VGL+|Vthp|; T7 is turned on, and EMISSION[n] is correspondingly pulled down, thereby completing the reset operation of EMISSION[n];

wherein, Vthp being the threshold voltage of T1 and T5.

[0039] Figure 4 shows the circuit diagram of the array substrate row driving unit according to a third embodiment of the present invention. The array substrate row driving unit according to the third embodiment of the present invention is based on that according to the first embodiment of the present invention. In the gate driving circuit unit according to the third embodiment of the present invention,

the gate driving module comprises a first thin film transistor T1, a second thin film transistor T2, a third thin film transistor T3, a fourth thin film transistor T4 and a first bootstrap capacitor C1, wherein,

the first thin film transistor T1, having a gate connected to the output for the gate driving signal of the previous-stage array substrate row driving unit, a source connected to a drain of the second thin film transistor T2, and a drain connected to the high-level output of the driving power supply;

the second thin film transistor T2, having a gate connected to the output for the gate driving signal of the next-stage array substrate row driving unit, and a source connected to the low-level output of the driving power supply;

the third thin film transistor T3, having a gate connected to the source of the first thin film transistor T1, a source connected to a drain of the fourth thin film transistor T4, and a drain connected to the input for a first clock signal;

the fourth thin film transistor T4, having a gate connected to the input for a second clock signal, and a source connected to the low-level output of the driving power supply;

the first bootstrap capacitor C1 being connected between the gate and source of the third thin film transistor T3;

the first thin film transistor T1, the second thin film transistor T2, the third thin film transistor T3 and the fourth thin film transistor T4 being n-type thin film transistors;

the emission control module comprising a fifth thin film transistor T5, a sixth fifth thin film transistor T6, a seventh thin film transistor T7, an eighth thin film transistor T8

and a second bootstrap capacitor C2, wherein,
the fifth thin film transistor T5, having a gate connected to the output for the gate driving signal of the next-stage array substrate row driving unit, a source connected to a drain of the sixth thin film transistor T6, and a drain connected to the high-level output of the driving power supply;
the sixth thin film transistor T6, having a gate connected to the drain of the fourth thin film transistor T4, and a source connected to the low-level output of the driving power supply;
the seventh thin film transistor T7, having a gate connected to the source of the fifth thin film transistor T5, a source connected to a drain of the eighth thin film transistor T8, and a drain connected to the high-level output of the driving power supply;
the eighth thin film transistor T8, having a gate connected to the gate of the sixth thin film transistor T6, and a source connected to the low-level output of the driving power supply;
the second bootstrap capacitor C2 being connected between the gate and source of the seventh thin film transistor T7;
the fifth thin film transistor T5, the sixth thin film transistor T6, the seventh thin film transistor T7 and the eighth thin film transistor T8 being n-type thin film transistors; the gate of the first thin film transistor T1 being the input of the array substrate row driving unit according to the third embodiment of present invention, the gate of the second thin film transistor T2 being the reset terminal of the array substrate row driving unit according to the third embodiment of present invention, and the source of the third thin film transistor T3 being the output for the gate driving signal of the array substrate row driving unit according to the third embodiment of present invention; the source of the seventh thin film transistor T7 being the output for the emission control signal of the array substrate row driving unit according to the third embodiment of present invention;
wherein, output voltage of the low-level output of the driving power supply being VGL, and output voltage of the high-level output of the driving power supply being VGH; a first clock signal CLK1 being inputted into the first clock signal input, and a second clock signal CLK2 being inputted into the second clock signal input; the output signal of the output for the gate driving signal of the previous-stage array substrate row driving unit being G[n-1], that of the present-stage array substrate row driving unit being G[n], and that of the next-stage array substrate row driving unit being G[n+1]; the output signal of the output for the emission control signal of the present-stage array substrate row driving unit being EMISSION[n]; point N1 being a node connected to the gate of the third thin film transistor T3, and point N2 being a node connected to the gate of the seventh thin film transistor T7.

[0040] The array substrate row driving unit according to the third embodiment of the present invention is controlled by the first clock signal CLK1 and the second clock signal CLK2. The output signal of the output for the gate driving signal of the previous-stage array substrate row driving unit G[n-1] serves as the input signal of the present-stage array substrate row driving unit, and the output signal of the output for the gate driving signal of the next-stage array substrate row driving unit G[n+1] serves as the reset signal of the present-stage array substrate row driving unit.

[0041] As shown in Fig. 5, the work process of the array substrate row driving unit according to the third embodiment of the present invention is divided into input sampling phase t1, signal output phase t2 and reset phase T3. The work process of the third embodiment of the present invention is similar to the second embodiment, and the related description will be omitted hereinafter.

[0042] The exemplary emission control module of the array substrate row driving unit according to the second and the third embodiment of the present invention are only by way of illustration, and have no limiting effect on the structure of the emission control module. Any control components that can generate, under control of the gate driving signal, an emission control signal which control the switching of the organic light-emitting diode and which has an opposite phase to that of the gate driving signal can all be used for constituting the emission control module.

[0043] An embodiment of the present invention also provides an array substrate row driving circuit, including multi-stages aforementioned array substrate row driving units manufactured on the array substrate of a liquid crystal through an array film-forming process.

[0044] Except for the first-stage array substrate row driving unit, the input of each stage of the array substrate row driving units is connected to the output for the gate driving signal of the previous-stage array substrate row driving unit;

[0045] Except for the final-stage array substrate row driving unit, the reset terminal of each stage of the array substrate row driving units is connected to the output for the gate driving signal of the next-stage array substrate row driving unit.

[0046] Fig. 6 shows an array substrate row driving circuit according to an embodiment of the present invention, comprising N+1 stages of array substrate row driving units, wherein N being a positive integer.

[0047] The input of the first-stage array substrate row driving unit is connected to the input signal INPUT.

[0048] Except for the first-stage array substrate row driving unit, the input of each stage of the array substrate row driving units IN is connected to the output for the gate driving signal of the previous-stage array substrate row driving unit.

[0049] Except for the final-stage array substrate row driving unit, the reset terminal of each stage of the array substrate row driving units RESET is connected to the output for the gate driving signal of the next-stage array substrate row driving unit.

[0050] In Fig. 6, EMISSION_1, EMISSION _2, EMIS-

SION _3, EMISSION _N and EMISSION _N +1 indicate the output for the emission control signal of the first-stage array substrate row driving unit, the output for the emission control signal of the second-stage array substrate row driving unit, the output for the emission control signal of the third-stage array substrate row driving unit, the output for the emission control signal of the Nth-stage array substrate row driving unit and the output for the emission control signal of the N+1th-stage array substrate row driving unit respectively.

[0051] STAGE_1, STAGE _2, STAGE _3, STAGE _N and STAGE _N +1 indicate the first-stage array substrate row driving unit, the second-stage array substrate row driving unit, the third-stage array substrate row driving unit, the Nth-stage array substrate row driving unit and the N+1 th-stage array substrate row driving unit.

[0052] An embodiment of the present invention also provides a display device, comprising the aforementioned array substrate row driving circuit.

Claims

1. An array substrate row driving circuit for an AMOLED display comprising multi-stages of array substrate row driving units, wherein a present-stage array substrate row driving unit comprises a gate driving module (11) for generating and outputting a gate driving signal (G[n]) and an emission control module (12) for generating and outputting an emission control signal (EMISSION[n]);
wherein the emission control module (12) is connected to the output for the gate driving signal (G[n]) of the gate driving module (11) and the emission control signal is for controlling the switching of an OLED under control of the gate driving signal, the gate driving signal having an opposite phase to that of the emission control signal;
characterized by the gate driving module (11) comprising a first thin film transistor (T1), a second thin film transistor (T2), a third thin film transistor (T3), a fourth thin film transistor (T4) and a first bootstrap capacitor (C1), wherein
the first thin film transistor (T1) has a gate connected to the output for the gate driving signal (G[n-1]) of the previous-stage array substrate row driving unit, a source connected to a drain of the second thin film transistor (T2) and a drain connected to a first level output of the driving power supply;
the second thin film transistor (T2) has a gate connected to the output for the gate driving signal (G[n+1]) of the next-stage array substrate row driving unit and a source connected to a second level output of the driving power supply;
the third thin film transistor (T3) has a gate connected to the source of the first thin film transistor (T1), a source connected to a drain of the fourth thin film transistor (T4) and a drain connected to the input for a first clock signal (CLK1);
the fourth thin film transistor (T4) has a gate connected to the input for a second clock signal (CLK2) and a source connected to the second level output of the driving power supply;
the first bootstrap capacitor (C1) is connected between the gate and source of the third thin film transistor (T3);
the gate of the first thin film transistor (T1) is an input, and the source of the third thin film transistor (T3) is the output for the gate driving signal (G[n]) of the gate driving module (11);
and further **characterized by** the emission control module (12) comprising a fifth thin film transistor (T5), a sixth thin film transistor (T6), a seventh thin film transistor (T7), an eighth thin film transistor (T8) and a second bootstrap capacitor (C2), wherein
the fifth thin film transistor (T5) has a gate connected to the output for the gate driving signal (G[n+1]) of the next-stage array substrate row driving unit, a source connected to a drain of the sixth thin film transistor (T6) and a drain being connected to the first output level of the driving power supply;
the sixth thin film transistor (T6) has a gate connected to the drain of the fourth thin film transistor (T4) and a source connected to the second output level of the driving power supply;
the seventh thin film transistor (T7) has a gate connected to the source of the fifth thin film transistor (T5), a source connected to a drain of the eighth thin film transistor (T8) and a drain connected to the first output level of the driving power supply;
the eighth thin film transistor (T8) has a gate connected to the gate of the sixth thin film transistor (T6) and a source connected to the second output level of the driving power supply;
the second bootstrap capacitor (C2) is connected between the gate and source of the seventh thin film transistor (T7);
the source of the seventh thin film transistor (T7) is the output for the emission control signal (EMISSION[n]).

2. The array substrate row driving circuit according to claim 1, wherein
the first level output of the driving power supply is a low-level output;
the second level output of the driving power supply is a high-level output;
the first thin film transistor (T1), the second thin film transistor (T2), the third thin film transistor (T3) and the fourth thin film transistor (T4) are p-type thin film transistors.

3. The array substrate row driving circuit according to claim 2, wherein
the first level output of the driving power supply is a low-level output;

the second level output of the driving power supply is a high-level output;
the fifth thin film transistor (T5), the sixth thin film transistor (T6), the seventh thin film transistor (T7) and the eighth thin film transistor (T8) are p-type thin film transistors.

4. The array substrate row driving circuit according to claim 1, wherein
the first level output of the driving power supply is a high-level output;
the second level output of the driving power supply is a low-level output;
the first thin film transistor (T1), the second thin film transistor (T2), the third thin film transistor (T3) and the fourth thin film transistor (T4) are n-type thin film transistors.

5. The array substrate row driving circuit according to claim 4, wherein
the first level output of the driving power supply is a high-level output;
the second level output of the driving power supply is a low-level output;
the fifth thin film transistor (T5), the sixth thin film transistor (T6), the seventh thin film transistor (T7) and the eighth thin film transistor (T8) are n-type thin film transistors.

6. The array substrate row driving circuit according to any of claims 1 to 5, wherein the array substrate row driving circuit is manufactured on the array substrate of an organic light-emitting diode display through an array film-forming process, wherein
except for the first-stage array substrate row driving unit, an input of each stage of the array substrate row driving units is connected to the output for the gate driving signal of the previous-stage array substrate row driving unit;
except for the final-stage array substrate row driving unit, a reset terminal of each stage of the array substrate row driving units is connected to the output for the gate driving signal of the next-stage array substrate row driving unit adjacent to the present-stage array substrate row driving unit.

7. A display device, comprising the array substrate row driving circuit according to claim 6.

Patentansprüche

1. Array-Substrat-Zeilentreiberschaltung für eine AMOLED-Anzeige mit mehreren Stufen von Array-Substrat-Zeilentreibereinheiten, wobei eine Array-Substrat-Zeilentreibereinheit einer aktuellen Stufe ein Gate-Treibermodul (11) zum Erzeugen und Ausgeben eines Gate-Treibersignals (G[n]) und ein Ausgabesteuermodul (12) zum Erzeugen und Ausgeben eines Ausgabesteuersignals (EMISSION[n]) aufweist;
wobei das Ausgabesteuermodul (12) mit dem Ausgang für das Gate-Treibersignal in (G[n]) des Gate-Treibermoduls (11) verschaltet ist und das Ausgabesteuersignal zum Steuern des Schaltens eines OLEDs unter Steuerung des Gate-Treibersignals bestimmt ist, wobei das Gate-Treibersignal eine gegenläufige Phase zu der des Ausgabesteuersignals aufweist;
gekennzeichnet dadurch, dass das Gate-Treibermodul (11) einen ersten Dünnschichttransistor (T1), einen zweiten Dünnschichttransistor (T2), einen dritten Dünnschichttransistor (T3), einen vierten Dünnschichttransistor (T4) und einen ersten Bootstrap-Kondensator (C1) aufweist, wobei
der erste Dünnschichttransistor (T1) ein Gate, welches mit dem Ausgang für das Gate-Treibersignal (G[n-1]) der Array-Substrat-Zeilentreibereinheit verschaltet ist, eine Source, die mit einem Drain des zweiten Dünnschichttransistors (T2) verschaltet ist, und einen Drain, der mit einem Treiberspannungsversorgungsausgang mit einem ersten Pegel verschaltet ist, aufweist;
der zweite Dünnschichttransistor (T2) ein Gate, welches mit dem Ausgang für das Gate-Treibersignal (G[n+1]) der Array-Substrat-Zeilentreibereinheit der nächsten Stufe verschaltet ist, und eine Source, die mit einem Treiberspannungsversorgungsausgang mit einem zweiten Pegel verschaltet ist, aufweist;
der dritte Dünnschichttransistor (T3) ein Gate, welches mit der Source des ersten Dünnschichttransistors (T1) verschaltet ist, eine Source, die mit einem Drain des vierten Dünnschichttransistors (T4) verschaltet ist, und einen Drain, der mit dem Eingang für ein erstes Taktsignal (CLK1) verschaltet ist, aufweist;
der vierte Dünnschichttransistor (T4) ein Gate, welches mit dem Eingang für ein zweites Taktsignal (CLK2) verschaltet ist, und eine Source, die mit dem Treiberspannungsversorgungsausgang mit dem zweiten Pegel verschaltet ist, aufweist;
der erste Bootstrap-Kondensator (C1) zwischen das Gate und die Source des dritten Dünnschichttransistors (T3) geschaltet ist;
das Gate des ersten Dünnschichttransistors (T1) ein Eingang ist und die Source des dritten Dünnschichttransistors (T3) der Ausgang für das Gate-Treibersignal (G[n]) des Gate-Treibermoduls (11) ist;
und weiter **dadurch gekennzeichnet, dass** das Ausgabesteuermodul (12) einen fünften Dünnschichttransistor (T5), einen sechsten Dünnschichttransistor (T6), einen siebten Dünnschichttransistor (T7), einen achten Dünnschichttransistor (T8) und einen zweiten Bootstrap-Kondensator (C2) aufweist, wobei
der fünfte Dünnschichttransistor (T5), ein Gate, wel-

ches mit dem Ausgang für das Gate-Treibersignal (G[n+1]) der Array-Substrat-Zeilentreibereinheit der nächsten Stufe verschaltet ist, eine Source, die mit einem Drain des sechsten Dünnschichttransistors (T6) verschaltet ist, und einem Drain, der mit dem Treiberspannungsversorgungsausgang mit dem ersten Pegel verschaltet ist, aufweist;
der sechste Dünnschichttransistor (T6), ein Gate, welches mit dem Drain des vierten Dünnschichttransistors (T4) verschaltet ist, und einer Source, die mit dem Treiberspannungsversorgungsausgang mit dem zweiten Pegel verschaltet ist, aufweist;
der siebte Dünnschichttransistor (T7), ein Gate, welches mit der Source des fünften Dünnschichttransistors (T5) verschaltet ist, eine Source, die mit einem Drain des achten Dünnschichttransistors (T8) verschaltet ist, und einem Drain, welches mit dem Treiberspannungsversorgungsausgang mit dem ersten Pegel verschaltet ist, aufweist;
der achte Dünnsichttransistor (T8), ein Gate, welches mit dem Gate des sechsten Dünnschichttransistors (T6) verschaltet ist, und einer Source, die mit dem Treiberspannungsversorgungsausgang mit dem zweiten Pegel verschaltet ist, aufweist;
der zweite Bootstrap-Kondensator (C2) zwischen das Gate und die Source des siebten Dünnschichttransistors (T7) geschaltet ist;
die Source des siebten Dünnschichttransistors (T7) der Ausgang für das Ausgabesteuersignal (EMISSION[n]) ist.

2. Array-Substrat-Zeilentreiberschaltung gemäß Anspruch 1, wobei
der Treiberspannungsversorgungsausgang mit dem ersten Pegel ein Niedrig-Pegel-Ausgang ist;
der Treiberspannungsversorgungsausgang mit dem zweiten Pegel ein Hoch-Pegel-Ausgang ist;
der erste Dünnschichttransistor (T1), der zweite Dünnschichttransistor (T2), der dritte Dünnschichttransistor (T3) und der vierte Dünnschichttransistor (T4) p-leitende Dünnschichttransistoren sind.

3. Array-Substrat-Zeilentreiberschaltung gemäß Anspruch 2, wobei
der Treiberspannungsversorgungsausgang mit dem ersten Pegel ein Niedrig-Pegel-Ausgang ist;
der Treiberspannungsversorgungsausgang mit dem zweiten Pegel ein Hoch-Pegel-Ausgang ist;
der fünfte Dünnschichttransistor (T5), der sechste Dünnschichttransistor (T6), der siebte Dünnschichttransistor (T7) und der achte Dünnschichttransistor (T8) p-leitende Dünnschichttransistoren sind.

4. Array-Substrat-Zeilentreiberschaltung gemäß Anspruch 1, wobei
der Treiberspannungsversorgungsausgang mit dem ersten Pegel ein Hoch-Pegel-Ausgang ist;
der Treiberspannungsversorgungsausgang mit dem zweiten Pegel ein Niedrig-Pegel-Ausgang ist;
der erste Dünnschichttransistor (T1), der zweite Dünnschichttransistor (T2), der dritte Dünnschichttransistor (T3) und der vierte Dünnschichttransistor (T4) n-leitende Dünnschichttransistoren sind.

5. Array-Substrat-Zeilentreiberschaltung gemäß Anspruch 4, wobei
der Treiberspannungsversorgungsausgang mit dem ersten Pegel ein Hoch-Pegel-Ausgang ist;
der Treiberspannungsversorgungsausgang mit dem zweiten Pegel ein Niedrig-Pegel-Ausgang ist;
der fünfte Dünnschichttransistor (T5), der sechste Dünnschichttransistor (T6), der siebte Dünnschichttransistor (T7) und der achte Dünnschichttransistor (T8) n-leitende Dünnschichttransistoren sind.

6. Array-Substrat-Zeilentreiberschaltung gemäß einem der Ansprüche 1 bis 5, wobei die Array-Substrat-Zeilentreiberschaltung auf dem Array-Substrat einer OLED-Anzeige durch einen Array-Dünnschicht-Ausbildungsprozess hergestellt wird, wobei mit Ausnahme der Array-Substrat-Zeilentreibereinheit der ersten Stufe ein Eingang jeder Stufe der Array-Substrat-Zeilentreibereinheiten mit dem Ausgang für das Gate-Treibersignal der Array-Substrat-Zeilentreibereinheit der vorhergehenden Stufe verschaltet ist;
mit Ausnahme der Array-Substrat-Zeilentreibereinheit der letzten Stufe ein Reset-Anschluss jeder Stufe der Array-Substrat-Zeilentreibereinheiten mit dem Ausgang für das Gate-Treibersignal der Array-Substrat-Zeilentreibereinheit der nächsten Stufe, die benachbart zur Array-Substrat-Zeilentreibereinheit der aktuellen Stufe ist, verschaltet ist.

7. Anzeigevorrichtung, die die Array-Substrat-Zeilentreiberschaltung gemäß Anspruch 6 aufweist.

Revendications

1. Circuit de commande de ligne pour substrat de matrice destiné à un affichage AMOLED, comprenant plusieurs étages d'unités de commande de ligne pour substrat de matrice, dans lequel une unité de commande de ligne pour substrat de matrice d'étage actuel comprend un module de commande de grille (11) destiné à générer et émettre un signal de commande de grille (G[n]) et un module de contrôle d'émission (12) destiné à générer et émettre un signal de contrôle d'émission (EMISSION [n]) ;
dans lequel le module de contrôle d'émission (12) est connecté à la sortie pour le signal de commande de grille (G[n]) du module de commande de grille (11), et le signal de contrôle d'émission est destiné à contrôler la commutation d'une OLED sous le contrôle du signal de commande de grille, le signal de

commande de grille présentant une phase opposée à celle du signal de contrôle d'émission ;

caractérisé par fait que le module de commande de grille (11) comprend un premier transistor à couches minces (T1), un deuxième transistor à couches minces (T2), un troisième transistor à couches minces (T3), un quatrième transistor à couches minces (T4) et un premier condensateur d'amorçage (C1), dans lequel

le premier transistor à couches minces (T1) présente une grille connectée à la sortie pour le signal de commande de grille G[n-1] de l'unité de commande de ligne pour substrat de matrice d'étage précédent, une source connectée à un drain du deuxième transistor à couches minces (T2), et un drain connecté à une sortie de premier niveau de l'alimentation électrique de commande ;

le deuxième transistor à couches minces (T2) présente une grille connectée à la sortie pour le signal de commande de grille (G[n+1]) de l'unité de commande de ligne pour substrat de matrice d'étage suivant, et une source connectée à une sortie de second niveau de l'alimentation électrique de commande ;

le troisième transistor à couches minces (T3) présente une grille connectée à la source du premier transistor à couches minces (T1), une source connectée à un drain du quatrième transistor à couches minces (T4), et un drain connecté à l'entrée pour un premier signal d'horloge (CLK1) ;

le quatrième transistor à couches minces (T4) présente une grille connectée à l'entrée pour un second signal d'horloge (CLK2), et une source connectée à la sortie de second niveau de l'alimentation électrique de commande ;

le premier condensateur d'amorçage (C1) est connecté entre la grille et la source du troisième transistor à couches minces (T3) ;

la grille du premier transistor à couches minces (T1) est une entrée, et la source du troisième transistor à couches minces (T3) est la sortie pour le signal de commande de grille (G[n]) du module de contrôle de grille (11), et

caractérisé en outre par fait que le module de contrôle d'émission (12) comprend un cinquième transistor à couches minces (T5), un sixième transistor à couches minces (T6), un septième transistor à couches minces (T7), un huitième transistor à couches minces (T8), et un second condensateur d'amorçage (C2), dans lequel

le cinquième transistor à couches minces (T5) présente une grille connectée à la sortie pour le signal de commande de grille (G[n+1]) de l'unité de commande de ligne pour substrat de matrice d'étage suivant, une source connectée à un drain du sixième transistor à couches minces (T6), et un drain connecté au premier niveau de sortie de l'alimentation électrique de commande ;

le sixième transistor à couches minces (T6) présente une grille connectée au drain du quatrième transistor à couches minces (T4), et une source connectée au second niveau de sortie de l'alimentation électrique de commande ;

le septième transistor à couches minces (T7) présente une grille connectée à la source du cinquième transistor à couches minces (T5), une source connectée à un drain du huitième transistor à couches minces (T8), et un drain connecté au premier niveau de sortie de l'alimentation électrique de commande ;

le huitième transistor à couches minces (T8) présente une grille connectée à la grille du sixième transistor à couches minces (T6), et une source connectée au second niveau de sortie de l'alimentation électrique de commande ;

le second condensateur d'amorçage (C2) est connecté entre la grille et la source du septième transistor à couches minces (T7), et

la source du septième transistor à couches minces (T7) est la sortie pour le signal de contrôle d'émission (EMISSION[n]).

2. Circuit de commande de ligne pour substrat de matrice selon la revendication 1, dans lequel

la sortie de premier niveau de l'alimentation électrique de commande est une sortie de niveau bas ;

la sortie de second niveau de l'alimentation électrique de commande est une sortie de niveau haut, et

le premier transistor à couches minces (T1), le deuxième transistor à couches minces (T2), le troisième transistor à couches minces (T3), et le quatrième transistor à couches minces (T4) sont des transistors à couches minces de type p.

3. Circuit de commande de ligne pour substrat de matrice selon la revendication 2, dans lequel

la sortie de premier niveau de l'alimentation électrique de commande est une sortie de niveau bas ;

la sortie de second niveau de l'alimentation électrique de commande est une sortie de niveau haut, et

le cinquième transistor à couches minces (T5), le sixième transistor à couches minces (T6), le septième transistor à couches minces (T7), et le huitième transistor à couches minces (T8) sont des transistors à couches minces de type p.

4. Circuit de commande de ligne pour substrat de matrice selon la revendication 1, dans lequel

la sortie de premier niveau de l'alimentation électrique de commande est une sortie de niveau haut ;

la sortie de second niveau de l'alimentation électrique de commande est une sortie de niveau bas, et

le premier transistor à couches minces (T1), le deuxième transistor à couches minces (T2), le troisième transistor à couches minces (T3), et le quatrième transistor à couches minces (T4) sont des transistors à couches minces de type n.

5. Circuit de commande de ligne pour substrat de matrice selon la revendication 4, dans lequel
la sortie de premier niveau de l'alimentation électrique de commande est une sortie de niveau haut ;
la sortie de second niveau de l'alimentation électrique de commande est une sortie de niveau bas, et
le cinquième transistor à couches minces (T5), le sixième transistor à couches minces (T6), le septième transistor à couches minces (T7), et le huitième transistor à couches minces (T8) sont des transistors à couches minces de type n.

6. Circuit de commande de ligne pour substrat de matrice selon l'une quelconque des revendications 1 à 5, dans lequel le circuit de commande de ligne pour substrat de matrice est fabriqué sur le substrat de matrice d'un affichage à diode électroluminescente organique par le biais d'un processus de formation de couche de matrice, dans lequel
à l'exception de l'unité de commande de ligne pour substrat de matrice de premier étage, une entrée de chaque étage des unités de commande de ligne pour substrat de matrice est connectée à la sortie pour le signal de commande de grille de l'unité de commande de ligne pour substrat de matrice d'étage précédent, et
à l'exception de l'unité de commande de ligne pour substrat de matrice d'étage final, une borne de réinitialisation de chaque étage des unités de commande de ligne pour substrat de matrice est connectée à la sortie pour le signal de commande de grille de l'unité de commande de ligne pour substrat de matrice d'étage suivant adjacente à l'unité de commande de ligne pour substrat de matrice d'étage actuel.

7. Dispositif d'affichage comprenant le circuit de commande de ligne pour substrat de matrice selon la revendication 6.

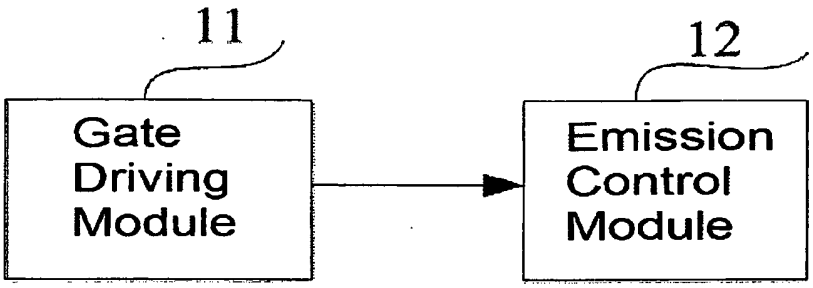

Figure 1

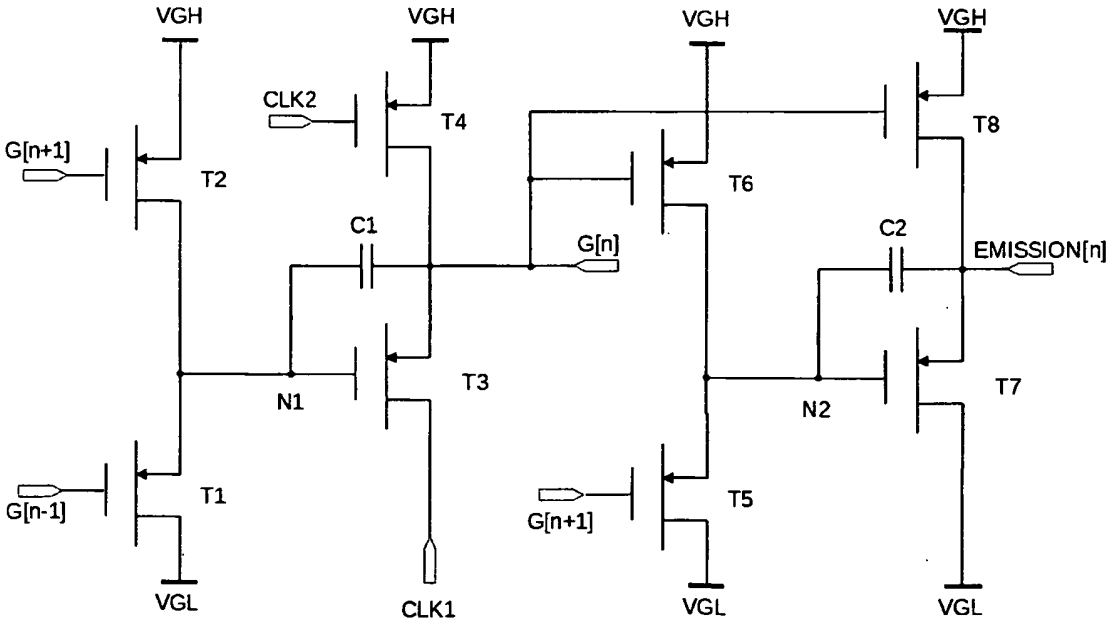

Figure 2

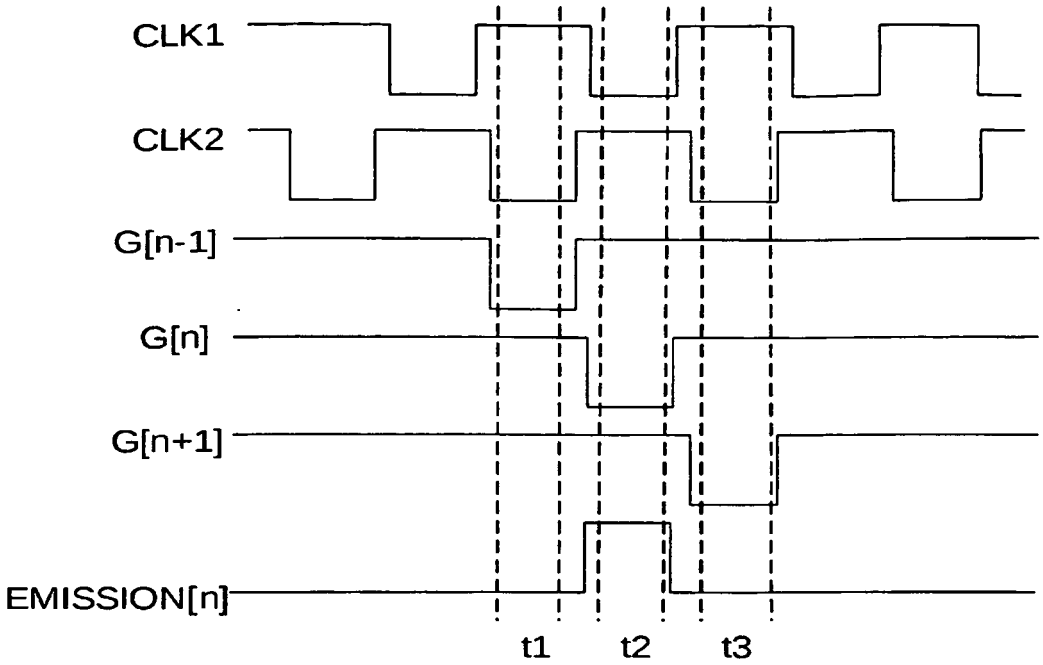

Figure 3

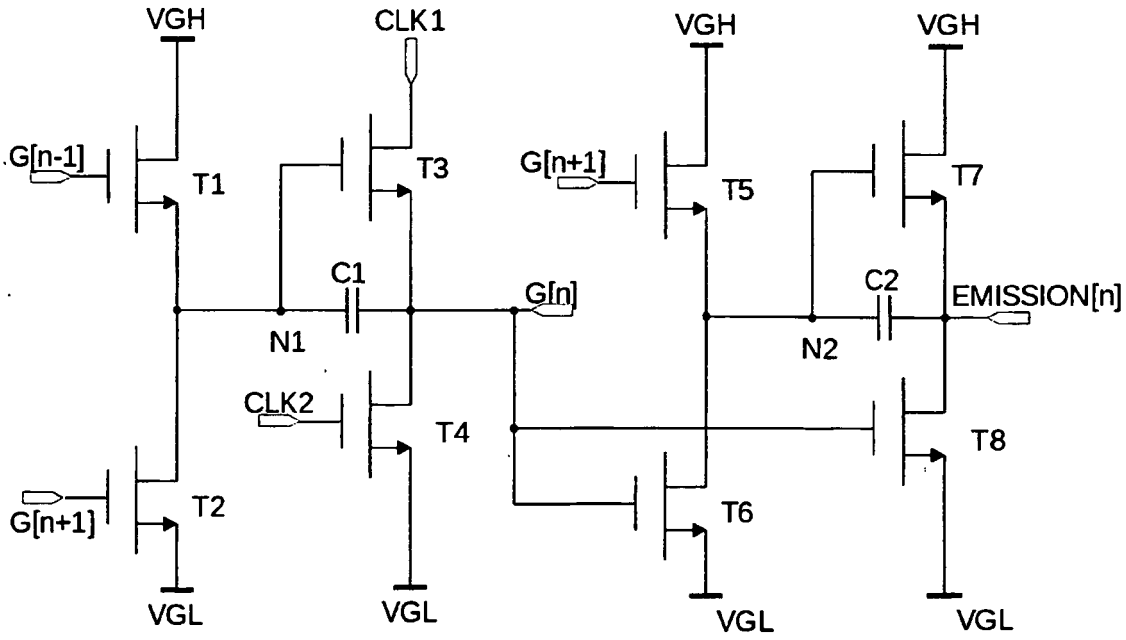

Figure 4

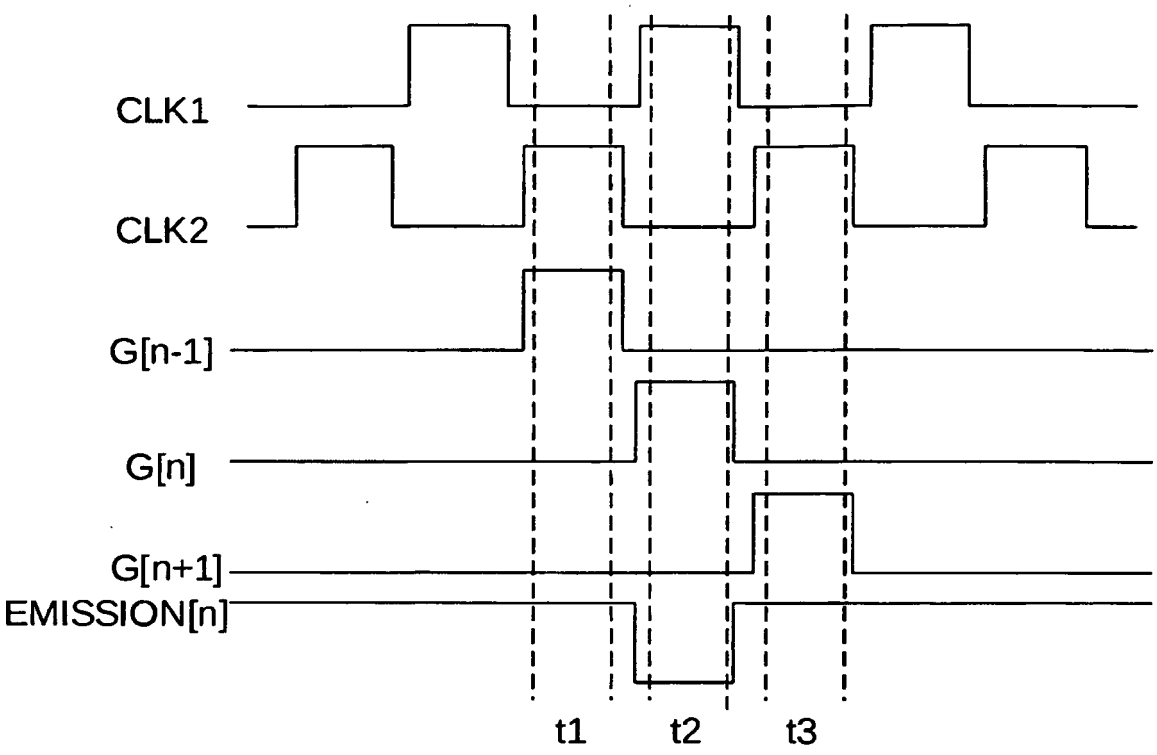

Figure 5

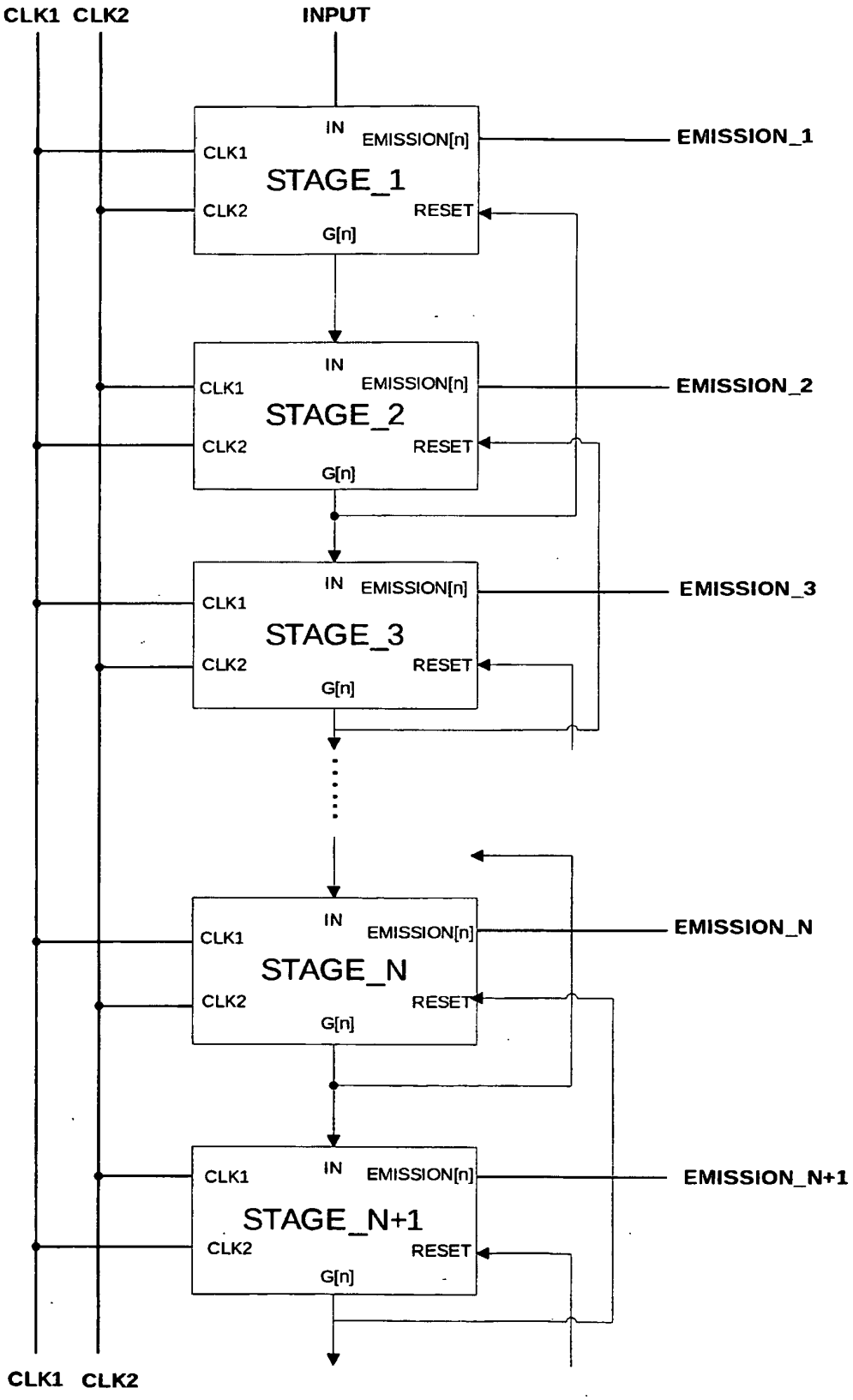
CLK1
CLK2
INPUT
IN
EMISSION[n]
CLK1
STAGE_1
CLK2
RESET
G[n]
EMISSION_1
STAGE_2
EMISSION_2
STAGE_3
EMISSION_3
STAGE_N
EMISSION_N
STAGE_N+1
EMISSION_N+1

Figure 6

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1843317 A1 **[0005]**
- US 2011012823 A1 **[0006]**
- US 2006001637 A1 **[0007]**

专利名称(译)	阵列驱动器单元上的栅极，阵列驱动器电路上的栅极和显示器件		
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[标]申请(专利权)人(译)	京东方科技集团股份有限公司		
申请(专利权)人(译)	京东方科技集团有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司.		
[标]发明人	KIM TAE GYU WANG YING KIM PIL SEOK		
发明人	KIM, TAE GYU WANG, YING KIM, PIL SEOK		
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优先权	201210050062.4 2012-02-29 CN		
其他公开文献	EP2672479A1 EP2672479A4		
外部链接	Espacenet		

摘要(译)

本发明提供一种阵列基板行驱动单元，阵列基板行驱动电路和显示装置。阵列基板行驱动单元包括用于产生栅极驱动信号的栅极驱动模块和发射控制模块;发光控制模块，连接到栅极驱动模块的栅极驱动信号的输出，用于在栅极驱动信号的控制下产生用于控制OLED的开关的发光控制信号，栅极驱动信号具有与栅极驱动信号相反的相位。发射控制信号。

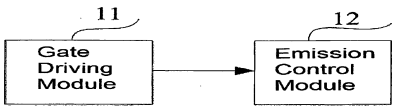

Figure 1

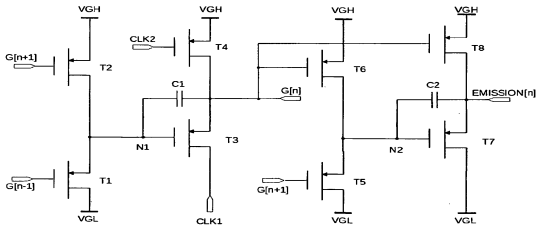

Figure 2