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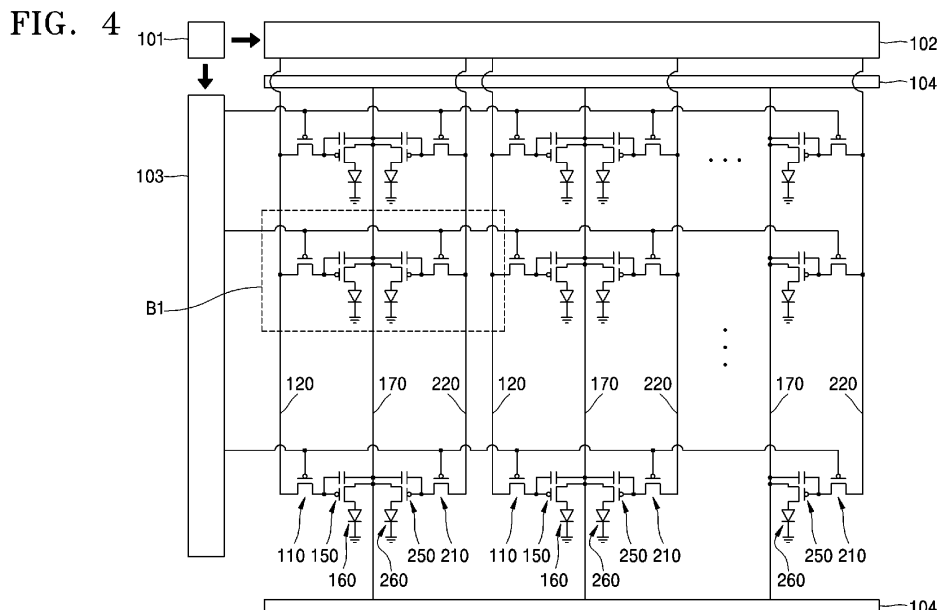
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(54) **Active matrix electroluminescent display device**

(57) Provided is an active matrix electroluminescent display apparatus in which a short circuit between a power line (170) and data line (120) in adjacent sub-pixels can be substantially substantially prevented. The active matrix electroluminescent display apparatus includes: a power line (170); a first transistor positioned (150) on a

side of the power line (170) and connected to the power line; a second transistor (250) positioned on the other side of the power line (170) and connected to the power line (170); and electroluminescent devices (160,260) respectively connected to the first transistor (150) and the second transistor (250).



## Description

### CROSS-REFERENCE TO RELATED PATENT APPLI- CATIONS

**[0001]** This application claims the benefit of Korean Patent Application No. 10-2004-0048648, filed on June 26, 2004, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

**[0002]** The present invention relates to an active matrix electroluminescent display apparatus, and more particularly, to an active matrix electroluminescent display apparatus in which a short circuit between a power line and a data line in adjacent sub-pixels is substantially prevented.

#### 2. Description of the Related Technology

**[0003]** FIG. 1 is a circuit diagram of a conventional active matrix electroluminescent display apparatus. FIG. 2 is an enlarged circuit diagram of a portion "A" of FIG. 1. FIG. 3 is an enlarged layout view of the portion "A" of FIG. 1.

**[0004]** Referring to FIGS. 1 through 3, a gate electrode 11 of a switching transistor 10 is connected to a scan line 30 connected to a scan driver (not shown), one electrode 12 of the switching transistor 10 is connected to a data line 20 connected to a data driver (not shown), the other electrode 13 of the switching transistor 10 is connected to a gate electrode 51 of a driving transistor 50 and a first capacitor electrode 41 of a storage capacitor 40, a second capacitor electrode 42 of the storage capacitor 40 and one electrode 52 of the driving transistor 50 is connected to a power line 70, and the other electrode 53 of the driving transistor 50 is connected to a pixel electrode 61 of an electroluminescent device 60.

**[0005]** When a scan signal is applied to the gate electrodes 11 of the switching transistors 10 in a selected row connected to scan lines 30, current flows from the one electrode 12 to the other electrode 13 of transistor 10. In this case, current is provided to the electrodes 12 of only the selected switching transistors 10 through the data lines 20sub-pixel.

**[0006]** In this case, current flowing in each selected sub-pixel emitting light is supplied through the power line 70. Therefore, a constant voltage is applied to the power line 70sub-pixel.

**[0007]** However, in this conventional structure, the data line 20 and the power line 70 are arranged as a pair in close proximity to each other, so that a short circuit is likely to occur between the data line 20 and the power line 70. When a short circuit occurs between the data line

20 and the power line 70 the proper data cannot be driven onto data line 20. As a result, sub-pixels which have not to be selected are erroneously selected and emit light .

### 5 SUMMARY OF CERTAIN INVENTIVE ASPECTS

**[0008]** The present invention provides an active matrix electroluminescent display apparatus in which a short circuit between a power interconnection line and a data line in adjacent sub-pixels can be substantially prevented.

**[0009]** According to an aspect of the present invention, there is provided an active matrix electroluminescent display apparatus including: first and second electroluminescent devices, a first transistor positioned adjacent to the first transistor and connected to the second electroluminescent device, and a power line positioned between the first and second transistors. The power line is configured to provide current to the first and second transistors

**[0010]** The apparatus may further include: a third transistor electrically connected to the first transistor; and a fourth transistor electrically connected to the second transistor.

**[0011]** The apparatus may further include: a first line electrically connected to the third transistor; and a second line electrically connected to the fourth transistor.

**[0012]** The apparatus may further include a first sub-pixel including the first transistor, the electroluminescent device electrically connected to the first transistor, and the third transistor is interposed between the power line and the first line; and a second sub-pixel including the second transistor, the electroluminescent device electrically connected to the second transistor, and the fourth transistor is interposed between the power line and the second line.

**[0013]** The first sub-pixel and the second sub-pixel may be symmetric with respect to the power line.

**[0014]** The first transistor and the second transistor may have different sizes.

**[0015]** The electroluminescent devices electrically connected to the first transistor and the second transistor may have different sizes.

**[0016]** According to another aspect of the present invention, there is provided an active matrix electroluminescent display apparatus including: first and second electroluminescent devices, a first transistor connected to the first electroluminescent device, a second transistor positioned adjacent to the first transistor and connected to the second electroluminescent device, and first and second substantially parallel power lines positioned between the first and second transistors. The first power line is configured to provide current to the first transistor and the second power line is configured to provide current to the second transistor.

**[0017]** The apparatus may further include: a third transistor electrically connected to the first transistor; and a fourth transistor electrically connected to the second tran-

sistor.

**[0018]** The apparatus may further include: a first line electrically connected to the third transistor; and a second line electrically connected to the fourth transistor.

**[0019]** The apparatus may further include: a first sub-pixel comprising the first transistor, the electroluminescent device electrically connected to the first transistor, and the third transistor is positioned between the first power line and the first line; and a second sub-pixel comprising the second transistor, the electroluminescent device electrically connected to the second transistor, and the fourth transistor is positioned between the second power line and the second line.

**[0020]** The first sub-pixel and the second sub-pixel may be symmetric with respect to the first power line and the second power line.

**[0021]** The first transistor and the second transistor may have different sizes.

**[0022]** The electroluminescent devices electrically connected to the first transistor and the second transistor may have different sizes.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0023]** Embodiments of the present invention will be described with reference to the attached drawings.

FIG. 1 is a circuit diagram of a conventional active matrix electroluminescent display apparatus (Prior Art);

FIG. 2 is an enlarged circuit diagram of a portion A of FIG. 1 (Prior Art);

FIG. 3 is an enlarged layout view of the portion A of FIG. 1 (Prior Art);

FIG. 4 is a circuit diagram of an active matrix electroluminescent display apparatus according to an embodiment of the present invention;

FIG. 5 is an enlarged circuit diagram of a portion B1 of FIG. 4;

FIG. 6 is an enlarged layout view of the portion B1 of FIG. 4;

FIG. 7 is a cross-sectional view taken along a line connecting points P1 through P12 of FIG. 6;

FIG. 8 is a modified circuit diagram of the portion B1 in FIG. 5;

FIG. 9 is a cross-sectional view of an active matrix electroluminescent display apparatus including the portion B1 in FIG. 8;

FIG. 10 is a cross-sectional view of an active matrix electroluminescent display apparatus having a structure modified from the structure in FIG. 7;

FIG. 11 is a circuit diagram of an active matrix electroluminescent display apparatus according to another embodiment of the present invention;

FIG. 12 is an enlarged circuit diagram of a portion B2 of FIG. 11;

FIG. 13 is an enlarged layout view of the portion B2 of FIG. 11;

FIG. 14 is a cross-sectional view taken along a line connecting Q1 through Q13 of FIG. 13;

FIG. 15 is a circuit diagram of an active matrix electroluminescent display apparatus modified from the structure in FIG. 4;

FIG. 16 is an enlarged circuit diagram of a portion B3 of FIG. 15;

FIG. 17 is a circuit diagram of an active matrix electroluminescent display apparatus modified from the structure in FIG. 11; and

FIG. 18 is an enlarged circuit diagram of a portion B4 of FIG. 17.

#### DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

**[0024]** The following detailed description is directed to certain specific embodiments of the invention. However, the invention can be embodied in a multitude of different ways. In this description, reference is made to the drawings wherein like parts are designated with like numerals throughout. The term "on" as used herein is does not necessarily mean physically touching. FIG. 4 is a circuit diagram of an active matrix electroluminescent display apparatus according to an embodiment of the present invention. FIG. 5 is an enlarged circuit diagram of a portion B1 of FIG. 4. FIG. 6 is an enlarged layout view of the portion B1 of FIG. 4. FIG. 7 is a cross-sectional view taken along a line connecting points P1 through P12 of FIG. 6.

**[0025]** Such an apparatus may be used in cell phones, televisions, computer monitors, and game displays.

**[0026]** Electroluminescence display apparatuses include various pixel arrangements according to the color of light generated in their emission layer. For example, each pixel includes red, green, and blue sub-pixels. Each sub-pixel in such an electroluminescent display apparatus is a current-driven electroluminescent device emitting light of red, green, or blue color as current flows electroded through it in order to form part of a predetermined image.

**[0027]** An electroluminescent display apparatus may include a pixel electrode, an intermediate layer including at least an emissive layer formed above the pixel electrode, and an opposite electrode formed above the intermediate layer. However, the present invention is not limited to this structure, and electroluminescent display apparatuses according to the present invention may have various structures.

**[0028]** Referring to FIG. 5, a first transistor 150 and the second transistor 250 are positioned on opposing sides of a power line 170, and are connected to the power line 170. An electroluminescent device 160 is electrically connected to the first transistor 150, and an electroluminescent device 260 is electrically connected to the second transistor 250. That is, adjacent sub-pixels arranged adjacent to the power line 170 share one power line 170.

**[0029]** Since two sub-pixels share one power line 170,

the power line 170 is not adjacent to other lines for selecting sub-pixels. Accordingly, a short circuit between the power line 170 and other lines and a malfunction of sub-pixels can be substantially prevented.

**[0030]** Referring to FIG. 5, a third transistor 110 is further electrically connected to the first transistor 150. A fourth transistor 210 is further electrically connected to the second transistor 250. A first storage capacitor 140 is further electrically connected to the first transistor 150 and the third transistor 110. A second storage capacitor 240 is electrically connected to the second transistor 250 and the fourth transistor 210. In this case, a first line 120, a second line 220, and a third line 130 are further formed. The first line 120 is electrically connected to the third transistor 110, and the second line 220 is electrically connected to the fourth transistor 210. The third line 130 is electrically connected to the third transistor 110 and the fourth transistor 210.

**[0031]** The structure will be described in detail. A fifth electrode 112 of the third transistor 110 is connected to a driving circuit (not shown) by the first line 120, a third gate electrode 111 of the third transistor 110 is connected to a driving circuit by the third line 130, and a sixth electrode 113 of the third transistor 110 is connected to a first capacitor electrode 141 of the first storage capacitor 140 and a first gate electrode 151 of the first transistor 150.

**[0032]** A seventh electrode 212 of the fourth transistor 210 is connected to a driving circuit (not shown) by the second line 220, a fourth gate electrode 211 of the fourth transistor 210 is connected to a driving circuit (not shown) by the third line 130, an eighth electrode 213 of the fourth transistor 210 is connected to a first capacitor electrode 241 of the second storage capacitor 240 and a second gate electrode 251 of the second transistor 250.

**[0033]** In the above structure, the first line 120 and the second line 220 may be data lines for transmitting data signal, the third line 130 may be a scan line. In this case, the third transistor 110 and the fourth transistor 210 may act as switching transistors (TRs), and the first transistor 150 and the second transistor 250 may act as driving TRs. In a circuit having such a structure described above each sub-pixel may comprise at least two TRs and an electroluminescent device. Hereafter, a structure in which two transistors, i.e., a switching TR and a driving TR, and an electroluminescent device will be described, but the present invention is not limited to this embodiment.

**[0034]** A second capacitor electrode 142 of the first storage capacitor 140 and a first electrode 152 of the first TR 150 are connected to the power line 170, and a second electrode 153 of the first TR 150 is connected to a pixel electrode 161 of the electroluminescent device 160. As illustrated in FIG. 7, the electroluminescent device 160 electrodecomprises an intermediate layer 187 including at least an emissive layer is interposed between the pixel electrode 161 and the opposite electrode 162.

**[0035]** A second capacitor electrode 242 of the second

storage capacitor 240 and a third electrode 252 of the second TR 250 are connected to the power line 170, and a fourth electrode 253 of the second TR 250 is connected to a pixel electrode 261 of the electroluminescent device 260. The structure of the electroluminescent device 260 is the same as described above.

**[0036]** FIGS. 6 and 7 illustrate a structure of the portion B1 of FIG. 4. FIG. 6 illustrates the first line 120, the second line 220, the third gate electrode 111, the fifth electrode 112, the sixth electrode 113, the fourth gate electrode 211, the seventh electrode 212, the eighth electrode 213, and the third line 130, which are not illustrated in FIG. 7. FIG. 7 illustrates a substrate 181, a buffer layer 182, a gate dielectric layer 183, an interlayer insulating layer 184, a first protecting layer 185, the opposite electrode 162, and a second protecting layer 189, which are not illustrated in FIG. 6.

**[0037]** When a scan signal is applied to the third gate electrode 111 by a driving circuit, a channel is formed in a semiconductor layer connecting the fifth electrode 112 and the sixth electrode 113, a data signal is transmitted through this channel from the first line 120 to the first capacitor 140 and the first TR 150. In response, a channel is formed in a semiconductor layer connecting the first electrode 152 and the second electrode 153, and a signal is transmitted through this channel from the power line 170 to the pixel electrode 161 of the electroluminescent device 160.

**[0038]** When a scan signal is applied to the fourth gate electrode 211 by the driving circuit, a conductive channel is formed in a semiconductor layer connecting the seventh electrode 212 and the eighth electrode 213, and a data signal is transmitted through this channel from the second line 220 to the second capacitor 240 and the second TR 250. In response, a channel is formed in a semiconductor layer connecting the third electrode 252 and the fourth electrode 253, and a signal is transmitted through this channel from the power line 170 to the pixel electrode 261 of the electroluminescent device 260.

**[0039]** A detailed structure of each sub-pixel will be described with reference to FIG. 7. Referring to FIG. 7, the electroluminescent device 160 is illustrated between P1 and P2, the electroluminescent device 260 is illustrated between P11 and P12, the first TR 150 is illustrated between P2 and P3, the second TR 250 is illustrated between P10 and P11, the first storage capacitor 140 is illustrated between P3 and P6, and the second storage capacitor 240 is illustrated between P7 and P10.

**[0040]** A buffer layer 182 can be formed on the entire upper surface of the substrate 181 to substantially prevent permeation of impurities into semiconductor layers 180 and 280 from the substrate 181 and to improve the surface evenness of the substrate 181. In this case, the first TR 150 and the second TR 250 are formed on the buffer layer 182. The first protecting layer 185 is formed to cover the first TR 150 and the second TR 250, and contact holes are formed in regions of the first protecting layer 185 that correspond to the second electrode 153

and the fourth electrode 253. Pixel electrodes 161 and 261 are formed in the regions including the contact holes. The pixel electrodes 161 and 261 are respectively connected to the second electrode 153 of the first TR 150 and the fourth electrode 153 of the second TR 250 through the contact holes formed in the first protecting layer 185.

**[0041]** Intermediate layers 187 and 287 including at least an emissive layer are respectively formed on the pixel electrodes 161 and 261. The opposite electrode 162 is formed on the intermediate layers 187 and 287. The second protecting layer 189 may be formed on the opposite electrode 162.

**[0042]** In a rear emission type electroluminescent device, the substrate 181, the buffer layer 182, the gate dielectric layer 183, the interlayer insulating layer 184, the first protecting layer 185, and the pixel electrodes 161 and 261 may be formed of transparent materials, and the opposite electrode 162 may be formed of a metal with a high reflectivity. Meanwhile, in a front emission type electroluminescent device, the pixel electrodes 161 and 261 may be formed of a metal with a high reflectivity, and the opposite electrode 162 and the second protecting layer 189 may be formed of transparent materials.

**[0043]** An electroluminescent device according to the present invention can be a rear emission type, a front emission type, or a double-side emission type. Light generated in these electroluminescent device may be externally emitted through at least one of the pixel electrodes 161 and 261 and the opposite electrode 162.

**[0044]** A transparent material for the pixel electrodes 161 and 261 may be ITO, IZO, ZnO or  $\text{In}_2\text{O}_3$ . When the pixel electrodes 161 and 261 are used as reflective electrodes, the pixel electrodes 161 and 261 can be formed by forming a reflecting layer using Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr or a compound of the foregoing materials and depositing ITO, IZO, ZnO or  $\text{In}_2\text{O}_3$  on the reflecting layer. The pixel electrodes 161 and 261 may have a pattern corresponding to a pattern of pixels as illustrated in FIGS. 4 through 7.

**[0045]** When a transparent material is used to form the opposite electrode 162, the opposite electrode 162 can be formed by depositing Li, Ca, LiF/Ca, LiF/Al, Al, Ag, Mg, or a compound of the foregoing materials on the intermediate layer 187 and forming on the intermediate layer 187 an auxiliary electrode line or a bus electrode line using a transparent material, such as ITO, IZO, ZnO,  $\text{In}_2\text{O}_3$ , or the like. When the opposite electrode 162 is used as a reflective electrode, Li, Ca, LiF/Ca, LiF/Al, Al, Ag, Mg, or a compound of the foregoing materials is formed on the entire surface of display apparatuses. However, materials for the pixel electrodes 161 and 261 and the opposite electrode 162 are not limited to the above, and organic materials, such as a conductive polymer, can be used to form the pixel electrodes 161 and 261 and the opposite electrode 162. In addition, the opposite electrode 162 may be formed to cover all the pixels or to correspond to each of the pixels.

**[0046]** The electroluminescent devices 160 and 260 include the intermediate layers 187 and 287, respectively, between the pixel electrodes 161 and 261, which are electrically connected to the second electrode 153 of the first TR 150 and the fourth electrode 253 of the second TR 250, respectively, and the opposite electrode 162 facing the pixel electrodes 161 and 261. Each of the electroluminescent devices is categorized into either an organic electroluminescent device or an inorganic electroluminescent device according to the material used to form the intermediate layer 187.

**[0047]** In organic electroluminescent devices, the intermediate layer 187 is may be composed of a low molecular weight organic material layer or a large molecular weight organic material layer.

**[0048]** When a low molecular weight organic material layer is used, the intermediate layer 187 may be formed of a layer selected from among a hole injection layer (HIL), a hole transport layer (HTL), an emission layer (EML), an electron transport layer (ETL), an electron injection layer (EIL), or a composite layer of these layers. Examples of the low molecular weight organic material that can be used may include copper phthalocyanine (CuPc), N,N'-Di(naphthalene-1-yl)-N,N'-diphenyl-benzidine (NPB), tris-8-hydroxyquinoline aluminum (Alq3), and the like.

**[0049]** Such a low molecular weight organic material layer can be formed by thermally depositing an organic material in a vacuum condition. However, the structure of the intermediate layer 187 formed using such a low molecular weight organic material is not limited to the above and can be varied into various structures if required. When a large molecular weight organic material layer is used, the intermediate layer 187 may include a HTL and an EML. A large molecular weight HTL may be formed using poly-(2,4)-ethylene-dihydroxy thiophene (PEDOT), polyaniline (PANI), or the like by inkjet-printing or spin-coating. A large molecular weight EML may be formed as a color pattern using PPV, soluble PPV, cyano-PPV, polyfluorene, or the like by inkjet-printing, spin-coating, thermal transferring using laser, etc. However, the structure of the intermediate layer 187 formed of such a large molecular weight organic layer is not limited to the above and can be varied into various structures if required.

**[0050]** In inorganic electroluminescent devices, the intermediate layer 187 is composed of an inorganic material. The intermediate layer 187 may include an EML and an insulating layer interposed between the EML and the electrode. However, the structure of the intermediate layer 187 is not limited to this structure and can be varied into various structures if required.

**[0051]** The EML of the inorganic electroluminescent device may be composed of a metal sulfide, such as ZnS, SrS, CaS, etc.; alkali earth potassium sulfide, such as  $\text{CaGa}_2\text{S}_4$ ,  $\text{SrGa}_2\text{S}_4$ , etc.; or a transition metal, such as Mn, Ce, Tb, Eu, Tm, Er, Pr, Pb, etc. or an alkali rare earth metal.

**[0052]** The first storage capacitor 140 includes the first capacitor electrode 141 and the second capacitor electrode 142. The first capacitor electrode 141 can be integrally formed with the first gate electrode 151. The second capacitor electrode 142 can be integrally formed with the first electrode 152. The second storage capacitor 240 includes the first capacitor electrode 241 and the second capacitor electrode 242. The first capacitor electrode 241 can be integrally formed with the second gate electrode 251. The second capacitor electrode 242 can be integrally formed with the third electrode 252 in a single body. In the present embodiment, two adjacent sub-pixels on opposite sides of the power line 170 share the one power line 170. Therefore, the second capacitor electrode 142 of the first capacitor 140 and the second capacitor electrode 242 of the second capacitor 240 can be integrally formed, as illustrated in FIGS. 6 and 7. The storage capacitors 140 and 240 maintain signals to the pixel electrodes 161 and 261.

**[0053]** In the above-described structures, the electroluminescent devices 160 and 260 may be formed within gaps in the pixel defining layer 186, the gaps defining emitting regions. As illustrated in FIG. 7, the pixel defining layer 186 is formed electrodeelectrodesubstantially preventelectrodesubstantially preventabove intermediate layers 187 and 287. The gaps in the pixel defining layer 186 can then be formed so that they are smaller than the width of the pixel electrodes 161 and 261. The intermediate layers 187 and 287 and the opposite electrode 162 are formed within the gaps. This structure minimizes the electric field strength between the edges of the pixel electrodes 161 and 261 and the opposite electrode 162, and therefore substantially preventing a short circuit between the pixel electrodes 161 and 261 and the opposite electrode 162.

**[0054]** In the above-described structure, two adjacent sub-pixels on opposite sides of power line 170 share the one power line 170 so that the power line 170 is not adjacent to other lines for selecting sub-pixels, in particular, the first and second lines 120 and 220, which can be used as data lines. Therefore, a short circuit between the power line 170 and other lines, such as the first line 120 and the second line 220, can be substantially prevented, thus substantially preventing a malfunction of sub-pixels. Due to the structure described above, the number of power lines is reduced by half of that of conventional active matrix electroluminescent display apparatuses, thereby resulting in a simplified interconnection structure. A first sub-pixel including the first TR 150, the third TR 110, and the electroluminescent device 160 electrically connected to the first TR 150 may be interposed between the power line 170 and the first line 120. A second sub-pixel including the second TR 250, the fourth TR 210, and the electroluminescent device 260 electrically connected to the second TR 250 may be interposed between the power line 170 and the second line 220.

**[0055]** The first sub-pixel and the second sub-pixel may be symmetric about the power line 170, as illustrated

in FIGS. 6 and 7. However, the first sub-pixel and the second sub-pixel may be arranged in a way different from the above and are not limited thereto. For example, the first sub-pixel and the second sub-pixel may be arranged not to be symmetric.

**[0056]** FIG. 8 is a modified circuit diagram of FIG. 5, and FIG. 9 is a cross-sectional view of an active matrix electroluminescent display apparatus having the structure of FIG. 8. The active matrix electroluminescent display apparatus in FIGS. 8 and 9 differ from the active matrix electroluminescent display apparatuses in FIGS. 5 and 7 in that the first TR 150 and the second TRs 250 have different sizes. The electroluminescent devices 160 and 260 form images by emitting red, green, and blue light with a different luminous efficiency for each color of light. Accordingly, uniformity in, for example, luminous efficiency, can be improved by changing the size of the driving TR according to a high or low luminous efficiency.

**[0057]** FIG. 10 is a modified cross-sectional view of the active matrix electroluminescent display apparatus of FIG. 7. The active matrix electroluminescent display apparatus of FIG. 10 differs from the active matrix electroluminescent display apparatus of FIG. 7 in that the electroluminescent device 160 electrically connected to the first TR 150 and the electroluminescent device 260 electrically connected to the second TR 250 have different sizes. That is, the difference in luminous efficiency between different colors of light can be compensated for by changing the size of the electroluminescent device according to the luminous efficiency of each color of light.

**[0058]** The modifications illustrated in FIGS. 8, 9, and 10 can be applied to the following embodiments.

**[0059]** FIG. 11 is a circuit diagram of an active matrix electroluminescent display apparatus according to another embodiment of the present invention. FIG. 12 is an enlarged circuit diagram of a portion B2 of FIG. 11. FIG. 13 is an enlarged layout view of the portion B2 of FIG. 11. FIG. 14 is a cross-sectional view of sub-pixels of the active matrix electroluminescent display apparatus of FIG. 13 taken along a line connecting points Q1 through Q13.

**[0060]** Referring to FIG. 11, a first power line 370 and a second power line 470 are arranged parallel to each other. A first TR 350 is positioned on a side away from the second power line 470 and is electrically connected to the first power line 370. A second TR 450 is positioned on a side away from the first power line 370 and is electrically connected to the second power line 470. An electroluminescent device 360 and an electroluminescent device 460 are respectively electrically connected to the first TR 350 and the second TR 450. In the above-described structure, the power lines 370 and 470 respectively connected to sub-pixels are positioned parallel to each other.

**[0061]** As described above, the power lines 370 and 470 connected to two sub-pixels and are not adjacent to other lines for selecting sub-pixels. As a result, a short circuit between the power lines 370 and 470 and the other

lines is substantially prevented, thus substantially preventing a malfunction of sub-pixels. Also, in the above-described structure, since the same voltage is applied to the power line 370 and the power line 470, there is no concern about a malfunction due to a short circuit between the power line 370 and the power line 470.

**[0062]** Referring to FIGS. 11 and 12, a third TR 310 electrically connected to the first TR 350 and a fourth TR 410 electrically connected to the second TR 450 are further included. A first storage capacitor 340 electrically connected to the first TR 350 and the third TR 310, and a second storage capacitor 440 electrically connected to the second TR 450 and the fourth TR 410 are further included. In this structure, a first line 320, a second line 420, and a third line 330 are further formed, wherein the first line 320 is connected to the third TR 310, and the second line 420 is connected to the fourth TR 410.

**[0063]** This structure will be described in detail with reference to FIGS. 12 and 13. A fifth electrode 312 of the third TR 310 is connected to a driving circuit (not shown) by the first line 320, a third gate electrode 311 of the third TR 310 is connected to a driving circuit (not shown) by the third line 330, and a sixth electrode 313 of the third TR 310 is electrically connected to a first capacitor electrode 341 of the first storage capacitor 340 and a gate electrode 351 of the first TR 350.

**[0064]** A seventh electrode 412 of the fourth TR 410 is connected to a driving circuit (not shown) by the second line 420, a fourth gate electrode 411 of the fourth TR 410 is connected to a driving circuit (not shown) by the third line 330, and an eighth electrode 413 of the fourth TR 410 is electrically connected to a first capacitor electrode 441 of the second storage capacitor 440 and a second gate electrode 451 of the second TR 450.

**[0065]** In such a structure described above, the first line 320 and the second line 420 may correspond to data lines for transmitting data, and the third line 330 may correspond to a scan line. In this case, the third TR 310 and the fourth TR 410 may act as switching TRs, and the first TR 350 and the second TR 450 may act as driving TRs. In such a circuit described above each sub-pixel may comprise at least two TRs and an electroluminescent device. Hereinafter, a case where two TRs, i.e., a switching TR and a driving TR, and an electroluminescent device, will be described.

**[0066]** A second capacitor electrode 342 of the first storage capacitor 340 and a first electrode 352 of the first TR 350 are connected to the first power line 370, and a second electrode 353 of the first TR 350 is connected to a pixel electrode 361 of the electroluminescent device 360. As illustrated in FIG. 14, an opposite electrode 362 of the electroluminescent device electrodecomprises an intermediate layer 387 including at least an emission layer is interposed between the pixel electrode 361 and the opposite electrode 362.

**[0067]** A second capacitor electrode 442 of the second storage capacitor 440 and a third electrode 452 of the second TR 450 are connected to the second power line

470, and a fourth electrode 453 of the second TR 450 is connected to a pixel electrode 461 of the electroluminescent device 460. The electroluminescent device 460 may have the same structure as in the embodiment described above, and the principle of driving each sub-pixel may also be the same as in the embodiment described above.

**[0068]** A detailed structure of each sub-pixel will be described in brief with reference to FIG. 14. Referring to FIG. 14, the electroluminescent device 360 is illustrated between Q1 and Q2, the electroluminescent device 460 is illustrated between Q12 and Q13, the first TR 350 is illustrated between Q2 and Q3, the second TR 450 is illustrated between Q11 and Q12, the first storage capacitor 340 is illustrated between Q3 and Q7, and the second storage capacitor 440 is illustrated between Q7 and Q11.

**[0069]** In some embodiments two adjacent sub-pixels are respectively connected to separate power lines-sub-pixel. Unlike the illustration in FIG. 7, which is a cross-sectional view of the active matrix electroluminescent display apparatus according to a first embodiment of the present invention described above, referring to FIG. 14, which is a cross-sectional view of the active matrix electroluminescent display apparatus according to another embodiment of the invention, the second capacitor electrode 342 of the first storage capacitor 340 and the second storage capacitor electrode 442 of the second storage capacitor 440 are separated from each other, not integrally connected. Except for this structural difference, the active matrix electroluminescent display apparatus according to the present embodiment is structurally the same as the active matrix electroluminescent display apparatus according to the first embodiment described above.

**[0070]** As described above, the power line 370 and the power line 470, which are respectively connected to two sub-pixels are not adjacent to lines for selecting sub-pixels. Therefore, a short circuit between the power lines 370 and 470 and the other lines is substantially prevented, thus substantially preventing a malfunction of sub-pixels. Also, in the above-described structure, since the same voltage is applied to the power line 370 and the power line 470, there is no concern about a malfunction due to a short circuit between the power line 370 and the power line 470.

**[0071]** A first sub-pixel including the first TR 350, the third TR 310, and the electroluminescent device 360 electrically connected to the first TR 350 can be interposed between the first power line 370 and the first line 320. A second sub-pixel including the second TR 450, the fourth TR 410, and the electroluminescent device 460 electrically connected to the second TR 450 can be interposed between the second power line 470 and the second line 420. In this case, the first sub-pixel and the second sub-pixel can be symmetric about the first line 370 and the second line 470. However, the first sub-pixel and the second sub-pixel may be positioned in other ways. The first sub-pixel and the second sub-pixel may

or may not be symmetric.

**[0072]** Although all the TRs electrically connected to the electroluminescent devices in FIGS. 4 through 14 are p type TRs, the present invention is not limited to this. In other words, as illustrated in FIGS. 15 through 18, n-type TRs can be connected to an electroluminescent device. Alternatively, both n-type and p-type TRs can be connected to an electroluminescent device. Other various modifications are possible.

**[0073]** An active matrix electroluminescent display apparatus according to the present invention constructed as described above provide the following benefits.

**[0074]** First, two adjacent sub-pixels may share one line so that a short circuit between the power line and other lines, such as a data line, can be substantially prevented.

**[0075]** Second, since a short circuit between the power interconnection and other lines, such as a data line, can be substantially prevented, a malfunction, such as luminescence of an unselected sub-pixel, can be substantially prevented, enabling an original image to be more clearly displayed.

**[0076]** Third, since adjacent two sub-pixels may share one power line, the number of power lines can be reduced by half, thereby resulting in a simplified line structure.

**[0077]** Fourth, by arranging power lines, which are respectively connected to two adjacent sub-pixels, to be close to each other, a short circuit between the power lines and other lines, such as a data line, can be substantially prevented.

**[0078]** While the above description has pointed out novel features of the invention as applied to various embodiments, the skilled person will understand that various omissions, substitutions, and changes in the form and details of the device or process illustrated may be made without departing from the scope of the invention. Therefore, the scope of the invention is defined by the appended claims rather than by the foregoing description. All variations coming within the meaning and range of equivalency of the claims are embraced within their scope.

## Claims

1. An active matrix electroluminescent display apparatus comprising:
  - first and second electroluminescent devices;
  - a first transistor connected to the first electroluminescent device;
  - a second transistor positioned adjacent to the first transistor and connected to the second electroluminescent device; and
  - a power line positioned between the first and second transistors, wherein the power line is configured to provide current to the first and second transistors.
2. The apparatus of claim 1, further comprising:
  - a third transistor electrically connected to the first transistor; and
  - a fourth transistor electrically connected to the second transistor.
3. The apparatus of claim 2, further comprising:
  - a first line electrically connected to the third transistor; and
  - a second line electrically connected to the fourth transistor.
4. The apparatus of claim 3, wherein a first sub-pixel including the first transistor, the electroluminescent device electrically connected to the first transistor, and the third transistor is positioned between the power line and the first line, and a second sub-pixel including the second transistor, the electroluminescent device electrically connected to the second transistor, and the fourth transistor is positioned between the power line and the second line.
5. The apparatus of claim 4, wherein the first sub-pixel and the second sub-pixel are symmetric about the power line.
6. The apparatus of claim 1, wherein the first transistor and the second transistors have different sizes.
7. The apparatus of claim 1, wherein the electroluminescent device electrically connected to the first transistor and the electroluminescent device electrically connected to the second transistor have different sizes.
8. The apparatus of claim 1 comprised by one of the following: cell phones, televisions, computer monitors, and game displays.
9. An active matrix electroluminescent display apparatus comprising:
  - first and second electroluminescent devices;
  - a first transistor connected to the first electroluminescent device;
  - a second transistor positioned adjacent to the first transistor and connected to the second electroluminescent device; and
  - first and second substantially parallel power lines positioned between the first and second transistors, wherein the first power line is configured to provide current to the first transistor and the second power line is configured to provide current to the second transistor.
10. The apparatus of claim 9, further comprising:

- a third transistor electrically connected to the first transistor; and  
a fourth transistor electrically connected to the second transistor.
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11. The apparatus of claim 10, further comprising:
- a first line electrically connected to the third transistor; and  
a second line electrically connected to the fourth transistor.
- 10
12. The apparatus of claim 11 wherein a first sub-pixel including the first transistor, the electroluminescent device electrically connected to the first transistor, and the third transistor is positioned between the first power line and the first line, and a second sub-pixel including the second transistor, the electroluminescent device electrically connected to the second transistor, and the fourth transistor is positioned between the second power line and the second line.
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- 20
13. The apparatus of claim 12, wherein the first sub-pixel and the second sub-pixel are symmetric about the first power line and the second power line.
- 25
14. The apparatus of claim 9, wherein the first transistor and the second transistor have different sizes.
- 30
15. The apparatus of claim 9, wherein the electroluminescent device electrically connected to the first transistor and the electroluminescent device electrically connected to the second transistor have different sizes.
- 35
16. The apparatus of claim 9 comprised by one of the following: cell phones, televisions, computer monitors, and game displays.
- 40
17. An active matrix electroluminescent display apparatus comprising:
- first and second means for producing light based on a current;  
first means for switching current connected to the first means for producing light;  
second means for switching current positioned adjacent to the first means for switching current and connected to the second means for producing light; and  
means for providing current positioned between the first and second means for switching current, wherein the means for providing current is configured to provide current to the first and second means for switching current.
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18. The apparatus of claim 17, further comprising:
- third means for switching current electrically connected to the first means for switching current;  
fourth means for switching current electrically connected to the second means for switching current;  
first means for providing a signal electrically connected to the third means for switching current; and  
second means for providing a signal electrically connected to the fourth means for switching current;  
wherein a first sub-pixel, including the first means for switching current, the means for producing light electrically connected to the first means for switching current, and the third means for switching current, is positioned between the means for providing current and the first means for providing a signal, and a second sub-pixel including the second means for switching current, the means for producing light electrically connected to the second means for switching current, and the fourth means for switching current is positioned between the means for providing current and the second means for providing a signal.
19. The apparatus of claim 18, wherein the first sub-pixel and the second sub-pixel are symmetric about the means for providing current.
20. A method of manufacturing an active matrix electroluminescent display apparatus on a substrate, the method comprising:
- forming first and second means for producing light based on a current on the substrate;  
forming first means for switching current connected to the first means for producing light;  
forming second means for switching current positioned adjacent to the first means for switching current and connected to the second means for producing light; and  
forming first and second substantially parallel means for providing current positioned between the first and second means for switching current, wherein the first means for providing current is configured to provide current to the first means for switching current and the second means for providing current is configured to provide current to the second means for switching current.
21. The method of claim 20, further comprising:
- forming third means for switching current electrically connected to the first means for switching current;  
forming fourth means for switching current elec-

trically connected to the second means for switching current;  
forming first means for providing a signal electrically connected to the third means for switching current; 5  
forming second means for providing a signal electrically connected to the fourth means for switching current;  
wherein a first sub-pixel including the first means for switching current, the means for producing light electrically connected to the first means for switching current, and the third means for switching current is positioned between the first means for providing current and the first means for providing a signal, and a second sub-pixel including the second means for switching current, the means for producing light electrically connected to the second means for switching current, and the fourth means for switching current is positioned between the second means for providing current and the second means for providing a signal. 10  
22. The method of claim 21, wherein the first sub-pixel and the second sub-pixel are symmetric about a line between the first and second means for providing current. 15  
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FIG. 1 (PRIOR ART)

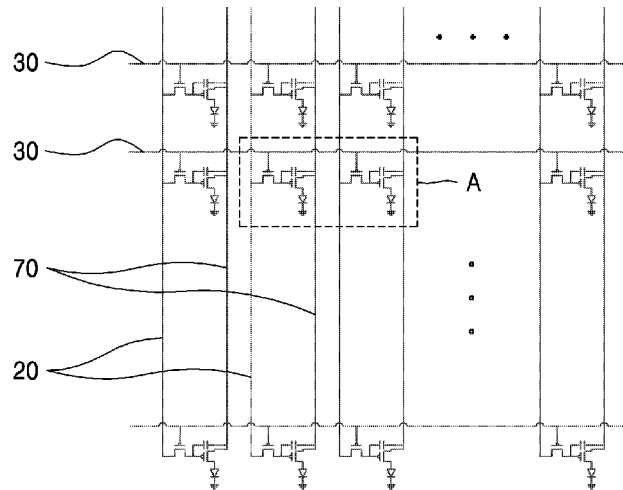
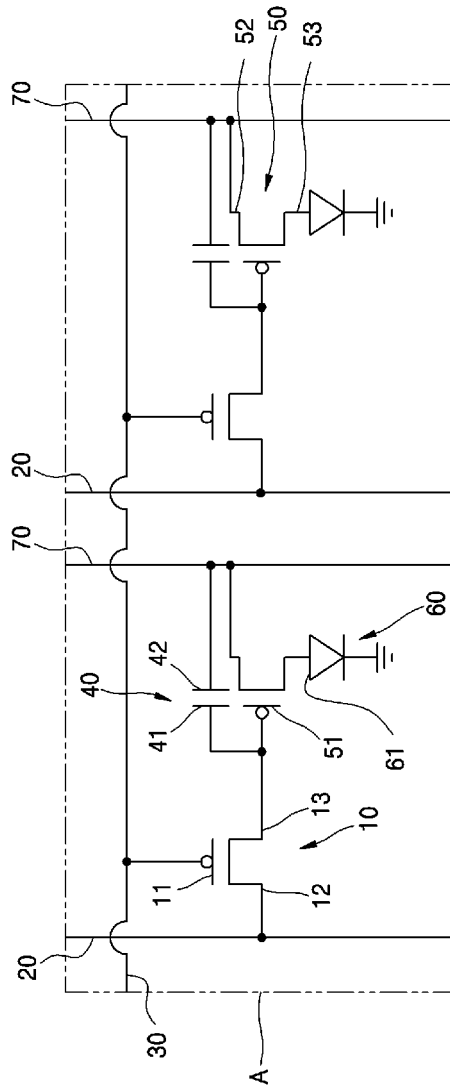
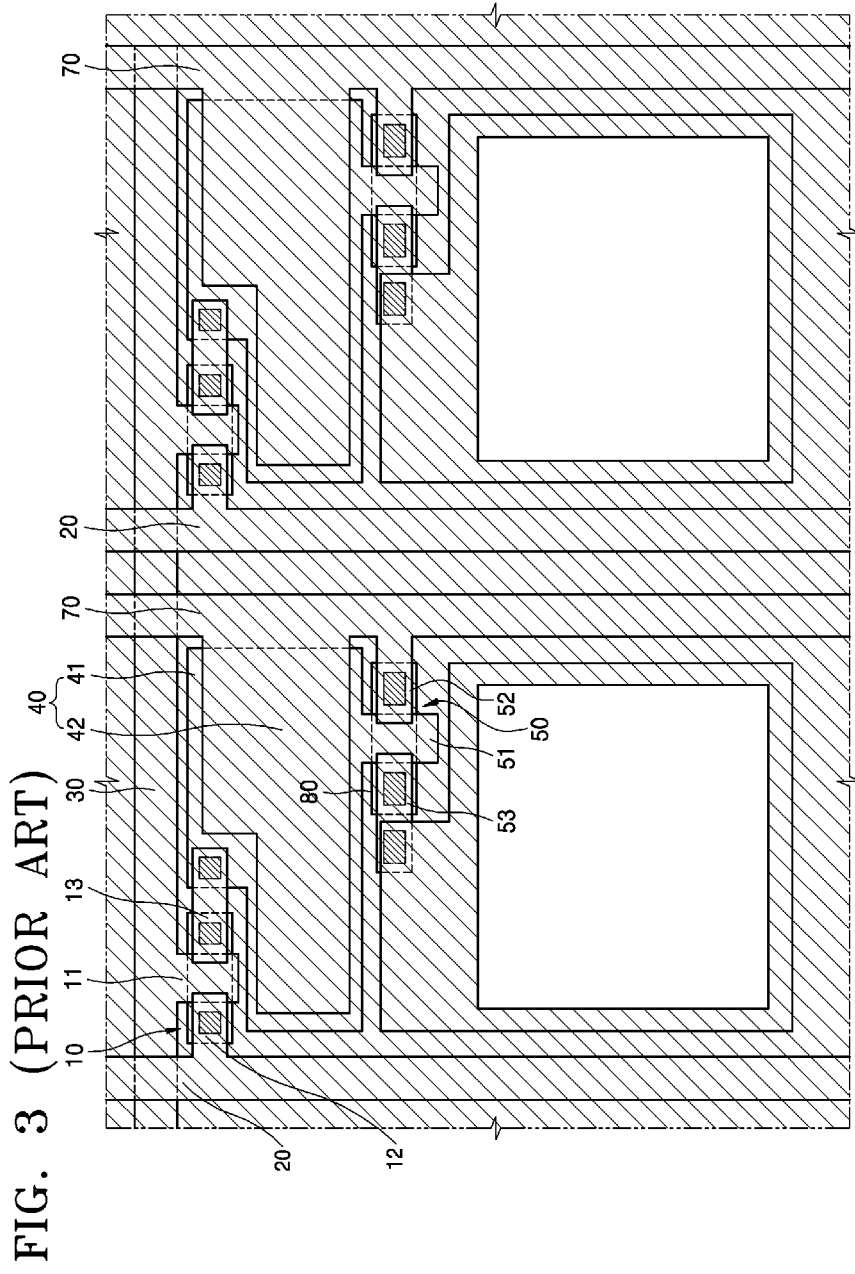


FIG. 2 (PRIOR ART)





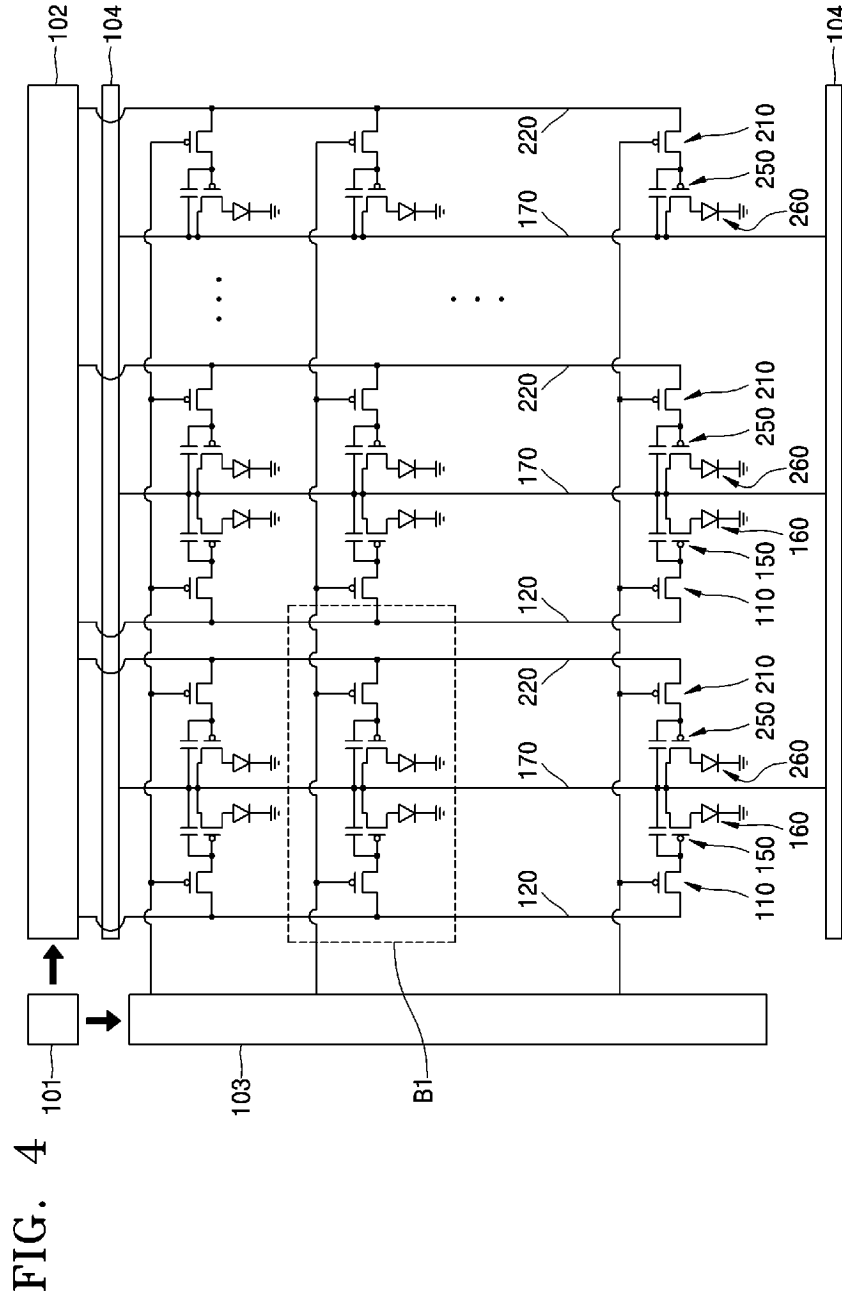


FIG. 5

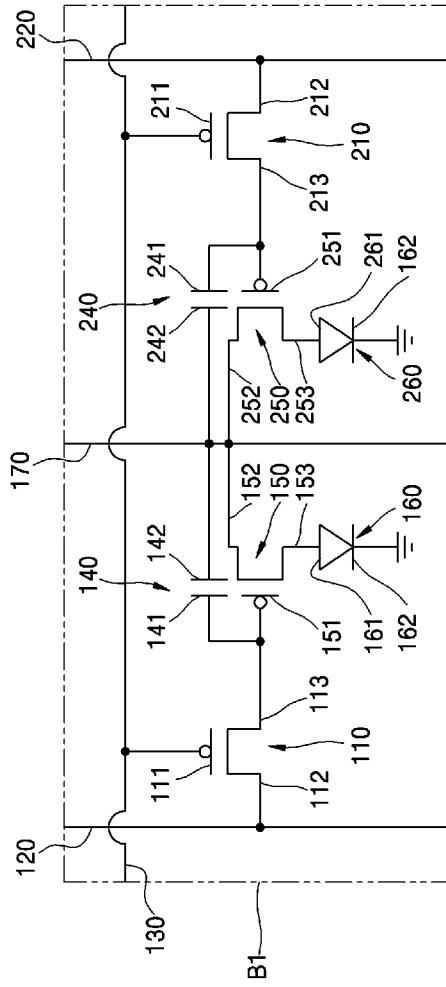




FIG. 7

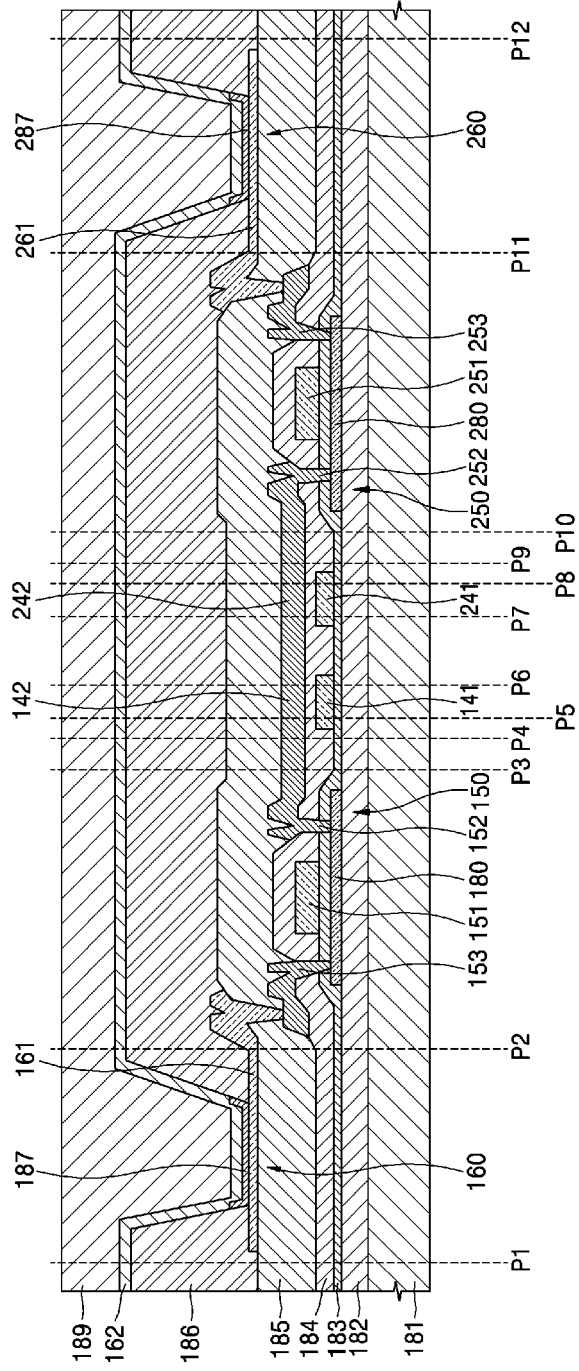


FIG. 8

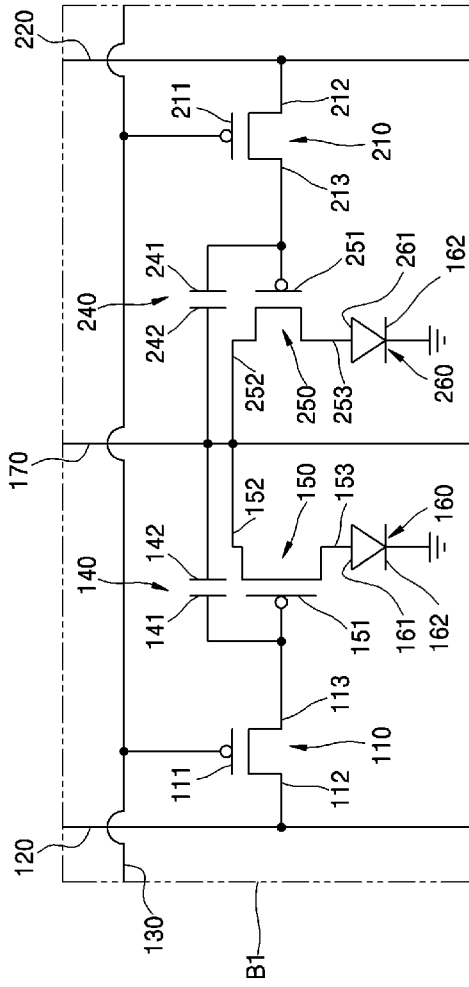


FIG. 9

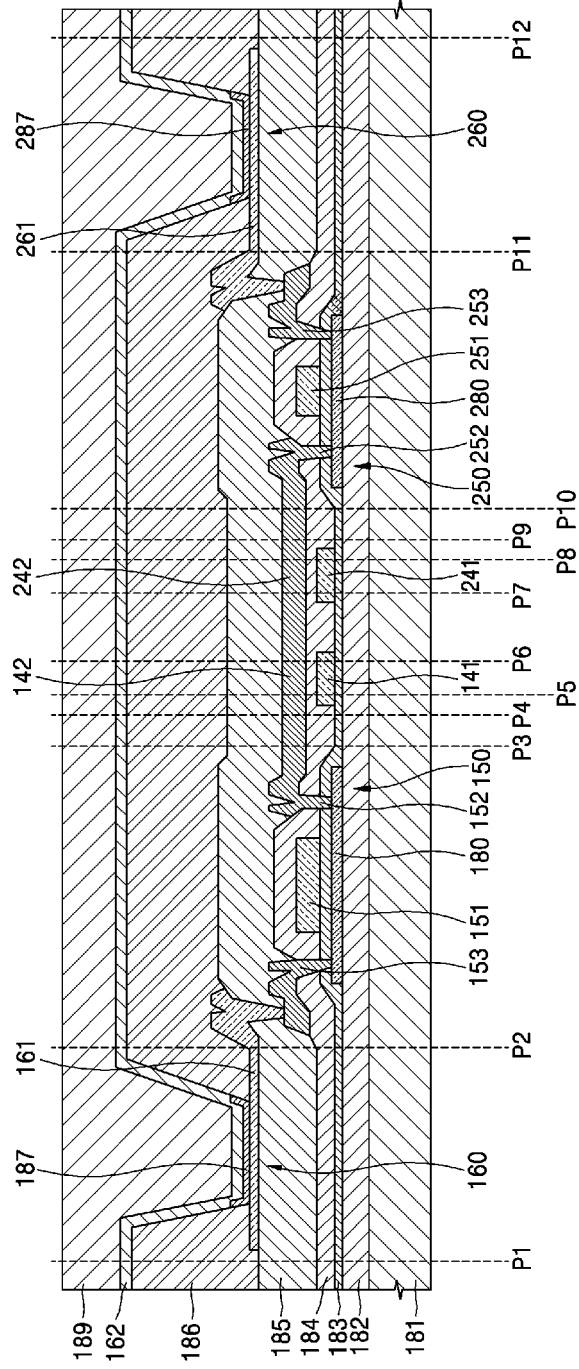
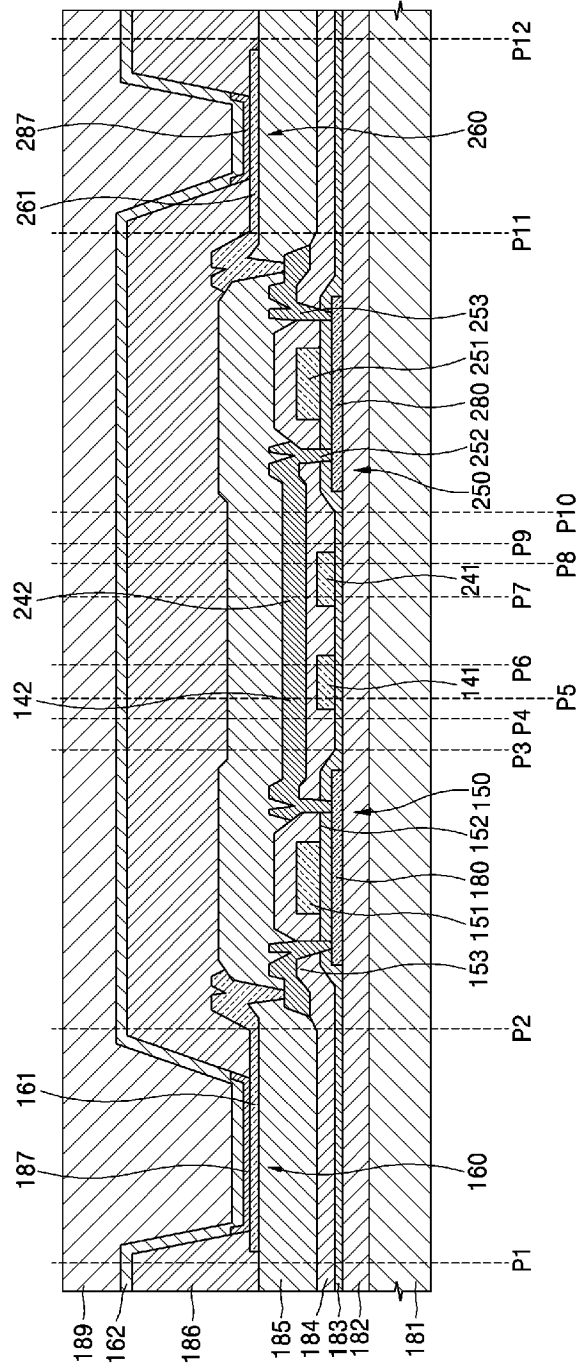


FIG. 10



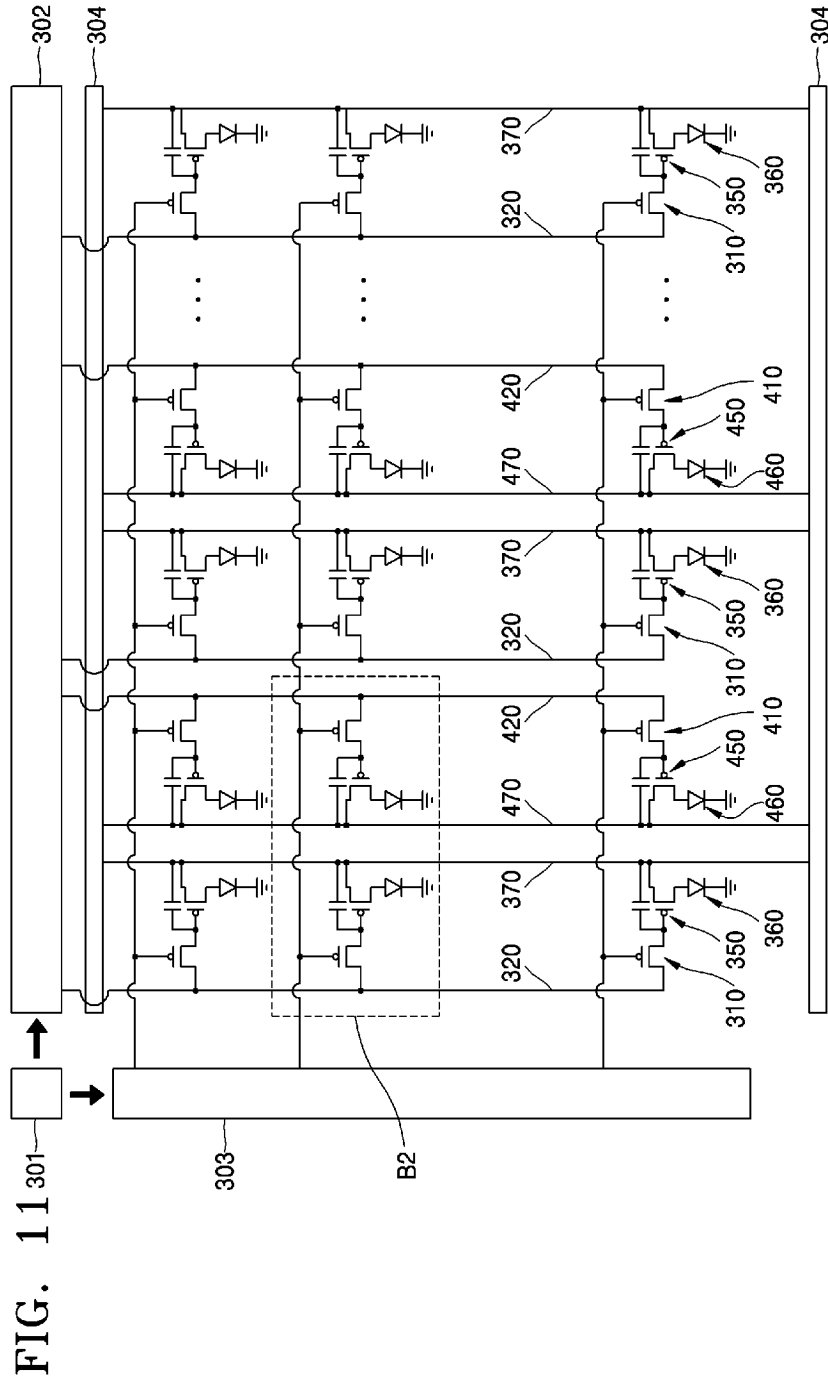


FIG. 12

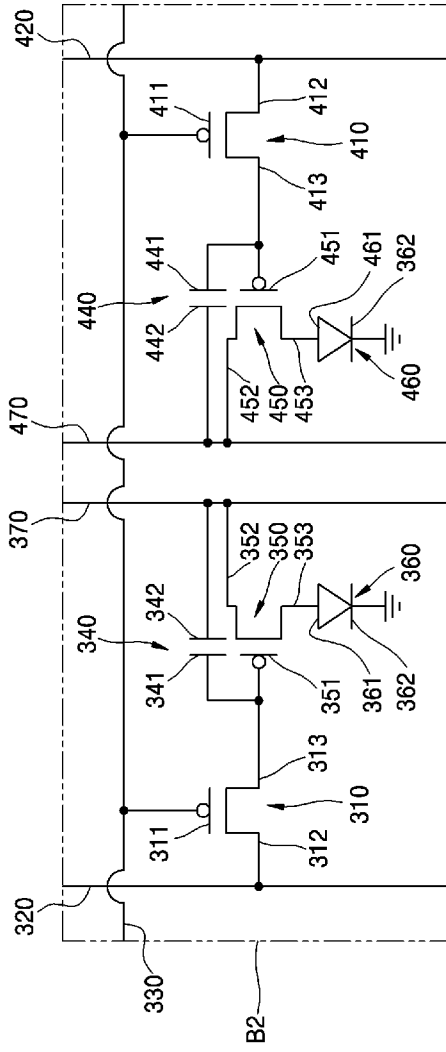
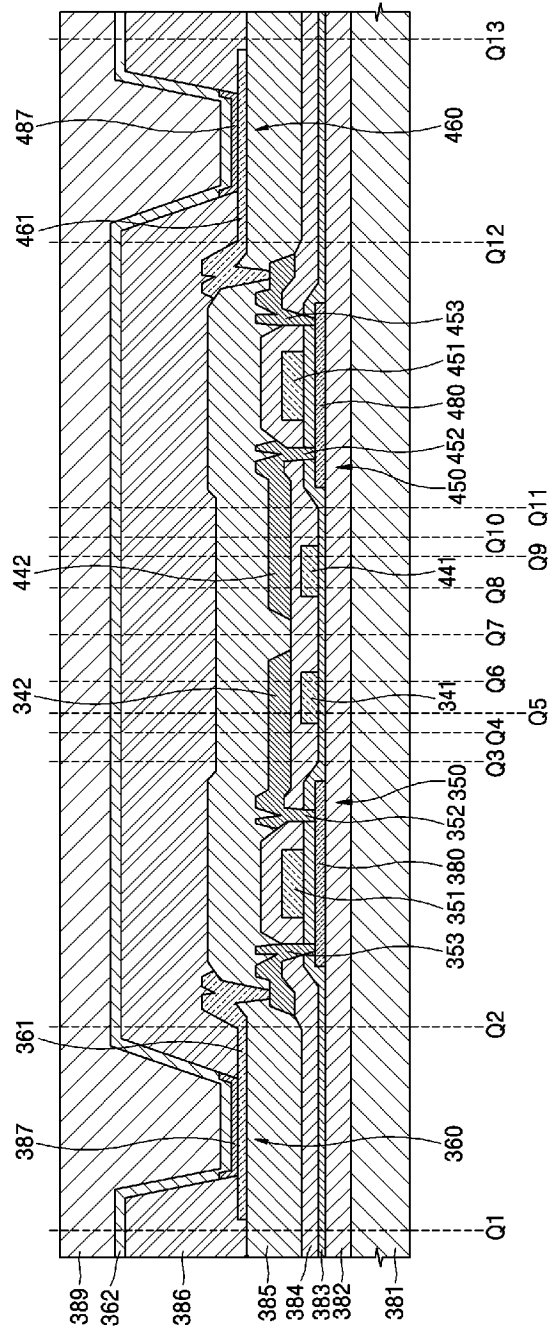




FIG. 14



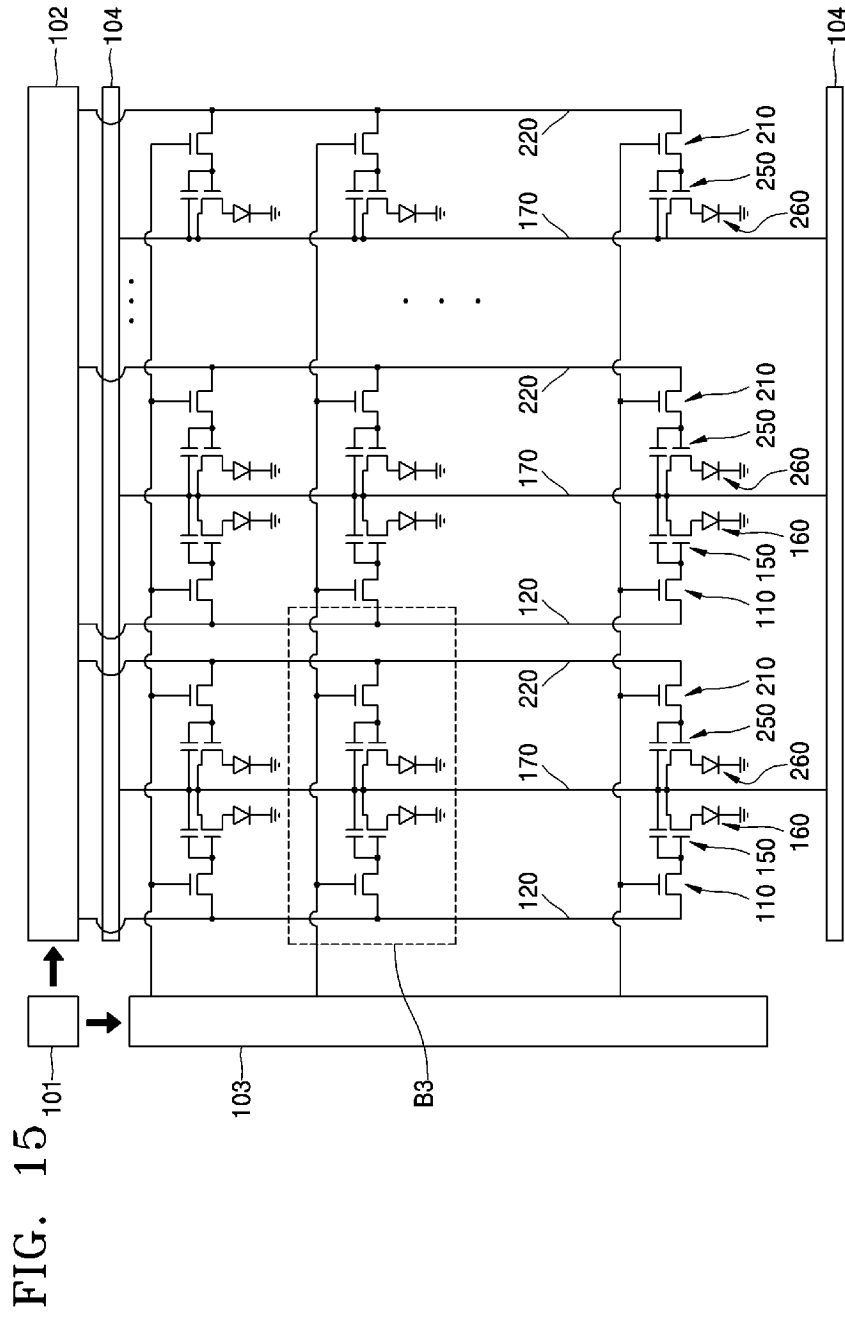


FIG. 16

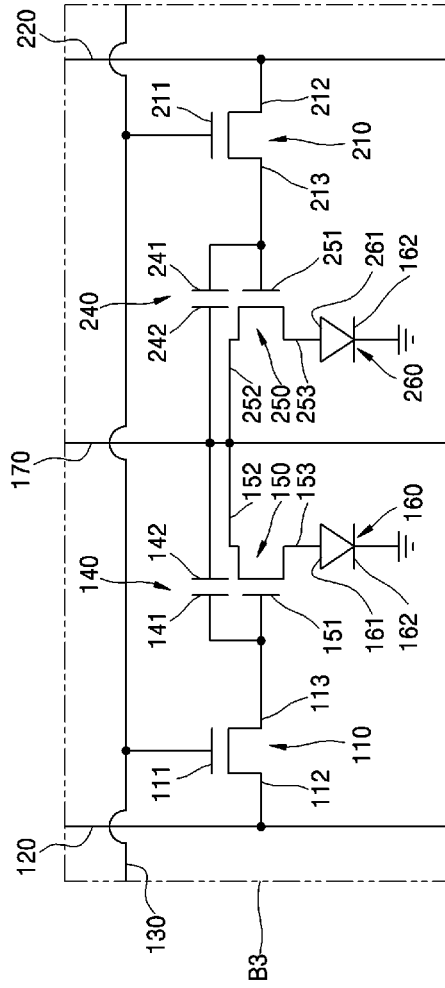
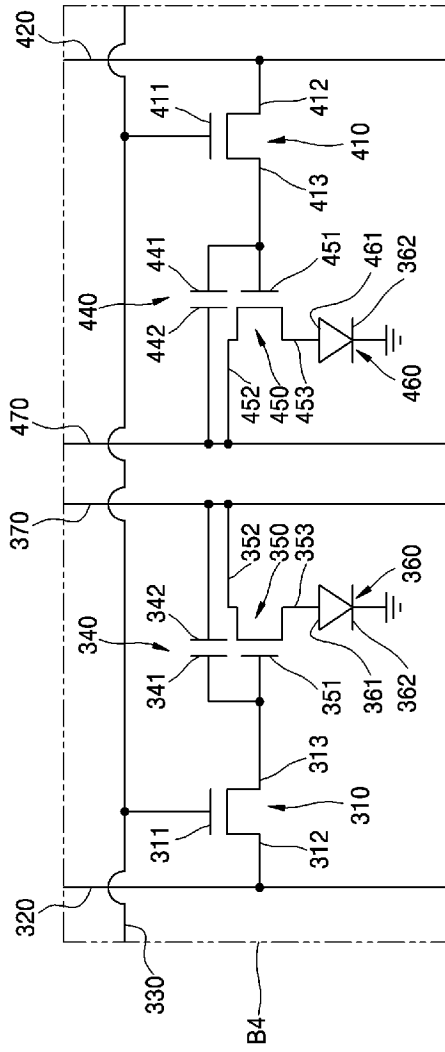




FIG. 18





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 1 255 240 A (SEIKO EPSON CORPORATION) 6 November 2002 (2002-11-06) * paragraphs [0001], [0022]; figures 2,3 *	1-22	G09G3/32
X	----- US 2003/189410 A1 (YAMAZAKI YU ET AL) 9 October 2003 (2003-10-09) * paragraphs [0063], [0064], [0103]; figures 3,7 *	1-22	
X	----- US 2001/015626 A1 (OZAWA TOKUROH) 23 August 2001 (2001-08-23) * paragraph [0067]; figures 2,3 *	1-22	
A	----- US 4 775 861 A (SAITO ET AL) 4 October 1988 (1988-10-04) * column 1, line 46 - column 2, line 5; figures 4,5 *	1-22	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G09G
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 5 October 2005	Examiner Kunze, H
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... & : member of the same patent family, corresponding document			

1  
EPO FORM 1503 03/82 (P04/C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 05 10 5547

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

05-10-2005

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			EP 1336953 A2	20-08-2003
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US 2001015626	A1	23-08-2001	NONE	
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US 4775861	A	04-10-1988	NONE	
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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	有源矩阵电致发光显示装置		
公开(公告)号	<a href="#">EP1612765A1</a>	公开(公告)日	2006-01-04
申请号	EP2005105547	申请日	2005-06-22
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO. , LTD.		
当前申请(专利权)人(译)	三星SDI CO. , LTD.		
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发明人	KANG, TAE-WOOK, SAMSUNG SDI CO., LTD KIM, CHANG-SOO, SAMSUNG SDI CO., LTD. JEONG, CHANG-YONG, SAMSUNG SDI CO., LTD.		
IPC分类号	G09G3/32 H05B33/08 G09G3/30		
CPC分类号	H01L27/3276 G09G3/32 G09G2300/0439 G09G2300/0809 G09G2330/08		
代理机构(译)	hengelhaupt , Jürgen		
优先权	1020040048648 2004-06-26 KR		
其他公开文献	EP1612765B1		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

提供一种有源矩阵电致发光显示装置，其中可以基本上基本上防止相邻子像素中的电源线（170）和数据线（120）之间的短路。有源矩阵电致发光显示装置包括：电源线（170）；第一晶体管，位于电源线（170）的一侧，并连接到电源线；第二晶体管（250），位于电源线（170）的另一侧，并连接到电源线（170）；电致发光器件（160,260）和电致发光器件（160,260）分别连接到第一晶体管（150）和第二晶体管（250）。

