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(54) **ELECTROLUMINESCENT DISPLAY DEVICE**

Description**BACKGROUND****Technical Field**

[0001] The present disclosure relates to an electroluminescent display device, and more particularly, to an electroluminescent display device including a pixel circuit for compensating a voltage drop.

Discussion of the Related Art

[0002] With the advancement of information-oriented technology, the market in display devices corresponding to a connection medium between a user and information is increasing. The use of various types of display devices such as electroluminescent display devices, liquid crystal display devices, and quantum dot display devices is increasing.

[0003] In the electroluminescent display devices, when a gate signal, a data signal, and the like are supplied to at least one of subpixels, a light emitting device of a selected subpixel emits light, thereby displaying an image. Light emitting devices may be implemented based on an organic material or an inorganic material.

[0004] The electroluminescent display devices display an image, based on light emitted from a light emitting device of each subpixel, and thus, it is required to enhance an accuracy of a pixel circuit which controls light emission of each subpixel, for enhancing the quality of an image displayed by the electroluminescent display devices. For example, an accuracy of the pixel circuit is enhanced by compensating for a sequential shift characteristic (or time-varying characteristic) where a threshold voltage of a transistor included in the pixel circuit is shifted.

[0005] There are various methods of compensating for a sequential shift characteristic of the electroluminescent display devices. Some of compensation methods do not consider the drop of a source voltage applied to each subpixel, causing an image quality issue such as the vertical luminance non-uniformity or crosstalk of the electroluminescent display devices.

[0006] Therefore, research for designing a pixel circuit compensated for the drop of the source voltage is being done in order for the electroluminescent display devices to display an accurate image.

SUMMARY

[0007] Accordingly, embodiments of the present disclosure are directed to an electroluminescent display device that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0008] An aspect of the present disclosure is to provide a display device for minimizing voltage drop occurring in a line to which a voltage is applied.

[0009] Another aspect of the present disclosure is to provide a pixel circuit and an electroluminescent display device including the same, in which an image quality issue such as the vertical luminance non-uniformity or crosstalk of a display panel is solved through compensation based on voltage drop occurring in a line to which a voltage is applied.

[0010] Another aspect of the present disclosure is to provide an electroluminescent display device in which the area for the subpixels can be reduced, e.g. by depositing some of transistors included in each subpixel in a non-display area, and thus, a high-resolution display device is realized.

[0011] Another aspect of the present disclosure is directed to an electroluminescent display device in which an operation of supplying a reference voltage is set based on a driving method of a subpixel in order for voltage drop not to affect a driving current applied to a light emitting device.

[0012] In addition to the aforesaid objects of the present disclosure, other features and advantages of the present disclosure will be described below but will be clearly understood by those skilled in the art from descriptions below.

[0013] Additional features and aspects will be set forth in part in the description that follows, and in part will be apparent from the description, or may be learned by practice of the inventive concepts may be realized and attained by the structure particularly pointed out in the written description, or derivable therefrom, and claims hereof as well as the appended drawings.

[0014] To achieve these and other aspects of the inventive concepts, as embodied and broadly described herein, an electroluminescent display device comprises a display panel including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an n th (where n is a natural number) pixel line of the plurality of pixel lines may include a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an n -1st scan signal, a second transistor applying a reference voltage to the first node in response to an n th scan signal, a third transistor applying a high-level power voltage to the first node in response to an n th emission signal, a fourth transistor allowing a current to flow between the third node and a fourth node in response to an $n+1$ st

emission signal, a fifth transistor applying an initialization voltage to the fourth node in response to the n-1st scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a seventh transistor applying a data voltage to the fifth node in response to the n-1st scan signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an anode connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. Accordingly, a subpixel supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electroluminescent display device.

[0015] The display panel may include a display area and a non-display area. The second and/or the third transistors may be disposed in the non-display area.

[0016] In another aspect, an electroluminescent display device comprises a display panel including a display area and a non-display area and including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an nth pixel line of the plurality of pixel lines may include a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an nth scan signal, a second transistor applying a reference voltage to the first node in response to the nth scan signal, a third transistor applying a high-level power voltage to the first node in response to an nth emission signal, a fourth transistor allowing a current to flow between the third node and a fourth node in response to the nth emission signal, a fifth transistor applying an initialization voltage to the fourth node in response to the nth scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a seventh transistor applying a data voltage to the fifth node in response to the nth scan signal, an eighth transistor supplying an initialization voltage to the second node in response to an n-1st scan signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an anode connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. Accordingly, a subpixel supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electroluminescent display device.

[0017] The display panel may include a display area and a non-display area. The second and/or the third transistors may be disposed in the non-display area.

[0018] In another aspect, an electroluminescent display device comprises a display panel including a display area and a non-display area and including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an nth pixel line of the plurality of pixel lines may include a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an n+1st scan signal, a second transistor applying a reference voltage to the first node in response to an nth scan signal, a third transistor applying a high-level power voltage to the first node in response to an nth emission signal, a fifth transistor applying an initialization voltage to the fourth node in response to an n-1st scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a ninth transistor applying the high-level power voltage to the fifth node in response to the n-1st scan signal, a seventh transistor applying a data voltage to the fifth node in response to the n+1st scan signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an anode connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. Accordingly, a subpixel supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electroluminescent display device.

[0019] The display panel may include a display area and a non-display area. The second and/or the third transistors may be disposed in the non-display area.

[0020] In another aspect, an electroluminescent display device comprises a display panel including a display area and a non-display area and including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an nth pixel line of the plurality of pixel lines may include a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an nth scan signal, a second transistor applying a reference voltage to the first node in response to the nth scan signal, a third transistor applying a high-level power voltage to the first node in response to an nth emission signal, a fifth transistor applying an initialization voltage to a fourth node in response to the nth scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a ninth transistor applying the high-level power voltage to a fifth node in response to an n-1st scan signal, a seventh transistor applying a data voltage to the fifth node in response to the nth scan signal, an eighth transistor supplying an initialization voltage to the second node in response to the n-1st scan signal, a fourth transistor allowing a current to flow between the third node and a fourth node in response to the nth emission signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an anode connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. Accordingly, a subpixel

supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electroluminescent display device.

[0021] The display panel may include a display area and a non-display area. The second and/or the third transistors may be disposed in the non-display area.

[0022] Details of other embodiments are included in the detailed description and the drawings.

[0023] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the inventive concepts as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated and constitute a part of this application, illustrate embodiments of the disclosure and together with the description serve to explain various principles. In the drawings:

FIG. 1 is a block diagram illustrating an electroluminescent display device according to an embodiment of the present disclosure;

FIG. 2 is a block diagram illustrating a subpixel illustrated in FIG. 1 and signal lines connected to the subpixel;

FIG. 3 is a circuit diagram of a subpixel according to a first embodiment of the present disclosure;

FIG. 4A is a diagram for describing driving of a subpixel according to a first embodiment of the present disclosure in an initialization period;

FIG. 4B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 4A;

FIG. 5A is a diagram for describing driving of a subpixel according to a first embodiment of the present disclosure in a sampling period;

FIG. 5B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 5A;

FIG. 6A is a diagram for describing driving of a subpixel according to a first embodiment of the present disclosure in a holding period;

FIG. 6B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 6A;

FIG. 7A is a diagram for describing driving of a subpixel according to a first embodiment of the present disclosure in a programming period;

FIG. 7B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 7A;

FIG. 8A is a diagram for describing driving of a subpixel according to a first embodiment of the present disclosure in an emission period;

FIG. 8B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 8A;

FIG. 9 is a circuit diagram of a subpixel according to a second embodiment of the present disclosure;

FIG. 10A is a diagram for describing driving of a subpixel according to a second embodiment of the present disclosure in an initialization period;

FIG. 10B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 10A;

FIG. 11A is a diagram for describing driving of a subpixel according to a second embodiment of the present disclosure in a sampling period;

FIG. 11B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 11A;

FIG. 12A is a diagram for describing driving of a subpixel according to a second embodiment of the present disclosure in a holding period;

FIG. 12B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 12A;

FIG. 13A is a diagram for describing driving of a subpixel according to a second embodiment of the present disclosure in an emission period;

FIG. 13B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 13A;

FIG. 14 is a circuit diagram of a subpixel according to a third embodiment of the present disclosure;

FIG. 15A is a diagram for describing driving of a subpixel according to a third embodiment of the present disclosure in an initialization period;

FIG. 15B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 15A;

FIG. 16A is a diagram for describing driving of a subpixel according to a third embodiment of the present disclosure in a first holding period;

FIG. 16B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 16A;

FIG. 17A is a diagram for describing driving of a subpixel according to a third embodiment of the present disclosure in a sampling period;

FIG. 17B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 17A;

FIG. 18A is a diagram for describing driving of a subpixel according to a third embodiment of the present disclosure in a second holding period;

FIG. 18B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 18A;
 FIG. 19A is a diagram for describing driving of a subpixel according to a third embodiment of the present disclosure in an emission period;
 FIG. 19B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 19A;
 FIG. 20 is a circuit diagram of a subpixel according to a fourth embodiment of the present disclosure;
 FIG. 21A is a diagram for describing driving of a subpixel according to a fourth embodiment of the present disclosure in an initialization period;
 FIG. 21B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 21A;
 FIG. 22A is a diagram for describing driving of a subpixel according to a fourth embodiment of the present disclosure in a sampling period;
 FIG. 22B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 22A;
 FIG. 23A is a diagram for describing driving of a subpixel according to a fourth embodiment of the present disclosure in a holding period;
 FIG. 23B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 23A;
 FIG. 24A is a diagram for describing driving of a subpixel according to a fourth embodiment of the present disclosure in an emission period; and
 FIG. 24B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 24A.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0025] Reference will now be made in detail to the embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0026] Advantages and features of the present disclosure, and implementation methods thereof will be clarified through following embodiments described with reference to the accompanying drawings. The present disclosure may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present disclosure to those skilled in the art. Furthermore, the present disclosure is only defined by scopes of claims.

[0027] A shape, a size, a ratio, an angle, and a number disclosed in the drawings for describing embodiments of the present disclosure are merely an example, and thus, the present disclosure is not limited to the illustrated details. Like reference numerals refer to like elements throughout. In the following description, when the detailed description of the relevant known function or configuration is determined to unnecessarily obscure the important point of the present disclosure, the detailed description will be omitted. In a case where 'comprise', 'have', and 'include' described in the present specification are used, another part may be added unless 'only~' is used. The terms of a singular form may include plural forms unless referred to the contrary.

[0028] In construing an element, the element is construed as including an error range although there is no explicit description.

[0029] In describing a position relationship, for example, when a position relation between two parts is described as 'on~', 'over~', 'under~', and 'next~', one or more other parts may be disposed between the two parts unless 'just' or 'direct' is used.

[0030] In describing a time relationship, for example, when the temporal order is described as 'after~', 'subsequent~', 'next~', and 'before~', a case which is not continuous may be included unless 'just' or 'direct' is used.

[0031] Features of various embodiments of the present disclosure may be partially or overall coupled to or combined with each other, and may be variously inter-operated with each other and driven technically as those skilled in the art can sufficiently understand. The embodiments of the present disclosure may be carried out independently from each other, or may be carried out together in co-dependent relationship.

[0032] In the present specification, a pixel circuit provided on a substrate of a display panel may be implemented with an n-type or p-type transistor. For example, the transistor may be implemented as a transistor having a metal oxide semiconductor field effect transistor (MOSFET) structure. The transistor may be a three-electrode element including a gate electrode (gate), a source electrode (source), and a drain electrode (drain). The source may be an electrode for supplying a carrier to the transistor. In the transistor, the carrier may start to flow from the source. The drain may be an electrode through which the carrier flows out from the transistor to the outside. For example, in the transistor, the carrier may flow from the source to the drain. In the n-type transistor, since the carrier is an electron, a source voltage may have a level which is lower than that of a drain voltage. In the n-type transistor, since the electron flows from the source to the drain, a current may flow from the drain to the source. In the p-type transistor, since the carrier is a hole, a source voltage may be higher than a drain voltage in order for the hole to flow from the source to the drain. In the p-type transistor, since the hole flows from the source to the drain, a current may flow from the source to the drain. The source and the drain of the transistor may not be fixed, and based on an applied voltage, the source and the drain of the transistor may

switch therebetween. Also, the source and the drain of the transistor may be respectively referred to as a first electrode and a second electrode, or may be respectively referred to as a second electrode and a first electrode.

[0033] Hereinafter, a gate-on voltage may be a voltage of a gate signal for turning on a transistor. A gate-off voltage may be a voltage of the gate signal for turning off the transistor. In the p-type transistor, the gate-on voltage may be a gate low voltage or a logic low voltage (VL) and the gate-off voltage may be a gate high voltage or a logic high voltage (VH). In the n-type transistor, the gate-on voltage may be a gate high voltage or a logic high voltage (VH), and the gate-off voltage may be a gate low voltage or a logic low voltage (VL). Also, levels of a high-level power voltage, a low-level power voltage, an initialization voltage, a reference voltage, a data voltage, a gate high voltage, and a gate low voltage described below may vary based on a luminance of an electroluminescent display device.

[0034] Hereinafter, an electroluminescent display device according to embodiments of the present disclosure will be described with reference to the accompanying drawings.

[0035] FIG. 1 is a block diagram illustrating an electroluminescent display device 100 according to an embodiment of the present disclosure.

[0036] Referring to FIG. 1, the electroluminescent display device 100 may include an image processor 110, a timing controller 120, a gate driver 130, a data driver 140, and a display panel 150.

[0037] The image processor 110 may output image data supplied from the outside and a driving signal for driving various elements. The driving signal output from the image processor 110 may include a data enable signal, a vertical sync signal, a horizontal sync signal, and a clock signal.

[0038] The timing controller 120 may be supplied with the image data and the driving signal from the image processor 110. The timing controller 120 may output a gate timing control signal GTC for controlling an operation timing of the gate driver 130 and a data timing control signal DTC for controlling an operation timing of the data driver 140, based on the driving signal.

[0039] The gate driver 130 may output a scan signal in response to the gate timing control signal GTC supplied from the timing controller 120. The gate driver 130 may output a gate signal through a plurality of gate lines GL1 to GLp (where p is an integer equal to or more than two). The gate driver 130 may be implemented as an integrated circuit (IC) type or may be implemented as a gate in panel (GIP) type which is embedded into the display panel 150. The gate driver 130 may be disposed on each or one of the left and the right of the display panel 150. The gate driver 130 may respectively output first to pth scan signals to first to pth scan lines of the display panel 150.

[0040] The data driver 140 may output a data voltage in response to the data timing control signal DTC supplied from the timing controller 120. The data driver 140 may sample and latch a digital data signal DATA supplied from the timing controller 120 to convert the digital data signal DATA into an analog data signal based on a gamma reference voltage. The data driver 140 may output the data signal through a plurality of data lines DL1 to DLq (where q is an integer equal to or more than two). The data driver 140 may be provided as an IC type on the display panel 150, or may be provided as a chip on film (COF) type on the display panel 150.

[0041] A power supply 180 may output a high-level power voltage VDD, a low-level power voltage VSS, etc. The high-level power voltage VDD and the low-level power voltage VSS output from the power supply 180 may be supplied to the display panel 150. The high-level power voltage VDD may be supplied to the display panel 150 through a high level power line, and the low-level power voltage VSS may be supplied to the display panel 150 through a low level power line. A voltage output from the power supply 180 may be used by the gate driver 130 or the data driver 140.

[0042] The display panel 150 may display an image, based on the gate signal and the data signal respectively supplied from the gate driver 130 and the data driver 140 and a source voltage supplied from the power supply 180.

[0043] The display panel 150 may include a display area, where a plurality of subpixels SP are provided, and a non-display area which is disposed outside the display area and includes various signal lines, a plurality of pads, and/or the like. The display area may be an area which displays an image, and thus, may be an area where the subpixels SP are disposed. The non-display area may be an area which does not display an image, and thus, may be an area where a plurality of dummy subpixels is disposed or the subpixels SP are not disposed. Each subpixel SP may be electrically operated by a pixel circuit. The pixel circuit may comprise a first part being arranged in the display area of the display panel 150 and thus may be a part DA of the subpixel SP. The pixel circuit may also comprise a second part being arranged in the non-display area DA of the display panel 150 and thus may not be a part of the subpixel SP. The combination of the first part and the second part may form the pixel circuit.

[0044] The display area may include the plurality of subpixels SP and may display an image, based on a gray level displayed by each of the subpixels SP. Each of the subpixels SP may be connected to a data line arranged along a column line and may be connected to a gate line arranged along a pixel line or a row line. Subpixels SP connected to the same pixel line may share the same gate line and may be simultaneously supplied with the gate signal through a corresponding gate line. Also, if subpixels SP disposed on a first pixel line are defined as first subpixels and subpixels SP disposed on a pth pixel line are defined as pth subpixels, first to pth subpixels may be sequentially driven.

[0045] The subpixels SP of the display panel 150 may be arranged as a matrix type to configure a pixel array, but are not limited thereto. The subpixels SP of the display panel 150 may be arranged as various types such as a pixel sharing

type, a stripe type, and a diamond type, in addition to the matrix type.

[0046] The subpixels SP may include a red subpixel, a green subpixel, and a blue subpixel, or may include a white subpixel, a red subpixel, a green subpixel, and a blue subpixel. The subpixels SP may have one or more different emission areas, based on an emission characteristic.

[0047] FIG. 2 is a block diagram illustrating a subpixel illustrated in FIG. 1 and signal lines connected to the subpixel SP.

[0048] One subpixel SP may be connected to a gate line GL, a data line DL, a high level power line VDDL, a low level power line VSSL, an initialization voltage line ViniL, and a reference voltage line VrefL. The number of transistors and capacitors included in the subpixel SP and a driving method of the subpixel SP may be determined based on a configuration of a pixel circuit, e.g. by the configuration of the first part of the pixel circuit disposed (arranged) on the display area. In this case, the gate line may include a plurality of scan lines, through which a scan signal is transferred, and a plurality of emission lines through which an emission signal is transferred.

[0049] FIG. 3 is a circuit diagram of a subpixel SP according to a first embodiment of the present disclosure.

[0050] The display panel 150 may include the display area, which displays an image based on the subpixels SP and/or the first part of the pixel circuits, and the non-display DA area which does not display an image and where signal lines, driving circuits, the second part of the pixel circuits, and the like are disposed.

[0051] The electroluminescent display device 100 may display an image based on light emitted from a light emitting device EL included in each of the subpixels SP. However, in each subpixel SP, the voltage drop of a line to which a source voltage is applied occurs due to a sequential shift characteristic where a threshold voltage of an element included in each subpixel SP is shifted and enlarging of the display panel 150, and thus, it is required to compensate for the voltage drop.

[0052] Therefore, a pixel circuit which recognizes a problem causing an image quality issue such as vertical luminance non-uniformity or crosstalk in an electroluminescent display device according to an embodiment of the present disclosure and solves the problem will be described below. Additionally, the first part of the pixel circuit that is arranged in the display area DA, needs to be miniaturized to enable higher resolutions of the display panel 150. An example where a below-described pixel circuit is configured with p-type transistors will be described, but the present embodiment is not limited thereto. In other embodiments, n-type transistors may be applied. Also, an example where a subpixel SP according to a first embodiment of the present disclosure is a subpixel SP disposed on an nth (where n is a natural number satisfying $1 \leq n \leq p$) pixel line will be described.

[0053] An nth subpixel SP may include first to seventh transistors T1 to T7, a driving transistor DT, a capacitor Cst, and a light emitting device EL. In the first embodiment of the present disclosure, the nth subpixel SP may be implemented based on a total of eight transistors and one capacitor.

[0054] The driving transistor DT may include a source connected to a first node N1, a gate connected to a second node N2, and a drain connected to a third node N3. When a gate-on voltage is applied to the second node N2, the driving transistor DT may be turned on to provide a constant current to the third node N3.

[0055] The first transistor T1 may include a gate connected to an n-1st scan line, a source connected to the second node N2, and a drain connected to the third node N3. The first transistor T1 may be turned on in response to a gate-on voltage of an n-1st scan signal Scan(n-1) applied through the n-1st scan line. When the first transistor T1 is turned on, the gate and the drain of the driving transistor DT may be electrically connected to each other, and thus, the driving transistor DT may be in a diode connection state.

[0056] The second transistor T2 may include a gate connected to an nth scan line, a source connected to a reference voltage line, and a drain connected to the first node N1. The second transistor T2 may be turned on in response to a gate-on voltage of an nth scan signal Scan(n) applied through the nth scan line. When the second transistor T2 is turned on, a reference voltage Vref may be applied to the first node N1.

[0057] The third transistor T3 may include a gate connected to an nth emission line, a source connected to a high level power line, and a drain connected to the first node N1. The third transistor T3 may be turned on in response to a gate-on voltage of an nth emission signal EM(n) applied through the nth emission line. When the third transistor T3 is turned on, a high-level power voltage VDD may be applied to the first node N1.

[0058] The fourth transistor T4 may include a gate connected to an n+1st emission line, a source connected to the third node N3, and a drain connected to a fourth node N4. In this case, the fourth node N4 may be connected to an anode of the light emitting device EL. The fourth transistor T4 may be turned on in response to a gate-on voltage of an n+1st emission signal EM(n+1) applied through the n+1st emission line. When the fourth transistor T4 is turned on, a current may flow between the third node N3 and the fourth node N4.

[0059] The light emitting device EL may include the anode connected to the fourth node N4 and a cathode to which a low-level power voltage VSS is applied. When the fourth transistor T4 is turned on, a driving current generated through the driving transistor DT may be applied to the anode of the light emitting device EL, and thus, the light emitting device EL may emit light. For example, the low-level power voltage VSS may be a voltage of -4V to -2.5V, but is not limited thereto.

[0060] The fifth transistor T5 may include a gate connected to the n-1st scan line, a source connected to the anode of the light emitting device EL, and a drain connected to an initialization line. The fifth transistor T5 may be turned on in

response to the gate-on voltage of the n-1st scan signal Scan(n-1) applied through the n-1st scan line. When the fifth transistor T5 is turned on, the anode of the light emitting device EL may be initialized based on an initialization voltage.

[0061] The sixth transistor T6 may include a gate connected to the nth emission line, a source connected to the high level power line, and a drain connected to a fifth node N5. The sixth transistor T6 may be turned on in response to the gate-on voltage of the nth emission signal EM(n) applied through the nth emission line. When the sixth transistor T6 is turned on, the high-level power voltage VDD may be applied to the fifth node N5.

[0062] The capacitor Cst may include a first electrode connected to the second node N2 and a second electrode connected to the fifth node N5.

[0063] The seventh transistor T7 may include a gate connected to the n-1st scan line, a source connected to a data line, and a drain connected to the fifth node N5. The seventh transistor T7 may be turned on in response to the gate-on voltage of the n-1st scan signal Scan(n-1) applied through the n-1st scan line. When the seventh transistor T7 is turned on, a data voltage Vdata may be applied to the fifth node N5.

[0064] Moreover, a voltage applied to the gate of the driving transistor DT may control a turn-on state of the driving transistor DT, and thus, a transistor including a source or a drain connected to the gate of the driving transistor DT may include two or more transistors serially connected to each other, for maximally suppressing an influence of a leakage current. In this case, the two or more transistors may be controlled by the same control signal. Accordingly, in the nth subpixel SP according to the first embodiment of the present disclosure, the first transistor T1 may be implemented as a double-gate type transistor.

[0065] The nth subpixel SP according to the first embodiment of the present disclosure may operate in the order of an initialization period, a sampling period, a holding period, a programming period, and an emission period. The initialization period may be a period where the gate of the driving transistor DT is initialized, the sampling period may be a period where a threshold voltage of the driving transistor DT is sampled and a data voltage Vdata is applied through a data line, and the holding period may be a period where the reference voltage Vref is held by a specific node and an error of a voltage applied to the gate of the driving transistor DT in the programming period subsequent thereto is prevented from being caused by an RC delay of the n-1st scan signal Scan(n-1). Also, the programming period may be a period where the high-level power voltage VDD is applied to the gate and the source of the driving transistor DT, and the emission period may be a period where the light emitting device EL emits light with a driving current generated based on the data voltage Vdata.

[0066] The nth subpixel SP according to the first embodiment of the present disclosure may have an initialization period INI, a sampling period SAM, a holding period HLD, and a programming period PRG during a period where a gate-off voltage of the nth emission signal EM(n) or the n+1st emission signal EM(n+1) is applied, and thus, compensation based on an internal circuit may be performed. An operation characteristic during the periods will be described below. For example, a gate-on voltage of a scan signal may be applied during two horizontal periods 2H, and a gate-off voltage of an emission signal may be applied during three horizontal periods 3H. Also, for example, each of the initialization period INI, the sampling period SAM, the holding period HLD, and the programming period PRG may be executed during one horizontal period 1H. Driving of the pixel circuit will be described below with reference to the drawings.

[0067] FIG. 4A is a diagram for describing driving of the subpixel according to the first embodiment of the present disclosure in the initialization period. FIG. 4B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 4A.

[0068] In the initialization period INI, the n-1st scan signal Scan(n-1) and the n+1st emission signal EM(n+1) may each have a gate-on voltage, and the nth scan signal Scan(n) and the nth emission signal EM(n) may each have a gate-off voltage. For example, the gate-on voltage may be a logic low voltage VL and may be -8V, and the gate-off voltage may be a logic high voltage VH and may be 8V. However, the present embodiment is not limited thereto.

[0069] The first transistor T1, the fifth transistor T5, and the seventh transistor T7 may be turned on by the gate-on voltage applied through the n-1st scan line, and the fourth transistor T4 may be turned on by the gate-on voltage applied through the n+1st emission line. An initialization voltage Vini may be applied to the second node N2 through the turned-on first transistor T1, fourth transistor T4, and fifth transistor T5, and thus, the gate of the driving transistor DT may be initialized to the initialization voltage Vini. Also, the data voltage Vdata may be applied to the fifth node N5 through the turned-on transistor T7, thereby preventing changing of the second node N2. In this case, the initialization voltage Vini may be a voltage which is equal to or lower than the low-level power voltage VSS. For example, the initialization voltage Vini may be a voltage of -4V to -3V, and the data voltage Vdata may be a voltage which varies within a range of 0.3V to 6.3V, based on luminance.

[0070] During the initialization period INI, the gate of the driving transistor DT may be initialized based on the initialization voltage Vini, and the capacitor Cst may be charged with the initialization voltage Vini and the data voltage Vdata.

[0071] FIG. 5A is a diagram for describing driving of the subpixel according to the first embodiment of the present disclosure in the sampling period. FIG. 5B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 5A.

[0072] In the sampling period SAM, the n-1st scan signal Scan(n-1) and the nth scan signal Scan(n) may each have a gate-on voltage, and the nth emission signal EM(n) and the n+1st emission signal EM(n+1) may each have a gate-off

voltage. A period where the n-1st scan signal Scan(n-1) has the gate-on voltage and a period where the nth scan signal Scan(n) has the gate-on voltage may overlap each other in the sampling period SAM.

[0073] The first transistor T1, the fifth transistor T5, and the seventh transistor T7 may maintain a turn-on state with the gate-on voltage applied through the n-1st scan line, and the second transistor T2 may be turned on by the gate-on voltage applied through the nth scan line and may be in the diode connection state. The reference voltage Vref may be applied to the source of the driving transistor DT through the turned-on second transistor T2, and the gate and the drain of the driving transistor DT may be connected to each other by the turned-on first transistor T1, whereby the driving transistor DT may be turned on. A voltage of the second node N2 connected to the gate of the driving transistor DT may increase up to a sum of the reference voltage Vref and a threshold voltage Vth of the driving transistor DT. Also, the data voltage Vdata applied to the fifth node N5 in the initialization period INI may be maintained even in the sampling period SAM. Therefore, a voltage corresponding to the sum of the reference voltage Vref and the threshold voltage Vth of the driving transistor DT may be applied to the first electrode of the capacitor Cst, and the data voltage Vdata may be applied to the second electrode of the capacitor Cst, whereby the capacitor Cst may be charged with a difference voltage "Vdata-(Vref+Vth)" between the voltage applied to the first electrode and the data voltage applied to the second electrode. Also, the fifth transistor T5 may be turned on to initialize the anode of the light emitting device EL to the initialization voltage Vini. In this case, the reference voltage Vref may be a voltage which is higher than the low-level power voltage VSS and is lower than the high-level power voltage VDD. For example, the reference voltage Vref may be 4V, and the threshold voltage Vth may be -4V. However, the present embodiment is not limited thereto.

[0074] During the sampling period SAM, since the n-1st scan signal Scan(n-1) and the nth scan signal Scan(n) having the gate-on voltage are applied, one electrode of the capacitor Cst may be held by applying the data voltage Vdata to the fifth node N5, and by applying the reference voltage Vref to the source of the driving transistor DT, the second node N2 may sample the threshold voltage Vth of the driving transistor DT and may sense the reference voltage Vref.

[0075] FIG. 6A is a diagram for describing driving of the subpixel according to the first embodiment of the present disclosure in the holding period. FIG. 6B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 6A.

[0076] In the holding period HLD, the nth scan signal Scan(n) may have a gate-on voltage, and the n-1st scan signal Scan(n-1), the nth emission signal EM(n), and the n+1st emission signal EM(n+1) may each have a gate-off voltage.

[0077] The second transistor T2 may maintain a turn-on state with the gate-on voltage applied through the nth scan signal Scan(n). The reference voltage Vref may be applied to the first node N1 through the turned-on second transistor T2. In the holding period HLD, the capacitor Cst may be charged with the data voltage Vdata and may hold the data voltage Vdata, based on a voltage difference between both ends thereof. In the holding period HLD, the n-1st scan signal Scan(n-1) may be shifted from the gate-on voltage to the gate-off voltage, and thus, a voltage at the gate of the driving transistor DT may slightly vary due to a parasitic capacitor of the first transistor T1. In this case, the driving transistor DT may be in a turn-off state.

[0078] FIG. 7A is a diagram for describing driving of the subpixel according to the first embodiment of the present disclosure in the programming period. FIG. 7B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 7A.

[0079] In the programming period PRG, the nth emission signal EM(n) may have a gate-on voltage, and the n-1st scan signal Scan(n-1), the nth scan signal Scan(n), and the n+1st emission signal EM(n+1) may each have a gate-off voltage.

[0080] The third transistor T3 and the sixth transistor T6 may be turned on by the gate-on voltage of the nth emission signal EM(n) applied thereto. The high-level power voltage VDD may be applied to the first node N1 through the turned-on third transistor T3, and the high-level power voltage VDD may be applied to the fifth node N5 through the turned-on sixth transistor T6. A voltage of the fifth node N5 connected to the second electrode of the capacitor Cst may be shifted from the data voltage Vdata to the high-level power voltage VDD, and due to coupling of the capacitor Cst, a voltage at the first electrode of the capacitor Cst may vary by a voltage variation of the fifth node N5. Therefore, a voltage of the second node N2 connected to the first electrode of the capacitor Cst may become "Vref+Vth+(VDD-Vdata)". In this case, since the high-level power voltage VDD is applied to the source of the driving transistor DT, the driving transistor DT may be turned on, but since the fourth transistor T4 is in a turn-off state, the light emitting device EL may not emit light. For example, the high-level power voltage VDD may be 4.6V, but is not limited thereto.

[0081] FIG. 8A is a diagram for describing driving of the subpixel according to the first embodiment of the present disclosure in the emission period. FIG. 8B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 8A.

[0082] In the emission period EMI, the nth emission signal EM(n) and the n+1st emission signal EM(n+1) may each have a gate-on voltage, and the n-1st scan signal Scan(n-1) and the nth scan signal Scan(n) may each have a gate-off voltage.

[0083] The third transistor T3 and the sixth transistor T6 may maintain a turn-on state with the gate-on voltage of the nth emission signal EM(n) applied thereto. Therefore, the second electrode of the capacitor Cst and the source of the driving transistor DT may maintain the high-level power voltage VDD, and thus, the driving transistor DT may maintain a turn-on state. Also, the fourth transistor T4 may be turned on by the gate-on voltage of the n+1st emission signal

EM(n+1) applied thereto, and thus, may allow a current to flow between the third node N3 and the fourth node N4. Accordingly, a driving current generated in the turned-on driving transistor DT may be applied to the anode of the light emitting device EL through the fourth transistor T4 to allow the light emitting device EL to emit light. Also, by connecting the gate of the fourth transistor T4 to the n+1st emission signal line, the gate of the driving transistor DT may be initialized in the initialization period INI, and the driving current may be applied to the anode of the light emitting device EL in the emission period EMI.

[0084] In the nth subpixel SP according to the first embodiment of the present disclosure, the high-level power voltage VDD may be reflected in each of the source and the gate of the driving transistor DT through the holding period HLD, in order to consider the voltage drop of the high-level power voltage VDD. Therefore, a current of the nth subpixel SP which has been compensated for may be expressed as the following Equation:

$$I_{oled} = K(V_{gs} - V_{th})^2 = K\{(V_{ref} + V_{th} + (V_{DD} - V_{data})) - V_{DD} - V_{th}\}^2 = K(V_{ref} - V_{data})^2$$

where I_{oled} denotes a current flowing through the light emitting device EL, K denotes a constant, V_{gs} denotes a voltage between the gate and the source of the driving transistor DT, V_{th} denotes the threshold voltage of the driving transistor DT, VDD denotes the high-level power voltage applied through the high level power line VDDL, V_{ref} denotes the reference voltage applied through the reference voltage line V_{refL} , and V_{data} denotes a data voltage applied through the data line DL.

[0085] As seen in the Equation, I_{oled} may be determined based on a difference between the reference voltage and the data voltage. According to the Equation, in the nth subpixel SP according to the first embodiment of the present disclosure, it can be seen that the voltage drop of the high-level power voltage is compensated for, based on the high-level power voltage VDD which is applied to the gate and the source of the driving transistor DT in the holding period HLD and the reference voltage V_{ref} which is applied to the source of the driving transistor DT in the sampling period SAM and the holding period HLD.

[0086] Therefore, a driving circuit for compensating for a sequential shift characteristic based on the voltage drop of the high-level power voltage may be implemented, and thus, an image quality issue such as the vertical luminance non-uniformity or crosstalk of a display device is solved.

[0087] Moreover, the second and third transistors T2 and T3 of the plurality of transistors configuring the nth subpixel SP according to the first embodiment of the present disclosure may be disposed on one side of the non-display area and may be used in common by q (where q is an integer equal to or more than two) number of subpixels disposed on an nth pixel line. Also, in a case where the gate driver 130 is disposed on each of the left and the right, the second and third transistors T2 and T3 may be disposed in each of a left non-display area and a right non-display area and may be used in common by q/2 number of subpixels. Therefore, the number of transistors configuring each subpixel is reduced, and thus, each subpixel is efficiently designed, thereby implementing a high-resolution display device. In this case, the other transistors (which are driving transistor DT, first transistor T1, fourth transistor T4, fifth transistor T5, sixth transistor T6, seventh transistor T7) except for the second and third transistors T2 and T3 among the plurality of transistors, the light emitting device EL and the capacitor Cst configuring the nth subpixel SP may be necessary for an individual operation of each subpixel SP are disposed in the display area, and thus, cannot be used in common by the nth pixel line. Accordingly, since the second and third transistors T2 and T3 are disposed in the non-display area DA, the high-resolution display device may be implemented.

[0088] FIG. 9 is a circuit diagram of a subpixel according to a second embodiment of the present disclosure. FIG. 9 is a modification example where one transistor is added to the pixel circuit of FIG. 3, and thus, overlapping descriptions are omitted or will be briefly described.

[0089] An nth subpixel SP according to a second embodiment of the present disclosure may include first to eighth transistors T1 to T8, a driving transistor DT, a capacitor Cst, and a light emitting device EL. In the second embodiment of the present disclosure, the nth subpixel SP may be implemented based on a total of nine transistors and one capacitor.

[0090] The driving transistor DT may include a source connected to a first node N1, a gate connected to a second node N2, and a drain connected to a third node N3. When a gate-on voltage is applied to the second node N2, the driving transistor DT may be turned on to provide a constant current to the third node N3.

[0091] The first transistor T1 may include a gate connected to an nth scan line, a source connected to the second node N2, and a drain connected to the third node N3. The first transistor T1 may be turned on in response to a gate-on voltage of an nth scan signal Scan(n) applied through the nth scan line. When the first transistor T1 is turned on, the gate and the drain of the driving transistor DT may be electrically connected to each other, and thus, the driving transistor DT may be in a diode connection state.

[0092] The second transistor T2 may include a gate connected to the nth scan line, a source connected to a reference voltage line, and a drain connected to the first node N1. The second transistor T2 may be turned on in response to a gate-on voltage of an nth scan signal Scan(n) applied through the nth scan line. When the second transistor T2 is turned

on, a reference voltage V_{ref} may be applied to the first node N1.

[0093] The third transistor T3 may include a gate connected to an nth emission line, a source connected to a high level power line, and a drain connected to the first node N1. The third transistor T3 may be turned on in response to a gate-on voltage of an nth emission signal EM(n) applied through the nth emission line. When the third transistor T3 is turned on, a high-level power voltage VDD may be applied to the first node N1.

[0094] The fourth transistor T4 may include a gate connected to an nth emission line, a source connected to the third node N3, and a drain connected to a fourth node N4. In this case, the fourth node N4 may be connected to an anode of the light emitting device EL. The fourth transistor T4 may be turned on in response to a gate-on voltage of the nth emission signal EM(n) applied through the nth emission line. When the fourth transistor T4 is turned on, a current may flow between the third node N3 and the fourth node N4.

[0095] The light emitting device EL may include the anode connected to the fourth node N4 and a cathode to which a low-level power voltage VSS is applied. When the fourth transistor T4 is turned on, a driving current generated through the driving transistor DT may be applied to the anode of the light emitting device EL, and thus, the light emitting device EL may emit light. For example, the low-level power voltage VSS may be a voltage of -4V to -2.5V.

[0096] The fifth transistor T5 may include a gate connected to the nth scan line, a source connected to the anode of the light emitting device EL, and a drain connected to an initialization line. The fifth transistor T5 may be turned on in response to the gate-on voltage of the nth scan signal Scan(n) applied through the nth scan line. When the fifth transistor T5 is turned on, the anode of the light emitting device EL may be initialized based on an initialization voltage.

[0097] The sixth transistor T6 may include a gate connected to the nth emission line, a source connected to the high level power line, and a drain connected to a fifth node N5. The sixth transistor T6 may be turned on in response to the gate-on voltage of the nth emission signal EM(n) applied through the nth emission line. When the sixth transistor T6 is turned on, the high-level power voltage VDD may be applied to the fifth node N5.

[0098] The capacitor Cst may include a first electrode connected to the second node N2 and a second electrode connected to the fifth node N5.

[0099] The seventh transistor T7 may include a gate connected to the nth scan line, a source connected to a data line, and a drain connected to the fifth node N5. The seventh transistor T7 may be turned on in response to the gate-on voltage of the nth scan signal Scan(n) applied through the nth scan line. When the seventh transistor T7 is turned on, a data voltage Vdata may be applied to the fifth node N5.

[0100] The eighth transistor T8 may include a gate connected to an n-1st scan line, a source connected to the second node N2, and a drain connected to an initialization line. The eighth transistor T8 may be turned on in response to the gate-on voltage of an n-1st scan signal Scan(n-1) applied through the n-1st scan line. When the eighth transistor T8 is turned on, an initialization voltage Vini may be applied to the second node N2.

[0101] Moreover, a voltage applied to the gate of the driving transistor DT may control a turn-on state of the driving transistor DT, and thus, a transistor including a source or a drain connected to the gate of the driving transistor DT may include two or more transistors serially connected to each other, for maximally suppressing an influence of a leakage current. In this case, the two or more transistors may be controlled by the same control signal. Accordingly, in the nth subpixel SP according to the second embodiment of the present disclosure, the first transistor T1 and the eighth transistor T8 may each be implemented as a double-gate type transistor.

[0102] The nth subpixel SP according to the second embodiment of the present disclosure may operate in the order of an initialization period, a sampling period, a holding period, and an emission period. The initialization period may be a period where the gate of the driving transistor DT is initialized, the sampling period may be a period where a threshold voltage of the driving transistor DT is sampled and a data voltage Vdata is applied through a data line, and the holding period may be a period where the data voltage Vdata is held by a specific node and undesired emission of light caused by a delay of the scan signal is prevented. Also, the emission period may be a period where the light emitting device EL emits light with a driving current generated based on the data voltage Vdata.

[0103] The nth subpixel SP according to the second embodiment of the present disclosure may have an initialization period INI and a sampling period SAM during a period where a gate-off voltage of the nth emission signal EM(n) is applied, and thus, compensation based on an internal circuit may be performed. An operation characteristic during the periods will be described below. For example, a gate-on voltage of the scan signal may be applied during one horizontal periods 1H, and a gate-off voltage of an emission signal may be applied during three horizontal periods 3H. Also, for example, each of the initialization period INI, the sampling period SAM, and the holding period HLD may be executed during one horizontal period 1H. Driving of the pixel circuit will be described below with reference to the drawings.

[0104] FIG. 10A is a diagram for describing driving of the subpixel according to the second embodiment of the present disclosure in the initialization period. FIG. 10B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 10A.

[0105] In the initialization period INI, the n-1st scan signal Scan(n-1) may have a gate-on voltage, and the nth scan signal Scan(n) and the nth emission signal EM(n) may each have a gate-off voltage. For example, the gate-on voltage may be a logic low voltage VL and may be - 8V, and the gate-off voltage may be a logic high voltage VH and may be

8V. However, the present embodiment is not limited thereto.

[0106] The eighth transistor T8 may be turned on by the gate-on voltage applied through the n-1st scan line. An initialization voltage Vini may be applied to the second node N2 through the turned-on eighth transistor T8, and thus, the gate of the driving transistor DT may be initialized to the initialization voltage Vini. In this case, the initialization voltage Vini may be a voltage which is equal to or lower than the low-level power voltage VSS. For example, the initialization voltage Vini may be a voltage of -4V to -3V, and the data voltage Vdata may be a voltage which varies within a range of 0.3V to 6.3V, based on luminance.

[0107] During the initialization period INI, the gate of the driving transistor DT may be initialized based on the initialization voltage Vini.

[0108] FIG. 11A is a diagram for describing driving of the subpixel according to the second embodiment of the present disclosure in the sampling period. FIG. 11B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 11A.

[0109] In the sampling period SAM, the nth scan signal Scan(n) may have a gate-on voltage, and the n-1st scan signal Scan(n-1) and the nth emission signal EM(n) may each have a gate-off voltage.

[0110] The first transistor T1, the second transistor T2, the fifth transistor T5, and the seventh transistor T7 may be turned on by the gate-on voltage applied through the nth scan line. The reference voltage Vref may be applied to the source of the driving transistor DT through the turned-on second transistor T2, and the gate and the drain of the driving transistor DT may be connected to each other by the turned-on first transistor T1, whereby the driving transistor DT may be turned on and may be in the diode connection state. A voltage of the second node N2 connected to the gate of the driving transistor DT may increase up to a sum of the reference voltage Vref and a threshold voltage Vth of the driving transistor DT. Also, the data voltage Vdata may be applied to the fifth node N5 through the turned-on seventh transistor T7. Therefore, a voltage corresponding to the sum of the reference voltage Vref and the threshold voltage Vth of the driving transistor DT may be applied to the first electrode of the capacitor Cst, and the data voltage Vdata may be applied to the second electrode of the capacitor Cst, whereby the capacitor Cst may be charged with a difference voltage "Vdata-(Vref+Vth)" between the voltage applied to the first electrode and the data voltage applied to the second electrode. Also, the fifth transistor T5 may be turned on to initialize the anode of the light emitting device EL to the initialization voltage Vini. In this case, the reference voltage Vref may be a voltage which is higher than the low-level power voltage VSS and is lower than the high-level power voltage VDD. For example, the reference voltage Vref may be 4V, and the threshold voltage Vth may be -4V. However, the present embodiment is not limited thereto.

[0111] During the sampling period SAM, since the nth scan signal Scan(n) having the gate-on voltage is applied, one electrode of the capacitor Cst may be held by applying the data voltage Vdata to the fifth node N5, and by applying the reference voltage Vref to the source of the driving transistor DT, the second node N2 may sample the threshold voltage Vth of the driving transistor DT and may sense the reference voltage Vref.

[0112] FIG. 12A is a diagram for describing driving of the subpixel according to the second embodiment of the present disclosure in the holding period. FIG. 12B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 12A.

[0113] In the holding period HLD, the n-1st scan signal Scan(n-1), the nth scan signal Scan(n), and the nth emission signal EM(n) may each have a gate-on voltage, and thus, the first to eighth transistors T1 to T8 may be turned off.

[0114] In the holding period HLD, the nth scan signal Scan(n) may be shifted from the gate-on voltage to the gate-off voltage, and thus, a voltage at the gate of the driving transistor DT may slightly vary due to a parasitic capacitor of the first transistor T1. In this case, the driving transistor DT may be in a turn-off state.

[0115] For example, if the nth emission signal EM(n) is shifted to the gate-on voltage at a time when the nth scan signal Scan(n) is shifted from the gate-on voltage to the gate-off voltage, a sampling error occurs. The reason is because, as illustrated, the nth scan signal Scan(n) is not ideally shifted from a logic low voltage to a logic high voltage, and a time when the logic low voltage is shifted to the logic high voltage is delayed due to RC delay. In this case, if the nth emission signal EM(n) is shifted to the gate-on voltage, undesired emission of light occurs. Accordingly, the subpixel according to the second embodiment of the present disclosure may include the holding period HLD, thereby preventing undesired emission of light caused by a delay of a scan signal.

[0116] FIG. 13A is a diagram for describing driving of the subpixel according to the second embodiment of the present disclosure in the emission period. FIG. 13B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 13A.

[0117] In the emission period EMI, the nth emission signal EM(n) may have a gate-on voltage.

[0118] The third transistor T3, the fourth transistor T4, and the sixth transistor T6 may be turned on by the gate-on voltage of the nth emission signal EM(n) applied thereto. Therefore, the high-level power voltage VDD may be applied to the second electrode of the capacitor Cst, and thus, due to coupling of the capacitor Cst, a voltage of the second node N2 may become "Vref+Vth+(Vdd-Vdata)". Also, the high-level power voltage VDD may be applied to the source of the driving transistor DT, and thus, the driving transistor DT may be turned on. Also, the fourth transistor T4 may be turned on, and thus, may allow a current to flow between the third node N3 and the fourth node N4. Accordingly, a driving

current generated in the turned-on driving transistor DT may be applied to the anode of the light emitting device EL through the fourth transistor T4 to allow the light emitting device EL to emit light.

[0119] A current of the nth subpixel SP according to the second embodiment of the present disclosure may be expressed as the following Equation:

$$I_{oled} = K(V_{gs} - V_{th})^2 = K\{(V_{ref} + V_{th} + (V_{DD} - V_{data})) - V_{DD} - V_{th}\}^2 = K(V_{ref} - V_{data})^2$$

where I_{oled} denotes a current flowing through the light emitting device EL, K denotes a constant, V_{gs} denotes a voltage between the gate and the source of the driving transistor DT, V_{th} denotes the threshold voltage of the driving transistor DT, VDD denotes the high-level power voltage applied through the high level power line VDDL, V_{ref} denotes the reference voltage applied through the reference voltage line V_{refL} , and V_{data} denotes a data voltage applied through the data line DL. For example, the high-level power voltage VDD may be 4.6V.

[0120] As seen in the Equation, I_{oled} may be determined based on a difference between the reference voltage and the data voltage. According to the Equation, in the nth subpixel SP according to the second embodiment of the present disclosure, it can be seen that the voltage drop of the high-level power voltage is compensated for, based on the reference voltage V_{ref} which is applied to the source of the driving transistor DT in the sampling period SAM and the high-level power voltage VDD which is applied to the gate and the source of the driving transistor DT in the emission period EMI.

[0121] Therefore, a driving circuit for compensating for a sequential shift characteristic based on the voltage drop of the high-level power voltage may be implemented, and thus, an image quality issue such as the vertical luminance non-uniformity or crosstalk of a display device is solved.

[0122] Moreover, since the nth subpixel SP according to the second embodiment of the present disclosure includes the eighth transistor T8, the gate of the driving transistor DT may be initialized without adding the n+1st emission signal $EM(n+1)$, and thus, a size of an emission driver for providing an emission signal is reduced, thereby decreasing a size of a bezel which is a non-display area of an electroluminescent display device.

[0123] Moreover, the second and third transistors T2 and T3 of the plurality of transistors configuring the nth subpixel SP according to the second embodiment of the present disclosure may be disposed on one side of the non-display area and may be used in common by q number of subpixels disposed on an nth pixel line. Also, in a case where the gate driver 130 is disposed on each of the left and the right, the second and third transistors T2 and T3 may be disposed in each of a left non-display area and a right non-display area and may be used in common by q/2 number of subpixels. Therefore, the number of transistors configuring each subpixel is reduced, and thus, each subpixel is efficiently designed, thereby implementing a high-resolution display device. In this case, the other transistors (which are driving transistor DT, first transistor T1, fourth transistor T4, fifth transistor T5, sixth transistor T6, seventh transistor T7, the eighth transistor T8) except for the second and third transistors T2 and T3 among the plurality of transistors, the light emitting device EL and the capacitor Cst configuring the nth subpixel SP may be necessary for an individual operation of each subpixel SP are disposed in the display area, and thus, cannot be used in common by the nth pixel line. Accordingly, since the second and third transistors T2 and T3 are disposed in the non-display area, the high-resolution display device may be implemented.

[0124] FIG. 14 is a circuit diagram of a subpixel according to a third embodiment of the present disclosure. In comparison with FIG. 3, an eighth transistor T8 is added to the subpixel of FIG. 14, and the fourth transistor T4 illustrated in FIG. 3 is not applied to the subpixel of FIG. 14. FIG. 14 is a modification example which is implemented by modifying the pixel circuit of FIG. 3, and thus, overlapping descriptions are omitted or will be briefly described.

[0125] An nth subpixel SP may include first to third transistors T1 to T3, fifth to seventh transistors T5 to T7, a ninth transistor T9, a driving transistor DT, a capacitor Cst, and a light emitting device EL. In the third embodiment of the present disclosure, the nth subpixel SP may be implemented based on a total of eight transistors and one capacitor.

[0126] The driving transistor DT may include a source connected to a first node N1, a gate connected to a second node N2, and a drain connected to a third node N3. When a gate-on voltage is applied to the second node N2, the driving transistor DT may be turned on to provide a constant current to the third node N3.

[0127] The first transistor T1 may include a gate connected to an n+1st scan line, a source connected to the second node N2, and a drain connected to the third node N3. The first transistor T1 may be turned on in response to a gate-on voltage of an n+1st scan signal $Scan(n+1)$ applied through the n+1st scan line. When the first transistor T1 is turned on, the gate and the drain of the driving transistor DT may be electrically connected to each other, and thus, the driving transistor DT may be in a diode connection state.

[0128] The second transistor T2 may include a gate connected to an nth scan line, a source connected to a reference voltage line, and a drain connected to the first node N1. The second transistor T2 may be turned on in response to a gate-on voltage of an nth scan signal $Scan(n)$ applied through the nth scan line. When the second transistor T2 is turned on, a reference voltage V_{ref} may be applied to the first node N1.

[0129] The third transistor T3 may include a gate connected to an nth emission line, a source connected to a high

level power line, and a drain connected to the first node N1. The third transistor T3 may be turned on in response to a gate-on voltage of an nth emission signal EM(n) applied through the nth emission line. When the third transistor T3 is turned on, a high-level power voltage VDD may be applied to the first node N1.

[0130] The fifth transistor T5 may include a gate connected to an n-1st scan line, a source connected to a fourth node N4, and a drain connected to an initialization line. The fifth transistor T5 may be turned on in response to the gate-on voltage of the n-1st scan signal Scan(n-1) applied through an n-1st scan line. When the fifth transistor T5 is turned on, the anode of the light emitting device EL may be initialized based on an initialization voltage. In this case, the fourth node N4 may be the same node as the third node N3.

[0131] The light emitting device EL may include the anode connected to the fourth node N4 and a cathode to which a low-level power voltage VSS is applied. When a driving current generated through the driving transistor DT is applied to the anode of the light emitting device EL, the light emitting device EL may emit light. For example, the low-level power voltage VSS may be a voltage of -4V to -2.5V.

[0132] The sixth transistor T6 may include a gate connected to the nth emission line, a source connected to the high level power line, and a drain connected to a fifth node N5. The sixth transistor T6 may be turned on in response to the gate-on voltage of the nth emission signal EM(n) applied through the nth emission line. When the sixth transistor T6 is turned on, the high-level power voltage VDD may be applied to the fifth node N5.

[0133] The capacitor Cst may include a first electrode connected to the second node N2 and a second electrode connected to the fifth node N5.

[0134] The ninth transistor T9 may include a gate connected to the n-1st scan line, a source connected to the high level power line, and a drain connected to the fifth node N5. The ninth transistor T9 may be turned on in response to the gate-on voltage of the n-1st scan signal Scan(n-1) applied through the n-1st scan line. When the ninth transistor T9 is turned on, a high-level power voltage VDD may be applied to the fifth node N5.

[0135] The seventh transistor T7 may include a gate connected to the n+1st scan line, a source connected to a data line, and a drain connected to the fifth node N5. The seventh transistor T7 may be turned on in response to the gate-on voltage of the n+1st scan signal Scan(n+1) applied through the n+1st scan line. When the seventh transistor T7 is turned on, a data voltage Vdata may be applied to the fifth node N5.

[0136] Moreover, a voltage applied to the gate of the driving transistor DT may control a turn-on state of the driving transistor DT, and thus, a transistor including a source or a drain connected to the gate of the driving transistor DT may include two or more transistors serially connected to each other, for maximally suppressing an influence of a leakage current. In this case, the two or more transistors may be controlled by the same control signal. Accordingly, in the nth subpixel SP according to the third embodiment of the present disclosure, the first transistor T1 may be implemented as a double-gate type transistor.

[0137] The nth subpixel SP according to the third embodiment of the present disclosure may operate in the order of an initialization period, a first holding period, a sampling period, a second holding period, and an emission period. The initialization period may be a period where the anode of the light emitting device EL is initialized, the first holding period may be a period where a reference voltage Vref is applied to the source of the driving transistor DT, and the sampling period may be a period where the data voltage Vdata is applied to a specific node and a threshold voltage of the driving transistor DT is sampled. Also, the second holding period may be a period where the data voltage Vdata is held by the specific node, and the emission period may be a period where the light emitting device EL emits light with a driving current generated based on the data voltage Vdata.

[0138] The nth subpixel SP according to the third embodiment of the present disclosure may have an initialization period INI, a first holding period HLD1, a sampling period SAM, and a second holding period HLD2 during a period where a gate-off voltage of the nth emission signal EM(n) is applied, and thus, compensation based on an internal circuit may be performed. An operation characteristic during the periods will be described below. For example, a gate-on voltage of a scan signal may be applied during two horizontal periods 2H, and a gate-off voltage of an emission signal may be applied during four horizontal periods 4H. Also, for example, each of the initialization period INI, the first holding period HLD1, the sampling period SAM, and the second holding period HLD2 may be executed during one horizontal period 1H. Driving of the pixel circuit will be described below with reference to the drawings.

[0139] FIG. 15A is a diagram for describing driving of the subpixel according to the third embodiment of the present disclosure in the initialization period. FIG. 15B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 15A.

[0140] In the initialization period INI, the n-1st scan signal Scan(n-1) may have a gate-on voltage, and the nth scan signal Scan(n), the n+1st scan signal Scan(n+1), and the nth emission signal EM(n) may each have a gate-off voltage. For example, the gate-on voltage may be a logic low voltage VL and may be -8V, and the gate-off voltage may be a logic high voltage VH and may be 8V.

[0141] The fifth transistor T5 and the ninth transistor T9 may be turned on by the gate-on voltage applied through the n-1st scan line. An initialization voltage Vini may be applied to the fourth node N4 through the turned-on fifth transistor T5, and thus, the anode of the light emitting device EL may be initialized to the initialization voltage Vini. In this case,

the initialization voltage V_{ini} may be a voltage which is equal to or lower than the low-level power voltage V_{SS} . For example, the initialization voltage V_{ini} may be a voltage of -4V to -3V, and the data voltage V_{data} may be a voltage which varies within a range of 0.3V to 6.3V, based on luminance.

[0142] During the initialization period INI , the anode of the light emitting device EL may be initialized based on the initialization voltage V_{ini} , and the high-level power voltage V_{DD} may be applied to one electrode of the capacitor C_{st} .

[0143] FIG. 16A is a diagram for describing driving of the subpixel according to the third embodiment of the present disclosure in the first holding period. FIG. 16B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 16A.

[0144] In the first holding period $HLD1$, the $n-1$ st scan signal $Scan(n-1)$ and the n th scan signal $Scan(n)$ may each have a gate-on voltage, and the $n+1$ st scan signal $Scan(n+1)$ and the n th emission signal $EM(n)$ may each have a gate-off voltage. A period where the $n-1$ st scan signal $Scan(n-1)$ has the gate-on voltage and a period where the n th scan signal $Scan(n)$ has the gate-on voltage may overlap each other in the first holding period $HLD1$.

[0145] The fifth transistor $T5$ and the ninth transistor $T9$ may maintain a turn-on state with the gate-on voltage applied through the $n-1$ st scan line, and the second transistor $T2$ may be turned on by the gate-on voltage applied through the n th scan line. The initialization voltage V_{ini} applied to the anode of the light emitting device EL through the turned-on fifth transistor $T5$ may be held, the high-level power voltage V_{DD} applied to the fifth node $N5$ through the turned-on ninth transistor $T9$ may be held, and the reference voltage V_{ref} may be applied to the first node $N1$ through the turned-on second transistor $T2$.

[0146] FIG. 17A is a diagram for describing driving of the subpixel according to the third embodiment of the present disclosure in the sampling period. FIG. 17B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 17A.

[0147] In the sampling period SAM , the n th scan signal $Scan(n)$ and the $n+1$ st scan signal $Scan(n+1)$ may each have a gate-on voltage, and the $n-1$ st scan signal $Scan(n-1)$ and the n th emission signal $EM(n)$ may each have a gate-off voltage.

[0148] The second transistor $T2$ may maintain a turn-on state with the gate-on voltage applied through the n th scan line, and the first transistor $T1$ may be turned on by the gate-on voltage applied through the $n+1$ st scan line, whereby the driving transistor DT may be in the diode connection state. The reference voltage V_{ref} applied through the turned-on second transistor $T2$ may be held by the source of the driving transistor DT , and the gate and the drain of the driving transistor DT may be connected to each other by the turned-on first transistor $T1$, whereby the driving transistor DT may be turned on. A voltage of the second node $N2$ connected to the gate of the driving transistor DT may increase up to a sum of the reference voltage V_{ref} and a threshold voltage V_{th} of the driving transistor DT . Also, the data voltage V_{data} may be applied to the fifth node $N5$ by the seventh transistor $T7$ which is turned on by the gate-on voltage applied through the $n+1$ st scan line. Therefore, a voltage corresponding to the sum of the reference voltage V_{ref} and the threshold voltage V_{th} of the driving transistor DT may be applied to the first electrode of the capacitor C_{st} , and the data voltage V_{data} may be applied to the second electrode of the capacitor C_{st} , whereby the capacitor C_{st} may be charged with a difference voltage " $V_{data}-(V_{ref}+V_{th})$ " between the voltage applied to the first electrode and the data voltage applied to the second electrode. In this case, the reference voltage V_{ref} may be a voltage which is higher than the low-level power voltage V_{SS} and is lower than the high-level power voltage V_{DD} . For example, the reference voltage V_{ref} may be 4V, and the threshold voltage V_{th} may be -4V. However, the present embodiment is not limited thereto.

[0149] During the sampling period SAM , since the n th scan signal $Scan(n)$ and the $n+1$ st scan signal $Scan(n+1)$ having the gate-on voltage are applied, one electrode of the capacitor C_{st} may be held by applying the data voltage V_{data} to the fifth node $N5$, and by applying the reference voltage V_{ref} to the source of the driving transistor DT , the second node $N2$ may sample the threshold voltage V_{th} of the driving transistor DT and may sense the reference voltage V_{ref} .

[0150] FIG. 18A is a diagram for describing driving of the subpixel according to the third embodiment of the present disclosure in the second holding period. FIG. 18B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 18A.

[0151] In the second holding period $HLD2$, the $n+1$ st scan signal $Scan(n+1)$ may hold a gate-on voltage, and the $n-1$ st scan signal $Scan(n-1)$, the n th scan signal $Scan(n)$, and the n th emission signal $EM(n)$ may each have a gate-off voltage.

[0152] The first transistor $T1$ and the seventh transistor $T7$ may maintain a turn-on state with the gate-on voltage applied through the $n+1$ st scan signal $Scan(n+1)$. In the second holding period $HLD2$, the capacitor C_{st} may be charged with the data voltage V_{data} and may hold the data voltage V_{data} , based on a voltage difference between both ends thereof.

[0153] FIG. 19A is a diagram for describing driving of the subpixel according to the third embodiment of the present disclosure in the emission period. FIG. 19B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 19A.

[0154] In the emission period EMI , the n th emission signal $EM(n)$ may have a gate-on voltage, and the $n-1$ st scan signal $Scan(n-1)$, the n th scan signal $Scan(n)$, and the $n+1$ st scan signal $Scan(n+1)$ may each have a gate-off voltage.

[0155] The third transistor $T3$ and the sixth transistor $T6$ may be turned on by the gate-on voltage of the n th emission signal $EM(n)$ applied thereto. The high-level power voltage V_{DD} may be applied to the first node $N1$ through the turned-

on third transistor T3, and the high-level power voltage VDD may be applied to the fifth node N5 through the turned-on sixth transistor T6. A voltage of the fifth node N5 connected to the second electrode of the capacitor Cst may be shifted from the data voltage Vdata to the high-level power voltage VDD, and due to coupling of the capacitor Cst, a voltage at the first electrode of the capacitor Cst may vary by a voltage variation of the fifth node N5. Therefore, a voltage of the second node N2 connected to the first electrode of the capacitor Cst may become "Vref+Vth+(VDD-Vdata)". In this case, since the high-level power voltage VDD is applied to the source of the driving transistor DT, the driving transistor DT may be turned on to apply a driving current to the anode of the light emitting device EL. Therefore, the light emitting device EL may emit light. For example, the high-level power voltage VDD may be 4.6V.

[0156] In the nth subpixel SP according to the third embodiment of the present disclosure, the high-level power voltage VDD may be applied to each of the source and the gate of the driving transistor DT, in order to consider the voltage drop of the high-level power voltage VDD. Therefore, a current of the nth subpixel SP which has been compensated for may be expressed as the following Equation:

$$I_{oled} = K(V_{gs} - V_{th})^2 = K\{(V_{ref} + V_{th} + (V_{DD} - V_{data})) - V_{DD} - V_{th}\}^2 = K(V_{ref} - V_{data})^2$$

where I_{oled} denotes a current flowing through the light emitting device EL, K denotes a constant, V_{gs} denotes a voltage between the gate and the source of the driving transistor DT, V_{th} denotes the threshold voltage of the driving transistor DT, VDD denotes the high-level power voltage applied through the high level power line VDDL, Vref denotes the reference voltage applied through the reference voltage line VrefL, and Vdata denotes a data voltage applied through the data line DL.

[0157] As seen in the Equation, I_{oled} may be determined based on a difference between the reference voltage and the data voltage. According to the Equation, in the nth subpixel SP according to the third embodiment of the present disclosure, it can be seen that the voltage drop of the high-level power voltage is compensated for, based on the high-level power voltage VDD which is applied to the gate and the source of the driving transistor DT in the emission period EMI and the reference voltage Vref which is applied to the source of the driving transistor DT in the sampling period SAM.

[0158] Therefore, a driving circuit for compensating for a sequential shift characteristic based on the voltage drop of the high-level power voltage may be implemented, and thus, an image quality issue such as the vertical luminance non-uniformity or crosstalk of a display device is solved.

[0159] Moreover, the second and third transistors T2 and T3 of the plurality of transistors configuring the nth subpixel SP according to the third embodiment of the present disclosure may be disposed on one side of the non-display area and may be used in common by q number of subpixels disposed on an nth pixel line. Also, in a case where the gate driver 130 is disposed on each of the left and the right, the second and third transistors T2 and T3 may be disposed in each of a left non-display area and a right non-display area and may be used in common by q/2 number of subpixels. Therefore, the number of transistors configuring each subpixel is reduced, and thus, each subpixel is efficiently designed, thereby implementing a high-resolution display device. In this case, the other transistors (which are driving transistor DT, first transistor T1, the fifth transistor T5, sixth transistor T6, seventh transistor T7, the ninth transistor T9) except for the second and third transistors T2 and T3 among the plurality of transistors, the light emitting device EL and the capacitor Cst configuring the nth subpixel SP may be necessary for an individual operation of each subpixel SP are disposed in the display area, and thus, cannot be used in common by the nth pixel line. Accordingly, since the second and third transistors T2 and T3 are disposed in the non-display area, the high-resolution display device may be implemented.

[0160] FIG. 20 is a circuit diagram of a subpixel according to a fourth embodiment of the present disclosure. FIG. 20 is a modification example where two transistors are added to the pixel circuit of FIG. 3, and thus, overlapping descriptions are omitted or will be briefly described.

[0161] An nth subpixel SP according to a fourth embodiment of the present disclosure may include first to ninth transistors T1 to T9, a driving transistor DT, a capacitor Cst, and a light emitting device EL. In the third embodiment of the present disclosure, the nth subpixel SP may be implemented based on a total of ten transistors and one capacitor.

[0162] The driving transistor DT may include a source connected to a first node N1, a gate connected to a second node N2, and a drain connected to a third node N3. When a gate-on voltage is applied to the second node N2, the driving transistor DT may be turned on to provide a constant current to the third node N3.

[0163] The first transistor T1 may include a gate connected to an nth scan line, a source connected to the second node N2, and a drain connected to the third node N3. The first transistor T1 may be turned on in response to a gate-on voltage of an nth scan signal Scan(n) applied through the nth scan line. When the first transistor T1 is turned on, the gate and the drain of the driving transistor DT may be electrically connected to each other, and thus, the driving transistor DT may be in a diode connection state.

[0164] The second transistor T2 may include a gate connected to the nth scan line, a source connected to a reference voltage line, and a drain connected to the first node N1. The second transistor T2 may be turned on in response to a gate-on voltage of an nth scan signal Scan(n) applied through the nth scan line. When the second transistor T2 is turned

on, a reference voltage V_{ref} may be applied to the first node N1.

[0165] The third transistor T3 may include a gate connected to an nth emission line, a source connected to a high level power line, and a drain connected to the first node N1. The third transistor T3 may be turned on in response to a gate-on voltage of an nth emission signal EM(n) applied through the nth emission line. When the third transistor T3 is turned on, a high-level power voltage VDD may be applied to the first node N1.

[0166] The fourth transistor T4 may include a gate connected to an nth emission line, a source connected to the third node N3, and a drain connected to a fourth node N4. In this case, the fourth node N4 may be connected to an anode of the light emitting device EL. The fourth transistor T4 may be turned on in response to a gate-on voltage of the nth emission signal EM(n) applied through the nth emission line. When the fourth transistor T4 is turned on, a current may flow between the third node N3 and the fourth node N4.

[0167] The fifth transistor T5 may include a gate connected to the nth scan line, a source connected to the fourth node N4, and a drain connected to an initialization line. The fifth transistor T5 may be turned on in response to the gate-on voltage of the nth scan signal Scan(n) applied through the nth scan line. When the fifth transistor T5 is turned on, an initialization voltage Vini may be applied to the fourth node N4, and thus, the anode of the light emitting device EL may be initialized.

[0168] The sixth transistor T6 may include a gate connected to the nth emission line, a source connected to the high level power line, and a drain connected to a fifth node N5. The sixth transistor T6 may be turned on in response to the gate-on voltage of the nth emission signal EM(n) applied through the nth emission line.

[0169] The ninth transistor T9 may include a gate connected to the n-1st scan line, a source connected to the high level power line, and a drain connected to the fifth node N5. The ninth transistor T9 may be turned on in response to the gate-on voltage of the n-1st scan signal Scan(n-1) applied through the n-1st scan line. When the ninth transistor T9 is turned on, a high-level power voltage VDD may be applied to the fifth node N5.

[0170] The capacitor Cst may include a first electrode connected to the second node N2 and a second electrode connected to the fifth node N5.

[0171] The seventh transistor T7 may include a gate connected to the nth scan line, a source connected to a data line, and a drain connected to the fifth node N5. The seventh transistor T7 may be turned on in response to the gate-on voltage of the nth scan signal Scan(n) applied through the nth scan line. When the seventh transistor T7 is turned on, a data voltage Vdata may be applied to the fifth node N5.

[0172] The eighth transistor T8 may include a gate connected to an n-1st scan line, a source connected to the second node N2, and a drain connected to an initialization line. The eighth transistor T8 may be turned on in response to the gate-on voltage of an n-1st scan signal Scan(n-1) applied through the n-1st scan line. When the eighth transistor T8 is turned on, an initialization voltage Vini may be applied to the second node N2.

[0173] The light emitting device EL may include the anode connected to the fourth node N4 and a cathode to which a low-level power voltage VSS is applied. When the fourth transistor T4 is turned on, a driving current generated through the driving transistor DT may be applied to the anode of the light emitting device EL, and thus, the light emitting device EL may emit light. For example, the low-level power voltage VSS may be a voltage of -4V to -2.5V, but is not limited thereto.

[0174] Moreover, a voltage applied to the gate of the driving transistor DT may control a turn-on state of the driving transistor DT, and thus, a transistor including a source or a drain connected to the gate of the driving transistor DT may include two or more transistors serially connected to each other, for maximally suppressing an influence of a leakage current. In this case, the two or more transistors may be controlled by the same control signal. Accordingly, in the nth subpixel SP according to the fourth embodiment of the present disclosure, the first transistor T1 and the eighth transistor T8 may each be implemented as a double-gate type transistor.

[0175] The nth subpixel SP according to the fourth embodiment of the present disclosure may operate in the order of an initialization period, a sampling period, a holding period, and an emission period. The initialization period may be a period where the gate of the driving transistor DT is initialized, the sampling period may be a period where a threshold voltage of the driving transistor DT is sampled and a data voltage Vdata is applied through a data line, and the holding period may be a period where undesired emission of light caused by a delay of the scan signal is prevented. Also, the emission period may be a period where the light emitting device EL emits light with a driving current generated based on the data voltage Vdata.

[0176] The nth subpixel SP according to the fourth embodiment of the present disclosure may have an initialization period INI and a sampling period SAM during a period where a gate-off voltage of the nth emission signal EM(n) is applied, and thus, compensation based on an internal circuit may be performed. An operation characteristic during the periods will be described below. For example, a gate-on voltage of the scan signal may be applied during one horizontal period 1H, and a gate-off voltage of an emission signal may be applied during three horizontal periods 3H. Also, for example, each of the initialization period INI, the sampling period SAM, and the holding period HLD may be executed during one horizontal period 1H. Driving of the pixel circuit will be described below with reference to the drawings.

[0177] FIG. 21A is a diagram for describing driving of the subpixel according to the fourth embodiment of the present disclosure in the initialization period. FIG. 21B is a waveform diagram for describing driving of the subpixel illustrated in

FIG. 21A.

[0178] In the initialization period INI, the n-1st scan signal Scan(n-1) may have a gate-on voltage, and the nth scan signal Scan(n) and the nth emission signal EM(n) may each have a gate-off voltage. For example, the gate-on voltage may be a logic low voltage VL and may be - 8V, and the gate-off voltage may be a logic high voltage VH and may be 8V. However, the present embodiment is not limited thereto.

[0179] The ninth transistor T9 and the eighth transistor T8 may be turned on by the gate-on voltage applied through the n-1st scan line. The high-level power voltage VDD may be applied to the fifth node N5 through the turned-on ninth transistor T9, and an initialization voltage Vini may be applied to the second node N2 through the turned-on eighth transistor T8, whereby the gate of the driving transistor DT may be initialized to the initialization voltage Vini. In this case, the initialization voltage Vini may be a voltage which is equal to or lower than the low-level power voltage VSS. For example, the initialization voltage Vini may be a voltage of -4V to -3V, and the data voltage Vdata may be a voltage which varies within a range of 0.3V to 6.3V, based on luminance.

[0180] During the initialization period INI, the gate of the driving transistor DT may be initialized based on the initialization voltage Vini.

[0181] FIG. 22A is a diagram for describing driving of the subpixel according to the fourth embodiment of the present disclosure in the sampling period. FIG. 22B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 22A.

[0182] In the sampling period SAM, the nth scan signal Scan(n) may have a gate-on voltage, and the n-1st scan signal Scan(n-1) and the nth emission signal EM(n) may each have a gate-off voltage.

[0183] The first transistor T1, the second transistor T2, the fifth transistor T5, and the seventh transistor T7 may be turned on by the gate-on voltage applied through the nth scan line. The reference voltage Vref may be applied to the source of the driving transistor DT through the turned-on second transistor T2, and the gate and the drain of the driving transistor DT may be connected to each other by the turned-on first transistor T1, whereby the driving transistor DT may be turned on and may be in the diode connection state. A voltage of the second node N2 connected to the gate of the driving transistor DT may increase up to a sum of the reference voltage Vref and a threshold voltage Vth of the driving transistor DT. Also, the data voltage Vdata may be applied to the fifth node N5 through the turned-on seventh transistor T7. Therefore, a voltage corresponding to the sum of the reference voltage Vref and the threshold voltage Vth of the driving transistor DT may be applied to the first electrode of the capacitor Cst, and the data voltage Vdata may be applied to the second electrode of the capacitor Cst, whereby the capacitor Cst may be charged with a difference voltage "Vdata-(Vref+Vth)" between the voltage applied to the first electrode and the data voltage applied to the second electrode. Also, the fifth transistor T5 may be turned on to initialize the anode of the light emitting device EL to the initialization voltage Vini. For example, the reference voltage Vref may be 4V, and the threshold voltage Vth may be -4V. However, the present embodiment is not limited thereto.

[0184] During the sampling period SAM, since the nth scan signal Scan(n) having the gate-on voltage is applied, one electrode of the capacitor Cst may be held by applying the data voltage Vdata to the fifth node N5, and by applying the reference voltage Vref to the source of the driving transistor DT, the second node N2 may sample the threshold voltage Vth of the driving transistor DT and may sense the reference voltage Vref.

[0185] FIG. 23A is a diagram for describing driving of the subpixel according to the fourth embodiment of the present disclosure in the holding period. FIG. 23B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 23A.

[0186] In the holding period HLD, the n-1st scan signal Scan(n-1), the nth scan signal Scan(n), and the nth emission signal EM(n) may each have a gate-on voltage, and thus, the first to ninth transistors T1 to T9 may be turned off.

[0187] In the holding period HLD, the nth scan signal Scan(n) may be shifted from the gate-on voltage to the gate-off voltage, and thus, a voltage at the gate of the driving transistor DT may slightly vary due to a parasitic capacitor of the first transistor T1. In this case, the driving transistor DT may be in a turn-off state.

[0188] For example, if the nth emission signal EM(n) is shifted to the gate-on voltage at a time when the nth scan signal Scan(n) is shifted from the gate-on voltage to the gate-off voltage, a sampling error occurs. The reason is because, as illustrated in the drawing, the nth scan signal Scan(n) is not ideally shifted from a logic low voltage to a logic high voltage, and a time when the logic low voltage is shifted to the logic high voltage is delayed due to RC delay. In this case, if the nth emission signal EM(n) is shifted to the gate-on voltage, undesired emission of light occurs. Accordingly, the subpixel according to the fourth embodiment of the present disclosure may include the holding period HLD, thereby preventing undesired emission of light caused by a delay of a scan signal.

[0189] FIG. 24A is a diagram for describing driving of the subpixel according to the fourth embodiment of the present disclosure in the emission period. FIG. 24B is a waveform diagram for describing driving of the subpixel illustrated in FIG. 24A.

[0190] In the emission period EMI, the nth emission signal EM(n) may have a gate-on voltage.

[0191] The third transistor T3, the sixth transistor T6, and the fourth transistor T4 may be turned on by the gate-on voltage of the nth emission signal EM(n) applied thereto. Therefore, the high-level power voltage VDD may be applied

to the second electrode of the capacitor Cst, and thus, due to coupling of the capacitor Cst, a voltage of the second node N2 may become "Vref+Vth+(Vdd-Vdata)". Also, the high-level power voltage VDD may be applied to the source of the driving transistor DT, and thus, the driving transistor DT may be turned on. Also, the fourth transistor T4 may be turned on, and thus, may allow a current to flow between the third node N3 and the fourth node N4. Accordingly, a driving current generated in the turned-on driving transistor DT may be applied to the anode of the light emitting device EL through the fourth transistor T4 to allow the light emitting device EL to emit light. The fourth transistor T5 may maintain a turn-off state in a period other than the emission period EMI, thereby preventing undesired emission of light.

[0192] A current of the nth subpixel SP according to the fourth embodiment of the present disclosure may be expressed as the following Equation:

$$I_{oled} = K(V_{gs} - V_{th})^2 = K\{(V_{ref} + V_{th} + (V_{DD} - V_{data})) - V_{DD} - V_{th}\}^2 = K(V_{ref} - V_{data})^2$$

where I_{oled} denotes a current flowing through the light emitting device EL, K denotes a constant, V_{gs} denotes a voltage between the gate and the source of the driving transistor DT, V_{th} denotes the threshold voltage of the driving transistor DT, V_{DD} denotes the high-level power voltage applied through the high level power line VDDL, V_{ref} denotes the reference voltage applied through the reference voltage line VrefL, and V_{data} denotes a data voltage applied through the data line DL. For example, the high-level power voltage VDD may be 4.6V.

[0193] As seen in the Equation, I_{oled} may be determined based on a difference between the reference voltage and the data voltage. According to the Equation, in the nth subpixel SP according to the fourth embodiment of the present disclosure, it can be seen that the voltage drop of the high-level power voltage is compensated for, based on the reference voltage V_{ref} which is applied to the source of the driving transistor DT in the sampling period SAM and the high-level power voltage VDD which is applied to the gate and the source of the driving transistor DT in the emission period EMI.

[0194] Therefore, a driving circuit for compensating for a sequential shift characteristic based on the voltage drop of the high-level power voltage may be implemented, and thus, an image quality issue such as the vertical luminance non-uniformity or crosstalk of a display device is solved.

[0195] Moreover, since the nth subpixel SP according to the fourth embodiment of the present disclosure includes the eighth transistor T8, the gate of the driving transistor DT may be initialized, thereby preventing an increase in luminance of a black screen of the display panel.

[0196] Moreover, the second and third transistors T2 and T3 of the plurality of transistors configuring the nth subpixel SP according to the fourth embodiment of the present disclosure may be disposed on one side of the non-display area and may be used in common by q number of subpixels disposed on an nth pixel line. Also, in a case where the gate driver 130 is disposed on each of the left and the right, the second and third transistors T2 and T3 may be disposed in each of a left non-display area and a right non-display area and may be used in common by q/2 number of subpixels. Therefore, the number of transistors configuring each subpixel is reduced, and thus, each subpixel is efficiently designed, thereby implementing a high-resolution display device. In this case, the other transistors (which are driving transistor DT, first transistor T1, fourth transistor T4, fifth transistor T5, sixth transistor T6, seventh transistor T7, the eighth transistor T8, the ninth transistor T9) except for the second and third transistors T2 and T3 among the plurality of transistors, the light emitting device EL and the capacitor Cst configuring the nth subpixel SP may be necessary for an individual operation of each subpixel, and thus, cannot be used in common by the nth pixel line. Accordingly, since the second and third transistors T2 and T3 are disposed in the non-display area, the high-resolution display device may be implemented.

[0197] The electroluminescent display device according to embodiments of the present disclosure will be described as follows.

[0198] In an electroluminescent display device according to an embodiment of the present disclosure, the electroluminescent display device includes a display panel including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an nth (where n is a natural number) pixel line of the plurality of pixel lines includes a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an n-1st scan signal, a second transistor applying a reference voltage to the first node in response to an nth scan signal, a third transistor applying a high-level power voltage to the first node in response to an nth emission signal, a fourth transistor allowing a current to flow between the third node and a fourth node in response to an n+1st emission signal, a fifth transistor applying an initialization voltage to the fourth node in response to the n-1st scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a seventh transistor applying a data voltage to the fifth node in response to the n-1st scan signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an anode connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. The display panel may include a display area and a non-display area. Accordingly, a subpixel supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electrolumi-

nescent display device.

[0199] According to another feature of the present disclosure, the reference voltage may be a voltage which is higher than the low-level power voltage and is lower than the high-level power voltage, the initialization voltage may be a voltage which is equal to or lower than the low-level power voltage, and a period where the n-1st scan signal has a gate-on voltage and a period where the nth scan signal has the gate-on voltage may overlap each other.

[0200] According to another feature of the present disclosure, the n-1st scan signal and the nth scan signal may be activated to the gate-on voltage during two horizontal periods, and the nth emission signal and the n+1st emission signal may be deactivated to a gate-off voltage during three horizontal periods.

[0201] According to another feature of the present disclosure, one frame for driving each of the plurality of pixel circuits may include an initialization period where a gate-on voltage of the n-1st scan signal is input to an n-1st pixel line and the gate-on voltage of the n+1st emission signal is held by an n+1st pixel line, a sampling period where the gate-on voltage of the n-1st scan signal is held by the n-1st pixel line and the gate-on voltage of the nth scan signal is input to an nth pixel line, a holding period where the gate-on voltage of the nth scan signal is held by the nth pixel line, a programming period where the gate-on voltage of the nth emission signal is input to the nth pixel line, and an emission period where the light emitting device emits light. Also, in the initialization period, the first transistor, the fourth transistor, the fifth transistor, and the seventh transistor may be turned on, and in the sampling period, the first transistor, the second transistor, the fifth transistor, and the seventh transistor may be turned on. Also, in the holding period, the second transistor may be turned on, and in the programming period, the third transistor and the sixth transistor may be turned on. Also, in the emission period, the third transistor, the fourth transistor, and the sixth transistor may be turned on.

[0202] According to another feature of the present disclosure, the first transistor may be a double-gate type transistor.

[0203] In an electroluminescent display device according to an embodiment of the present disclosure, the electroluminescent display device includes a display panel including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an nth pixel line of the plurality of pixel lines includes a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an nth scan signal, a second transistor applying a reference voltage to the first node in response to the nth scan signal, a third transistor applying a high-level power voltage to the first node in response to an nth emission signal, a fourth transistor allowing a current to flow between the third node and a fourth node in response to the nth emission signal, a fifth transistor applying an initialization voltage to the fourth node in response to the nth scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a seventh transistor applying a data voltage to the fifth node in response to the nth scan signal, an eighth transistor supplying an initialization voltage to the second node in response to an n-1st scan signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an node connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. The display panel may include a display area and a non-display area. Accordingly, a subpixel supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electroluminescent display device.

[0204] According to another feature of the present disclosure, one frame for driving each of the plurality of pixel circuits may include an initialization period where a gate-on voltage of the n-1st scan signal is input to an n-1st pixel line, a sampling period where the gate-on voltage of the nth scan signal is input to an nth pixel line, a holding period where a gate-off voltage of each of the n-1st scan signal and the nth scan signal is input to the nth pixel line, and an emission period where the gate-on voltage of the nth emission signal is input to the nth pixel line. Also, in the initialization period, the eighth transistor may be turned on, and in the sampling period, the first transistor, the second transistor, the fifth transistor, and the seventh transistor may be turned on. Also, in the holding period, the first to eighth transistors may be turned off, and in the emission period, the third transistor, the fourth transistor, and the sixth transistor may be turned on.

[0205] According to another feature of the present disclosure, in the initialization period, the sampling period, and the holding period, the nth emission signal may have the gate-off voltage.

[0206] According to another feature of the present disclosure, the n-1st scan signal and the nth scan signal may be activated to the gate-on voltage during one horizontal period, and the nth emission signal may be deactivated to the gate-off voltage during three horizontal periods.

[0207] According to another feature of the present disclosure, each of the first transistor and the eighth transistor may be a double-gate type transistor.

[0208] In an electroluminescent display device according to an embodiment of the present disclosure, the electroluminescent display device includes a display panel including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an nth pixel line of the plurality of pixel lines includes a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an n+1st scan signal, a second transistor applying a reference voltage to the first node in response to an nth scan signal, a third transistor applying a high-level power voltage to the first node in response to an nth emission signal, a fifth transistor applying an

initialization voltage to the fourth node in response to an n-1st scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a ninth transistor applying the high-level power voltage to the fifth node in response to the n-1st scan signal, a seventh transistor applying a data voltage to the fifth node in response to the n+1st scan signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an node connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. The display panel may include a display area and a non-display area. Accordingly, a subpixel supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electroluminescent display device.

[0209] According to another feature of the present disclosure, the reference voltage may be a voltage which is higher than the low-level power voltage and is lower than the high-level power voltage, the initialization voltage may be a voltage which is equal to or lower than the low-level power voltage, and a period where the n-1st scan signal has a gate-on voltage and a period where the nth scan signal has the gate-on voltage may overlap each other.

[0210] According to another feature of the present disclosure, the n-1st scan signal and the nth scan signal may be activated to the gate-on voltage during two horizontal periods, and the nth emission signal may be deactivated to a gate-off voltage during four horizontal periods.

[0211] According to another feature of the present disclosure, one frame for driving each of the plurality of pixel circuits may include an initialization period where a gate-on voltage of the n-1st scan signal is input to an n-1st pixel line, a first holding period where the gate-on voltage of the n-1st scan signal is held by the n-1st pixel line and the gate-on voltage of the nth scan signal is input to an nth pixel line, a sampling period where the gate-on voltage of the nth scan signal is held by the nth pixel line and the gate-on voltage of the n+1st scan signal is input to an n+1st pixel line, a second holding period where the gate-on voltage of the n+1st scan signal is held by the n+1st pixel line, and an emission period where the light emitting device emits light. Also, in the initialization period, the fifth transistor and the ninth transistor may be turned on, and in the first holding period, the second transistor, the fifth transistor, and the ninth transistor may be turned on. Also, in the sampling period, the first transistor, the second transistor, and the seventh transistor may be turned on, and in the second holding period, the first transistor and the seventh may be turned on. Also, in the emission period, the third transistor and the sixth transistor may be turned on.

[0212] According to another feature of the present disclosure, the first transistor may be a double-gate type transistor.

[0213] In an electroluminescent display device according to an embodiment of the present disclosure, the electroluminescent display device includes a display panel including a plurality of pixel lines each including a plurality of pixel circuits. Also, each of the plurality of pixel circuits included in an nth pixel line of the plurality of pixel lines includes a driving transistor connected between a first node and a third node and including a gate connected to a second node, a first transistor allowing a current to flow between the second node and the third node in response to an nth scan signal, a second transistor applying a reference voltage to the first node in response to the nth scan signal, a third transistor applying a high-level power voltage to the first node in response to an nth emission signal, a fifth transistor applying an initialization voltage to a fourth node in response to the nth scan signal, a sixth transistor applying the high-level power voltage to a fifth node in response to the nth emission signal, a ninth transistor applying the high-level power voltage to a fifth node in response to an n-1st scan signal, a seventh transistor applying a data voltage to the fifth node in response to the nth scan signal, an eighth transistor supplying an initialization voltage to the second node in response to the n-1st scan signal, a fourth transistor allowing a current to flow between the third node and a fourth node in response to the nth emission signal, a capacitor connected between the second node and the fifth node, and a light emitting device including an node connected to the fourth node and a cathode connected to a line to which a low-level power voltage is applied. The display panel may include a display area and a non-display area. Accordingly, a subpixel supplied with the reference voltage may provide the light emitting device with a driving current unaffected by the high-level power voltage, thereby solving an image quality issue of the electroluminescent display device.

[0214] According to another feature of the present disclosure, one frame for driving each of the plurality of pixel circuits may include an initialization period where a gate-on voltage of the n-1st scan signal is input to an n-1st pixel line, a sampling period where the gate-on voltage of the nth scan signal is input to an nth pixel line, a holding period where a gate-off voltage of each of the n-1st scan signal and the nth scan signal is input to the nth pixel line, and an emission period where the gate-on voltage of the nth emission signal is input to the nth pixel line. Also, in the initialization period, the ninth transistor and the eighth transistor may be turned on, and in the sampling period, the first transistor, the second transistor, the fifth transistor, and the seventh transistor may be turned on. Also, in the holding period, the first to ninth transistors may be turned off, and in the emission period, the third transistor, the sixth transistor, and the fourth transistor may be turned on.

[0215] According to another feature of the present disclosure, in the initialization period, the sampling period, and the holding period, the nth emission signal may have the gate-off voltage.

[0216] According to another feature of the present disclosure, the n-1st scan signal and the nth scan signal may be activated to the gate-on voltage during one horizontal period, and the nth emission signal may be deactivated to the gate-off voltage during three horizontal periods.

[0217] According to another feature of the present disclosure, each of the first transistor and the eighth transistor may be a double-gate type transistor.

[0218] According to another feature of the present disclosure, the second transistor and the third transistor may be in the non-display area.

[0219] According to another feature of the present disclosure, the second transistor and the third transistor may be used in common by each the plurality of pixel lines.

[0220] According to another feature of the present disclosure, the initialization voltage may be equal to or lower than the low-level power voltage, and the reference voltage may be higher than the low-level power voltage and lower than the high-level power voltage.

[0221] As described above, according to the embodiments of the present disclosure, a pixel circuit for compensating for a sequential shift characteristic based on the voltage drop of a source voltage may be implemented, thereby solving an image quality issue such as the vertical luminance non-uniformity or cross-talk of a display panel.

[0222] Moreover, according to the embodiments of the present disclosure, some of a plurality of transistors for driving each pixel circuit may be disposed in a non-display area and may be used in common by pixel circuits connected to the same pixel line, and thus, an efficiency of designing pixel circuits is enhanced, thereby realizing a high-resolution display device.

[0223] It will be apparent to those skilled in the art that various modifications and variations can be made in the electroluminescent display device of the present disclosure without departing from the technical idea or scope of the disclosures. Thus, it is intended that the present disclosure covers the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

Claims

1. An electroluminescent display device comprising:

a display panel (150) including a display area and a non-display area,
wherein the display panel (150) including a plurality of pixel lines each including a plurality of pixel circuits,
wherein each of the plurality of pixel circuits included in an nth (where n is a natural number) pixel line of the
plurality of pixel lines comprises:

a driving transistor (DT) connected between a first node (N1) and a third node (N3), the driving transistor (DT) including a gate connected to a second node (N2);

a first transistor (T1) allowing a current to flow between the second node (N2) and the third node (N3) in response to an nth scan signal (Scan (n));

a second transistor (T2) applying a reference voltage (Vref) to the first node (N1) in response to the nth scan signal (Scan (n));

a third transistor (T3) applying a high-level power voltage (VDD) to the first node (N1) in response to an nth emission signal (EM(n));

a fourth transistor (T4) allowing a current to flow between the third node (N3) and a fourth node (N4) in response to the nth emission signal (EM(n));

a fifth transistor (T5) applying an initialization voltage (Vini) to the fourth node (N4) in response to the nth scan signal (Scan (n));

a sixth transistor (T6) applying the high-level power voltage (VDD) to a fifth node (N5) in response to the nth emission signal (EM(n));

a seventh transistor (T7) applying a data voltage to the fifth node (N5) in response to the nth scan signal (Scan (n));

an eighth transistor (T8) supplying an initialization voltage (Vini) to the second node (N2) in response to an n-1st scan signal (Scan(n-1));

a capacitor (Cst) connected between the second node (N2) and the fifth node (N5); and

a light emitting device (EL) including an anode connected to the fourth node (N4) and a cathode connected to a line to which a low-level power voltage (VSS) is applied.

2. The electroluminescent display device of claim 1, wherein

one frame for driving each of the plurality of pixel circuits comprises an initialization period where a gate-on voltage of the n-1st scan signal (Scan(n-1)) is input to an n-1st pixel line, a sampling period where the gate-on voltage of the nth scan signal (Scan (n)) is input to an nth pixel line, a holding period where a gate-off voltage of each of the n-1st scan signal (Scan(n-1)) and the nth scan signal (Scan (n)) is input to the nth pixel line, and an emission period

where the gate-on voltage of the nth emission signal (EM(n)) is input to the nth pixel line,
 in the initialization period, the eighth transistor (T8) is turned on,
 in the sampling period, the first transistor (T1), the second transistor (T2), the fifth transistor (T5), and the seventh
 transistor (T7) are turned on,
 in the holding period, the first to eighth transistors (T1, T2, T3, T4, T5, T6, T7, T8) are turned off, and
 in the emission period, the third transistor (T3), the fourth transistor (T4), and the sixth transistor (T6) are turned on.

3. The electroluminescent display device of claim 2, wherein in the initialization period, the sampling period, and the
 holding period, the nth emission signal (EM(n)) has the gate-off voltage.

4. The electroluminescent display device of claim 3, wherein the n-1st scan signal (Scan(n-1)) and the nth scan signal
 (Scan (n)) are activated to the gate-on voltage during one horizontal period, and the nth emission signal (EM(n)) is
 deactivated to the gate-off voltage during three horizontal periods.

5. The electroluminescent display device of one of the claims 1 to 4, wherein each of the first transistor and the eighth
 transistor is a double-gate type transistor.

6. The electroluminescent display device of claim 1, the display panel (150) further comprises
 a ninth transistor (T9) applying the high-level power voltage to a fifth node (N5) in response to an n-1st scan signal
 (Scan(n-1)).

7. The electroluminescent display device of claim 6, wherein
 one frame for driving each of the plurality of pixel circuits comprises an initialization period where a gate-on voltage
 of the n-1st scan signal (Scan(n-1)) is input to an n-1st pixel line, a sampling period where the gate-on voltage of
 the nth scan signal (Scan (n)) is input to an nth pixel line, a holding period where a gate-off voltage of each of the
 n-1st scan signal (Scan(n-1)) and the nth scan signal (Scan (n)) is input to the nth pixel line, and an emission period
 where the gate-on voltage of the nth emission signal (EM(n)) is input to the nth pixel line,
 in the initialization period, the ninth transistor (T9) and the eighth transistor (T8) are turned on,
 in the sampling period, the first transistor (T1), the second transistor (T2), the fifth transistor (T5), and the seventh
 transistor (T7) are turned on,
 in the holding period, the first to ninth transistors (T1, T2, T3, T4, T5, T6, T7, T8, T9) are turned off, and
 in the emission period, the third transistor (T3), the sixth transistor (T6), and the fourth transistor (T4) are turned on.

8. The electroluminescent display device of claim 7, wherein in the initialization period, the sampling period, and the
 holding period, the nth emission signal (EM(n)) has the gate-off voltage.

9. The electroluminescent display device of claim 8, wherein the n-1st scan signal (Scan(n-1)) and the nth scan signal
 (Scan (n)) are activated to the gate-on voltage during one horizontal period, and the nth emission signal (EM(n)) is
 deactivated to the gate-off voltage during three horizontal periods.

10. The electroluminescent display device of one of the preceding claims, wherein the second transistor (T2) and/or
 the third transistor (T3) is disposed in the non-display area.

11. The electroluminescent display device of claim 10, wherein the second transistor (T2) and the third transistor (T3)
 are used in common by each the plurality of pixel lines.

12. The electroluminescent display device of one of the preceding claims, wherein the initialization voltage (Vini) is
 equal to or lower than the low-level power voltage (VSS).

13. The electroluminescent display device of one of the preceding claims, wherein the reference voltage (Vref) is higher
 than the low-level power voltage (VSS) and lower than the high-level power voltage (VDD).

14. The electroluminescent display device of one of the preceding claims, wherein the driving transistor (DT), the first
 transistor (T1), the fourth transistor (T4), the fifth transistor (T5), the sixth transistor (T6), the seventh transistor (T7),
 the eighth transistor (T8), the light emitting device (EL) and the capacitor (Cst) are disposed in the display area.

15. The electroluminescent display device of claims 6 to 14, wherein the ninth transistor (T9) are disposed in the display
 area.

FIG. 1

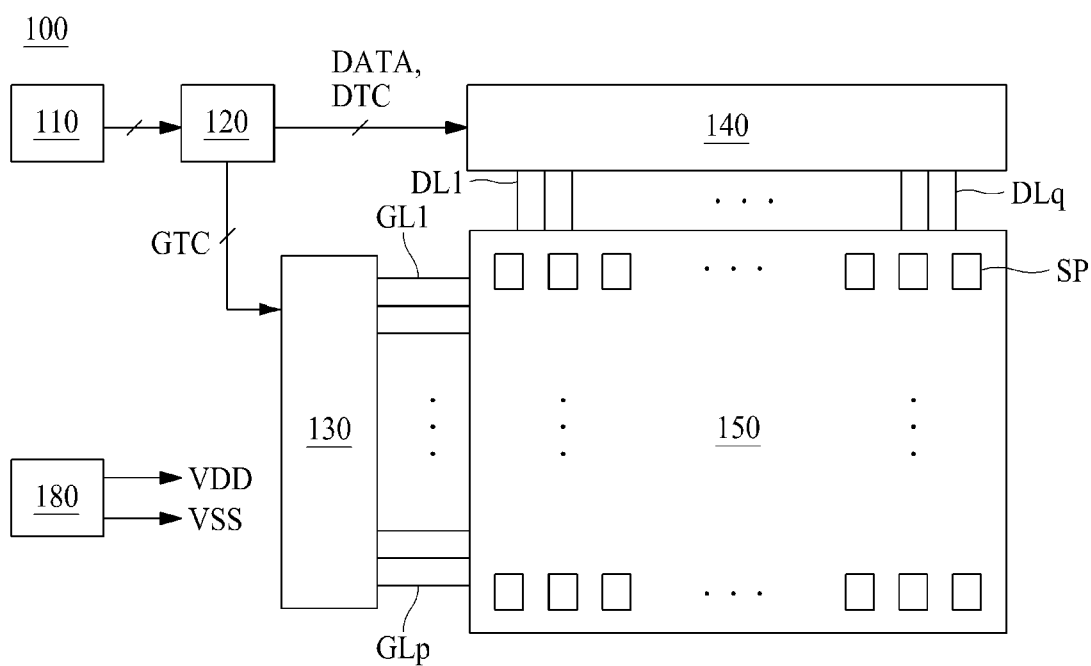


FIG. 2

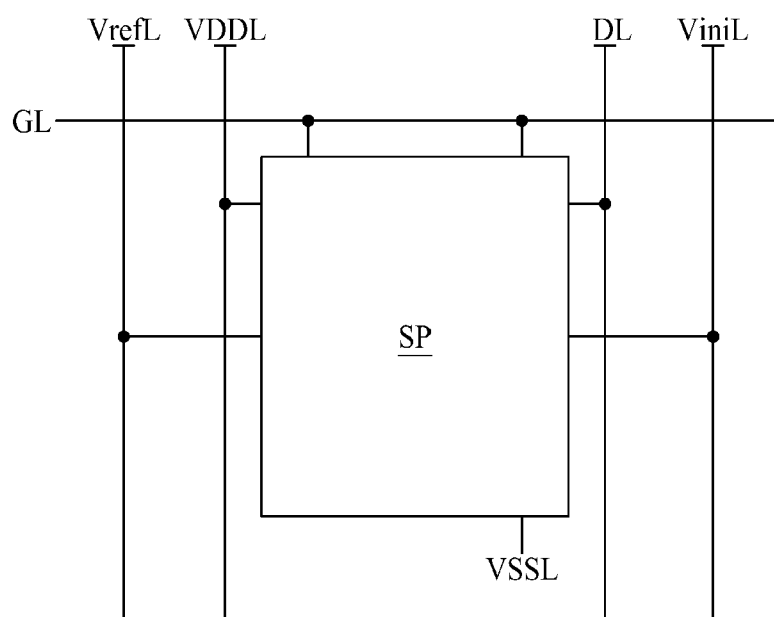


FIG. 3

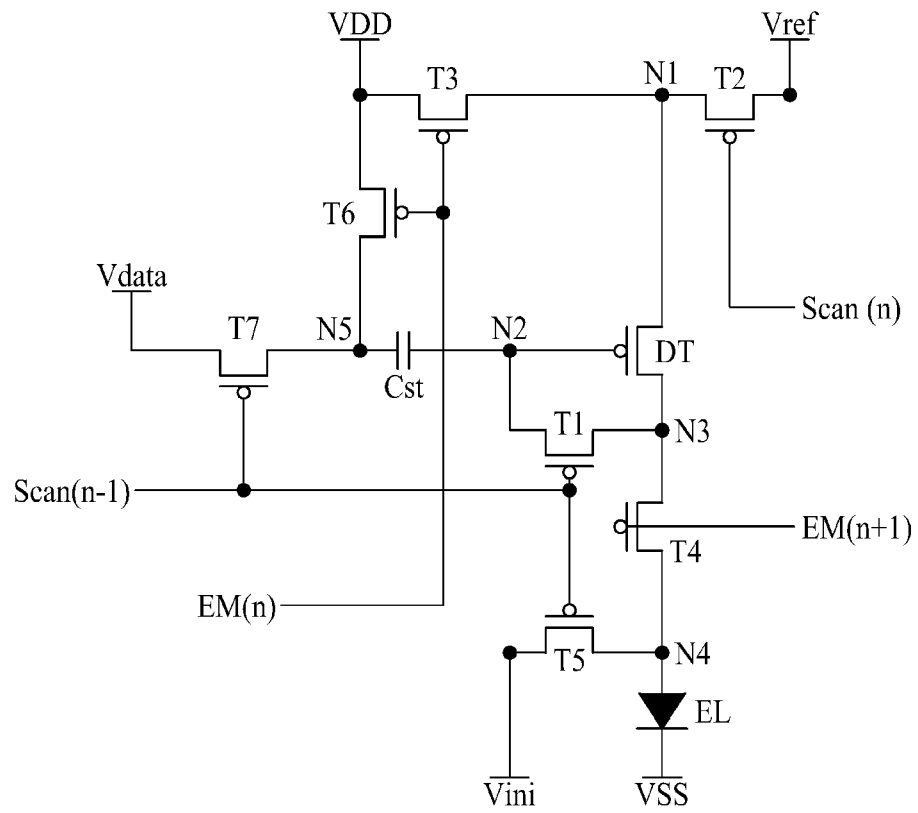


FIG. 4A

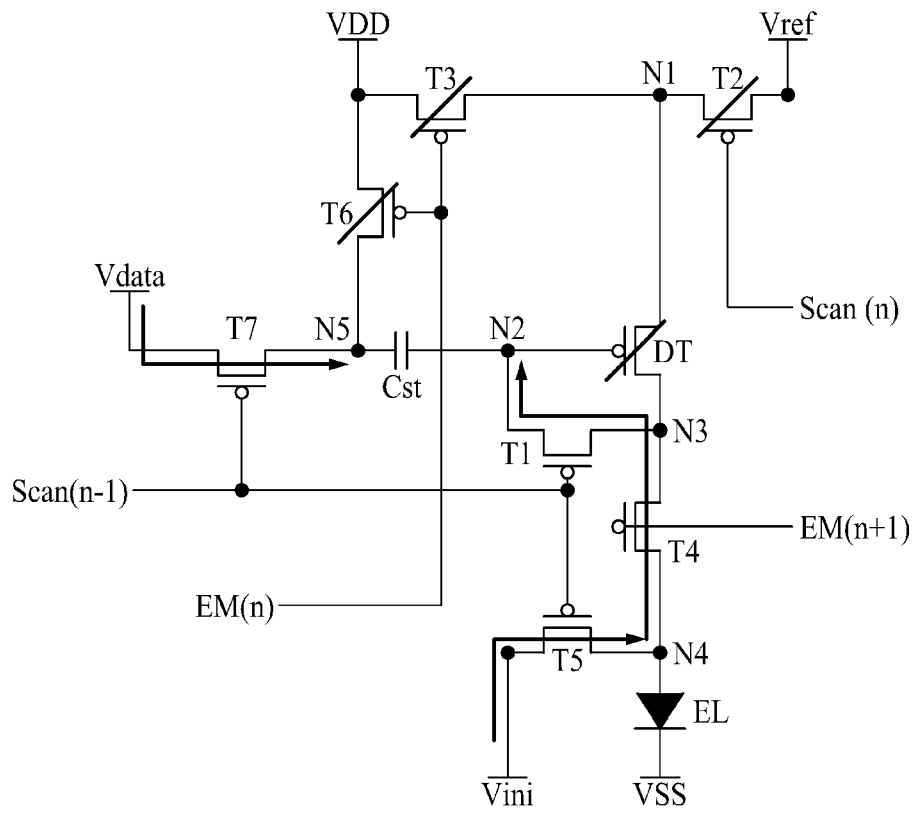


FIG. 4B

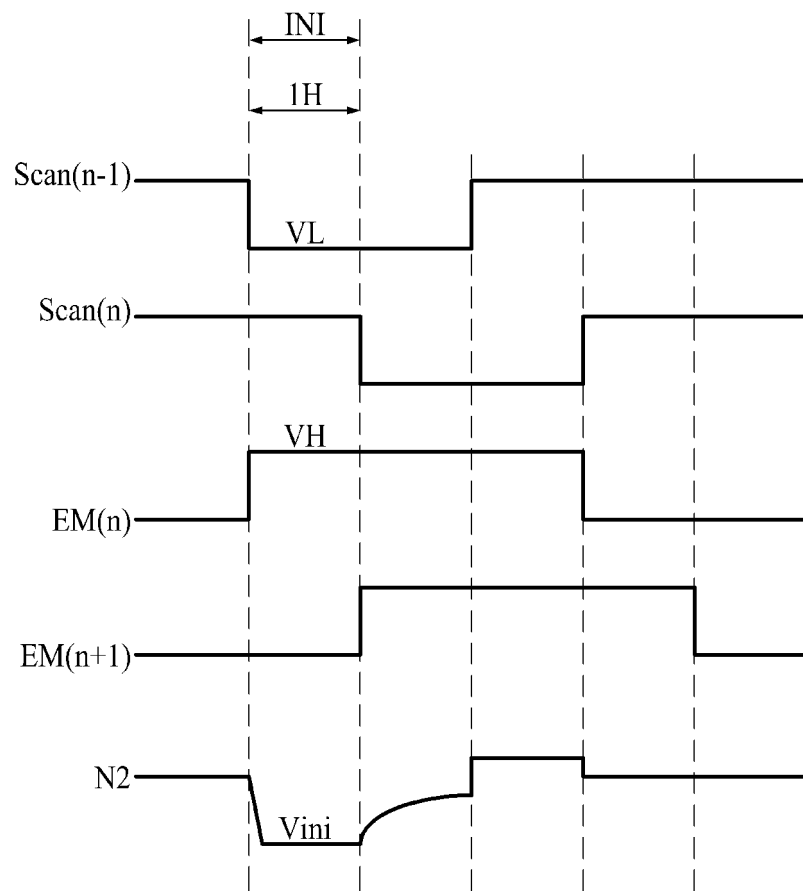


FIG. 5A

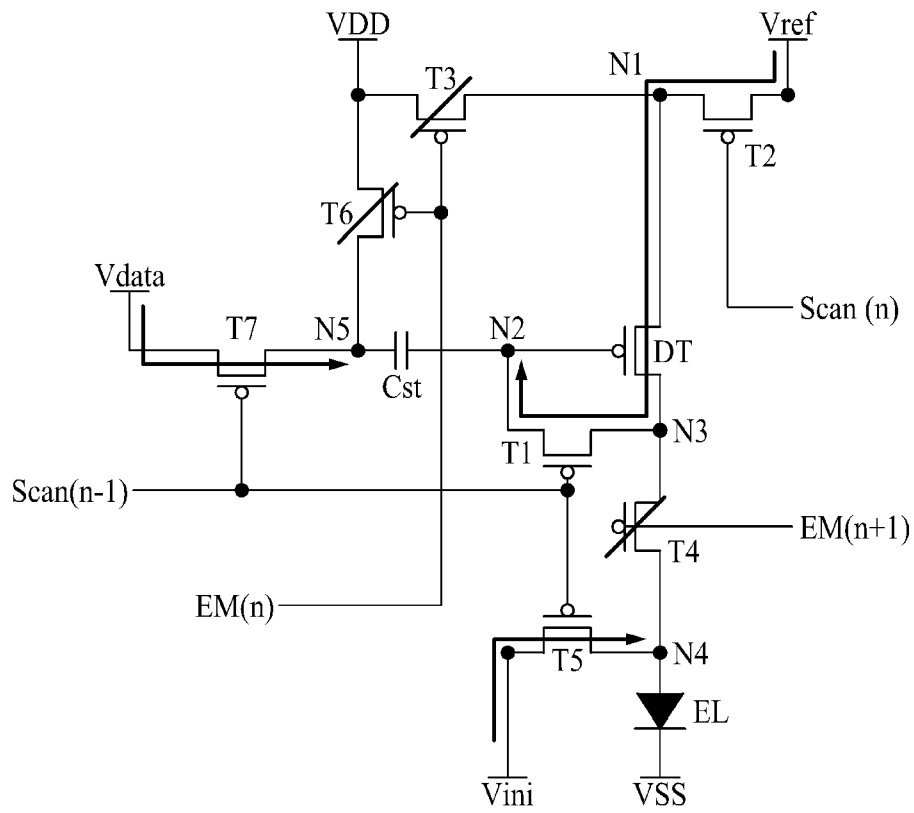


FIG. 5B

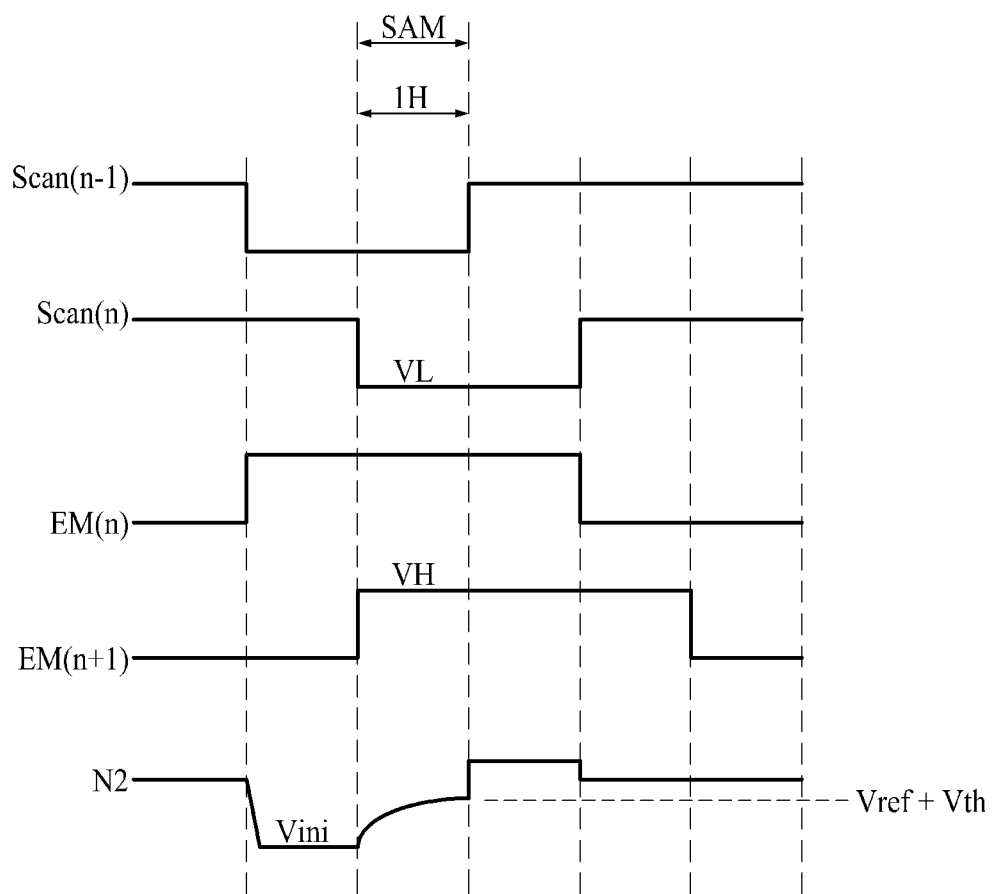


FIG. 6A

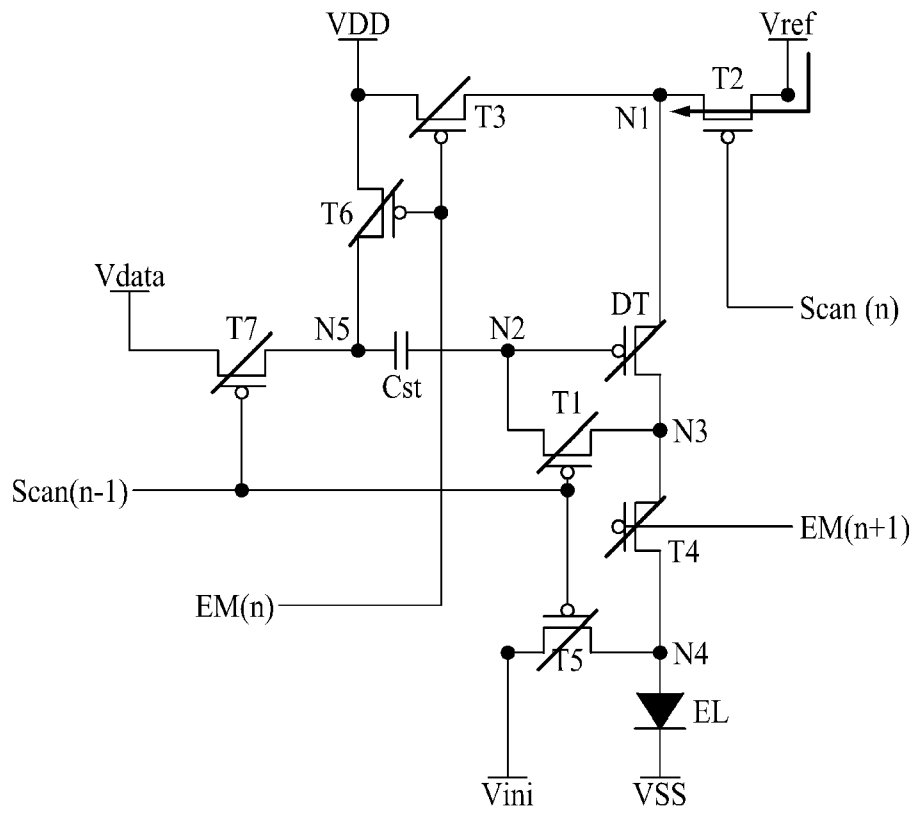


FIG. 6B

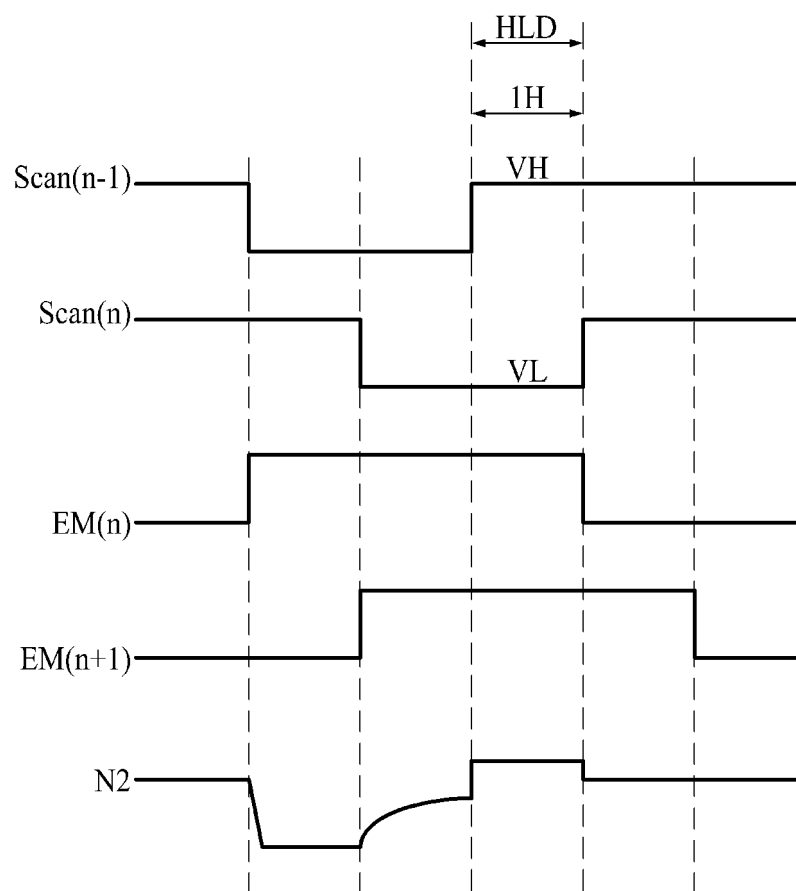


FIG. 7A

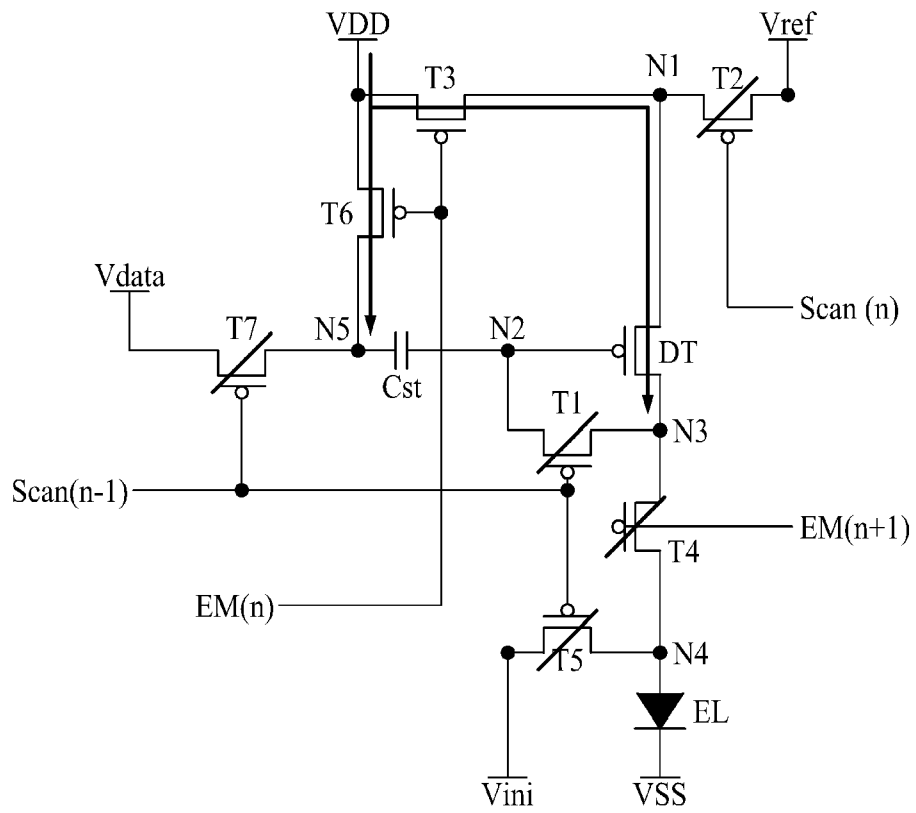


FIG. 7B

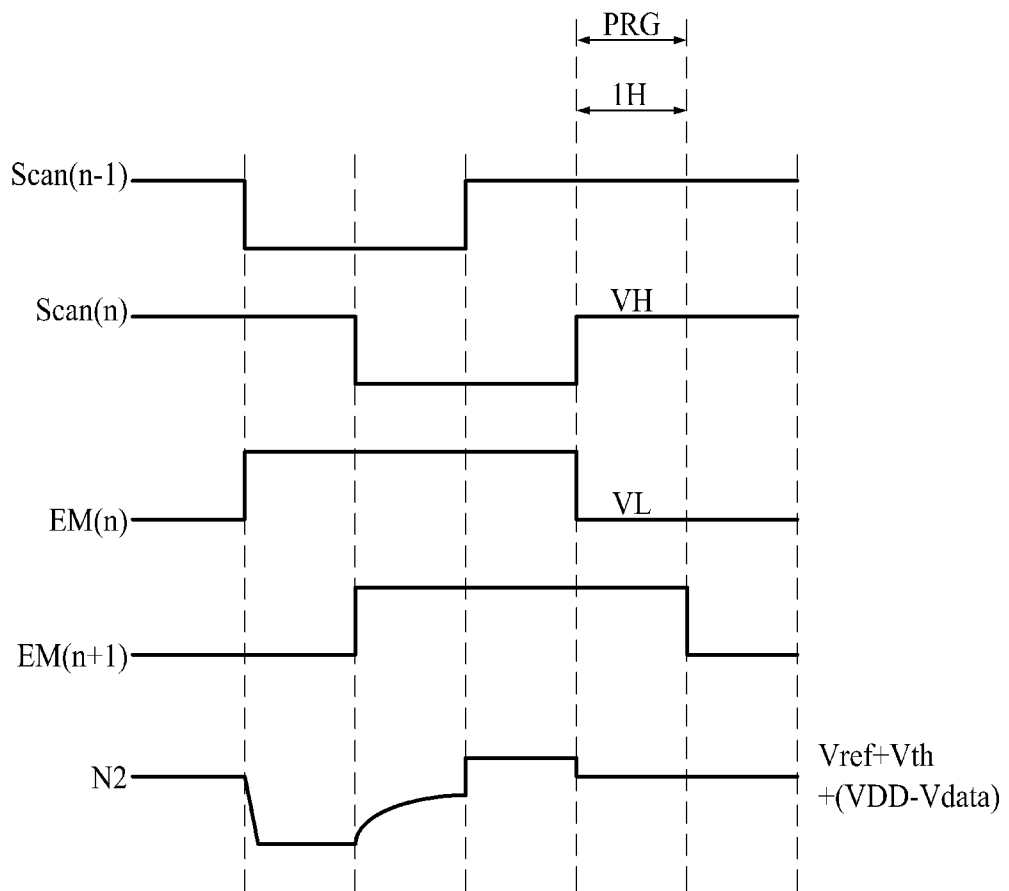


FIG. 8A

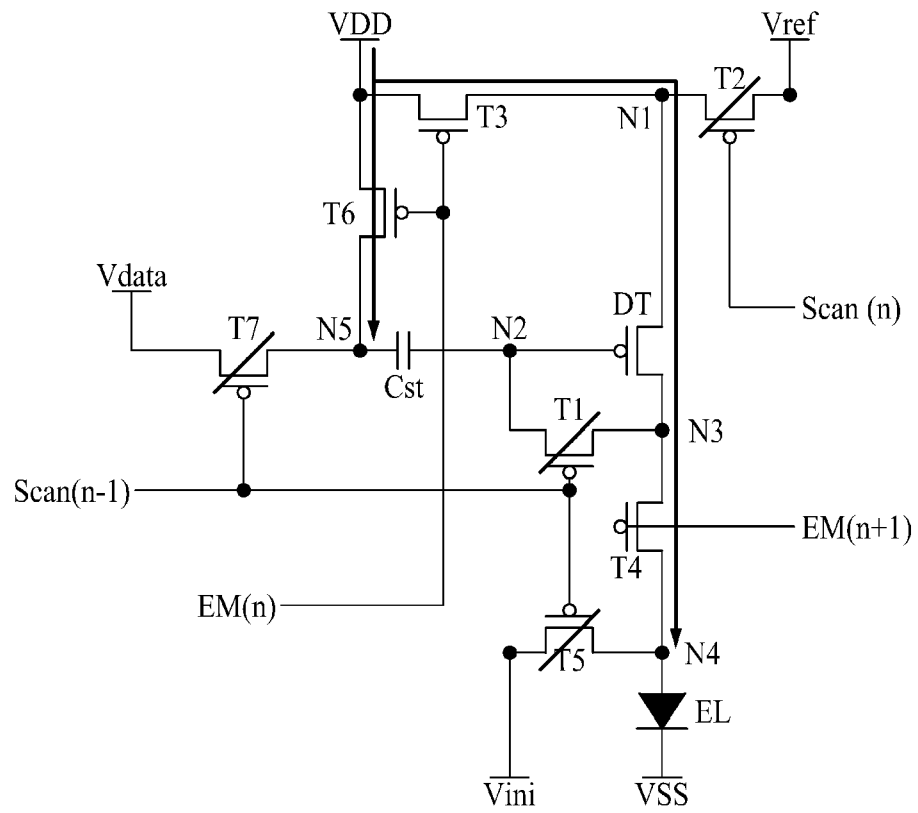


FIG. 8B

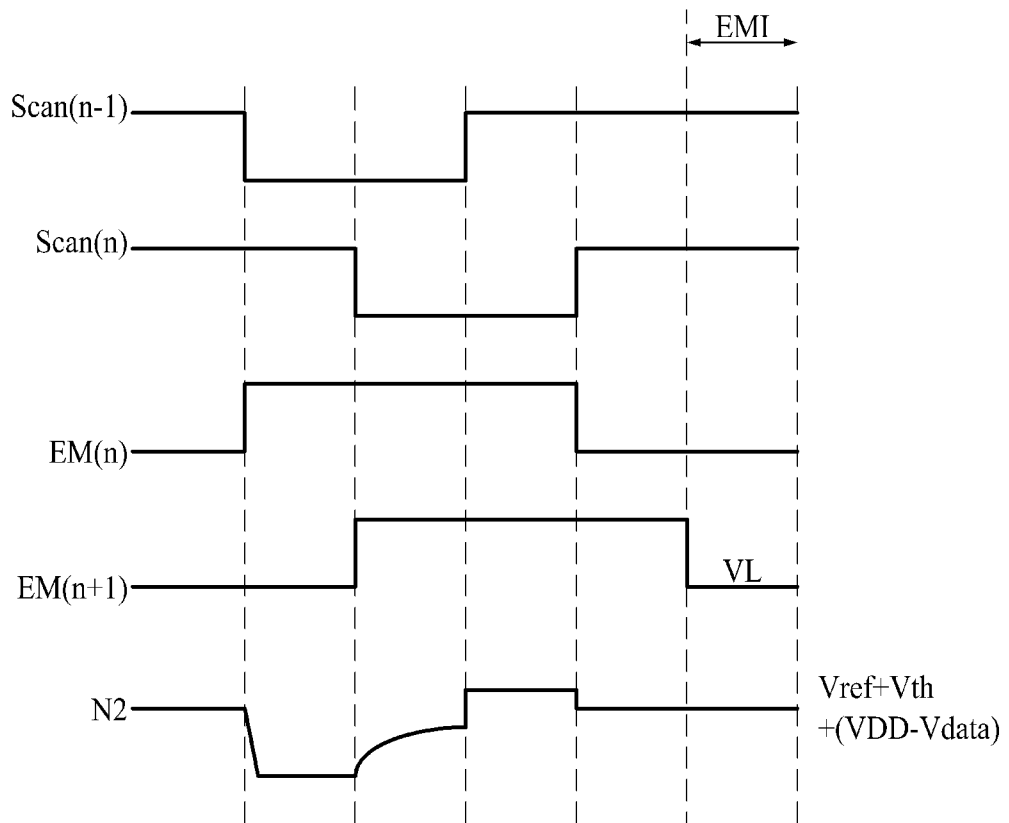


FIG. 9

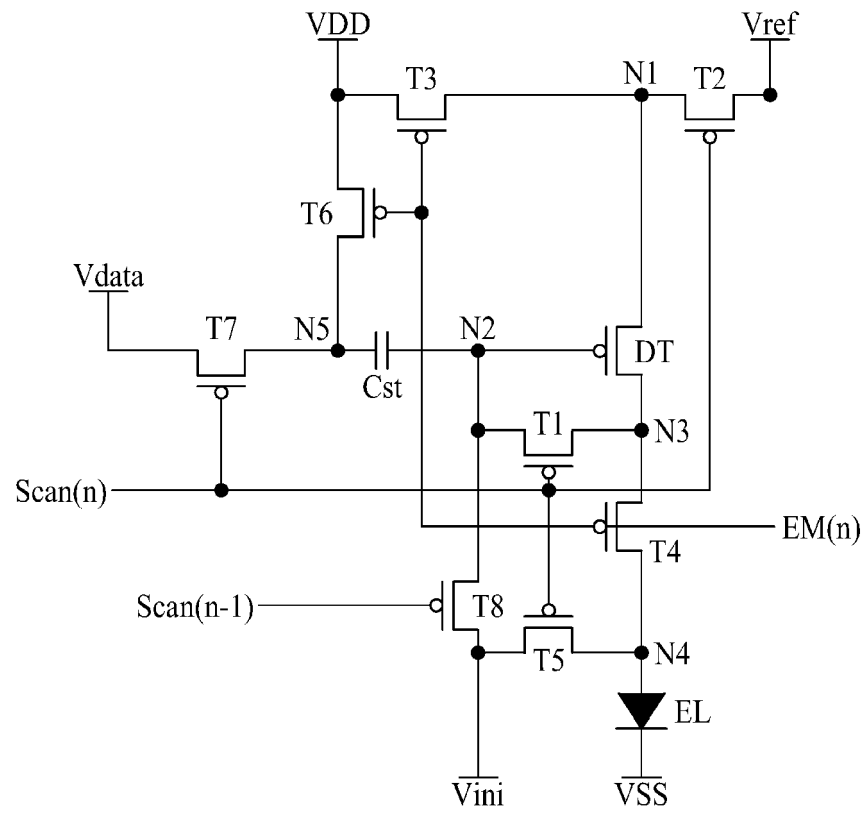


FIG. 10A

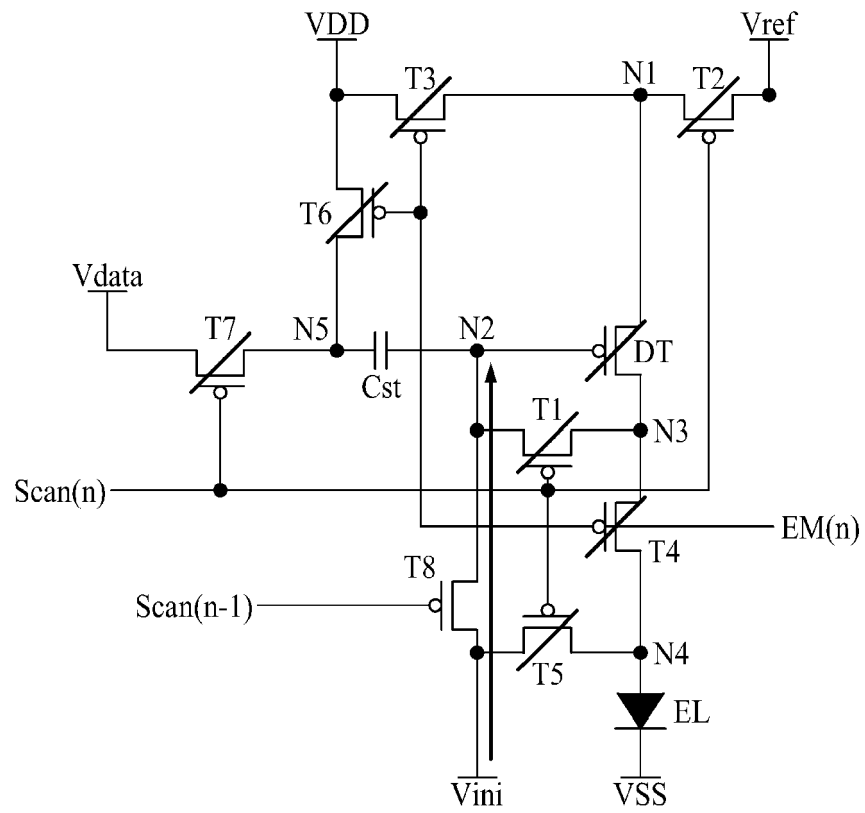


FIG. 10B

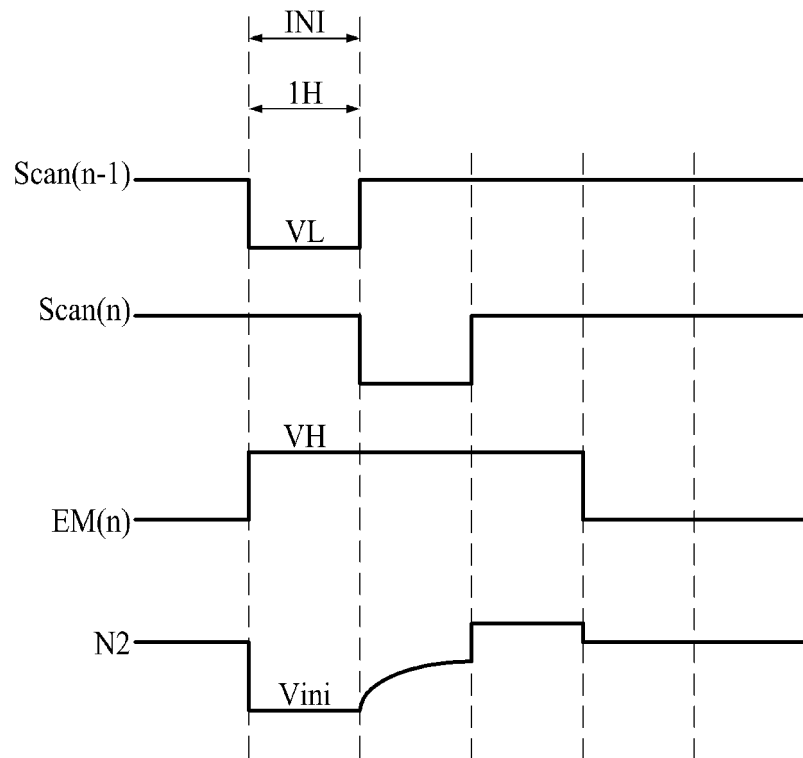


FIG. 11A

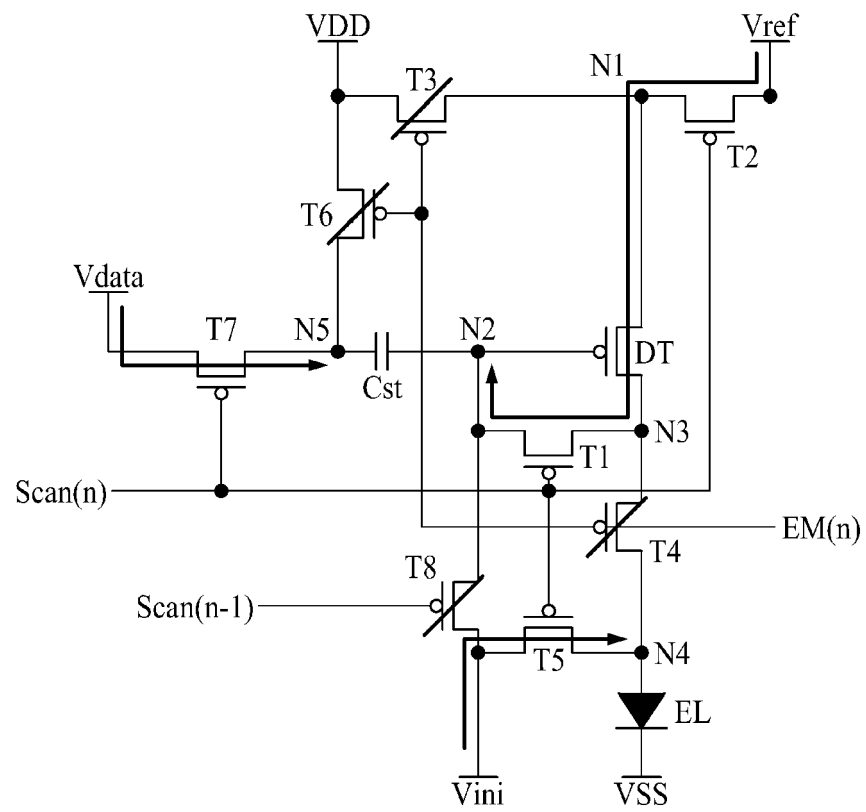


FIG. 11B

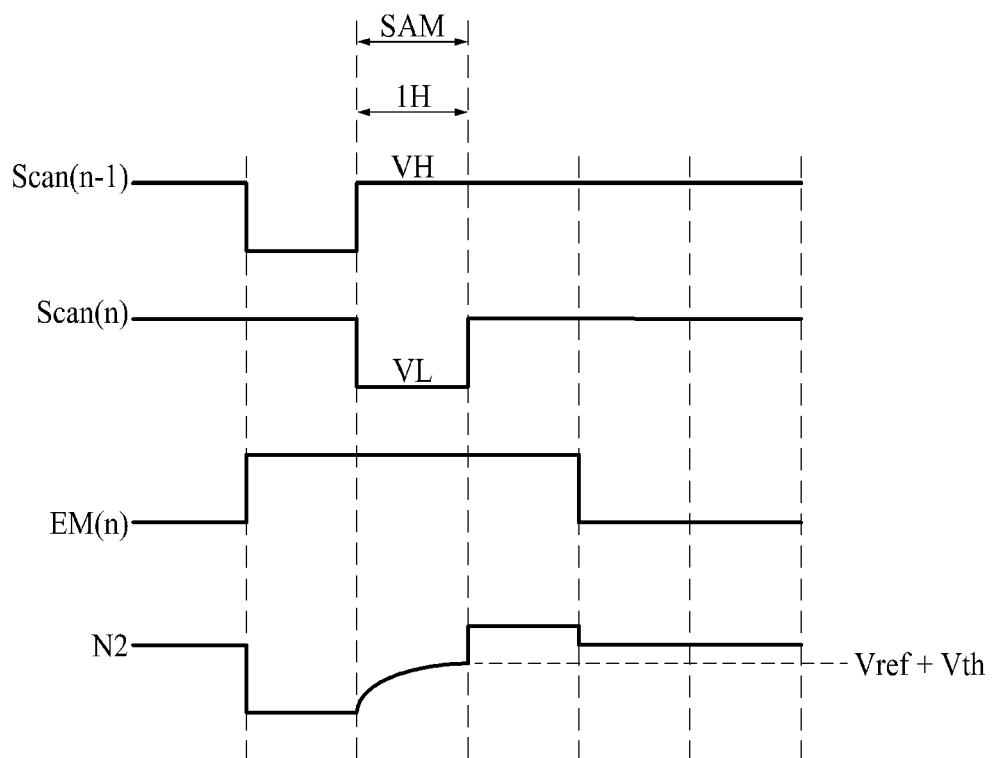


FIG. 12A

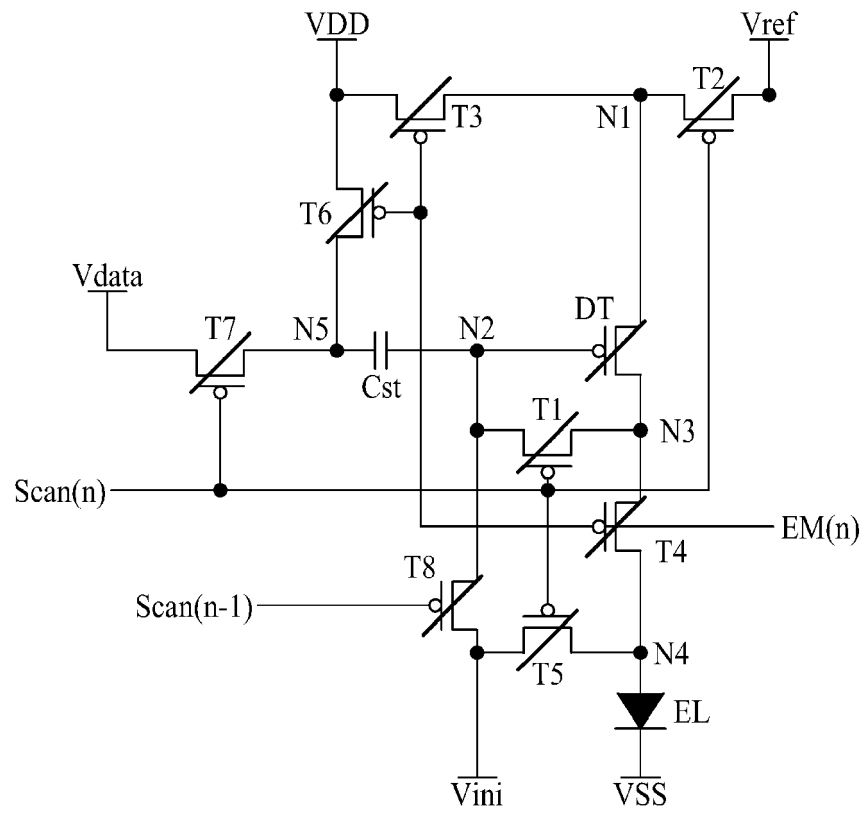


FIG. 12B

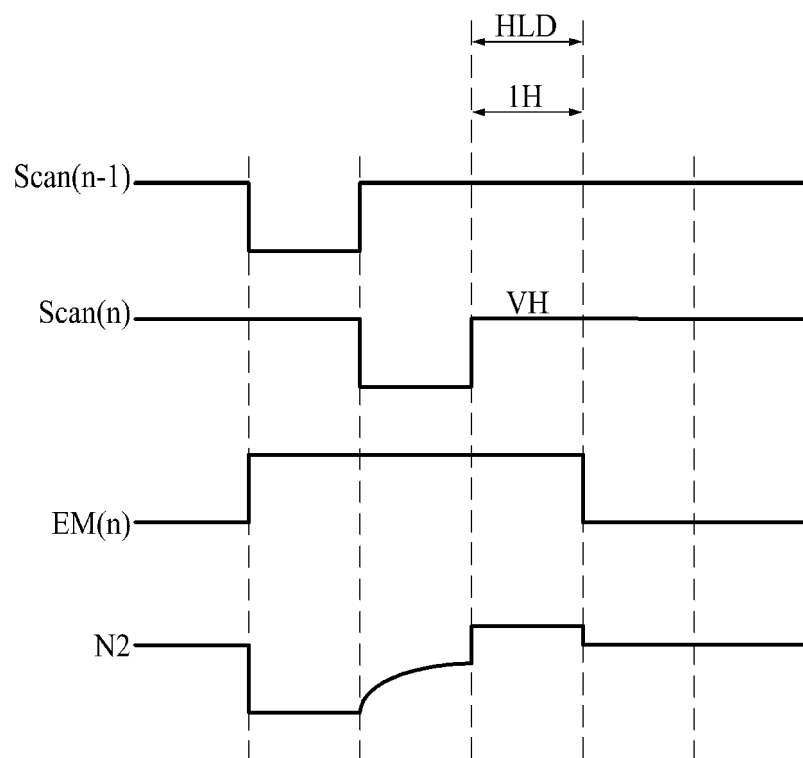


FIG. 13A

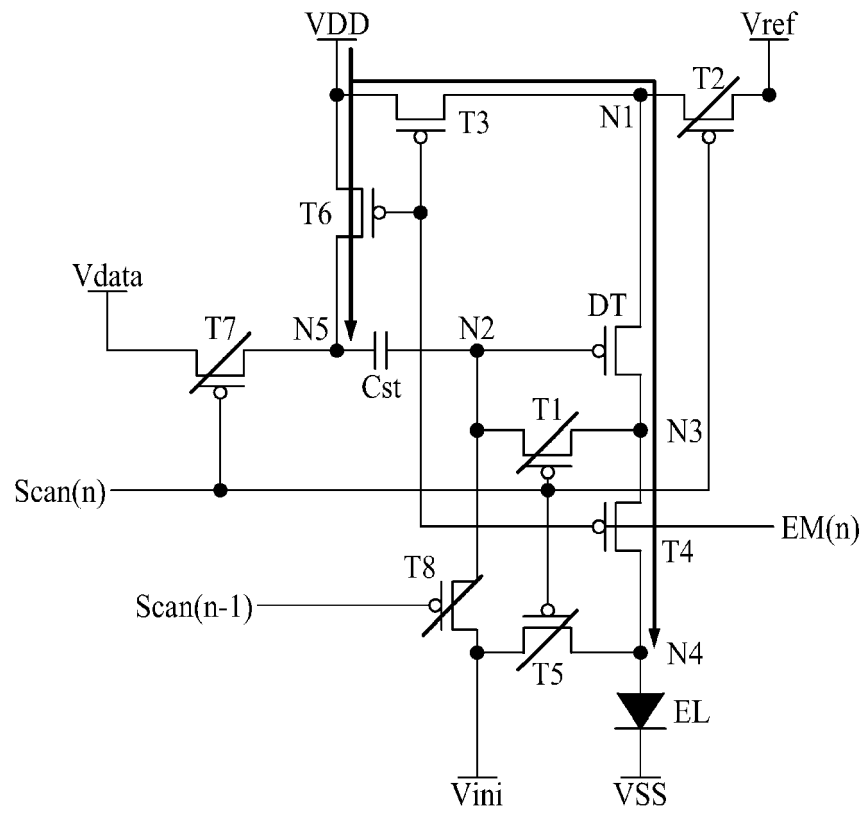


FIG. 13B

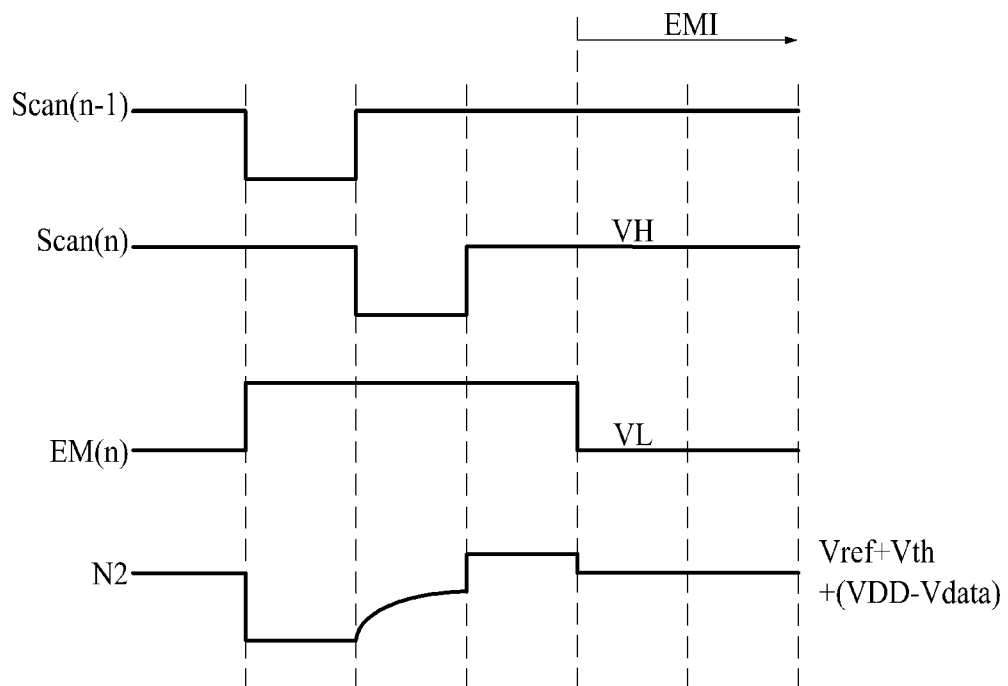


FIG. 14

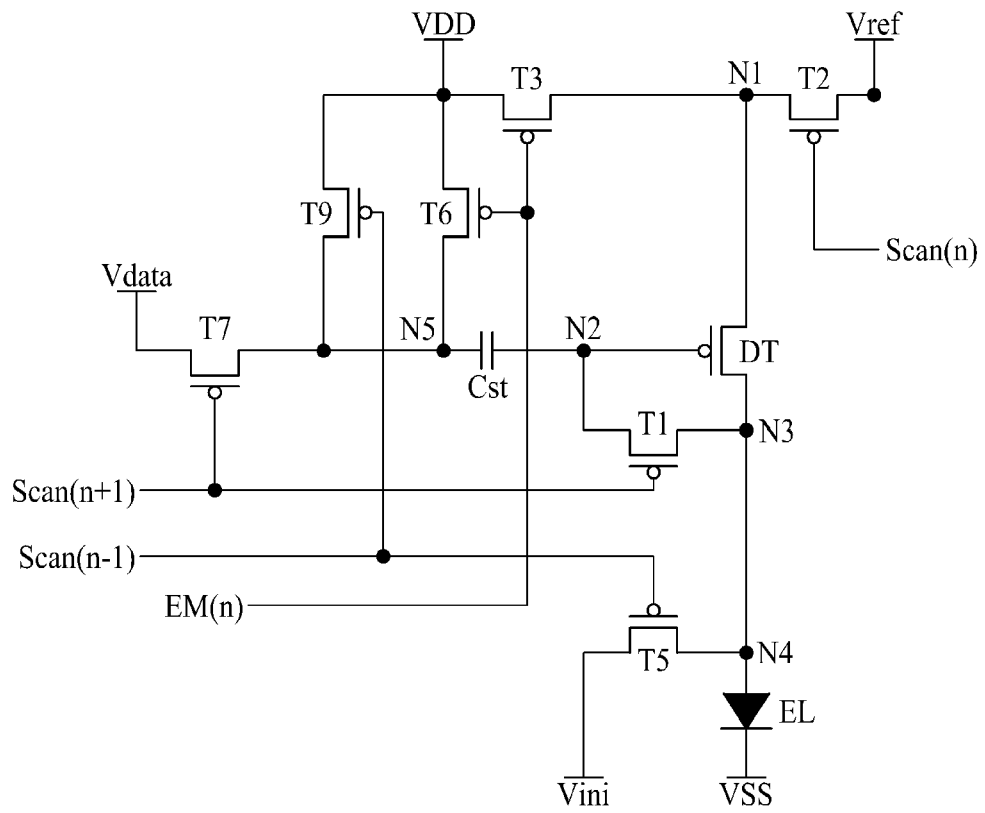


FIG. 15A

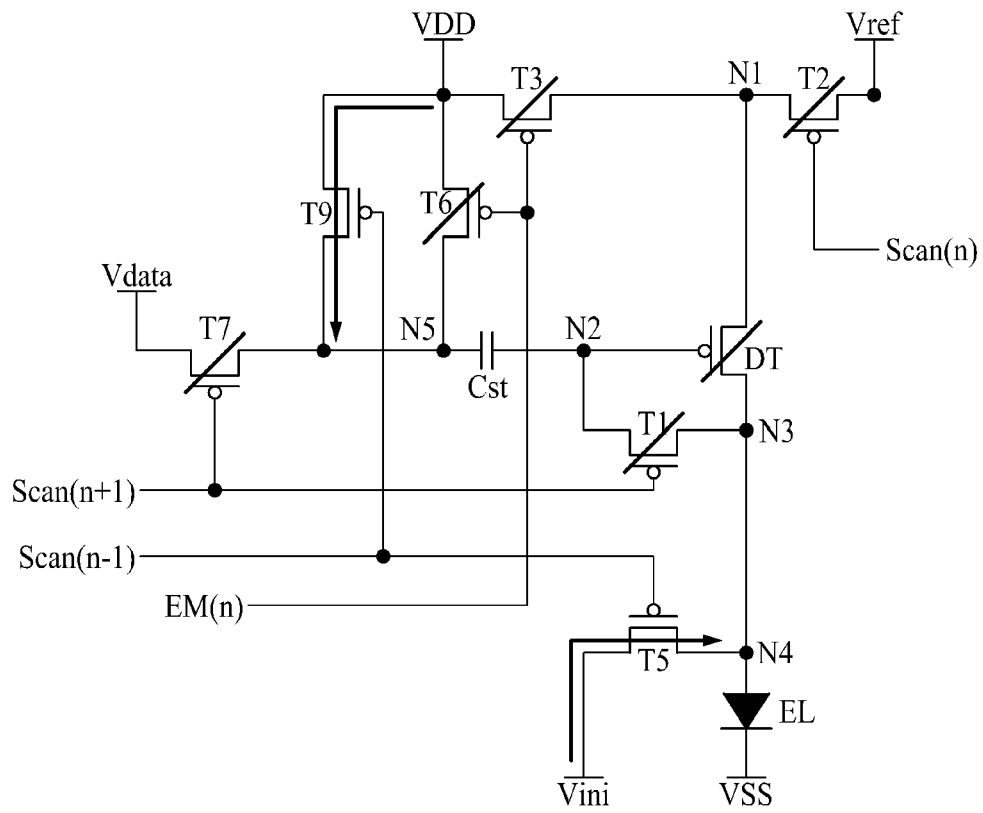


FIG. 15B

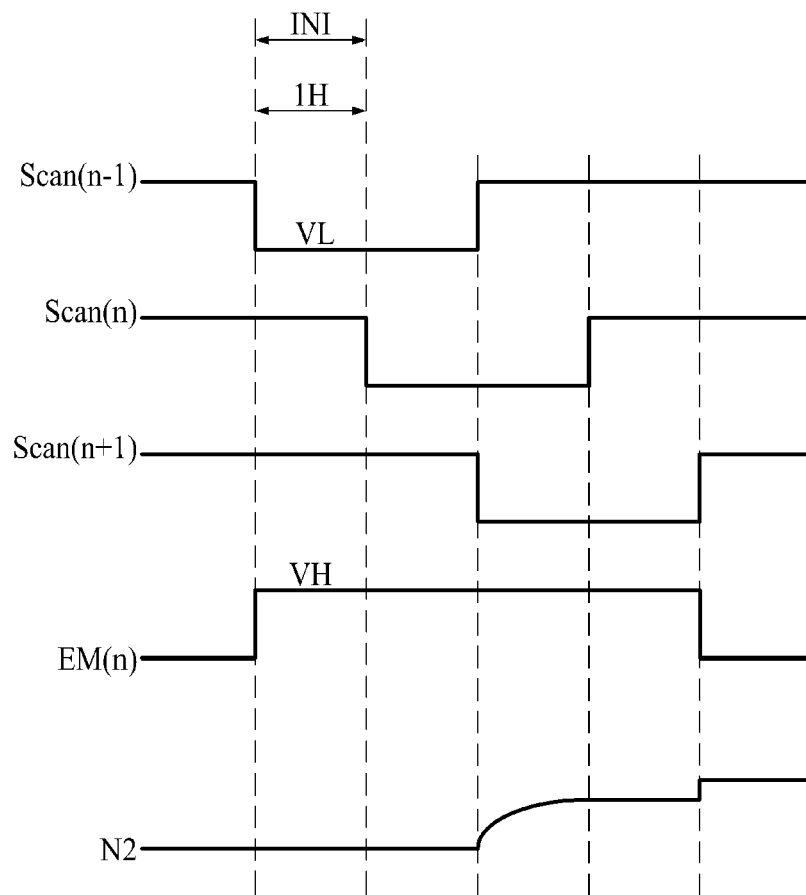


FIG. 16A

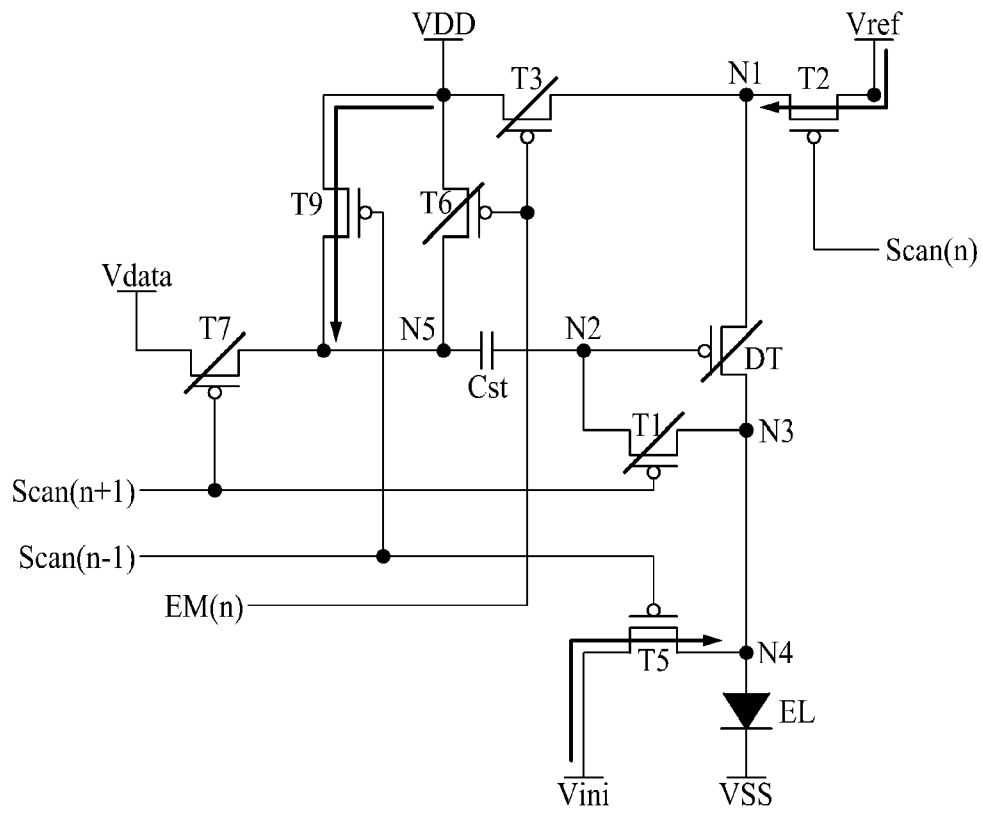


FIG. 16B

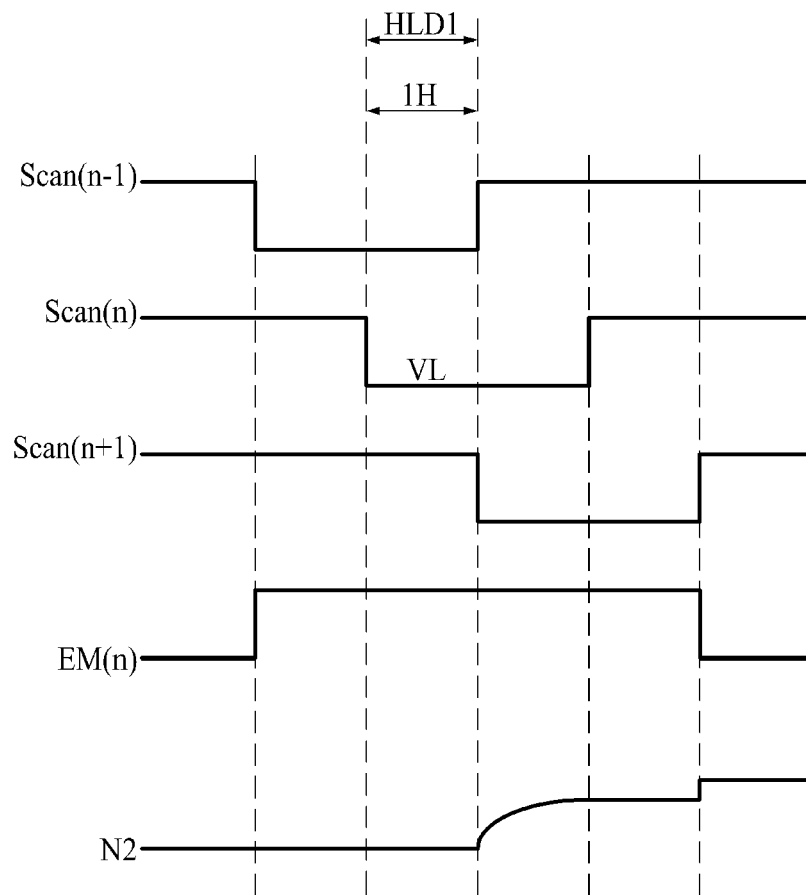


FIG. 17A

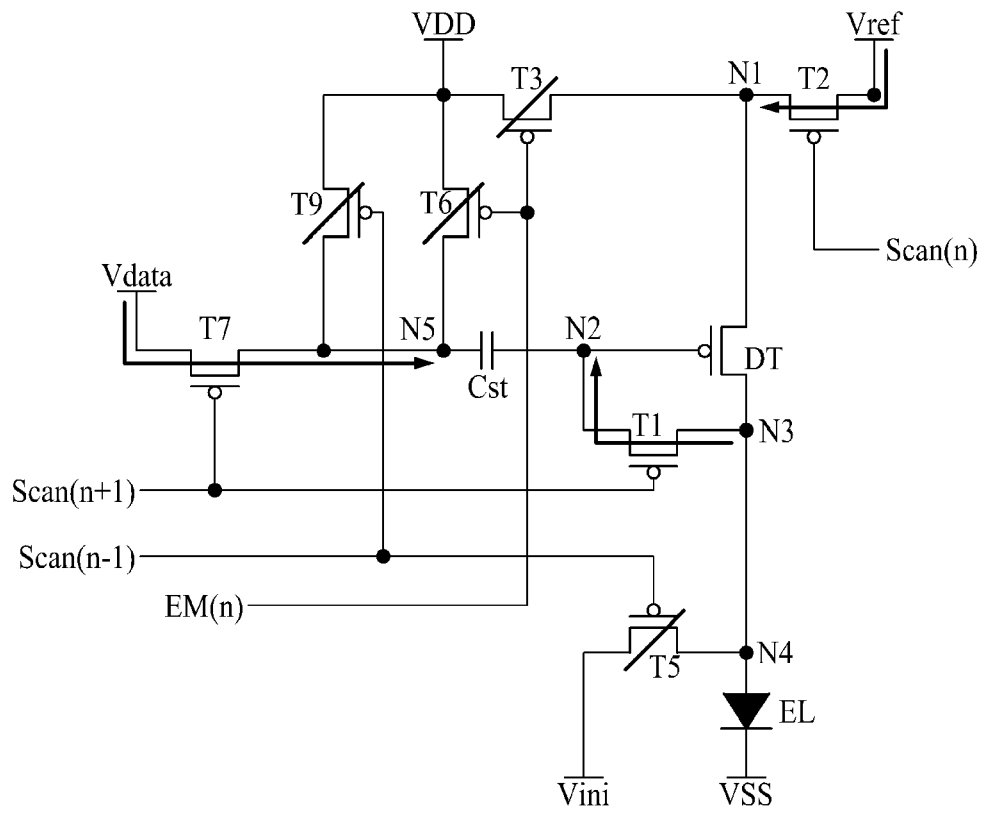


FIG. 17B

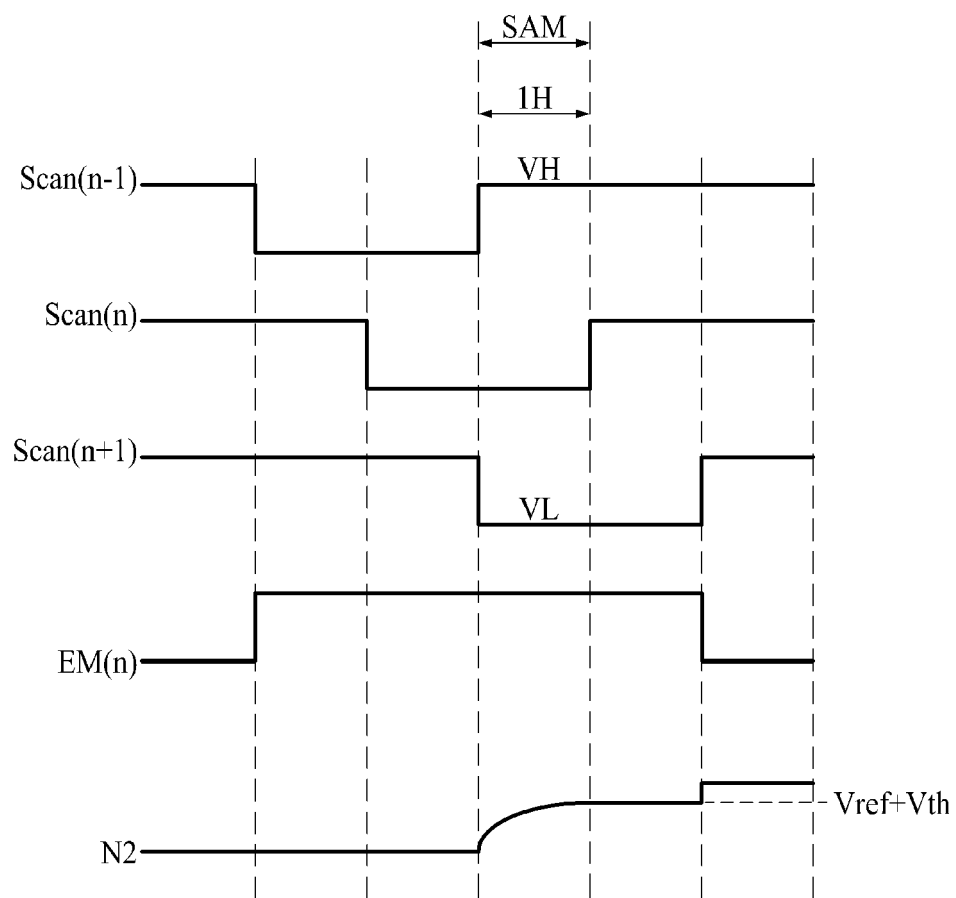


FIG. 18A

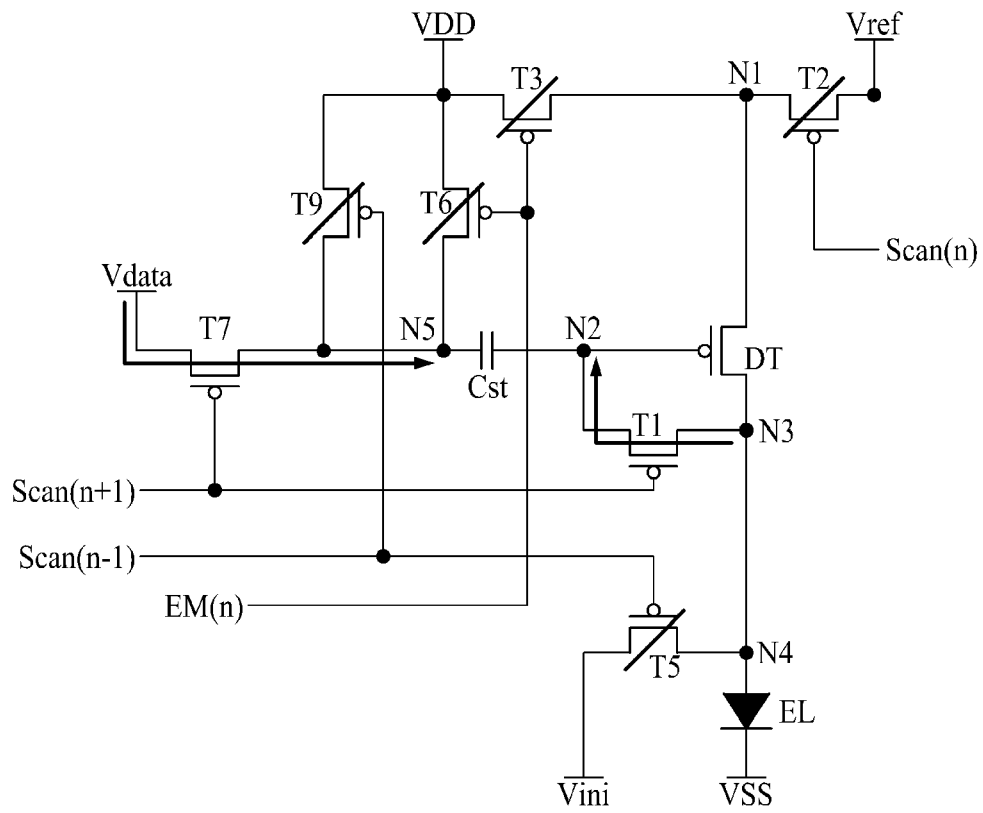


FIG. 18B

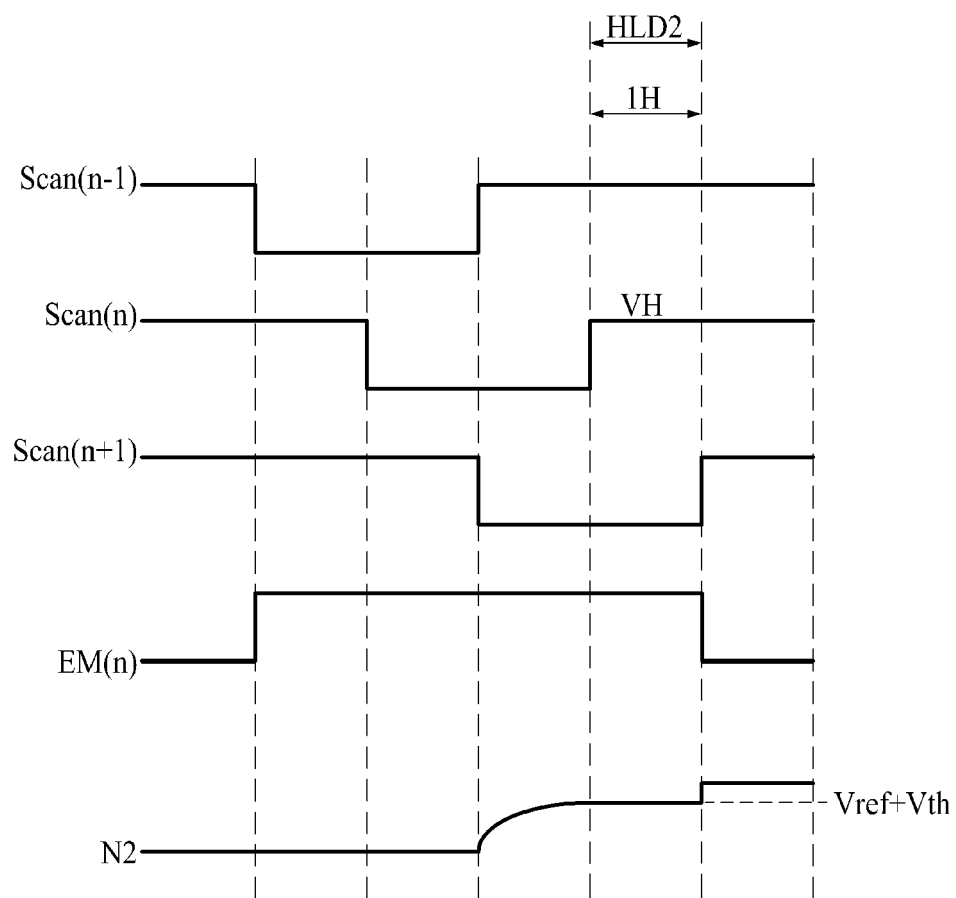


FIG. 19A

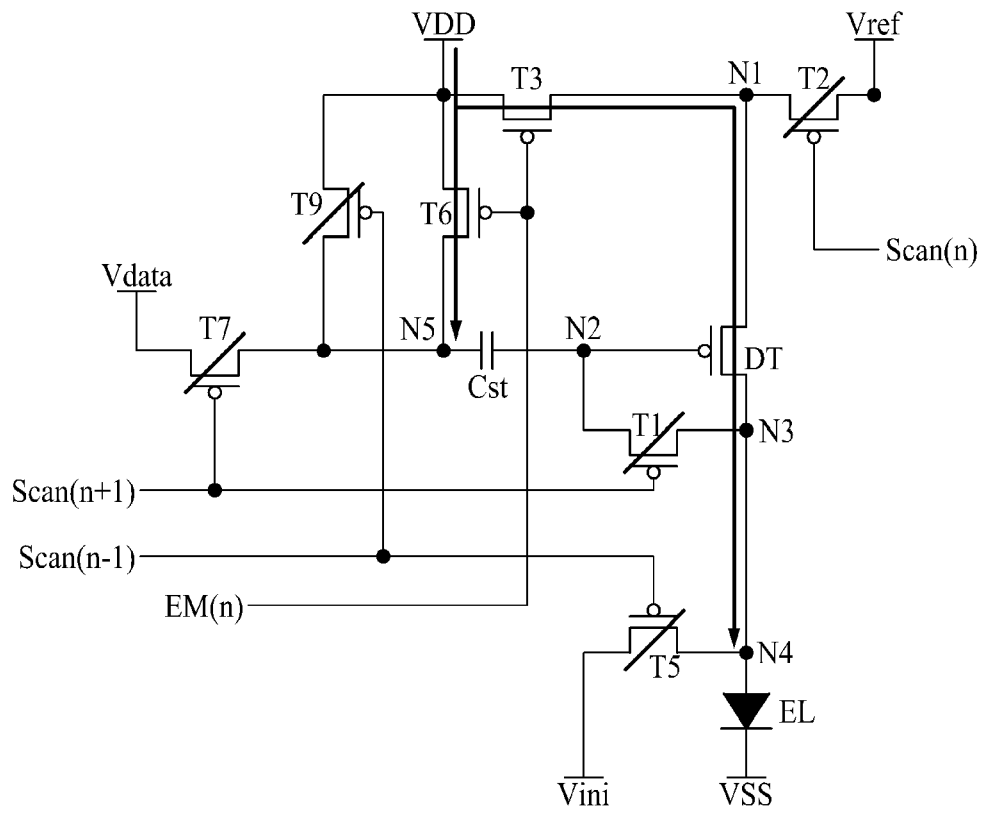


FIG. 19B

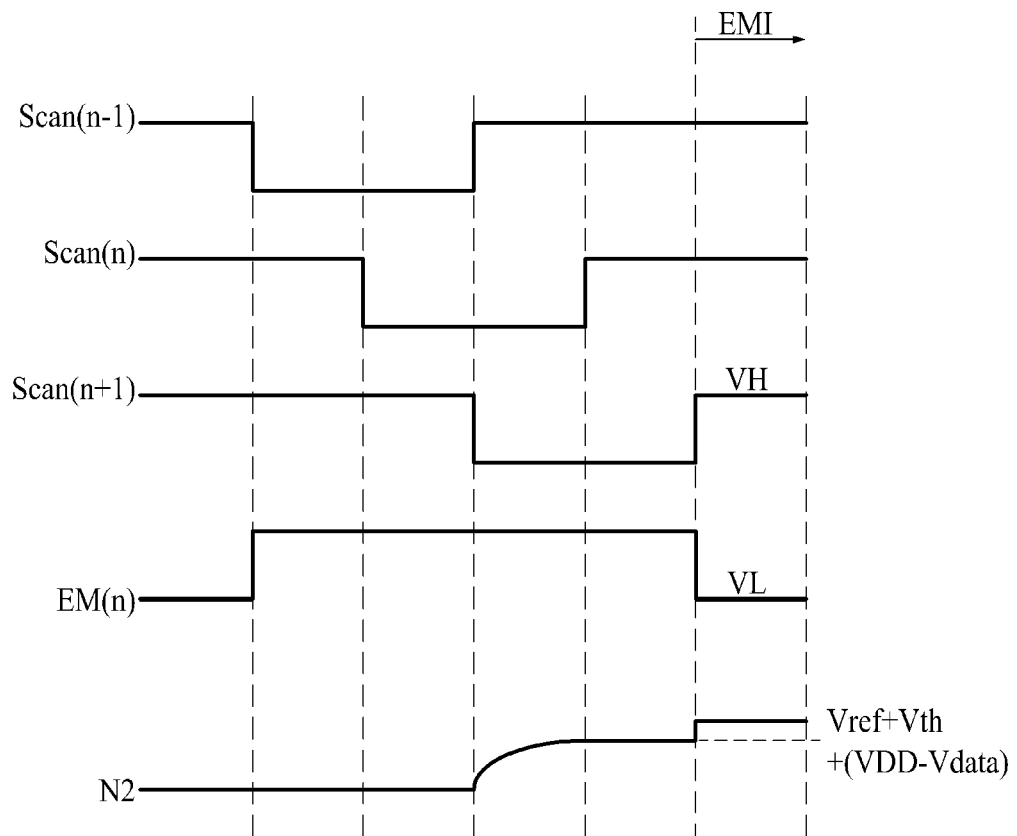


FIG. 20

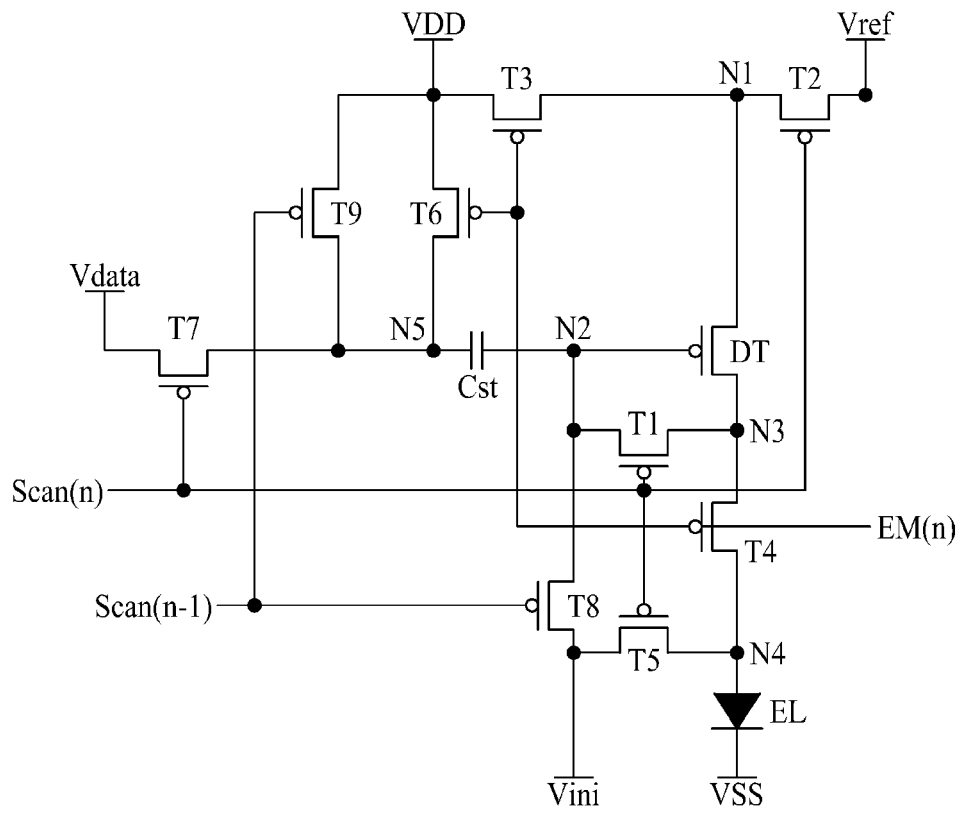


FIG. 21A

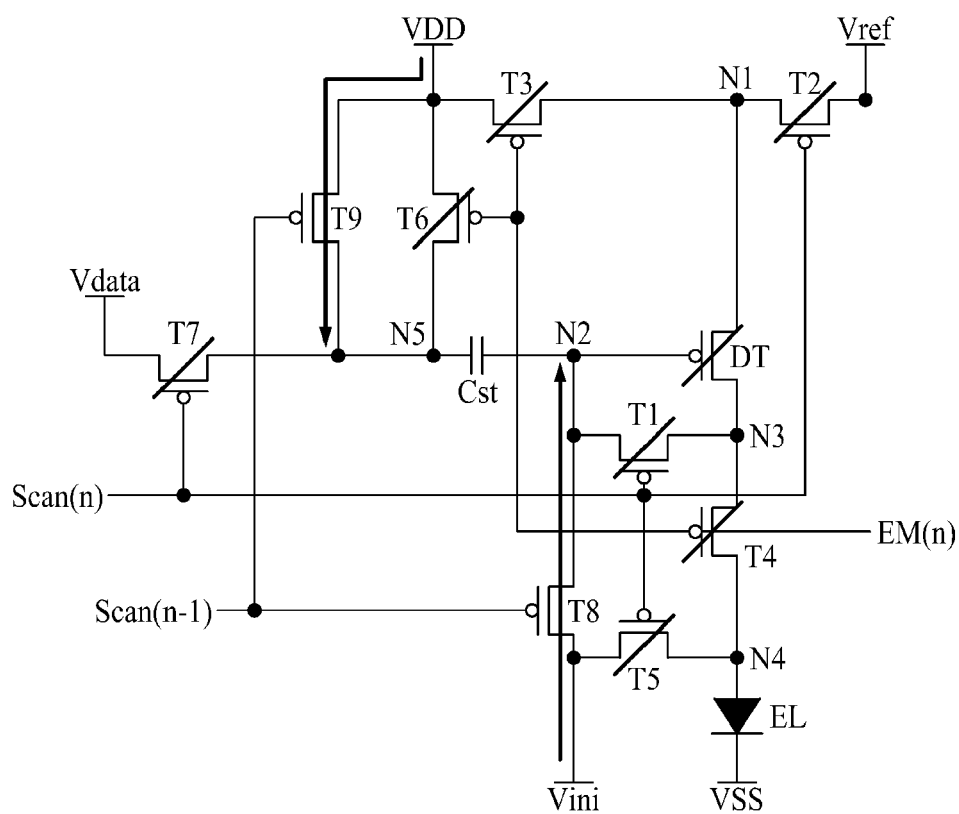


FIG. 21B

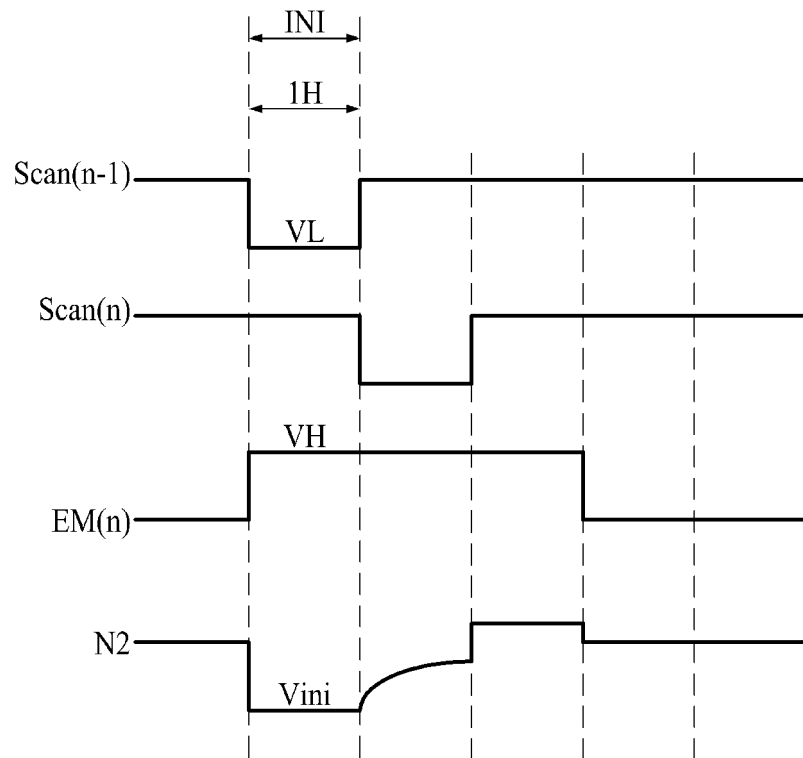


FIG. 22A

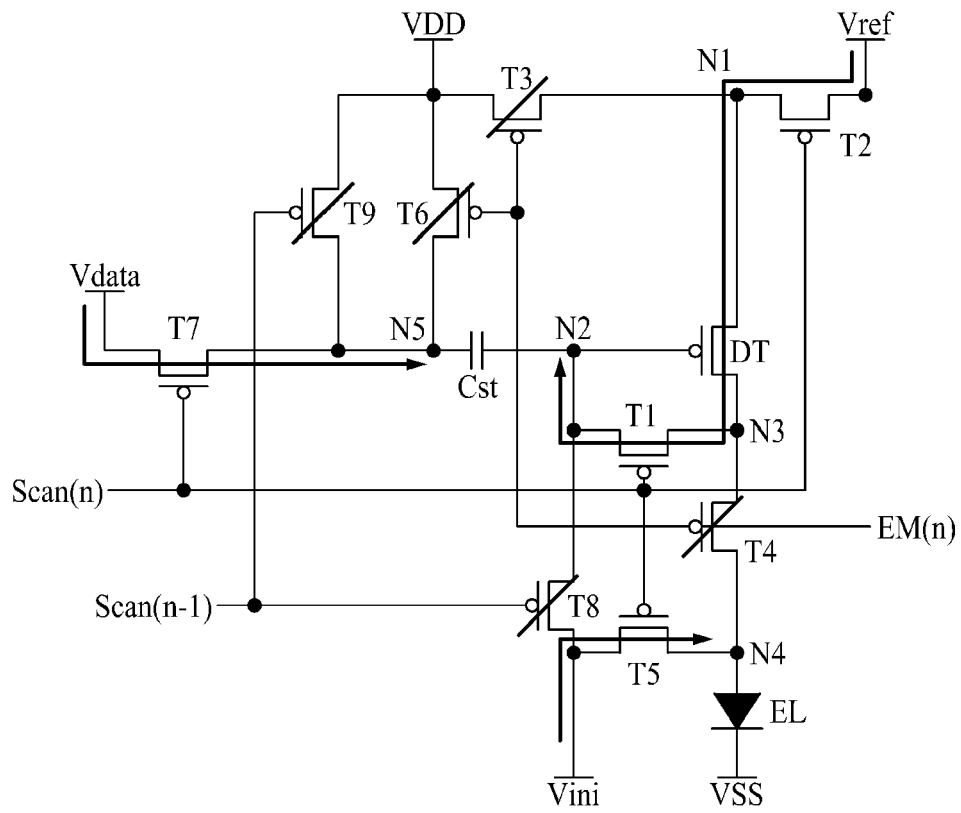


FIG. 22B

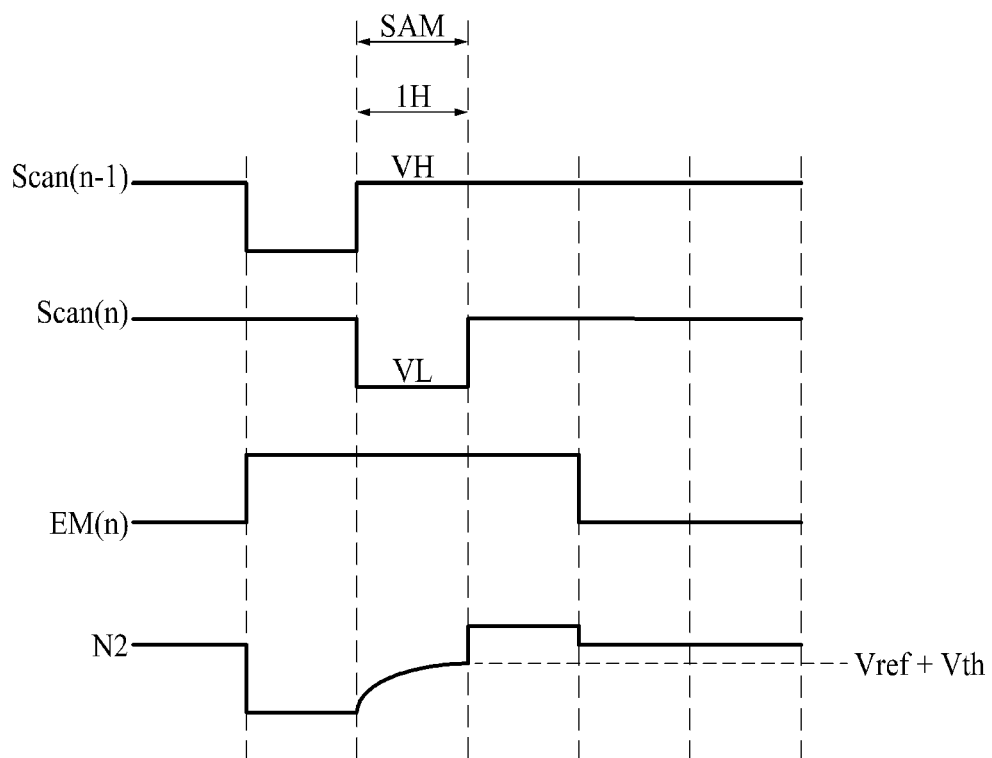


FIG. 23A

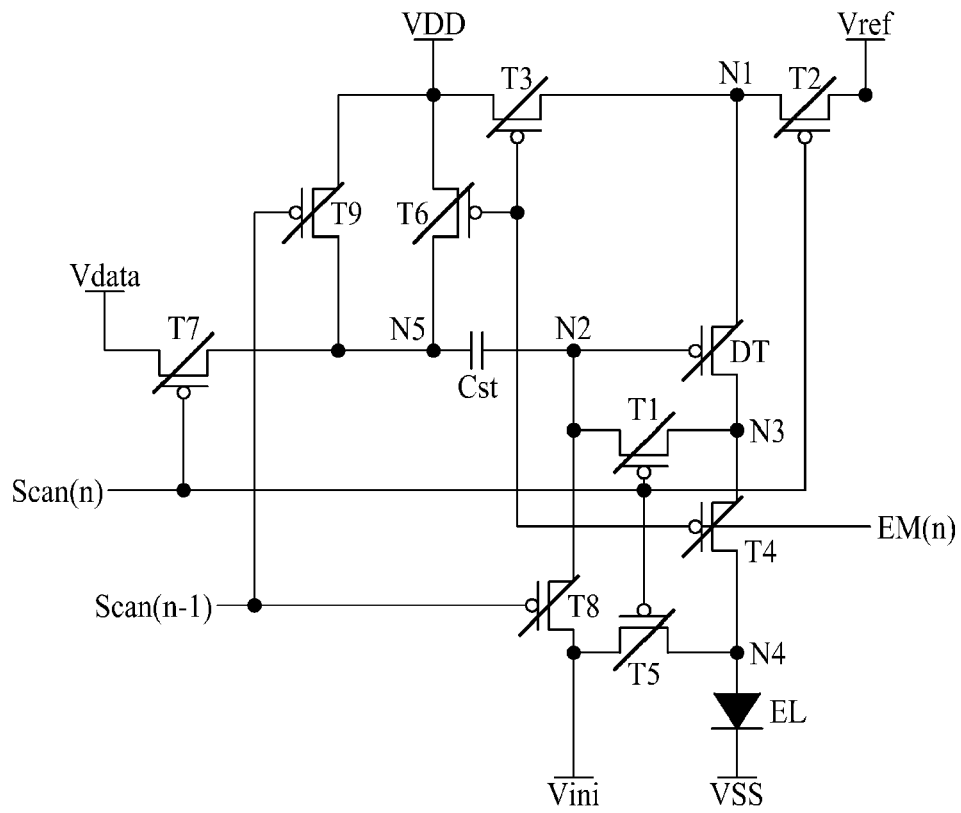


FIG. 23B

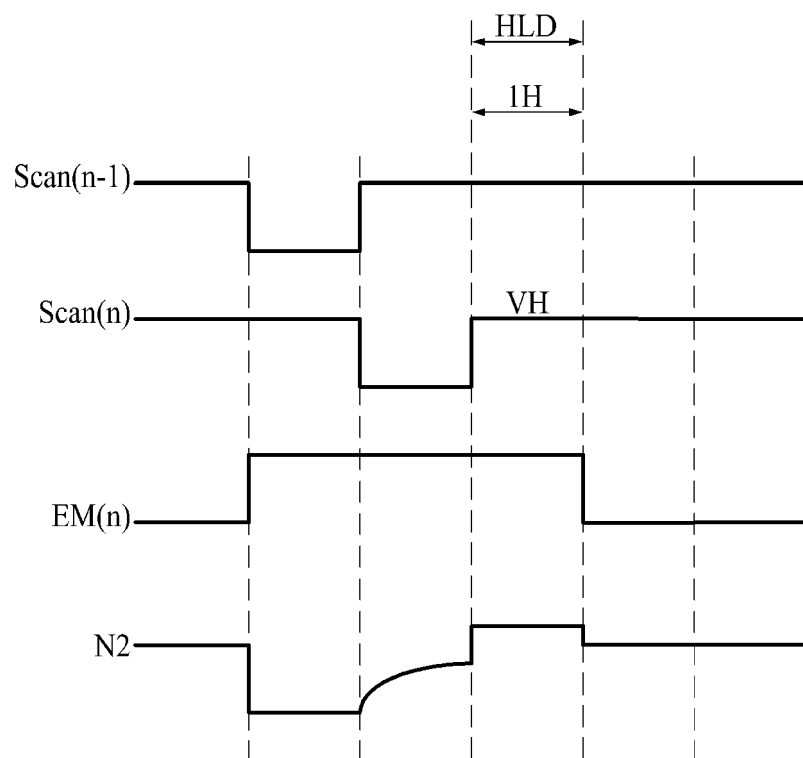


FIG. 24A

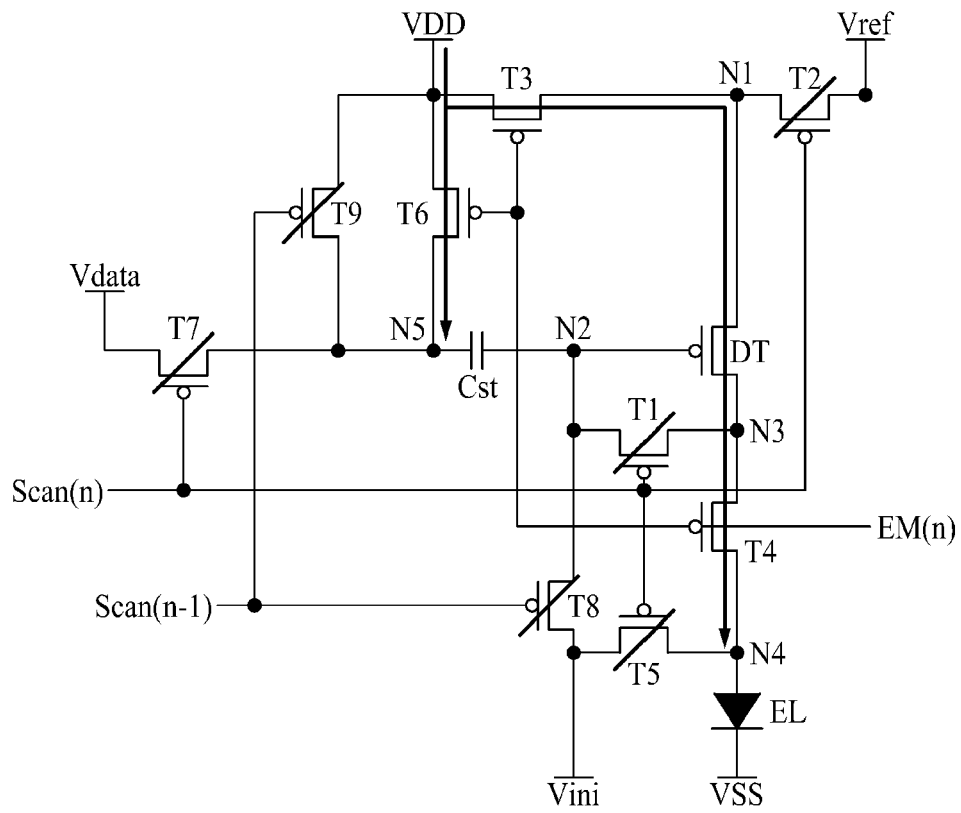
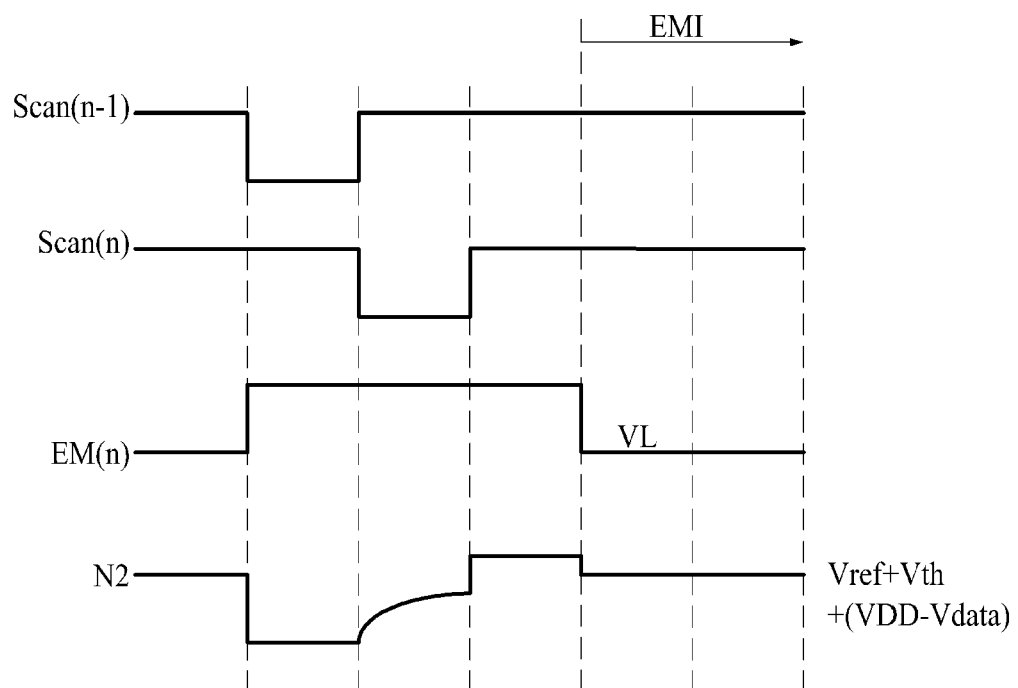


FIG. 24B





EUROPEAN SEARCH REPORT

 Application Number
 EP 18 18 2401

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	CN 103 021 333 B (KUNSHAN NEW FLAT PANEL DISPLAY TECHNOLOGY CT CO LTD) 20 January 2016 (2016-01-20) * par. 1, 12-14, 31-44 fig. 2-3 *	1-5, 12-14	INV. G09G3/3233
A	----- EP 3 098 804 A2 (LG DISPLAY CO LTD [KR]) 30 November 2016 (2016-11-30) * fig. 14A-14C par. 47, 73-74, 120 *	6-9,15	
Y	----- CN 107 274 829 A (SHANGHAI TIANMA AM-OLED CO LTD) 20 October 2017 (2017-10-20) * fig. 1A * & US 2018/130409 A1 (XIANG DONGXU [CN] ET AL) 10 May 2018 (2018-05-10)	5	
A	----- US 2013/057532 A1 (LEE YOUNG-HAK [KR] ET AL) 7 March 2013 (2013-03-07) * the whole document *	6-9,15	
A	----- US 2016/351121 A1 (KIM JUNGCHUL [KR] ET AL) 1 December 2016 (2016-12-01) * the whole document *	6,9-15	TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 22 November 2018	Examiner Bader, Arnaud
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03.82 (P04C01)



Application Number

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing claims for which payment was due.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☒ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

1-9, 12-15

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

☐ The present supplementary European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims (Rule 164 (1) EPC).

**LACK OF UNITY OF INVENTION
SHEET B**

Application Number

EP 18 18 2401

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-5, 12-14

OLED display with a reduction of the influence of the voltage drop of the high level voltage (known), together with a reduction of leakage current.

2. claims: 6-9, 15

OLED display with a reduction of the influence of the voltage drop of the high level voltage (known), together with an initialization of a capacitor.

3. claims: 10, 11

OLED display with a reduction of the influence of the voltage drop of the high level voltage (known), together with gain of physical space for high resolution displays.

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 18 18 2401

5

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

22-11-2018

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CN 103021333 B	20-01-2016	NONE	
EP 3098804 A2	30-11-2016	CN 106205490 A	07-12-2016
		EP 3098804 A2	30-11-2016
		US 2016351124 A1	01-12-2016
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US 2013057532 A1	07-03-2013	KR 20130026338 A	13-03-2013
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US 2016351121 A1	01-12-2016	CN 106205493 A	07-12-2016
		KR 20160141167 A	08-12-2016
		US 2016351121 A1	01-12-2016

专利名称(译)	电致发光显示装置		
公开(公告)号	EP3493189A1	公开(公告)日	2019-06-05
申请号	EP2018182401	申请日	2018-07-09
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KIM DONGHYUN YOO JUHNSUK KIM JUNGCHUL CHUNG HOONJU		
发明人	KIM, DONGHYUN YOO, JUHNSUK KIM, JUNGCHUL JEONG, HAEYOON CHUNG, HOONJU		
IPC分类号	G09G3/3233		
CPC分类号	G09G3/3233 G09G2300/043 G09G2300/0814 G09G2300/0819 G09G2320/0214 G09G2320/0223 G09G3/3258 G09G2310/0243 G09G2310/0264 H01L27/3248 H01L27/3276		
优先权	1020170163682 2017-11-30 KR 1020170163688 2017-11-30 KR		
外部链接	Espacenet		

摘要(译)

公开了一种电致发光显示装置。电致发光显示装置包括显示区域和非显示区域。显示面板包括显示面板，该显示面板包括多个像素线，每个像素线包括多个像素电路。

FIG. 9

