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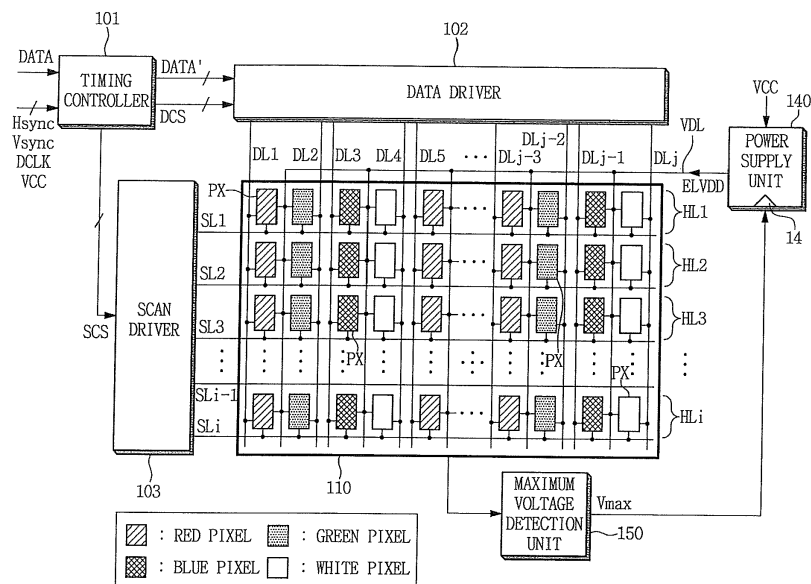
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(54) **LIGHT EMITTING DISPLAY DEVICE**

(57) A light emitting display device including: a display panel; a plurality of pixels included in the display panel, each of the plurality of pixels including a driving switching element connected to a first power line and a light emitting element connected to a second power line; a maximum voltage detection unit for detecting a voltage

from each of the light emitting elements of each of the pixels and outputting a maximum voltage that has a highest voltage level among the detected voltages; and a power supply unit for correcting a first driving voltage based on the maximum voltage and applying the corrected first driving voltage to the first power line.

**FIG. 1**



## Description

### Technical Field

[0001] Embodiments of the present invention relate to a light emitting display device, and more particularly, to a light emitting display device capable of reducing power consumption.

### Description of the Related Art

[0002] Flat panel display devices are lighter and thinner than a traditional cathode ray tube (CRT) television set. Example flat panel devices include a liquid crystal display (LCD) device, a field emission display (FED) device, a plasma display panel (PDP) device, and an organic light emitting diode (OLED) display device.

[0003] OLED display devices display an image using an OLED that generates light by recombination of electrons and holes.

### SUMMARY

[0004] According to an embodiment of the present invention, a light emitting display device includes: a display panel; a plurality of pixels included in the display panel, each of the plurality of pixels including a driving switching element connected to a first power line and a light emitting element connected to a second power line; a maximum voltage detection unit for detecting a voltage from each of the light emitting elements of each of the pixels and outputting a maximum voltage that has a highest voltage level among the detected voltages; and a power supply unit for correcting a first driving voltage based on the maximum voltage and applying the corrected first driving voltage to the first power line.

[0005] The maximum voltage detection unit may include a plurality of diode-type elements, a first terminal of each of the plurality of diode-type elements may be connected to a corresponding one of the light emitting elements, and a second terminal of each of the plurality of diode-type elements may be connected to a feedback input terminal of the power supply unit, and the feedback input terminal may be connected to the second power line.

[0006] The maximum voltage detection unit may further include a resistor connected between the feedback input terminal and the second power line.

[0007] The power supply unit may decrease the first driving voltage as the maximum voltage decreases.

[0008] At least one of the diode-type elements may be a diode or a diode-type transistor.

[0009] The power supply unit may correct the first driving voltage so that a difference voltage between the first driving voltage and a second driving voltage of the second power line may be substantially equal to a sum of the maximum voltage and a minimum drain-source voltage of a driving switching element connected to the light

emitting element having the maximum voltage.

[0010] According to an embodiment of the present invention, a light emitting display device includes: a plurality of first pixels in a first display area of a display panel, each of the plurality of first pixels including a first driving switching element connected to a first power line and a first light emitting element connected to a second power line; a first maximum voltage detection unit for detecting a voltage from each of the first light emitting elements of each of the first pixels and outputting a first maximum voltage that has a highest voltage level among the detected voltages; a first power supply unit for correcting a first driving voltage based on the first maximum voltage and applying the corrected first driving voltage to the first power line; a plurality of second pixels in a second display area of the display panel, each of the plurality of second pixels including a second driving switching element connected to a third power line and a second light emitting element connected to the second power line; a second maximum voltage detection unit for detecting a voltage from each of the second light emitting elements of each of the second pixels and outputting a second maximum voltage that has a highest voltage level among the detected voltages; and a second power supply unit for correcting a third driving voltage based on the second maximum voltage and applying the corrected third driving voltage to the third power line.

[0011] The first maximum voltage detection unit may include: a first resistor connected between a first feedback input terminal of the first power supply unit and the second power line; and a first diode-type element connected between each one of the first light emitting elements of the first pixels and the first resistor, and a first terminal of each of the first diode-type elements may be connected to a corresponding one of the first light emitting elements of the first pixels, and a second terminal of each of the first diode-type elements may be connected to the first feedback input terminal.

[0012] The second maximum voltage detection unit may include: a second resistor connected between a second feedback input terminal of the second power supply unit and the second power line; and a second diode-type element connected between each one of the second light emitting elements of the second pixels and the second resistor, and a first terminal of each of the second diode-type elements may be connected to a corresponding one of the second light emitting elements of the second pixels, and a second terminal of each of the second diode-type elements may be connected to the second feedback input terminal.

[0013] The first power supply unit may correct the first driving voltage so that a difference voltage between the first driving voltage and a second driving voltage of the second power line may be substantially equal to a sum of the first maximum voltage and a minimum drain-source voltage of a first driving switching element connected to the first light emitting element having the first maximum voltage, and the second power supply unit may correct

the third driving voltage so that a difference voltage between the second driving voltage and the third driving voltage may be substantially equal to a sum of the second maximum voltage and a minimum drain-source voltage of a second driving switching element connected to the second light emitting element having the second maximum voltage.

**[0014]** The first light emitting elements may include at least one of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.

**[0015]** The second light emitting elements may include at least one of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.

**[0016]** According to an embodiment of the present invention, a light emitting display device includes: a display panel; a plurality of first pixels disposed in the display panel, each of the plurality of first pixels including a first driving switching element connected to a first power line and a first light emitting element connected to a second power line; a first maximum voltage detection unit for detecting a voltage from each of the first light emitting elements of each of the first pixels and outputting a first maximum voltage that has a highest voltage level among the detected voltages; a first power supply unit for correcting a first driving voltage based on the first maximum voltage and applying the corrected first driving voltage to the first power line; a plurality of second pixels disposed in the display panel, each of the plurality of second pixels including a second driving switching element connected to a third power line and a second light emitting element connected to the second power line; a second maximum voltage detection unit for detecting a voltage from each of the second light emitting elements of each of the second pixels and outputting a second maximum voltage that has a highest voltage level among the detected voltages; and a second power supply unit for correcting a third driving voltage based on the second maximum voltage and applying the corrected third driving voltage to the third power line. The first light emitting element emits a light having a color different from a color of a light emitted from the second light emitting element.

**[0017]** The first maximum voltage detection unit may include: a first resistor connected between a first feedback input terminal of the first power supply unit and the second power line; and a first diode-type element connected between each one of the first light emitting elements of the first pixels and the first resistor, and a first terminal of each of the first diode-type elements may be connected to a corresponding one of the first light emitting elements of the first pixels, and a second terminal of each of the first diode-type elements may be connected to the first feedback input terminal.

**[0018]** The second maximum voltage detection unit may include: a second resistor connected between a second feedback input terminal of the second power supply unit and the second power line; and a second diode-type

element connected between each one of the second light emitting elements of the second pixels and the second resistor, and a first terminal of each of the second diode-type elements may be connected to a corresponding one of the second light emitting elements of the second pixels, and a second terminal of each of the second diode-type elements may be connected to the second feedback input terminal.

**[0019]** The first power supply unit may correct the first driving voltage so that a difference voltage between the first driving voltage and a second driving voltage of the second power line may be substantially equal to a sum of the first maximum voltage and a minimum drain-source voltage of a first driving switching element connected to the first light emitting element having the first maximum voltage, and the second power supply unit may correct the third driving voltage so that a difference voltage between the second driving voltage and the third driving voltage may be substantially equal to a sum of the second maximum voltage and a minimum drain-source voltage of a second driving switching element connected to the second light emitting element having the second maximum voltage.

**[0020]** The first light emitting elements may include at least two of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.

**[0021]** The second light emitting elements may include at least two of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.

**[0022]** According to an embodiment of the present invention, a light emitting display device includes: a display panel including a plurality of pixels, each of the plurality of pixels including a driving switching element connected to a first power line and a light emitting element connected to a second power line; a maximum voltage detection unit for detecting a voltage from each of the light emitting elements of each of the pixels and outputting a maximum voltage that has a highest voltage level among the detected voltages; a timing controller for outputting a highest gray level image data signal having a highest gray level among image data signals applied to the plurality of pixels; a compensation voltage selection unit for storing compensation voltages corresponding to respective gray levels of a plurality of image data signals and selecting a compensation voltage corresponding to the highest gray level image data signal; a compensation voltage update unit for correcting the compensation voltage of the compensation voltage selection unit corresponding to the highest gray level image data signal based on the maximum voltage; and a power supply unit for correcting a first driving voltage based on the compensation voltage selected by the compensation voltage selection unit and applying the corrected first driving voltage to the first power line.

**[0023]** The compensation voltage update unit may further correct at least one other compensation voltage

stored in the compensation voltage selection unit based on a variation amount of the compensation voltage corrected according to the maximum voltage.

**[0024]** When the number of image data signals having a lower gray level than a reference gray level among the image data signals applied to the plurality of pixels exceeds a threshold value, the timing controller may further generate a holding signal and apply the holding signal to the compensation voltage update unit.

**[0025]** In response to the holding signal, the compensation voltage update unit may maintain the compensation voltages of the compensation voltage selection unit to keep values they had before the generation of the highest gray level image data signal, regardless of an input of the highest gray level image data signal.

**[0026]** The compensation voltage update unit may correct the compensation voltage once every  $y$ -th horizontal period ( $y$  being a natural number greater than 2).

**[0027]** The maximum voltage detection unit may include: a resistor connected between a feedback input terminal of the compensation voltage update unit and the second power line; and a diode-type element connected between each one of the light emitting elements and the resistor, and a first terminal of each of the diode-type elements may be connected to a corresponding one of the light emitting elements, and a second terminal of each of the diode-type elements may be connected to the feedback input terminal.

**[0028]** The power supply unit may correct the first driving voltage so that a difference voltage between the first driving voltage and a second driving voltage of the second power line may be substantially equal to a sum of the selected compensation voltage and a minimum drain-source voltage of a driving switching element connected to the light emitting element having the maximum voltage.

**[0029]** The compensation voltage selection unit may be a look-up table.

**[0030]** According to an embodiment of the present invention, a light emitting display device includes: a display panel including a plurality of pixels, each of the plurality of pixels including a driving switching element connected to a first power line and a light emitting element connected to a second power line; a power supply unit for applying a power to the first power line; and a diode connected between an anode electrode of the light emitting element disposed in at least one pixel and a feedback input terminal of the power supply unit.

**[0031]** At least some of the above features that accord with the invention and other features according to the invention are set out in the claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0032]** The above and other features the present invention will be more clearly understood by referring to the following description of embodiments thereof which is given with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram illustrating a light emitting display device according to an embodiment of the present invention;

FIG. 2 is a detailed view illustrating one of pixels illustrated in FIG. 1 according to an embodiment of the present invention;

FIG. 3 is a detailed view illustrating a plurality of pixels and a maximum voltage detection unit of FIG. 1 according to an embodiment of the present invention;

FIG. 4 is an explanatory view illustrating the relationship between the maximum voltage detection unit and a light emitting element of each pixel of FIG. 3 according to an embodiment of the present invention;

FIG. 5 is an enlarged view illustrating portion A of FIG. 3 according to an embodiment of the present invention;

FIG. 6 is an explanatory view illustrating a method of detecting a maximum voltage from first, second, third and fourth pixels of FIG. 5 according to an embodiment of the present invention;

FIGS. 7A, 7B and 7C are explanatory views illustrating a method of driving a display device according to an embodiment of the present invention;

FIG. 8 is an explanatory view illustrating a method of correcting a high electric potential driving voltage based on a maximum voltage of a light emitting element detected from the first, second, third and fourth pixels according to an embodiment of the present invention, and power consumption reducing effects according to the method;

FIG. 9 is a graph illustrating a characteristic curve of a transistor and a characteristic curve of a light emitting element associated with a variation amount of the high electric potential driving voltage of FIG. 8 according to an embodiment of the present invention;

FIG. 10 is an explanatory view illustrating a method of correcting a high electric potential driving voltage based on a maximum voltage of a light emitting element detected from the first, second, third and fourth pixels according to an embodiment of the present invention and power consumption reducing effects according to the method;

FIG. 11 is a graph illustrating a characteristic curve of a transistor and a characteristic curve of a light emitting element associated with a variation amount of the high electric potential driving voltage of FIG. 10 according to an embodiment of the present invention;

FIG. 12 is a detailed view illustrating the plurality of pixels and the maximum voltage detection unit of FIG. 1 according to an embodiment of the present invention;

FIG. 13 is an explanatory view illustrating the relationship among first and second maximum voltage detection units and a light emitting element of each

pixel of FIG. 12 according to an embodiment of the present invention;

FIG. 14 is a detailed view illustrating the plurality of pixels and the maximum voltage detection unit of FIG. 1 according to an embodiment of the present invention;

FIG. 15 is an explanatory view illustrating the relationship among first, second, third and fourth maximum voltage detection units and a light emitting element of each pixel of FIG. 14 according to an embodiment of the present invention;

FIG. 16 is a block diagram illustrating a light emitting display device according to an embodiment of the present invention;

FIG. 17 is an explanatory view illustrating the relationship among a maximum voltage detection unit, a compensation value output unit, and a light emitting element of each pixel in FIG. 16 according to an embodiment of the present invention;

FIG. 18 is a detailed block diagram illustrating the compensation value output unit of FIG. 16 according to an embodiment of the present invention;

FIG. 19 is an explanatory view illustrating a time-dependent variation of compensation voltages stored in a compensation voltage selection unit of FIG. 18 according to an embodiment of the present invention; and

FIG. 20 is an explanatory view illustrating a variation of a high electric potential driving voltage by the compensation value output unit of FIG. 16 according to an embodiment of the present invention.

## DETAILED DESCRIPTION

**[0033]** Hereinafter, embodiments of the present invention will be described more fully with reference to the accompanying drawings. The present invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Like reference numerals may refer to like elements throughout the specification.

**[0034]** In the drawings, thicknesses of a plurality of layers and areas may be illustrated in an enlarged manner for clarity and ease of description thereof. When a layer, area, or plate is referred to as being "on" another layer, area, or plate, it may be directly on the other layer, area, or plate, or intervening layers, areas, or plates may be present therebetween.

**[0035]** Throughout the specification, when an element is referred to as being "connected" to another element, the element is "directly connected" to the other element, or "electrically connected" to the other element with one or more intervening elements interposed therebetween.

**[0036]** Hereinafter, a light emitting display device according to embodiments of the present invention will be described with reference to FIGS. 1 to 20.

**[0037]** FIG. 1 is a block diagram illustrating a light emitting display device according to an embodiment of the

present invention, and FIG. 2 is a detailed view illustrating one of pixels illustrated in FIG. 1 according to an embodiment of the present invention.

**[0038]** As illustrated in FIG. 1, the display device includes a display panel 110, a timing controller 101, a scan driver 103, a data driver 102, a power supply unit 140, and a maximum voltage detection unit 150.

**[0039]** The display panel 110 includes  $i$  number of scan lines SL1 to SL $i$ ,  $j$  number of data lines DL1 to DL $j$ ,  $i * j$  number of pixels PX, a high electric potential power line VDL and a low electric potential power line VSL. For the low electric potential power line VSL, refer to FIG. 2. In an embodiment of the present invention, each of  $i$  and  $j$  is a natural number greater than 1.

**[0040]** First to  $i$ -th scan signals are applied to the first to  $i$ -th scan lines SL1 to SL $i$ , and first to  $j$ -th data voltages are applied to the first to  $j$ -th data lines DL1 to DL $j$ .

**[0041]** The pixels PX are arranged on the display panel 110 in a matrix. The pixels PX may include red pixels for emitting red light, green pixels for emitting green light, blue pixels for emitting blue light, and white pixels for emitting white light.

**[0042]** A pixel connected to a  $(4p + 1)$ -th data line may be a red pixel, a pixel connected to a  $(4p + 2)$ -th data line may be a green pixel, a pixel connected to a  $(4p + 3)$ -th data line may be a blue pixel, and a pixel connected to a  $(4p + 4)$ -th data line may be a white pixel. In an embodiment of the present invention,  $p$  is 0 or a natural number. For example, as illustrated in FIG. 1, a pixel PX connected to the first data line DL1 may be a red pixel, a pixel PX connected to the second data line DL2 may be a green pixel, a pixel PX connected to the third data line DL3 may be a blue pixel, and a pixel PX connected to the fourth data line DL4 may be a white pixel.

**[0043]** A red pixel, a green pixel, a blue pixel and a white pixel adjacent to each other in a horizontal direction may be a unit pixel for displaying one unit image.

**[0044]** In an embodiment of the present invention,  $j$  number of pixels (hereinafter,  $n$ -th horizontal line pixels) arranged along an  $n$ -th horizontal line are individually connected to the first to  $j$ -th data lines DL1 to DL $j$ , respectively. In addition, the  $n$ -th horizontal line pixels are connected in common to the  $n$ -th scan line, wherein  $n$  (of the  $n$ -th scan line) is one selected from 1 to  $i$ .

**[0045]** The  $n$ -th horizontal line pixels receive an  $n$ -th scan signal in common. In other words, all of  $j$  number of pixels located in the same horizontal line receive the same scan signal, but pixels located in different horizontal lines receive different scan signals. For example, red pixels, green pixels, blue pixels and white pixels located in the first horizontal line HL1 all receive a first scan signal, while red pixels, green pixels, blue pixels and white pixels located in the second horizontal line HL2 all receive a second scan signal that is output later in time than the first scan signal.

**[0046]** Two adjacent ones of the  $n$ -th horizontal line pixels are located between a  $(2q-1)$ -th data line and a  $2q$ -th data line, wherein  $q$  is a natural number. In other

words, two adjacent pixels of a horizontal line are located between a pair of data lines. For example, as illustrated in FIG. 1, a red pixel which is most adjacent to the scan driver 103 among the first horizontal line pixels and a green pixel adjacent to the red pixel are located between the first data line DL1 and the second data line DL2.

**[0047]** In the display panel 110, the high electric potential power line VDL is located between the  $(2q-1)$ -th data line and the  $2q$ -th data line. In an embodiment of the present invention, one of two adjacent pixels between the  $(2q-1)$ -th data line and the  $2q$ -th data line among the  $n$ -th horizontal line pixels is between the  $(2q-1)$ -th data line and the high electric potential power line VDL and the other of the two adjacent pixels is between the high electric potential power line VDL and the  $2q$ -th data line. For example, as illustrated in FIG. 1, the red pixel which is most adjacent to the scan driver 103 among the first horizontal line pixels is between the first data line DL1 and the high electric potential power line VDL, and the green pixel adjacent to the red pixel is between the high electric potential power line VDL and the second data line DL2.

**[0048]** As will be described in detail later, the two adjacent pixels between the  $(2q-1)$ -th data line and the  $2q$ -th data line among the  $n$ -th horizontal line pixels may have a symmetrical shape with respect to the high electric potential power line VDL passing between the two adjacent pixels.

**[0049]** Each pixel PX receives a high electric potential driving voltage ELVDD and a low electric potential driving voltage ELVSS.

**[0050]** Hereinafter, configurations of one of the pixels illustrated in FIG. 1 will be described in detail with reference to FIG. 2.

**[0051]** As illustrated in FIG. 2, an  $n$ -th pixel PX $_n$  may include a driving switching element Tdr, a data switching element Tsw, a storage capacitor Cst and a light emitting element (e.g., a light emitting diode, hereinafter referred to as "light emitting element LED").

**[0052]** The data switching element Tsw includes a gate electrode connected to an  $n$ -th scan line SL $_n$  and is connected between an  $m$ -th data line DL $_m$  and a gate electrode of the driving switching element Tdr. A drain electrode of the data switching element Tsw is connected to the  $m$ -th data line DL $_m$ , and a source electrode of the data switching element Tsw is connected to the gate electrode of the driving switching element Tdr, wherein  $m$  is a natural number.

**[0053]** The driving switching element Tdr includes the gate electrode connected to the source electrode of the data switching element Tsw and is connected between the high electric potential power line VDL and an anode electrode of the light emitting element LED. A drain electrode of the driving switching element Tdr is connected to the high electric potential power line VDL, and a source electrode of the driving switching element Tdr is connected to the anode electrode of the light emitting element LED.

**[0054]** The driving switching element Tdr adjusts an amount (e.g., density) of a driving current flowing from the high electric potential power line VDL to the low electric potential power line VSL according to a level of a signal applied to the gate electrode of the driving switching element Tdr.

**[0055]** The storage capacitor Cst is connected between the gate electrode of the driving switching element Tdr and the anode electrode of the light emitting element LED. The storage capacitor Cst stores a signal applied to the gate electrode of the driving switching element Tdr for one frame period.

**[0056]** The light emitting element LED emits light in accordance with the driving current applied through the driving switching element Tdr. The light emitting element LED emits light of a different brightness depending on the level of the driving current. The anode electrode of the light emitting element LED is connected to the source electrode (or the drain electrode) of the driving switching element Tdr, and a cathode electrode of the light emitting element LED is connected to the low electric potential power line VSL. The light emitting element LED may be an organic light emitting diode (OLED).

**[0057]** A light emitting element LED of the red pixel is a red light emitting element LED that emits a red light, a light emitting element LED of the green pixel is a green light emitting element LED that emits a green light, a light emitting element LED of the blue pixel is a blue light emitting element LED that emits a blue light, and a light emitting element LED of a white pixel is a white light emitting element LED that emits a white light.

**[0058]** It is to be understood the pixels may have various structures other than the structure illustrated in FIG. 2 and described above. For example, a pixel may further include a light emission control switching element connected between the high electric potential power line VDL and the driving switching element Tdr, and may further include another light emission control switching element connected between the driving switching element Tdr and the anode electrode of the light emitting element LED. In an embodiment of the present invention, the high electric potential power line VDL is indirectly connected to the driving switching element Tdr through the light emission control switching element.

**[0059]** As illustrated in FIG. 1, the timing controller 101 receives a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, an image data signal DATA, a reference clock signal DCLK and the like, which are output from a graphic controller provided in a system.

**[0060]** An interface circuit is provided between the timing controller 101 and the system, and the aforementioned signals output from the system are input to the timing controller 101 through the interface circuit. The interface circuit may be embedded in the timing controller 101.

**[0061]** The interface circuit may include a low voltage differential signaling (LVDS) receiver. The interface cir-

cuit lowers voltage levels of the vertical synchronization signal Vsync, the horizontal synchronization signal Hsync, the image data signal DATA and the reference clock signal DCLK output from the system, while raising frequencies thereof.

**[0062]** Electromagnetic interference (EMI) may occur due to high frequency components of a signal input from the interface circuit to the timing controller 101. To prevent the EMI, an EMI filter may be further provided between the interface circuit and the timing controller 101.

**[0063]** The timing controller 101 generates a scan control signal SCS for controlling the scan driver 103 and a data control signal DCS for controlling the data driver 102, using the vertical synchronization signal Vsync, the horizontal synchronization signal Hsync, and the reference clock signal DCLK.

**[0064]** The scan control signal SCS includes a gate start pulse, a gate shift clock, a gate output enable signal and the like.

**[0065]** The data control signal DCS includes a source start pulse, a source shift clock, a source output enable signal and the like.

**[0066]** In addition, the timing controller 101 rearranges the image data signals DATA input through the system and applies the rearranged image data signals DATA' to the data driver 102.

**[0067]** In an embodiment of the present invention, the timing controller 101 is operated by a driving power VCC output from a power unit provided in the system. For example, the driving power VCC is used as a power voltage of a phase locked loop ("PLL") circuit embedded in the timing controller 101.

**[0068]** The PLL circuit compares a reference clock signal DCLK input to the timing controller 101 with a reference frequency generated from an oscillator. When there is a deviation between the reference clock signal DCLK and the reference frequency, the PLL circuit adjusts the frequency of the reference clock signal DCLK by the deviation to generate a sampling clock signal. This sampling clock signal is a signal for sampling the image data signals DATA'.

**[0069]** The power supply unit 140 increases or decreases a driving power VCC input through the system to generate various voltages required for the display panel 110. The power supply unit 140 may be a direct current (DC) to DC converter.

**[0070]** The power supply unit 140 may include, for example, an output switching element for switching an output voltage of an output terminal thereof. The power supply unit 140 may include, for example, a pulse width modulator PWM for adjusting a duty ratio or a frequency of a control signal applied to a control terminal of the output switching element to increase or decrease the output voltage. Herein, the power supply unit 140 may include a pulse frequency modulator PFM, instead of the pulse width modulator PWM.

**[0071]** The pulse width modulator PWM may increase the duty ratio of the aforementioned control signal to raise

the output voltage of the power supply unit 140 or decrease the duty ratio of the control signal to lower the output voltage of the power supply unit 140. The pulse frequency modulator PFM may increase the frequency of the aforementioned control signal to raise the output voltage of the power supply unit 140 or decrease the frequency of the control signal to lower the output voltage of the power supply unit 140.

**[0072]** The output voltage of the power supply unit 140 may include the high electric potential driving voltage ELVDD and the low electric potential driving voltage ELVSS (refer to FIG. 2 for ELVSS). In addition, the output voltage of the power supply unit 140 may further include a reference voltage, gamma reference voltages, a gate high voltage, and a gate low voltage.

**[0073]** The gamma reference voltages are voltages generated by voltage division of the reference voltage. The gamma reference voltages are analog voltages, which are applied to the data driver 102.

**[0074]** The high electric potential driving voltage ELVDD and the low electric potential driving voltage ELVSS output from the power supply unit 140 are applied to the display panel 110. For example, the high electric potential driving voltage ELVDD is applied to the pixels PX of the display panel 110 through the high electric potential power line VDL, and the low electric potential driving voltage ELVSS is applied to the pixels PX of the display panel 110 through the low electric potential power line VSL.

**[0075]** The gate high voltage is a high logic voltage of a gate signal set to be equal to or higher than a threshold voltage of the data switching element Tsw. The gate low voltage is a low logic voltage of the gate signal set to be an off voltage of the data switching element Tsw. The gate high voltage and the gate low voltage are applied to the scan driver 103.

**[0076]** The scan driver 103 generates scan signals according to the scan control signal SCS provided from the timing controller 101 and sequentially applies the scan signals to the plurality of scan lines SL1 to SLi.

**[0077]** The scan driver 103 may include, for example, a shift register that shifts the gate start pulse according to the gate shift clock to generate scan signals. The shift register may include a plurality of switching elements. The switching elements may be formed at a non-display area of the display panel 110. The switching elements may be formed through a substantially same process as a process through which the data switching element Tsw and the driving switching element Tdr at a display area of the display panel 110 are formed.

**[0078]** The data driver 102 receives the image data signals DATA' and the data control signal DCS from the timing controller 101. The data driver 102 samples the image data signals DATA' according to the data control signal DCS, sequentially latches the sampled image data signals corresponding to one horizontal line in each horizontal period, and simultaneously applies the latched image data signals to the data lines DL1 to DLj.

**[0079]** For example, the data driver 102 converts the image data signals DATA' applied from the timing controller 101 into analog image data signals using the gamma reference voltages input from the power supply unit 140 and applies the analog image data signals to the data lines DL1 to DLj.

**[0080]** The data driver 102 may include a gray level generator, which generates a plurality of gray level voltages using the gamma reference voltages applied from the power supply unit 140. The data driver 102 converts the image data signals DATA' applied from the timing controller 101 into analog signals using the gray level voltages.

**[0081]** In an embodiment of the present invention, the gray level generator may be located inside or outside the data driver 102.

**[0082]** The maximum voltage detection unit 150 detects a greatest voltage among respective voltages of the light emitting elements LED provided in the respective pixels PX. To accomplish this, the maximum voltage detection unit 150 detects a voltage from each of the light emitting elements LED in each pixel PX, selects a greatest voltage (hereinafter, "a maximum voltage Vmax") among the detected voltages, and applies the selected maximum voltage Vmax to the power supply unit 140. For example, the maximum voltage detection unit 150 detects  $i * j$  number of voltages from all pixels PX included in the display panel 110, and selects a greatest voltage among the  $i * j$  number of voltages to output the greatest voltage. For example,  $i * j$  number of voltages are selected because there are  $i * j$  number of pixels. In other words, as illustrated in FIG. 2, in a case where one light emitting element LED is provided for each pixel PX, the maximum voltage detection unit 150 detects  $i * j$  number of voltages from the  $i * j$  number of light emitting elements LEDs, and selects a greatest voltage that has a highest voltage level among the detected  $i * j$  number of voltages as the maximum voltage Vmax. The aforementioned voltage of the light emitting element LED refers to a voltage across opposite ends of the light emitting element LED. In other words, the voltage of the light emitting element LED refers to a voltage substantially equal to a difference between a voltage of the anode electrode of the light emitting element LED and the low electric potential driving voltage ELVSS.

**[0083]** The maximum voltage detection unit 150 may detect a voltage from the anode electrode of the light emitting element LED.

**[0084]** The maximum voltage detection unit 150 may be located outside the display panel 110. Alternatively, at least one of the components of the maximum voltage detection unit 150 may be located inside the display panel 110.

**[0085]** The maximum voltage Vmax output from the maximum voltage detection unit 150 is applied to the power supply unit 140. For example, the maximum voltage Vmax is input to a feedback input terminal 14 of the power supply unit 140.

**[0086]** The power supply unit 140 corrects the high electric potential driving voltage ELVDD based on the maximum voltage Vmax applied from the maximum voltage detection unit 150 and applies the corrected high electric potential driving voltage ELVDD to the high electric potential power line VDL.

**[0087]** FIG. 3 is a detailed view illustrating the plurality of pixels and the maximum voltage detection unit 150 of FIG. 1 according to an embodiment of the present invention, FIG. 4 is an explanatory view illustrating the relationship between the maximum voltage detection unit 150 and the light emitting element LED of each pixel of FIG. 3 according to an embodiment of the present invention, and FIG. 5 is an enlarged view illustrating portion A of FIG. 3 according to an embodiment of the present invention.

**[0088]** As illustrated in FIGS. 3 and 4, the maximum voltage detection unit 150 includes a plurality of diode-type elements D and at least one resistor R.

**[0089]** The plurality of diode-type elements D and the resistor R may be located on the display panel 110, as illustrated in FIG. 3. For example, the diode-type element D may be located on the display panel 110, one for each pixel PX. As a more specific example, as illustrated in FIG. 5, one diode-type element D is located in each of the first, second, third and fourth pixels PX1, PX2, PX3 and PX4.

**[0090]** The diode-type element D may be a diode or a diode-type transistor. For example, as illustrated in FIG. 5, the diode-type element D may be a diode-type transistor including a gate electrode connected to the anode electrode of the light emitting element LED and connected between the anode electrode and a feedback line FL. The gate electrode and a drain electrode of the diode-type element D are connected in common to the anode electrode. In an embodiment of the present invention, a contact point between the gate electrode and the drain electrode of the diode-type element D is an anode electrode of the diode-type element D, and a source electrode of the diode-type element D is a cathode electrode of the diode-type element D.

**[0091]** The respective anode electrodes of the diode-type elements D are individually connected to the light emitting elements LED, respectively. For example, as illustrated in FIG. 4, the respective anode electrodes of the diode-type elements D are individually connected to the anode electrodes of the light emitting elements LED, respectively.

**[0092]** The respective cathode electrodes of the diode-type elements D are connected in common to the feedback line FL, as illustrated in FIG. 4. The respective cathode electrodes of the diode-type elements D are connected in common to the feedback input terminal 14 of the power supply unit 140 through the feedback line FL.

**[0093]** The resistor R is connected between the feedback line FL and the low electric potential power line VSL, as illustrated in FIGS. 3 and 4. The resistor R is connected to the feedback input terminal 14 of the power supply unit

140 through the feedback line FL. In addition, one terminal of the resistor R is connected to the respective cathode electrodes of the diode-type elements D through the feedback line FL.

**[0094]** As described above, two adjacent ones of the n-th horizontal line pixels PX between the (2q-1)-th data line and the 2q-th data line may have a symmetrical shape with respect to the high electric potential power line VDL passing between the two adjacent pixels PX. For example, as illustrated in FIG. 5, a first pixel PX1 and a second pixel PX2 connected in common to a first scan line SL1 are between the first data line DL1 and the second data line DL2. Here, the first pixel PX1 and the second pixel PX2 may have a symmetrical shape with respect to the high electric potential power line VDL passing between the first pixel PX1 and the second pixel PX2. For example, with respect to the high electric potential power line VDL, the data switching element Tsw, the driving switching element Tdr, the storage capacitor Cst, the light emitting element LED and the diode-type element D of the first pixel PX1 may have symmetry with the data switching element Tsw, the driving switching element Tdr, the storage capacitor Cst, the light emitting element LED and the diode-type element D of the second pixel PX2, respectively.

**[0095]** FIG. 6 is an explanatory view illustrating a method of detecting the maximum voltage Vmax from the first, second, third and fourth pixels PX1, PX2, PX3 and PX4 of FIG. 5 according to an embodiment of the present invention.

**[0096]** The aforementioned diode-type element D may be a diode, as illustrated in FIG. 6.

**[0097]** In the case where four pixels PX are provided in the display panel 110 as illustrated in FIG. 6, first, second, third and fourth diode-type elements D1, D2, D3 and D4 detect voltages of respective light emitting elements LED1, LED2, LED3 and LED4 provided in the four pixels PX1, PX2, PX3, and PX4, respectively, select a maximum voltage Vmax that has a highest voltage level among the detected voltages, and output the maximum voltage Vmax to the feedback line FL.

**[0098]** When data voltages of different gray levels are applied to the first, second, third and fourth pixels PX1, PX2, PX3 and PX4, voltages of the respective light emitting elements LED1, LED2, LED3 and LED4 provided in the four pixels PX1, PX2, PX3, and PX4 are different from each other. For example, when a greatest data voltage is applied to the fourth pixel PX4 among the first, second, third and fourth pixels PX1, PX2, PX3 and PX4, a voltage of the light emitting element LED4 in the fourth pixel PX4 has a highest voltage level. In other words, a voltage of a fourth node n4 among voltages of first, second, third and fourth nodes n1, n2, n3 and n4 is the greatest.

**[0099]** The first node n1 refers to an anode electrode of the first light emitting element LED1 provided in the first pixel PX1, the second node n2 refers to an anode electrode of the second light emitting element LED2 provided in the second pixel PX2, the third node n3 refers

to an anode electrode of the third light emitting element LED3 provided in the third pixel PX3, and the fourth node n4 refers to an anode electrode of the fourth light emitting element LED4 provided in the fourth pixel PX4.

**[0100]** When the voltage of the fourth node n4 has a highest voltage level as described above, the voltage of the fourth node n4 is applied to the feedback line FL through the fourth diode-type element D4. Since the voltages of the first, second and third nodes n1, n2 and n3 are less than the voltage of the fourth node n4, the first, second and third diode-type elements D1, D2 and D3 are biased in the reverse direction by the voltage of the fourth node n4 applied to the feedback line FL. Accordingly, the voltage of the feedback line FL is substantially equal to the voltage of the fourth node n4. To be more exact, the voltage of the feedback line FL is a voltage obtained by subtracting a threshold voltage of the fourth diode-type element D4 from the voltage of the fourth node n4.

**[0101]** The maximum voltage Vmax applied to the feedback line FL, in other words, the voltage of the fourth node n4 is applied to the power supply unit 140 through the feedback input terminal 14.

**[0102]** The power supply unit 140 corrects the high electric potential driving voltage ELVDD based on the maximum voltage Vmax. For example, the power supply unit 140 decreases or increases a level of the high electric potential driving voltage ELVDD according to the level of the maximum voltage Vmax. For example, the power supply unit 140 decreases the high electric potential driving voltage ELVDD as the maximum voltage Vmax decreases. As a more specific example, the power supply unit 140 adjusts the level of the high electric potential driving voltage ELVDD so that the following Mathematical Formula 1 is satisfied.

<Mathematical Formula 1>

$$ELVDD - ELVSS = V_{max} + V_{ds.min}$$

**[0103]** In the above Mathematical Formula 1, Vds.min denotes a minimum drain-source voltage Vds.min of the driving switching element Tdr.

**[0104]** The minimum drain-source voltage Vds.min refers to a drain-source voltage that has a lowest voltage level among drain-source voltages of the driving switching element Tdr that may stably generate a driving current of a predetermined gray level. In other words, the minimum drain-source voltage Vds.min of the driving switching element Tdr is a drain-source voltage that has a lowest voltage level among drain-source voltages of the driving switching element Tdr that may generate a driving current of a predetermined gray level in a saturation region of the driving switching element Tdr.

**[0105]** A drain voltage of the driving switching element Tdr is a voltage of the drain electrode of the driving switching element Tdr, a source voltage of the driving switching element Tdr is a voltage of the source electrode of the

driving switching element Tdr, and a drain-source voltage of the driving switching element Tdr is a difference voltage obtained by subtracting the voltage of the source electrode of the driving switching element Tdr from the voltage of the drain electrode of the driving switching element Tdr.

**[0106]** According to the above Mathematical Formula 1, the power supply unit 140 corrects the high electric potential driving voltage ELVDD so that a difference voltage between the high electric potential driving voltage ELVDD and the low electric potential driving voltage ELVSS becomes substantially equal to a sum of the maximum voltage Vmax and the minimum drain-source voltage Vds.min of the driving switching element Tdr. Accordingly, when the low electric potential driving voltage ELVSS and the minimum drain-source voltage Vds.min of the driving switching element Tdr are constant, the high electric potential driving voltage ELVDD decreases as the maximum voltage Vmax decreases.

**[0107]** FIGS. 7A, 7B and 7C are explanatory views illustrating a method of driving a display device according to an embodiment of the present invention.

**[0108]** For ease of description, it is assumed that the display panel 110 of the display device includes a total of 12 pixels PX1 to PX12, as illustrated in FIGS. 7A, 7B and 7C. Further, for ease of description, a data switching element Tsw and a storage capacitor Cst of each of the pixels PX1 to PX12 are not illustrated.

**[0109]** First, as illustrated in FIG. 7A, a first scan signal SC1 is applied to the first scan line SL1 in a first horizontal period. Then, the first, second, third and fourth pixels PX1, PX2, PX3 and PX4 connected to the first scan line SL1 are activated. The first scan signal SC1 is applied to each of a gate electrode of a data switching element in the first pixel PX1, a gate electrode of a data switching element in the second pixel PX2, a gate electrode of a data switching element in the third pixel PX3, and a gate electrode of a data switching element in the fourth pixel PX4. Accordingly, the respective data switching elements of the first, second, third and fourth pixels PX1, PX2, PX3 and PX4 are turned on.

**[0110]** In an embodiment of the present invention, the activated first pixel PX1 receives a first data voltage Vdt1 through a first data line DL1 connected thereto, the activated second pixel PX2 receives a second data voltage Vdt2 through a second data line DL2 connected thereto, the activated third pixel PX3 receives a third data voltage Vdt3 through a third data line DL3 connected thereto, and the activated fourth pixel PX4 receives a fourth data voltage Vdt4 through a fourth data line DL4 connected thereto.

**[0111]** The first data voltage Vdt1 is applied to a drain electrode and a source electrode of the data switching element in the first pixel PX1, the second data voltage Vdt2 is applied to a drain electrode and a source electrode of the data switching element in the second pixel PX2, the third data voltage Vdt3 is applied to a drain electrode and a source electrode of the data switching

element in the third pixel PX3, and the fourth data voltage Vdt4 is applied to a drain electrode and a source electrode of the data switching element in the fourth pixel PX4.

5 **[0112]** Then, the first data voltage Vdt1 is applied to a gate electrode of a first driving switching element Tdr1 through the turned-on data switching element of the first pixel PX1, the second data voltage Vdt2 is applied to a gate electrode of a second driving switching element  
10 Tdr2 through the turned-on data switching element of the second pixel PX2, the third data voltage Vdt3 is applied to a gate electrode of a third driving switching element Tdr3 through the turned-on data switching element of the third pixel PX3, and the fourth data voltage Vdt4 is applied  
15 to a gate electrode of a fourth driving switching element Tdr4 through the turned-on data switching element of the fourth pixel PX4. Accordingly, the first, second, third and fourth driving switching elements Tdr1, Tdr2, Tdr3 and Tdr4 are turned on.

20 **[0113]** A first light emitting element LED1 emits light by a driving current generated through the turned on first driving switching element Tdr1, a second light emitting element LED2 emits light by a driving current generated through the turned on second driving switching element  
25 Tdr2, a third light emitting element LED3 emits light by a driving current generated through the turned on third driving switching element Tdr3, and a fourth light emitting element LED4 emits light by a driving current generated through the turned on fourth driving switching element  
30 Tdr4.

**[0114]** In an embodiment of the present invention, a voltage of the first light emitting element LED1 is determined based on the first data voltage Vdt1 applied to the gate electrode of the first driving switching element Tdr1, a voltage of the second light emitting element LED2 is determined based on the second data voltage Vdt2 applied to the gate electrode of the second driving switching element Tdr2, a voltage of the third light emitting element LED3 is determined based on the third data voltage Vdt3 applied to the gate electrode of the third driving switching element Tdr3, and a voltage of the fourth light emitting element LED4 is determined based on the fourth data voltage Vdt4 applied to the gate electrode of the fourth driving switching element Tdr4. The respective voltages  
35 of the first, second, third and fourth light emitting elements LED1, LED2, LED3 and LED4 are maintained for one frame period.

**[0115]** During a first horizontal period, the voltage of the first light emitting element LED1 is detected through a first diode-type element D1, the voltage of the second light emitting element LED2 is detected through a second diode-type element D2, the voltage of the third light emitting element LED3 is detected through a third diode-type element D3, and the voltage of the fourth light emitting element LED4 is detected through a fourth diode-type element D4.  
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**[0116]** In an embodiment of the present invention, during the first horizontal period, voltages of the fifth, sixth,

seventh, eighth, ninth, tenth, eleventh and twelfth light emitting elements LED5, LED6, LED7, LED8, LED9, LED10, LED11 and LED12 are detected in the fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth pixels PX5, PX6, PX7, PX8, PX9, PX10, PX11 and PX12 that are in an inactive state. The voltages of the fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth light emitting elements LED5, LED6, LED7, LED8, LED9, LED10, LED11 and LED12 are detected through fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth diode-type elements D5, D6, D7, D8, D9, D10, D11 and D12, respectively. In an embodiment of the present invention, during the first horizontal period, the fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth pixels PX5, PX6, PX7, PX8, PX9, PX10, PX11 and PX12 that are in the inactive state respectively maintain the data voltages applied in a previous frame period. Accordingly, the voltages of the fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth light emitting elements LED5, LED6, LED7, LED8, LED9, LED10, LED11 and LED12 detected in the first horizontal period are voltages determined based on data voltages of the previous frame period.

**[0117]** The aforementioned first horizontal period is a horizontal period included in a current frame period. Further, the data voltages maintained by the fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth pixels PX5, PX6, PX7, PX8, PX9, PX10, PX11 and PX12 in the first horizontal period may be data voltages applied in one horizontal period of the aforementioned previous frame period.

**[0118]** A maximum voltage  $V_{max}$  among the voltages detected from the first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth light emitting elements LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11 and LED12 in the first horizontal period is applied to a power supply unit 140 through a feedback line FL.

**[0119]** The power supply unit 140 corrects a high electric potential driving voltage ELVDD based on the maximum voltage  $V_{max}$  detected in the first horizontal period.

**[0120]** Subsequently, as illustrated in FIG. 7B, a second scan signal SC2 is applied to a second scan line SL2 in a second horizontal period. Then, the fifth, sixth, seventh and eighth pixels PX5, PX6, PX7 and PX8 connected to the second scan line SL2 are activated.

**[0121]** In an embodiment of the present invention, the activated fifth pixel PX5 receives a fifth data voltage Vdt5 through the first data line DL1 connected thereto, the activated sixth pixel PX6 receives a sixth data voltage Vdt6 through the second data line DL2 connected thereto, the activated seventh pixel PX7 receives a seventh data voltage Vdt7 through the third data line DL3 connected thereto, and the activated eighth pixel PX8 receives an eighth data voltage Vdt8 through the fourth data line DL4 connected thereto.

**[0122]** In an embodiment of the present invention, the fifth data voltage Vdt5 is applied to a gate electrode of a

fifth driving switching element Tdr5, the sixth data voltage Vdt6 is applied to a gate electrode of a sixth driving switching element Tdr6, the seventh data voltage Vdt7 is applied to a gate electrode of a seventh driving switching element Tdr7, and the eighth data voltage Vdt8 is applied to a gate electrode of an eighth driving switching element Tdr8. Accordingly, the fifth, sixth, seventh and eighth driving switching elements Tdr5, Tdr6, Tdr7 and Tdr8 are turned on. Further, the fifth, sixth, seventh and eighth light emitting elements LED5, LED6, LED7 and LED8 emit light by the turned on fifth, sixth, seventh and eighth driving switching elements Tdr5, Tdr6, Tdr7 and Tdr8.

**[0123]** In an embodiment of the present invention, a voltage of the fifth light emitting element LED5 is determined based on the fifth data voltage Vdt5 applied to the gate electrode of the fifth driving switching element Tdr5, a voltage of the sixth light emitting element LED6 is determined based on the sixth data voltage Vdt6 applied to the gate electrode of the sixth driving switching element Tdr6, a voltage of the seventh light emitting element LED7 is determined based on the seventh data voltage Vdt7 applied to the gate electrode of the seventh driving switching element Tdr7, and a voltage of the eighth light emitting element LED8 is determined based on the eighth data voltage Vdt8 applied to the gate electrode of the eighth driving switching element Tdr8. The respective voltages of the fifth, sixth, seventh and eighth light emitting elements LED5, LED6, LED7 and LED8 are maintained for one frame period.

**[0124]** During the second horizontal period, the voltage of the fifth light emitting element LED5 is detected through the fifth diode-type element D5, the voltage of the sixth light emitting element LED6 is detected through the sixth diode-type element D6, the voltage of the seventh light emitting element LED7 is detected through the seventh diode-type element D7, and the voltage of the eighth light emitting element LED8 is detected through the eighth diode-type element D8.

**[0125]** In an embodiment of the present invention, during the second horizontal period, voltages of the first, second, third, fourth, ninth, tenth, eleventh and twelfth light emitting elements LED1, LED2, LED3, LED4, LED9, LED10, LED11 and LED12 are detected from the first, second, third, fourth, ninth, tenth, eleventh and twelfth pixels PX1, PX2, PX3, PX4, PX9, PX10, PX11 and PX12 that are in the inactive state. The voltages of the first, second, third, fourth, ninth, tenth, eleventh and twelfth light emitting elements LED1, LED2, LED3, LED4, LED9, LED10, LED11 and LED12 are respectively detected through the first, second, third, fourth, ninth, tenth, eleventh and twelfth diode-type elements D1, D2, D3, D4, D9, D10, D11 and D12. In an embodiment of the present invention, during the second horizontal period, the first, second, third and fourth pixels PX1, PX2, PX3 and PX4 in the inactive state respectively maintain the first, second, third and fourth data voltages Vdt1, Vdt2, Vdt3 and Vdt4 applied in the first horizontal period, and the ninth,

tenth, eleventh and twelfth pixels PX9, PX10, PX11 and PX12 respectively maintain the data voltages applied in the previous frame period. Accordingly, voltages of the first, second, third and fourth light emitting elements LED1, LED2, LED3 and LED4 detected in the second horizontal period are voltages determined based on the first, second, third and fourth data voltages Vdt1, Vdt2, Vdt3 and Vdt4 applied in the first horizontal period. Further, voltages of the ninth, tenth, eleventh and twelfth light emitting elements LED9, LED10, LED11 and LED12 detected in the second horizontal period are voltages determined based on the data voltages of the previous frame period.

**[0126]** A maximum voltage Vmax among the voltages detected from the first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth light emitting elements LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11 and LED12 in the second horizontal period is applied to the power supply unit 140 through the feedback line FL. In an embodiment of the present invention, the maximum voltage Vmax detected in the second horizontal period may be different from the maximum voltage Vmax detected in the first horizontal period, depending on the voltages of the fifth, sixth, seventh and eighth light emitting elements LED5, LED6, LED7 and LED8.

**[0127]** The power supply unit 140 corrects the high electric potential driving voltage ELVDD based on the maximum voltage Vmax detected in the second horizontal period.

**[0128]** Next, as illustrated in FIG. 7C, a third scan signal SC3 is applied to a third scan line SL3 in a third horizontal period. Then, the ninth, tenth, eleventh and twelfth pixels PX9, PX10, PX11 and PX12 connected to the third scan line SL3 are activated.

**[0129]** In an embodiment of the present invention, the activated ninth pixel PX9 receives a ninth data voltage Vdt9 through the first data line DL1 connected thereto, the activated tenth pixel PX10 receives a tenth data voltage Vdt10 through the second data line DL2 connected thereto, the activated eleventh pixel PX11 receives an eleventh data voltage Vdt11 through the third data line DL3 connected thereto, and the activated twelfth pixel PX12 receives a twelfth data voltage Vdt12 through the fourth data line DL4 connected thereto.

**[0130]** In an embodiment of the present invention, the ninth data voltage Vdt9 is applied to a gate electrode of a ninth driving switching element Tdr9, the tenth data voltage Vdt10 is applied to a gate electrode of a tenth driving switching element Tdr10, the eleventh data voltage Vdt11 is applied to a gate electrode of an eleventh driving switching element Tdr11, and the twelfth data voltage Vdt12 is applied to a gate electrode of a twelfth driving switching element Tdr12. Accordingly, the ninth, tenth, eleventh and twelfth driving switching elements Tdr9, Tdr10, Tdr11 and Tdr12 are turned on. Further, the ninth, tenth, eleventh and twelfth light emitting elements LED9, LED10, LED11 and LED12 emit light by the turned on

ninth, tenth, eleventh and twelfth driving switching elements Tdr9, Tdr10, Tdr11 and Tdr12.

**[0131]** In an embodiment of the present invention, a voltage of the ninth light emitting element LED9 is determined based on the ninth data voltage Vdt9 applied to the gate electrode of the ninth driving switching element Tdr9, a voltage of the tenth light emitting element LED10 is determined based on the tenth data voltage Vdt10 applied to the gate electrode of the tenth driving switching element Tdr10, a voltage of the eleventh light emitting element LED11 is determined based on the eleventh data voltage Vdt11 applied to the gate electrode of the eleventh driving switching element Tdr11, and a voltage of the twelfth light emitting element LED12 is determined based on the twelfth data voltage Vdt12 applied to the gate electrode of the twelfth driving switching element Tdr12. The respective voltages of the ninth, tenth, eleventh and twelfth light emitting elements LED9, LED10, LED11 and LED12 are maintained for one frame period.

**[0132]** During the third horizontal period, the voltage of the ninth light emitting element LED9 is detected through the ninth diode-type element D9, the voltage of the tenth light emitting element LED10 is detected through the tenth diode-type element D10, the voltage of the eleventh light emitting element LED 11 is detected through the eleventh diode-type element D11, and the voltage of the twelfth light emitting element LED12 is detected through the twelfth diode-type element D12.

**[0133]** In an embodiment of the present invention, during the third horizontal period, voltages of the first, second, third, fourth, fifth, sixth, seventh and eighth light emitting elements LED1, LED2, LED3, LED4, LED5, LED6, LED7 and LED8 are detected from the first, second, third, fourth, fifth, sixth, seventh and eighth pixels PX1, PX2, PX3, PX4, PX5, PX6, PX7 and PX8 that are in the inactive state. The voltages of the first, second, third, fourth, fifth, sixth, seventh and eighth light emitting elements LED1, LED2, LED3, LED4, LED5, LED6, LED7 and LED8 are respectively detected through the first, second, third, fourth, fifth, sixth, seventh and eighth diode-type elements D1, D2, D3, D4, D5, D6, D7 and D8. In an embodiment of the present invention, during the third horizontal period, the first, second, third and fourth pixels PX1, PX2, PX3 and PX4 in the inactive state respectively maintain the first, second, third and fourth data voltages Vdt1, Vdt2, Vdt3 and Vdt4 applied in the first horizontal period, and the fifth, sixth, seventh and eighth pixels PX5, PX6, PX7 and PX8 respectively maintain the fifth, sixth, seventh and eighth data voltages Vdt5, Vdt6, Vdt7 and Vdt8 applied in the second horizontal period. Accordingly, voltages of the first, second, third and fourth light emitting elements LED1, LED2, LED3 and LED4 detected in the third horizontal period are voltages determined based on the first, second, third and fourth data voltages Vdt1, Vdt2, Vdt3 and Vdt4 applied in the first horizontal period. Further, voltages of the fifth, sixth, seventh and eighth light emitting elements LED5, LED6, LED7 and LED8 detected in the third horizontal period are voltages de-

terminated based on the fifth, sixth, seventh and eighth data voltages Vdt5, Vdt6, Vdt7 and Vdt8 applied in the second horizontal period.

**[0134]** A maximum voltage Vmax among the voltages detected from the first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth light emitting elements LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11 and LED12 in the third horizontal period is applied to the power supply unit 140 through the feedback line FL. In an embodiment of the present invention, the maximum voltage Vmax detected in the third horizontal period may be different from the maximum voltage Vmax detected in the second horizontal period, depending on the voltages of the ninth, tenth, eleventh and twelfth light emitting elements LED9, LED10, LED11 and LED12. In addition, the maximum voltage Vmax detected in the third horizontal period may be different from the maximum voltage Vmax detected in the second horizontal period.

**[0135]** The power supply unit 140 corrects the high electric potential driving voltage ELVDD based on the maximum voltage Vmax detected in the third horizontal period.

**[0136]** As such, the maximum voltage Vmax is detected from the light emitting elements (for example, light emitting elements LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11 and LED12) of all of the pixels (for example, pixels PX1, PX2, PX3, PX4, PX5, PX6, PX7, PX8, PX9, PX10, PX11 and PX12) of a display panel 110 in each horizontal period, and the level of the high electric potential driving voltage ELVDD is optimized in each horizontal period based on the maximum voltage Vmax. Accordingly, power consumption of the display device may be reduced.

**[0137]** In an embodiment of the present invention, each horizontal period includes a data enable period and a blank period. During the data enable period, data voltages of one horizontal line are input to the data lines. During the blank period in each horizontal period, the voltage (the maximum voltage Vmax) of the feedback line FL is discharged by the low electric potential driving voltage ELVSS. Accordingly, the voltage of the feedback line FL may be maintained at 0 V after the maximum voltage Vmax is detected and before a succeeding horizontal period starts.

**[0138]** FIG. 8 is an explanatory view illustrating a method of correcting the high electric potential driving voltage ELVDD based on the maximum voltage Vmax of light emitting elements detected from first, second, third and fourth pixels PX1, PX2, PX3 and PX4 according to an embodiment of the present invention and power consumption reducing effects according to the method.

**[0139]** Herein, it is assumed that the display panel 110 includes four pixels PX in total as illustrated in FIG. 8.

**[0140]** In the case where, in a predetermined horizontal period, a voltage of a first light emitting element LED1 included in the first pixel PX1 is 13 V, a voltage of a second light emitting element LED2 included in the second pixel

PX2 is 14 V, a voltage of a third light emitting element LED3 included in the third pixel PX3 is 15 V, and a voltage of a fourth light emitting element LED4 included in the fourth pixel PX4 is 16 V, a maximum voltage Vmax among the voltages of the first, second, third and fourth light emitting elements LED1, LED2, LED3 and LED4 is 16 V. The maximum voltage Vmax of 16 V is applied to the power supply unit 140 through the feedback line FL.

**[0141]** Then, the power supply unit 140 sets a high electric potential driving voltage ELVDD based on the above Mathematical Formula 1. For example, when a low electric potential driving voltage ELVSS is a DC voltage of 0 V and a minimum drain-source voltage Vds.min of a fourth driving switching element Tdr4 at a gray level corresponding to the detected maximum voltage Vmax of 16 V is 7 V, the power supply unit 140 sets a sum (23 V) of the maximum voltage (Vmax: 16 V) and the minimum drain-source voltage Vds.min (7 V) as a value of the high electric potential driving voltage ELVDD in the predetermined horizontal period.

**[0142]** In the case where an initial high electric potential driving voltage ELVDD before correction is 28 V, a difference between the initial high electric potential driving voltage ELVDD (28 V) and the high electric potential driving voltage ELVDD (23 V) corrected in the predetermined horizontal period is 5 V. In other words, in the above predetermined horizontal period, the high electric potential driving voltage ELVDD is reduced from 28 V to 23 V. Accordingly, power consumption of the display device may be improved by about 18% in the above predetermined horizontal period.

**[0143]** In an embodiment of the present invention, as the high electric potential driving voltage ELVDD is reduced to 23 V in the above predetermined horizontal period, the drain-source voltages of respective driving switching elements Tdr1, Tdr2, Tdr3 and Tdr4 also change. The respective drain-source voltages of the driving switching elements Tdr1, Tdr2, Tdr3 and Tdr4 are determined based on the following Mathematical Formula 2.

<Mathematical Formula 2>

$$VDS = ELVDD - VOLED$$

**[0144]** In Mathematical Formula 2, VDS denotes a drain-source voltage of a driving switching element, and VOLED denotes a voltage of a light emitting element LED.

**[0145]** As illustrated in FIG. 8, in the case where the corrected high electric potential driving voltage ELVDD is 23 V and the voltage of the first light emitting element LED1 is 13 V, the drain-source voltage of the first driving switching element Tdr1 is determined to be 10 V (23 V - 13 V). In addition, a drain-source voltage of the second driving switching element Tdr2 is determined to be 9 V (23 V - 14 V), a drain-source voltage of the third driving

switching element Tdr3 is determined to be 8 V (23 V - 15 V), and a drain-source voltage of the fourth driving switching element Tdr4 is determined to be 7 V (23 V - 16 V).

**[0146]** Referring to the drain-source voltages of the first, second, third and fourth driving switching elements Tdr1, Tdr2, Tdr3 and Tdr4, it can be seen that the fourth driving switching element Tdr4 of the fourth pixel PX4, which provides the maximum voltage Vmax in the above predetermined horizontal period, is set to have the aforementioned minimum drain-source voltage (Vds.min: 7 V).

**[0147]** FIG. 9 is a graph illustrating a characteristic curve of a transistor and a characteristic curve of a light emitting element LED associated with a variation amount of the high electric potential driving voltage ELVDD of FIG. 8 according to an embodiment of the present invention.

**[0148]** In FIG. 9, each of transistor characteristic curves TC1, TC2, TC3, and TC4 is a transistor characteristic curve illustrating a variation of a drain-source current of a driving switching element according to a drain-source voltage thereof with respect to a gate-source voltage thereof.

**[0149]** For example, in the case where a difference voltage between a gate electrode and a source electrode of the first driving switching element Tdr1 has a level corresponding to a first gate-source voltage VGS1, the first transistor characteristic curve TC1 shows a variation of a drain-source current of the first driving switching element Tdr1 in accordance with a drain-source voltage of the first driving switching element Tdr1. In the case where a difference voltage between a gate electrode and a source electrode of the second driving switching element Tdr2 has a level corresponding to a second gate-source voltage VGS2, the second transistor characteristic curve TC2 shows a variation of a drain-source current of the second driving switching element Tdr2 in accordance with a drain-source voltage of the second driving switching element Tdr2. In the case where a difference voltage between a gate electrode and a source electrode of the third driving switching element Tdr3 has a level corresponding to a third gate-source voltage VGS3, the third transistor characteristic curve TC3 shows a variation of a drain-source current of the third driving switching element Tdr3 in accordance with a drain-source voltage of the third driving switching element Tdr3. Further, in the case where a difference voltage between a gate electrode and a source electrode of the fourth driving switching element Tdr4 has a level corresponding to a fourth gate-source voltage VGS4, the fourth transistor characteristic curve TC4 shows a variation of a drain-source current of the fourth driving switching element Tdr4 in accordance with a drain-source voltage of the fourth driving switching element Tdr4.

**[0150]** In an embodiment of the present invention, the gate-source voltage varies in accordance with a level (e.g., a gray level) of a data voltage. Accordingly, in FIG. 9, the first transistor characteristic curve TC1 corre-

sponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a first gray level, the second transistor characteristic curve TC2 corresponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a second gray level, the third transistor characteristic curve TC3 corresponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a third gray level, and the fourth transistor characteristic curve TC4 corresponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a fourth gray level.

**[0151]** The drain-source voltage in each transistor characteristic curve is a drain-source voltage of the corresponding driving switching element in a saturation region.

**[0152]** The first gate-source voltage VGS1 of the first transistor characteristic curve TC1 corresponds to a first gray level, the second gate-source voltage VGS2 of the second transistor characteristic curve TC2 corresponds to a second gray level, the third gate-source voltage VGS3 of the third transistor characteristic curve TC3 corresponds to a third gray level, and the fourth gate-source voltage VGS4 of the fourth transistor characteristic curve TC4 corresponds to a fourth gray level

**[0153]** Among the first, second, third and fourth gray levels, the first gray level is the lowest, and the fourth gray level is the highest. The second gray level is higher than the first gray level, the third gray level is higher than the second gray level, and the fourth gray level is higher than the third gray level. In an embodiment of the present invention, the fourth gray level is a gray level corresponding to a maximum voltage Vmax that has a highest voltage level among voltages of light emitting elements detected during a predetermined horizontal period. In other words, the fourth gray level corresponds to a luminance Lmax of a light generated from the fourth light emitting element LED4 that provides the maximum voltage Vmax among the four light emitting elements LED1, LED2, LED3 and LED4 in the predetermined horizontal period. The luminance of the light is the highest among luminances of lights respectively generated from the four light emitting elements LED1, LED2, LED3 and LED4 in the predetermined horizontal period.

**[0154]** In FIG. 9, EC1 and EC2 denote characteristic curves of a light emitting element LED illustrating a voltage variation of the light emitting element LED depending on the gray level.

**[0155]** As the high electric potential driving voltage ELVDD of 28 V is corrected to the high electric potential driving voltage ELVDD' of 23 V as described in reference to FIG. 8, a first light emitting element characteristic curve EC1 moves to the left as illustrated in FIG. 9. In other words, the first light emitting element characteristic curve EC1 is corrected to a second light emitting element characteristic curve EC2.

**[0156]** In an embodiment of the present invention, the

first light emitting element characteristic curve EC1 is corrected based on the minimum drain-source voltage  $V_{ds.min}$  of the fourth driving switching element Tdr4. For example, the minimum drain-source voltage  $V_{ds.min}$  in the predetermined horizontal period is 7 V, and the minimum drain-source voltage  $V_{ds.min}$  is at a boundary between a saturation region and a linear region of the driving switching element.

**[0157]** FIG. 10 is an explanatory view illustrating a method of correcting the high electric potential driving voltage ELVDD based on the maximum voltage  $V_{max}$  of a light emitting element detected from the first, second, third and fourth pixels according to an embodiment of the present invention and power consumption reducing effects according to the method.

**[0158]** As illustrated in FIG. 10, it is assumed that the display panel 110 includes four pixels PX1, PX2, PX3 and PX4 in total.

**[0159]** In the case where, in a predetermined horizontal period, a voltage of a first light emitting element LED1 included in the first pixel PX1 is 10 V, a voltage of the second light emitting element LED2 included in the second pixel PX2 is 11 V, a voltage of the third light emitting element LED3 included in the third pixel PX3 is 12 V, and a voltage of the fourth light emitting element LED4 included in the fourth pixel PX4 is 13 V, a maximum voltage  $V_{max}$  among the voltages of the first, second, third and fourth light emitting elements LED1, LED2, LED3 and LED4 is 13 V. The maximum voltage  $V_{max}$  of 13 V is applied to the power supply unit 140 through the feedback line FL.

**[0160]** Then, the power supply unit 140 sets a high electric potential driving voltage ELVDD based on the above Mathematical Formula 1. For example, when a low electric potential driving voltage ELVSS is a DC voltage of 0 V and a minimum drain-source voltage  $V_{ds.min}$  of a fourth driving switching element Tdr4 at a gray level corresponding to the detected maximum voltage  $V_{max}$  of 13 V is 7 V, the power supply unit 140 sets a sum (20 V) of the maximum voltage ( $V_{max}$ : 13 V) and the minimum drain-source voltage  $V_{ds.min}$  (7 V) as a value of the high electric potential driving voltage ELVDD in the predetermined horizontal period.

**[0161]** In the case where an initial high electric potential driving voltage ELVDD before correction is 28 V, a difference between the initial high electric potential driving voltage ELVDD (28 V) and the high electric potential driving voltage ELVDD (20V) corrected in the predetermined horizontal period is 8 V. In other words, in the above predetermined horizontal period, the high electric potential driving voltage ELVDD is reduced from 28 V to 20 V. Accordingly, power consumption of the display device may be improved by about 28% in the above predetermined horizontal period.

**[0162]** In an embodiment of the present invention, as the high electric potential driving voltage ELVDD is reduced to 20 V in the above predetermined horizontal period, the drain-source voltages of respective driving

switching elements Tdr1, Tdr2, Tdr3 and Tdr4 also change. The respective drain-source voltages of the driving switching elements Tdr1, Tdr2, Tdr3 and Tdr4 are determined based on the above Mathematical Formula 2.

**[0163]** As illustrated in FIG. 10, in the case where the corrected high electric potential driving voltage ELVDD is 20 V and the voltage of the first light emitting element LED1 is 10 V, the drain-source voltage of the first driving switching element Tdr1 is 10 V (20 V - 10 V). In this way, a drain-source voltage of the second driving switching element Tdr2 is 9 V (20 V - 11 V), a drain-source voltage of the third driving switching element Tdr3 is 8 V (20 V - 12 V), and a drain-source voltage of the fourth driving switching element Tdr4 is 7 V (20 V - 13 V).

**[0164]** Referring to the drain-source voltages of the first, second, third and fourth driving switching elements Tdr1, Tdr2, Tdr3 and Tdr4, the fourth driving switching element Tdr4 of the fourth pixel PX4, which provides the maximum voltage  $V_{max}$  in the above predetermined horizontal period, is set as the aforementioned minimum drain-source voltage ( $V_{ds.min}$ : 7 V).

**[0165]** FIG. 11 is a graph illustrating a characteristic curve of a transistor and a characteristic curve of a light emitting element LED associated with a variation amount of the high electric potential driving voltage ELVDD of FIG. 10 according to an embodiment of the present invention.

**[0166]** In FIG. 11, each of transistor characteristic curves TC1, TC2, TC3, and TC4 is a transistor characteristic curve illustrating a variation of a drain-source current of a driving switching element according to a drain-source voltage thereof with respect to a gate-source voltage thereof.

**[0167]** For example, in the case where a difference voltage between a gate electrode and a source electrode of the first driving switching element Tdr1 has a level corresponding to a first gate-source voltage VGS1, the first transistor characteristic curve TC1 shows a variation of a drain-source current of the first driving switching element Tdr1 in accordance with a drain-source voltage of the first driving switching element Tdr1. In the case where a difference voltage between a gate electrode and a source electrode of the second driving switching element Tdr2 has a level corresponding to a second gate-source voltage VGS2, the second transistor characteristic curve TC2 shows a variation of a drain-source current of the second driving switching element Tdr2 in accordance with a drain-source voltage of the second driving switching element Tdr2. In the case where a difference voltage between a gate electrode and a source electrode of the third driving switching element Tdr3 has a level corresponding to a third gate-source voltage VGS3, the third transistor characteristic curve TC3 shows a variation of a drain-source current of the third driving switching element Tdr3 in accordance with a drain-source voltage of the third driving switching element Tdr3. Further, in the case where a difference voltage between a gate electrode and a source electrode of the fourth driving switch-

ing element Tdr4 has a level corresponding to a fourth gate-source voltage VGS4, the fourth transistor characteristic curve TC4 shows a variation of a drain-source current of the fourth driving switching element Tdr4 in accordance with a drain-source voltage of the fourth driving switching element Tdr4.

**[0168]** In an embodiment of the present invention, the gate-source voltage varies in accordance with a level (e.g., a gray level) of a data voltage. Accordingly, in FIG. 11, the first transistor characteristic curve TC1 corresponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a first gray level, the second transistor characteristic curve TC2 corresponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a second gray level, the third transistor characteristic curve TC3 corresponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a third gray level, and the fourth transistor characteristic curve TC4 corresponds to a drain-source voltage of a driving switching element used to generate a driving current IDS corresponding to a fourth gray level.

**[0169]** The drain-source voltage in each transistor characteristic curve refers to a drain-source voltage of the corresponding driving switching element in a saturation region.

**[0170]** The first gate-source voltage VGS1 of the first transistor characteristic curve TC1 corresponds to a first gray level, the second gate-source voltage VGS2 of the second transistor characteristic curve TC2 corresponds to a second gray level, the third gate-source voltage VGS3 of the third transistor characteristic curve TC3 corresponds to a third gray level, and the fourth gate-source voltage VGS4 of the fourth transistor characteristic curve TC4 corresponds to a fourth gray level

**[0171]** Among the first, second, third and fourth gray levels, the first gray level is the lowest, and the fourth gray level is the highest. The second gray level is higher than the first gray level, the third gray level is higher than the second gray level, and the fourth gray level is higher than the third gray level. In an embodiment of the present invention, the fourth gray level is a gray level corresponding to a maximum voltage Vmax that has a highest voltage level among voltages of light emitting elements detected during a predetermined horizontal period. In other words, the fourth gray level corresponds to a luminance Lmax of a light generated from the fourth light emitting element LED4 that provides the maximum voltage Vmax among the four light emitting elements LED1, LED2, LED3 and LED4 in the predetermined horizontal period. The luminance of the light is the highest among luminances of lights respectively generated from the four light emitting elements LED1, LED2, LED3 and LED4 in the predetermined horizontal period.

**[0172]** In FIG. 11, EC1 and EC2 denote characteristic curves of a light emitting element LED illustrating a voltage variation of the light emitting element LED depending

on the gray level.

**[0173]** As the high electric potential driving voltage ELVDD of 28 V is corrected to the high electric potential driving voltage ELVDD' of 20 V as in FIG. 10, a first light emitting element characteristic curve EC1 moves to the left as illustrated in FIG. 11. In other words, the first light emitting element characteristic curve EC1 is corrected to a second light emitting element characteristic curve EC2.

**[0174]** In an embodiment of the present invention, the first light emitting element characteristic curve EC1 is corrected based on the minimum drain-source voltage Vds.min of the fourth driving switching element Tdr4. For example, the minimum drain-source voltage Vds.min in the predetermined horizontal period is 7 V, and the minimum drain-source voltage Vds.min is at a boundary between a saturation region and a linear region of the fourth driving switching element Tdr4.

**[0175]** FIG. 12 is a detailed view illustrating the plurality of pixels PX and the maximum voltage detection unit 150 of FIG. 1 according to an embodiment of the present invention, and FIG. 13 is an explanatory view illustrating the relationship among first and second maximum voltage detection units 151 and 152 and a light emitting element LED of each pixel PX of FIG. 12 according to an embodiment of the present invention.

**[0176]** A display panel 110 may include at least two display areas. For example, as illustrated in FIG. 12, the display panel 110 may include a first display area 111 and a second display area 112.

**[0177]** A plurality of first pixels PX1 are located in the first display area 111 and a plurality of second pixels PX2 are located in the second display area 112.

**[0178]** The first pixels PX1 may include at least one of a red pixel, a green pixel, a blue pixel, and a white pixel. The second pixels PX2 may include at least one of a red pixel, a green pixel, a blue pixel, and a white pixel. The red pixel includes a red light emitting element, the green pixel includes a green light emitting element, the blue pixel includes a blue light emitting element, and the white pixel includes a white light emitting element.

**[0179]** A power supply unit 140 may include a first power supply unit 141 and a second power supply unit 142.

**[0180]** The maximum voltage detection unit 150 may include a first maximum voltage detection unit 151 and a second maximum voltage detection unit 152.

**[0181]** The first maximum voltage detection unit 151 detects a greatest voltage among voltages of first light emitting elements LED1 provided in the first pixels PX1 in the first display area 111. To this end, the first maximum voltage detection unit 151 detects a voltage from each of the first light emitting elements LED1 in the respective first pixels PX1, and detects a greatest voltage (hereinafter, "a first maximum voltage Vmax1") that has a highest voltage level among the detected voltages and applies the detected first maximum voltage Vmax1 to the first power supply unit 141.

**[0182]** The first maximum voltage detection unit 151

includes a plurality of first diode-type elements D1 and at least one first resistor R1 as illustrated in FIGS. 12 and 13.

**[0183]** The plurality of first diode-type elements D1 and the first resistor R1 may be located in the first display area 111 of the display panel 110 as illustrated in FIG. 12. For example, the first diode-type elements D1 may be located on the first display area 111, one for each first pixel PX1.

**[0184]** The first diode-type element D1 may be a diode or a diode-type transistor, whose detailed descriptions were made with reference to FIG. 5.

**[0185]** Respective anode electrodes of the first diode-type elements D1 are individually connected to the first light emitting elements LED1 in the first display area 111, respectively.

**[0186]** Respective cathode electrodes of the first diode-type elements D1 are connected in common to a first feedback line FL1, as illustrated in FIGS. 12 and 13. The respective cathode electrodes of the first diode-type elements D1 are connected in common to a feedback input terminal 14 of the first power supply unit 141 through the first feedback line FL1.

**[0187]** The first resistor R1 is connected between the first feedback line FL1 and a low electric potential power line VSL, as illustrated in FIG. 12. The first resistor R1 is connected to the feedback input terminal 14 of the first power supply unit 141 through the first feedback line FL1. In addition, one terminal of the first resistor R1 is connected in common to the respective cathode electrodes of the first diode-type elements D1 through the first feedback line FL1.

**[0188]** The operation of the first maximum voltage detection unit 151 is substantially the same as that of the maximum voltage detection unit 150 described above.

**[0189]** An output voltage of the first power supply unit 141 may include a first high electric potential driving voltage ELVDD1 and a low electric potential driving voltage ELVSS.

**[0190]** The first high electric potential driving voltage ELVDD1 and the low electric potential driving voltage ELVSS output from the first power supply unit 141 are applied to the first display area 111 of the display panel 110. For example, the first high electric potential driving voltage ELVDD1 is applied to the first pixels PX1 of the first display area 111 through a first high electric potential power line VDL1, and the low electric potential driving voltage ELVSS is applied to the first pixels PX1 of the first display area 111 through a low electric potential power line VSL.

**[0191]** The first power supply unit 141 corrects the first high electric potential driving voltage ELVDD1 based on the first maximum voltage Vmax1 applied from the first maximum voltage detection unit 151 and outputs the corrected first high electric potential driving voltage ELVDD1 to the first high electric potential power line VDL1.

**[0192]** The operation of the first power supply unit 141 is substantially the same as that of the power supply unit

140 described above. For example, the first power supply unit 141 corrects the first high electric potential driving voltage ELVDD1 so that a difference voltage between the first high electric potential driving voltage ELVDD1 and the low electric potential driving voltage ELVSS becomes substantially equal to a sum of the first maximum voltage Vmax1 and a minimum drain-source voltage Vds.min of a driving switching element Tdr in the first pixel PX1.

**[0193]** As described above, two adjacent first pixels PX1 between a (2q-1)-th data line and a 2q-th data line among n-th horizontal line pixels PX may have a symmetrical shape with respect to the first high electric potential power line VDL1 passing through the two adjacent first pixels PX1.

**[0194]** The second maximum voltage detection unit 152 detects a greatest voltage among voltages of second light emitting elements LED2 provided in the second pixels PX2 in the second display area 112. For example, the second maximum voltage detection unit 152 detects a voltage from each of the second light emitting elements LED2 in the respective second pixels PX2, and detects a greatest voltage (hereinafter, "a second maximum voltage Vmax2") that has a highest voltage level among the detected voltages and applies the detected second maximum voltage Vmax2 to the second power supply unit 142.

**[0195]** The second maximum voltage detection unit 152 includes a plurality of second diode-type elements D2 and at least one second resistor R2 as illustrated in FIGS. 12 and 13.

**[0196]** The plurality of second diode-type elements D2 and the second resistor R2 may be located in the second display area 112 of the display panel 110 as illustrated in FIG. 12. For example, the second diode-type elements D2 may be located on the second display area 112, one for each second pixel PX2.

**[0197]** The second diode-type element D2 may be a diode or a diode-type transistor, whose detailed descriptions were made with reference to FIG. 5.

**[0198]** Respective anode electrodes of the second diode-type elements D2 are individually connected to the second light emitting elements LED2 in the second display area 112, respectively.

**[0199]** Respective cathode electrodes of the second diode-type elements D2 are connected in common to a second feedback line FL2, as illustrated in FIGS. 12 and 13. The respective cathode electrodes of the second diode-type elements D2 are connected in common to a feedback input terminal 14 of the second power supply unit 142 through the second feedback line FL2.

**[0200]** The second resistor R2 is connected between the second feedback line FL2 and the low electric potential power line VSL, as illustrated in FIG. 12. The second resistor R2 is connected to the feedback input terminal 14 of the second power supply unit 142 through the second feedback line FL2. In addition, one terminal of the second resistor R2 is connected in common to the re-

spective cathode electrodes of the second diode-type elements D2 through the second feedback line FL2.

**[0201]** The operation of the second maximum voltage detection unit 152 is substantially the same as that of the maximum voltage detection unit 150 described above.

**[0202]** An output voltage of the second power supply unit 142 may include a second high electric potential driving voltage ELVDD2 and the low electric potential driving voltage ELVSS.

**[0203]** The second high electric potential driving voltage ELVDD2 and the low electric potential driving voltage ELVSS output from the second power supply unit 142 are applied to the second display area 112 of the display panel 110. For example, the second high electric potential driving voltage ELVDD2 is applied to the second pixels PX2 of the second display area 112 through a second high electric potential power line VDL2, and the low electric potential driving voltage ELVSS is applied to the second pixels PX2 of the second display area 112 through the low electric potential power line VSL.

**[0204]** The second power supply unit 142 corrects the second high electric potential driving voltage ELVDD2 based on the second maximum voltage Vmax2 applied from the second maximum voltage detection unit 152 and outputs the corrected second high electric potential driving voltage ELVDD2 to the second high electric potential power line VDL2.

**[0205]** The operation of the second power supply unit 142 is substantially the same as that of the power supply unit 140 described above. For example, the second power supply unit 142 corrects the second high electric potential driving voltage ELVDD2 so that a difference voltage between the second high electric potential driving voltage ELVDD2 and the low electric potential driving voltage ELVSS becomes substantially equal to a sum of the second maximum voltage Vmax2 and a minimum drain-source voltage Vds.min of a driving switching element Tdr in the second pixel PX2.

**[0206]** As described above, two adjacent second pixels PX2 between the (2q-1)-th data line and the 2q-th data line among the n-th horizontal line pixels PX may have symmetry with respect to the second high electric potential power line VDL2 passing between the two adjacent second pixels PX2.

**[0207]** FIG. 14 is a detailed view illustrating the plurality of pixels PX and the maximum voltage detection unit 150 of FIG. 1 according to an embodiment of the present invention, and FIG. 15 is an explanatory view illustrating the relationship among first, second, third and fourth maximum voltage detection units 151, 152, 153 and 154 and a light emitting element LED of each pixel PX of FIG. 14 according to an embodiment of the present invention.

**[0208]** A display panel 110 of FIG. 14 is substantially the same as the display panel 110 of FIG. 3 described above.

**[0209]** As illustrated in FIGS. 14 and 15, a power supply unit 140 may include a first power supply unit 141, a second power supply unit 142, a third power supply unit 143

and a fourth power supply unit 144 .

**[0210]** The maximum voltage detection unit 150 may include a first maximum voltage detection unit 151, a second maximum voltage detection unit 152, a third maximum voltage detection unit 153, and a fourth maximum voltage detection unit 154.

**[0211]** The first maximum voltage detection unit 151 detects a greatest voltage among respective voltages of red light emitting elements LED1 respectively provided in red pixels PX1 in the display panel 110. To accomplish this, the first maximum voltage detection unit 151 detects a voltage from each of the red light emitting elements LED1 in the respective red pixels PX1, and detects a greatest voltage (hereinafter, "a first maximum voltage Vmax1") that has a highest voltage level among the detected voltages and applies the detected first maximum voltage Vmax1 to the first power supply unit 141.

**[0212]** The first maximum voltage detection unit 151 includes a plurality of first diode-type elements D1 and at least one first resistor R1 as illustrated in FIGS. 14 and 15.

**[0213]** The plurality of first diode-type elements D1 may be located on the display panel 110 as illustrated in FIG. 14. For example, the first diode-type elements D1 may be located on the display panel 110, one for each red pixel PX1. The first resistor R1 may be disposed away from the display panel 110.

**[0214]** The first diode-type element D1 may be a diode or a diode-type transistor, whose detailed descriptions were made reference to FIG. 5.

**[0215]** Respective anode electrodes of the first diode-type elements D1 are individually connected to the red light emitting elements LED1, respectively.

**[0216]** Respective cathode electrodes of the first diode-type elements D1 are connected in common to a first feedback line FL1, as illustrated in FIGS. 14 and 15. The respective cathode electrodes of the first diode-type elements D1 are connected in common to a feedback input terminal 14 of the first power supply unit 141 through the first feedback line FL1.

**[0217]** The first resistor R1 is connected between the first feedback line FL1 and a low electric potential power line VSL, as illustrated in FIGS. 14 and 15. The first resistor R1 is connected to the feedback input terminal 14 of the first power supply unit 141 through the first feedback line FL1. In addition, one terminal of the first resistor R1 is connected in common to the respective cathode electrodes of the first diode-type elements D1 through the first feedback line FL1.

**[0218]** The operation of the first maximum voltage detection unit 151 is substantially the same as that of the maximum voltage detection unit 150 described above.

**[0219]** An output voltage of the first power supply unit 141 may include a first high electric potential driving voltage ELVDD1 and a low electric potential driving voltage ELVSS.

**[0220]** The first high electric potential driving voltage ELVDD1 and the low electric potential driving voltage

ELVSS output from the first power supply unit 141 are applied to the display panel 110. For example, the first high electric potential driving voltage ELVDD1 is applied to the red pixels PX1 of the display panel 110 through a first high electric potential power line VDL1, and the low electric potential driving voltage ELVSS is applied to the red pixels PX1 of the display panel 110 through a low electric potential power line VSL.

**[0221]** The first power supply unit 141 corrects the first high electric potential driving voltage ELVDD1 based on the first maximum voltage Vmax1 applied from the first maximum voltage detection unit 151 and outputs the corrected first high electric potential driving voltage ELVDD1 to the first high electric potential power line VDL1.

**[0222]** The operation of the first power supply unit 141 is substantially the same as that of the power supply unit 140 described above. For example, the first power supply unit 141 corrects the first high electric potential driving voltage ELVDD1 so that a difference voltage between the first high electric potential driving voltage ELVDD1 and the low electric potential driving voltage ELVSS becomes substantially equal to a sum of the first maximum voltage Vmax1 and a minimum drain-source voltage Vds.min of a driving switching element Tdr in the red pixel PX1.

**[0223]** As described above, a red pixel PX1 and a green pixel PX2 adjacent to each other between a (2q-1)-th data line and a 2q-th data line among n-th horizontal line pixels PX may have symmetry with respect to the first high electric potential power line VDL1 between the red pixel PX1 and the green pixel PX2.

**[0224]** The second maximum voltage detection unit 152 detects a greatest voltage among respective voltages of green light emitting elements LED2 respectively provided in green pixels PX2 in the display panel 110. To accomplish this, the second maximum voltage detection unit 152 detects a voltage from each of the green light emitting elements LED2 in the respective green pixels PX2, and detects a greatest voltage (hereinafter, "a second maximum voltage Vmax2") that has a highest voltage level among the detected voltages and applies the detected second maximum voltage Vmax2 to the second power supply unit 142.

**[0225]** The second maximum voltage detection unit 152 includes a plurality of second diode-type elements D2 and at least one second resistor R2 as illustrated in FIGS. 14 and 15.

**[0226]** The plurality of second diode-type elements D2 may be located on the display panel 110 as illustrated in FIG. 14. For example, the second diode-type elements D2 may be located on the display panel 110, one for each green pixel PX2. The second resistor R2 may be disposed away from the display panel 110.

**[0227]** The second diode-type element D2 may be a diode or a diode-type transistor, whose detailed descriptions were made with reference to FIG. 5.

**[0228]** Respective anode electrodes of the second diode-type elements D2 are individually connected to the

green light emitting elements LED2, respectively.

**[0229]** Respective cathode electrodes of the second diode-type elements D2 are connected in common to a second feedback line FL2, as illustrated in FIGS. 14 and 15. The respective cathode electrodes of the second diode-type elements D2 are connected in common to a feedback input terminal 14 of the second power supply unit 142 through the second feedback line FL2.

**[0230]** The second resistor R2 is connected between the second feedback line FL2 and the low electric potential power line VSL, as illustrated in FIGS. 14 and 15. The second resistor R2 is connected to the feedback input terminal 14 of the second power supply unit 142 through the second feedback line FL2. In addition, one terminal of the second resistor R2 is connected in common to the respective cathode electrodes of the second diode-type elements D2 through the second feedback line FL2.

**[0231]** The operation of the second maximum voltage detection unit 152 is substantially the same as that of the maximum voltage detection unit 150 described above.

**[0232]** An output voltage of the second power supply unit 142 may include a second high electric potential driving voltage ELVDD2 and the low electric potential driving voltage ELVSS.

**[0233]** The second high electric potential driving voltage ELVDD2 and the low electric potential driving voltage ELVSS output from the second power supply unit 142 are applied to the display panel 110. For example, the second high electric potential driving voltage ELVDD2 is applied to the green pixels PX2 of the display panel 110 through a second high electric potential power line VDL2, and the low electric potential driving voltage ELVSS is applied to the green pixels PX2 of the display panel 110 through the low electric potential power line VSL.

**[0234]** The second power supply unit 142 corrects the second high electric potential driving voltage ELVDD2 based on the second maximum voltage Vmax2 applied from the second maximum voltage detection unit 152 and outputs the corrected second high electric potential driving voltage ELVDD2 to the second high electric potential power line VDL2.

**[0235]** The operation of the second power supply unit 142 is substantially the same as that of the power supply unit 140 described above. For example, the second power supply unit 142 corrects the second high electric potential driving voltage ELVDD2 so that a difference voltage between the second high electric potential driving voltage ELVDD2 and the low electric potential driving voltage ELVSS becomes substantially equal to a sum of the second maximum voltage Vmax2 and a minimum drain-source voltage Vds.min of a driving switching element Tdr in the green pixel PX2.

**[0236]** As described above, the red pixel PX1 and the green pixel PX2 adjacent to each other between the (2q-1)-th data line and the 2q-th data line among the n-th horizontal line pixels PX may have symmetry with respect to the second high electric potential power line VDL2 between the red pixel PX1 and the green pixel PX2.

**[0237]** The third maximum voltage detection unit 153 detects a greatest voltage among respective voltages of blue light emitting elements LED3 respectively provided in blue pixels PX3 in the display panel 110. To accomplish this, the third maximum voltage detection unit 153 detects a voltage from each of the blue light emitting elements LED3 in the respective blue pixels PX3, and detects a greatest voltage (hereinafter, "a third maximum voltage Vmax3") that has a highest voltage level among the detected voltages and applies the detected third maximum voltage Vmax3 to the third power supply unit 143.

**[0238]** The third maximum voltage detection unit 153 includes a plurality of third diode-type elements D3 and at least one third resistor R3 as illustrated in FIGS. 14 and 15.

**[0239]** The plurality of third diode-type elements D3 may be located on the display panel 110 as illustrated in FIG. 14. For example, the third diode-type elements D3 may be located on the display panel 110, one for each blue pixel PX3. The third resistor R3 may be disposed away from the display panel 110.

**[0240]** The third diode-type element D3 may be a diode or a diode-type transistor, whose detailed descriptions were made with reference to FIG. 5.

**[0241]** Respective anode electrodes of the third diode-type elements D3 are individually connected to the blue light emitting elements LED3, respectively.

**[0242]** Respective cathode electrodes of the third diode-type elements D3 are connected in common to a third feedback line FL3, as illustrated in FIGS. 14 and 15. The respective cathode electrodes of the third diode-type elements D3 are connected in common to a feedback input terminal 14 of the third power supply unit 143 through the third feedback line FL3.

**[0243]** The third resistor R3 is connected between the third feedback line FL3 and the low electric potential power line VSL, as illustrated in FIGS. 14 and 15. The third resistor R3 is connected to the feedback input terminal 14 of the third power supply unit 143 through the third feedback line FL3. In addition, one terminal of the third resistor R3 is connected in common to the respective cathode electrodes of the third diode-type elements D3 through the third feedback line FL3.

**[0244]** The operation of the third maximum voltage detection unit 153 is substantially the same as that of the maximum voltage detection unit 150 described above.

**[0245]** An output voltage of the third power supply unit 143 may include a third high electric potential driving voltage ELVDD3 and the low electric potential driving voltage ELVSS.

**[0246]** The third high electric potential driving voltage ELVDD3 and the low electric potential driving voltage ELVSS output from the third power supply unit 143 are applied to the display panel 110. For example, the third high electric potential driving voltage ELVDD3 is applied to the blue pixels PX3 of the display panel 110 through a third high electric potential power line VDL3, and the low electric potential driving voltage ELVSS is applied to

the blue pixels PX3 of the display panel 110 through the low electric potential power line VSL.

**[0247]** The third power supply unit 143 corrects the third high electric potential driving voltage ELVDD3 based on the third maximum voltage Vmax3 applied from the third maximum voltage detection unit 153 and outputs the corrected third high electric potential driving voltage ELVDD3 to the third high electric potential power line VDL3.

**[0248]** The operation of the third power supply unit 143 is substantially the same as that of the power supply unit 140 described above. For example, the third power supply unit 143 corrects the third high electric potential driving voltage ELVDD3 so that a difference voltage between the third high electric potential driving voltage ELVDD3 and the low electric potential driving voltage ELVSS becomes substantially equal to a sum of the third maximum voltage Vmax3 and a minimum drain-source voltage Vds.min of a driving switching element Tdr in the blue pixel PX3.

**[0249]** As described above, a blue pixel PX3 and a white pixel PX4 adjacent to each other between the (2q-1)-th data line and the 2q-th data line among the n-th horizontal line pixels PX may have symmetry with respect to the third high electric potential power line VDL3 between the blue pixel PX3 and the white pixel PX4.

**[0250]** The fourth maximum voltage detection unit 154 detects a greatest voltage among respective voltages of white light emitting elements LED4 respectively provided in white pixels PX4 in the display panel 110. To accomplish this, the fourth maximum voltage detection unit 154 detects a voltage from each of the white light emitting elements LED4 in the respective white pixels PX4, and detects a greatest voltage (hereinafter, "a fourth maximum voltage Vmax4") that has a highest voltage level among the detected voltages and applies the detected fourth maximum voltage Vmax4 to the fourth power supply unit 144.

**[0251]** The fourth maximum voltage detection unit 154 includes a plurality of fourth diode-type elements D4 and at least one fourth resistor R4 as illustrated in FIGS. 14 and 15.

**[0252]** The plurality of fourth diode-type elements D4 may be located on the display panel 110 as illustrated in FIG. 14. For example, the fourth diode-type elements D4 may be located on the display panel 110, one for each white pixel PX4. The fourth resistor R4 may be disposed away from the display panel 110.

**[0253]** The fourth diode-type element D4 may be a diode or a diode-type transistor, whose detailed descriptions were made with reference to FIG. 5.

**[0254]** Respective anode electrodes of the fourth diode-type elements D4 are individually connected to the white light emitting elements LED4, respectively.

**[0255]** Respective cathode electrodes of the fourth diode-type elements D4 are connected in common to a fourth feedback line FL4, as illustrated in FIGS. 14 and 15. The respective cathode electrodes of the fourth di-

ode-type elements D4 are connected in common to a feedback input terminal 14 of the fourth power supply unit 144 through the fourth feedback line FL4.

**[0256]** The fourth resistor R4 is connected between the fourth feedback line FL4 and the low electric potential power line VSL, as illustrated in FIGS. 14 and 15. The fourth resistor R4 is connected to the feedback input terminal 14 of the fourth power supply unit 144 through the fourth feedback line FL4. In addition, one terminal of the fourth resistor R4 is connected in common to the respective cathode electrodes of the fourth diode-type elements D4 through the fourth feedback line FL4.

**[0257]** The operation of the fourth maximum voltage detection unit 154 is substantially the same as that of the maximum voltage detection unit 150 described above.

**[0258]** An output voltage of the fourth power supply unit 144 may include a fourth high electric potential driving voltage ELVDD4 and the low electric potential driving voltage ELVSS.

**[0259]** The fourth high electric potential driving voltage ELVDD4 and the low electric potential driving voltage ELVSS output from the fourth power supply unit 144 are applied to the display panel 110. For example, the fourth high electric potential driving voltage ELVDD4 is applied to the white pixels PX4 of the display panel 110 through a fourth high electric potential power line VDL4, and the low electric potential driving voltage ELVSS is applied to the white pixels PX4 of the display panel 110 through the low electric potential power line VSL.

**[0260]** The fourth power supply unit 144 corrects the fourth high electric potential driving voltage ELVDD4 based on the fourth maximum voltage  $V_{max4}$  applied from the fourth maximum voltage detection unit 154 and outputs the corrected fourth high electric potential driving voltage ELVDD4 to the fourth high electric potential power line VDL4.

**[0261]** The operation of the fourth power supply unit 144 is substantially the same as that of the power supply unit 140 described above. For example, the fourth power supply unit 144 corrects the fourth high electric potential driving voltage ELVDD4 so that a difference voltage between the fourth high electric potential driving voltage ELVDD4 and the low electric potential driving voltage ELVSS becomes substantially equal to a sum of the fourth maximum voltage  $V_{max4}$  and a minimum drain-source voltage  $V_{ds.min}$  of a driving switching element Tdr in the white pixel PX4.

**[0262]** As described above, the blue pixel PX3 and the white pixel PX4 adjacent to each other between the (2q-1)-th data line and the 2q-th data line among the n-th horizontal line pixels PX may have symmetry with respect to the fourth high electric potential power line VDL4 passing between the blue pixel PX3 and the white pixel PX4.

**[0263]** In an embodiment of the present invention, the red pixel PX1, the green pixel PX2 and the blue pixel PX3 may be connected in common to one high electric potential driving power line and the white pixel PX4 may be connected to another high electric potential driving power

line.

**[0264]** FIG. 16 is a block diagram illustrating a light emitting display device according to an embodiment of the present invention, and FIG. 17 is an explanatory view illustrating the relationship among a maximum voltage detection unit 150, a compensation voltage output unit 700, and a light emitting element LED of each pixel PX in FIG. 16 according to an embodiment of the present invention.

**[0265]** As illustrated in FIG. 16, the display device includes a display panel 110, a timing controller 101, a scan driver 103, a data driver 102, a power supply unit 140, a maximum voltage detection unit 150, and a compensation voltage output unit 700.

**[0266]** The display panel 110, the scan driver 103, the data driver 102, and the maximum voltage detection unit 150 of FIG. 16 are substantially the same as the display panel 110, the scan driver 103, the data driver 102, and the maximum voltage detection unit 150 of FIG. 1, and thus, repetitive descriptions thereof may be omitted.

**[0267]** The timing controller 101 of FIG. 16 performs the following operation in addition to the above-described operation of the timing controller 101 of FIG. 1. For example, the timing controller 101 of FIG. 16 outputs an image data signal having a highest gray level (hereinafter, "a highest gray level image data signal  $G_{max}$ ") among image data signals applied to all of the pixels PX of the display panel 110. In an embodiment of the present invention, the highest gray level image data signal  $G_{max}$  does not always correspond to, for example, a gray level 255, which is a highest gray level among a gray level 0 to a gray level 255. In other words, the highest gray level image data signal  $G_{max}$  refers to an image data signal having a highest gray level among image data signals included in a screen data of one horizontal period. Thus, depending on the configuration of the screen data, an image data signal having a highest gray level in each horizontal period may have one selected from a gray level 0 to a gray level 255.

**[0268]** The aforementioned screen data is different from a frame data. In other words, as in the above descriptions made with reference to FIGS. 7A, 7B and 7C, one screen data in one horizontal period may include image data signals of a previous frame period in addition to image data signals of a current frame period.

**[0269]** The timing controller 101 of FIG. 16 detects the highest gray level image data signal  $G_{max}$  based on the screen data updated on the basis of a horizontal period. The maximum voltage detection unit 150 of FIGS. 1 and 16 detects a maximum voltage  $V_{max}$  based on data voltages of one screen corresponding to the screen data updated on the basis of the horizontal period. Accordingly, the highest gray level image data signal  $G_{max}$  and the maximum voltage  $V_{max}$  detected in a same horizontal period have a substantially same gray level.

**[0270]** However, in a same horizontal period, the gray level of the highest gray level image data signal  $G_{max}$  does not always coincide with a gray level of the maxi-

imum voltage  $V_{max}$ . For example, in the case where a light emitting element of a single pixel among a plurality of pixels PX emits light of a predetermined gray level and the remaining pixels all have a gray level 0, e.g., the remaining pixels are turned off, a feedback line FL may not be charged sufficiently in one horizontal period. In this case, because the feedback line FL is only charged by a driving current generated from the light emitting element of the single pixel, a voltage of the feedback line FL may not reach a target voltage (e.g., the maximum voltage  $V_{max}$ ) in the one horizontal period. In this case, the maximum voltage  $V_{max}$  in the one horizontal period may not coincide with the highest gray level image data signal  $G_{max}$  which is a digital signal corresponding to the maximum voltage  $V_{max}$ . However, since it is a rare case that only one pixel PX is turned on, the highest gray level image data signal  $G_{max}$  and the maximum voltage  $V_{max}$  detected in the same horizontal period may have substantially the same gray level. In other words, a highest gray level image data signal  $G_{max}$  detected in a predetermined horizontal period may be used to identify a gray level of a maximum voltage  $V_{max}$  in the predetermined horizontal period.

**[0271]** As illustrated in FIG. 17, the maximum voltage detection unit 150 of FIG. 16 includes a plurality of diode-type elements D and at least one resistor R. The maximum voltage detection unit 150 of FIG. 17 is substantially the same as the maximum voltage detection unit 150 of FIG. 1 described above. However, the maximum voltage detection unit 150 of FIGS. 16 and 17 provides the maximum voltage  $V_{max}$  generated from the maximum voltage detection unit 150 to the compensation voltage output unit 700 instead of the power supply unit 140. For example, the maximum voltage  $V_{max}$  output from the maximum voltage detection unit 150 is applied to the compensation voltage output unit 700 through the feedback line FL. In addition, the compensation voltage output unit 700 receives a compensation voltage of the feedback line FL through a feedback input terminal thereof.

**[0272]** The compensation voltage output unit 700 stores compensation voltages corresponding to each gray level of the image data signal. For example, in the case where the image data signal has a gray level selected from a gray level 0 to a gray level 255, 256 compensation voltages from the gray level 0 to the gray level 255 are stored in advance in the compensation voltage output unit 700.

**[0273]** The compensation voltage output unit 700 receives the maximum voltage  $V_{max}$  from the maximum voltage detection unit 150 and receives the highest gray level image data signal  $G_{max}$  from the timing controller 101.

**[0274]** The compensation voltage output unit 700 refers to the highest gray level image data signal  $G_{max}$  to identify a gray level of the maximum voltage  $V_{max}$ . In other words, as described above, the highest gray level image data signal  $G_{max}$  and the maximum voltage  $V_{max}$  detected in a same horizontal period have substantially

the same gray level.

**[0275]** The compensation voltage output unit 700 corrects at least one of the compensation voltages based on the maximum voltage  $V_{max}$ . For example, the compensation voltage output unit 700 corrects the compensation voltage corresponding to the highest gray level image data signal  $G_{max}$ .

**[0276]** In addition, the compensation voltage output unit 700 selects a compensation voltage  $V_c$  corresponding to the highest gray level image data signal  $G_{max}$  applied from the timing controller 101 and applies the selected compensation voltage  $V_c$  to the power supply unit 140.

**[0277]** The power supply unit 140 corrects a high electric potential driving voltage ELVDD based on the compensation voltage  $V_c$  provided from the compensation voltage output unit 700 and applies the corrected high electric potential driving voltage ELVDD to a high electric potential power line VDL. For example, as in the above Mathematical Formula 1, the power supply unit 140 corrects the high electric potential driving voltage ELVDD so that a difference voltage between the high electric potential driving voltage ELVDD and a low electric potential driving voltage ELVSS becomes substantially equal to a sum of the compensation voltage  $V_c$  and a minimum drain-source voltage  $V_{ds.min}$  of a driving switching element Tdr.

**[0278]** FIG. 18 is a detailed block diagram illustrating the compensation value output unit 700 of FIG. 16 according to an embodiment of the present invention.

**[0279]** As illustrated in FIG. 18, the compensation voltage output unit 700 may include a compensation voltage selection unit 702 and a compensation voltage update unit 701.

**[0280]** The compensation voltage selection unit 700 stores compensation voltages corresponding to each gray level of the image data signal. For example, in the case where the image data signal has a gray level selected from a gray level 0 to a gray level 255, 256 compensation voltages from the gray level 0 to the gray level 255 are stored in advance in the compensation voltage output unit 700.

**[0281]** The compensation voltage selection unit 702 receives the highest gray level image data signal  $G_{max}$  from the timing controller 101. Since the highest gray level image data signal  $G_{max}$  is output every horizontal period, the compensation voltage selection unit 702 receives the highest gray level image data signal  $G_{max}$  in each horizontal period. The compensation voltage selection unit 702 outputs the compensation voltage  $V_c$  each time the highest gray level image data signal  $G_{max}$  is input. For example, the compensation voltage selection unit 702 selects a compensation voltage  $V_c$  corresponding to the highest gray level image data signal  $G_{max}$  among the compensation voltages stored therein, and applies the selected compensation voltage  $V_c$  to the power supply unit 140.

**[0282]** The compensation voltage selection unit 702

may be a lookup table in which the aforementioned compensation voltages are stored.

**[0283]** The compensation voltage update unit 701 periodically corrects the compensation voltages stored in the compensation voltage selection unit 702. For example, the compensation voltage selection unit 702 may store compensation data reflecting the latest information.

**[0284]** To update the compensation voltage, the compensation voltage update unit 701 receives the maximum voltage  $V_{max}$  from the maximum voltage detection unit 150 and receives the highest gray level image data signal  $G_{max}$  from the timing controller 101. The compensation voltage update unit 701 corrects at least one of the compensation voltages based on the maximum voltage  $V_{max}$ . For example, the compensation voltage update unit 701 corrects a compensation voltage having substantially the same gray level as a gray level of the highest gray level image data signal  $G_{max}$ . To be more specific, in the case where the highest gray level image data signal detected in a predetermined horizontal period is an image data signal of a gray level 100, the compensation voltage update unit 701 selects a compensation voltage of a gray level 100 among the stored 256 compensation voltages (e.g., compensation voltages from a gray level 0 to a gray level 255) and corrects the compensation voltage of a gray level 100. In this case, the compensation voltage update unit 701 may perform the correcting operation by replacing the compensation voltage of a gray level 100 with a maximum voltage  $V_{max}$  detected in the predetermined horizontal period. Accordingly, the compensation voltages stored in the compensation voltage selection unit 702 may have different values as time elapses. In other words, the compensation voltages stored in the compensation voltage selection unit 702 may have different values over time.

**[0285]** In an embodiment of the present invention, the compensation voltage update unit 701 may further correct at least one of other compensation voltages stored in the compensation voltage selection unit 702 based on an amount of change in the compensation voltage corrected based on the maximum voltage  $V_{max}$ . For example, in the case where the compensation voltage of a gray level 100 is changed to the maximum voltage  $V_{max}$  detected in the aforementioned predetermined horizontal period as described above, the compensation voltage update unit 701 calculates an amount of change in the compensation voltage of a gray level 100. In the case where the compensation voltage of a gray level 100 before the correction has a value of about 10 V and the compensation voltage of a gray level 100 after the correction has a value of about 15 V, a voltage variation rate is +50 %. In this case, the compensation voltage update unit 701 may correct at least one of other compensation voltages of other gray levels to a voltage 50 % greater than the at least one of the other compensation voltages.

**[0286]** The compensation voltage update unit 701 may periodically correct the compensation voltages stored in the compensation voltage selection unit 702 at every  $y$ -

th horizontal period, wherein  $y$  is a natural number. To accomplish this, the compensation voltage update unit 701 may include a counter.

**[0287]** The counter counts the highest gray level image data signals  $G_{max}$  input to the compensation voltage update unit 701 in each horizontal period, and generates an output when the number of the counted highest gray level image data signals  $G_{max}$  reaches a preset value " $y$ ." In response to the output from the counter, the compensation voltage update unit 701 performs the above-described correcting operation based on the maximum voltage  $V_{max}$  detected in a horizontal period in which the output is generated.

**[0288]** In an embodiment of the present invention, after the output is generated, the counter is reset and starts counting the highest gray level image data signals  $G_{max}$  from the beginning.

**[0289]** In the case where  $y$  is sufficiently large, the compensation voltage update unit 701 may perform the correcting operation as described above on a frame basis.

**[0290]** As described above, in the case where a voltage of the feedback line FL does not reach a target voltage (e.g., the maximum voltage  $V_{max}$ ) in one horizontal period, the maximum voltage  $V_{max}$  detected by the maximum voltage detection unit 150 in the one horizontal period may not coincide with the maximum voltage  $V_{max}$  in said one horizontal period. This is because the voltage is detected in a state where the feedback line FL is not sufficiently charged to the target voltage (e.g., the maximum voltage  $V_{max}$ ).

**[0291]** The compensation voltage output unit 700 outputs the compensation voltage  $V_c$  based on the gray level of the highest gray level image data signal  $G_{max}$ , and thus, may almost always directly output the maximum voltage  $V_{max}$  (e.g., the compensation voltage  $V_c$ ) having a normal level to the power supply unit 140, regardless of the charging time of the feedback line FL. In other words, since the compensation voltages depending on the gray level of the highest gray level image data signal  $G_{max}$  are stored in advance in the compensation voltage selection unit 702, the compensation voltage output unit 700 may provide the compensation voltage  $V_c$  to the power supply unit 140 according to the highest gray level image data signal  $G_{max}$  applied to the compensation voltage output unit 700 in each horizontal period.

**[0292]** However, since the compensation voltages stored in the compensation voltage selection unit 702 are corrected based on the maximum voltage  $V_{max}$  detected from the feedback line FL, the charging time of the feedback line FL may become long. Accordingly, in the case where substantially all of the pixels receive an image data signal of a gray level 0 as described above, the compensation voltage selection unit 702 does not have to correct the compensation voltages.

**[0293]** For example, in the case where the number of image data signals having a lower gray level than a preset reference gray level among image data signals of all of the pixels PX included in a screen data in each horizontal

period exceeds a preset threshold value, the timing controller 101 further outputs a holding signal HS. The holding signal HS is applied to the compensation voltage update unit 701.

**[0294]** The compensation voltage update unit 701 that receives the holding signal HS does not correct the compensation voltages although the highest gray level image data signal Gmax is input in the corresponding horizontal period. In other words, in response to the holding signal HS, the compensation voltage update unit 701 maintains the compensation voltages of the compensation voltage selection unit 702 to a value before the generation of the highest gray level image data signal Gmax, regardless of the input of the highest gray level image data signal Gmax.

**[0295]** Accordingly, the high electric potential driving voltage ELVDD output from the power supply unit 140 may properly vary in accordance with a level of the maximum voltage Vmax which is almost always correct in each horizontal period.

**[0296]** FIG. 19 is an explanatory view illustrating a time-dependent variation of compensation voltages stored in the compensation voltage selection unit 702 of FIG. 18 according to an embodiment of the present invention.

**[0297]** Each of curves C1, C2 and C3 illustrated in FIG. 19 is a curve representing a level of a compensation voltage depending on a gray level.

**[0298]** Each of the curves C1, C2, and C3 represents the level of 256 compensation voltages from a gray level 0 to a gray level 255. As a gray level of a compensation voltage increases, a voltage level of the compensation voltage increases.

**[0299]** For example, a first curve C1 represents 256 correction voltages that are corrected based on a maximum voltage Vmax detected in an (x-2)-th horizontal period, a second curve C2 represents 256 correction voltages that are corrected based on a maximum voltage Vmax detected in an (x-1)-th horizontal period, and a third curve C3 represents 256 correction voltages that are corrected based on a maximum voltage Vmax detected in an x-th horizontal period, wherein x is natural number greater than 2.

**[0300]** As illustrated in FIG. 19, a level of a compensation voltage of a gray level 255 may be different from one time to another. For example, a compensation voltage of a gray level 255 in the third curve C3 may have a greater value than a value of a compensation voltage of a gray level 255 in the first curve C1.

**[0301]** FIG. 20 is an explanatory view illustrating a variation of a high electric potential driving voltage ELVDD by the compensation value output unit 700 of FIG. 16 according to an embodiment of the present invention.

**[0302]** Each of first and second curves C11 and C22 is a curve showing a variation of a level of the maximum voltage Vmax depending on time, wherein the time refers to a horizontal period. The first and second curves C11 and C22 represent changes in the level of the maximum

voltage Vmax detected in respective horizontal periods. In the graph of FIG. 20, 't' represents time and 'V' represents voltage.

**[0303]** As used herein, a maximum voltage Vmax in the first curve C11 denotes a voltage detected by the maximum voltage detection unit 150, and a maximum voltage Vmax in the second curve C22 denotes a maximum voltage Vmax based on the highest gray level image data signal Gmax.

**[0304]** The third curve C33 is a curve showing a variation of a level of the high electric potential driving voltage ELVDD depending on time, wherein time refers to a horizontal period.

**[0305]** As described above, in the case where a voltage of the feedback line FL does not reach a target voltage (e.g., the maximum voltage Vmax) in one horizontal period, the first curve C11 may not coincide with the second curve C22. This is because the voltage is detected in a state where the feedback line FL is not fully charged to the target voltage (e.g., the maximum voltage Vmax).

**[0306]** Since the compensation voltage output unit 700 outputs a compensation voltage based on a gray level of the highest gray level image data signal Gmax, the compensation voltage output unit 700 may almost always directly output the maximum voltage Vmax (e.g., the compensation voltage Vc) having a substantially correct level to the power supply unit 140, regardless of the charging time of the feedback line FL. Accordingly, as the third curve C33, the high electric potential driving voltage ELVDD from the power supply unit 140 varies in accordance with the second curve C22, not the first curve C11. In other words, the high electric potential driving voltage ELVDD may vary in correspondence with the level of the correct maximum voltage Vmax in each horizontal period.

**[0307]** In an embodiment of the present invention, the light emitting display device generates a high electric potential driving voltage having a substantially minimum voltage level required for driving a display panel. Accordingly, power consumption of the display device may be reduced.

**[0308]** In an embodiment of the present invention, the light emitting display device corrects the high electric potential driving voltage using a voltage detected from a light emitting element. Accordingly, a detection circuit and a correction circuit may have a simple structure. As a result, resource consumption of a system may be also reduced.

**[0309]** In an embodiment of the present invention, the display device corrects the high electric potential driving voltage using a compensation voltage for each corresponding gray level of an image data signal. Accordingly, response speed of the high electric potential driving voltage may be fast.

**[0310]** While the present invention has been particularly shown and described with reference to certain embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and

details may be made therein without departing from the scope of the present invention as defined by the following claims.

## Claims

### 1. A light emitting display device, comprising:

a display panel including a plurality of first pixels, each of the plurality of first pixels comprising a first driving switching element connected to a first power line and a first light emitting element connected to a second power line;

a first maximum voltage detection unit for detecting a voltage from each of the first light emitting elements of each of the first pixels and outputting a first maximum voltage that has a highest voltage level among the detected voltages; and

a first power supply unit for correcting a first driving voltage based on the first maximum voltage and applying the corrected first driving voltage to the first power line.

2. A light emitting display device as claimed in claim 1, wherein the first maximum voltage detection unit comprises a plurality of diode-type elements, a first terminal of each of the plurality of diode-type elements is individually connected to a corresponding one of the first light emitting elements, and a second terminal of each of the plurality of diode-type elements is connected in common to a feedback input terminal of the first power supply unit, the first maximum voltage being applied to the feedback input terminal, and the feedback input terminal is connected to the second power line.

3. A light emitting display device as claimed in claim 2, wherein the first maximum voltage detection unit further comprises a resistor connected between the feedback input terminal and the second power line.

4. A light emitting display device as claimed in claim 2 or 3, wherein at least one of the diode-type elements is a diode or a diode-type transistor.

5. A light emitting display device as claimed in any preceding claim, wherein the first power supply unit is configured to decrease the first driving voltage as the first maximum voltage decreases.

6. A light emitting display device as claimed in claim 1, wherein the first power supply unit is configured to correct the first driving voltage so that a difference voltage between the first driving voltage and a second driving voltage of the second power line is sub-

stantially equal to a sum of the first maximum voltage and a minimum drain-source voltage of the first driving switching element.

7. A light emitting display device as claimed in Claim 1, Wherein the display device further comprises:

a plurality of second pixels disposed in the display panel, each of the plurality of second pixels comprising a second driving switching element connected to a third power line and a second light emitting element connected to the second power line;

a second maximum voltage detection unit for detecting a voltage from each of the second light emitting elements of each of the second pixels and outputting a second maximum voltage that has a highest voltage level among the detected voltages; and

a second power supply unit for correcting a third driving voltage based on the second maximum voltage and applying the corrected third driving voltage to the third power line.

8. A light emitting display device as claimed in claim 7, wherein the first maximum voltage detection unit comprises:

a first resistor connected between a first feedback input terminal of the first power supply unit and the second power line, the first maximum voltage being input to the first feedback input terminal; and

a first diode-type element connected between each one of the first light emitting elements of the first pixels and the first resistor, and a first terminal of each of the first diode-type elements is individually connected to a corresponding one of the first light emitting elements of the first pixels, and a second terminal of each of the first diode-type elements is connected in common to the first feedback input terminal.

9. A light emitting display device as claimed in claim 7 or 8, wherein the second maximum voltage detection unit comprises:

a second resistor connected between a second feedback input terminal of the second power supply unit and the second power line, the second maximum voltage being input to the second feedback input terminal; and

a second diode-type element connected between each one of the second light emitting elements of the second pixels and the second resistor, and

a first terminal of each of the second diode-type elements is individually connected to a corre-

- sponding one of the second light emitting elements of the second pixels, and a second terminal of each of the second diode-type elements is connected in common to the second feedback input terminal.
- 5
10. A light emitting display device as claimed in claim 7, 8 or 9 wherein the first power supply unit is configured to correct the first driving voltage so that a difference voltage between the first driving voltage and a second driving voltage of the second power line is substantially equal to a sum of the first maximum voltage and a minimum drain-source voltage of a first driving switching element, and
- 10
- the second power supply unit is configured to correct the third driving voltage so that a difference voltage between the second driving voltage and the third driving voltage is substantially equal to a sum of the second maximum voltage and a minimum drain-source voltage of a second driving switching element.
- 15
- 20
11. A light emitting display device as claimed in any one of Claims 7 to 10, wherein the first light emitting elements comprise at least one of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.
- 25
12. A light emitting display device as claimed in claim 11, wherein the first light emitting elements comprise at least two of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.
- 30
13. A light emitting display device as claimed in any one of Claims 7 to 10, wherein the second light emitting elements comprise at least one of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.
- 35
- 40
14. A light emitting display device as claimed in claim 13, wherein the second light emitting elements comprise at least two of a red light emitting element, a green light emitting element, a blue light emitting element, and a white light emitting element.
- 45
- 50
15. A light emitting display device, according to one of Claims 7 to 14, wherein the first light emitting element emits a light having a color different from a color of a light emitted from the second light emitting element.
- 55
16. A light emitting display device, comprising:
- a display panel including a plurality of pixels, each of the plurality of pixels comprising a driving switching element connected to a first power line and a light emitting element connected to a
- second power line;
- a maximum voltage detection unit for detecting a voltage from each of the light emitting elements of each of the pixels and outputting a maximum voltage that has a highest voltage level among the detected voltages;
- a timing controller for outputting a highest gray level image data signal having a highest gray level among image data signals applied to the plurality of pixels;
- a compensation voltage selection unit for storing compensation voltages corresponding to respective gray levels of a plurality of image data signals and selecting a compensation voltage corresponding to the highest gray level image data signal;
- a compensation voltage update unit for correcting the compensation voltage of the compensation voltage selection unit corresponding to the highest gray level image data signal based on the maximum voltage; and
- a power supply unit is configured to correct the first driving voltage based on the compensation voltage selected by the compensation voltage selection unit and apply the corrected first driving voltage to the first power line.
17. A light emitting display device as claimed in claim 16, wherein the compensation voltage update unit is configured to further correct at least one other compensation voltage stored in the compensation voltage selection unit based on a variation amount of the compensation voltage corrected according to the maximum voltage.
18. A light emitting display device as claimed in claim 16 or 17, wherein, when the number of image data signals having a lower gray level than a reference gray level among the image data signals applied to the plurality of pixels exceeds a threshold value, the timing controller is configured to further generate a holding signal and apply the holding signal to the compensation voltage update unit.
19. A light emitting display device as claimed in claim 18, wherein, in response to the holding signal, the compensation voltage update unit is configured to maintain the compensation voltages of the compensation voltage selection unit to keep values they had before the generation of the highest gray level image data signal, regardless of an input of the highest gray level image data signal.
20. A light emitting display device as claimed in one of Claims 16 to 19, wherein the compensation voltage update unit is configured to correct the compensation voltage once every y-th horizontal period, wherein y is a natural number greater than 2.

21. A light emitting display device as claimed in one of Claims 16 to 20, wherein the maximum voltage detection unit comprises:

- a resistor connected between a feedback input terminal of the compensation voltage update unit and the second power line, the maximum voltage being input to the feedback input terminal; and 5
- a diode-type element connected between each one of the light emitting elements and the resistor, and 10
- a first terminal of each of the diode-type elements is individually connected to a corresponding one of the light emitting elements, and a second terminal of each of the diode-type elements is connected in common to the feedback input terminal. 15

22. A light emitting display device as claimed in one of Claims 16 to 21, wherein the power supply unit is configured to correct the first driving voltage so that a difference voltage between the first driving voltage and a second driving voltage of the second power line is substantially equal to a sum of the selected compensation voltage and a minimum drain-source voltage of a driving switching element. 20 25

23. A light emitting display device as claimed in one of Claims 16 to 22, wherein the compensation voltage selection unit is a look-up table. 30

24. A light emitting display device, comprising:

- a display panel comprising a plurality of pixels, each the plurality of pixels comprising a driving switching element connected to a first power line and a light emitting element connected to a second power line; 35
- a power supply unit for applying a power to the first power line; and 40
- a diode connected between an anode electrode of the light emitting element disposed in at least one pixel and a feedback input terminal of the power supply unit. 45

50

55

FIG. 1

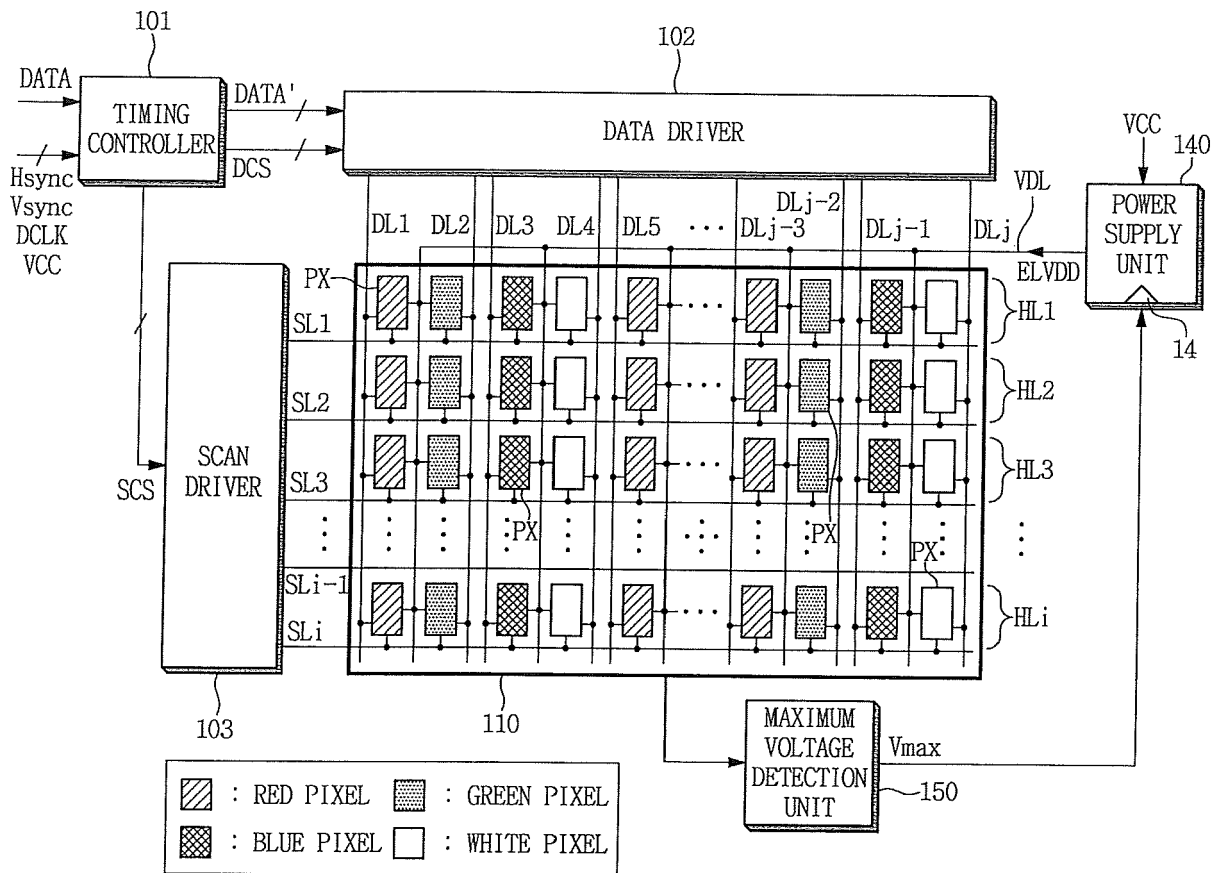
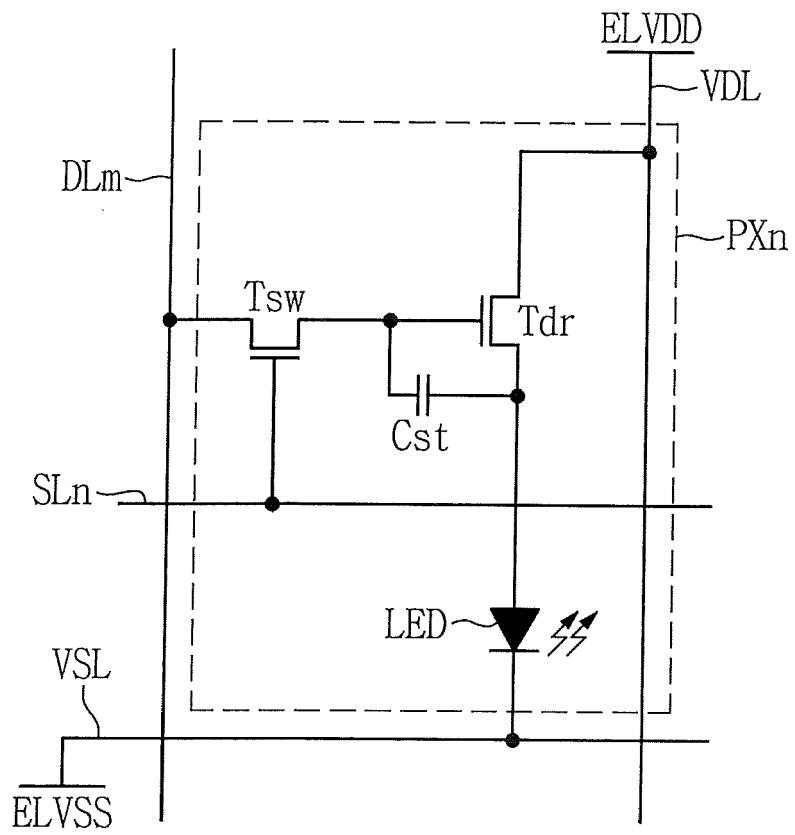


FIG. 2



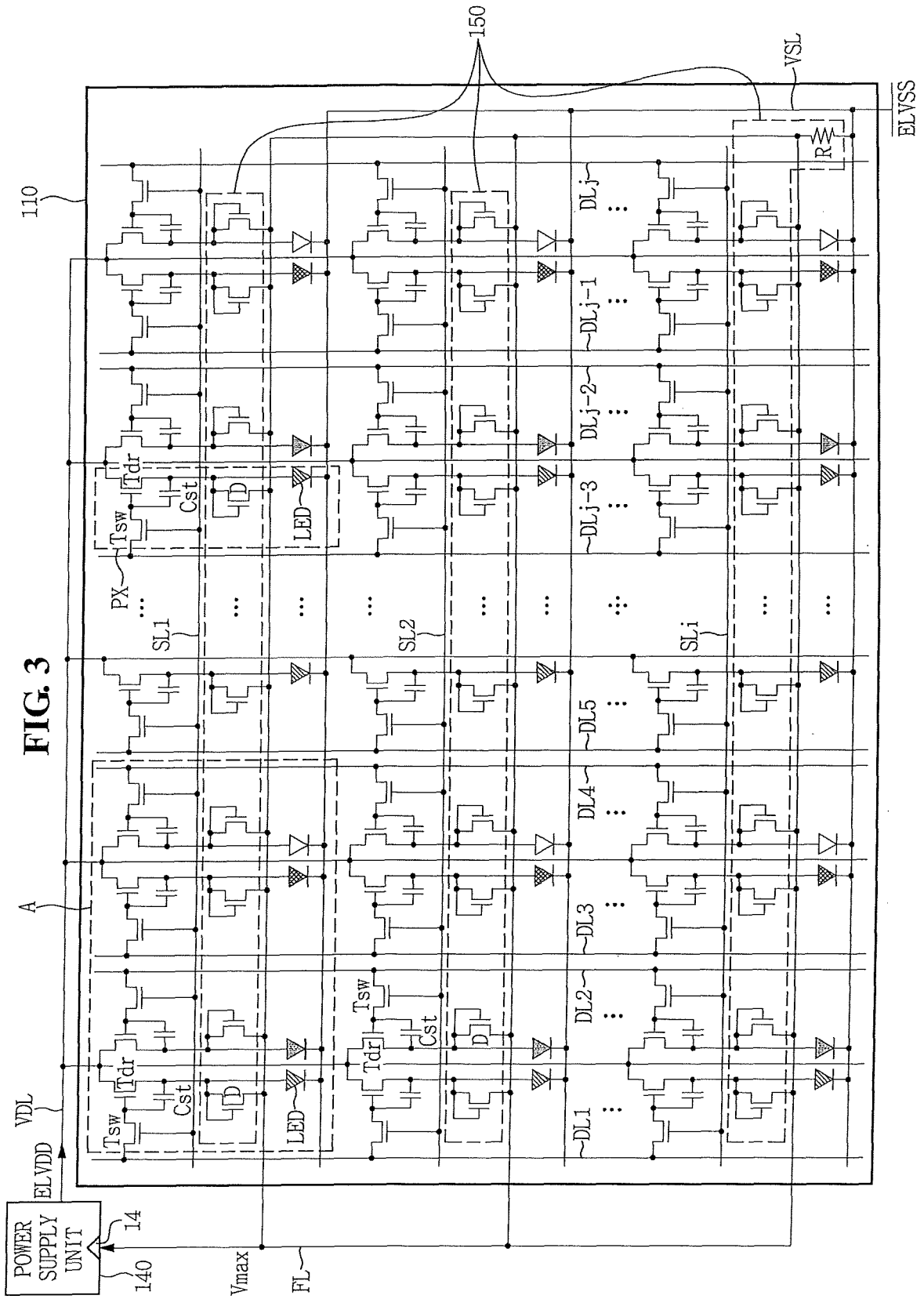


FIG. 4

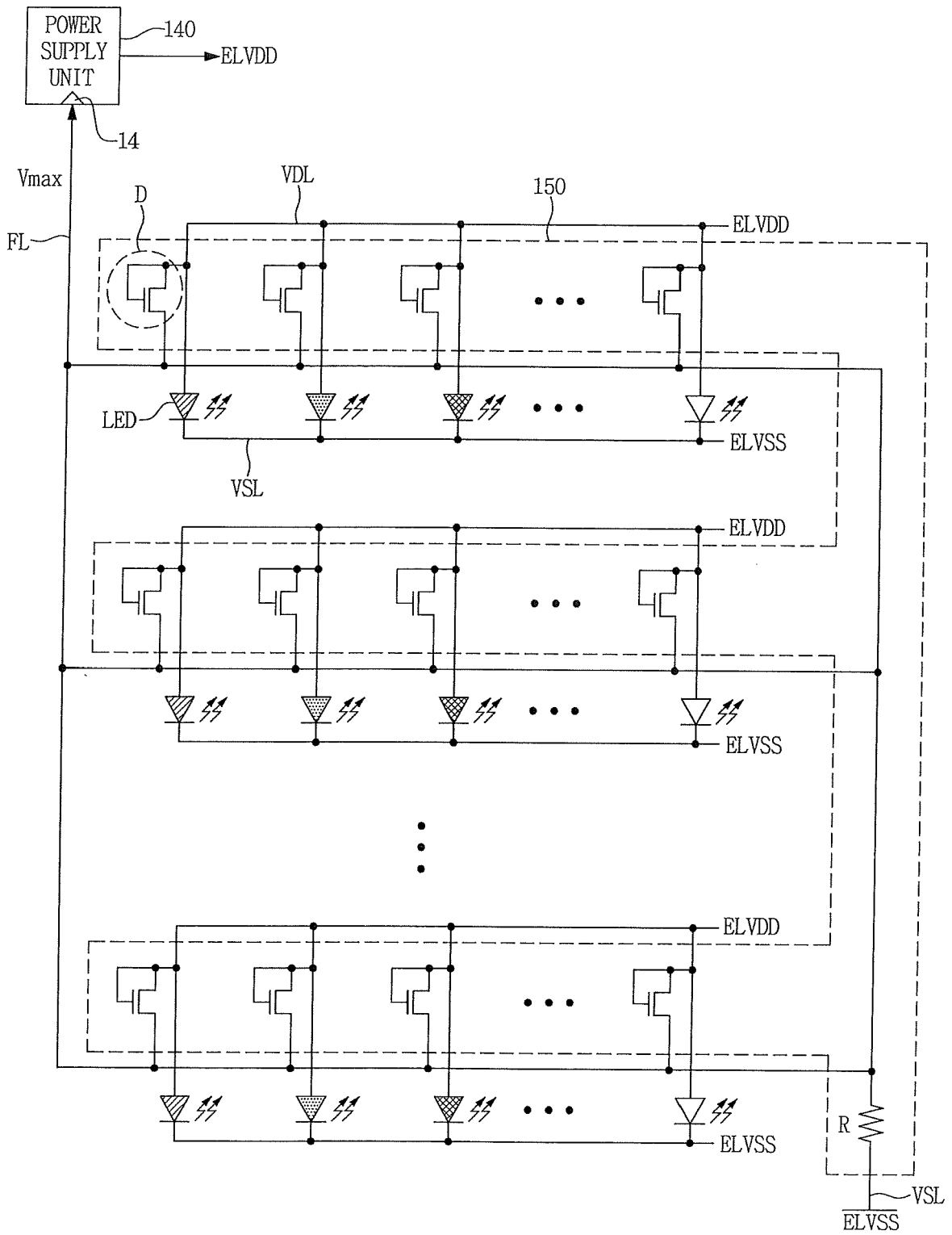




FIG. 6

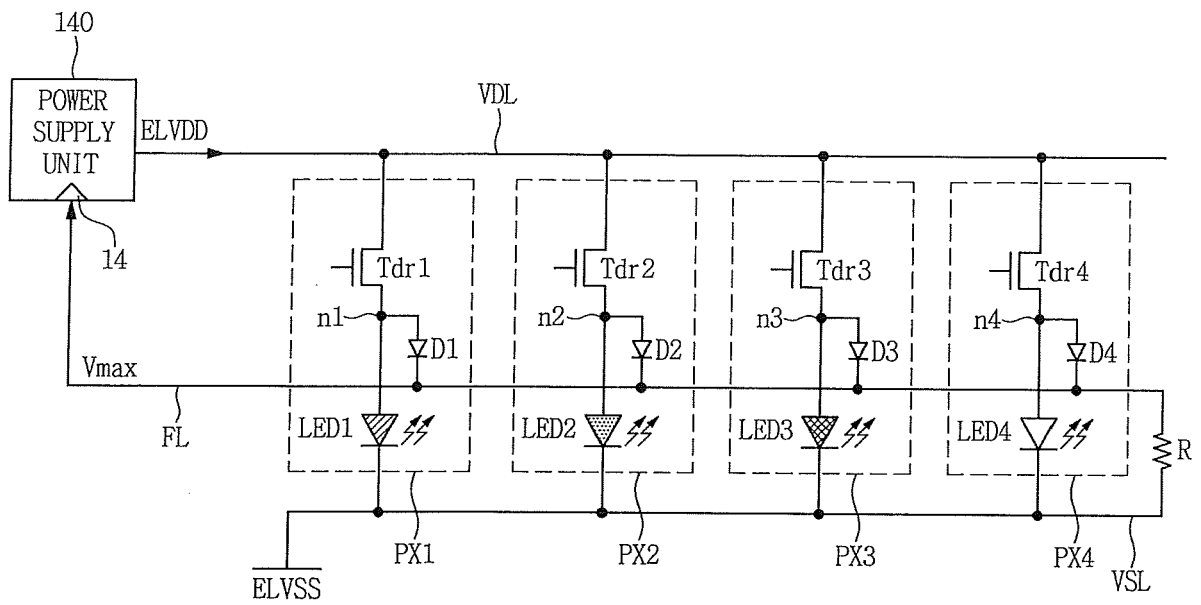


FIG. 7A

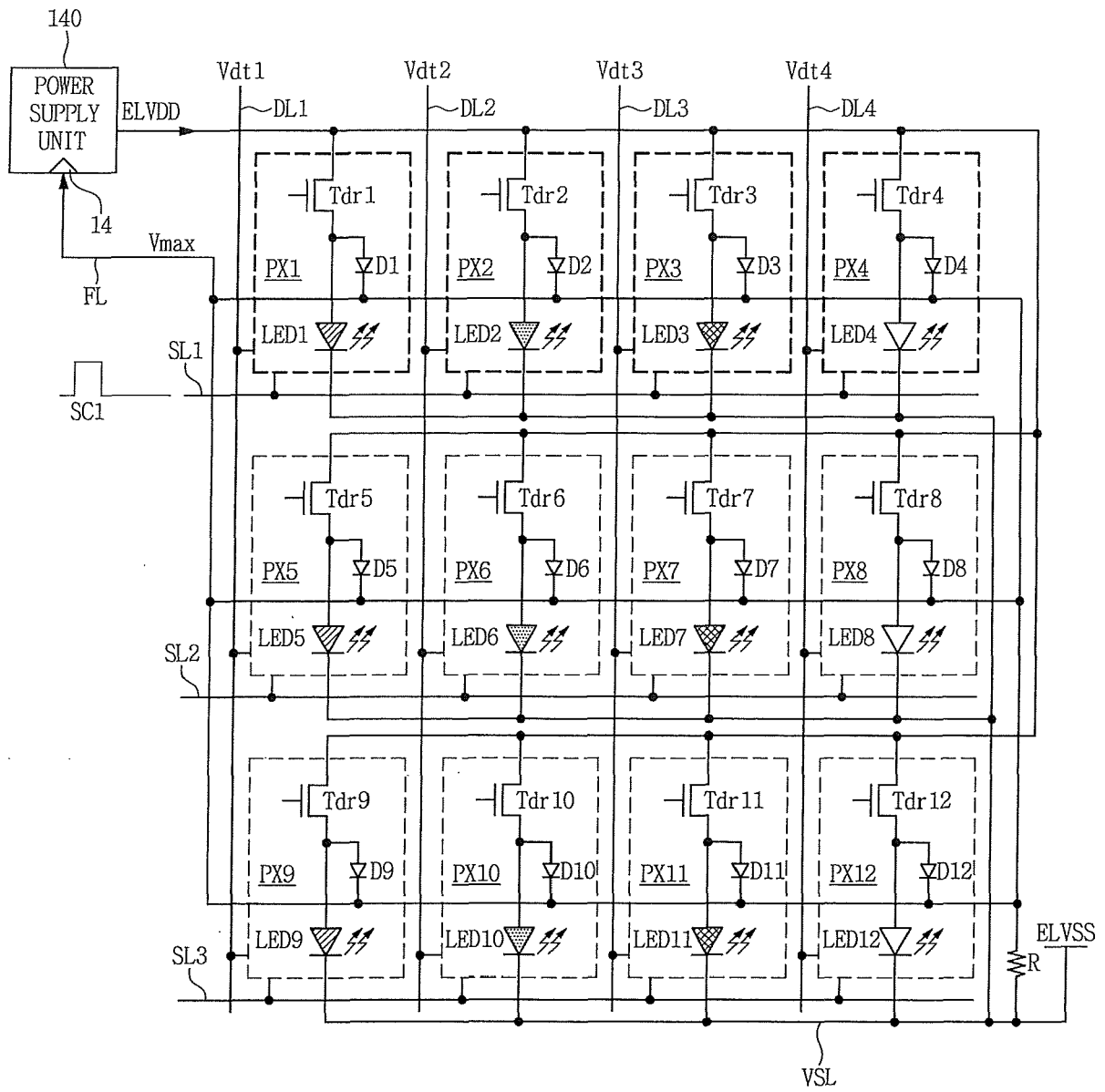


FIG. 7B

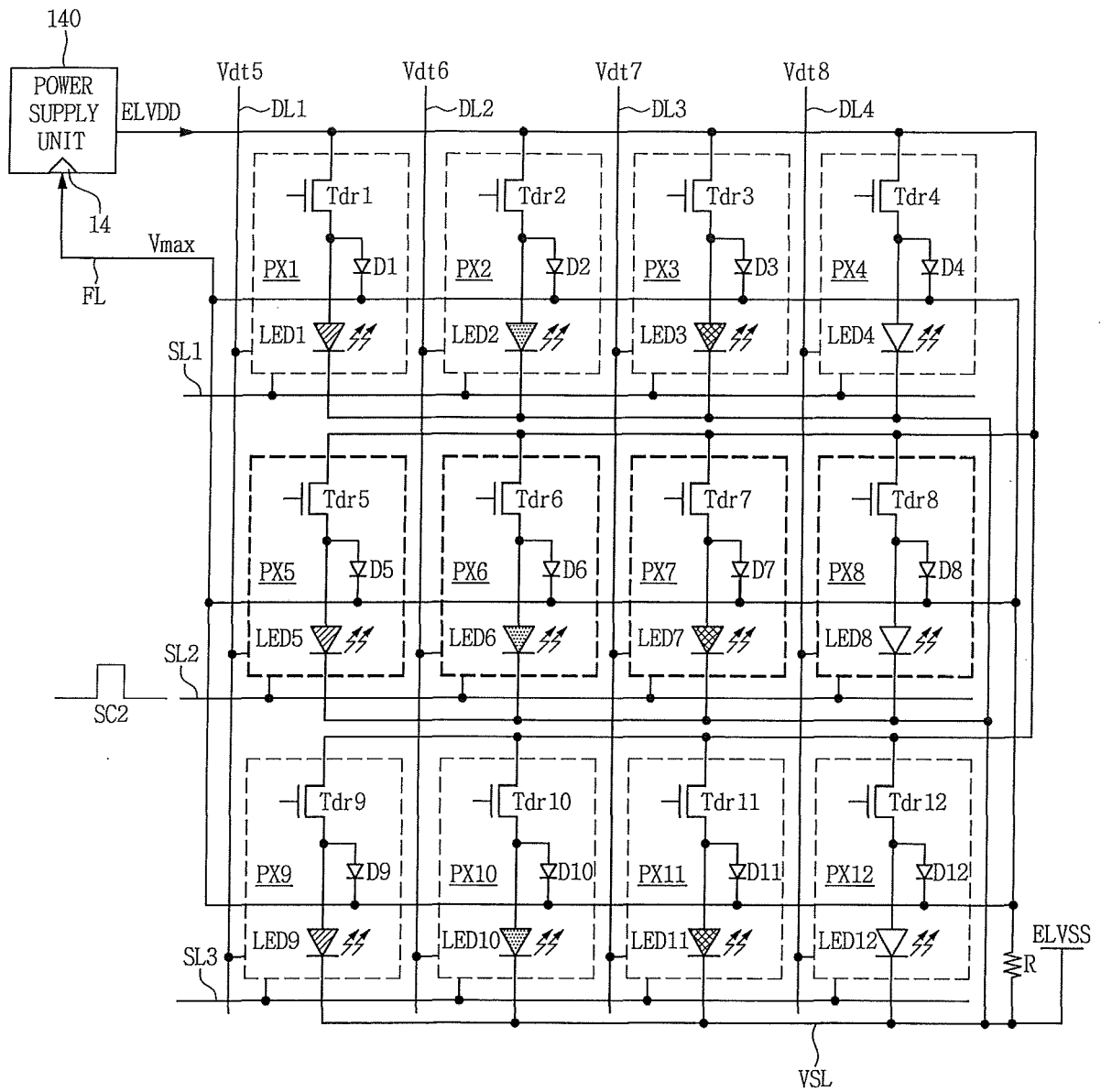




FIG. 8

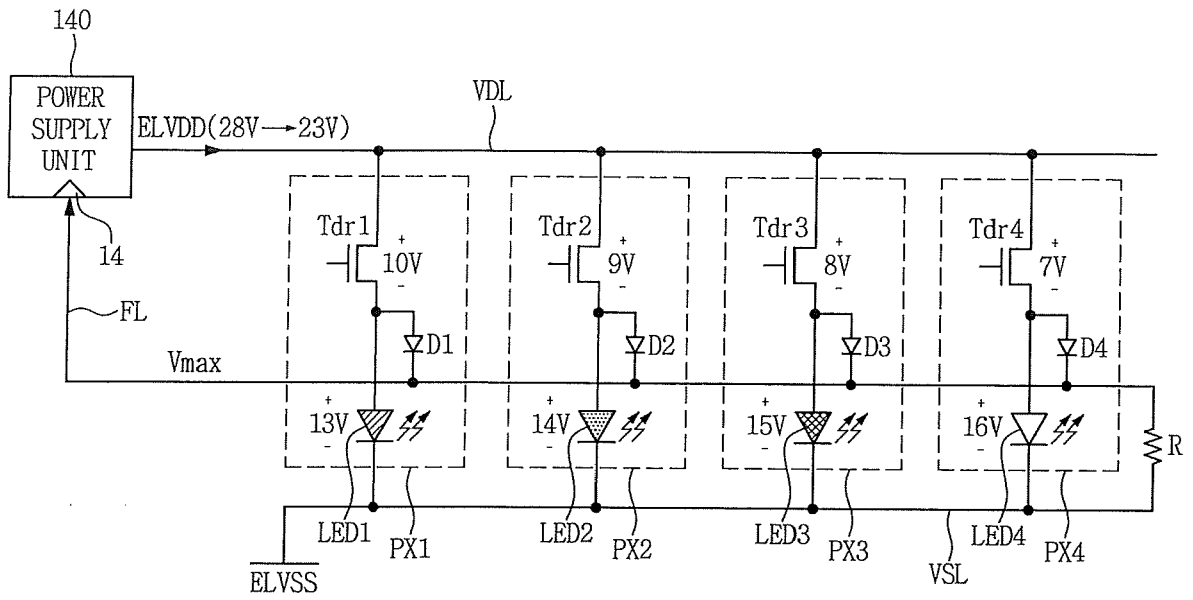


FIG. 9

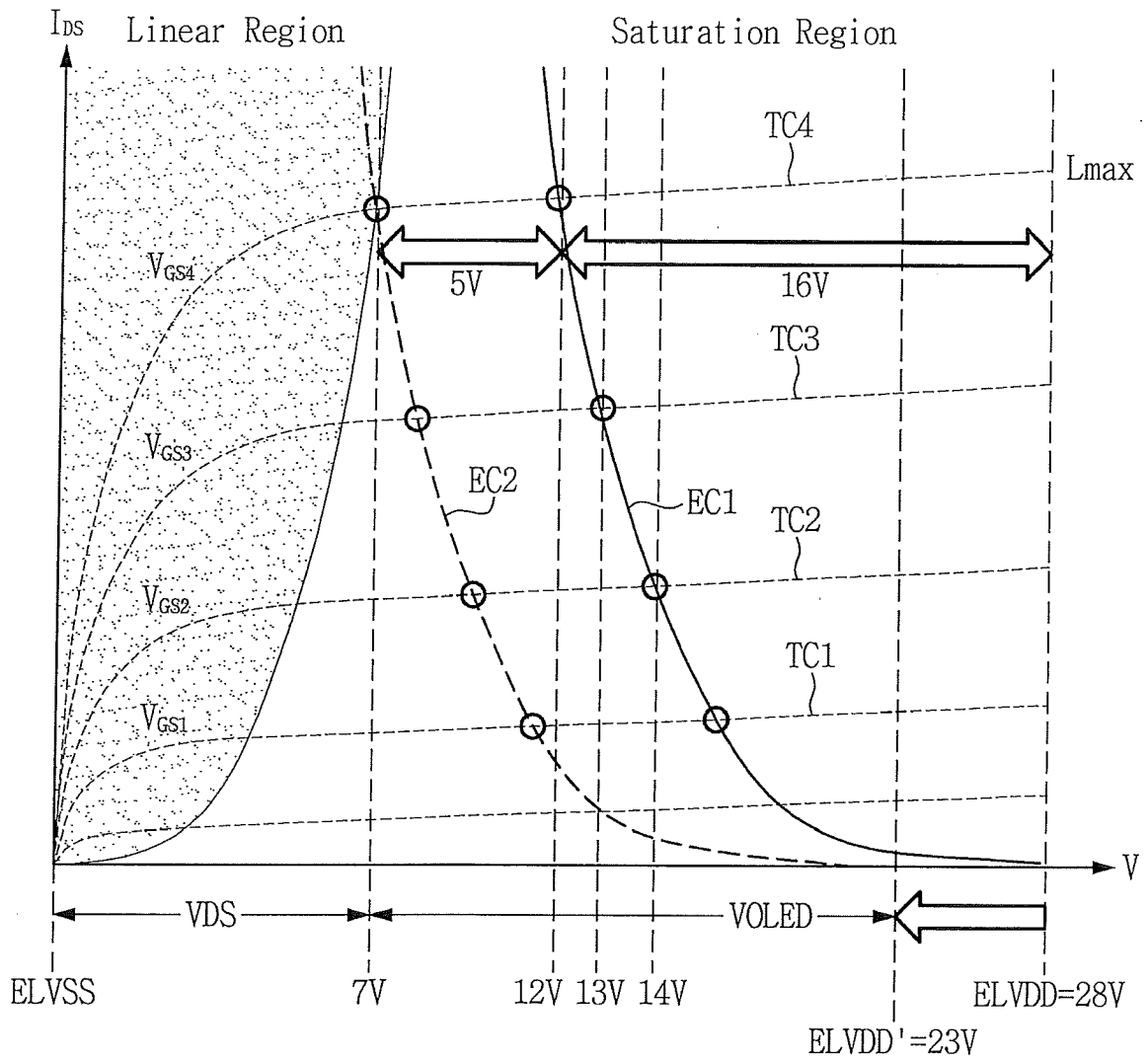


FIG. 10

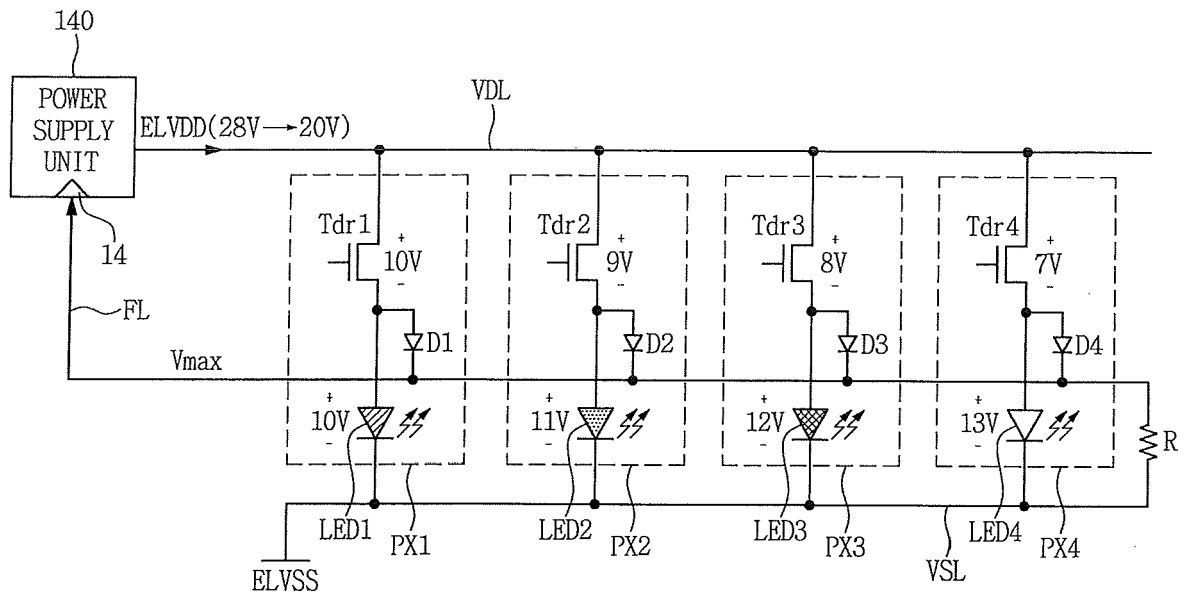
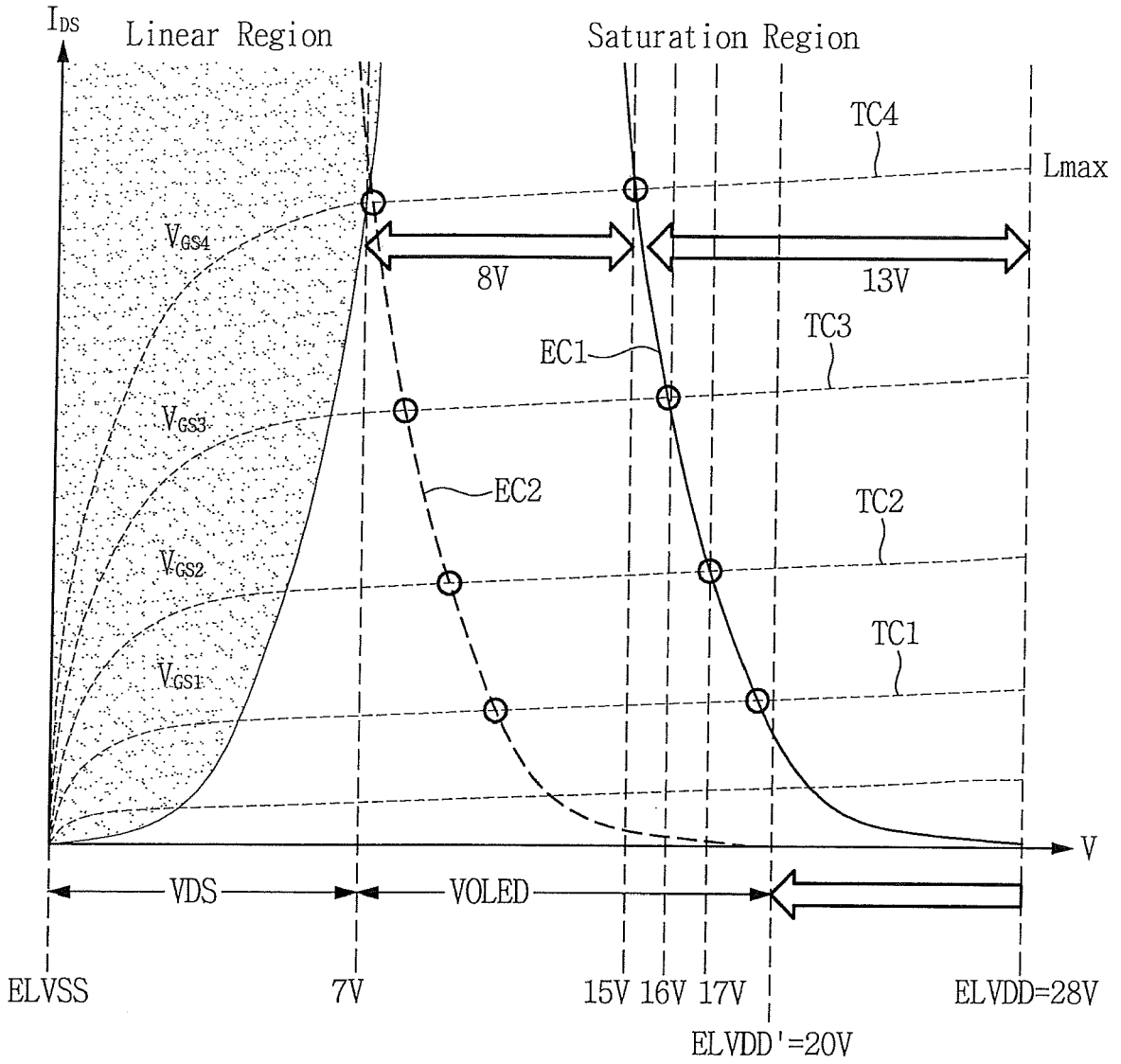


FIG. 11



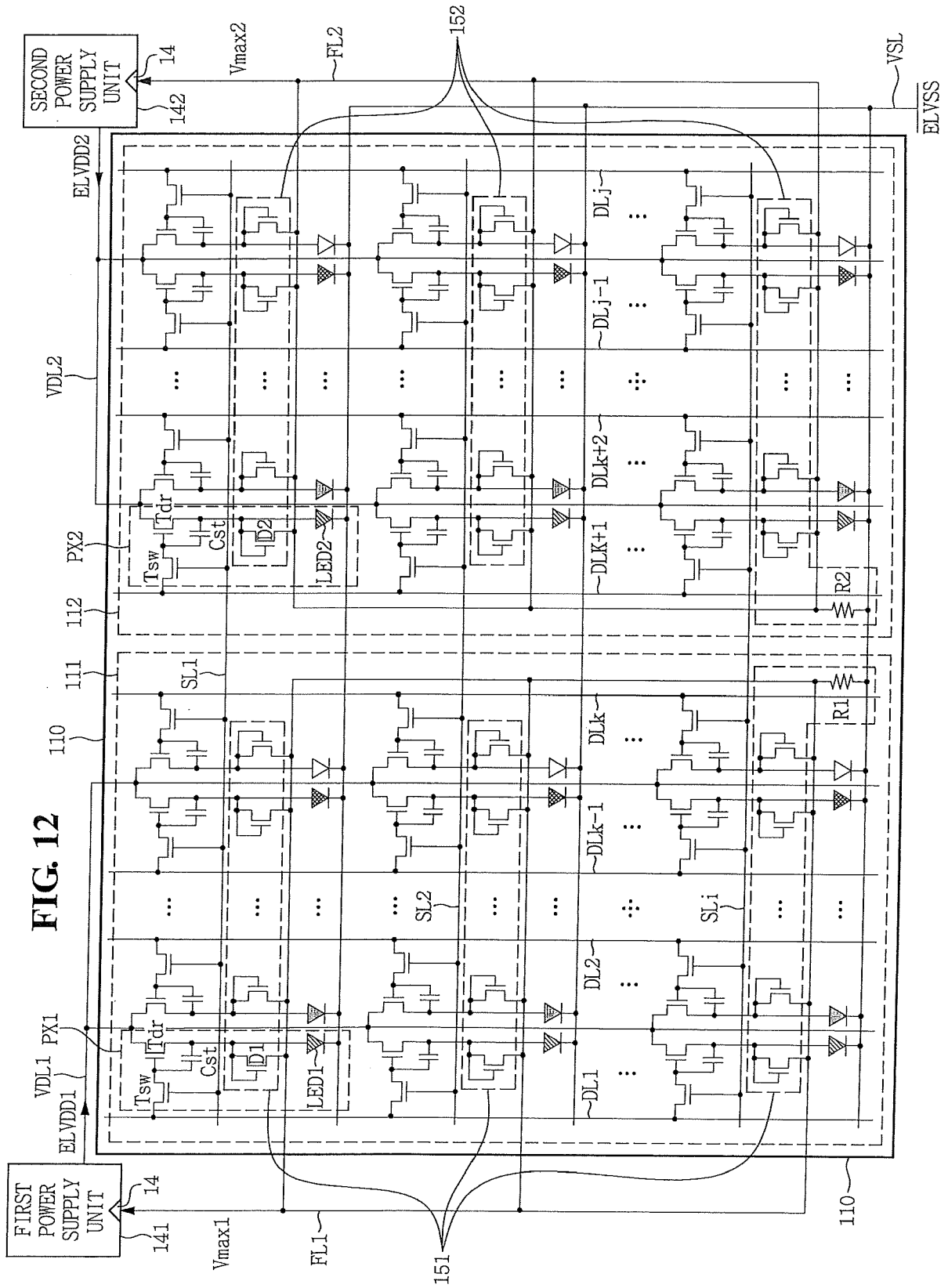


FIG. 12

FIG. 13

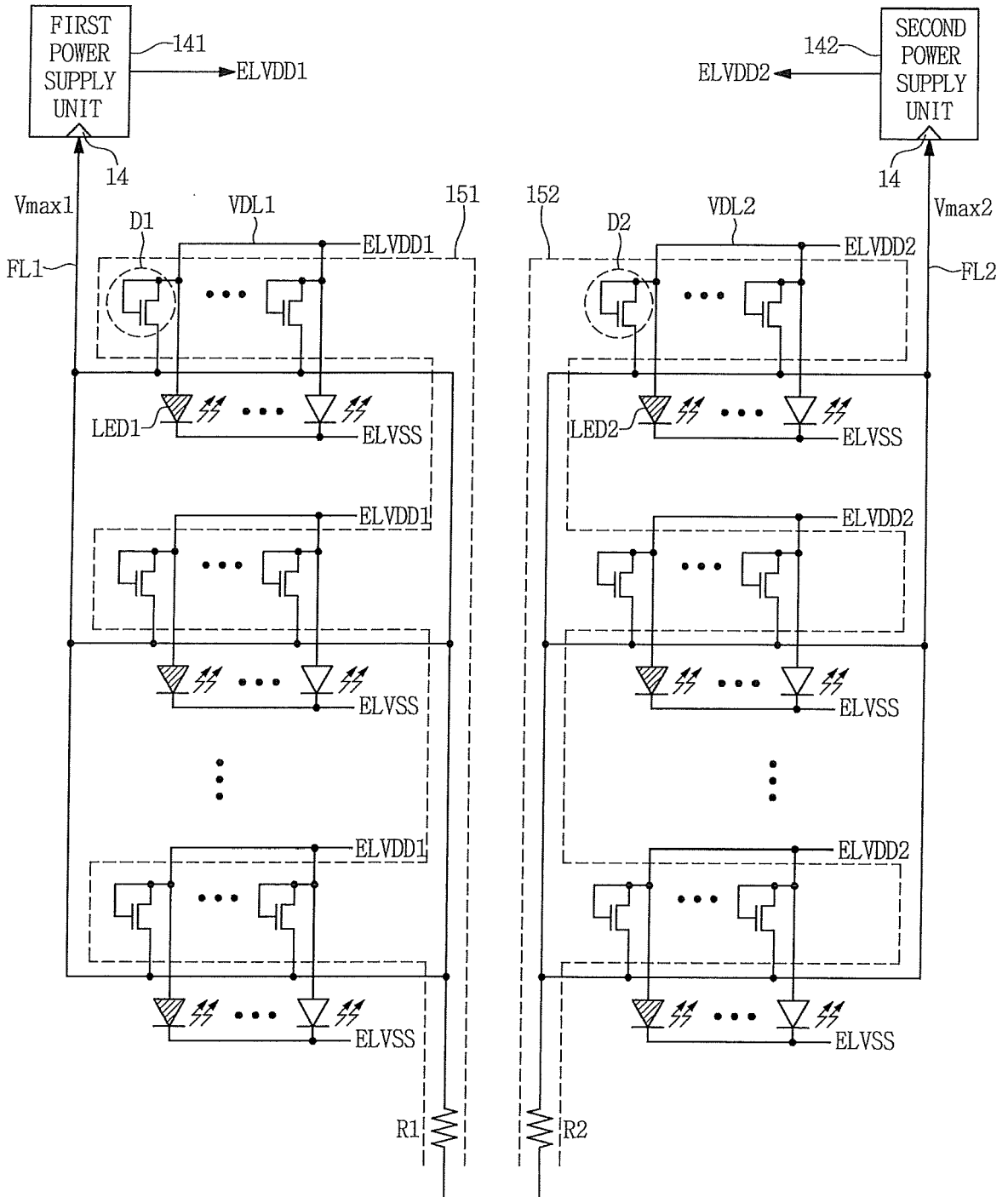




FIG. 15

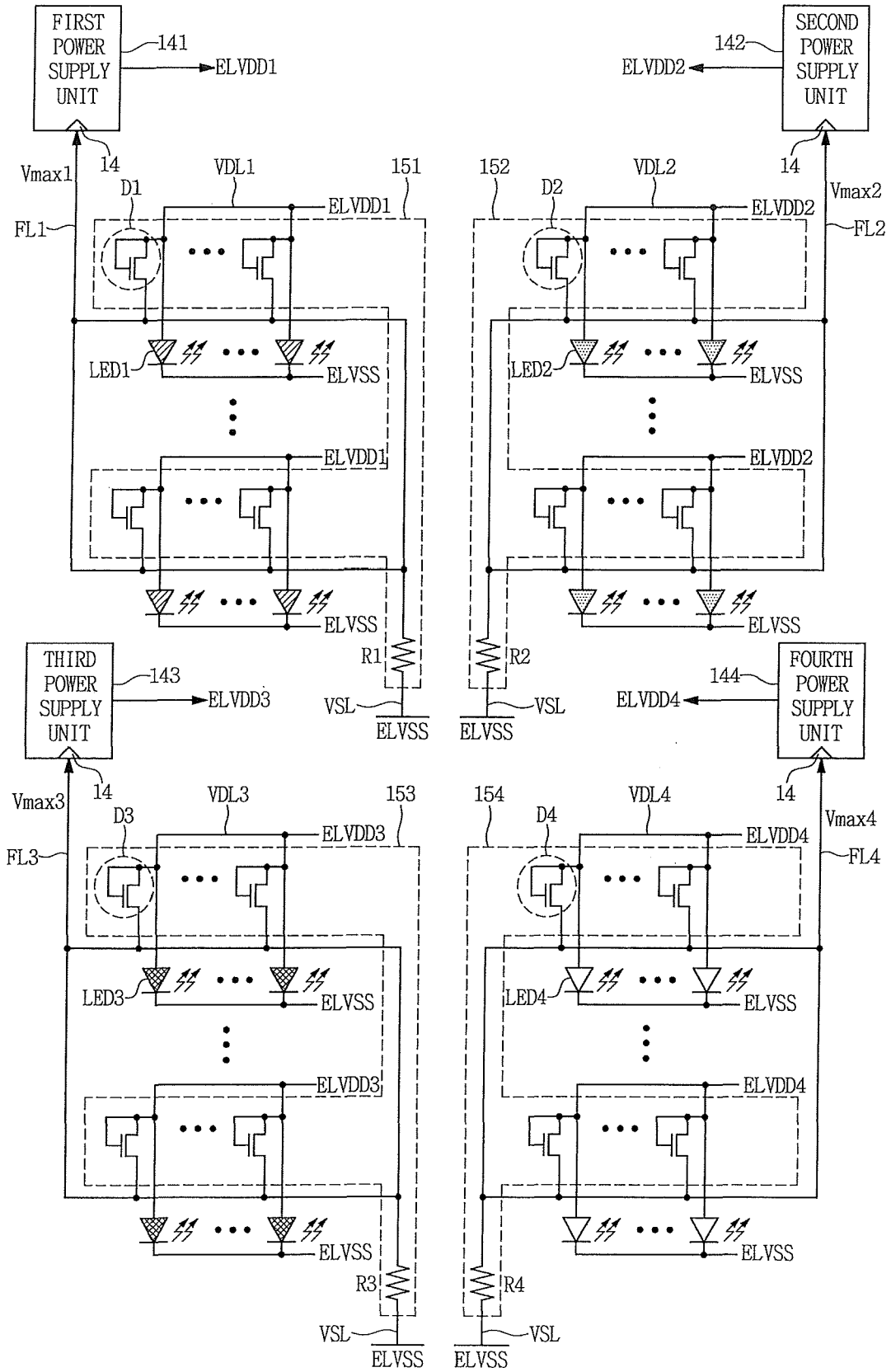


FIG. 16

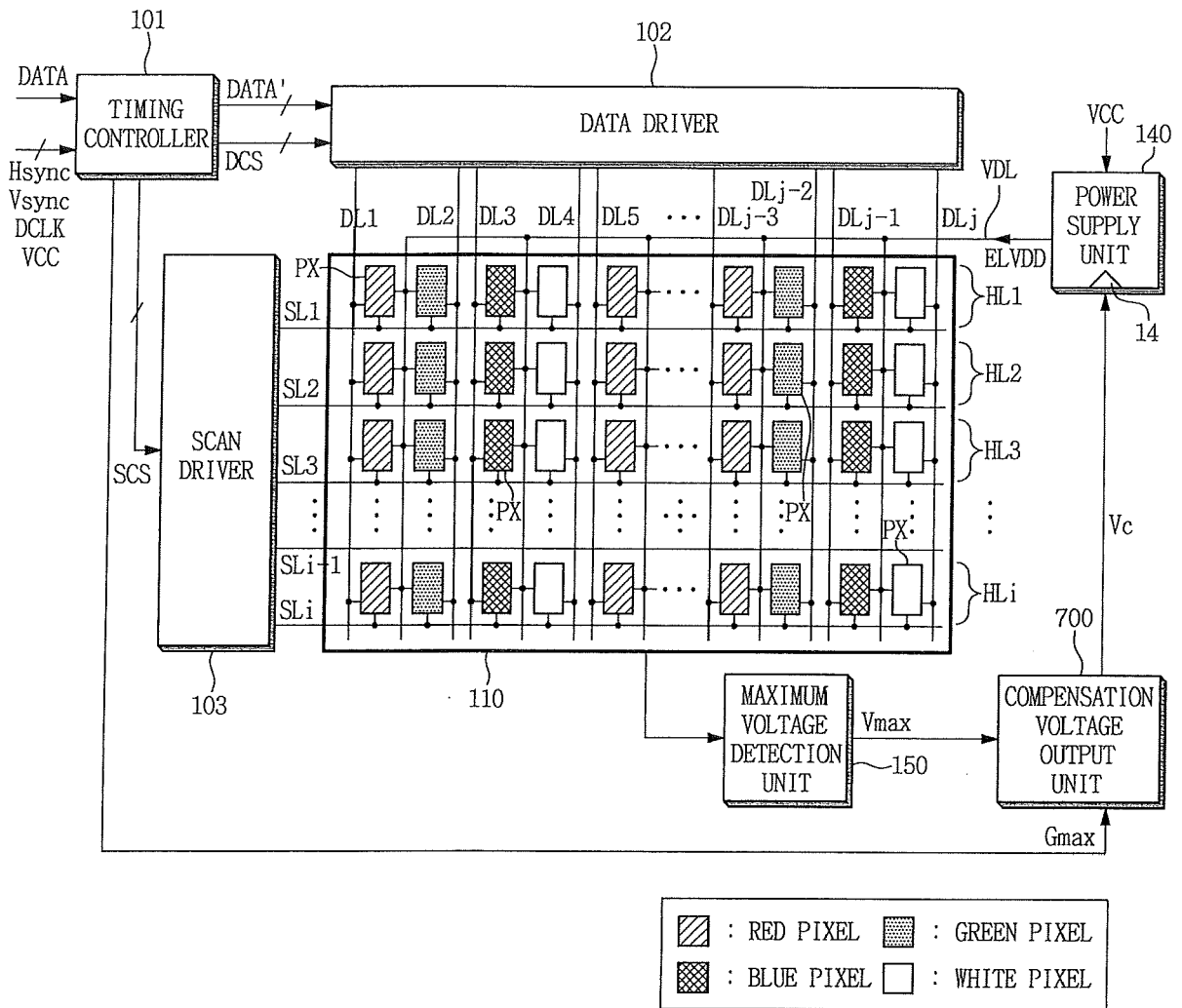




FIG. 18

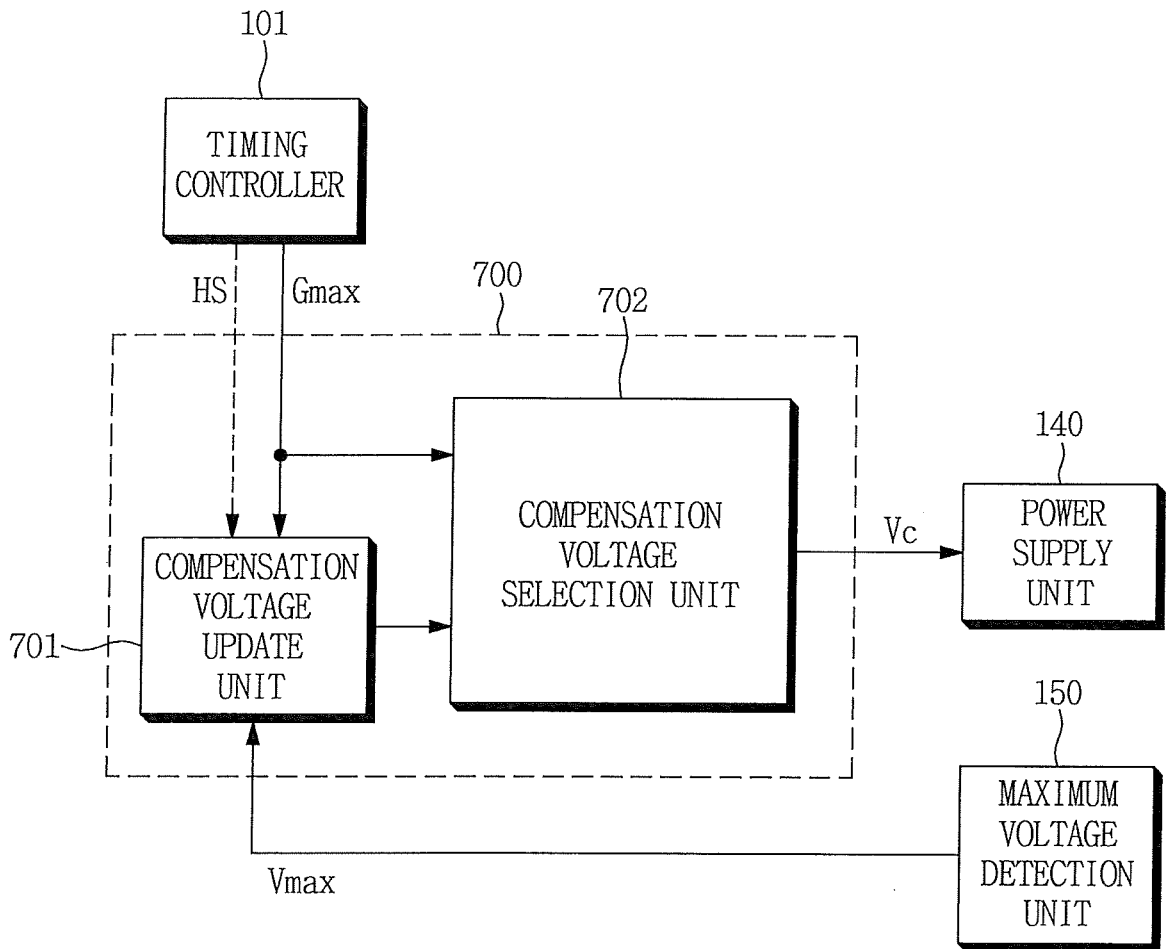


FIG. 19

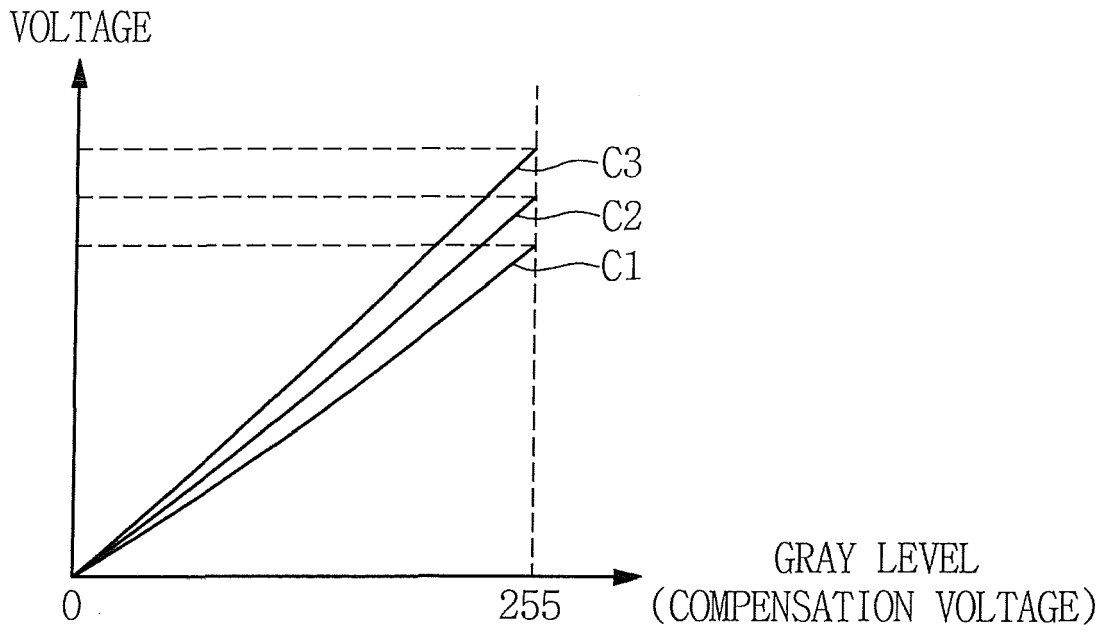
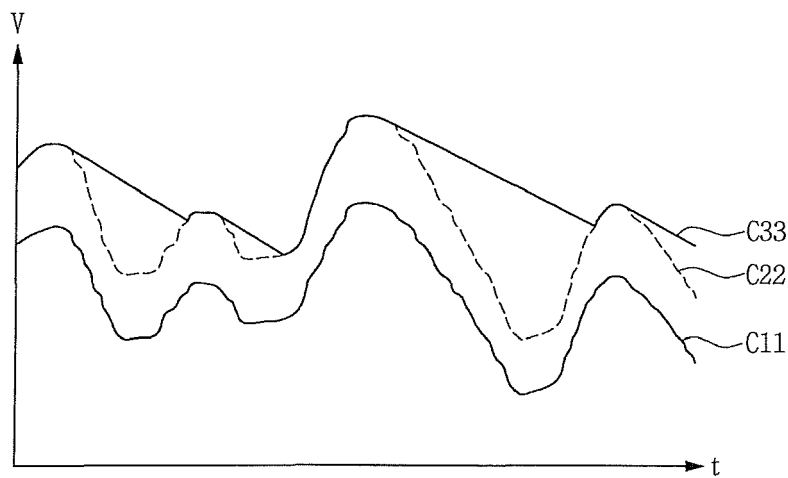


FIG. 20



专利名称(译)	发光显示装置		
公开(公告)号	<a href="#">EP3300065A2</a>	公开(公告)日	2018-03-28
申请号	EP2017193303	申请日	2017-09-26
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO., LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO., LTD.		
[标]发明人	OH WONSIK LEE MYUNGHO PARK GEUNJEONG SONG MYOUNGSEOP		
发明人	OH, WONSIK LEE, MYUNGHO PARK, GEUNJEONG SONG, MYOUNGSEOP		
IPC分类号	G09G3/3225		
CPC分类号	G09G3/3233 G09G3/3225 G09G3/3258 G09G3/3266 G09G2300/0866 G09G2310/08 G09G2320/0285 G09G2320/0295 G09G2330/021 G09G2330/028		
优先权	1020160123234 2016-09-26 KR		
其他公开文献	EP3300065A3		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

一种发光显示装置，包括：显示面板；包括在所述显示面板中的多个像素，所述多个像素中的每一个包括连接到第一电力线的驱动开关元件和连接到第二电力线的发光元件；最大电压检测单元，用于检测来自每个像素的每个发光元件的电压，并输出检测到的电压中具有最高电压电平的最大电压；以及电源单元，用于基于最大电压校正第一驱动电压并将校正后的第一驱动电压施加到第一电源线。

FIG. 1

