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(54) Title: PIXEL CIRCUIT, DISPLAY DEVICE, AND INSPECTION METHOD

FIG. 1A

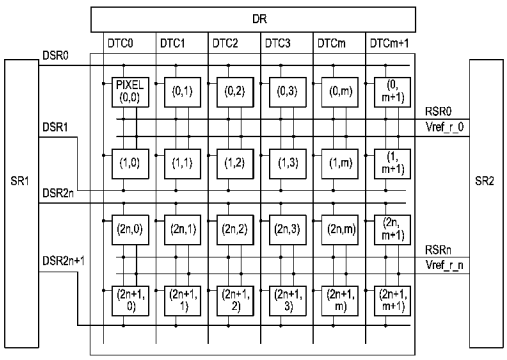
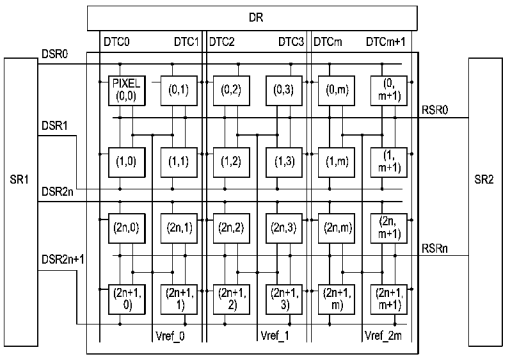


FIG. 1B



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(57) Abstract: Compensate for the variations of threshold voltage of a driving transistor. During the period of the reference signal voltage Vref being set to the signal line DTC, voltage between the gate and source of the driving transistor IOC is made equal to or greater than the threshold voltage of the driving transistor IOC, and the difference in voltage of the reference signal voltage Vref and the reference power supply voltage VreCr is charged to the retentive capacitance IOB. At the same time, the voltage of the source of the said driving transistor IOC is set to the reference power supply voltage VreCr to make the voltage applied to the said light emitting elements equal to or lower than its threshold voltage. Subsequently, while maintaining the voltage applied to the said light emitting elements IOE equal to or lower than its threshold voltage.

Specifications

PIXEL CIRCUIT, DISPLAY DEVICE, AND INSPECTION METHOD

[Technical Field]

[0001]

The present invention relates to a pixel circuit which drives light emitting elements using a driving transistor, a display device and an inspection method.

[Background Art]

[0002]

With a display device that uses current drive type light emitting elements, such as an organic EL element (OLED), a driving transistor is normally arranged in a pixel circuit. A display is made by driving the driving transistor based on display signals. However, because OLED is a current driving element, variable output current of the driving transistor is directly connected to a deterioration of visual quality. Therefore, a wide variety of proposals have been made to control variable driving current for example as in patent reference 1.

[Prior Art References]

[Patent References]

[0003]

[Patent reference 1] Japanese unexamined patent application No. 2003-271095

[Patent reference 2] Japanese unexamined patent application No. 2004-191603

[General Description of the Invention]

[Problems to be solved by the Invention]

[0004]

A switching transistor is used in the patent reference 1 to control the variation in the driving current, and the source electrode of this switching transistor and the cathode electrode of the light emitting elements are in common. Thus, the source electrode of the switching transistor becomes an open status before the light emitting elements are formed and it is difficult to conduct an inspection in such condition.

[0005]

To conduct an inspection of pixels before the light emitting elements are formed has been proposed, for example, in patent reference 2. However, this patent reference 2 does not include a method of controlling variations in the driving current, and it is impossible to prevent deterioration of display quality as is.

[Means for Solving the Problems]

[0006]

A pixel circuit according to the present invention comprises a sampling transistor which is connected to a signal line by one end and is turned on and off by the first scanning line; a driving transistor with a gate being connected to the other end of the sampling transistor and with a drain being connected to the first power supply; light emitting elements which are connected in between a source of the driving transistor and the second power supply and is driven by the current applied to the said driving transistor; a retentive capacitance connected in between the gate and source of the said driving transistor; and a switching transistor which is arranged in between the source of the said driving transistor and a reference potential line and turned on and off by the second scanning line. The said sampling transistor and the said switching transistor are electrically connected during the period when a reference signal voltage is set to the said signal line, the difference in voltage between a reference signal voltage and a reference potential is charged to the said retentive capacitance under the condition of the voltage between the gate and source of the said driving transistor being equal to or greater than the threshold voltage of the said driving transistor, and the source voltage of the said driving transistor is set to the reference potential

in order to make the voltage applied to the said light emitting elements equal to or lower than its threshold voltage. Subsequently, while a reference signal voltage is set to the said signal line, the said sampling transistor and the said switching transistor are electrically connected and by turning off the said switching transistor, the voltage equivalent to the threshold voltage of the said driving transistor is retained by the said retentive capacitance while maintaining the voltage applied to the said light emitting elements below its threshold voltage, and the said sampling transistor is electrically connected to sample the said signal voltage during the period when the display signal voltage is set to the said signal line to superimpose the said signal voltage on the threshold voltage retained by the said retentive capacitance.

[0007]

Also the present invention is a display device having a plurality of pixels arranged in a matrix, comprising a plurality of signal lines; a signal line driving circuit for driving the plurality of signal lines; a plurality of the first scanning lines; the first scanning line driving circuit for driving this first scanning lines; a plurality of the second scanning lines; the second scanning line driving circuit for driving this first scanning lines; and a reference potential line for supplying reference potential, and each pixel with one end being connected to the signal line comprises a sampling transistor, switched between being on and off by a first scanning line; a driving transistor with a gate connected to the other end of the sampling transistor and a drain connected to the first power supply; a light emitting element which is connected in between the source of the driving transistor and a second power supply and driven by the current applied to the said driving transistor; a retentive capacitance connected to between the gate and source of the said driving transistor; and a switching transistor which is arranged between the source of the said driving transistor and the reference potential line and being switched between being on and off by a second scanning line. The said sampling transistor and the said switching transistor are electrically connected during the period when a reference signal voltage is set to the said signal line, the difference in voltage between a reference signal voltage and a reference potential is charged to the said retentive capacitance under the condition of the voltage between the gate and source of the said driving transistor being equal to

or greater than the threshold voltage of the said driving transistor, and the source voltage of the said driving transistor is set to the reference potential in order to make the voltage applied to the said light emitting elements equal to or lower than its threshold voltage. Subsequently, while a reference signal voltage is set to the said signal line, the said sampling transistor and the said switching transistor are electrically connected and by turning off the said switching transistor, the voltage equivalent to the threshold voltage of the said driving transistor is retained by the said retentive capacitance while maintaining the voltage applied to the said light emitting elements equal to or lower than its threshold voltage, and the said sampling transistor is electrically connected to sample the said signal voltage during the period when the display signal voltage is set to the said signal line to superimpose the said signal voltage on the threshold voltage retained by the said retentive capacitance.

[0008]

Also, it is preferred that the said reference potential line is common for two rows of pixels and arranged in the row direction per two rows of pixels.

[0009]

Also, it is preferred that the said reference potential line is common for two columns of pixels and arranged in the column direction per two rows of pixels.

[0010]

It is preferred that the said reference potential lines are connected in a group outside of the display area where the said pixels are arranged.

[0011]

It is preferred that a probe point which is connected to the said reference potential line is a probe point which can be pointed by probe from outside at least before the said light emitting elements are formed.

[0012]

Also, it is preferred that the said second scanning line is common for two rows of pixels and arranged in the column direction per 2 rows of pixels.

[0013]

Also, it is preferred that the current – voltage characteristic of the driving transistor is measured before the said light emitting elements are formed, by connecting a probe to the reference potential line to control the said sampling transistor and the on and off of the switching transistor to detect current which flows out from the reference potential line

[Advantages of the Invention]

[0014]

According to the present invention, threshold voltage at which current starts to flow to the driving transistor is corrected in a pixel circuit to make variations in the driving current small. Also, the cost reduction can be realized by not sending defective products to the next step, because pixels can be inspected before the said light emitting elements are formed.

[Brief Description of the Drawings]

[0015]

Fig. 1A is a block diagram of the present invention.

Fig. 1B is a block diagram of the present invention.

Fig. 2 is a pixel circuit of the present invention.

Fig. 3 is operation waves of the present invention.

Fig. 4A is an explanatory diagram of the present invention.

Fig. 4B is an explanatory diagram of the present invention.

Fig. 4C is an explanatory diagram of the present invention.

Fig. 4D is an explanatory diagram of the present invention.

Fig. 4E is an explanatory diagram of the present invention.

Fig. 4F is an explanatory diagram of the present invention.

Fig. 4G is an explanatory diagram of the present invention.

Fig. 4H is an explanatory diagram of the present invention.

Fig. 4J is an explanatory diagram of the present invention.

Fig. 4K is an explanatory diagram of the present invention.

Fig. 5A is a block diagram of the present invention.

Fig. 5B is an explanatory diagram of the present invention.

[Mode for Carrying out the Invention]

[0016]

An embodiment of the present invention will be explained based on the figures below.

[0017]

A block diagram of the entire display device according to the embodiment is indicated in Fig. 1A. As illustrated, pixels 10 are arranged in a matrix in a display area and a column direction signal line DTC for each column of pixels 10, the first scanning lines DSR corresponding to each row of pixels, the second scanning lines RSR corresponding to two rows of pixels, and a reference potential line Vref_r are arranged. Two of the first scanning lines DSR are arranged in between two rows of pixels and are connected to both upper and lower sides of pixels respectively, while the second scanning lines PSR and the reference potential line Vref_r are arranged between rows of pixels where there is no first scanning line DSR arranged, and each are connected to upper and lower pixels.

[0018]

Also, a signal line driving circuit DR for controlling the column direction signal lines, a first scanning line DSR in the row direction and a first scanning line driving circuit SRI for controlling the same, and a second scanning line drive circuit SR2 for controlling a second scanning line RSR in the row direction are arranged at the periphery of the display section in which pixels 10 are arranged. The second scanning line RSR and the reference potential line Vref_r are commonly connected to the pixels of upper and lower two rows.

[0019]

Also, the reference potential line Vref_r may be in a line direction. In this case, the reference potential line Vref_r is common for every two lines and connected to the pixels in left and right two lines. The constitution of such is indicated in Fig. 1B. Hereinafter, the reference potential line Vref_r in the row direction will be explained.

[0020]

The actual structure of a pixel circuit contained in the display device shown in Fig. 1 is shown in Fig. 2. Since the second scanning lines DSR and the reference potential lines Vref_r are each shared by two rows, 2 pixels are illustrated in this figure. As shown in Fig. 2, this pixel circuit comprises a light emitting element 10E which emits light as a result of current flow, such as an OLED (organic EL element), a sampling transistor 10A, a driving transistor 10C, a switching transistors 10D, and a retentive capacitance 10B. A gate of the sampling transistor 10A is connected to the first scanning lines DSR while one end is connected to the column direction signal line DTC and the other end is connected to the gate of the driving transistor 10C. The drain electrode of the driving transistor 10C is connected to the power supply VCC and the source electrode is connected to the anode of a current drive type light emitting elements 10E such as organic EL elements. The cathode of the light emitting elements 10E is connected to a cathode power supply VEE. Also, a retentive capacitance 10B is connected in between the gate of the driving transistor 10C and the source electrode. One end of a switching transistor 10D is connected in between the drain of the driving transistor 10C and the anode of the light emitting elements 10E, and the other end as well as the gate electrode are connected to the neighboring pixels of the switching transistor 10D by the other end and the gate electrode.

[0021]

In Fig. 2, the upper section is pixel 10, the lower section is pixel 11 and each element in the lower pixel is given symbols 11A to 11E.

[0022]

Also Fig. 2 is illustrated so as the first scanning line DSR is arranged within a column of a pixel one by one and the number of lines arranged in column is indicated as 1, 3, … but for arranging pixels, the first scanning line DSR may be arranged by 2 lines in every other column of a pixel as in Fig. 1A, B which is mentioned above.

[0023]

Fig. 3 indicates a timing chart. Figs. 4A to 4K illustrate operations of each step.

[0024]

Fig. 4A is a light emitting period, and the sampling transistors 10A, the switching transistor 1-D are turned off, while the light emitting elements 10E, 11E emit light as a result of the current which is supplied from the driving transistors 10C, 11E.

[0025]

Fig. 4B is a threshold detection period, and the sampling transistor 10A is made conductive by making the signal line DTCm a reference potential Vref with the first scanning line DSR being H level. By doing so, the voltage of the gate electrode of the driving transistor 10C becomes Vref. Meanwhile, the voltage of the source electrode of the driving transistor 10C is made Vref_r by turing on the switching transistor 10D with the second scanning line RSR being H level. The difference in voltage of Vref and Vref_r is made greater than the threshold voltage of the driving transistor 10C and the voltages of the source electrode of the driving transistor 10C is made equal to or lower than the threshold voltage Vth_10E of the light emitting elements 10E. That is, it is set to satisfy the following equation: Vgs_10C = Vref – Vref_r > Vth_10C, VEE + Vth_10E > Vref_r

[0026]

Consequently, although the driving transistor 10 is turned on, current is not applied to the light emitting elements 10E. In the retentive capacitance 10B, Vgs – 10C is retained.

[0027]

Fig. 4C is a sampling period for 2 x (n – 4)th column and 2 x (n – 3)th column. It is therefore necessary to ensure that there is no impact on pixels of columns other than this. Thus, the sampling transistors 10A and 11A are therefore made non-conductive.

[0028]

Fig. 4D is a threshold detection preparation period for pixels. The signal line DTCm is made the reference potential Vref, and the gate electrodes of the driving transistors 10C and 11C are made Vref, and so the sampling transistors 10A and 11A are made conductive. The switching transistors 10D, 11D are made conductive to make the voltage of Vgs_10C, Vgs_11C between the gate electrode and source electrode of the driving transistors 10C, 11C greater than the threshold voltage Vth_10C, Vth_11C and also to make the light emitting elements 10E, 11E equal to or lower than the threshold voltage.

[0029]

This is expressed in the equations below:

$Vgs\_10C = Vref - Vref\_r > Vth\_10C$……1

$Vgs\_11C = Vref - Vref\_r > Vth\_11C$……2

$VEE + Vth\_10E > Vref\_r$……..3

$VEE + Vth\_11E > Vref\_r$……..4

[0030]

The second scanning line here is common per two lines, the pixel having address (2n, m) requires a threshold detection period longer by 1H than the pixel having address (n + 1, m). Also in Fig. 3, threshold detection period for the pixel having address (2n, m) is set to 1H, the pixel having address (2n + 1, m) is set to 2H, but the steps should be repeated until the conditions of equation 1 – 4 are met. The retentive capacitance 10B and parasitic capacitance are discharged enough as to satisfy the above equations.

[0031]

Fig. 4D is a threshold detection period for pixels. The signal line DTCm is made the reference potential Vref, and the gate electrodes of the driving transistors 10C and 11C are made Vref, and so the sampling transistors 10A and 11A are made conductive. In order to detect threshold voltage of the driving transistors 10C, 11C, the switching transistors 10D, 11D are therefore made non-conductive. Consequently, the condition of the driving transistors 10C, 11C being on and no current flows in the light emitting elements 10E, 11E is maintained and the voltage Vgs between the gate electrode and the source electrode of the driving transistors 10C, 11C should be set to the threshold voltage of each transistor. The difference in voltage of Vref and Vref_r is accumulated in the retentive capacitances 10B, 11B which modifies towards the threshold voltage of each transistor.

[0032]

Fig. 4F is a sampling preparation period of five step F, 2 x (n – 3) + 1th column, 2 x (n – 2)th column, 2 x (n – 2)＋1th column, 2 x (n – 1)th column and 2 x (n – 1)＋1th column. It is therefore necessary to ensure that there is no impact on pixels of columns other than this. The sampling transistors 10A and 11A are therefore made non-conductive. In this period the voltage of the previous threshold detection period is retained for each electrode.

[0033]

The steps of Fig. 4E and 4E are repeated until the voltage between the gate electrode and the source electrode of the driving transistor Vgs becomes the threshold voltage Vth. In the figures, it is repeated 5 times. At this time, the voltage Vs of the source electrode of the driving transistors 10C, 11C are as below:

Vs_10C = Vref – Vth_10C…….5

Vs_11C = Vref – Vth_11C.....6

Therefore, Vth_10C, Vth_11C are retained in the retentive capacitances 10B, 11B respectively.

[0034]

Also at this time, the voltage applied to the light emitting elements 10E, 11E must be less than the threshold voltage Vth_10E, Vth_11E. That is, it must satisfy the following equations:

VEE + Vth_10E > VS_10C.....7

VEE + Vth_11E > Vs_11C.....8

[0035]

In regards to 2nth column, Vref must satisfy equation 9 which is obtained from equations 5 and 7, and Vref_r must satisfy equation 1.

VEE + Vth_10E + Vth_10C > Vref.....9

[0036]

Fig. 4G is a sampling period for sampling signal voltage Vsig0 by making the signal lines a desired signal voltage Vsig0 and making the sampling transistor 10A conductive. The gate electrode potential of the driving transistor 10C changes from Vref to Vsig0.

[037]

At this time, the source electrode of the driving transistor 10C becomes:

Vs_10C = Vref – Vth_10C + (Vsig0 – Vref) x Cap_10E / (Cap_10B + Cap_10E) + VEExCap_10B / (Cap_10B + Cap_10E)

= {Cap_10BX (VEE + Vref + Cap_10ExVsig0} / (Cap_10B + Cap_10E) – Vth_10C

The voltage between the gate electrode and source electrode becomes:

Vgs_10C = Cap_10B / (Cap_10B + Cap_10E) (Vsig0 – VEE – Vref) + Vth_10C

[0038]

In Fig. 4H, the sampling transistors 10A, 11A are non-conductive, and therefore the potential of the previous step is retained for each electrode.

[0039]

Fig. 4J is the final threshold detecting period of 2n + 1th column, and the sampling transistor 10A is made non-conductive while 11A is conductive.

[0040]

Fig. 4K is a sampling period for sampling signal voltage Vsig1 by making the signal lines a desired signal voltage Vsig1 at the sampling transistor 11A. The gate electrode potential of the driving transistor 11C changes from Vref to Vsig1.

[0041]

At this time, the source electrode of the driving transistor 11C becomes:

$Vs\_11C = Vref - Vth\_11C + (Vsig0 - Vref) \times Cap\_11E / (Cap\_11B + Cap\_11E) + VEE \times Cap\_11B / (CAp\_11B + Cap\_11E)$

The voltage between the gate electrode and source electrode becomes:

$Vgs\_11C = Cap\_11B / (Cap\_11B + Cap\_11E) X (Vsig0 - VEE - Vref) + Vth\_11E$

[0042]

A characteristic formula for Ids of driving transistors is expressed by $Ids=\beta / 2(Vgs - Vth)^2$. If Vgs_10C and Vgs_11C are respectively input, it becomes:

$Ids0 = \beta / 2\{Cap\_10B / (Cap\_10B + Cap\_10E) X (Vsig0 - VEE - Vref)\}^2$

$Ids1 = \beta / 2\{Cap\_11B / (Cap\_11B + Cap\_11E) X (Vsig1 - VEE - Vref)\}^2$

The term Vth is corrected, and variations in drive current can be suppressed.

[0043]

Fig. 5A is an overall view of checking failures in transistors, driving transistors, and switching transistors for sampling signal voltage before light emitting elements are formed. The reference potential lines Vref_r is outside of display area and a certain number of lines are connected in a group. The number of the reference potential lines Vref_r to be bound together is determined considering the number of current measuring device, measuring time and S / N ratio. In the figure, Vref_r_0 and Vref_r_n are bound together. And to one end of the bound reference potential line Vref_r, a probe point for measuring is created.

[0044]

Fig. 5B indicates a pixel circuit of before light emitting elements 10E are formed and of when checking failures in sampling transistors 10A, driving transistors 10C, and switching transistors 10D which are for sampling signal voltage before light emitting elements are formed. That is, when the light emitting elements 10E are formed, the source of the driving transistor 10C is connected to the anode of the light emitting elements 10E, but this connection does not exist before the light emitting elements 10E are formed.

[0045]

The sampling transistor 10A and the switching transistor 10D are made conductive and the signal potential is given to the gate electrode of the driving transistor 10C from the signal line DTCm. At this time, the current which flows between the drain electrode and source electrode of the driving transistor 10C is measured at the probe point connected to Vref_r to check failures. That is, the second scanning line RSR is made H level and the first scanning line DSR is sequentially made H level. By doing so, the sampling transistors 10A of corresponding pixel are turned on, the potential of the signal line DTC is brought into a pixel, a current corresponding to the current is applied, and the current flowing from the probe point to an external ground is measured using a measuring device to confirm operation of pixel circuit.

[0046]

In particular, IV characteristics including threshold voltage of the driving transistor 10C in one pixel circuit can be detected.

[0047]

Also, by turning on the signal line DTC one by one, inspections of pixel is conducted one by one, but failures in elements can be detected when inspecting a group of pixels.

[0048]

Although a n-channel transistor is used in the embodiment above, p-channel transistor may be used. When a p-channel transistor is used in the driving transistor 10C, the source electrode is arranged on

the power supply VCC side and the light emitting elements 10# and the retentive capacitance 10B are also arranged on the power supply VCC side.

[0049]

According to the embodiment of the present invention, threshold voltage at which current starts to flow to the driving transistor is corrected in each pixel circuit to make variations in the driving current small. Also, when inspection of pixel before light emitting elements are formed, that is, failures in sampling transistors, driving transistors, and switching transistors can be checked before the light emitting elements are formed. Consequently, by not sending failure products to the next step, cost reduction is realized.

[Description of the Symbols]

[0050]

10, 11 pixels, 10A, 11A sampling transistors, 10B, 11B retentive capacitances, 10C, 11C driving transistors, 10D, 11D switching transistors, 10E, 11E light emitting elements.

Claims

[Claim 1]

A pixel circuit comprising a sampling transistor which is connected to a signal line by one end and is turned on and off by the first scanning line;

a driving transistor with a gate being connected to the other end of the sampling transistor and with a drain being connected to the first power supply;

light emitting elements which are connected in between a source of the driving transistor and the second power supply and is driven by the current applied to the said driving transistor;

a retentive capacitance connected in between the gate and source of the said driving transistor; and

a switching transistor which is arranged in between the source of the said driving transistor and a reference potential line and turned on and off by the second scanning line. The said sampling transistor and the said switching transistor are electrically connected during the period when a reference signal voltage is set to the said signal line, the difference in voltage between a reference signal voltage and a reference potential is charged to the said retentive capacitance under the condition of the voltage between the gate and source of the said driving transistor being equal to or greater than the threshold voltage of the said driving transistor, and the source voltage of the said driving transistor is set to the reference potential in order to make the voltage applied to the said light emitting elements equal to or lower than its threshold voltage. Subsequently, while a reference signal voltage is set to the said signal line, the said sampling transistor and the said switching transistor are electrically connected and by turning off the said switching transistor, the voltage equivalent to the threshold voltage of the said driving transistor is retained by the said retentive capacitance while maintaining the voltage applied to the said light emitting elements equal to or lower than its threshold voltage, and the said sampling transistor is electrically connected to sample the said signal voltage during the period when the display signal voltage is set to the said signal line to superimpose the said signal voltage on the threshold voltage retained by the said retentive capacitance.

[Claim 2]

A display device having a plurality of pixels arranged in a matrix, comprising:

a plurality of signal lines;

a signal line driving circuit for driving the plurality of signal lines;

a plurality of the first scanning lines;

the first scanning line driving circuit for driving this first scanning lines;

a plurality of the second scanning lines;

the second scanning line driving circuit for driving this first scanning lines; and a reference potential line for supplying reference potential, and

each pixel with one end being connected to the signal line comprises a sampling transistor, switched between being on and off by a first scanning line;

a driving transistor with a gate connected to the other end of the sampling transistor and a drain connected to the first power supply;

a light emitting element which is connected in between the source of the driving transistor and a second power supply and driven by the current applied to the said driving transistor;

a retentive capacitance connected to between the gate and source of the said driving transistor; and

a switching transistor which is arranged between the source of the said driving transistor and the reference potential line and being switched between being on and off by a second scanning line. The said sampling transistor and the said switching transistor are electrically connected during the period when a reference signal voltage is set to the said signal line, the difference in voltage between a reference signal voltage and a reference potential is charged to the said retentive capacitance under the condition of the voltage between the gate and source of the said driving transistor being equal to or greater than the threshold voltage of the said driving transistor, and the source voltage of the said driving transistor is set to the reference potential in order to make the voltage applied to the said light emitting elements below its

threshold voltage. Subsequently, while a reference signal voltage is set to the said signal line, the said sampling transistor and the said switching transistor are electrically connected and by turning off the said switching transistor, the voltage equivalent to the threshold voltage of the said driving transistor is retained by the said retentive capacitance while maintaining the voltage applied to the said light emitting elements below its threshold voltage, and the said sampling transistor is electrically connected to sample the said signal voltage during the period when the display signal voltage is set to the said signal line to superimpose the said signal voltage on the threshold voltage retained by the said retentive capacitance.

[Claim 3]

The display device according to claim 2, where in the said reference potential lines are common for two rows of pixels and arranged in the row direction per two rows of pixels.

[Claim 4]

The display device according to claim 2, where in the said reference potential lines are common for two columns of pixels and arranged in the column direction per two rows of pixels.

[Claim 5]

The display device according to any of claims 2 – 4, wherein the said reference potential lines are connected in a group outside of the display area where the said pixels are arranged.

[Claim 6]

The display device according to claim 5 comprising a probe point which is connected to the said reference potential line and which can be pointed by probe from outside at least before the said light emitting elements are formed.

[Claim 7]

The display device according to claim 2, where in the said second scanning line is common to two rows of pixels and arranged in the column direction per two rows of pixels.

[Claim 8]

An inspection method of the display method according to claims – 7, wherein the current – voltage characteristic of the driving transistor is measured before the said light emitting elements are formed by connecting a probe to the reference potential line to control the said sampling transistor and the on and off of the switching transistor to detect current which flows out from the reference potential line.

FIG. 1A

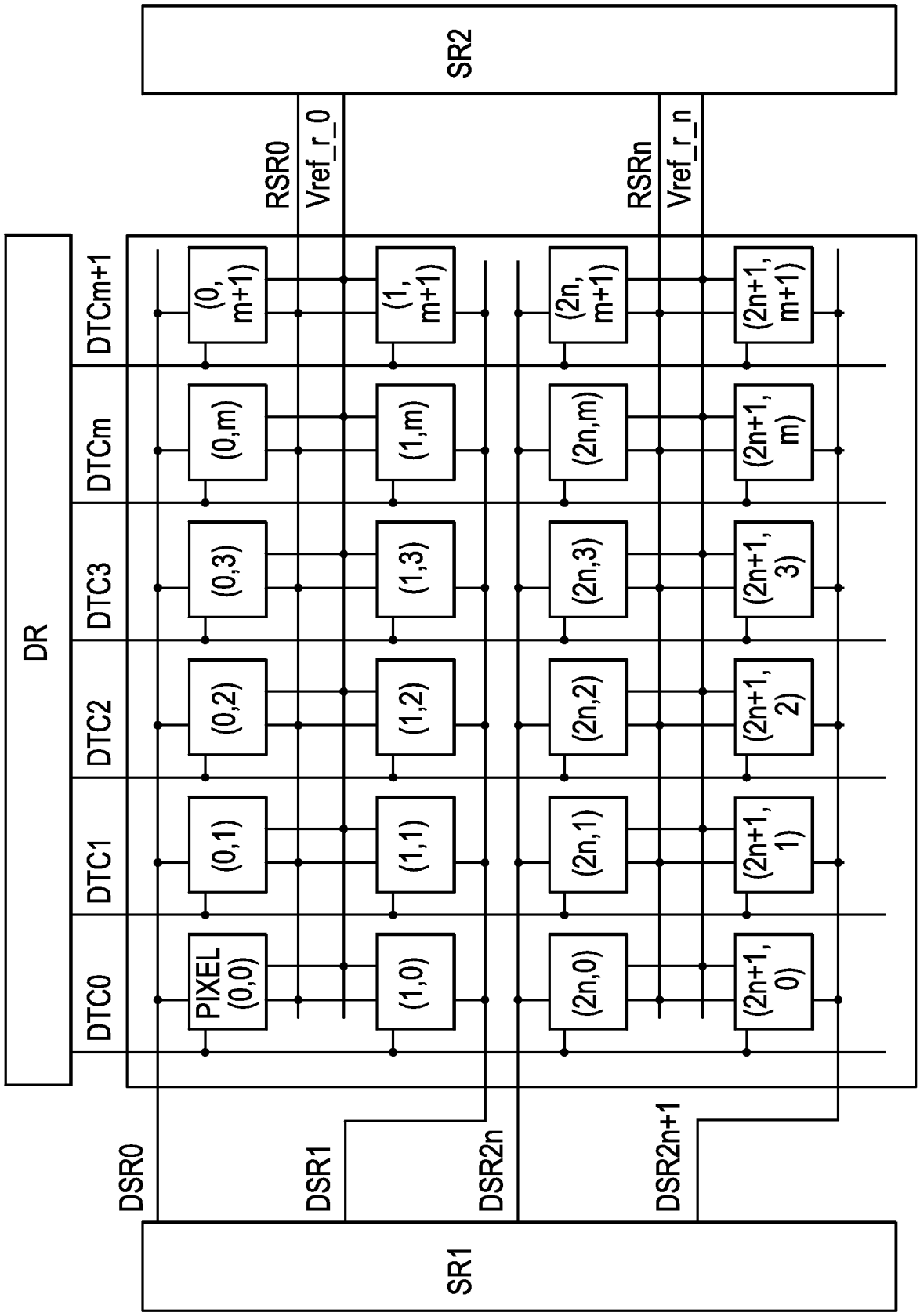

SR2
RSR0
Vref_r_0
RSRn
Vref_r_n
DR
DTC0
DTC1
DTC2
DTC3
DTCm
DTCm+1
PIXEL (0,0)
(0,1)
(0,2)
(0,3)
(0,m)
(0, m+1)
(1,0)
(1,1)
(1,2)
(1,3)
(1,m)
(1, m+1)
(2n,0)
(2n,1)
(2n,2)
(2n,3)
(2n,m)
(2n, m+1)
(2n+1, 0)
(2n+1, 1)
(2n+1, 2)
(2n+1, 3)
(2n+1, m)
(2n+1, m+1)
DSR0
DSR1
DSR2n
DSR2n+1
SR1

FIG. 1B

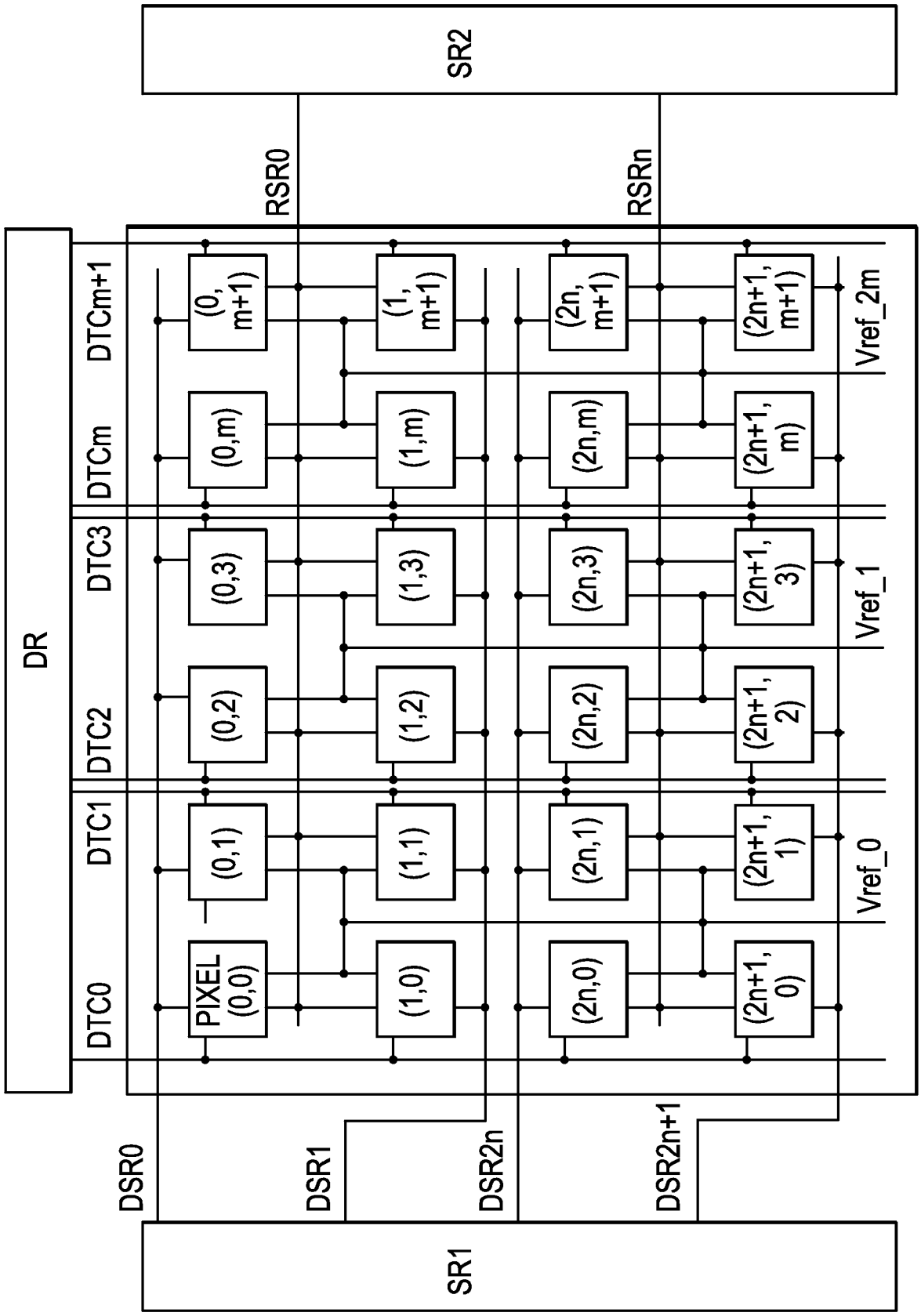

SR2
RSR0
RSRn
DR
DTCm+1
DTCm
DTC3
DTC2
DTC1
DTC0
(0, m+1)
(1, m+1)
(2n, m+1)
(2n+1, m+1)
(0,m)
(1,m)
(2n,m)
(2n+1, m)
(0,3)
(1,3)
(2n,3)
(2n+1, 3)
(0,2)
(1,2)
(2n,2)
(2n+1, 2)
(0,1)
(1,1)
(2n,1)
(2n+1, 1)
PIXEL (0,0)
(1,0)
(2n,0)
(2n+1, 0)
Vref_2m
Vref_1
Vref_0
DSR0
DSR1
DSR2n
DSR2n+1
SR1

FIG. 2

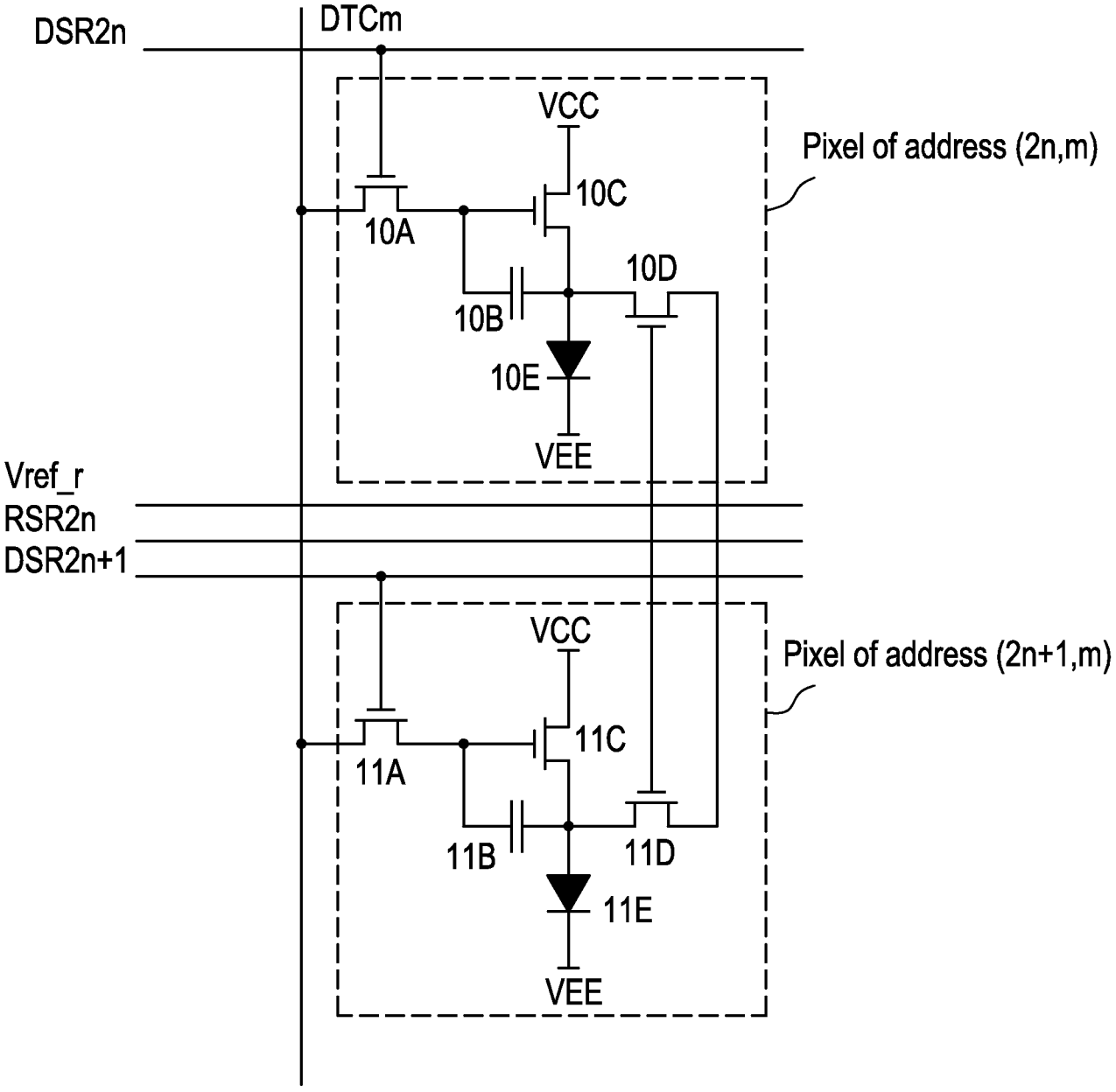

DSR2n
DTCm
VCC
Pixel of address (2n,m)
10C
10A
10D
10B
10E
VEE
Vref_r
RSR2n
DSR2n+1
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 3

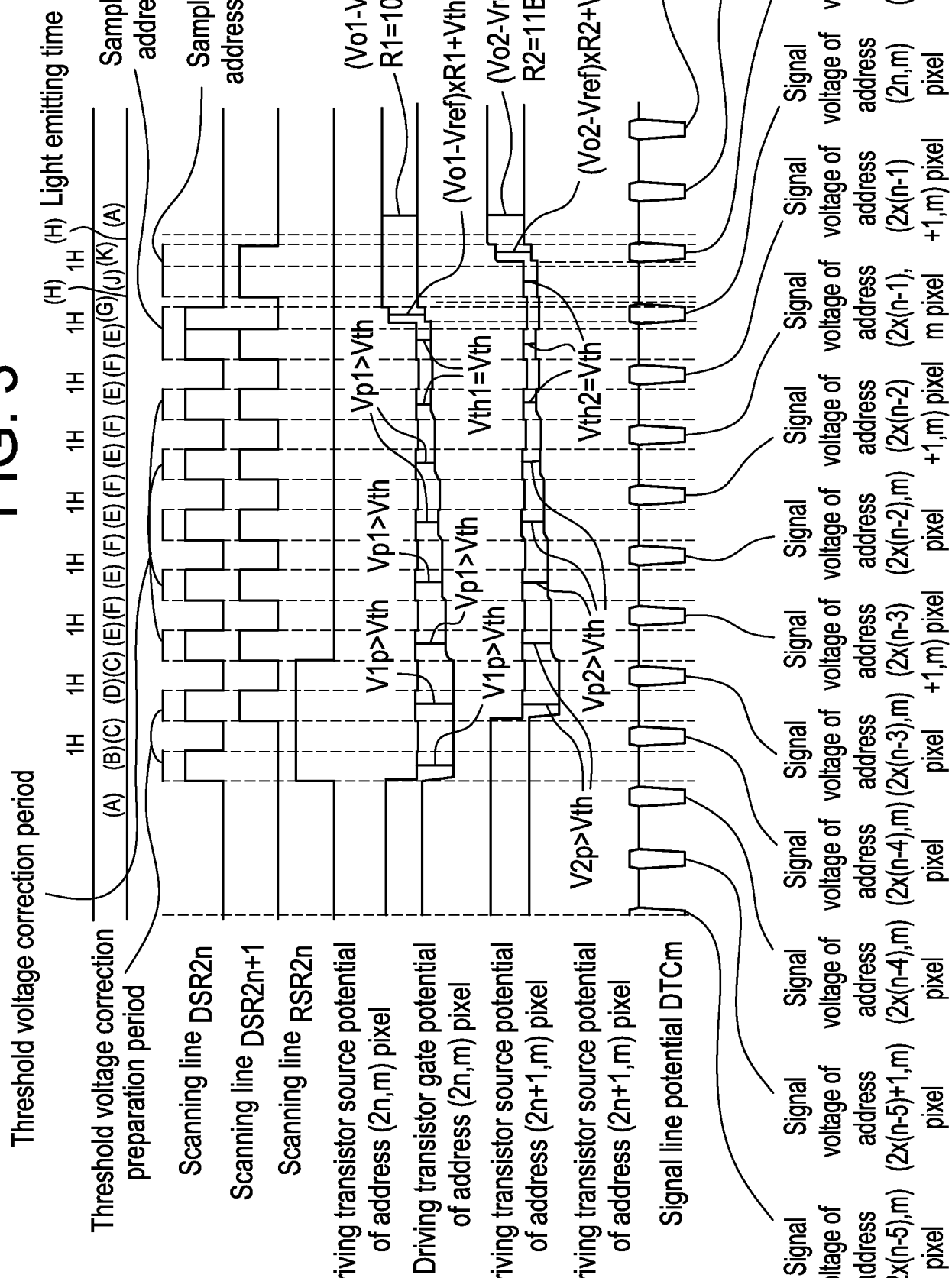

Threshold voltage correction period
1H
(A)
1H
(B)(C)
1H
(D)(C)
1H
(E)(F)
1H
(E)
1H
(F)
1H
(E)
1H
(F)
1H
(E)
1H
(G)/(J)
(H)
1H
(K)/
(H)
1H
(A)
Light emitting time
Sampling period of address (2n,m) pixel
Sampling period of address (2n+1,m) pixel
Threshold voltage correction preparation period
Scanning line DSR2n
Scanning line DSR2n+1
Scanning line RSR2n
Driving transistor source potential of address (2n,m) pixel
Driving transistor gate potential of address (2n,m) pixel
Driving transistor source potential of address (2n+1,m) pixel
Driving transistor source potential of address (2n+1,m) pixel
Signal line potential DTCm
V1p>Vth
V1p>Vth
V1p>Vth
V1p>Vth
V2p>Vth
V2p>Vth
Vp1>Vth
Vp1>Vth
Vth1=Vth
Vth2=Vth
(Vo1-Vref)xR1+Vth1
R1=10B/(10B+10C)
(Vo1-Vref)xR1+Vth1
(Vo2-Vref)xR2+Vth2
R2=11B/(11B+11C)
(Vo2-Vref)xR2+Vth2
Signal voltage of address (2x(n+1)+1,m) pixel
Signal voltage of address (2x(n-5),m) pixel
Signal voltage of address (2x(n-4),m) pixel
Signal voltage of address (2x(n-4),m) pixel
Signal voltage of address (2x(n-3),m) pixel
Signal voltage of address (2x(n-3),m) pixel
Signal voltage of address (2x(n-2),m) pixel
Signal voltage of address (2x(n-2),m) pixel
Signal voltage of address (2x(n-1),m) pixel
Signal voltage of address (2x(n-1),m) pixel
Signal voltage of address (2n,m) pixel
Signal voltage of address (2n+1,m) pixel

FIG. 4A

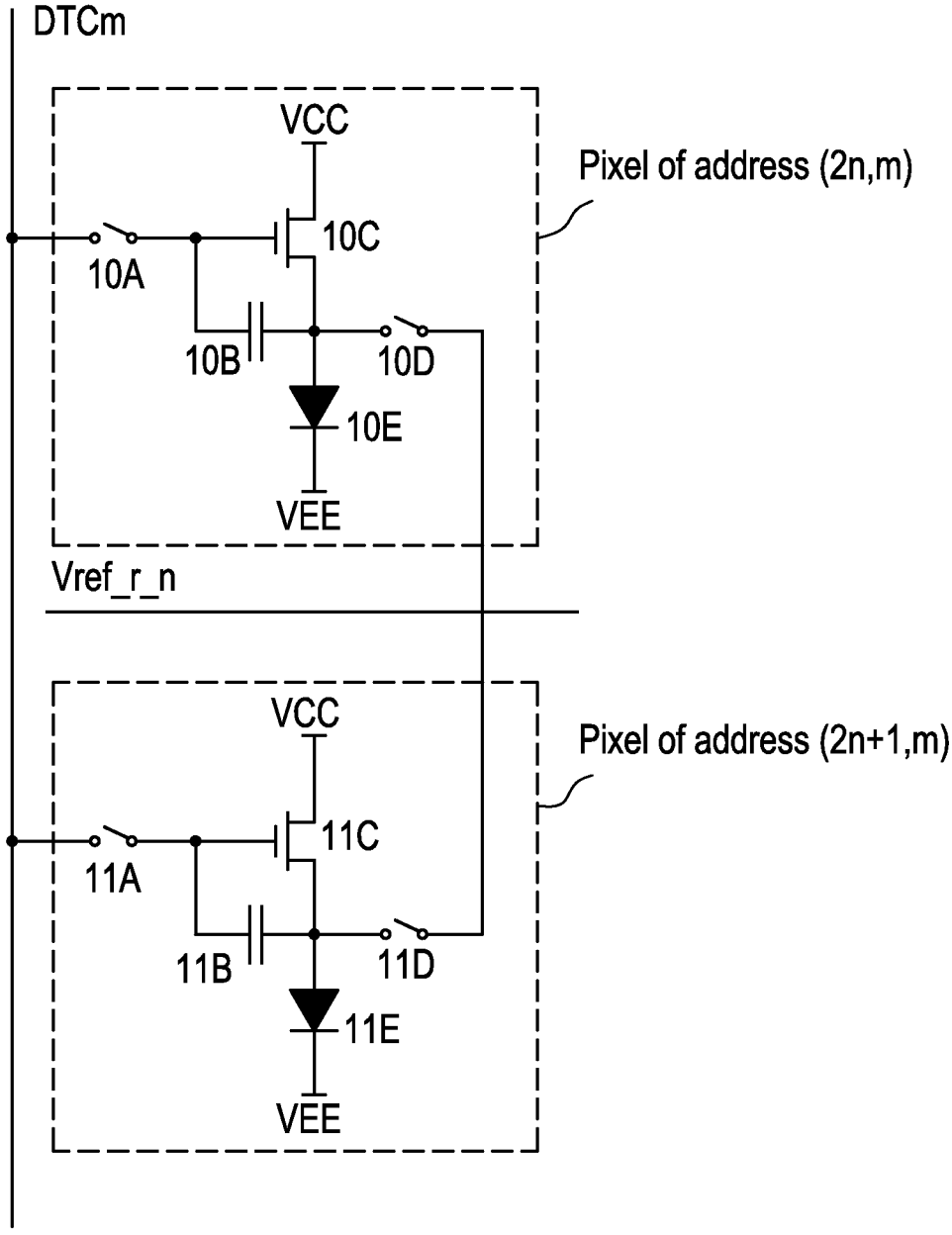

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4B

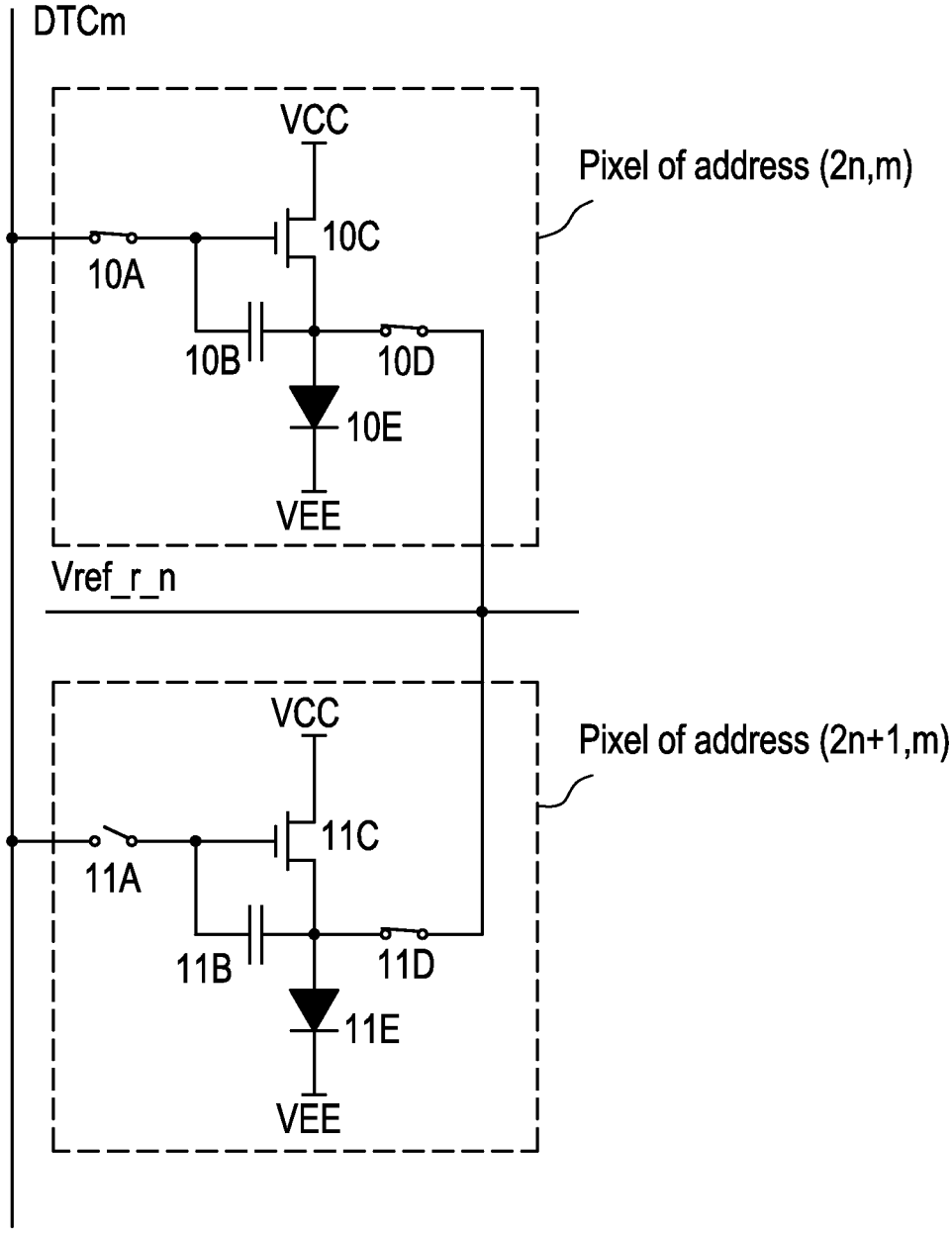

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4C

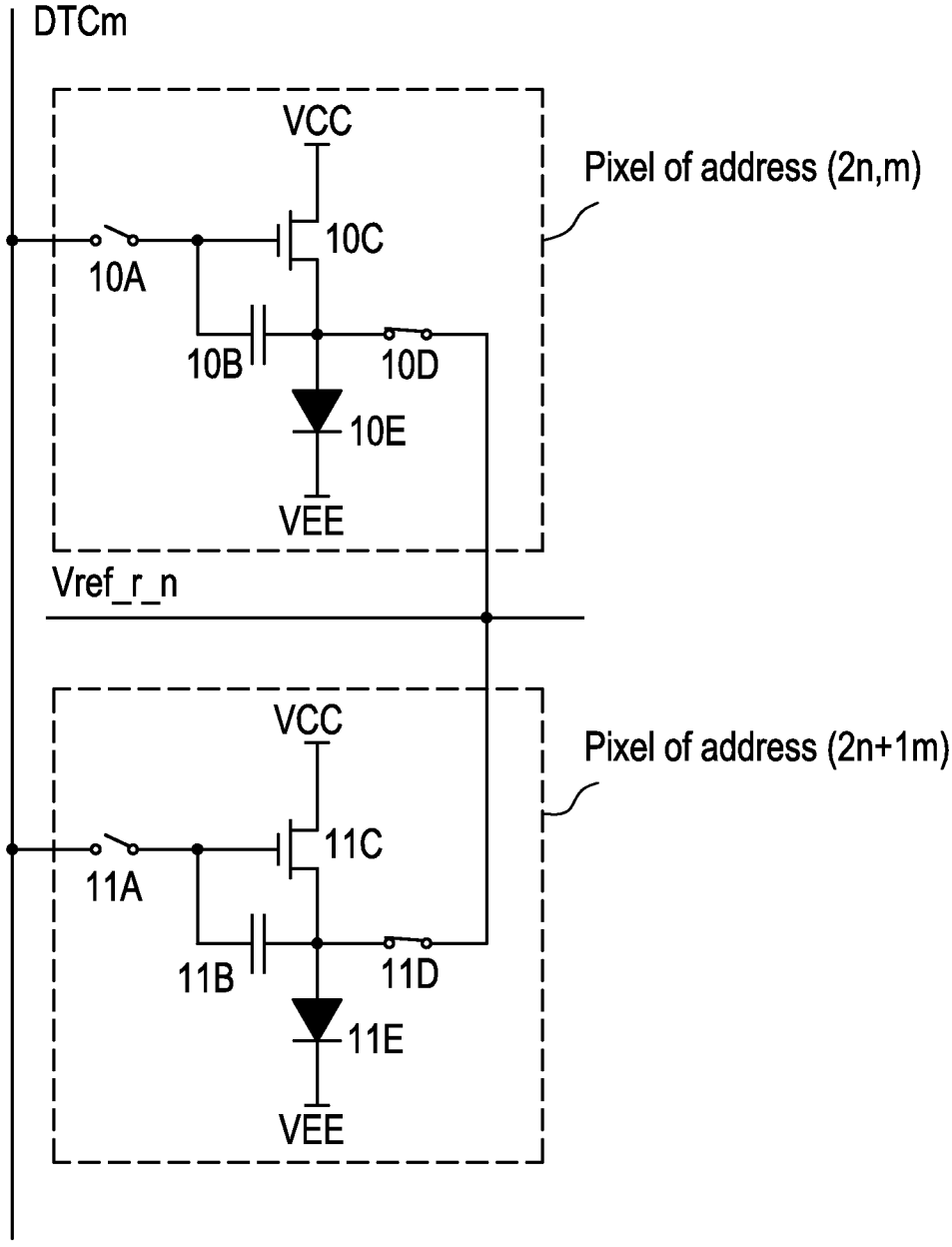

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1m)
11C
11A
11B
11D
11E
VEE

FIG. 4D

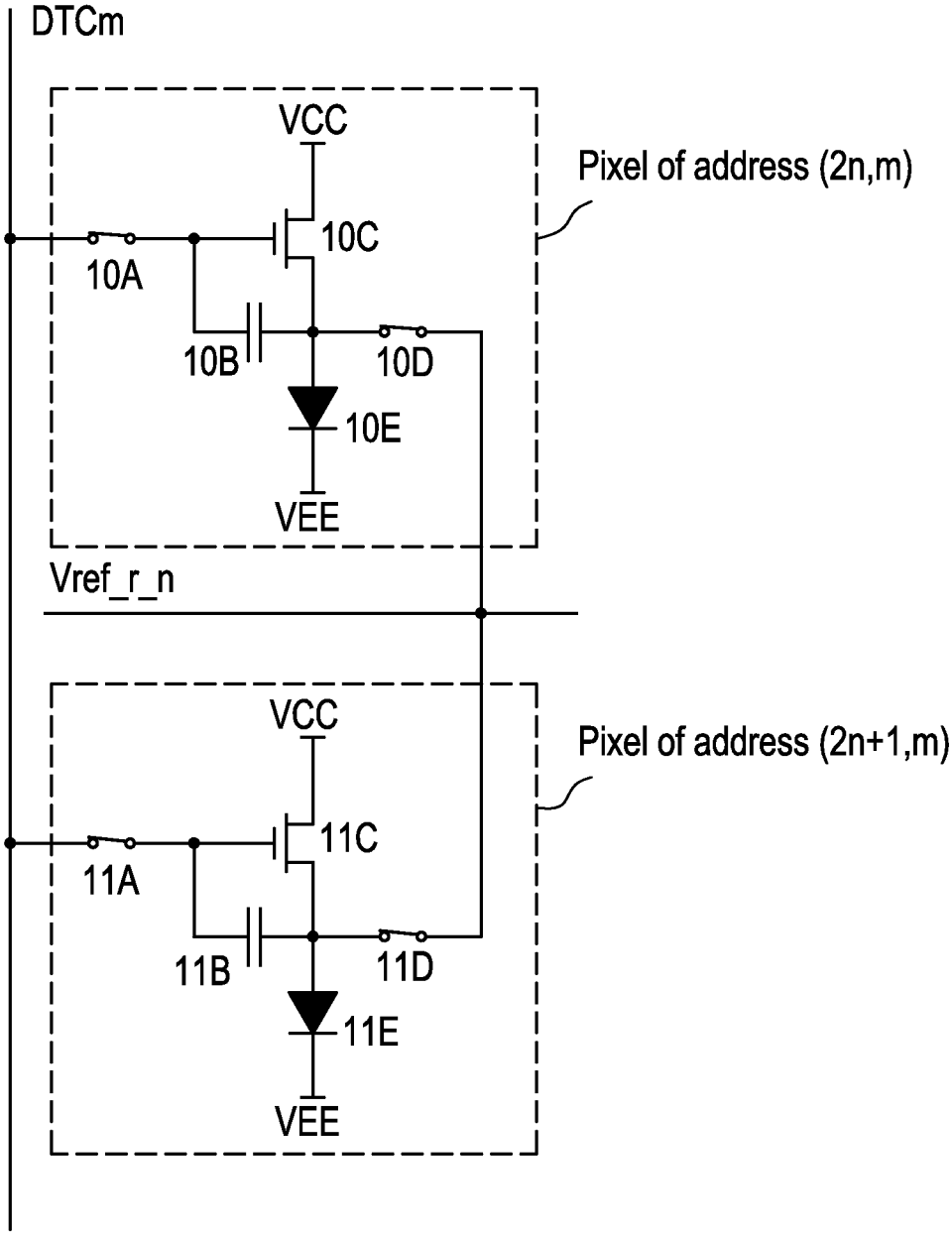

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4E

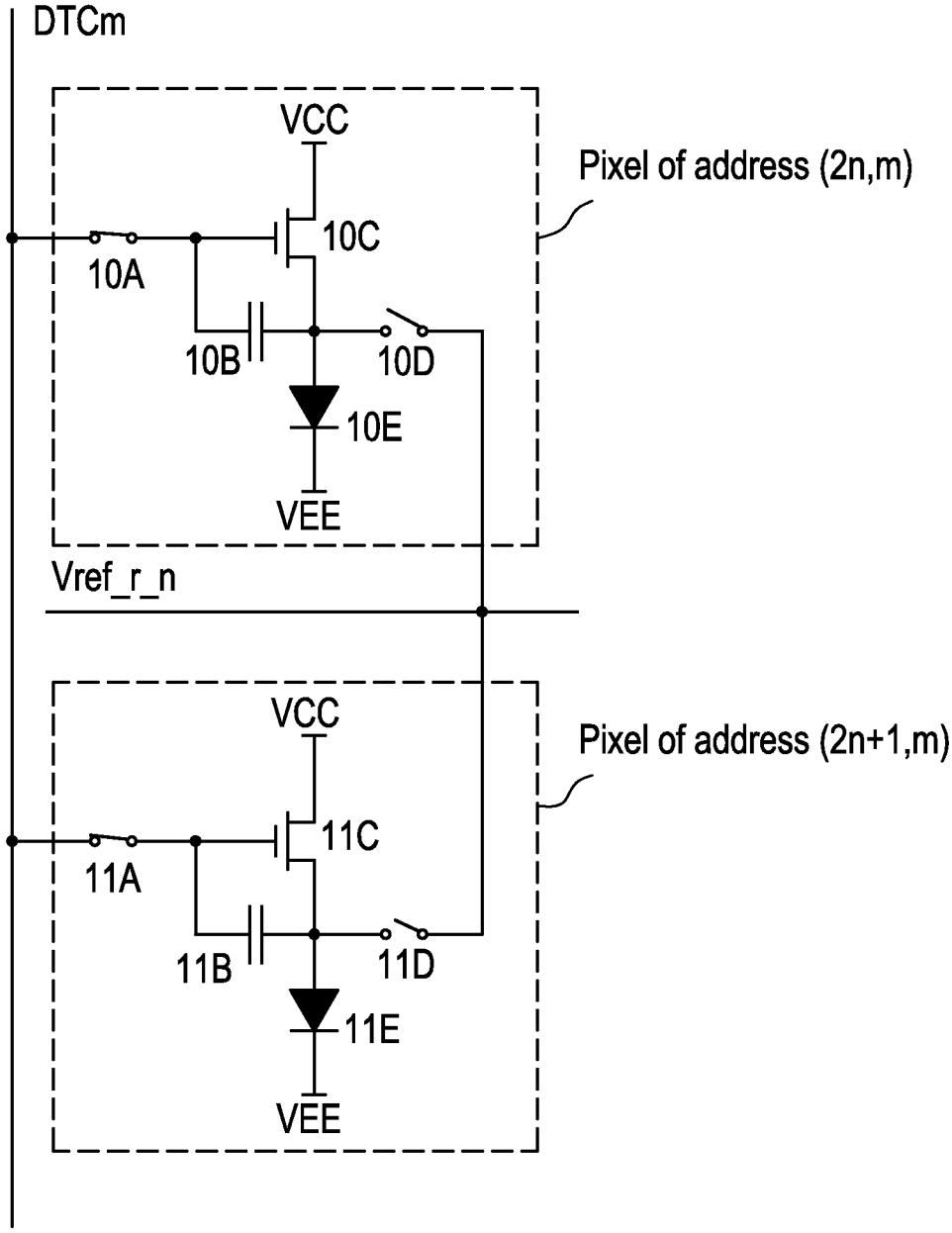

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4F

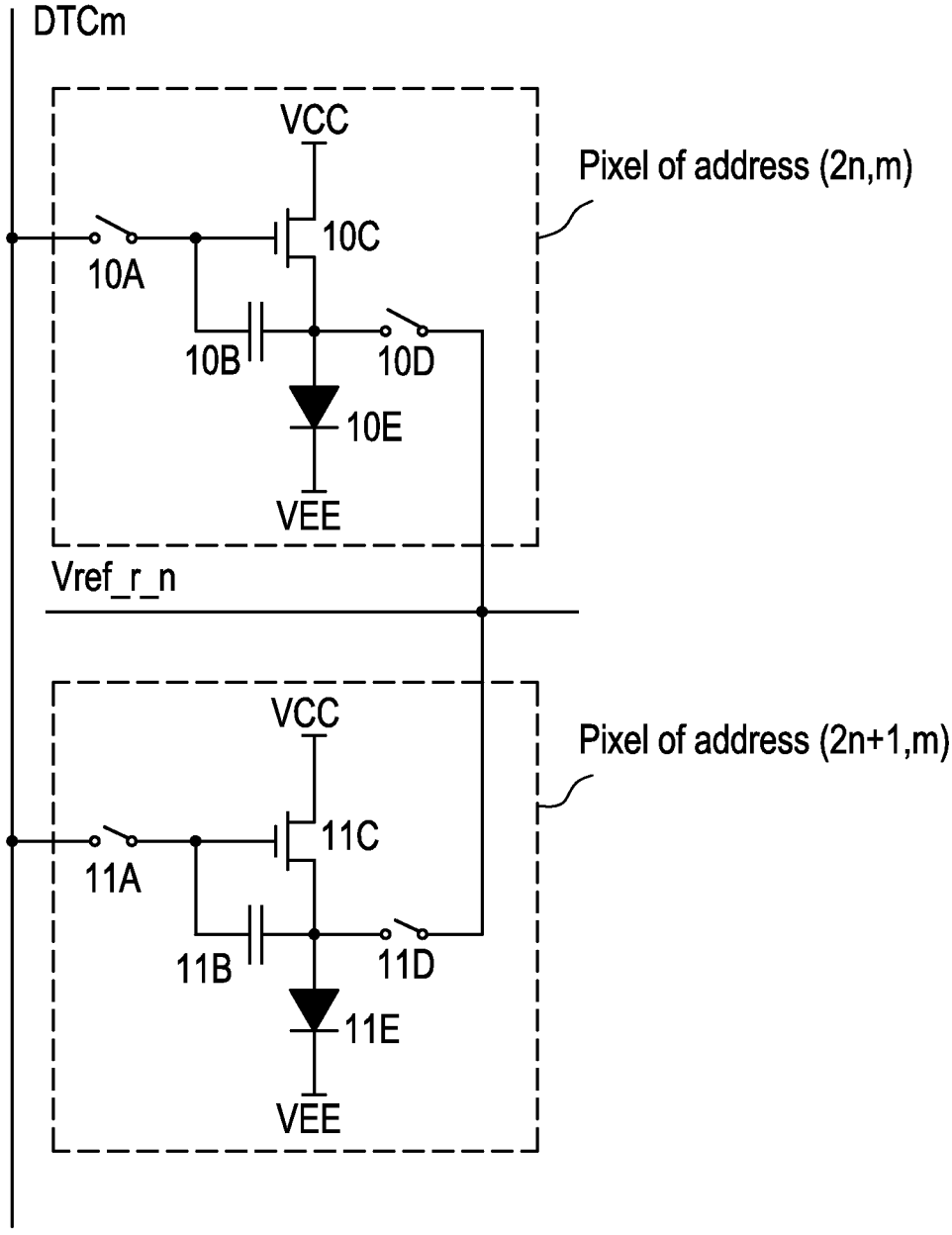

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4G

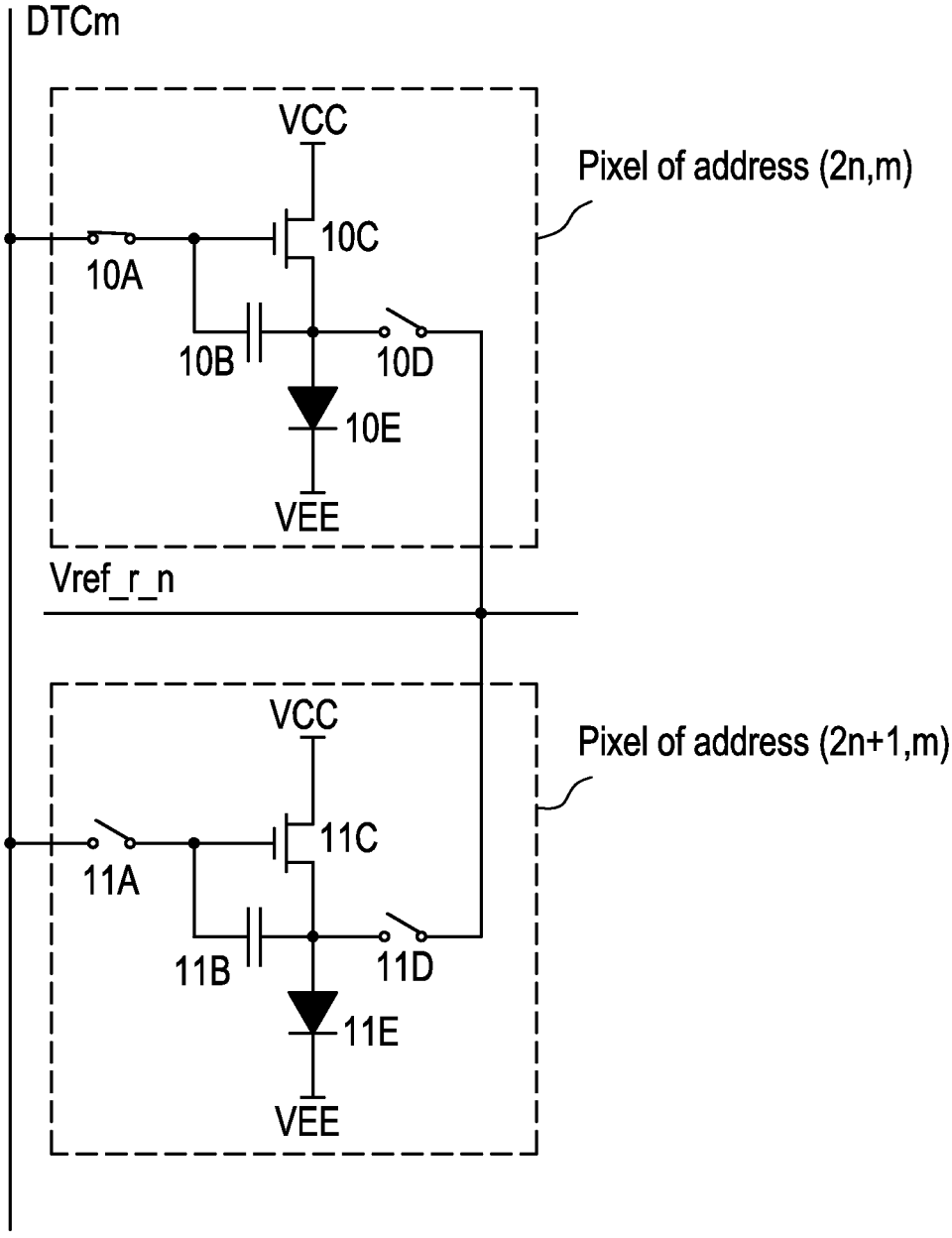

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4H

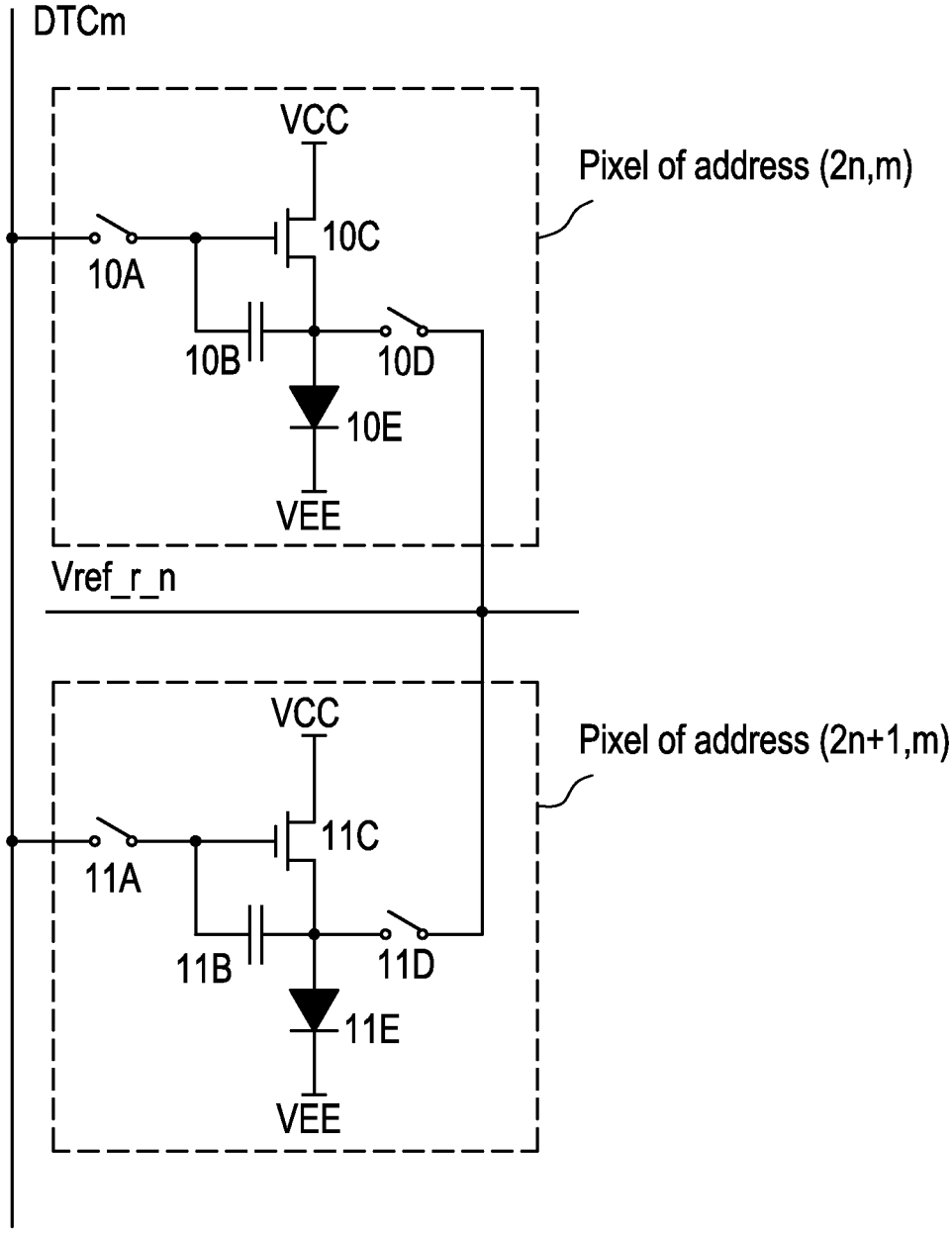

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4J

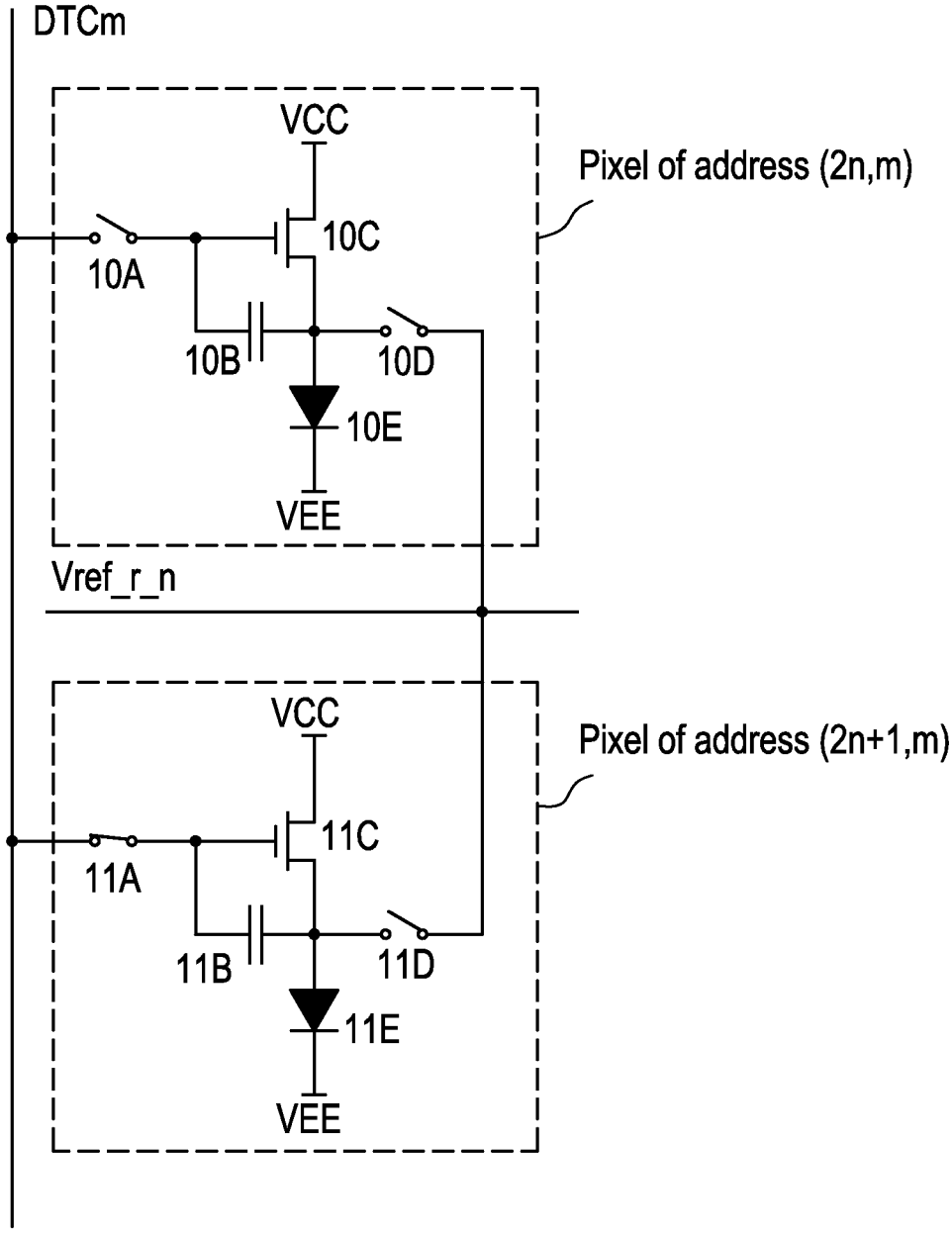

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 4K

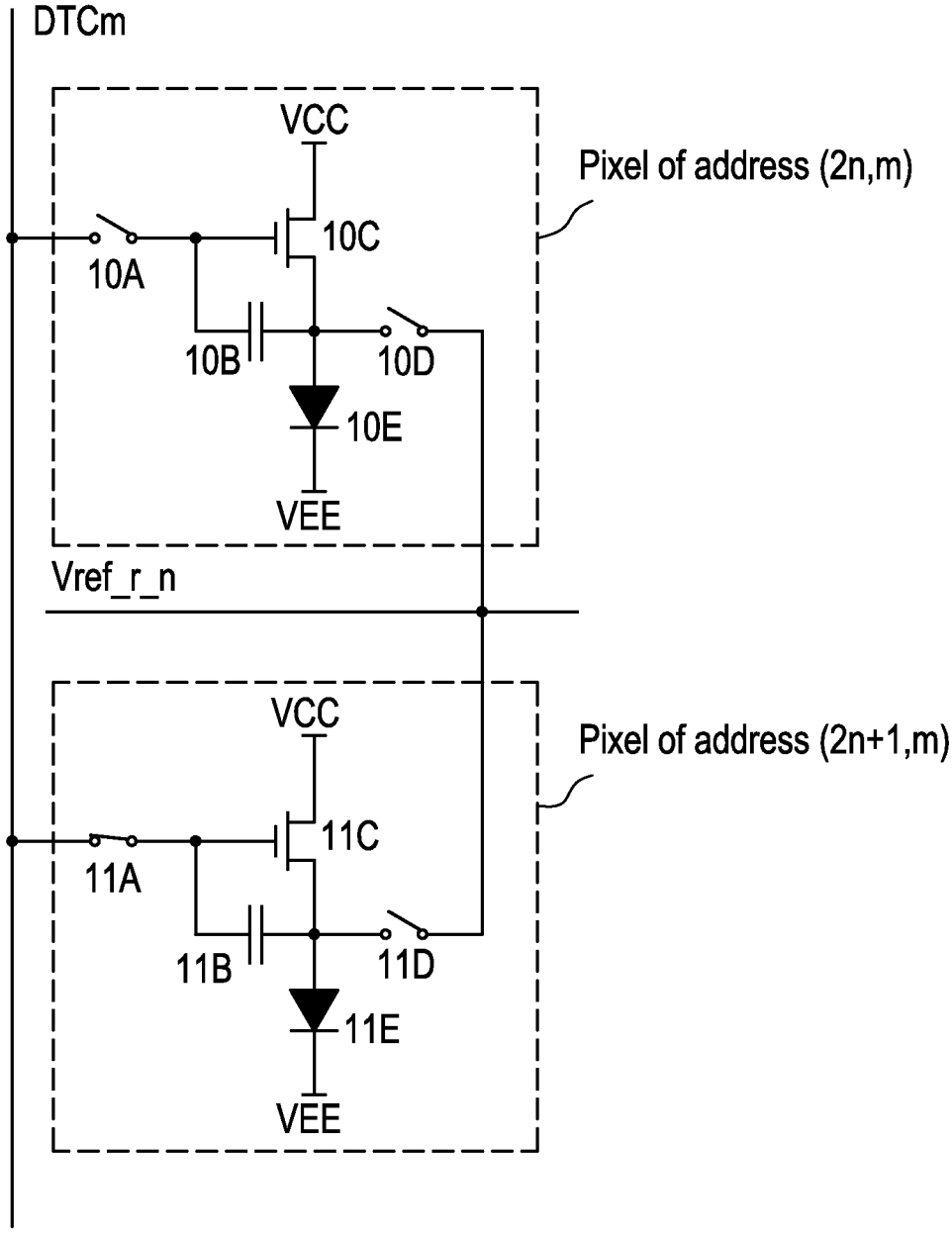

DTCm
VCC
Pixel of address (2n,m)
10C
10A
10B
10D
10E
VEE
Vref_r_n
VCC
Pixel of address (2n+1,m)
11C
11A
11B
11D
11E
VEE

FIG. 5A

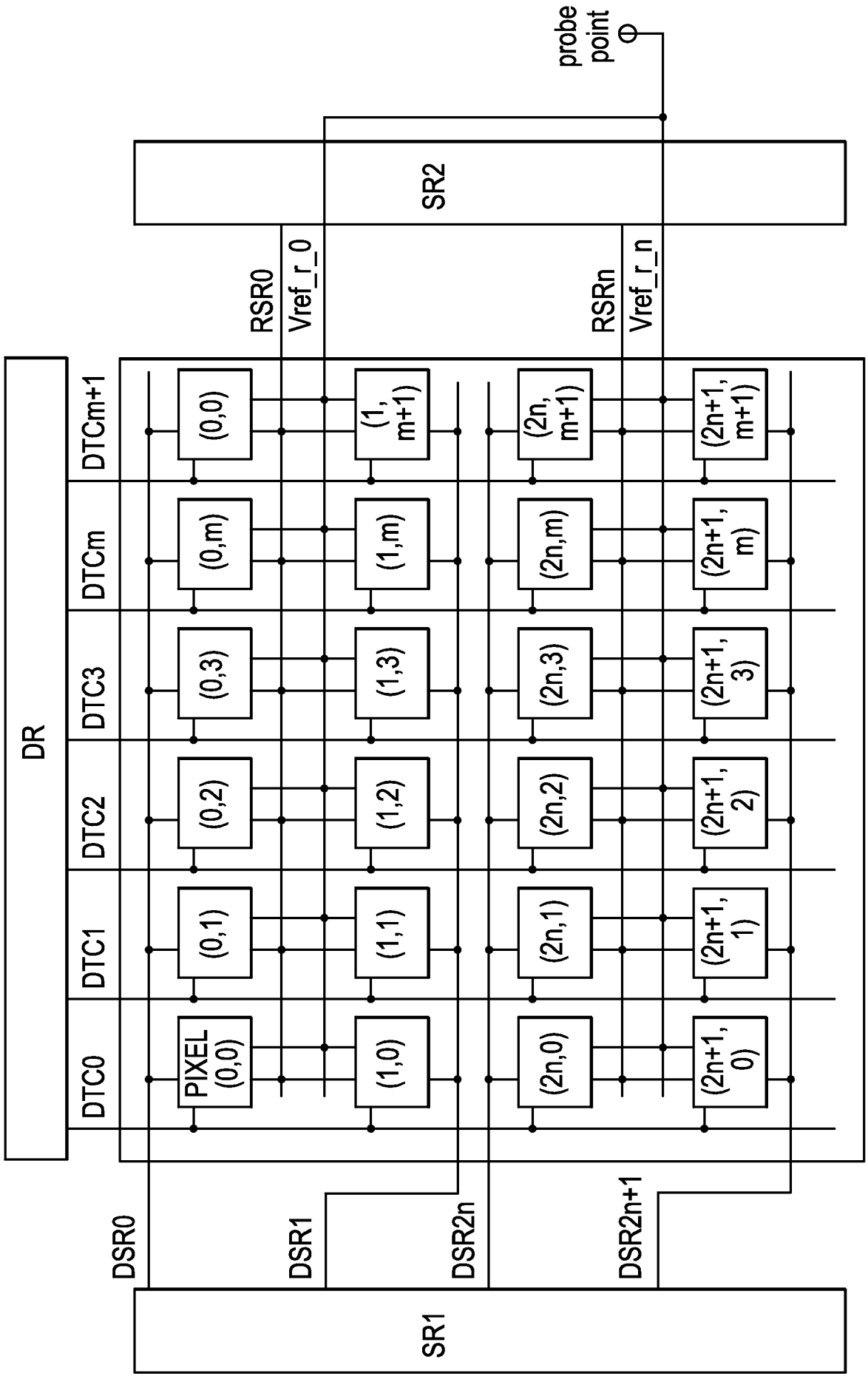
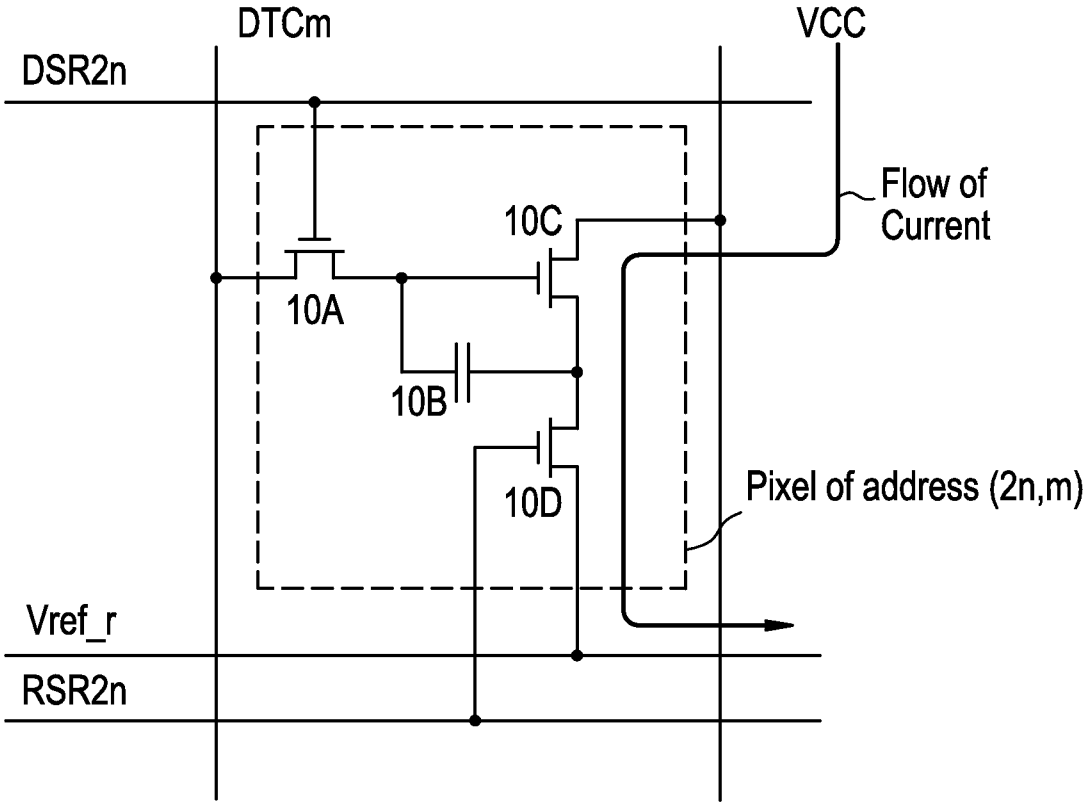

probe point
SR2
RSR0
Vref_r_0
RSRn
Vref_r_n
DR
DTCm+1
DTCm
DTC3
DTC2
DTC1
DTC0
(0,0)
(1, m+1)
(2n, m+1)
(2n+1, m+1)
(0,m)
(1,m)
(2n,m)
(2n+1, m)
(0,3)
(1,3)
(2n,3)
(2n+1, 3)
(0,2)
(1,2)
(2n,2)
(2n+1, 2)
(0,1)
(1,1)
(2n,1)
(2n+1, 1)
PIXEL (0,0)
(1,0)
(2n,0)
(2n+1, 0)
DSR0
DSR1
DSR2n
DSR2n+1
SR1

FIG. 5B


DTCm
VCC
DSR2n
Flow of
Current
10C
10A
10B
10D
Pixel of address (2n,m)
Vref_r
RSR2n

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/055368

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G09G 3/00 (2010.01)
USPC - 345/55
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - G09G 3/00, 30, 32 (2010.01)
USPC - 345/55, 76, 78, 904

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Google Patents, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---- Y	US 2006/0119548 A1 (LAN et al) 08 June 2006 (08.06.2006) entire document	1 ---- 2-8
Y	US 2006/0113919 A1 (CHILDS et al) 01 June 2006 (01.06.2006) entire document	2-8
A	WO 2004/088626 A1 (HECTOR et al) 14 October 2004 (14.10.2004) entire document	1-8
A	US 2009/0109142 A1 (TAKAHARA) 30 April 2009 (30.04.2009) entire document	1-8
A	US 2005/0269959 A1 (UCHINO et al) 08 December 2005 (08.12.2005) entire document	1-8
A	US 7,265,572 B2 (OSADA) 04 September 2007 (04.09.2007) entire document	1-8
A	US 2009/0262258 A1 (TANEDA et al) 22 October 2009 (22.10.2009) entire document	1-8

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2010	23 DEC 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

专利名称(译)	像素电路，显示装置和检查方法		
公开(公告)号	EP2499632A1	公开(公告)日	2012-09-19
申请号	EP2010830537	申请日	2010-11-04
[标]申请(专利权)人(译)	全球OLED TECH		
申请(专利权)人(译)	全球OLED科技有限责任公司		
当前申请(专利权)人(译)	全球OLED科技有限责任公司		
[标]发明人	MAEKAWA YUICHI MIWA KOICHI		
发明人	MAEKAWA, YUICHI MIWA, KOICHI		
IPC分类号	G09G3/00 G09G3/32		
CPC分类号	G09G3/006 G09G3/3233 G09G2300/0842 G09G2310/0251		
优先权	2009257527 2009-11-10 JP		
其他公开文献	EP2499632A4		
外部链接	Espacenet		

摘要(译)

补偿驱动晶体管的阈值电压的变化。在参考信号电压Vref被设置到信号线DTC的时段期间，使驱动晶体管10C的栅极和源极之间的电压等于或大于驱动晶体管10C的阈值电压，并且电压差为参考信号电压Vref和参考电源电压VreCr被充电到保持电容IOB。同时，将所述驱动晶体管10C的源极电压设置为参考电源电压VreCr，以使施加到所述发光元件的电压等于或低于其阈值电压。随后，在保持施加到所述发光元件IOE的电压等于或低于其阈值电压的同时。