



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
18.05.2016 Bulletin 2016/20

(51) Int Cl.:
H01L 51/52 (2006.01) H01L 27/32 (2006.01)

(21) Application number: **14425146.9**

(22) Date of filing: **14.11.2014**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(71) Applicants:
• **E.T.C. S.r.l.**
40129 Bologna BO (IT)
• **Polyera Corporation**
Skokie, IL 60077 (US)

(72) Inventors:
• **Muccini, Michele**
40121 Bologna BO (IT)

• **Generali, Gianluca**
40127 Bologna BO (IT)
• **D'Alpaos, Riccardo**
32041 Auronzo di Cadore BL (IT)
• **Facchetti, Antonio**
Chicago, IL 60640 (US)
• **Hsiao, Chung-Chin**
302 Zhubei City (TW)
• **Lien, Hugh**
351 Toufen Township (TW)

(74) Representative: **Barbaro, Gaetano et al**
Società Italiana Brevetti S.p.A.
Via G. Carducci, 8
20123 Milano (IT)

(54) **Display containing improved pixel architectures**

(57) The invention relates to improved Organic Light Emitting Transistor (OLET) pixel architecture for OLET based displays.

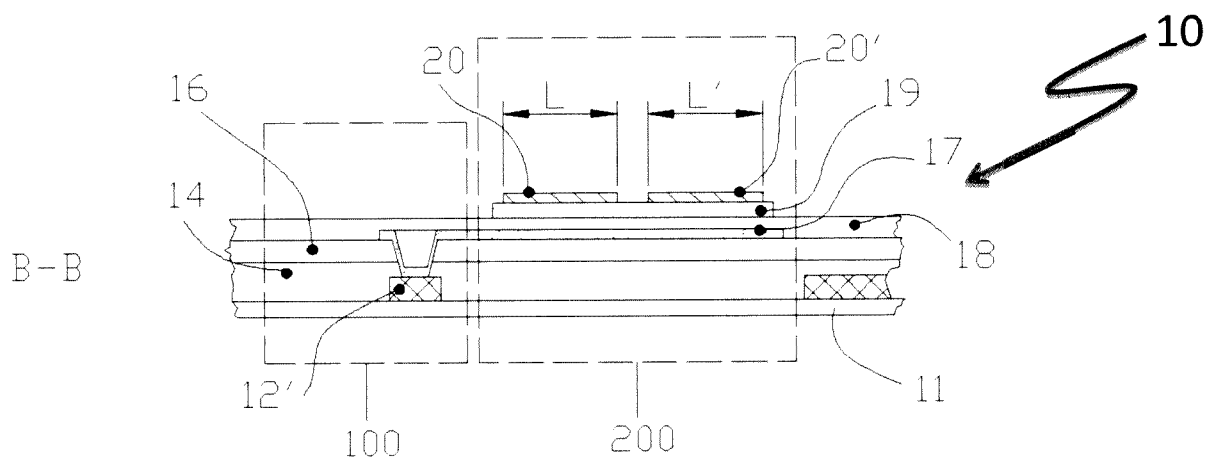


FIG. 2B

Description

[0001] The present invention relates to improved Organic Light Emitting Transistor (OLET) pixel architecture for OLET based displays.

[0002] OLET light emission structures are a recent type of light emitting devices, that is attracting increasing attention with respect to other devices such as Organic Light Emitting Diode (OLED) due to their ease of manufacturing, highest brightness and other improved features. More details on those aspects could be found in the 2010 article from Muccini et al, "Organic light-emitting transistors with an efficiency that outperforms the equivalent light-emitting diodes", published in Nature Materials, Volume: 9, Pages: 496-503.

[0003] More information on the relevant development of OLET structures may also be found in US patent US 8,497,501, European patent application 2,737,559, European patent 2,574,219, European patent 2,583,329, and European patent application 2,786,437.

[0004] All the above-identified patent documents are related to OLET structures as such, i.e. light emitting devices, but not to specific architectures and solutions for making display pixels.

[0005] This aspect is instead addressed by US patent application 2013/0240842, disclosing a vertical OLET coupled with an organic thin film transistor.

[0006] The purpose of the present invention is to provide a new pixel architecture with a TFT as a switching transistor of an OLET capable to provide optimized performances. In particular the inventors have found that in the vast and wide scenario of suitable OLET light sources, a well-defined and limited OLET subcategory provides distinctive advantages when coupled with a TFT for making a display pixel and in a first aspect thereof consist in a display containing an array of pixels, wherein each pixel comprises at least a first driving transistor (100) and at least a second light emitting transistor (200) mounted on a common substrate (11), wherein the first switching transistor (100) comprises the following elements:

- a first source and a first drain electrodes (12, 12') separated and connected to each other by a semiconductor layer (13)
- a first dielectric layer (14)
- at least one first gate electrode (15)

[0007] The second light emitting transistor (200) comprises the following elements:

- a second gate electrode (17)
- a second dielectric layer (18)
- a light emitting channel layer (19)
- a second source and a second drain electrodes (20, 20'), respectively having widths w_s and w_d ,

wherein the second gate electrode (17) is in electrical

contact with at least one of the first source and first drain electrodes (12, 12') and

characterized in that at least one of the second source and second drain electrodes (20, 20') vertically overlaps with the second gate electrode (17) by at least 5 μm (L , L') and that said second source and second drain electrodes are horizontally separated by at least 2 μm .

[0008] The term vertically overlaps by at least 5 μm means that these elements are at least partly vertically aligned, i.e. the projection of the second source/drain electrodes onto the second gate electrode plane has a certain length in common with the second gate electrode (at least 5 μm , and preferably being equal or less than 150 μm).

[0009] Similarly, horizontally separated means that the elements are not vertically aligned and moreover that their projection into a common plane will have a minimal distance (at least 2 μm , and preferably being equal or less than 50 μm).

A display pixel according to the present invention is different from what shown in US patent application 2013/0240842 as such structure requires an almost complete overlap between the source and the drain electrodes, with a charge transport and recombination mechanism that is essentially the opposite with respect to the one used by the second transistor in the present invention. A vertical light emitting transistor, such as the one described in 2013/0240842, when coupled with a switching TFT for making a pixel will suffer from the limitations related to the vertical charge transport that occurs across the stack of organic layers forming the channel of the light emitting transistors, that is orders of magnitude lower than that occurring in the plane of the films under the driving force of the lateral field effect.

As mentioned, one of the key points of the pixel architectures according to the present invention is the vertical overlap of at least one of the source and drain electrodes with the OLET gate electrodes, and the horizontal separation between the source and drain electrodes, as this ensures from one hand the establishment of a virtual capacity that allows a better and simpler driving of the OLET itself, and from the other hand the lateral charge transport between the source and the drain electrodes, which allows better electrical device characteristics.

[0010] It is also important to underline in this regards that the OLET Pixel structures, i.e. the second light emitting transistor structures selected by the inventors are a well-defined subset of OLET structures, as for example OLET such as the ones shown in US patent 8,664,648, international patent application WO 2011/147523, US patent 8,758,649, US patent application US 2014/117317, International patent application WO 2010/049871, to cite a few, in which there is no vertical overlap of the OLET gate with one of its source and drain electrodes, as well as the so called vertical OLET, such as the one described in the already mentioned patent application US 2013/0240842 are outside the scope and not encompassed by the present invention.

[0011] It is also important to underline that OLET structures showing such vertical overlap of source drain contacts, do not provide information about the useful intervals, as well as other constitutional characteristics such as the useful range of the second source and second drain horizontal separation, that allows to make an improved display pixel by coupling such OLET with a TFT by contacting its gate with one of the first transistor source or drain electrodes.

[0012] The invention will be further described with the help of the following figures where:

- Figure 1 is a top view of a first preferred embodiment of a display pixel according to the present invention.
- Figure 2A is a cross section view of the display pixel illustrated in Figure 1 along line A-A, whereas Figure 2B is a cross section view of the very same display pixel along line B-B.
- Figure 3 is a cross section view of a display pixel according to another embodiment of the present invention along line B-B, wherein at least one of the second source and second drain electrodes of the second light emitting transistor is on top of the light emitting channel and is in contact with the second dielectric layer.
- Figure 4 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which both the second source and second drain electrodes of the second light emitting transistor lie on the second dielectric layer and are positioned at the bottom of the light emitting channel layer.
- Figure 5 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which one of the second source and second drain electrodes of the second light emitting transistor is positioned at the bottom and the other is positioned at the top of the light emitting channel layer.
- Figure 6 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which the light emitting channel layer comprises a stack of a plurality n of organic semiconductor layers.
- Figure 7 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which one of the second source and second drain electrodes of the second light emitting transistor is positioned on top and the other is positioned within the stack of a plurality n of organic semiconductor layers.
- Figure 8 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which the light emitting channel layer comprises a stack of a plurality n of organic semiconductor layers, the second dielectric layer is deposited over the light emitting channel layer, the second gate electrode is positioned on top of

the second dielectric layer and the second source and second drain electrodes are positioned at the bottom of the light emitting channel layer.

- Figure 9 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which the light emitting channel layer comprises a stack of a plurality n of organic semiconductor layers, the second dielectric layer is deposited over the light emitting channel layer, the second gate electrode is positioned on top of the second dielectric layer, the second source and second drain electrodes are in contact with different organic semiconductor layers within the light emitting channel layer (as illustrated, one of the second source and second drain electrodes is in contact with the first organic semiconductor layer while the other of the second source and second drain electrodes is in contact with the nth organic semiconductor layer).
- Figure 10 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which the second light emitting transistor comprises more than two second source and drain electrodes alternately disposed on the light emitting channel layer (e.g., source / drain / source or drain / source / drain in the illustrated configuration).
- Figure 11 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which the second light emitting transistor comprises a reflecting layer R positioned below the light emitting channel layer.
- Figure 12 is a cross section view of a display pixel according to yet another embodiment of the present invention along line B-B, in which the second light emitting transistor comprises an insulating layer "i" deposited over the light emitting channel layer and the second source and second drain electrodes, and a reflecting layer R positioned on top of the insulating layer "i".
- Figure 13 is a cross section view of a display pixel according to yet another embodiment of the present invention along line A-A, wherein the first switching transistor is configured such that the first drain and first source electrodes are not completely coplanar with the semiconductor layer. In the configuration illustrated, one of the first drain and first source electrodes lies on the semiconductor layer while the other of the first drain and first source electrodes is in contact with both the semiconductor layer and the substrate.

In the figures the dimensions and dimensional ratios of some elements may not be to scale, but in some cases have been altered in order to improve the drawings readability and comprehension, such as for instance layer thicknesses and source-drain distances and thicknesses. Moreover just one exemplary top view has been

shown, while all other figures are intended to show specific features that are characteristic of particular embodiments, which are more clearly and efficiently illustrated by cross section views.

As used herein, a cross section according to line A-A refers to a cross section in the upper part of the display pixel according to the present invention, or, more precisely, to the part of the display pixel showing a first source electrode, a first drain electrode and a first gate electrode; while a cross section according to line B-B refers to a cross section showing the lower part of the present display pixel, or, more precisely, to the part of the display pixel showing the connection between the second gate of the second light emitting transistor and the first source/drain contact of the first switching transistor. Figure 1 is a top view showing the main components of a display pixel 10 according to the present invention. The display pixel 10 comprises a first transistor the electrodes of which are the layers 12, 12' and a third one (not shown), and a second transistor, that is a light emitting transistor, the electrodes of which are the layers 20, 20' and 17. In the top view of figure 1 it is shown in particular a common substrate 11 over which the first (switching) transistor and the second (light emitting) transistor are realized, first source and first drain electrodes 12 and 12' respectively of the first transistor, second source and second drain electrodes 20 and 20' respectively of the second transistor, a first gate electrode (not observable from this view) of the first transistor, a second gate electrode 17 of the second transistor, a semiconductor layer 13 coupling the first source and first drain electrodes 12 and 12', and a light emitting channel 19 of the second transistor. Either the first source electrode 12 or the first drain electrode 12' of the first transistor is connected to an address line DATA of the display pixel, and the first gate electrode 15 is connected to an enable line SCAN of the display pixel.

As outlined above, the relative positions and connections of these elements with the ones not indicated in Figure 1 (because they are almost completely overlapped along the illustrated perspective), are instead more clearly observable in the cross section views along lines A-A and B-B.

Figure 2A shows a cross section view along line A-A of the display pixel 10.

In particular, Figure 2A shows the vertical structure of the first switching transistor 100 with its constituting elements:

- First source and first drain electrodes 12 and 12'
- Semiconductor layer 13
- First dielectric layer 14
- First gate electrode 15

and the vertical structure of the second light emitting transistor 200 with its constituting elements:

- Second gate electrode 17

- Second dielectric layer 18
- Light emitting channel layer 19
- Second source and second drain electrodes 20 and 20'.

In the cited figure there is also an insulating layer 16 over which the second gate electrode 17 of the second transistor is formed.

The first transistor is functionally coupled with the second transistor so that, when a voltage sufficient to turn on the first transistor is applied at the enable line SCAN, the light emitting transistor is addressed with the voltage available in that moment at the address line DATA. Figure 2B shows a cross section view along line B-B of the display pixel 10 and indicates the connection between the first switching transistor 100 and the second light emitting transistor 200, via the second gate electrode 17 which is in electrical contact with element 12' (first source or first drain electrode).

The display pixel shown in figures 1, 2A and 2B is realized according to a preferred embodiment where the second source and second drain electrodes 20, 20' are horizontally (or laterally) separated (preferably at a distance between at least 2 μm and 50 μm), and the respective entirety of each of the second source and second drain electrodes 20, 20' overlaps vertically with (different parts of) the second gate electrode 17.

However, the invention is not limited to such an embodiment. For example, in certain alternative embodiments, only one of the second source and second drain electrodes needs to overlap vertically with the second gate electrode. In certain embodiments, only a portion (and not the entirety) of the second source and/or second drain electrode(s) may overlap vertically with the second gate electrode. Generally, the second drain and second source electrodes have dimensions and are arranged such that at least one of them overlaps vertically with the second gate electrode for a length of at least 5 μm . Preferably such overlapping length is between 5 μm and 150 μm .

[0013] Also, figures 1, 2A and 2B show a display pixel in which the light emitting channel layer 19 comprises a single organic semiconductor layer, with the second source and second drain electrodes both positioned on top of the light emitting channel layer 19. In operation, the light emitting channel layer 19 can be unipolar or ambipolar.

[0014] With respect to the first transistor, in the embodiment shown in figures 1, 2A and 2B, the semiconductor layer 13 is realized on the same substrate layer 11 on which the first source and first drain electrodes 12, 12' are formed (i.e., the first source and first drain electrodes 12, 12' are co-planar with the semiconductor layer 13), and the first dielectric layer 14 is formed on the substrate 11 over the first source and first drain electrodes 12, 12' and the semiconductor layer 13. The first gate electrode 15 is then formed on top of the first dielectric layer 14 above the semiconductor layer 13. In preferred

embodiments, the first gate electrode 15 is dimensioned to overlap the semiconductor layer 13 completely. This is because the semiconductor layer often is composed of an air-sensitive metal oxide or organic compound; accordingly, a top-gate configuration and the use of a large gate electrode would protect the semiconductor layer from air exposure. Nevertheless, it is also possible to fabricate the first transistor in other configurations. For example, an alternative embodiment of the first transistor can have a top-contact bottom-gate architecture, where both the first source electrode 12 and the first drain electrode 12' are formed on top of the semiconductor layer 13 and the first gate electrode 15 is formed below the semiconductor layer 13.

[0015] Regardless of the relative arrangements of the electrodes 12, 12' and 15, the first transistor can be encapsulated by one or more additional insulating layers. Referring to figure 2A, an overlying insulating layer 16 is formed over the first transistor. More specifically, this insulating layer 16 is deposited on top of the first dielectric layer 14 over the first gate electrode 15 (or in alternative embodiments, not shown, over the first source and first drain electrodes). Referring to figure 2B, a via hole is formed through both the insulating layer 16 and the first dielectric layer 14 to provide access to element 12' (the first source or first drain electrode), and a via is formed by either filling the via hole or lining the sidewalls of the via hole with a conductive material and is in electrical contact with the second gate electrode 17, which is formed on the insulating layer 16. The via, therefore, electrically connects the first transistor 100 and the second transistor 200, by providing electrical contact between element 12' (the first source or first drain electrode) and the second gate electrode 17. More specifically, the via hole can be V-shaped with non-vertical sidewalls. This helps to assure film continuity when the conductive material is deposited to form the via. The via hole can be generated via photolithography; specifically, with the use of a sequence of masks with increasing apertures.

[0016] In an even more preferred embodiment, the width of the second source electrode (ws) and the width of the second drain electrode (wd) may fulfill the following relationship:

$$1 \leq \text{Max}(wd, ws) / \text{Min}(wd, ws) \leq 25$$

and even more preferably

$$1 \leq \text{Max}(wd, ws) / \text{Min}(wd, ws) \leq 10$$

It is clearly observable that in the embodiment shown in figures 1, 2A, 2B such ratio is 1.

Although the embodiments illustrated in figures 1, 2A, 2B are preferred, the display pixels according to the present

invention are not limited thereto.

Other alternative embodiments of the display pixels according to the present invention are shown in figures 3 to 14. The same elements in the various figures are labeled with the same reference numerals.

A cross section along the line B-B of a display pixel according to another embodiment of the present invention is shown in Fig. 3. According to this embodiment, the second source and second drain electrodes 20 and 20' of the second (light emitting) transistor are formed over the light emitting channel layer 19 and are also in contact with the second dielectric layer 18.

Another embodiment of a display pixel of the present invention is illustrated in Fig. 4, which shows its cross section along the line B-B. According to this embodiment, the second source and second drain electrodes 20 and 20' are deposited on the second dielectric layer 18 and are positioned at the bottom of the light emitting channel layer 19, that is also in contact with the second dielectric layer 18.

[0017] According to another embodiment, the cross-sectional view of which is shown in Fig. 5, one of the second source and second drain electrodes 20 and 20' of the second light emitting transistor can be positioned at the bottom of the light emitting channel layer 19, and the other of the second source and second drain electrodes 20 and 20' can be positioned on top of the light emitting channel layer 19. In other words, according to this embodiment, the second source and second drain electrodes are both horizontally and vertically displaced from each other.

[0018] It is not necessary to realize the light emitting channel layer with a single layer of organic material. For example, the light emitting channel layer 19 may be composed of a stack of a plurality of layers, for example, from 2 to an integer number n, as shown in figure 6. In particular, the light emitting channel layer 19 may include one or more hole transport layers each comprising a p-type semiconductor, one or more emissive layers in which the recombination of electrons and holes can take place, and one or more electron transport layers each comprising an n-type semiconductor. The second source and second drain electrodes 20 and 20' may be formed both above the topmost layer of the stack, as shown in figure 6, or one above the topmost layer and the other below the stack or buried within an intermediate layer of the stack, as illustrated in figure 7.

[0019] The second (light emitting) transistor may also be realized as shown in figures 8 and 9, that is, having a top-gate architecture, with the stack of n layers constituting the light emitting channel layer surmounted by the second dielectric layer 18 over which the second gate electrode 17 is realized. In the embodiment of figure 8 both the second electrodes 20 and 20' are positioned below the light emitting channel layer 19. In the embodiment of figure 9, a second electrode (for example, the second source electrode 20) is positioned above the second topmost layer of the stack and is buried by the top-

most layer of the light emitting channel, the other second electrode (for example, the second drain electrode 20') is realized on the insulating layer 16 and is positioned at the bottom of the stack.

[0020] The various second light emitting transistors illustrated in Figures 1 to 9 all have a single channel structure. Figure 10 illustrates an alternative embodiment in which the second light emitting transistor has a multi-channel structure. Specifically, the second light emitting transistor has at least 3 second electrodes which are horizontally (i.e., orthogonal to the stacking direction of the layers that comprise the second transistor) alternated. For example, such embodiments can include a common second drain electrode positioned between two second source electrodes. Each of the second source electrodes is horizontally displaced from the common second drain electrode, thereby defining two channels. This embodiment can lead to advantages including much improved light emission under the common drain electrode, and higher light/dark ratio.

[0021] As illustrated in the sectional view along the line B-B shown in figures 11 and 12, the second transistor (i.e. the light emitting transistor) may be equipped with a reflecting layer R for reflecting upwards (figure 11) or downwards (figure 12) the light emitted by the light emitting channel layer 19. In the former case (figure 11) the reflecting layer R is realized in the insulating layer 16 below the second gate electrode 17; in the latter case (figure 12) the second source and second drain electrodes 20 and 20' are buried by an electrically isolating layer i above which the reflecting layer R is realized.

[0022] According to yet another embodiment, not shown in the figures, the second gate electrode 17 of the light emitting transistor acts as a reflecting layer in order to reflect upward the light emitted by the light emitting channel layer 19. In a preferred embodiment the gate is formed by a reflecting and conducting material, like, e.g., silver or aluminum.

[0023] In all embodiments so far presented of the display pixel of the present disclosure, reference was made only to the cross-section along the line B-B assuming that the cross section along the line A-A may be as in figure 2A. Nevertheless, the display pixel according to the shown embodiments may have a cross section along the lines A-A as depicted in figure 13, in which the first source electrode 12 is realized partially on the substrate 11 and partially on the semiconducting layer 13, over which the first drain electrode 12' is formed.

[0024] As an alternative not shown in the figures, both the first source and drain electrodes 12 and 12' are realized either above or below the semiconductor layer 13.

[0025] According to yet another embodiment not shown in the figures, the first gate electrode 15 is realized on the substrate 11 and is located below the first dielectric layer 14 and the semiconductor layer 13.

The display pixel of the present invention may be realized on a same substrate with other identical display pixels disposed in rows and columns for forming an array of

display pixels having a plurality of enable lines SCAN and address lines DATA. Conveniently, the display pixels of a same row will be connected to a same enable line SCAN and the display pixels of a same column will be connected to a same address line DATA, so as to singularly command each display pixel of the array by applying appropriate voltages at the respective enable line and address line. The drain and source electrodes of each light emitting transistor in each pixel will be connected to a same drain line and a same source line to provide the same voltage bias to all the pixels.

Claims

1. A display containing an array of pixels, wherein each pixel comprises at least a first driving transistor (100) and at least a second light emitting transistor (200) mounted on a common substrate (11), wherein the first driving transistor stack comprises the following elements:

- a first source and a first drain electrodes (12, 12') separated and connected to each other by a semiconductor layer (13)
- a first dielectric layer (14)
- at least one first gate electrode (15)

The second light emitting transistor comprises the following elements:

- a second gate electrode (17)
- a second dielectric layer (18)
- a light emitting channel (19)
- a second source and a second drain electrodes (20, 20'), having widths w_s and w_d , respectively,

wherein the second gate electrode (17) is in electrical contact with at least one of the first source or drain electrodes (12') and

characterized in that at least one of the second source and second drain electrodes (20, 20') vertically overlaps with the second gate (17) by at least $5\ \mu\text{m}$ (L , L') and that said second source and second drain are horizontally separated by at least $2\ \mu\text{m}$.

2. A display according to claim 1 wherein said vertical overlap is comprised between 5 and $150\ \mu\text{m}$.

3. A display according to any of the previous claims wherein said second source and second drain horizontal separation is comprised between 2 and $50\ \mu\text{m}$.

4. A display according to any of the previous claims wherein both said second source and second drain are vertically overlapped by at least $5\ \mu\text{m}$ with said second gate.

5. A display according to any of the previous claims wherein said second source and second drain are completely vertically overlapped with said second gate.
6. A display according to any of the previous claims wherein the second source width w_s and the second drain width w_d are chosen in accordance to the following formula:

$$1 \leq \text{Max}(w_d, w_s) / \text{Min}(w_d, w_s) \leq 25$$

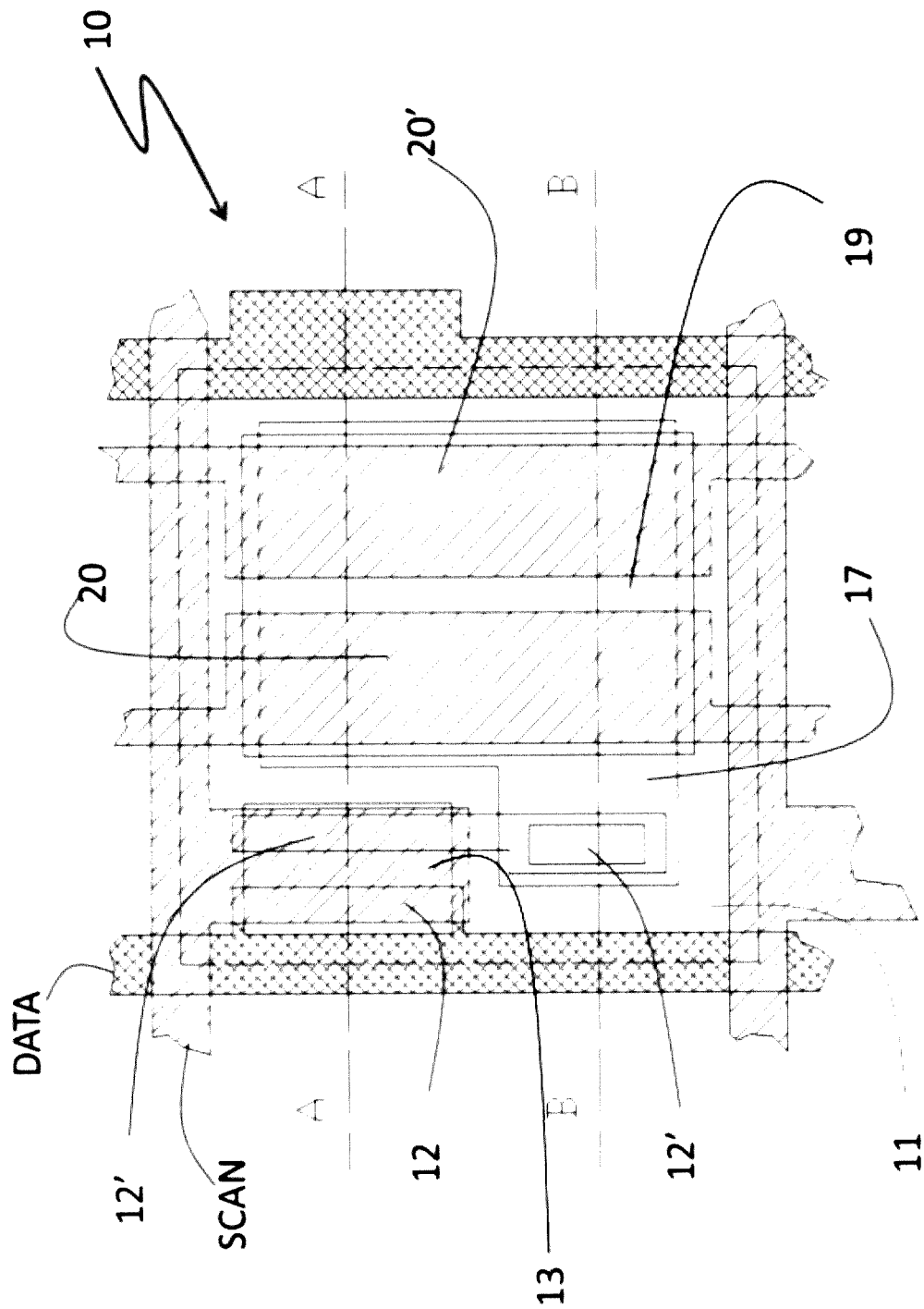
and preferably

$$1 \leq \text{Max}(w_d, w_s) / \text{Min}(w_d, w_s) \leq 10$$

7. A display according to any of the previous claims wherein at least one of said second source and second drain is in contact with both light emitting channel and the second dielectric layer.
8. A display according to any of the previous claims wherein the light emitting channel is ambipolar.
9. A display according to any of the previous claims wherein the light emitting channel is formed by a single layer of an organic semiconductor.
10. A display panel according to claim 9 wherein said second source and said second drain are both above or both below the light emitting channel.
11. A display panel according to claim 9 wherein one of said second source and said second drain is below the light emitting channel and the other one is above the light emitting channel.
12. A display panel according to claims 1-9 wherein said light emitting channel comprises at least two different layers of organic semiconductors, preferably the number of organic semiconductor layers is three.
13. A display panel according to claim 12 wherein said second source and drain are above or within the light emitting channel.
14. A display panel according to claim 12 wherein the second gate is above the light emitting channel.
15. A display panel according to claim 14 wherein said second source and second drain are below or within the light emitting channel
16. A display according to any of the previous claims wherein said second light emitting transistor com-

prises a third source or drain electrode disposed in such a way that source and drain electrodes are horizontally alternated.

17. A display according to any of the previous claims comprising a reflecting layer above or below the light emitting channel.
18. A display panel according to any of the previous claims wherein said first source and said first drain are both above or both below the semiconductor layer.
19. A display panel according to any of the previous claims wherein the first gate is below the semiconductor layer.
20. A display panel according to any of the previous claims wherein the first gate is above the semiconductor layer.



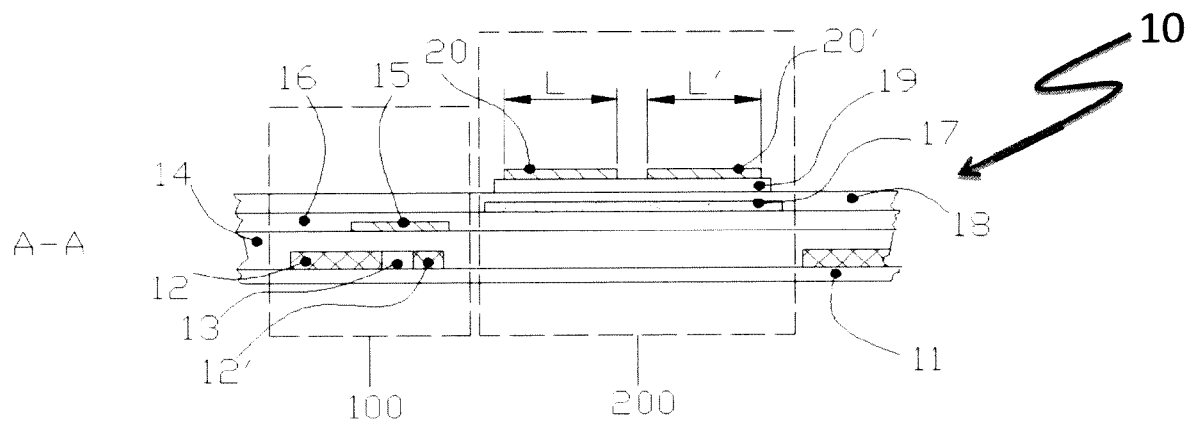


FIG. 2A

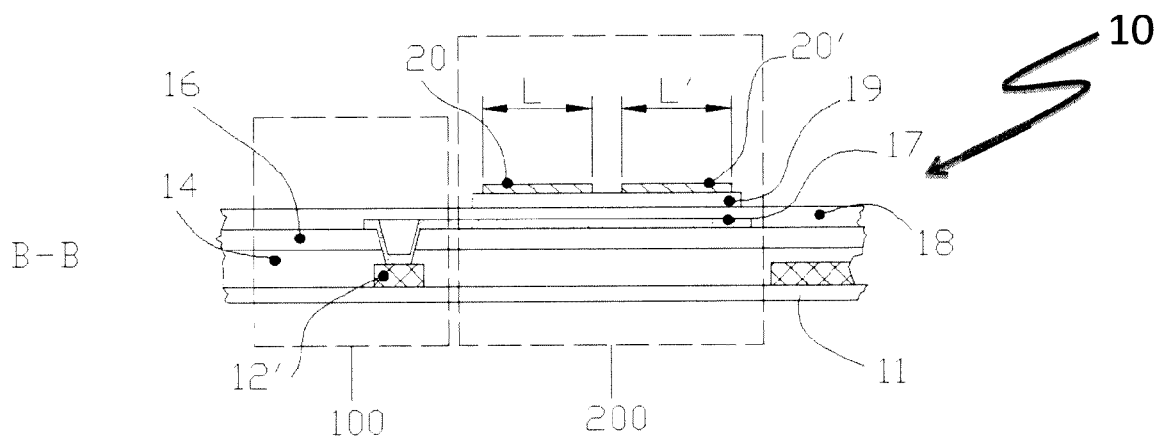
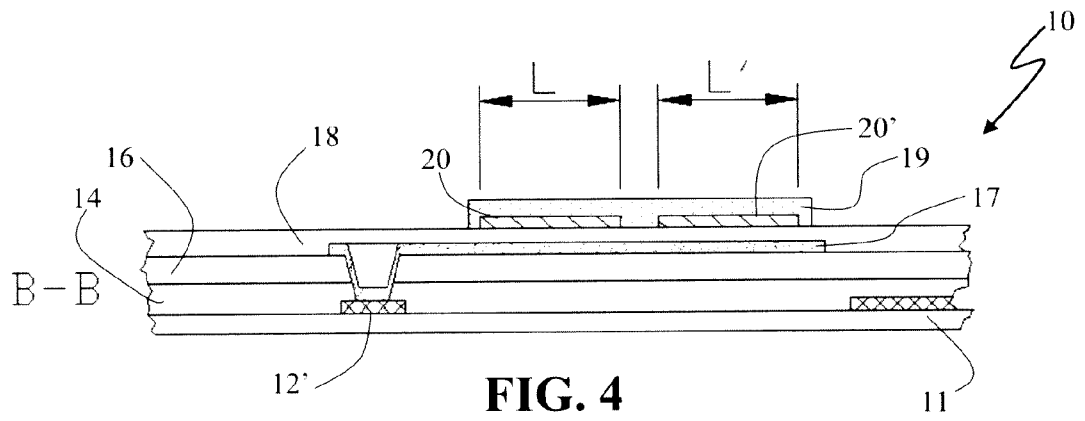
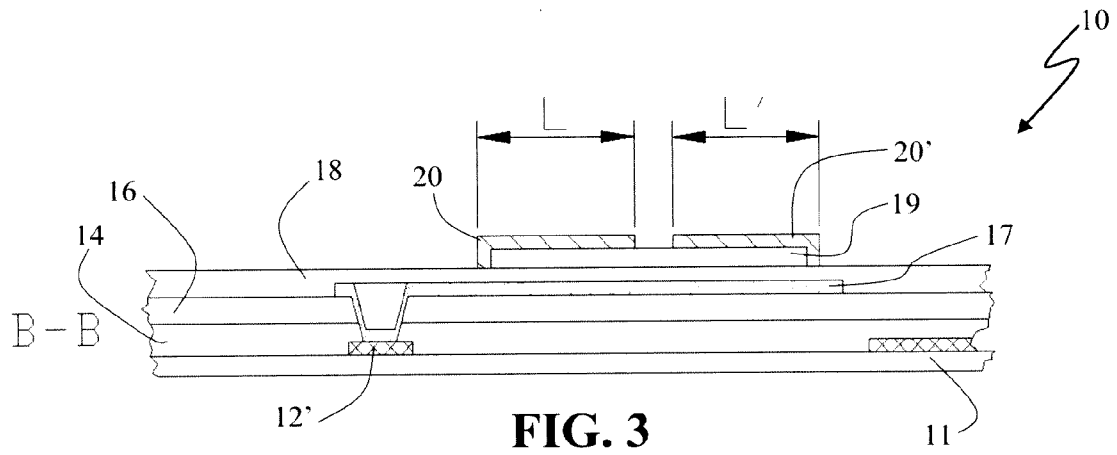
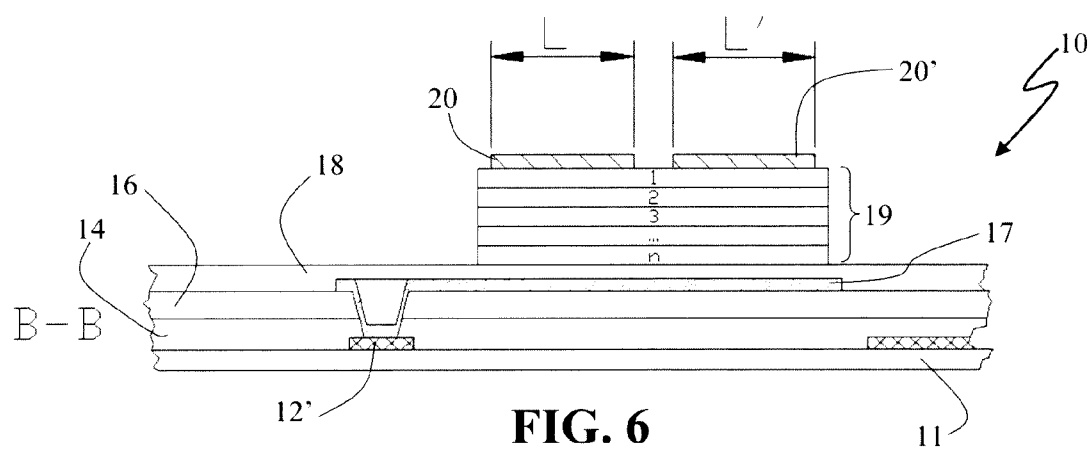
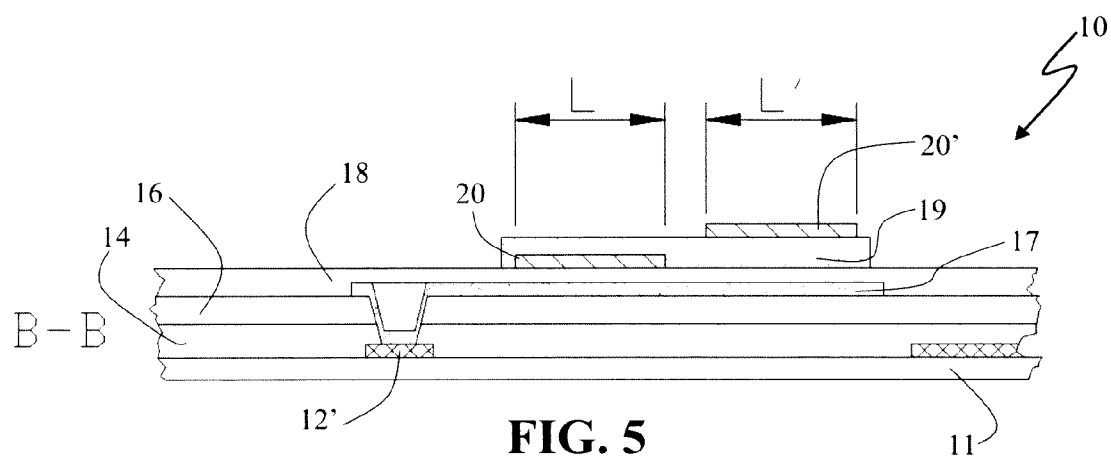
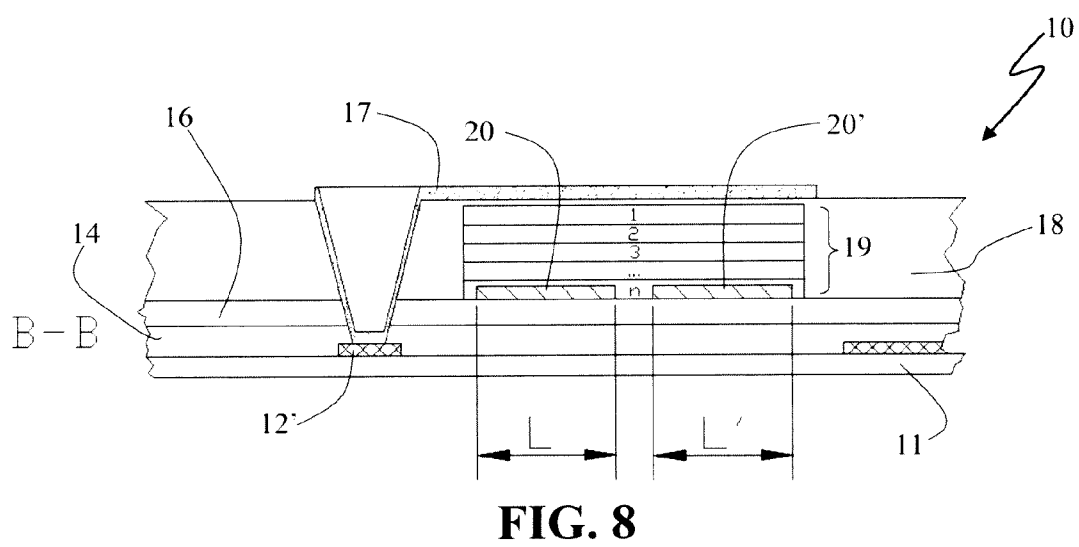
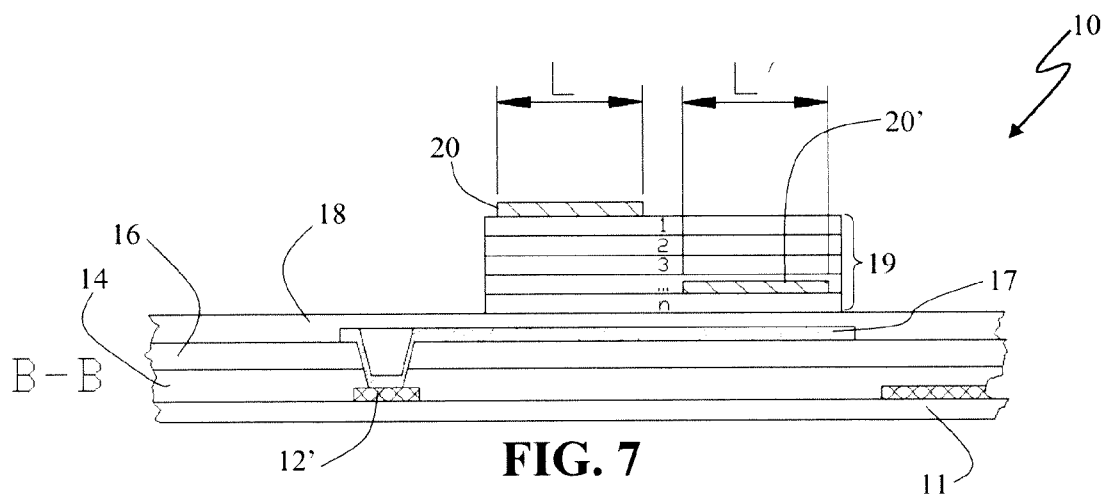


FIG. 2B







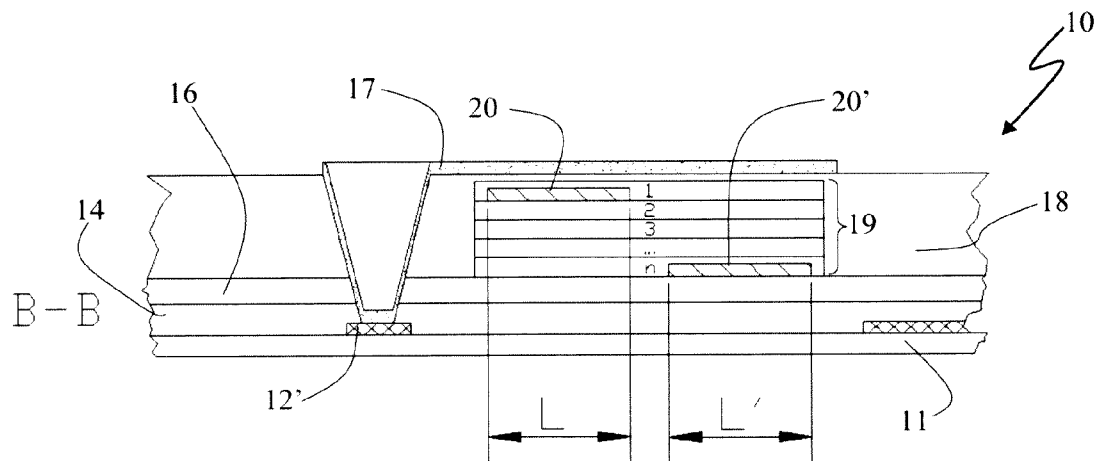


FIG. 9

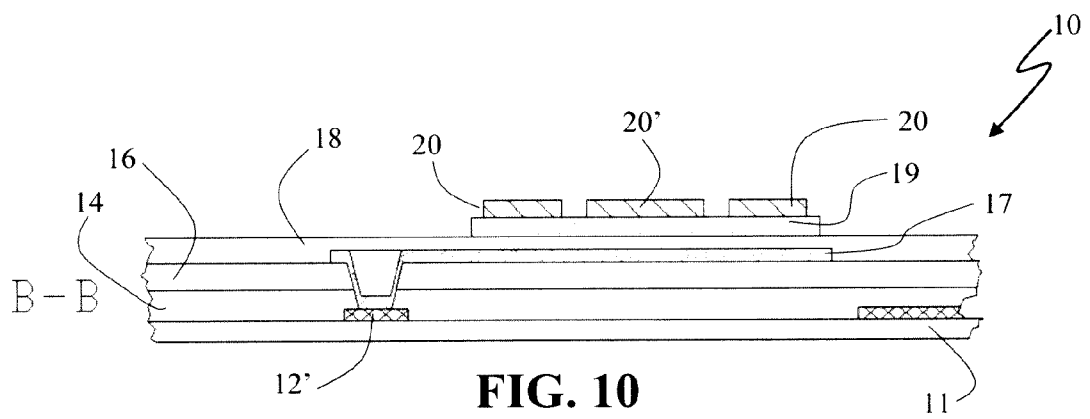
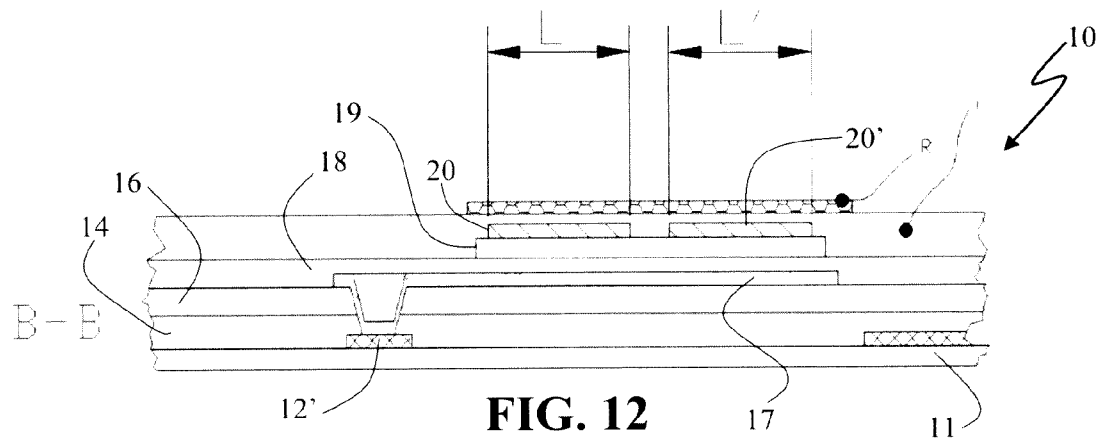
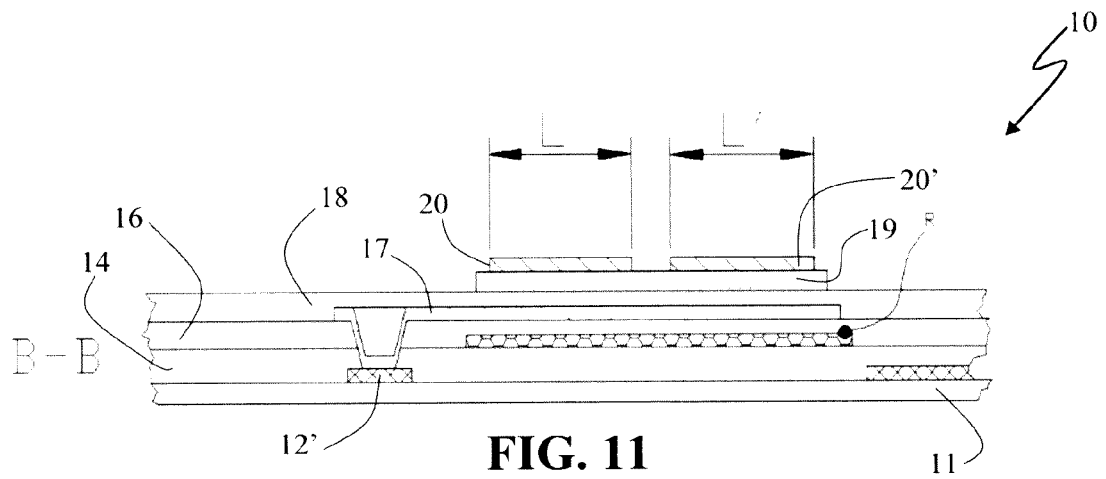


FIG. 10



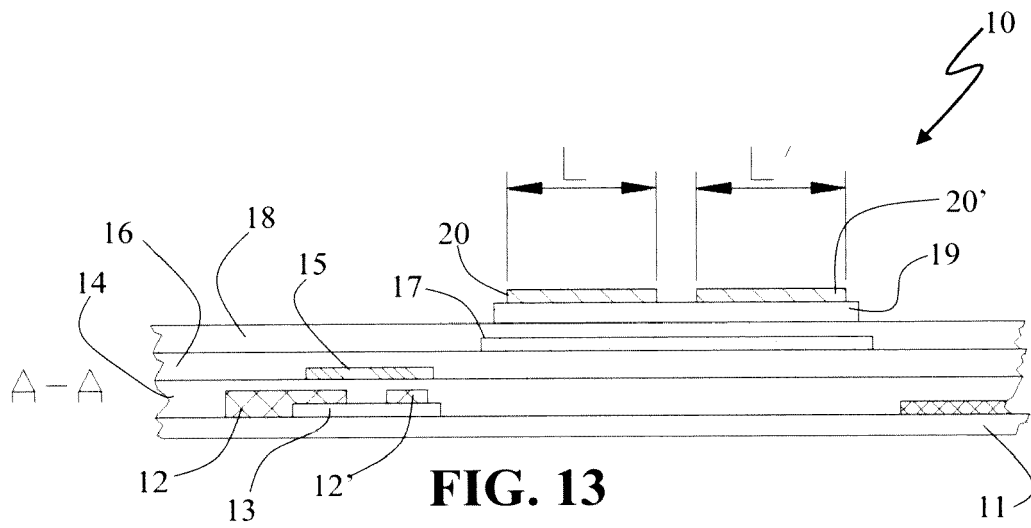


FIG. 13



EUROPEAN SEARCH REPORT

Application Number
EP 14 42 5146

5

10

15

20

25

30

35

40

45

50

55

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	GB 2 433 161 A (UNIV KYOTO [JP]; PIONEER CORP [JP]; HITACHI LTD [JP]; ROHM CO LTD [JP]) 13 June 2007 (2007-06-13) * page 28; figures 1,12B,18 *	1-20	INV. H01L51/52 H01L27/32
Y	WO 2013/128344 A1 (E T C S R L [IT]) 6 September 2013 (2013-09-06) * page 14; figures 4,5 *	1-20	
Y	US 2006/208962 A1 (SEKIYA TAKURO [JP]) 21 September 2006 (2006-09-21) * paragraph [0136] - paragraph [0146]; figures 1,19 *	1-20	
A	WO 2007/043696 A1 (PIONEER CORP [JP]; HATA TAKUYA [JP]; NAKAMURA KENJI [JP]; YOSHIZAWA AT) 19 April 2007 (2007-04-19) * figure 16 *	1-20	
A	US 2014/117317 A1 (KIM KI SEO [KR]) 1 May 2014 (2014-05-01) * figures 2-7 *	1-20	TECHNICAL FIELDS SEARCHED (IPC) H01L
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 27 May 2015	Examiner Bernabé Prieto, A
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03/02 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 14 42 5146

5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

27-05-2015

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2433161 A	13-06-2007	CN 101069298 A	07-11-2007
		GB 2433161 A	13-06-2007
		JP 4972730 B2	11-07-2012
		KR 20070083520 A	24-08-2007
		US 2008164460 A1	10-07-2008
		WO 2006025274 A1	09-03-2006

WO 2013128344 A1	06-09-2013	CN 104094436 A	08-10-2014
		EP 2786437 A1	08-10-2014
		KR 20140126699 A	31-10-2014
		TW 201349606 A	01-12-2013
		US 2015001518 A1	01-01-2015
		WO 2013128344 A1	06-09-2013

US 2006208962 A1	21-09-2006	NONE	

WO 2007043696 A1	19-04-2007	NONE	

US 2014117317 A1	01-05-2014	CN 103794724 A	14-05-2014
		KR 20140055142 A	09-05-2014
		TW 201417366 A	01-05-2014
		US 2014117317 A1	01-05-2014

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 8497501 B [0003]
- EP 2737559 A [0003]
- EP 2574219 A [0003]
- EP 2583329 A [0003]
- EP 2786437 A [0003]
- US 20130240842 A [0005] [0009] [0010]
- US 8664648 B [0010]
- WO 2011147523 A [0010]
- US 8758649 B [0010]
- US 2014117317 A [0010]
- WO 2010049871 A [0010]

Non-patent literature cited in the description

- **MUCCINI.** Organic light-emitting transistors with an efficiency that outperforms the equivalent light-emitting diodes. *Nature Materials*, 2010, vol. 9, 496-503 [0002]

专利名称(译)	显示包含改进的像素架构		
公开(公告)号	EP3021373A1	公开(公告)日	2016-05-18
申请号	EP2014425146	申请日	2014-11-14
[标]申请(专利权)人(译)	天光材料科技股份有限公司		
申请(专利权)人(译)	等等. S.R.L. POLYERA CORPORATION		
当前申请(专利权)人(译)	等等. S.R.L. POLYERA CORPORATION		
[标]发明人	MUCCINI MICHELE GENERALI GIANLUCA DALPAOS RICCARDO FACCHETTI ANTONIO HSIAO CHUNG CHIN LIEN HUGH		
发明人	MUCCINI, MICHELE GENERALI, GIANLUCA D'ALPAOS, RICCARDO FACCHETTI, ANTONIO HSIAO, CHUNG-CHIN LIEN, HUGH		
IPC分类号	H01L51/52 H01L27/32		
CPC分类号	H01L27/3262 H01L27/3274 H01L51/5296 H01L51/5271		
外部链接	Espacenet		

摘要(译)

本发明涉及用于基于OLET的显示器的改进的有机发光晶体管 (OLET) 像素架构。

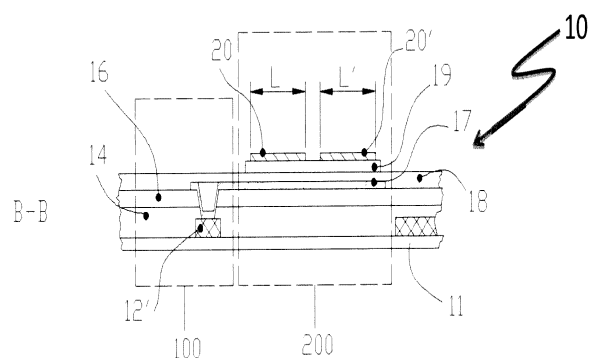


FIG. 2B