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(54) **DISPLAY DEVICE AND METHOD FOR DRIVING SAME**

ANZEIGEVORRICHTUNG UND BETRIEBSVERFAHREN DAFÜR

DISPOSITIF D'AFFICHAGE ET SON PROCÉDÉ D'ENTRAÎNEMENT

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Description

TECHNICAL FIELD

[0001] The present invention relates to display devices, and more specifically, the invention relates to a display device, such as an organic EL display, which includes self-luminous elements driven by current, and a method for driving the same.

BACKGROUND ART

[0002] Organic EL (electroluminescent) displays are conventionally known as being thin display devices featuring high image quality and low power consumption. The organic EL display has a plurality of pixel circuits arranged in a matrix, each circuit including an organic EL element, which is a self-luminous element driven by current, and a drive transistor for driving the element.

[0003] The method for controlling the amount of current to be applied to a current-driven display element such as the organic EL element is generally classified into a constant-current control mode (or current-programmed drive mode) in which the current to be applied to a display element is controlled by a data signal current applied to a data signal line electrode of the display element, and a constant-voltage control mode (or voltage-programmed drive mode) in which the current to be applied to a display element is controlled by a voltage corresponding to a data signal voltage. Among these modes, when the constant-voltage control mode is used for display on an organic EL display, it is necessary to compensate for current reduction (luminance decrease), which is caused by variations in the threshold voltage among drive transistors and high resistance due to deterioration of organic EL elements over time. On the other hand, in the constant-current control mode, the current value of the data signal is controlled such that current is applied to the organic EL element at a constant level regardless of the threshold voltage and the internal resistance of the organic EL element, and therefore compensation as mentioned above is normally not required. However, more drive transistors and lines are used in the constant-current control mode than in the constant-voltage control mode, resulting in a reduced aperture ratio, hence wide use of the constant-voltage control mode.

[0004] Here, there are various conventionally known types of pixel circuit that perform compensation operations as mentioned above in the configuration employing the constant-voltage control mode. Japanese Laid-Open Patent Publication No. 2006-215275 describes a pixel circuit 80 shown in FIG. 21. The pixel circuit 80 includes TFTs (thin-film transistors) 81 to 85, a capacitor 86, and an organic EL element 87. To perform writing to the pixel circuit 80, first, the TFTs 82 and 84 are brought into ON state, thereby initializing a gate-source voltage of the TFT 85 (drive transistor). Next, the TFT 84 is brought into OFF state, and then the TFT 83 is brought into OFF state, so that a threshold voltage of the TFT 85 is held by the capacitor 86. Subsequently, a data potential is applied to a data line DTL, and also the TFT 81 is brought into ON state. By controlling the TFTs in this manner, it is rendered possible to compensate for variations in the threshold voltage among TFTs 85 and high resistance (and resulting current reduction), which occurs due to deterioration of organic EL elements 87 over time.

[0005] The pixel circuit 80 is connected to the data line DTL, four control lines WSL, AZL1, AZL2, and DSL, and three power lines (lines for Vofs, Vcc, and Vss). In general, as the number of lines (particularly, control lines) connected to the pixel circuit increases, the circuit becomes more complicated, resulting in increased production cost. Therefore, the pixel circuit described in Japanese Laid-Open Patent Publication No. 2006-215275 has the TFT 82 or 84 connected at its source terminal to the control line WSL. Also, Japanese Laid-Open Patent Publication No. 2007-316453 describes a pixel circuit in which the TFT 82 is connected at its gate terminal to a control line WSL for an immediately preceding row. By commonly using a line as both the control line and the power line, the number of lines used can be reduced.

[0006] Japanese Laid-Open Patent Publication No. 2007-310311 describes a pixel circuit 90 shown in FIG. 22. The pixel circuit 90 includes a TFT 91, a TFT 92, a capacitor 93, and an organic EL element 94. To perform writing to the pixel circuit 90, first, the TFT 91 is controlled to be in ON state. Next, an initialization potential is applied to a power line DSL and thereby to an anode terminal of the organic EL element 94. Then, a power potential is applied to the power line DSL, so that a threshold voltage of the TFT 92 (drive transistor) is held by the capacitor 93. Subsequently, a data potential is applied to a data line DTL. Such provision of the initialization potential through the power line makes it possible for a small number of elements to achieve compensation for variations in the threshold voltage among TFTs 92. Japanese Laid-Open Patent Publication No. 2007-148129 describes a pixel circuit to which an initialization potential is provided through a power line and a reference potential is provided through a data line. Japanese Laid-Open Patent Publication No. 2008-33193 describes a pixel circuit in which a compensation operation is performed in a plurality of horizontal periods before writing.

[0007] US 2006/0290614 A1 provides a method and system for driving a light emitting device display. The system provides a timing schedule which increases accuracy in the display. The system may provide the timing schedule by which an operation cycle is implemented consecutively in a group of rows. The system may provide the timing schedule by which an aging factor is used for a plurality of frames.

[0008] US 2009/0244050 A1 provides a panel, including a plurality of pixel circuits disposed in rows and columns and each including a light emitting element for emitting light in response to driving current, a sampling transistor for sampling an image signal, a driving transistor for supplying the driving current to the light emitting element, and a storage capacitor for storing a predetermined potential; and a power supplying section configured to supply a power supply voltage of a high potential or a low potential at a time to all of the pixel circuits arranged in rows and columns; the power supplying section setting the power supply voltage to be supplied to the low potential, with which the gate-source voltage of the driving transistor becomes higher than a threshold voltage of the driving transistor, by Q times within a one-field period, Q being equal to or greater than 2.

[0009] US 2004/0174349 A1 shows a pixel circuit which includes a light emitting device, a storage device configured to represent a level of illumination, and a driving device used to drive the light emitting device. Configuring the storage device includes changing a voltage difference across the storage device to a level larger than a threshold voltage of the driving device. The driving device reduces driving of the light emitting device while the storage device is being configured. After the storage device has been configured, the driving device is permitted to drive the light emitting device to emit light having a luminance level corresponding to the level of illumination represented by the storage device.

[0010] US 2009/0244055 A1 provides an image displaying apparatus which is configured to display a desired image on an image displaying section employed in the image displaying apparatus by making use of a signal-line driving circuit and a scan-line driving circuit to drive pixel circuits. Each of the pixel circuits employs at least a light emitting device, a signal-level holding capacitor, a driving transistor for driving the light emitting device and a signal writing transistor. The signal-line driving circuit and the scan-line driving circuit drive each of the pixel circuits so as to put the light emitting device employed in the pixel circuit in a no-light emission state of emitting no light in a no-light emission period and a light emission state of emitting light in a light emission period repeatedly.

[0011] US 2010/0091207 A1 provides a three-dimensional image system which includes a display device including a pixel array section, a driving circuit section, and a display end timing extracting section; a transmitting section; and wearable means including a receiving section, a pair of shutter mechanisms, and a shutter driving section.

[0012] US 2009/0109146 A1 discloses a display apparatus, including a pixel array section having a plurality of pixels each including an electro-optical element, a writing transistor, a driving transistor, and a holding capacitor; a power supply scanning circuit; and a signal outputting circuit. The power supply scanning circuit is operable to supply a second power supply potential to initialize the potential of a second electrode of the driving transistor and then change over the potential of a power supply line to a first power supply potential. The signal outputting circuit is operable to output, when the writing transistor is in a conducting state, a first reference potential, supply, midway while a threshold value correction process is carried out, a second reference potential, output a third reference potential within a period within which the writing transistor remains in the conducting state, and output an image signal after the threshold correction process ends.

[0013] US 2009/0278771 A1 shows an organic electro luminescence display panel provided with a pixel structure and a wiring structure which are adapted to an active matrix driving method. The panel is driven by an electric potential asserted on each multi-consecutive-row bundle composed of adjacent power-supply lines, which are electrically tied to each other, each stretched in a horizontal direction and each used for supplying a driving current to an organic electro luminescence light emitting device employed in every pixel circuit of said organic electro luminescence display panel, to serve as an electric potential having two or more different magnitudes.

[0014] US 2007/0115225 A1 shows an active-matrix organic light-emitting display, wherein each of the pixel circuits includes (fig.29-30) an electro-optic element (EL), a drive transistor (T5), a write control transistor (T1), an emission control transistor (T4), a capacitor (C1), wherein a power control circuit is adapted to provide the power lines with initialization potentials and power potentials.

SUMMARY OF THE INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

[0015] By applying the method described in Japanese Laid-Open Patent Publication No. 2006-215275 or 2007-316453 to the pixel circuit 80 shown in FIG. 21, it is rendered possible to reduce the number of lines to be connected to the pixel circuit. However, the pixel circuit resulting from such a method has a problem with a higher number of TFTs. On the other hand, the pixel circuit 90 shown in FIG. 22 has a smaller number of TFTs. However, when the pixel circuit 90 is used, the power line DSL needs to be driven in conjunction with the control line WSL. Accordingly, a power control circuit requires output buffers the number of which is the same as the power lines WSL. In addition, the potential of the power lines DSL needs to change at short intervals in accordance with periods in which the control lines WSL are selected, and therefore the output buffers provided in the power control circuit need high current drive capability. As a result, the pixel circuit 90 has a problem with an increased scale and power consumption of the power control circuit.

[0016] Furthermore, application of the method described in Japanese Laid-Open Patent Publication No. 2008-33193 can ensure a sufficient amount of time for a compensation operation but results in a complicated configuration, and if

the operation of compensating for a threshold voltage (also called "threshold detection") is performed in a selection period as in other conventional methods described above, the configuration can be simplified, but a sufficient amount of time cannot be ensured for a compensation operation.

[0017] Therefore, an objective of the present invention is to provide a display device capable of reducing the scale and power consumption of a power control circuit while maintaining a high aperture ratio of pixel circuits, and also capable of ensuring a sufficient amount of time for threshold detection with a simplified configuration.

SOLUTION TO THE PROBLEMS

[0018] The invention is defined in the independent claims. Advantageous embodiment of the invention are subject to the dependent claims.

[0019] Examples called embodiments in the description, where these do not fall within the scope of the claims, are illustrative examples and not embodiments claimed in the present application.

EFFECT OF THE INVENTION

[0020] According to the first aspect of the invention, the need for signal lines or suchlike for providing initialization potentials is eliminated, so that the number of elements in the pixel circuits can be reduced, and therefore, the aperture ratio does not decrease, and further, the need for the power control circuit to be driven, for example, each time the scanning signal line is selected, so that power consumption can be reduced, and the number of output buffers provided in the power control circuit can be reduced, resulting in a reduced circuit scale of the power control circuit. Moreover, the threshold detection period can be set to a suitable length, typically longer than the selection period, and therefore, threshold detection can be reliably performed, so that accuracy in threshold compensation can be enhanced. In addition, when compared to the configuration where threshold detection is performed in the selection period, a sufficient amount of time can be spared for writing pixel data. Therefore, for example, this configuration is particularly suitable for a three-dimensional image display device (typically, a 3D television) or suchlike where the writing period is short, i.e., high-speed drive is normally performed.

[0021] Still according to the first aspect of the invention, the circuit scale of the power control circuit can be reduced, power consumption can be reduced, and besides the initialization period can be set to a suitable length, typically longer than the selection period, so that even a power control circuit with relatively low drive capability can ensure a reliable initialization operation.

[0022] Still according to the first aspect of the invention, aside from the initialization period and the threshold detection period, a different initialization period and a different threshold detection period are set, typically so as to be later than (typically, immediately succeeding) the start of a frame period, and pixel circuits to be subjected to initialization and threshold detection operations in such periods are not required to finish emitting light at the end of the frame period, and therefore can be selected for image display until the end of the frame period. Thus, a sufficient amount of time can be ensured for a data writing period (selection period).

[0023] According to the second aspect of the invention, the emission period length can be equalized among all pixel circuits, thereby inhibiting variations in luminance. Moreover, since the pixel circuits are unlit except in the emission period, moving picture performance can be enhanced as in the case where black insertion is carried out.

[0024] According to the third aspect of the invention, in the configuration where different groups of power lines are provided such that two power lines in the same group are adjacent to each other, for example, when there is a significant difference in the amount of current flowing through the power line between the upper and lower halves of the screen, there might be a difference in luminance at the center of the screen. However, in the configuration where power lines are provided such that two power lines in the same group are not adjacent to each other, the amount of current flowing through the power line can be approximately averaged among a plurality of rows, so that such a difference in luminance that might occur at the screen center can be prevented.

[0025] According to the fourth aspect of the invention, the number of common power lines is equal to the number of outputs of the power control circuit, and therefore, for example, the number of output buffers provided in the power control circuit can be reduced, thereby reducing the circuit scale of the power control circuit.

[0026] Still according to the first aspect of the invention, the period from the end of threshold detection to the start of light emission is set to be equal for all rows, so that leakage current that occurs from the end of threshold detection can be approximately equalized among all rows of pixel circuits. As a result, the amount of decrease in luminance due to leakage current can be approximately equalized among all rows of pixel circuits, thereby inhibiting uneven display. Note that moving picture performance can be advantageously enhanced by black insertion, as in the fourth aspect of the invention.

[0027] Still according to the first aspect of the invention, uneven display can be advantageously inhibited and further, a sufficient amount of time can be advantageously ensured for a data writing period (selection period), as outlined above.

[0028] According to the fifth aspect of the invention, the power control circuit is provided with only one output terminal, which simply outputs a constant power potential and is not driven at all, resulting in a reduced circuit scale of the power control circuit.

[0029] According to the sixth aspect of the invention, the auxiliary capacitor is added parallel to the electro-optic element, ensuring that the capacitance value of the electro-optic element can be higher than that of the capacitor included in the pixel circuit (typically, it can be significantly high), thereby enhancing approximation accuracy of approximation formulae for use in threshold compensation, resulting in enhanced accuracy of threshold detection.

[0030] According to the seventh aspect of the invention, the method for driving a display device can achieve similar effects to those achieved by the first aspect of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031]

FIG. 1 is a block diagram illustrating the configuration of a display device according to an embodiment of the invention.
FIG. 2 is a circuit diagram of a pixel circuit in an embodiment of the invention.
FIG. 3 is a diagram showing a timing chart describing a method for driving the pixel circuit in an embodiment of the invention.
FIG. 4 is a diagram illustrating the connecting arrangement of power lines according to an implementation useful for understanding the invention.
FIG. 5 is a diagram illustrating the operation of rows of pixel circuits according to an implementation useful for understanding the invention.
FIG. 6 is a diagram showing another example of the operation of rows of pixel circuits according to an implementation useful for understanding the invention.
FIG. 7 is a diagram illustrating another example of the connecting arrangement of control lines according to an implementation useful for understanding the invention.
FIG. 8 is a block diagram illustrating another exemplary configuration of the display device according to an embodiment of the invention.
FIG. 9 is a diagram illustrating the connecting arrangement of power lines in a display device according to an embodiment of the invention.
FIG. 10 is a diagram showing the operation of rows of pixel circuits according to an implementation useful for understanding the invention.
FIG. 11 is a diagram illustrating the connecting arrangement of power lines in a display device according to an embodiment of the invention.
FIG. 12 is a diagram showing the operation of rows of pixel circuits according to an implementation useful for understanding the invention.
FIG. 13 is a block diagram illustrating the configuration of a display device according to an embodiment of the invention.
FIG. 14 is a diagram showing the operation of rows of pixel circuits according to an implementation useful for understanding the invention.
FIG. 15 is a diagram showing a timing chart describing a method for driving a pixel circuit in a display device according to an implementation useful for understanding the invention.
FIG. 16 is a diagram showing the connecting arrangement of control lines E_i according to an embodiment of the invention.
FIG. 17 is a diagram showing the operation of rows of pixel circuits 10 in a display device according to an embodiment of the invention.
FIG. 18 is a diagram showing the connecting arrangement of control lines E_i in another embodiment of the invention.
FIG. 19 is a diagram showing the operation of rows of pixel circuits 10 in a display device according to the other embodiment of the invention.
FIG. 20 is a circuit diagram of another pixel circuit according to an embodiment of the invention.
FIG. 21 is a circuit diagram of a pixel circuit included in a conventional display device.
FIG. 22 is a circuit diagram of a pixel circuit included in another conventional display device.

MODES FOR CARRYING OUT THE INVENTION

[0032] FIG. 1 is a block diagram illustrating the configuration of a display device according to an embodiment of the present invention. The display device 100 shown in FIG. 1 is an organic EL display including a display control circuit 1, a gate driver circuit 2, a source driver circuit 3, a power control circuit 4, and ($m \times n$) pixel circuits 10. Hereinafter, m

and n are integers of 2 or more, i is an integer of 1 or more, and *j* is an integer of from 1 to *m*.

[0033] The display device 100 is provided with n parallel scanning signal lines G_i and *m* parallel data lines S_j perpendicular thereto. The ($m \times n$) pixel circuits 10 are arranged in a matrix so as to correspond to intersections of the scanning signal lines G_i and the data lines S_j. Moreover, n control lines E_i and *n* power lines VP_i are provided parallel to the scanning signal lines G_i. In addition, there is provided a common power line 9, which is a current supply bus line for connecting the power control circuit 4 to the power lines VP_i. The scanning signal lines G_i and the control lines E_i are connected to the gate driver circuit 2, and the data lines S_j are connected to the source driver circuit 3. The power lines VP_i are connected to the power control circuit 4 via the common power line 9. The pixel circuits 10 are supplied with a common potential Vcom by an unillustrated common electrode. Note that in the configuration here, the power lines VP_i are connected at one end to the common power line 9, but they may be connected at both ends (or at three or more contacts).

[0034] The display control circuit 1 outputs control signals to the gate driver circuit 2, the source driver circuit 3, and the power control circuit 4. More specifically, the display control circuit 1 outputs a timing signal OE, a start pulse YI, and a clock YCK to the gate driver circuit 2, a start pulse SP, a clock CLK, a display data DA, and a latch pulse LP to the source driver circuit 3, and a control signal CS to the power control circuit 4.

[0035] The gate driver circuit 2 includes a shift register circuit, logical operation circuits, and buffers (none of which are shown). The shift register circuit sequentially transfers the start pulse YI in synchronization with the clock YCK. The logical operation circuits perform logical operations between the timing signal OE and pulses outputted from stages in the shift register circuit. The logical operation circuits provide outputs to their corresponding scanning signal lines G_i and control lines E_i by way of the buffers. Each scanning signal line G_i is connected to *m* pixel circuits 10, which are collectively selected by using the scanning signal line G_i.

[0036] The source driver circuit 3 includes an *m*-bit shift register 5, a register 6, a latch circuit 7, and *m* D/A converters 8. The shift register 5 has *m* registers cascaded in such a manner that the start pulse SP supplied to the first stage register is transferred in synchronization with the clock CLK, so that a timing pulse DLP is outputted from each stage register. The register 6 is supplied with display data DA at the same time as the output of the timing pulse DLP. The register 6 stores the display data DA in accordance with the timing pulse DLP. Once the register 6 stores display data DA for one row, the display control circuit 1 outputs a latch pulse LP to the latch circuit 7. Upon reception of the latch pulse LP, the latch circuit 7 holds the display data stored in the register 6. The D/A converters 8 are provided so as to correspond to the data lines S_j. Each D/A converter 8 converts the display data held in the latch circuit 7 into an analog voltage, and applies the analog voltage to the data line S_j.

[0037] In accordance with the control signal CS, the power control circuit 4 applies a power potential and an initialization potential to the common power line 9 while switching therebetween. As shown in FIG. 1, all power lines VP_i are connected to one common power line 9, and therefore, all of the power lines VP_i switch between the power potential and the initialization potential at the same time. It is assumed below that the power potential is a high-level potential, and the initialization potential is a low-level potential.

[0038] FIG. 2 is a circuit diagram of the pixel circuit 10. As shown in FIG. 2, the pixel circuit 10 includes TFTs 11 to 13, a capacitor 15, and an organic EL element 16. The TFTs 11 to 13 are all n-channel transistors. The TFTs 11 to 13 function as a write control transistor, a drive transistor, and an emission control transistor, respectively. The organic EL element 16 functions as an electro-optic element.

[0039] Note that in addition to the organic EL element, the electro-optic element herein refers to any element whose optical characteristics change upon application of electricity, e.g., an FED (field emission display), an LED, a charge-driven element, a liquid crystal, or E Ink (electronic ink). Moreover, in the following description, the organic EL element will be exemplified as an electro-optic element, but the same description applies to any light-emitting element, so long as its amount of luminance is controlled in accordance with an amount of current.

[0040] As shown in FIG. 2, the pixel circuit 10 is connected to the scanning signal line G_i, the control line E_i, the data line S_j, the power line VP_i, and an electrode with a common potential Vcom. The TFT 11 has one conductive terminal connected to the data line S_j and the other conductive terminal connected to a gate terminal of the TFT 12. The TFT 13 has a drain terminal connected to the power line VP_i and a source terminal connected to a drain terminal of the TFT 12. The TFT 12 has a source terminal connected to an anode terminal of the organic EL element 16. The organic EL element 16 has a cathode terminal to which the common potential Vcom is applied. The capacitor 15 is provided between the gate terminal and the source terminal of the TFT 12. The TFT 11 has a gate terminal connected to the scanning signal line G_i, and the TFT 13 has a gate terminal connected to the control line E_i.

[0041] FIG. 3 is a diagram showing a timing chart describing a method for driving the pixel circuit 10. In FIG. 3, VG_i denotes a gate potential of a TFT 12 included in a pixel circuit in an *i*'th row, and VS_i denotes a source potential of that TFT 12 (an anode potential of the organic EL element 16). The pixel circuit 10 performs each of the following operations once per frame period: initialization; threshold detection (detection of the threshold for the TFT 12) ; writing; and light emission, and the pixel circuit 10 is unlit except in the emission period. Although it is the organic EL element 16 that is lit up (and turned off), the pixel circuit 10 includes the organic EL element 16, and therefore, in the following, the pixel

circuit 10 is described as being lit up or unlit. Moreover, the frame period is a unit period in which to display an image, which may include, for example, a black insertion period and can be set to various lengths.

[0042] Referring to FIG. 3, the operation of the pixel circuit in the first row will be described below. Prior to time t_{11}, scanning signal line G_1 and control line E_1 have low-level potentials, and power line VP_1 has a high-level potential. At time t_{11}, the potential of control line E_1 changes to high level (i.e., the line is activated), and the potential of power line VP_1 changes to low level (hereinafter, the low-level potential of the power line VP_i will be denoted by "VP_L") . Used as the potential VP_L is a significantly low potential, specifically, a potential lower than the gate potential of the TFT 12 immediately before time t_{11}. Moreover, at this time, the data line S_j has a reference potential Vref applied thereto, and this potential is provided to the gate of the TFT 12, so that the TFT 12 is brought into ON state. In addition, the TFT 13 is brought into ON state as well, so that source potential VS_1 of the TFT 12 is approximately equal to the potential VP_L.

[0043] At time t_{12}, the potential of power line VP_1 changes to high level. Moreover, at this time, the data line S_j has the reference potential Vref applied thereto. The reference potential Vref is determined such that the TFT 12 is brought into ON state immediately after time t_{12}, and thereafter, a voltage applied to the organic EL element 16 does not exceed an emission threshold voltage. Accordingly, after time t_{12}, the TFT 12 is in ON state, but no current flows through the organic EL element 16 (because the threshold for the organic EL element 16 is not exceeded) . Therefore, current flows from power line VP_1 through the TFT 13 to the TFT 12 and then to the source terminal thereof, so that source potential VS_1 of the TFT 12 rises. Source potential VS_1 of the TFT 12 rises and reaches (Vref - Vth) at the point where the gate-source voltage Vgs is equal to the threshold voltage Vth.

[0044] At time t_{13}, the potential of scanning signal line G_1 changes to low level. The potential of control line E_1 also changes to low level, so that after time t_{13}, the TFT 13 is in OFF state. As a result, source potential VS_1 of the TFT 12 remains approximately at (Vref - Vth).

[0045] At time t_{14}, the potential of scanning signal line G_1 changes to high level, and the potential (not shown) of the data line S_j changes to a level in accordance with display data (hereinafter, the potential of the data line S_j at this time will be referred to as the "data potential Vdat1"). After time t_{14}, the TFT 11 is in ON state, and gate potential VG_1 of the TFT 12 changes from Vref to Vdat1. The gate-source voltage Vgs of the TFT 12 after time t_{14} is obtained by the following equation (1).

$$Vgs = \{C_{OLED} / (C_{OLED} + C_{st})\} \times (Vdat1 - Vref) + Vth \quad \cdots (1)$$

[0046] Note that in equation (1), C_{OLED} is a capacitance value of the organic EL element 16, and C_{st} is a capacitance value of the capacitor 15.

[0047] The capacitance value of the organic EL element 16 is significantly high, hence $C_{OLED} >> C_{st}$. Therefore, equation (1) can be transformed (or can approximate) to the following equation (2).

$$Vgs = Vdat1 - Vref + Vth \quad \cdots (2)$$

[0048] In this manner, when gate potential VG_1 of the TFT 12 changes from Vref to Vdat1, source potential VS_1 of the TFT 12 barely changes, so that the gate-source voltage Vgs of the TFT 12 is approximately equal to (Vdat1 - Vref + Vth).

[0049] At time t_{15}, the potential of scanning signal line G_1 changes to low level. After time t_{15}, the TFT 11 is in OFF state. Therefore, the gate-source voltage Vgs of the TFT 12 remains approximately at (Vdat1 - Vref + Vth) even when the potential of the data line S_j changes.

[0050] At time t_{16}, the potential of control line E_1 changes to high level. After time t_{16}, the TFT 13 is in ON state, so that the drain terminal of the TFT 12 is connected to power line VP_1 via the TFT 13. At this time, the potential of power line VP_1 is high level, and therefore current flows from the power line VP_i through the TFT 13 to the TFT 12 and then to the source terminal thereof, so that source potential VS_1 of the TFT 12 rises. At this point, the gate terminal of the TFT 12 is in floating state. Accordingly, when source potential VS_1 of the TFT 12 rises, gate potential VG_1 of the TFT 12 also rises. At this time, the gate-source voltage Vgs of the TFT 12 is maintained approximately at a constant level.

[0051] The high-level potential applied to the power line VP_i is determined such that the TFT 12 operates in a saturated area in the emission period (from time t_{16} to time t_{17}). Accordingly, without considering a channel-length modulation effect, current I flowing through the TFT 12 in the emission period can be obtained by the following equation (3) .

$$I = 1 / 2 \cdot W / L \cdot \mu \cdot C_{ox}(Vgs - Vth)^2 \cdots (3)$$

[0052] Note that in equation (3), *W* is a gate width, L is a gate length, μ is a carrier mobility, and C_{ox} is a gate oxide film capacitance.

[0053] From equations (2) and (3), the following equation (4) can be derived.

$$I = 1 / 2 \cdot W / L \cdot \mu \cdot C_{ox}(Vdat1 - Vref)^2 \cdots (4)$$

[0054] Current I given by equation (4) changes in accordance with data potential Vdat1 but does not depend on the threshold voltage Vth of the TFT 12. Accordingly, even when there are variations in the threshold voltage Vth, or when the threshold voltage Vth changes over time, current is applied to the organic EL element 16 in accordance with data potential Vdat1, so that the organic EL element 16 can be lit up with a desired luminance.

[0055] At time t_{17}, the potential of control line E_1 changes to low level. After time t_{17}, the TFT 13 is in OFF state. Accordingly, no current flows through the organic EL element 16, so that the pixel circuit 10 is unlit.

[0056] In this manner, the pixel circuit in the first row performs initialization in the period from time t_{11} to time t_{12}, threshold detection in the period from time t_{12} to time t_{13}, and writing in the period from time t_{14} to time t_{15}, and then emits light in the period from time t_{16} to time t_{17}, and the pixel circuit in the first row is unlit except in the period from time t_{16} to time t_{17}. As with the pixel circuit in the first row, the pixel circuit in the second row performs initialization in the period from time t_{11} to time t_{12}, and threshold detection in the period from time t_{12} to time t_{13}, and the writing and light-emission operations are performed with a delay of predetermined period T_a compared to the pixel circuit in the first row. In general, the pixel circuit in the *i*'th row performs initialization and threshold detection in the same periods as pixel circuits in other rows, and performs the writing and light-emission operations with a delay of time T_a compared to the pixel circuit in the (*i*-1)'th row.

[0057] Accordingly, the initialization period can be set to a suitable length, typically longer than a selection period, and therefore, even when the current capability of an output buffer included in the power control circuit 4a is low, the power control circuit 4a can perform the driving satisfactorily. Moreover, the threshold detection period can also be set to a suitable length, typically longer than the selection period, and therefore threshold detection can be reliably performed, so that accuracy in threshold compensation can be enhanced. In addition, when compared to the configuration where threshold detection is performed in the selection period, a sufficient amount of time can be spared for writing pixel data. Therefore, even in the case of, for example, a three-dimensional image display device (typically, a 3D television) where the writing period is short, i.e., high-speed drive is performed, the configuration of the present invention can be readily applied.

[0058] Connections of the power lines and the operation of the pixel circuits 10 being driven by current applied via the power lines will be described next with reference to FIGS. 4 and 5. FIG. 4 is a diagram illustrating the connecting arrangement of power lines VP_i in the display device. The display device shown in FIG. 4 is provided with one common power line 111 for connecting the power control circuit 4a to the power lines VP_i. The common power line 111 is connected at one end to an output terminal of the power control circuit 4a, and all of the power lines VP_i are connected to the common power line 111.

[0059] Note that as described earlier, the common power line 111 is a bus line for current supply, but it does not have to be a bus line so long as all of the power lines VP_i can be commonly connected to the power control circuit 4a, and the number of common power lines and their connecting points with the power lines VP_i can be determined in accordance with any well-known configuration.

[0060] FIG. 5 is a diagram illustrating the operation of rows of pixel circuits 10 in the display device according to an implementation useful for understanding the invention. The power control circuit 4a applies a low-level potential to the common power line 111 for a predetermined period of time at the beginning of a frame period. Accordingly, the pixel circuits in all rows perform initialization at the beginning of the frame period. Immediately after initialization, the pixel circuits in all rows perform threshold detection. Subsequently, the pixel circuits in the first row are selected and perform writing. Next, the pixel circuits in the second row are selected and perform writing. Thereafter, similarly, the pixel circuits in the third through *n*'th rows are sequentially selected row by row, and the selected pixel circuits perform writing.

[0061] The pixel circuits in each row are unlit after threshold detection until immediately before writing. Here, the pixel circuits in each row need to be lit up for the same period of time, and the pixel circuits in the *n*'th row need to stop emitting light before the end of the frame period. Therefore, the pixel circuits in each row are lit up for a prescribed period of time T1 after writing, and they are unlit in other periods.

[0062] In a general display device, writing to the pixel circuit takes one frame period. On the other hand, in the configuration shown in FIG. 5, about half a frame period is taken for writing to the pixel circuit (such that about half a frame period can be ensured for light emission). Therefore, the scanning speed of the pixel circuit is about twice the normal speed. Note that in this example, the emission period length T1 of the pixel circuit is about half a frame period, but it may be shorter than half a frame period while the scanning speed of the pixel circuit remains about twice the normal speed. Alternatively, the scanning speed of the pixel circuit may be set faster than about twice the normal speed, with the emission period length longer than half a frame period.

[0063] Furthermore, in the exemplary operation shown in FIG. 5, the emission period starts not long after data writing (e.g., at time t_{16}), but the start of the emission period may be later than that. Moreover, as shown in FIG. 6, the emission period may be set to start at the same time in all rows.

[0064] FIG. 6 shows another example of the operation of rows of pixel circuits 10. As can be appreciated in comparison with FIG. 5, in FIG. 6 also, the pixel circuits 10 perform each of the initialization, threshold detection (detection of the threshold for the TFT 12), writing, and light-emission operations once per frame period, and are unlit except in the emission period, but after the writing, the pixel circuits in each row are unlit for a predetermined different period of time from other rows, and then the pixel circuits in all rows are simultaneously (collectively) lit up for a prescribed period of time T1, and are turned off simultaneously at the end of the frame period (in other words, immediately before initialization in the next frame). In this manner, the period from the end of threshold detection to the start of light emission is set to be equal for all rows, so that uneven display can be inhibited.

[0065] Specifically, as described earlier in conjunction with FIG. 4, when the TFT 11 is in OFF state, the gate-source voltage Vgs of the TFT 12 remains approximately unchanged at (Vdat1 - Vref + Vth) even if the potential of the data line S_j changes. However, the TFT 12 slightly leaks current, so that the gate-source voltage Vgs in fact decreases slowly. Accordingly, the period from the end of threshold detection (which occurs at the same time in all rows) to the start of light emission is set to be equal for all rows, so that the leakage current from the TFT 12 can be approximately equalized among all rows of pixel circuits 10, and therefore the amount of decrease in luminance due to leakage current can be approximately equalized among all rows of pixel circuits 10, thereby inhibiting uneven display.

[0066] Here, in the case where the initialization, threshold detection, and light-emission operations are performed in the above manner, these operations occur at the same times in all rows, so that the same signals are used for activating (and deactivating) the control lines E_i. Accordingly, a common control line for connecting all control lines may be provided, as shown in FIG. 7.

[0067] FIG. 7 is a diagram illustrating the connecting arrangement of control lines E_i in the above configuration. The display device shown in FIG. 7 is provided with a common control line 211 for connecting a scanning signal line driver circuit 102a and the control lines E_i. The common control line 211 is connected at one end to a control signal output terminal of the scanning signal line driver circuit 102a, and all of the control lines E_i are connected to the common control line 211. Note that the common control line 211 does not have to be a bus line so long as all of the control lines E_i can be commonly connected to the scanning signal line driver circuit 102a, and the number of common control lines and their connecting points with the control lines E_i can be determined in accordance with any well-known configuration, e.g., in the case where the control lines E_i are divided into groups, all control lines E_i included in one group are commonly connected to a common control line (i.e., the number of common control lines provided is the same as the number of groups). This results in a simplified configuration because the scanning signal line driver circuit 102a requires only one control signal output terminal, and further, the area of wiring up to the control lines E_i can be reduced.

[0068] As described above, the power control circuit 4 included in the display device 100 according applies an initialization potential to the common power line 9, and therefore the initialization potential can be readily provided through the power lines VP_i to the pixel circuits 10. As a result, the need for any additional feature for providing the initialization potential is eliminated, so that the number of elements in the pixel circuits 10 can be reduced. Moreover, the power control circuit 4 drives one common power line 9 electrically connected to all of the power lines VP_i. Accordingly, when compared to the case where the power lines VP_i are driven individually, the number of output buffers provided in the power control circuit 4 can be significantly reduced, resulting in a reduced circuit scale of the power control circuit 4. Moreover, the number of times at which to drive the power source can be set to be once per frame, and therefore, power consumption can be reduced compared to the case where, for example, the power source is driven the number of times corresponding to the number of rows. In addition, since the number of common power lines 9 is one (or relatively low), the area of wiring for power supply can be reduced.

[0069] Note that in the case where one common power line 9 is electrically connected to all power lines VP_i, the arrangement and connecting fashion of the common power line 9 and the power lines VP_i can be determined in accordance with any well-known configuration, and for example, a configuration as shown in FIG. 8 can be employed.

[0070] FIG. 8 is a block diagram illustrating another exemplary configuration of the display device according to an embodiment of the inevention. Unlike in the configuration shown in FIG. 1, *m* power lines VP_i provided in the display device 100 shown in FIG. 8 are provided parallel to *m* data lines S_j rather than to n control lines E_i and n scanning signal lines G_i. By arranging the power lines VP_i in this manner, the number of pixel circuits 10 to be connected per power line

VP_i can be reduced, and the difference in the amount of current to be provided among the pixel circuits 10 can be reduced. However, to ensure a significantly large electrode width, the configuration shown in FIG. 1 is more preferable.

[0071] Furthermore, in the present embodiment, the gate driver circuit 2 selects and controls all of the initialized pixel circuits 10 to perform threshold detection on the TFTs 12. Moreover, the gate driver circuit 2 selects and controls the initialized pixel circuits 10 row by row to sequentially perform writing to the TFTs 12 and emit light. As a result, a screen can be displayed with the threshold voltage of the TFTs 12 being compensated for.

[0072] Furthermore, upon initialization, the TFT 13 is controlled and brought into ON state, and when an initialization potential is applied to the power line VP_i for initialization, the gate voltage of the TFT 12 is set to the reference potential Vref, so that the TFT 12 is brought into ON state, and the initialization potential can be applied to the source terminal of the TFT 12. Moreover, upon light emission, the TFT 13 is controlled and brought into ON state for a prescribed period of time. As a result, the emission period length is equalized among the pixel circuits 10, thereby inhibiting variations in luminance. Moreover, since the pixel circuits 10 are unlit except in the emission period, moving picture performance can be enhanced as in the case where black insertion is carried out.

[0073] Furthermore, all transistors included in the pixel circuits 10 are of n-channel type. In this manner, since the transistors included in the pixel circuits 10 are of the same conductive type, cost of the display device can be reduced.

[0074] The configuration and operation of a display device according to another embodiment of the present invention are approximately the same as those of the display device shown in FIG. 1, except for the connecting arrangement of the power lines and the operation of the pixel circuits, therefore, the same components are denoted by the same reference characters, and any descriptions thereof will be omitted. Hereinafter, features and operations characteristic of this embodiment will be described.

[0075] FIG. 9 is a diagram illustrating the connecting arrangement of power lines VP_i in the display device according to an embodiment of the invention. The display device is provided with two common power lines 121 and 122 for connecting a power control circuit 4b to the power lines VP_i. The common power lines 121 and 122 are connected at one end to two output terminals, respectively, of the power control circuit 4b. Power lines VP_1 to $VP_{n/2}$ are connected to the common power line 121, and power lines $VP_{(n/2+1)}$ to VP_n are connected to the common power line 122.

[0076] FIG. 10 is a diagram showing the operation of rows of pixel circuits 10 in the display device according to an implementation useful for understanding the invention. The power control circuit 4b applies a low-level potential to the common power line 121 for a predetermined period of time at the beginning of a frame period, and after half a frame period, the power control circuit 4b applies a low-level potential to the common power line 122 for a predetermined period of time. Accordingly, the pixel circuits in the first through (n/2) 'th rows are initialized at the beginning of the frame period, and the pixel circuits in the (n/2+1)'th through n'th rows are initialized with a delay of half a frame period. Immediately after the first initialization, all of the pixel circuits in the first through (n/2)'th rows are selected simultaneously for a predetermined period of time, and immediately after the second initialization, all of the pixel circuits in the (n/2+1) 'th to n'th rows are selected simultaneously for a predetermined period of time, and the selected pixel circuits perform threshold detection. After the first threshold detection, the pixel circuits in the first through (n/2)'th rows are sequentially selected row by row, and after the second threshold detection, the pixel circuits in the (n/2+1)'th to n'th rows are sequentially selected row by row. The selected pixel circuits perform writing. The pixel circuits in each row are lit up for a predetermined period of time T2 after the writing, and they are unlit in other periods.

[0077] The pixel circuits in each row in the display device need to be lit up for the same period of time, but unlike in Figs. 5 and 6 where initialization always takes place at the beginning of a frame, the pixel circuits in the n'th row do not need to finish emitting light by the end of the frame period. Therefore, in the example shown in FIG. 10, the scanning speed of the pixel circuits is the same as normal, and the emission period length T2 of the pixel circuits is about half a frame period.

[0078] As described above, in the display device the scanning speed of the pixel circuit can be set to be the same as normal, and therefore a sufficient amount of time can be ensured for writing as in the normal case. Note that the emission period length may be set to be shorter than half a frame period while setting the scanning speed of the pixel circuits to be the same as normal. Alternatively, the emission period length may be set to be longer than half a frame period while setting the scanning speed of the pixel circuit to be faster than normal.

[0079] Furthermore, in the display device, since the number of output buffers provided in the power control circuit 4 is increased to two, the circuit scale of the power control circuit 4 is larger than in the display device of Fig. 1, so that the number of output buffers provided in the power control circuit 4 can be less than the number of power lines VP_i, and therefore, it can be said that the circuit scale of the power control circuit 4 can be reduced. In addition, the configuration makes it possible to achieve effects similar to those described in connection with the display device of Fig. 1, and further, an initialization potential is applied to the common power lines 121 and 122 at different times from each other, whereby the pixel circuits 10 can be initialized at suitable times in accordance with selection periods of the pixel circuits 10. Moreover, a plurality of adjacently disposed power lines VP_i are connected to the common power lines 121 and 122, so that writing to the pixel circuits 10 can be performed in accordance with sequential order within the display screen.

[0080] The configuration and operation of a display device according to an implementation useful for understanding

the invention are approximately the same as those of the display device according to the display device shown in FIG. 1, except for the connecting arrangement of the power lines and the operation of the pixel circuits, therefore, the same components are denoted by the same reference characters, and any descriptions thereof will be omitted. Hereinafter, features and operations characteristic of the third embodiment will be described.

[0081] FIG. 11 is a diagram illustrating the connecting arrangement of power lines VP_i in the display device according to an embodiment of the invention. The display device is provided with two common power lines 131 and 132 for connecting a power control circuit 4c to the power lines VP_i. The common power lines 131 and 132 are connected at one end to two output terminals, respectively, of the power control circuit 4c. Power lines VP_1, VP_3, and so on, in odd rows are connected to the common power line 131, and power lines VP_2, VP_4, and so on, in even rows are connected to the common power line 132.

[0082] FIG. 12 is a diagram showing the operation of rows of pixel circuits 10 in the display device according to an implementation useful for understanding the invention. The power control circuit 4c applies a low-level potential to the common power line 131 for a predetermined period of time at the beginning of a frame period, and after half a frame period, the power control circuit 4c applies a low-level potential to the common power line 132 for a predetermined period of time. Accordingly, the pixel circuits in odd rows are initialized at the beginning of the frame period, and the pixel circuits in even rows are initialized with a delay of half a frame period. All of the pixel circuits in odd rows are selected simultaneously for a predetermined period of time immediately after the first initialization, all of the pixel circuits in even rows are selected simultaneously for a predetermined period of time immediately after the second initialization, and the selected pixel circuits perform threshold detection. After the first threshold detection, the pixel circuits in odd rows are sequentially selected row by row, and after the second threshold detection, the pixel circuits in even rows are sequentially selected row by row. The selected pixel circuits perform writing. The pixel circuits in each row are lit up for a predetermined period of time T3 after the writing, and they are unlit in other periods. In the example shown in FIG. 12, the scanning speed of the pixel circuits is the same as normal, and the emission period length T3 of the pixel circuits is about half a frame period.

[0083] As described above, it can be said that the circuit scale of the power control circuit 4 can be reduced. In addition, the configuration makes it possible to achieve effects similar to those achieved in the implementation described in connection with Fig. 1, and further, writing to the pixel circuits 10 can be performed in accordance with sequential order within the display screen. However, in the case where there is a significant difference in the amount of current flow between the common power lines 121 and 122, e.g., when the luminance of a screen greatly varies between the upper and lower halves of the screen, there might be a difference in luminance at the center of the screen. In the display device the amount of current flow in most cases is approximately equal between the common power lines 131 and 132, so that such a difference in luminance that might occur at the screen center can be prevented.

[0084] The configuration and operation of a display device according to an implementation useful for understanding better the invention are approximately the same as those of the display device shown in FIG. 1, except for the connecting arrangement of the power lines and the operation of the pixel circuits, therefore, the same components are denoted by the same reference characters, and any descriptions thereof will be omitted. Hereinafter, features and operations characteristic of the fourth embodiment will be described.

[0085] FIG. 13 is a diagram illustrating the connecting arrangement of power lines VP_i in the display device according to an implementation useful for understanding better the invention. The display device is provided with three common power lines 141 to 143 for connecting a power control circuit 4d to the power lines VP_i. The common power lines 141 to 143 are connected at one end to three output terminals, respectively, of the power control circuit 4d. Power lines VP_1 to $VP_{n/3}$ are connected to the common power line 141, power lines $VP_{(n/3+1)}$ to $VP_{(2n/3)}$ to the common power line 142, and power lines $VP_{(2n/3+1)}$ to VP_n to the common power line 143.

[0086] FIG. 14 is a diagram showing the operation of rows of pixel circuits 10 in the display device according to an implementation useful for understanding better the invention. The power control circuit 4d applies a low-level potential to the common power line 141 for a predetermined period of time at the beginning of a frame period, to the common power line 142 for a predetermined period of time after a third of the frame period, and to the common power line 143 for a predetermined period of time after another third of the frame period. Accordingly, the pixel circuits in the first through (n/3) 'th rows are initialized at the beginning of the frame period, the pixel circuits in the (n/3+1)'th to (2n/3)'th rows are initialized with a delay of a third of the frame period, and the pixel circuits in the (2n/3+1)'th to n'th rows are initialized with a delay of another third of the frame period.

[0087] Immediately after the first initialization, all of the pixel circuits in the first through (n/3)'th rows are selected simultaneously, immediately after the second initialization, all of the pixel circuits in the (n/3+1) 'th to (2n/3)'th rows are selected simultaneously, and immediately after the third initialization, all of the pixel circuits in the (2n/3+1)'th to n'th rows are selected simultaneously. The selected pixel circuits perform threshold detection.

[0088] After the first threshold detection, the pixel circuits in the first through (n/3)'th rows are sequentially selected, after the second threshold detection, the pixel circuits in the (n/3+1)'th to (2n/3) 'th rows are sequentially selected, and after the third threshold detection, the pixel circuits in the (2n/3+1)'th to n'th rows are sequentially selected. The selected pixel circuits perform writing. The pixel circuits in each row are lit up for a predetermined period of time T4 after the

writing, and they are unlit in other periods. In the example shown in FIG. 14, the scanning speed of the pixel circuits is the same as normal, and the emission period length T4 of the pixel circuits is about two thirds of a frame period.

[0089] Note that the number *p* of common power lines 9 may be four or more. Even when the number *p* is four or more, the connecting arrangement of the power lines VP_i and the operation of rows of pixel circuits 10 are the same as described above. Moreover, when the number *p* is three or more, (*n*/*p*) adjacently disposed power lines may be connected to the same common power line, or every (*p*-1)'th power line, in total (*n*/*p*) lines, may be connected to the same common power line. For example, where *p* = 3, every third power line VP_i may be selected, such that power lines VP_1, VP_4, and so on, are connected to the first common power line, power lines VP_2, VP_5, and so on, to the second common power line, and power lines VP_3, VP_6, and so on, to the third common power line. Moreover, where *p* = 1, *m* power lines may be provided so as to correspond to columns of pixel circuits 10 as shown in FIG. 8, rather than *n* power lines VP_i being provided so as to correspond to rows of pixel circuits 10. In addition, where *p* = *n,* the common power line 9 is substantially the same as the power line VP_i.

[0090] In this manner, there are tradeoffs among the number p of common power lines 9, the scanning speed of the pixel circuits 10, and the emission period length of the pixel circuits 10. For example, by increasing the number p of common power lines 9, it is rendered possible to lower the scanning speed of the pixel circuits 10 and extend the emission period of the pixel circuits 10. However, in such a case, the number of output buffers provided in the power control circuit 4 increases, resulting in an increased circuit scale of the power control circuit 4. Accordingly, these parameters need to be determined considering the specifications and cost of the display device.

[0091] As described above, in the display device the circuit scale of the power control circuit 4 can be reduced.

[0092] Furthermore, the display device 100 includes a plurality of pixel circuits 10 arranged in a matrix, a plurality of scanning signal lines G_i and control lines E_i provided so as to correspond to rows of pixel circuits 10, a plurality of data lines S_j provided so as to corresponding to columns of pixel circuits 10, a plurality of power lines VP_i provided to supply a power potential to the pixel circuits 10, *p* ($p \geq 1$) common power lines 9 connected to two or more power lines VP_i, a gate driver circuit 2 for driving the scanning signal lines G_i and the control lines E_i, a source driver circuit 3 for driving the data lines S_j and a power control circuit 4 for driving the power lines VP_i. Each pixel circuit 10 includes an organic EL element 16 (electro-optic element), a TFT 12 (drive transistor) provided in a path of current flowing through the organic EL element 16, a TFT 11 (write control transistor) provided between a gate terminal of the TFT 12 and the data line S_j, a TFT 13 (emission control transistor) provided between a drain terminal of the TFT 12 and the power line VP_i, and a capacitor 15 provided between a source terminal of the TFT 12 and the gate terminal. The power control circuit 4 applies a power potential and an initialization potential to the p common power lines 9 while switching therebetween. This configuration achieves the aforementioned effects.

[0093] The configuration and operation of a display device according to an implementation useful for understanding better the invention are approximately the same as those of the display device shown in FIG. 1, except for an initialization operation in accordance with a potential change of a video signal line, therefore, the same components are denoted by the same reference characters, and any descriptions thereof will be omitted. Hereinafter, features and operations characteristic of the fifth embodiment will be described.

[0094] FIG. 15 is a diagram showing a timing chart describing a method for driving a pixel circuit 20 according to an implementation useful for understanding better the invention. The operation of a pixel circuit in the first row will be described below with reference to FIG. 15. Note that characters shown in FIG. 15 denote the same as in FIG. 3.

[0095] The operation of the pixel circuit in the first row will now be described with reference to FIG. 15. The potential of power line VP_1 is kept at a constant power potential level without changing therefrom. Accordingly, the potential is not shown in FIG. 15. Prior to time t_{21}, the potentials of scanning signal line G_1 and control line E_1 are low level. Accordingly, the pixel circuit 10 is unlit, and source potential VS_1 of the TFT 12 is kept low at the same level as a cutoff voltage Vth_EL for the organic EL element 16 since no current is applied through power line VP_1.

[0096] At time t_{21}, a predetermined initialization voltage VH is applied to the data line S_j. The initialization voltage VH is a predetermined high-level signal voltage for reset, which changes the level of potential, as will be described later.

[0097] At time t_{22}, the potential of scanning signal line G_1 is set to high level, turning the TFT 11 on, so that the initialization voltage VH is written to the TFT 12 as gate potential VG_1. At this time, source potential VS_1 of the TFT 12 capacitively coupled by the capacitor 15 temporarily rises, but immediately after discharge occurs via the organic EL element 16, source potential VS_1 of the TFT 12 falls to the level of the cutoff voltage Vth_EL.

[0098] At time t_{23}, the potential of the data line S_j falls from the initialization voltage VH to the reference potential Vref with the TFT 11 on. Such a change in potential lowers the source potential of the TFT 12 capacitively coupled via the capacitor 15. Specifically, the gate-source voltage Vgs of the TFT 12 at and after time t_{23} can be obtained by the following equation (5).

$$Vgs = Vth\_EL - C_{st} / (C_{OLED} + C_{st}) \times (VH - Vref) \cdots (5)$$

[0099] Note that in equation (5), C_{OLED} is a capacitance value of the organic EL element 16, and C_{st} is a capacitance value of the capacitor 15.

[0100] Subsequently, from time t_{24} onward, threshold detection, writing, and light-emission operations are performed as described in connection with Fig. 3, and therefore, any descriptions of these subsequent operations will be omitted.

[0101] As described above, in the display device, an output buffer provided in the power control circuit 4 simply outputs a constant power potential and is not driven at all. Accordingly, the need for the capability to perform drive for a potential change is eliminated, resulting in a reduced circuit scale of the power control circuit 4.

[0102] In embodiments of the invention, the emission period starts not long after data writing, but the emission period may be determined so as to start simultaneously in the first through (*n*/2)'th rows and also in the (*n*/2+1)'th to *n*'th rows, as described in the example implementation of FIG. 6.

[0103] FIG. 16 is a diagram showing the connecting arrangement of control lines E_i in an embodiment of the invention. The display device shown in FIG. 16 is provided with two common control lines 221 and 222 for connecting a scanning signal line driver circuit 102b to the control lines E_i. The common control lines 221 and 222 are connected at one end to two output terminals, respectively, of the scanning signal line driver circuit 102b. Control lines E_1 to $E_{n/2}$ are connected to the common control line 221, and control lines $E_{(n/2+1)}$ to E_n are connected to the common control line 222.

[0104] FIG. 17 is a diagram showing the operation of rows of pixel circuits 10 in the display device according to an embodiment of the invention. As can be appreciated in comparison of the example shown in FIG. 17 with the example shown in FIG. 10, the initialization, threshold detection, and selection operations for the rows are performed in the same manner, but unlike in the example shown in FIG. 6, the emission period does not start simultaneously in all of the rows, however it starts simultaneously in the first through (*n*/2)'th rows, and then in the (*n*/2+1)'th to n'th rows.

[0105] In this manner, in this embodiment, the scanning speed of the pixel circuits can be set to be the same as normal, and therefore a sufficient amount of time can be ensured for writing as in the normal case. Moreover, leakage current from the TFT 12 can be approximately equalized among the pixel circuits 10 in the first through (*n*/2)'th rows and among the pixel circuits 10 in the (*n*/2+1)'th to n'th rows, and therefore the amount of decrease in luminance due to leakage current can be approximately equalized among the pixel circuits 10 in the first through (*n*/2) 'th rows and among the pixel circuits 10 in the (*n*/2+1) 'th to n'th rows, thereby inhibiting uneven display. In addition, since the scanning signal line driver circuit 102b uses only two control signal output terminals, a simplified configuration can be achieved, and further, since there are required only two common control lines, the area of wiring up to the control lines E_i can be reduced.

[0106] Furthermore, the emission period starts not long after data writing, but the emission period may be defined so as to start simultaneously in even rows and also in odd rows.

[0107] FIG. 18 is a diagram showing the connecting arrangement of control lines E_i in another embodiment of the invention. The display device shown in FIG. 18 is provided with two common control lines 231 and 232 for connecting a scanning signal line driver circuit 102c to the control lines E_i. The common control lines 231 and 232 are connected at one end to two output terminals, respectively, of the scanning signal line driver circuit 102c. Control lines E_1, E_3, and so on, in odd rows are connected to the common control line 231, and control lines E_2, E_4, and so on, in even rows are connected to the common control line 232.

[0108] FIG. 19 is a diagram showing the operation of rows of pixel circuits 10 in the display device according to an embodiment of the invention. As can be appreciated in comparison of the example shown in FIG. 19 with the example shown in FIG. 12, the initialization, threshold detection, and selection operations for the rows are performed in the same manner, but unlike in the example shown in FIG. 6, the emission period does not start simultaneously in all of the rows, however it starts simultaneously in even rows, and also in odd rows.

[0109] In this manner, in this embodiment, the scanning speed of the pixel circuits can be set to be the same as normal, and therefore a sufficient amount of time can be ensured for writing as in the normal case. Moreover, leakage current from the TFT 12 can be approximately equalized among the pixel circuits 10 in even rows and among the pixel circuits 10 in odd rows, and therefore the amount of decrease in luminance due to leakage current can be approximately equalized among them, thereby inhibiting uneven display. In addition, since the scanning signal line driver circuit 102c uses only two control signal output terminals, a simplified configuration can be achieved, and further, since there are required only two common control lines, the area of wiring up to the control lines E_i can be reduced.

[0110] Note that similarly to the implementations shown in FIGS. 13 and 14, the emission period can be controlled so as to start simultaneously in a manner as described above, although any detailed description thereof will be omitted herein, and therefore, this similar configuration makes it possible to achieve similar effects to those described above.

[0111] In the embodiments and example implementations above, normally, the capacitance value of the organic EL element 16 is considerably higher than that of the capacitor 15, but there can be conceived a configuration example where such a difference in capacitance value would not be extremely large. In such a case, the aforementioned transformation from equation (1) to equation (2) cannot be performed in a manner as described earlier (at least not with high accuracy), and therefore, it cannot be said that the gate-source voltage Vgs of the TFT 12 is approximately equal to (Vdat1 - Vref + Vth). Therefore, a configuration with an inserted auxiliary capacitor 25 as shown in FIG. 20 can be conceived.

[0112] FIG. 20 is a variant of the circuit diagram of the pixel circuit 10 shown in FIG. 2. As shown in FIG. 20, a pixel circuit 20 has approximately the same configuration as the pixel circuit 10 shown in FIG. 2, but the auxiliary capacitor 25 is additionally provided and connected parallel to the organic EL element 16. The auxiliary capacitor 25 has a capacitance value appropriately determined on the basis of the capacitance value of the organic EL element 16 and the capacitance value of the capacitor 15, and the relationship $C_{OLED} >> C_{st}$ is desirably established. As a result, equation (1) can be transformed to equation (2), and therefore, compensation accuracy can be enhanced by a simplified calculation process.

INDUSTRIAL APPLICABILITY

[0113] The present invention relates to display devices, and is suitable for display devices, such as an organic EL display, which include current-driven self-luminous elements, e.g., organic EL elements.

DESCRIPTION OF THE REFERENCE CHARACTERS

[0114]

1	display control circuit
2	gate driver circuit
3	source driver circuit
4	power control circuit
5	shift register
6	register
7	latch circuit
8	D/A converter
9	common power line
10, 20, 30	pixel circuit
11	TFT (write control transistor)
12	TFT (drive transistor)
13	TFT (emission control transistor)
15	capacitor
16	organic EL element (electro-optic element)
25	auxiliary capacitor
100	display device
G_i	scanning signal line
E_i	control line
S_j	data line
VP_i	power line

Claims

1. An active-matrix display device (100) comprising:

a plurality of video signal lines (Sj) for transmitting signals representing an image to be displayed;
a plurality of scanning signal lines (Gi) and control lines (Ei) crossing the video signal lines (Sj);
a plurality of pixel circuits (10, 20, 30) for forming the image to be displayed, the pixel circuits (10, 20, 30) being arranged in a matrix so as to correspond to intersections of the video signal lines (Sj) and the scanning signal lines (Gi);
a plurality of power lines (VPi) for supplying power potentials to the pixel circuits (10, 20, 30);
a scanning signal line driver circuit (2) for selectively or collectively driving the scanning signal lines (Gi) and the control lines (Ei);
a video signal line driver circuit (3) for driving the video signal lines (Sj) by applying thereto the signals representing the image to be displayed; and
a power control circuit (4) for driving the power lines (VPi), wherein,
wherein each of the pixel circuits (10, 20, 30) includes:

an electro-optic element (16) to be driven by current provided via one of the power lines (VPi) associated

with the respective pixel circuit (10, 20, 30);
a drive transistor (12) provided in a current path through the electro-optic element (16), to determine current that is to flow through the path;
a write control transistor (11) provided between a control terminal of the drive transistor (12) and one of the video signal lines (Sj) associated with the respective pixel circuit (10, 20, 30), to connect the control terminal of the drive transistor (12) and the one video signal line (Sj) when the scanning signal line driver circuit (2) drives and activates one of the scanning signal lines (Gi) associated with the respective pixel circuit (10, 20, 30);

wherein each of the pixel circuits (10, 20, 30) further includes an emission control transistor (13) provided between one conductive terminal of the drive transistor (12) and the one power line (VPi), to connect the conductive terminal and the one power line (VPi) when the scanning signal line driver circuit (2) drives and activates one of the control lines (Ei) associated with the respective pixel circuit (10, 20, 30); and
a capacitor (15) provided between the other conductive terminal of the drive transistor (12) and the control terminal;
characterized in that
the scanning signal line driver circuit (2) is adapted to:

collectively drive and activate the scanning signal lines (G_1-G_n) and the control lines (E_1-E_n) of in a initialization period and a threshold detection period that follows the initialization period, to initialize the electro-optic elements (16) of the pixel circuits (10) in the initialization period and to compensate for a threshold voltage of the drive transistors (12) of the pixel circuits (10) in the threshold detection period;
thereafter selectively drive the scanning signal lines (Gi) in a selection period for writing display data into the pixel circuits (10, 20, 30) selected by the scanning signal lines (G_1-G_n) , and
thereafter collectively drive the control lines (E_1-E_n) to display the image data in a emission period that simultaneously starts for the pixel circuits (10);

wherein the power control circuit (4) is adapted to provide the power lines (VPi) with initialization potentials to initialize the electro-optic elements (16) in the initialization period and with the power potentials different from the initialization potentials except in the initialization period, and
wherein the period from the end of threshold detection period to the start of the emission period is set to be equal for all rows.

2. An active-matrix display device (100) comprising:

a plurality of video signal lines (Sj) for transmitting signals representing an image to be displayed;
a plurality of scanning signal lines (Gi) and control lines (Ei) crossing the video signal lines (Sj);
a plurality of pixel circuits (10, 20, 30) for forming the image to be displayed, the pixel circuits (10, 20, 30) being arranged in a matrix so as to correspond to intersections of the video signal lines (Sj) and the scanning signal lines (Gi);
a plurality of power lines (VPi) for supplying power potentials to the pixel circuits (10, 20, 30);
a scanning signal line driver circuit (2) for selectively or collectively driving the scanning signal lines (Gi) and the control lines (Ei);
a video signal line driver circuit (3) for driving the video signal lines (Sj) by applying thereto the signals representing the image to be displayed; and
a power control circuit (4) for driving the power lines (VPi), wherein,
wherein each of the pixel circuits (10, 20, 30) includes:

an electro-optic element (16) to be driven by current provided via one of the power lines (VPi) associated with the respective pixel circuit (10, 20, 30);
a drive transistor (12) provided in a current path through the electro-optic element (16), to determine current that is to flow through the path;
a write control transistor (11) provided between a control terminal of the drive transistor (12) and one of the video signal lines (Sj) associated with the respective pixel circuit (10, 20, 30), to connect the control terminal of the drive transistor (12) and the one video signal line (Sj) when the scanning signal line driver circuit (2) drives and activates one of the scanning signal lines (Gi) associated with the respective pixel circuit (10, 20, 30);

wherein each of the pixel circuits (10, 20, 30) further includes an emission control transistor (13) provided between one conductive terminal of the drive transistor (12) and the one power line (VPi), to connect the conductive terminal and the one power line (VPi) when the scanning signal line driver circuit (2) drives and activates one of the control lines (Ei) associated with the respective pixel circuit (10, 20, 30); and
a capacitor (15) provided between the other conductive terminal of the drive transistor (12) and the control terminal;
characterized in that
there is a first group of scanning signal lines (G_1-$G_{n/2}$) and control lines (E_1-$E_{n/2}$) connected to a first subset of the pixel circuits (10, 20, 30), and second group of scanning signal lines ($G_{n/2+1}$-G_n) and control lines ($E_{n/2+1}$-E_n) connected to a second subset of the pixel circuits (10, 20, 30) different from said first group of the pixel circuits (10, 20, 30),
wherein the scanning signal line driver circuit (2) is adapted to:

collectively drive and activate the scanning signal lines (G_1-$G_{n/2}$) and the control lines (E_1-$E_{n/2}$) of the first group in a first initialization period and a first threshold detection period that follows the first initialization period, to initialize the electro-optic elements (16) of the first subset of pixel circuits (10) in the first initialization period and to compensate for a threshold voltage of the drive transistors (12) of the first subset of pixel circuits (10) in the first threshold detection period;
thereafter selectively drive the scanning signal lines (Gi) of the first group in a selection period for writing first display data into the first subset of pixel circuits (10, 20, 30) selected by the scanning signal lines (G_1-$G_{n/2}$) of the first group, and
thereafter collectively drive the control lines (E_1-$E_{n/2}$) of the first group to display the first image data in a first emission period that simultaneously starts for the first subset of pixel circuits (10), wherein the period from the end of first threshold detection period to the start of the first emission period is set to be equal for all rows of said first group, and
collectively drive and activate the scanning signal lines ($G_{n/2+1}$-G_n) and the control lines ($E_{n/2+1}$-E_n) of the second group in a second initialization period, different from the first initialization period, and a second threshold detection period, different from the first initialization period and that follows the second initialization period, to initialize the electro-optic elements (16) of the second subset of pixel circuits (10) in the second initialization period and to compensate for a threshold voltage of the drive transistors (12) of the second subset of pixel circuits (10) in the second threshold detection period;
thereafter selectively drive the scanning signal lines ($G_{n/2+1}$-G_n) of the second group in a second selection period, different from the first selection period, for writing second display data into the second subset of pixel circuits (10, 20, 30) selected by the scanning signal lines ($G_{n/2+1}$-G_n) of the second group, and
thereafter collectively drive the control lines ($E_{n/2+1}$-E_n) of the second group to display the second image data in a second emission period that simultaneously starts for the second subset of pixel circuits (10), wherein the period from the end of second threshold detection period to the start of the second emission period is set to be equal for all rows of said second group; and

wherein the power control circuit (4) is adapted to provide the power lines (VPi) with initialization potentials to initialize the electro-optic elements (16) in the initialization period and with the power potentials different from the initialization potentials except in the initialization period.

3. The display device (100) according to claim 2, wherein the scanning signal line driver circuit (2) is adapted to drive and activate, in the first and second emission periods, respectively, the control lines (Ei) corresponding to the scanning signal lines (Gi) of the first group and second group, such that the emission control transistors (13) of the first subset and second subset of pixels circuits (10, 20, 30), respectively, are made conductive approximately for the same duration.

4. The display device (100) according to claim 2, wherein the power lines (VPi) are sequentially provided one by one from the first group and second group to avoid any two power lines (VPi) corresponding to a pixel circuit (10, 20, 30) of the same subset being adjacent to each other.

5. The display device (100) according to claim 2, further comprising one first common power line (121) connected to the power lines (VPi) supplying power to the pixels of the first subset of pixel circuits (10, 20, 30), and one second common power line (122) connected to the power lines (VPi) supplying power to the pixels of the second subset of pixel circuits (10, 20, 30)
wherein in the first initialization period or in the second initialization period, the power control circuit (4) provides the

power lines (VPi) with initialization potentials via their respective corresponding first or second common power line (121, 122).

6. The display device (100) according to claim 1 or 2, further comprising an auxiliary capacitor (25) connected parallel to the electro-optic element (16).

7. A method for driving an active-matrix display device (100) of claim 1, the method comprising the steps of:

a scanning signal line driving step of selectively or collectively driving the scanning signal lines (Gi) and the control lines (Ei);
a video signal line driving step of driving the video signal lines (Sj) by applying thereto the signals representing the image to be displayed; and
a power control step of driving the power lines (VPi),
characterized by
a scanning signal line driver circuit (2) performs the steps of:

collectively driving and activating the scanning signal lines (G_1-G_n) and the control lines (E_1-E_n) of in a initialization period and a threshold detection period that follows the initialization period, to initialize the electro-optic elements (16) of the pixel circuits (10) in the initialization period and to compensate for a threshold voltage of the drive transistors (12) of the pixel circuits (10) in the threshold detection period;
thereafter selectively driving the scanning signal lines (Gi) in a selection period for writing display data into the pixel circuits (10, 20, 30) selected by the scanning signal lines (G_1-G_n);
thereafter collectively driving the control lines (E_1-E_n) to display the image data in a emission period that simultaneously starts for the pixel circuits (10); and

the method further comprises the step of providing the power lines (VPi) with initialization potentials to initialize the electro-optic elements (16) in the initialization period and with the power potentials different from the initialization potentials except in the initialization period.

8. A method for driving an active-matrix display device (100) of claim 2, the method comprising the steps of:

a scanning signal line driving step of selectively or collectively driving the scanning signal lines (Gi) and the control lines (Ei);
a video signal line driving step of driving the video signal lines (Sj) by applying thereto the signals representing the image to be displayed; and
a power control step of driving the power lines (VPi),
characterized in that
there is a first group of scanning signal lines (G_1-$G_{n/2}$) and the control lines (E_1-$E_{n/2}$) connected to a first subset of the pixel circuits (10, 20, 30), and second group of scanning signal lines ($G_{n/2+1}$-G_n) and the control lines ($E_{n/2+1}$-E_n) connected to a second subset of the pixel circuits (10, 20, 30) different from said first group of the pixel circuits (10, 20, 30), and
wherein the scanning signal line driver circuit (2) performs the following steps:

collectively driving and activating the scanning signal lines (G_1-$G_{n/2}$) and the control lines (E_1-$E_{n/2}$) of the first group in a first initialization period and a first threshold detection period that follows the first initialization period, to initialize the electro-optic elements (16) of the first subset of pixel circuits (10) in the first initialization period and to compensate for a threshold voltage of the drive transistors (12) of the first subset of pixel circuits (10) in the first threshold detection period;
thereafter selectively driving the scanning signal lines (Gi) of the first group in a selection period for writing first display data into the first subset of pixel circuits (10, 20, 30) selected by the scanning signal lines (G_1-$G_{n/2}$) of the first group, and
thereafter collectively driving the control lines (E_1-$E_{n/2}$) of the first group to display the first image data in a first emission period that simultaneously starts for the first subset of pixel circuits (10), wherein the period from the end of first threshold detection period to the start of the first emission period is set to be equal for all rows of said first group, and
collectively driving and activating the scanning signal lines ($G_{n/2+1}$-G_n) and the control lines ($E_{n/2+1}$-E_n) of the second group in a second initialization period, different from the first initialization period, and a second threshold detection period, different from the first initialization period and that follows the second initialization

period, to initialize the electro-optic elements (16) of the second subset of pixel circuits (10) in the second initialization period and to compensate for a threshold voltage of the drive transistors (12) of the second subset of pixel circuits (10) in the second threshold detection period;
thereafter selectively driving the scanning signal lines ($G_{n/2+1}$-G_n) of the second group in a second selection period, different from the first selection period, for writing second display data into the second subset of pixel circuits (10, 20, 30) selected by the scanning signal lines ($G_{n/2+1}$-G_n) of the second group, and
thereafter collectively driving the control lines ($E_{n/2+1}$-E_n) of the second group to display the second image data in a second emission period that simultaneously starts for the second subset of pixel circuits (10), wherein the period from the end of second threshold detection period to the start of the second emission period is set to be equal for all rows of said second group; and

the method further comprises providing, by the power control circuit (4), the power lines (VPi) with initialization potentials to initialize the electro-optic elements (16) in the initialization period and with the power potentials different from the initialization potentials except in the initialization period.

Patentansprüche

1. Aktivmatrixanzeigevorrichtung (100), die Folgendes umfasst:

eine Vielzahl von Videosignalleitungen (Sj) zum Übertragen von Signalen, die ein anzuzeigendes Bild repräsentieren;
eine Vielzahl von Abtastsignalleitungen (Gi) und Steuerleitungen (Ei), die die Videosignalleitungen (Sj) kreuzen;
eine Vielzahl von Pixelschaltungen (10, 20, 30) zum Bilden des anzuzeigenden Bildes, wobei die Pixelschaltungen (10, 20, 30) derart in einer Matrix angeordnet sind, dass sie Schnittpunkten der Videosignalleitungen (Sj) und der Abtastsignalleitungen (Gi) entsprechen;
eine Vielzahl von Leistungsleitungen (VPi) zum Liefern von Leistungspotenzialen an die Pixelschaltungen (10, 20, 30);
eine Abtastsignalleitungstreiberschaltung (2) zum selektiven oder kollektiven Ansteuern der Abtastsignalleitungen (Gi) und der Steuerleitungen (Ei);
eine Videosignalleitungstreiberschaltung (3) zum Ansteuern der Videosignalleitungen (Sj) durch Anlegen der Signale, die das anzuzeigende Bild repräsentieren, daran und
eine Leistungssteuerschaltung (4) zum Ansteuern der Leistungsleitungen (VPi),
wobei jede der Pixelschaltungen (10, 20, 30) Folgendes beinhaltet:

ein elektrooptisches Element (16), das von Strom anzusteuern ist, der via die Leistungsleitungen (VPi) bereitgestellt wird, die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft sind;
einen Ansteuertransistor (12), der in einem Strompfad durch das elektrooptische Element (16) bereitgestellt ist, um einen Strom, der durch den Pfad fließen soll, zu bestimmen;
einen Schreibsteuertransistor (11), der zwischen einem Steueranschluss des Ansteuertransistors (12) und einer der Videosignalleitungen (Sj), die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft ist, bereitgestellt ist, um den Steueranschluss des Ansteuertransistors (12) und die eine Videosignalleitung (Sj) zu verbinden, wenn die Abtastsignalleitungstreiberschaltung (2) eine der Abtastsignalleitungen (Gi), die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft ist, ansteuert und aktiviert;
wobei jede der Pixelschaltungen (10, 20, 30) ferner einen Emissionssteuertransistor (13) beinhaltet, der zwischen einem leitenden Anschluss des Ansteuertransistors (12) und der einen Leistungsleitung (VPi) bereitgestellt ist, um den leitenden Anschluss und die eine Leistungsleitung (VPi) zu verbinden, wenn die Abtastsignalleitungstreiberschaltung (2) eine der Steuerleitungen (Ei), die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft ist, ansteuert und aktiviert; und
einen Kondensator (15), der zwischen dem leitenden Anschluss des Ansteuertransistors (12) und dem Steueranschluss bereitgestellt ist;
dadurch gekennzeichnet ist, dass
die Abtastsignalleitungstreiberschaltung (2) zu Folgendem angepasst ist:

kollektives Ansteuern und Aktivieren der Abtastsignalleitungen (G_1-G_n) und der Steuerleitungen (E_1-E_n) in einer Initialisierungsperiode und einer Schwellwertdetektionsperiode, die der Initialisierungsperiode folgt, um die elektrooptischen Elemente (16) der Pixelschaltungen (10) in der Initialisierungsperiode zu initialisieren und um eine Schwellwertspannung der Ansteuertransistoren (12) der Pixelschaltungen

(10) in der Schwellwertdetektionsperiode zu kompensieren;
danach selektives Ansteuern der Abtastsignalleitungen (Gi) in einer Auswahlperiode zum Schreiben von Anzeigedaten in die Pixelschaltungen (10, 20, 30), die von den Abtastsignalleitungen (G_1-G_n) ausgewählt werden, und
danach kollektives Ansteuern der Steuerleitungen (E_1-E_n), um in einer Emissionsperiode, die für die Pixelschaltungen (10) gleichzeitig beginnt, die Bilddaten anzuzeigen;
wobei die Leistungssteuerschaltung (4) angepasst ist, den Leistungsleitungen (VPi) Initialisierungspotenziale bereitzustellen, um die elektrooptischen Elemente (16) in der Initialisierungsperiode zu initialisieren, und wobei sich die Leistungspotenziale außer in der Initialisierungsperiode von den Initialisierungspotenzialen unterscheiden, und
wobei die Periode vom Ende der Schwellwertdetektionsperiode bis zum Beginn der Emissionsperiode derart eingestellt ist, dass sie für alle Zeilen gleich ist.

2. Aktivmatrixanzeigevorrichtung (100), die Folgendes umfasst:

eine Vielzahl von Videosignalleitungen (Sj) zum Übertragen von Signalen, die ein anzuzeigendes Bild repräsentieren;
eine Vielzahl von Abtastsignalleitungen (Gi) und Steuerleitungen (Ei), die die Videosignalleitungen (Sj) kreuzen;
eine Vielzahl von Pixelschaltungen (10, 20, 30) zum Bilden des anzuzeigenden Bildes, wobei die Pixelschaltungen (10, 20, 30) derart in einer Matrix angeordnet sind, dass sie Schnittpunkten der Videosignalleitungen (Sj) und der Abtastsignalleitungen (Gi) entsprechen;
eine Vielzahl von Leistungsleitungen (VPi) zum Liefern von Leistungspotenzialen an die Pixelschaltungen (10, 20, 30);
eine Abtastsignalleitungstreiberschaltung (2) zum selektiven oder kollektiven Ansteuern der Abtastsignalleitungen (Gi) und der Steuerleitungen (Ei);
eine Videosignalleitungstreiberschaltung (3) zum Ansteuern der Videosignalleitungen (Sj) durch Anlegen der Signale, die das anzuzeigende Bild repräsentieren, daran und
eine Leistungssteuerschaltung (4) zum Ansteuern der Leistungsleitungen (VPi), wobei
wobei jede der Pixelschaltungen (10, 20, 30) Folgendes beinhaltet:

ein elektrooptisches Element (16), das von Strom anzusteuern ist, der via die Leistungsleitungen (VPi) bereitgestellt wird, die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft sind;
einen Ansteuertransistor (12), der in einem Strompfad durch das elektrooptische Element (16) bereitgestellt ist, um einen Strom, der durch den Pfad fließen soll, zu bestimmen;
einen Schreibsteuertransistor (11), der zwischen einem Steueranschluss des Ansteuertransistors (12) und einer der Videosignalleitungen (Sj), die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft ist, bereitgestellt ist, um den Steueranschluss des Ansteuertransistors (12) und die eine Videosignalleitung (Sj) zu verbinden, wenn die Abtastsignalleitungstreiberschaltung (2) eine der Abtastsignalleitungen (Gi), die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft ist, ansteuert und aktiviert;
wobei jede der Pixelschaltungen (10, 20, 30) ferner einen Emissionssteuertransistor (13) beinhaltet, der zwischen einem leitenden Anschluss des Ansteuertransistors (12) und der einen Leistungsleitung (VPi) bereitgestellt ist, um den leitenden Anschluss und die eine Leistungsleitung (VPi) zu verbinden, wenn die Abtastsignalleitungstreiberschaltung (2) eine der Steuerleitungen (Ei), die mit der jeweiligen Pixelschaltung (10, 20, 30) verknüpft ist, ansteuert und aktiviert; und
einen Kondensator (15), der zwischen dem leitenden Anschluss des Ansteuertransistors (12) und dem Steueranschluss bereitgestellt ist;
dadurch gekennzeichnet ist, dass
es eine erste Gruppe von Abtastsignalleitungen (G_1-$G_{n/2}$) und Steuerleitungen (E_1-$E_{n/2}$), die mit einem ersten Untersatz der Pixelschaltungen (10, 20, 30) verbunden sind, und eine zweite Gruppe von Abtastsignalleitungen ($G_{n/2+1}$-G_n) und Steuerleitungen ($E_{n/2+1}$-E_n), die mit einem zweiten Untersatz der Pixelschaltungen (10, 20, 30) verbunden sind, die sich von der ersten Gruppe der Pixelschaltungen (10, 20, 30) unterscheidet, gibt,
wobei die Abtastsignalleitungstreiberschaltung (2) zu Folgendem angepasst ist:

kollektives Ansteuern und Aktivieren der Abtastsignalleitungen (G_1-$G_{n/2}$) und der Steuerleitungen (E_1-$E_{n/2}$) der ersten Gruppe in einer ersten Initialisierungsperiode und einer ersten Schwellwertdetektionsperiode, die der ersten Initialisierungsperiode folgt, um die elektrooptischen Elemente (16) des ersten Untersatzes von Pixelschaltungen (10) in der ersten Initialisierungsperiode zu initialisieren und

um eine Schwellwertspannung der Ansteuertransistoren (12) des ersten Untersatzes von Pixelschaltungen (10) in der ersten Schwellwertdetektionsperiode zu kompensieren;
danach selektives Ansteuern der Abtastsignalleitungen (Gi) der ersten Gruppe in einer Auswahlperiode zum Schreiben von ersten Anzeigedaten in den ersten Untersatz von Pixelschaltungen (10, 20, 30), die von den Abtastsignalleitungen (G_1-$G_{n/2}$) der ersten Gruppe ausgewählt werden, und
danach kollektives Ansteuern der Steuerleitungen (E_1-$E_{n/2}$) der ersten Gruppe, um in einer ersten Emissionsperiode, die für den ersten Untersatz von Pixelschaltungen (10) gleichzeitig beginnt, die ersten Bilddaten anzuzeigen, wobei die Periode vom Ende der ersten Schwellwertdetektionsperiode bis zum Beginn der ersten Emissionsperiode derart eingestellt ist, dass sie für alle Zeilen der ersten Gruppe gleich ist, und
kollektives Ansteuern und Aktivieren der Abtastsignalleitungen ($G_{n/2+1}$-G_n) und der Steuerleitungen ($E_{n/2+1}$-E_n) der zweiten Gruppe in einer zweiten Initialisierungsperiode, die sich von der ersten Initialisierungsperiode unterscheidet, und einer zweiten Schwellwertdetektionsperiode, die sich von der ersten Initialisierungsperiode unterscheidet und die der zweiten Initialisierungsperiode folgt, um die elektrooptischen Elemente (16) des zweiten Untersatzes von Pixelschaltungen (10) in der zweiten Initialisierungsperiode zu initialisieren und um eine Schwellwertspannung der Ansteuertransistoren (12) des zweiten Untersatzes von Pixelschaltungen (10) in der zweiten Schwellwertdetektionsperiode zu kompensieren;
danach selektives Ansteuern der Abtastsignalleitungen ($G_{n/2+1}$-G_n) der zweiten Gruppe in einer zweiten Auswahlperiode, die sich von der ersten Auswahlperiode unterscheidet, zum Schreiben von zweiten Anzeigedaten in den zweiten Untersatz von Pixelschaltungen (10, 20, 30), die von den Abtastsignalleitungen ($G_{n/2+1}$-G_n) der zweiten Gruppe ausgewählt werden, und
danach kollektives Ansteuern der Steuerleitungen ($E_{n/2+1}$-E_n) der zweiten Gruppe, um in einer zweiten Emissionsperiode, die für den zweiten Untersatz von Pixelschaltungen (10) gleichzeitig beginnt, die zweiten Bilddaten anzuzeigen, wobei die Periode vom Ende der zweiten Schwellwertdetektionsperiode bis zum Beginn der zweiten Emissionsperiode derart eingestellt ist, dass sie für alle Zeilen der zweiten Gruppe gleich ist; und
wobei die Leistungssteuerschaltung (4) angepasst ist, den Leistungsleitungen (VPi) Initialisierungspotenziale bereitzustellen, um die elektrooptischen Elemente (16) in der Initialisierungsperiode zu initialisieren, und wobei sich die Leistungspotenziale außer in der Initialisierungsperiode von den Initialisierungspotenzialen unterscheiden.

3. Anzeigevorrichtung (100) nach Anspruch 2, wobei die Abtastsignalleitungstreiberschaltung (2) angepasst ist, die Steuerleitungen (Ei), die den Abtastsignalleitungen (Gi) der ersten Gruppe und der zweiten Gruppe entsprechen, in der ersten bzw. der zweiten Emissionsperiode anzusteuern und zu aktivieren, derart, dass die Emissionssteuertransistoren (13) des ersten Untersatzes bzw. des zweiten Untersatzes von Pixelschaltungen (10, 20, 30) für ungefähr dieselbe Dauer leitend gemacht werden.

4. Anzeigevorrichtung (100) nach Anspruch 2, wobei die Leistungsleitungen (VPi) sequenziell eine nach der anderen von der ersten Gruppe und der zweiten Gruppe bereitgestellt werden, um zu vermeiden, dass zwei Leistungsleitungen (VPi), die einer Pixelschaltung (10, 20, 30) desselben Untersatzes entsprechen, einander benachbart sind.

5. Anzeigevorrichtung (100) nach Anspruch 2, die ferner eine erste gemeinsame Leistungsleitung (121), die mit den Leistungsleitungen (VPi) verbunden ist, die Strom an die Pixel des ersten Untersatzes von Pixelschaltungen (10, 20, 30) liefern, und eine zweite gemeinsame Leistungsleitung (122), die mit den Leistungsleitungen (VPi) verbunden ist, die Strom an die Pixel des zweiten Untersatzes von Pixelschaltungen (10, 20, 30) liefern, umfasst wobei die Leistungssteuerschaltung (4) den Leistungsleitungen (VPi) in der ersten Initialisierungsperiode oder in der zweiten Initialisierungsperiode via deren jeweilige entsprechende erste oder zweite gemeinsame Leistungsleitung (121, 122) Initialisierungspotenziale bereitstellt.

6. Anzeigevorrichtung (100) nach Anspruch 1 oder 2, die ferner einen Hilfskondensator (25) umfasst, der parallel mit dem elektrooptischen Element (16) verbunden ist.

7. Verfahren zum Ansteuern einer Aktivmatrixanzeigevorrichtung (100) nach Anspruch 1, wobei das Verfahren die folgenden Schritte umfasst:

einen Abtastsignalleitungsansteuerschritt zum selektiven oder kollektiven Ansteuern der Abtastsignalleitungen (Gi) und der Steuerleitungen (Ei);

einen Videosignalleitungsansteuerschritt zum Ansteuern der Videosignalleitungen (Sj) durch Anlegen der Signale, die das anzuzeigende Bild repräsentieren, daran und
einen Leistungssteuerschritt zum Ansteuern der Leistungsleitungen (VPi),
dadurch gekennzeichnet, dass
eine Abtastsignalleitungstreiberschaltung (2) die folgenden Schritte durchführt:

kollektives Ansteuern und Aktivieren der Abtastsignalleitungen (G_1-G_n) und der Steuerleitungen (E_1-E_n) in einer Initialisierungsperiode und einer Schwellwertdetektionsperiode, die der Initialisierungsperiode folgt, um die elektrooptischen Elemente (16) der Pixelschaltungen (10) in der Initialisierungsperiode zu initialisieren und um eine Schwellwertspannung der Ansteuertransistoren (12) der Pixelschaltungen (10) in der Schwellwertdetektionsperiode zu kompensieren;
danach selektives Ansteuern der Abtastsignalleitungen (Gi) in einer Auswahlperiode zum Schreiben von Anzeigedaten in die Pixelschaltungen (10, 20, 30), die von den Abtastsignalleitungen (G_1-G_n) ausgewählt werden;
danach kollektives Ansteuern der Steuerleitungen (E_1-E_n), um in einer Emissionsperiode, die für die Pixelschaltungen (10) gleichzeitig beginnt, die Bilddaten anzuzeigen; und
das Verfahren ferner den Schritt des Bereitstellens von Initialisierungspotenzialen für die Leistungsleitungen (VPi), um die elektrooptischen Elemente (16) in der Initialisierungsperiode zu initialisieren, umfasst, und wobei sich die Leistungspotenziale außer in der Initialisierungsperiode von den Initialisierungspotenzialen unterscheiden.

8. Verfahren zum Ansteuern einer Aktivmatrixanzeigevorrichtung (100) nach Anspruch 2, wobei das Verfahren die folgenden Schritte umfasst:

einen Abtastsignalleitungsansteuerschritt zum selektiven oder kollektiven Ansteuern der Abtastsignalleitungen (Gi) und der Steuerleitungen (Ei);
einen Videosignalleitungsansteuerschritt zum Ansteuern der Videosignalleitungen (Sj) durch Anlegen der Signale, die das anzuzeigende Bild repräsentieren, daran und
einen Leistungssteuerschritt zum Ansteuern der Leistungsleitungen (VPi),
dadurch gekennzeichnet ist, dass
es eine erste Gruppe von Abtastsignalleitungen (G_1-$G_{n/2}$) und den Steuerleitungen (E_1-$E_{n/2}$), die mit einem ersten Untersatz der Pixelschaltungen (10, 20, 30) verbunden sind, und eine zweite Gruppe von Abtastsignalleitungen ($G_{n/2+1}$-G_n) und den Steuerleitungen ($E_{n/2+1}$-E_n), die mit einem zweiten Untersatz der Pixelschaltungen (10, 20, 30)verbunden sind, die sich von der ersten Gruppe der Pixelschaltungen (10, 20, 30) unterscheidet, gibt, und
wobei die Abtastsignalleitungstreiberschaltung (2) die folgenden Schritte durchführt:

kollektives Ansteuern und Aktivieren der Abtastsignalleitungen (G_1-$G_{n/2}$) und der Steuerleitungen (E_1-$E_{n/2}$) der ersten Gruppe in einer ersten Initialisierungsperiode und einer ersten Schwellwertdetektionsperiode, die der ersten Initialisierungsperiode folgt, um die elektrooptischen Elemente (16) des ersten Untersatzes von Pixelschaltungen (10) in der ersten Initialisierungsperiode zu initialisieren und um eine Schwellwertspannung der Ansteuertransistoren (12) des ersten Untersatzes von Pixelschaltungen (10) in der ersten Schwellwertdetektionsperiode zu kompensieren;
danach selektives Ansteuern der Abtastsignalleitungen (Gi) der ersten Gruppe in einer Auswahlperiode zum Schreiben von ersten Anzeigedaten in den ersten Untersatz von Pixelschaltungen (10, 20, 30), die von den Abtastsignalleitungen (G_1-$G_{n/2}$) der ersten Gruppe ausgewählt werden, und
danach kollektives Ansteuern der Steuerleitungen (E_1-$E_{n/2}$) der ersten Gruppe, um in einer ersten Emissionsperiode, die für den ersten Untersatz von Pixelschaltungen (10) gleichzeitig beginnt, die ersten Bilddaten anzuzeigen, wobei die Periode vom Ende der ersten Schwellwertdetektionsperiode bis zum Beginn der ersten Emissionsperiode derart eingestellt ist, dass sie für alle Zeilen der ersten Gruppe gleich ist, und
kollektives Ansteuern und Aktivieren der Abtastsignalleitungen ($G_{n/2+1}$-G_n) und der Steuerleitungen ($E_{n/2+1}$-E_n) der zweiten Gruppe in einer zweiten Initialisierungsperiode, die sich von der ersten Initialisierungsperiode unterscheidet, und einer zweiten Schwellwertdetektionsperiode, die sich von der ersten Initialisierungsperiode unterscheidet und die der zweiten Initialisierungsperiode folgt, um die elektrooptischen Elemente (16) des zweiten Untersatzes von Pixelschaltungen (10) in der zweiten Initialisierungsperiode zu initialisieren und um eine Schwellwertspannung der Ansteuertransistoren (12) des zweiten Untersatzes von Pixelschaltungen (10) in der zweiten Schwellwertdetektionsperiode zu kompensieren;
danach selektives Ansteuern der Abtastsignalleitungen ($G_{n/2+1}$-G_n) der zweiten Gruppe in einer zweiten

Auswahlperiode, die sich von der ersten Auswahlperiode unterscheidet, zum Schreiben von zweiten Anzeigedaten in den zweiten Untersatz von Pixelschaltungen (10, 20, 30), die von den Abtastsignalleitungen ($G_{n/2+1}$-G_n) der zweiten Gruppe ausgewählt werden, und

danach kollektives Ansteuern der Steuerleitungen ($E_{n/2+1}$-E_n) der zweiten Gruppe, um in einer zweiten Emissionsperiode, die für den zweiten Untersatz von Pixelschaltungen (10) gleichzeitig beginnt, die zweiten Bilddaten anzuzeigen, wobei die Periode vom Ende der zweiten Schwellwertdetektionsperiode bis zum Beginn der zweiten Emissionsperiode derart eingestellt ist, dass sie für alle Zeilen der zweiten Gruppe gleich ist; und

das Verfahren ferner das Bereitstellen von Initialisierungspotenzialen für die Leistungsleitungen (VPi), um die elektrooptischen Elemente (16) in der Initialisierungsperiode zu initialisieren, durch die Leistungssteuerschaltung (4) umfasst, und wobei sich die Leistungspotenziale außer in der Initialisierungsperiode von den Initialisierungspotenzialen unterscheiden.

Revendications

1. Dispositif d'affichage à matrice active (100) comprenant :

une pluralité de lignes de signaux vidéo (Sj) pour transmettre des signaux représentant une image à afficher ;
une pluralité de lignes de signaux de balayage (Gi) et de lignes de commande (Ei) croisant les lignes de signaux vidéo (Sj) ;
une pluralité de circuits de pixels (10, 20, 30) pour former l'image à afficher, les circuits de pixels (10, 20, 30) étant agencés en une matrice de manière à correspondre à des intersections des lignes de signaux vidéo (Sj) et des lignes de signaux de balayage (Gi) ;
une pluralité de lignes de puissance (VPi) pour fournir des potentiels de puissance aux circuits de pixels (10, 20, 30) ;
un circuit d'attaque de lignes de signaux de balayage (2) pour attaquer sélectivement ou collectivement les lignes de signaux de balayage (Gi) et les lignes de commande (Ei) ;
un circuit d'attaque de lignes de signaux vidéo (3) pour attaquer les lignes de signaux vidéo (Sj) en leur appliquant les signaux représentant l'image à afficher ; et
un circuit de commande de puissance (4) pour attaquer les lignes de puissance (VPi), dans lequel,
chacun des circuits de pixels (10, 20, 30) inclut :

un élément électro-optique (16) devant être attaqué par un courant fourni par l'intermédiaire de l'une des lignes de puissance (VPi) associées au circuit de pixels respectif (10, 20, 30) ;
un transistor d'attaque (12) fourni dans un trajet de courant à travers l'élément électro-optique (16), en vue de déterminer un courant qui doit circuler à travers le trajet ;
un transistor de commande d'écriture (11) fourni entre une borne de commande du transistor d'attaque (12) et l'une des lignes de signaux vidéo (Sj) associées au circuit de pixels respectif (10, 20, 30), pour connecter la borne de commande du transistor d'attaque (12) et ladite une ligne de signaux vidéo (Sj) lorsque le circuit d'attaque de lignes de signaux de balayage (2) attaque et active l'une des lignes de signaux de balayage (Gi) associées au circuit de pixels respectif (10, 20, 30) ;
dans lequel chacun des circuits de pixels (10, 20, 30) inclut en outre un transistor de commande d'émission (13) fourni entre une borne conductrice du transistor d'attaque (12) et ladite une ligne de puissance (VPi), pour connecter la borne conductrice et ladite une ligne de puissance (VPi) lorsque le circuit d'attaque de lignes de signaux de balayage (2) attaque et active l'une des lignes de commande (Ei) associées au circuit de pixels respectif (10, 20, 30) ; et
un condensateur (15) fourni entre l'autre borne conductrice du transistor d'attaque (12) et la borne de commande ;
caractérisé en ce que :
le circuit d'attaque de lignes de signaux de balayage (2) est apte à :

attaquer et activer collectivement les lignes de signaux de balayage (G_l-G_n) et les lignes de commande (E_l-E_n) dans une période d'initialisation et une période de détection de seuil qui suit la période d'initialisation, pour initialiser les éléments électro-optiques (16) des circuits de pixels (10) dans la période d'initialisation et pour compenser une tension de seuil des transistors d'attaque (12) des circuits de pixels (10) dans la période de détection de seuil ;
subséquemment, attaquer sélectivement les lignes de signaux de balayage (Gi) dans une période de

sélection pour écrire des données d'affichage dans les circuits de pixels (10, 20, 30) sélectionnés par les lignes de signaux de balayage (G_l-G_n) ; et
subséquemment, attaquer collectivement les lignes de commande (E_l-E_n) en vue d'afficher les données d'image dans une période d'émission qui commence simultanément pour les circuits de pixels (10) ;
dans lequel le circuit de commande de puissance (4) est apte à fournir, aux lignes de puissance (VPi), des potentiels d'initialisation pour initialiser les éléments électro-optiques (16) dans la période d'initialisation, et des potentiels de puissance différents des potentiels d'initialisation hormis dans la période d'initialisation ; et
dans lequel la période entre la fin de la période de détection de seuil et le début de la période d'émission est définie de manière à être égale pour toutes les rangées.

2. Dispositif d'affichage à matrice active (100) comprenant :

une pluralité de lignes de signaux vidéo (Sj) pour transmettre des signaux représentant une image à afficher ;
une pluralité de lignes de signaux de balayage (Gi) et de lignes de commande (Ei) croisant les lignes de signaux vidéo (Sj) ;
une pluralité de circuits de pixels (10, 20, 30) pour former l'image à afficher, les circuits de pixels (10, 20, 30) étant agencés en une matrice de manière à correspondre à des intersections des lignes de signaux vidéo (Sj) et des lignes de signaux de balayage (Gi) ;
une pluralité de lignes de puissance (VPi) pour fournir des potentiels de puissance aux circuits de pixels (10, 20, 30) ;
un circuit d'attaque de lignes de signaux de balayage (2) pour attaquer sélectivement ou collectivement les lignes de signaux de balayage (Gi) et les lignes de commande (Ei) ;
un circuit d'attaque de lignes de signaux vidéo (3) pour attaquer les lignes de signaux vidéo (Sj) en leur appliquant les signaux représentant l'image à afficher ; et
un circuit de commande de puissance (4) pour attaquer les lignes de puissance (VPi), dans lequel,
chacun des circuits de pixels (10, 20, 30) inclut :

un élément électro-optique (16) devant être attaqué par un courant fourni par l'intermédiaire de l'une des lignes de puissance (VPi) associées au circuit de pixels respectif (10, 20, 30) ;
un transistor d'attaque (12) fourni dans un trajet de courant à travers l'élément électro-optique (16), en vue de déterminer un courant qui doit circuler à travers le trajet ;
un transistor de commande d'écriture (11) fourni entre une borne de commande du transistor d'attaque (12) et l'une des lignes de signaux vidéo (Sj) associées au circuit de pixels respectif (10, 20, 30), pour connecter la borne de commande du transistor d'attaque (12) et ladite une ligne de signaux vidéo (Sj) lorsque le circuit d'attaque de lignes de signaux de balayage (2) attaque et active l'une des lignes de signaux de balayage (Gi) associées au circuit de pixels respectif (10, 20, 30) ;
dans lequel chacun des circuits de pixels (10, 20, 30) inclut en outre un transistor de commande d'émission (13) fourni entre une borne conductrice du transistor d'attaque (12) et ladite une ligne de puissance (VPi), pour connecter la borne conductrice et ladite une ligne de puissance (VPi) lorsque le circuit d'attaque de lignes de signaux de balayage (2) attaque et active l'une des lignes de commande (Ei) associées au circuit de pixels respectif (10, 20, 30) ; et
un condensateur (15) fourni entre l'autre borne conductrice du transistor d'attaque (12) et la borne de commande ;
caractérisé en ce que :

il existe un premier groupe de lignes de signaux de balayage (G_l-$G_{n/2}$) et de lignes de commande (E_l-$E_{n/2}$) connectées à un premier sous-ensemble des circuits de pixels (10, 20, 30), et un second groupe de lignes de signaux de balayage ($G_{n/2+l}$-G_n) et de lignes de commande ($E_{n/2+l}$-E_n) connectées à un second sous-ensemble des circuits de pixels (10, 20, 30) différent dudit premier groupe des circuits de pixels (10, 20, 30) ;
dans lequel le circuit d'attaque de lignes de signaux de balayage (2) est apte à :

attaquer et activer collectivement les lignes de signaux de balayage (G_l-$G_{n/2}$) et les lignes de commande (E_l-$E_{n/2}$) du premier groupe dans une première période d'initialisation et une première période de détection de seuil qui suit la première période d'initialisation, pour initialiser les éléments électro-optiques (16) du premier sous-ensemble de circuits de pixels (10) dans la première période d'initialisation, et pour compenser une tension de seuil des transistors d'attaque (12) du premier

sous-ensemble de circuits de pixels (10) dans la première période de détection de seuil ;
subséquemment, attaquer sélectivement les lignes de signaux de balayage (Gi) du premier groupe dans une période de sélection pour écrire des premières données d'affichage dans le premier sous-ensemble de circuits de pixels (10, 20, 30) sélectionné par les lignes de signaux de balayage (G_l-$G_{n/2}$) du premier groupe ; et
subséquemment, attaquer collectivement les lignes de commande (E_l-$E_{n/2}$) du premier groupe en vue d'afficher les premières données d'image dans une première période d'émission qui commence simultanément pour le premier sous-ensemble de circuits de pixels (10), dans lequel la période entre la fin de la première période de détection de seuil et le début de la première période d'émission est définie de manière à être égale pour toutes les rangées dudit premier groupe ; et
attaquer et activer collectivement les lignes de signaux de balayage ($G_{n/2+l}$-G_n) et les lignes de commande ($E_{n/2+l}$-E_n) du second groupe dans une seconde période d'initialisation, différente de la première période d'initialisation, et dans une seconde période de détection de seuil, différente de la première période d'initialisation et qui suit la seconde période d'initialisation, pour initialiser les éléments électro-optiques (16) du second sous-ensemble de circuits de pixels (10) dans la seconde période d'initialisation et pour compenser une tension de seuil des transistors d'attaque (12) du second sous-ensemble de circuits de pixels (10) dans la seconde période de détection de seuil ;
subséquemment, attaquer sélectivement les lignes de signaux de balayage ($G_{n/2+l}$-G_n) du second groupe dans une seconde période de sélection, différente de la première période de sélection, pour écrire des secondes données d'affichage dans le second sous-ensemble de circuits de pixels (10, 20, 30) sélectionné par les lignes de signaux de balayage ($G_{n/2+l}$-G_n) du second groupe ; et
subséquemment, attaquer collectivement les lignes de commande ($E_{n/2+l}$-E_n) du second groupe pour afficher les secondes données d'image dans une seconde période d'émission qui commence simultanément pour le second sous-ensemble de circuits de pixels (10), dans lequel la période entre la fin de la seconde période de détection de seuil et le début de la seconde période d'émission est définie de manière à être égale pour toutes les rangées dudit second groupe ; et
dans lequel le circuit de commande de puissance (4) est apte à fournir, aux lignes de puissance (VPi), des potentiels d'initialisation pour initialiser les éléments électro-optiques (16) dans la période d'initialisation, et des potentiels de puissance différents des potentiels d'initialisation hormis dans la période d'initialisation.

3. Dispositif d'affichage (100) selon la revendication 2, dans lequel le circuit d'attaque de lignes de signaux de balayage (2) est apte à attaquer et activer, dans les première et seconde périodes d'émission, respectivement, les lignes de commande (Ei) correspondant aux lignes de signaux de balayage (Gi) du premier groupe et du second groupe, de sorte que des transistors de commande d'émission (13) du premier sous-ensemble et du second sous-ensemble de circuits de pixels (10, 20, 30), respectivement, sont rendus conducteurs approximativement pour la même durée.

4. Dispositif d'affichage (100) selon la revendication 2, dans lequel les lignes de puissance (VPi) sont fournies séquentiellement, une par une, à partir du premier groupe et du second groupe, pour éviter que deux lignes de puissance (VPi) quelconques correspondant à un circuit de pixels (10, 20, 30) du même sous-ensemble soient mutuellement adjacentes.

5. Dispositif d'affichage (100) selon la revendication 2, comprenant en outre une première ligne de puissance commune (121) connectée aux lignes de puissance (VPi) alimentant les pixels du premier sous-ensemble de circuits de pixels (10, 20, 30), et une seconde ligne de puissance commune (122) connectée aux lignes de puissance (VPi) alimentant les pixels du second sous-ensemble de circuits de pixels (10, 20, 30) ;
dans lequel, dans la première période d'initialisation ou dans la seconde période d'initialisation, le circuit de commande de puissance (4) fournit, aux lignes de puissance (VPi), des potentiels d'initialisation, par l'intermédiaire de leur première ou seconde ligne de puissance commune correspondante respective (121, 122).

6. Dispositif d'affichage (100) selon la revendication 1 ou 2, comprenant en outre un condensateur auxiliaire (25) connecté en parallèle à l'élément électro-optique (16).

7. Procédé d'attaque d'un dispositif d'affichage à matrice active (100) selon la revendication 1, le procédé comprenant les étapes ci-dessous :

une étape d'attaque de lignes de signaux de balayage consistant à attaquer sélectivement ou collectivement

les lignes de signaux de balayage (Gi) et les lignes de commande (Ei) ;
une étape d'attaque de lignes de signaux vidéo consistant à attaquer les lignes de signaux vidéo (Sj) en leur appliquant les signaux représentant l'image à afficher ; et
une étape de commande de puissance consistant à attaquer les lignes de puissance (VPi) ;
caractérisé en ce que :
un circuit d'attaque de lignes de signaux de balayage (2) met en œuvre les étapes ci-dessous consistant à :

attaquer et activer collectivement les lignes de signaux de balayage (G_l-G_n) et les lignes de commande (E_l-E_n) dans une période d'initialisation et une période de détection de seuil qui suit la période d'initialisation, pour initialiser les éléments électro-optiques (16) des circuits de pixels (10) dans la période d'initialisation et pour compenser une tension de seuil des transistors d'attaque (12) des circuits de pixels (10) dans la période de détection de seuil ;
subséquemment, attaquer sélectivement les lignes de signaux de balayage (Gi) dans une période de sélection pour écrire des données d'affichage dans les circuits de pixels (10, 20, 30) sélectionnés par les lignes de signaux de balayage (G_l-G_n) ;
subséquemment, attaquer collectivement les lignes de commande (E_l-E_n) en vue d'afficher les données d'image dans une période d'émission qui commence simultanément pour les circuits de pixels (10) ; et
dans lequel le procédé comprend en outre l'étape consistant à fournir, aux lignes de puissance (VPi), des potentiels d'initialisation pour initialiser les éléments électro-optiques (16) dans la période d'initialisation, et des potentiels de puissance différents des potentiels d'initialisation hormis dans la période d'initialisation.

8. Procédé d'attaque d'un dispositif d'affichage à matrice active (100) selon la revendication 2, le procédé comprenant les étapes ci-dessous consistant à :

une étape d'attaque de lignes de signaux de balayage consistant à attaquer sélectivement ou collectivement les lignes de signaux de balayage (Gi) et les lignes de commande (Ei) ;
une étape d'attaque de lignes de signaux vidéo consistant à attaquer les lignes de signaux vidéo (Sj) en leur appliquant les signaux représentant l'image à afficher ; et
une étape de commande de puissance consistant à attaquer les lignes de puissance (VPi) ;
caractérisé en ce que :

il existe un premier groupe de lignes de signaux de balayage (G_l-$G_{n/2}$) et de lignes de commande (E_l-$E_{n/2}$) connectées à un premier sous-ensemble des circuits de pixels (10, 20, 30), et un second groupe de lignes de signaux de balayage ($G_{n/2+l}$-G_n) et de lignes de commande ($E_{n/2+l}$-E_n) connectées à un second sous-ensemble des circuits de pixels (10, 20, 30) différent dudit premier groupe des circuits de pixels (10, 20, 30) ; et
dans lequel le circuit d'attaque de lignes de signaux de balayage (2) met en œuvre les étapes ci-dessous consistant à :

attaquer et activer collectivement les lignes de signaux de balayage (G_l-$G_{n/2}$) et les lignes de commande (E_l-$E_{n/2}$) du premier groupe dans une première période d'initialisation et une première période de détection de seuil qui suit la première période d'initialisation, pour initialiser les éléments électro-optiques (16) du premier sous-ensemble de circuits de pixels (10) dans la première période d'initialisation, et pour compenser une tension de seuil des transistors d'attaque (12) du premier sous-ensemble de circuits de pixels (10) dans la première période de détection de seuil ;
subséquemment, attaquer sélectivement les lignes de signaux de balayage (Gi) du premier groupe dans une période de sélection pour écrire des premières données d'affichage dans le premier sous-ensemble de circuits de pixels (10, 20, 30) sélectionné par les lignes de signaux de balayage (G_l-$G_{n/2}$) du premier groupe ; et
subséquemment, attaquer collectivement les lignes de commande (E_l-$E_{n/2}$) du premier groupe en vue d'afficher les premières données d'image dans une première période d'émission qui commence simultanément pour le premier sous-ensemble de circuits de pixels (10), dans lequel la période entre la fin de la première période de détection de seuil et le début de la première période d'émission est définie de manière à être égale pour toutes les rangées dudit premier groupe ; et
attaquer et activer collectivement les lignes de signaux de balayage ($G_{n/2+l}$-G_n) et les lignes de commande ($E_{n/2+l}$-E_n) du second groupe dans une seconde période d'initialisation, différente de la première période d'initialisation, et dans une seconde période de détection de seuil, différente de la première période d'initialisation et qui suit la seconde période d'initialisation, pour initialiser les éléments électro-

optiques (16) du second sous-ensemble de circuits de pixels (10) dans la seconde période d'initialisation et pour compenser une tension de seuil des transistors d'attaque (12) du second sous-ensemble de circuits de pixels (10) dans la seconde période de détection de seuil ;

subséquemment, attaquer sélectivement les lignes de signaux de balayage ($G_{n/2+l}$-G_n) du second groupe dans une seconde période de sélection, différente de la première période de sélection, pour écrire des secondes données d'affichage dans le second sous-ensemble de circuits de pixels (10, 20, 30) sélectionné par les lignes de signaux de balayage ($G_{n/2+l}$-G_n) du second groupe ; et

subséquemment, attaquer collectivement les lignes de commande ($E_{n/2+l}$-E_n) du second groupe pour afficher les secondes données d'image dans une seconde période d'émission qui commence simultanément pour le second sous-ensemble de circuits de pixels (10), dans lequel la période entre la fin de la seconde période de détection de seuil et le début de la seconde période d'émission est définie de manière à être égale pour toutes les rangées dudit second groupe ; et

dans lequel le procédé comprend en outre l'étape consistant à fournir, par le biais du circuit de commande de puissance (4), aux lignes de puissance (VPi), des potentiels d'initialisation pour initialiser les éléments électro-optiques (16) dans la période d'initialisation, et des potentiels de puissance différents des potentiels d'initialisation hormis dans la période d'initialisation.

FIG. 1

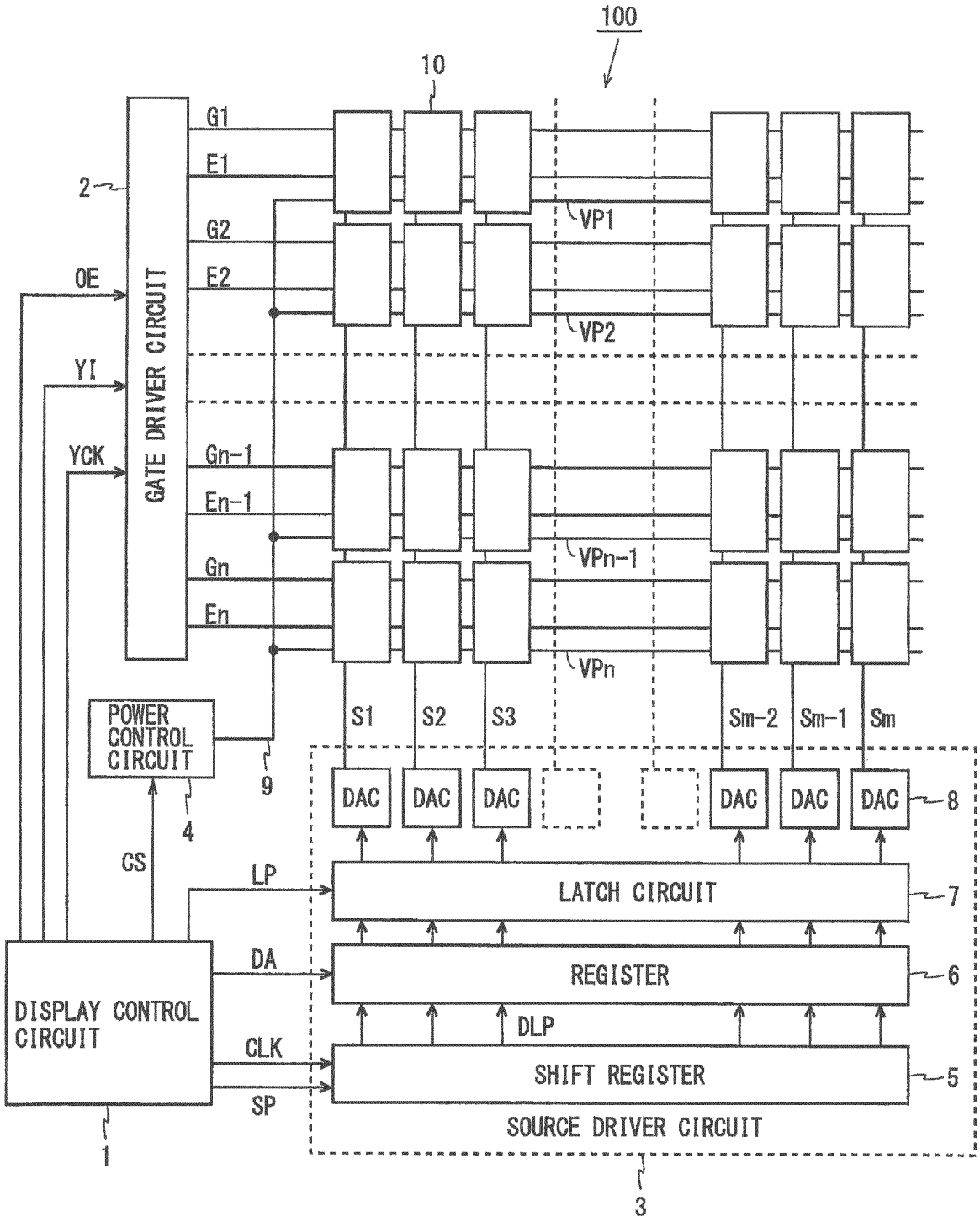

100
10
G1
E1
G2
E2
Gn-1
En-1
Gn
En
VP1
VP2
VPn-1
VPn
2
GATE DRIVER CIRCUIT
OE
YI
YCK
POWER CONTROL CIRCUIT
4
9
CS
S1
S2
S3
Sm-2
Sm-1
Sm
DAC
8
LP
LATCH CIRCUIT
7
DA
REGISTER
6
DLP
CLK
SHIFT REGISTER
5
SP
SOURCE DRIVER CIRCUIT
3
DISPLAY CONTROL CIRCUIT
1

FIG. 2

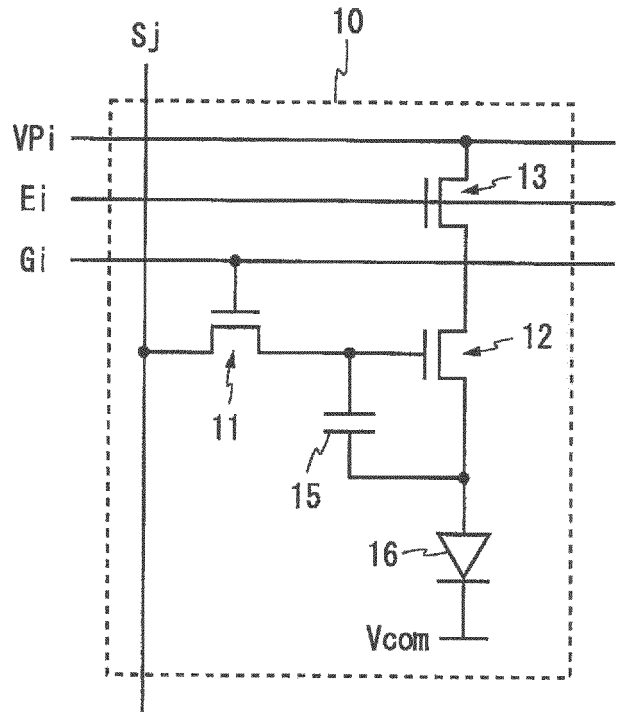


FIG. 3

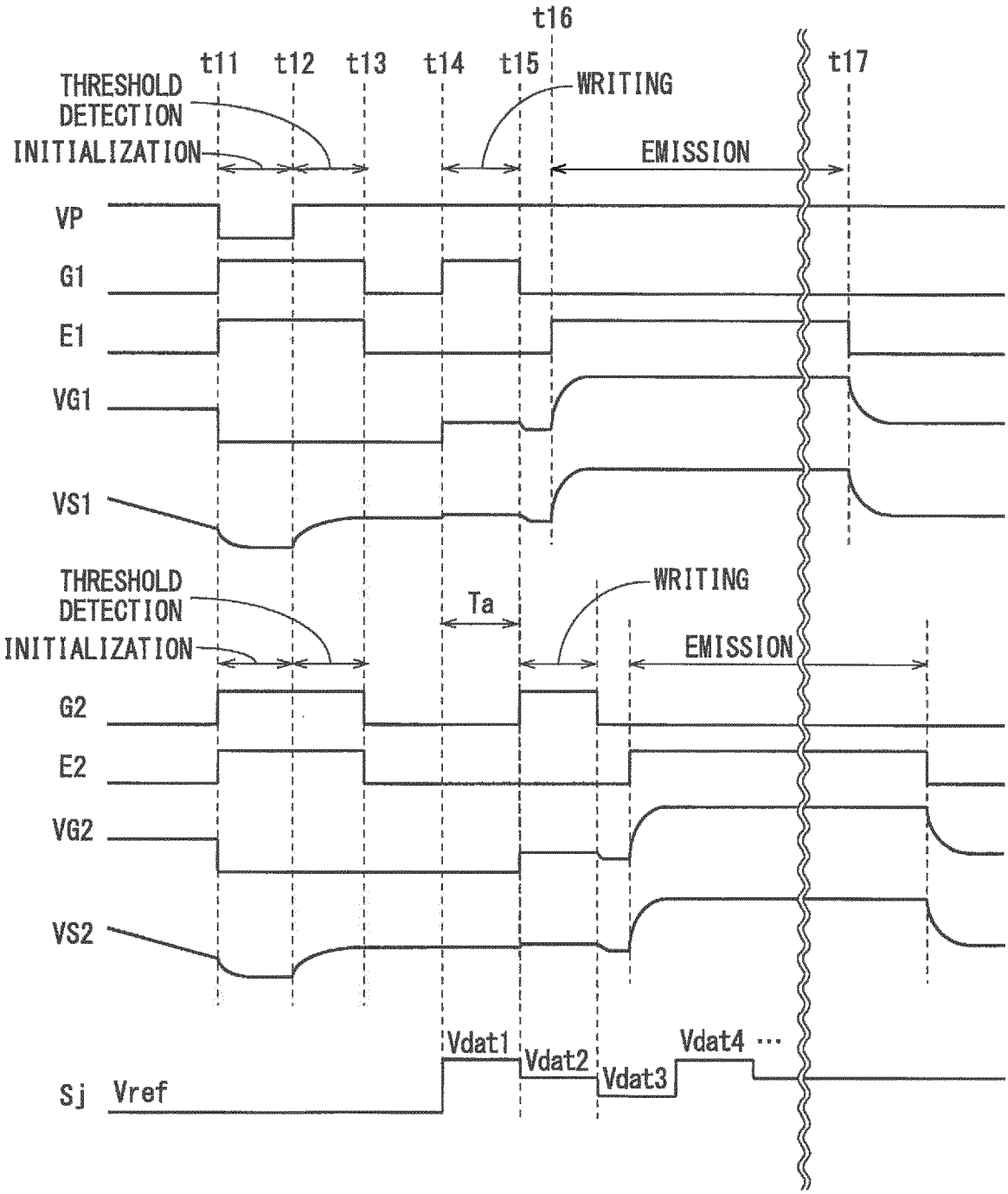

t11
t12
t13
t14
t15
t16
t17
THRESHOLD DETECTION
INITIALIZATION
WRITING
EMISSION
VP
G1
E1
VG1
VS1
THRESHOLD DETECTION
INITIALIZATION
Ta
WRITING
EMISSION
G2
E2
VG2
VS2
Sj
Vref
Vdat1
Vdat2
Vdat3
Vdat4 ···

FIG. 4

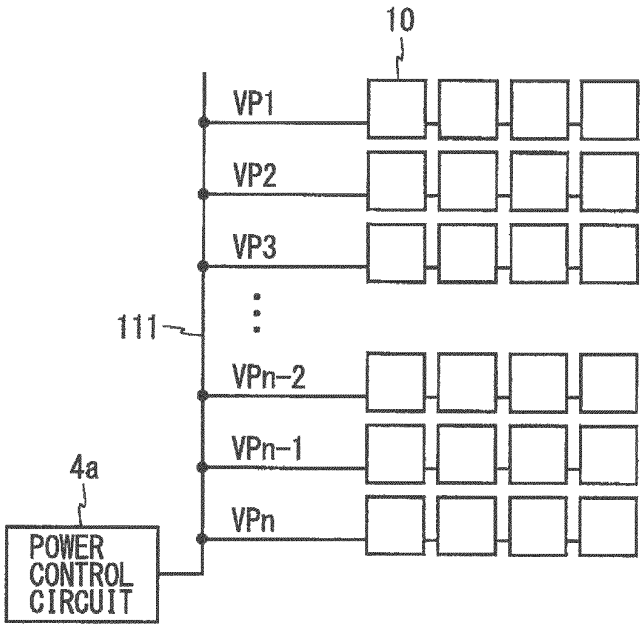

10
VP1
VP2
VP3
111
VPn-2
VPn-1
VPn
4a
POWER CONTROL CIRCUIT

FIG. 5

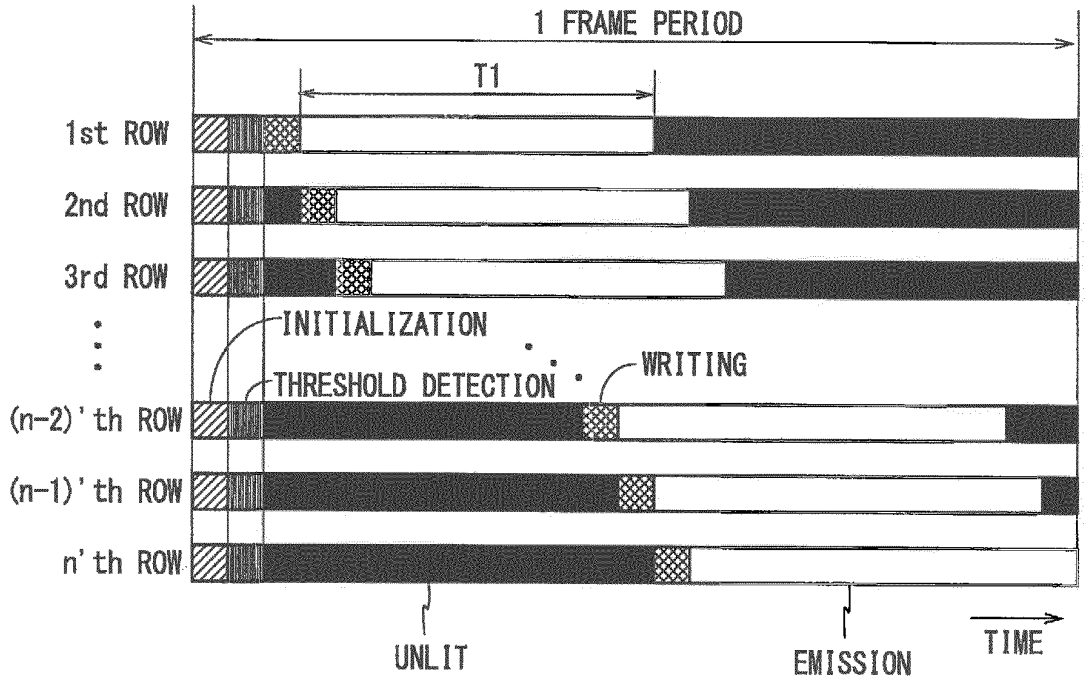

1 FRAME PERIOD
T1
1st ROW
2nd ROW
3rd ROW
INITIALIZATION
THRESHOLD DETECTION
WRITING
(n-2)'th ROW
(n-1)'th ROW
n'th ROW
UNLIT
EMISSION
TIME

FIG. 6

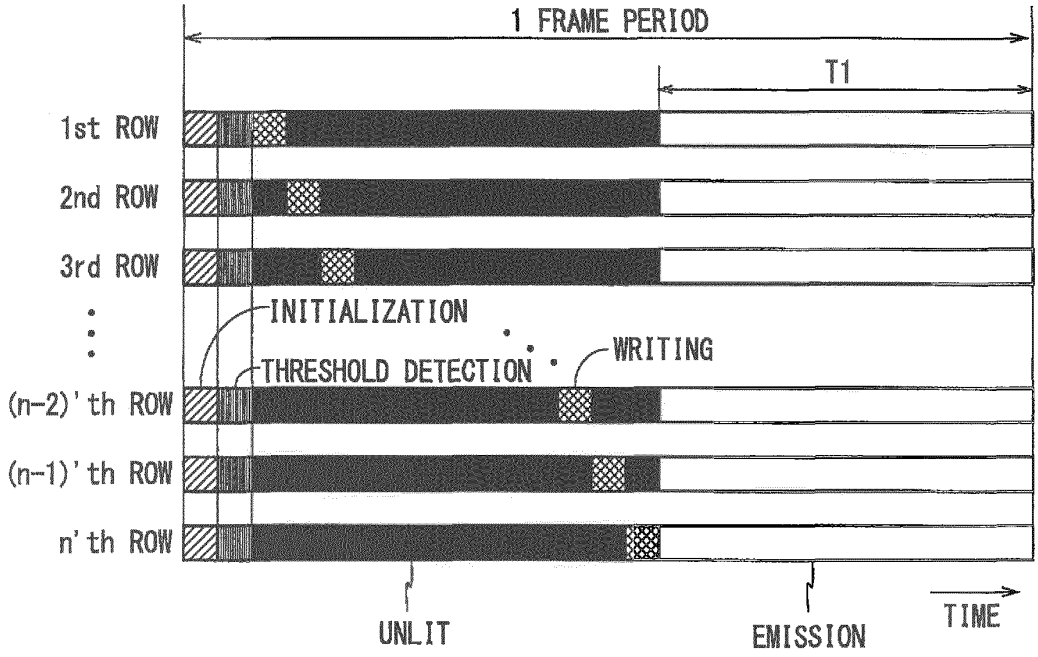

1 FRAME PERIOD
T1
1st ROW
2nd ROW
3rd ROW
INITIALIZATION
THRESHOLD DETECTION
WRITING
(n-2)'th ROW
(n-1)'th ROW
n'th ROW
UNLIT
EMISSION
TIME

FIG. 7

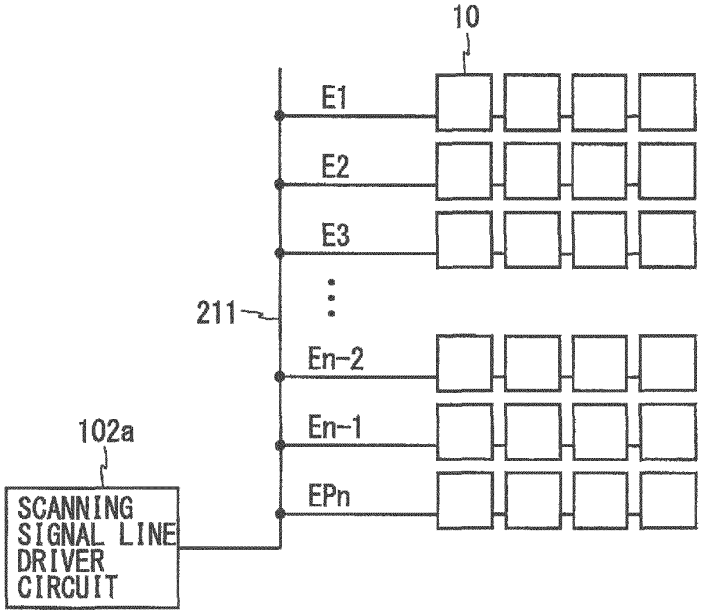

10
E1
E2
E3
211
En-2
En-1
EPn
102a
SCANNING SIGNAL LINE DRIVER CIRCUIT

FIG. 8

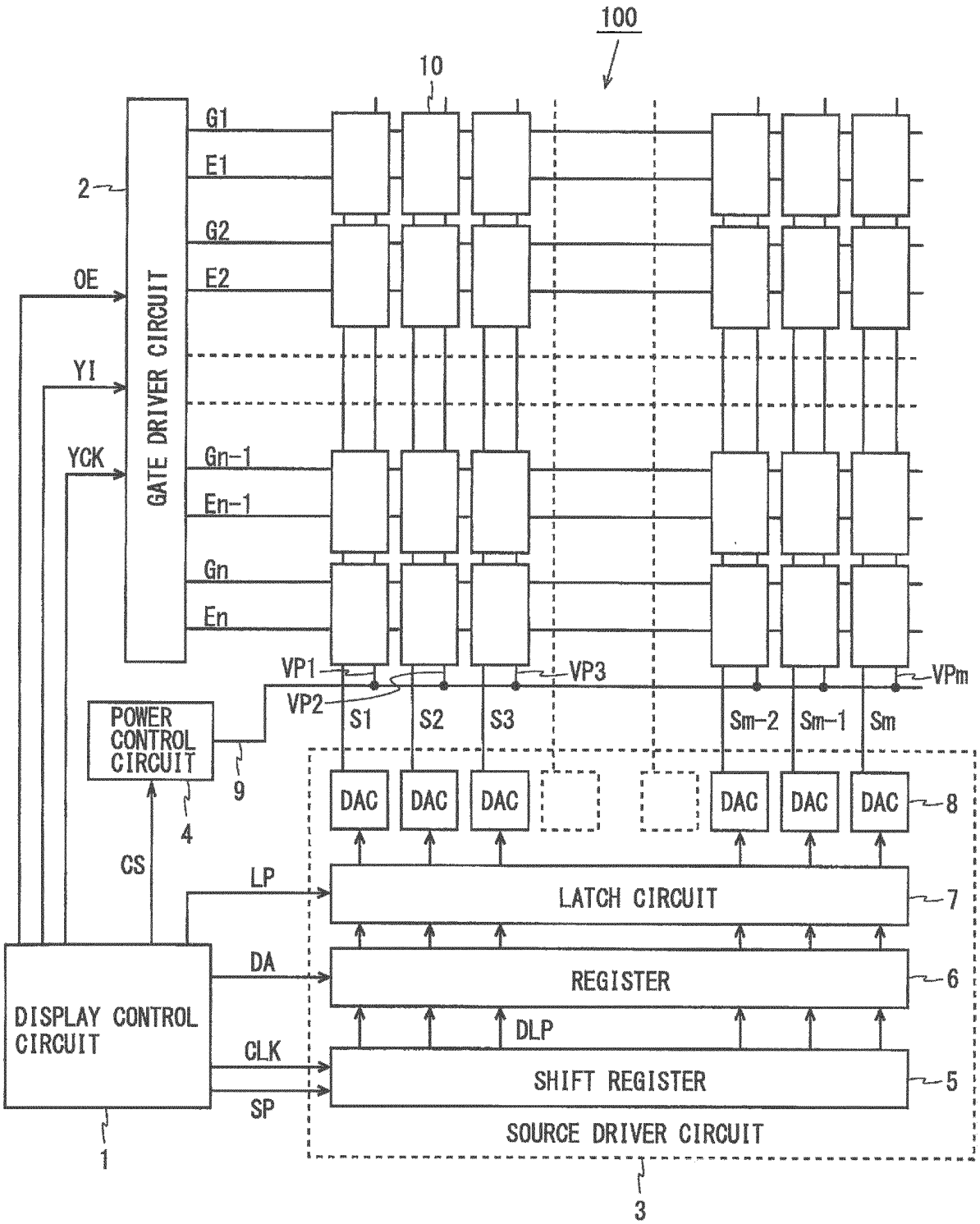

100
10
G1
E1
G2
E2
Gn-1
En-1
Gn
En
2
GATE DRIVER CIRCUIT
OE
YI
YCK
VP1
VP2
VP3
VPm
S1
S2
S3
Sm-2
Sm-1
Sm
POWER CONTROL CIRCUIT
9
4
DAC
8
CS
LP
LATCH CIRCUIT
7
DA
REGISTER
6
DLP
DISPLAY CONTROL CIRCUIT
CLK
SHIFT REGISTER
5
SP
SOURCE DRIVER CIRCUIT
1
3

FIG. 9

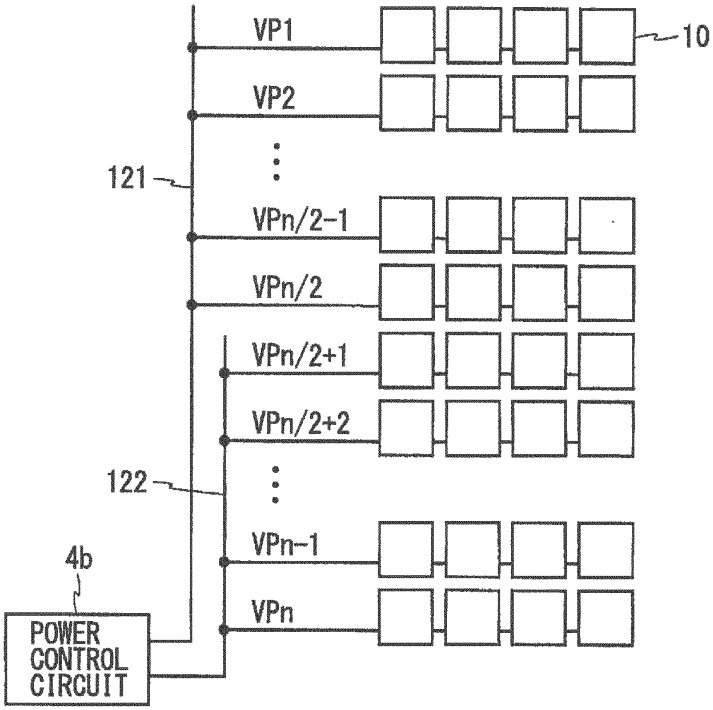

VP1
10
VP2
121
VPn/2-1
VPn/2
VPn/2+1
VPn/2+2
122
VPn-1
4b
VPn
POWER CONTROL CIRCUIT

FIG. 10

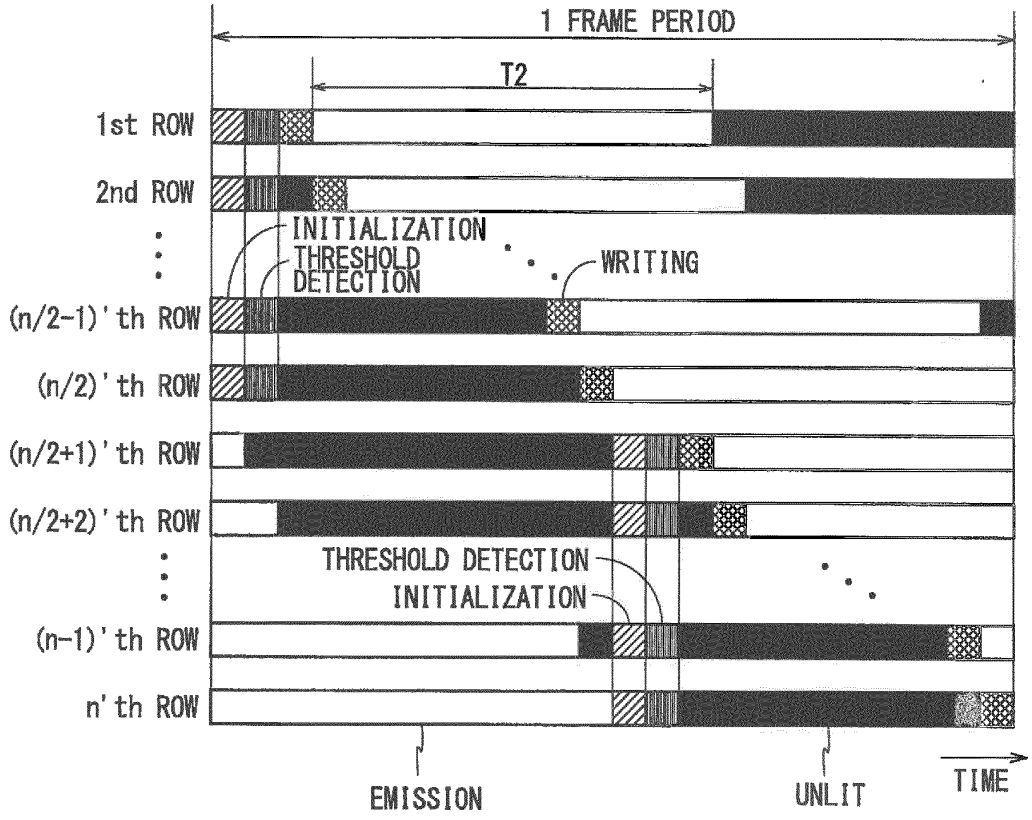

1 FRAME PERIOD
T2
1st ROW
2nd ROW
INITIALIZATION
THRESHOLD DETECTION
WRITING
(n/2-1)'th ROW
(n/2)'th ROW
(n/2+1)'th ROW
(n/2+2)'th ROW
THRESHOLD DETECTION
INITIALIZATION
(n-1)'th ROW
n'th ROW
EMISSION
UNLIT
TIME

FIG. 11

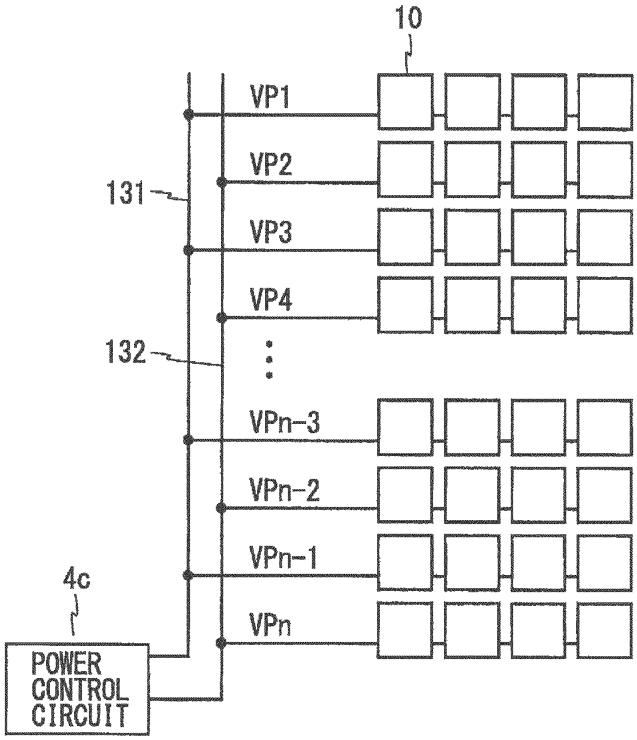

10
VP1
VP2
131
VP3
VP4
132
VPn-3
VPn-2
VPn-1
4c
VPn
POWER CONTROL CIRCUIT

FIG. 12

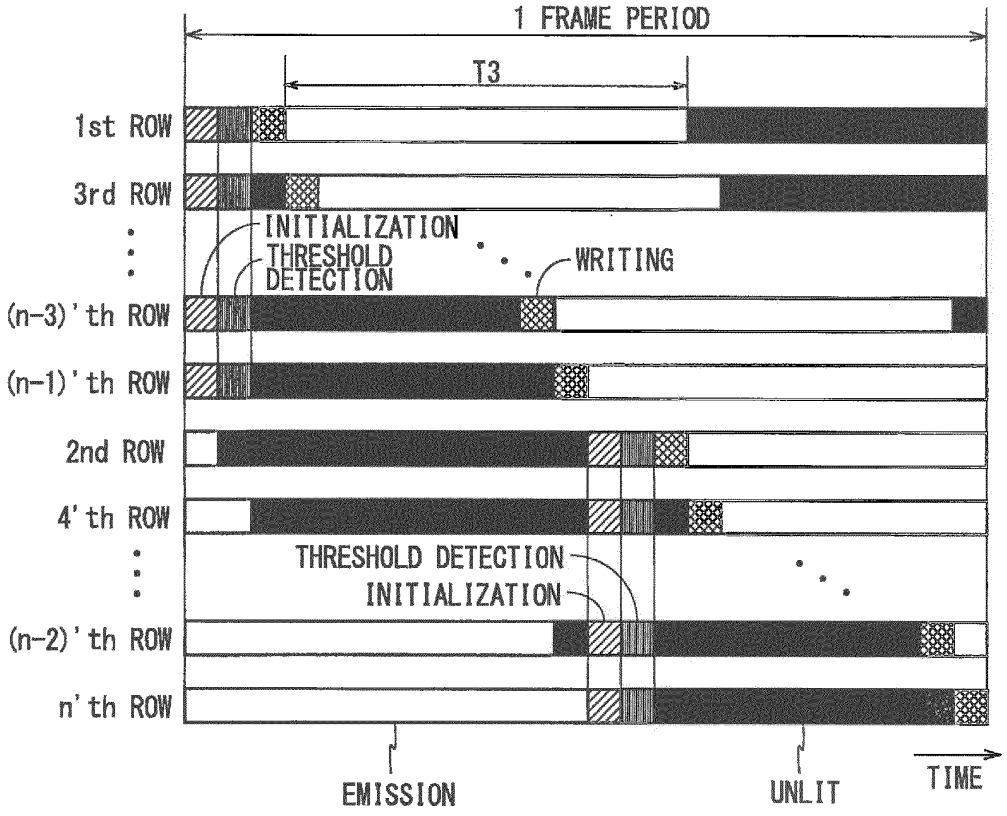

1 FRAME PERIOD
T3
1st ROW
3rd ROW
INITIALIZATION
THRESHOLD DETECTION
WRITING
(n-3)'th ROW
(n-1)'th ROW
2nd ROW
4'th ROW
THRESHOLD DETECTION
INITIALIZATION
(n-2)'th ROW
n'th ROW
EMISSION
UNLIT
TIME

FIG. 13

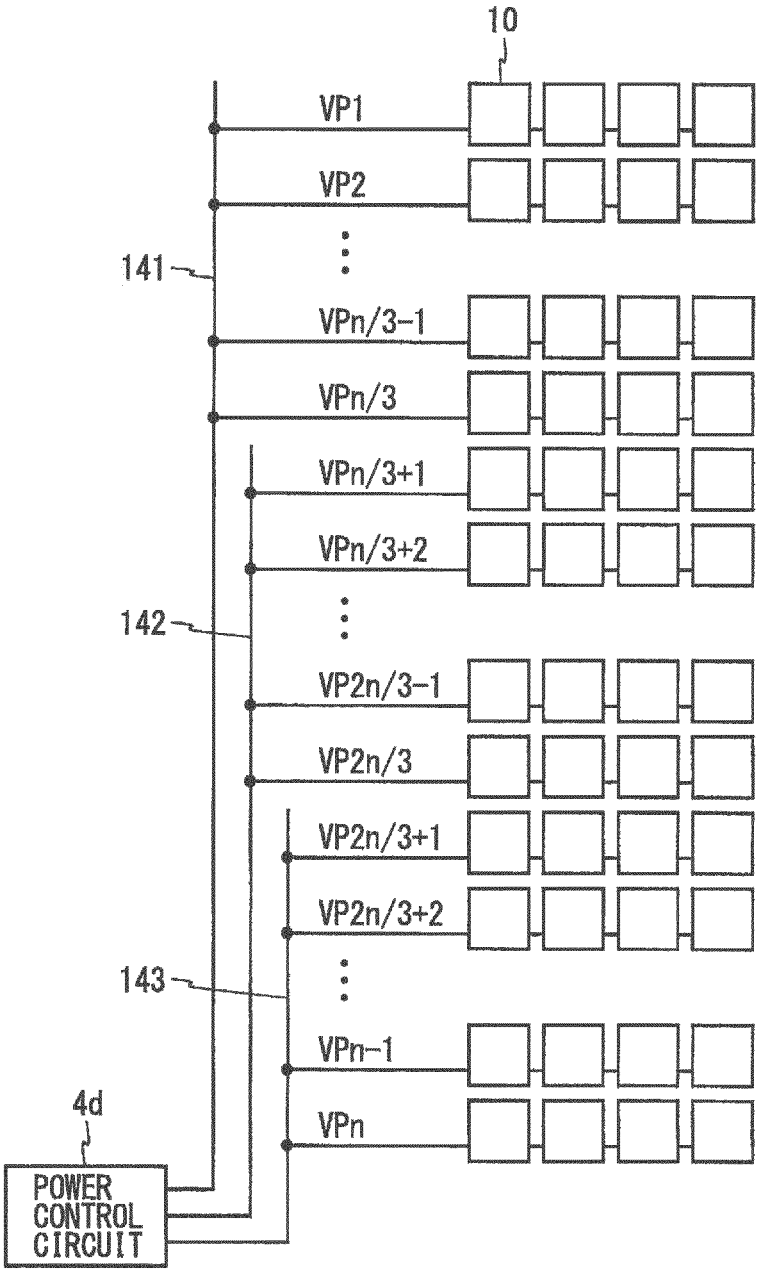

10
VP1
VP2
141
VPn/3-1
VPn/3
VPn/3+1
VPn/3+2
142
VP2n/3-1
VP2n/3
VP2n/3+1
VP2n/3+2
143
VPn-1
VPn
4d
POWER CONTROL CIRCUIT

FIG. 14

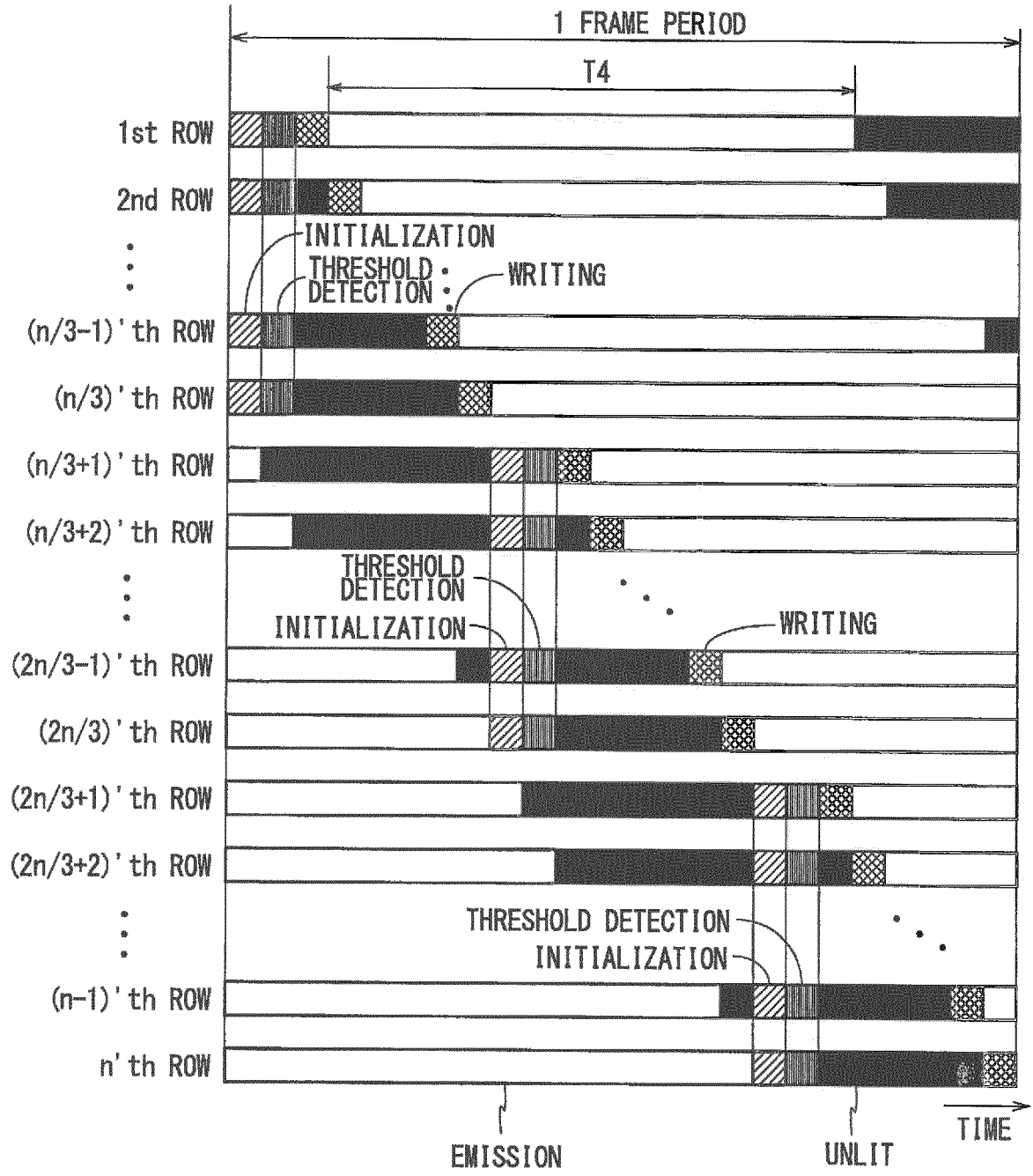

1 FRAME PERIOD
T4
1st ROW
2nd ROW
INITIALIZATION
THRESHOLD DETECTION
WRITING
(n/3-1)'th ROW
(n/3)'th ROW
(n/3+1)'th ROW
(n/3+2)'th ROW
THRESHOLD DETECTION
INITIALIZATION
WRITING
(2n/3-1)'th ROW
(2n/3)'th ROW
(2n/3+1)'th ROW
(2n/3+2)'th ROW
THRESHOLD DETECTION
INITIALIZATION
(n-1)'th ROW
n'th ROW
EMISSION
UNLIT
TIME

FIG. 15

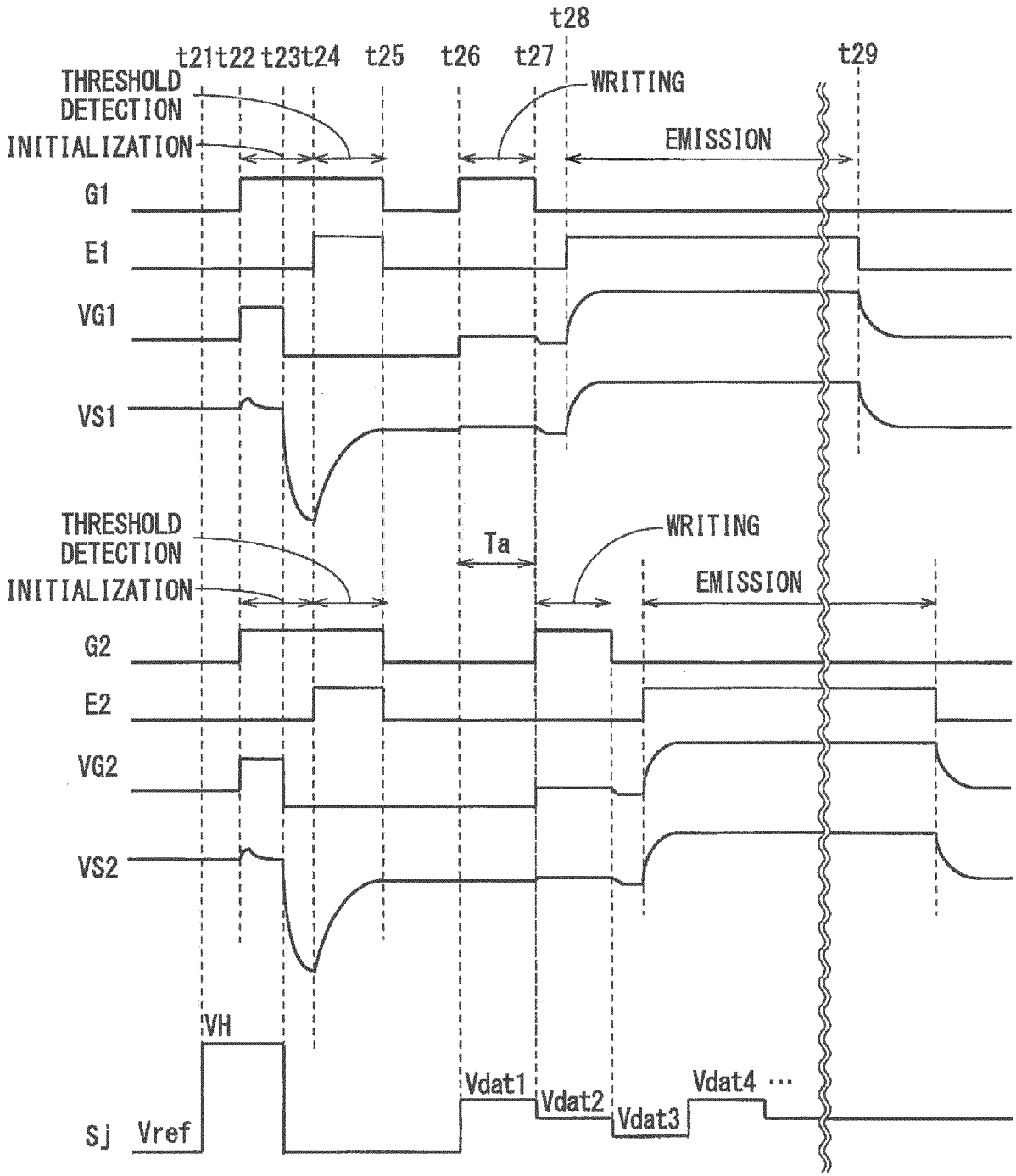

t21
t22
t23
t24
t25
t26
t27
t28
t29
THRESHOLD DETECTION
INITIALIZATION
WRITING
EMISSION
G1
E1
VG1
VS1
THRESHOLD DETECTION
INITIALIZATION
Ta
WRITING
EMISSION
G2
E2
VG2
VS2
VH
Sj
Vref
Vdat1
Vdat2
Vdat3
Vdat4 ···

FIG. 16

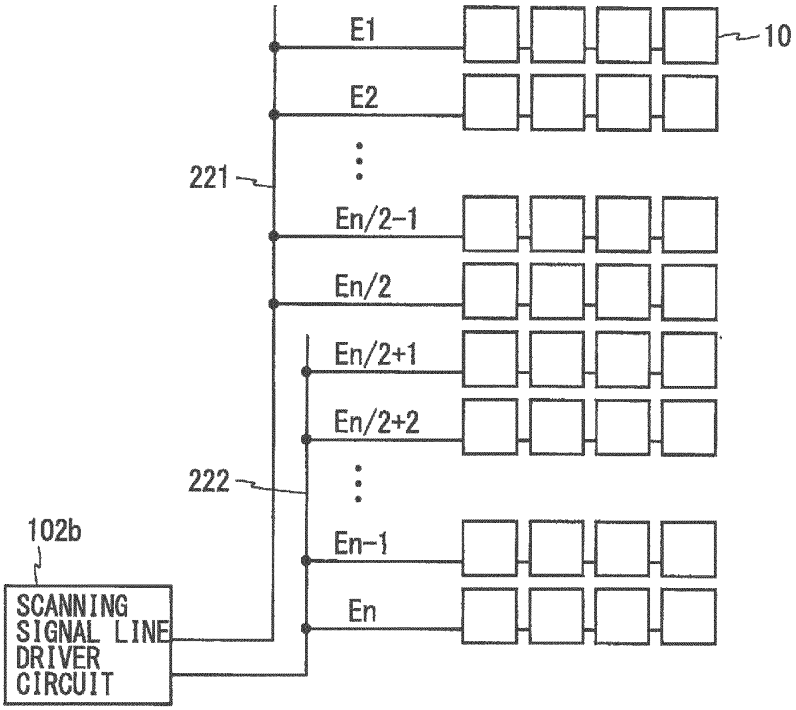

E1
E2
221
En/2-1
En/2
En/2+1
En/2+2
222
En-1
En
10
102b
SCANNING SIGNAL LINE DRIVER CIRCUIT

FIG. 17

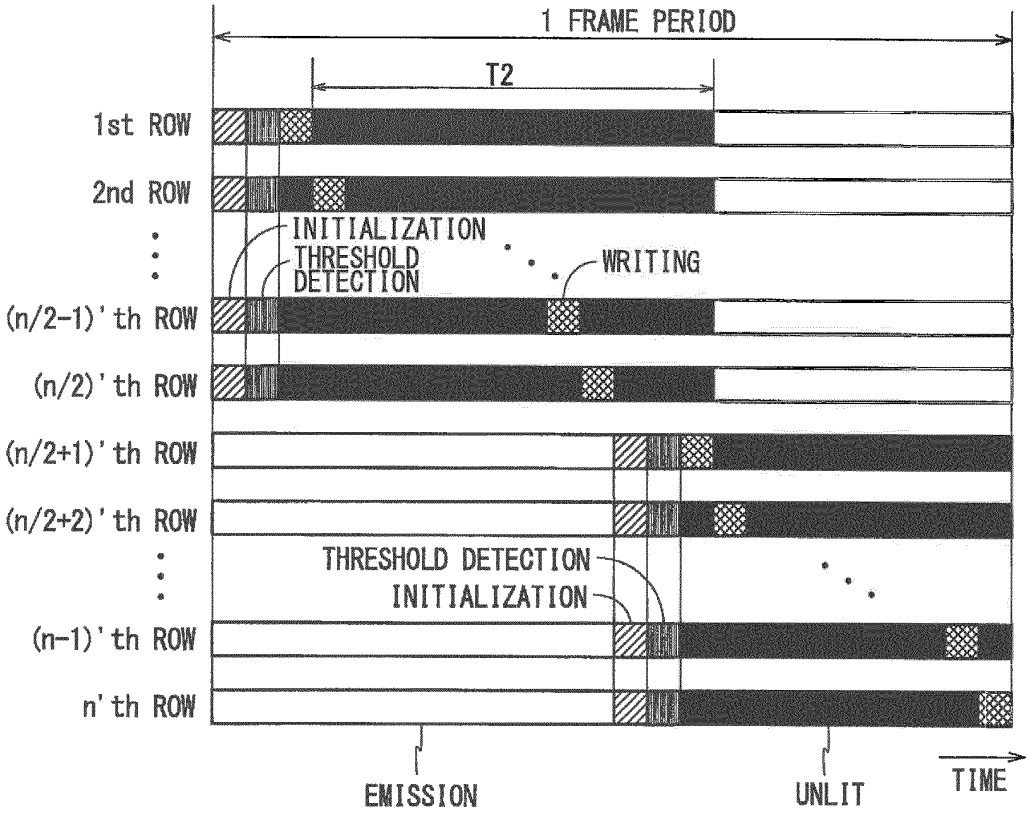

1 FRAME PERIOD
T2
1st ROW
2nd ROW
INITIALIZATION
THRESHOLD DETECTION
WRITING
(n/2-1)'th ROW
(n/2)'th ROW
(n/2+1)'th ROW
(n/2+2)'th ROW
THRESHOLD DETECTION
INITIALIZATION
(n-1)'th ROW
n'th ROW
EMISSION
UNLIT
TIME

FIG. 18

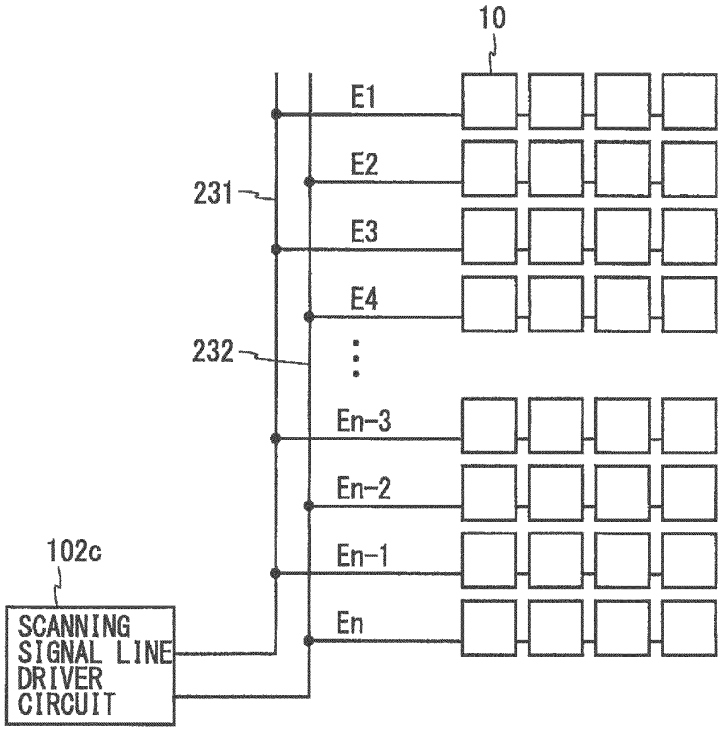

10
E1
E2
231
E3
E4
232
En-3
En-2
102c
En-1
SCANNING SIGNAL LINE DRIVER CIRCUIT
En

FIG. 19

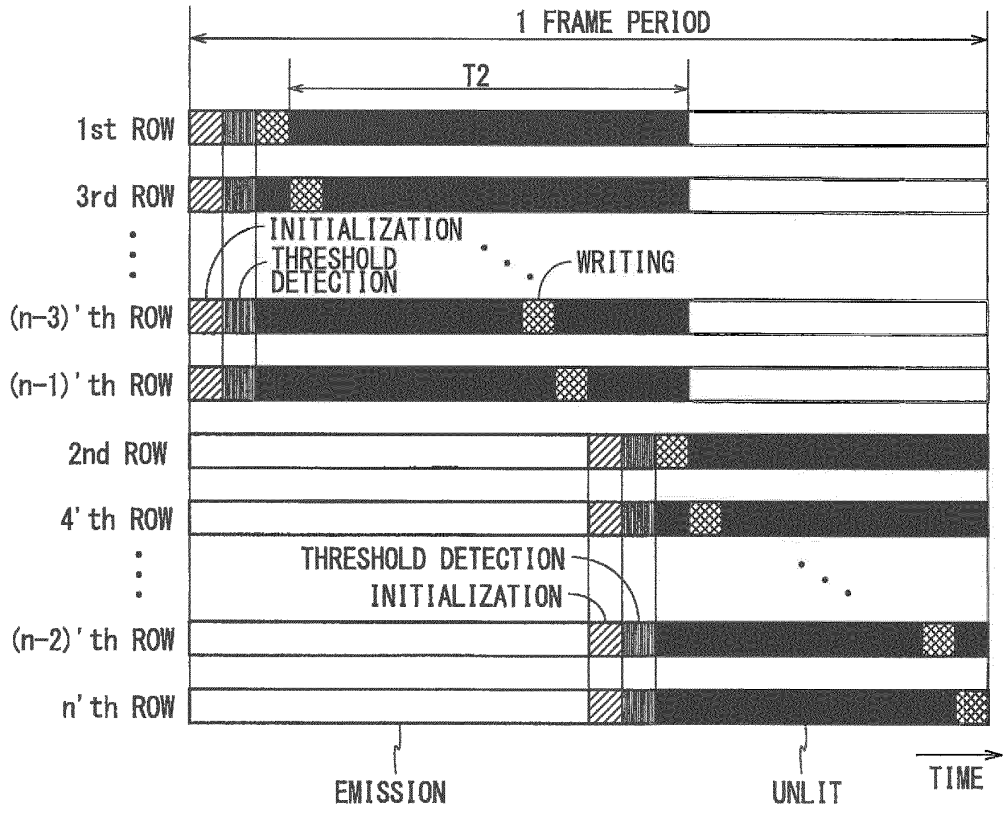

1 FRAME PERIOD
T2
1st ROW
3rd ROW
INITIALIZATION
THRESHOLD DETECTION
WRITING
(n-3)'th ROW
(n-1)'th ROW
2nd ROW
4'th ROW
THRESHOLD DETECTION
INITIALIZATION
(n-2)'th ROW
n'th ROW
EMISSION
UNLIT
TIME

FIG. 20

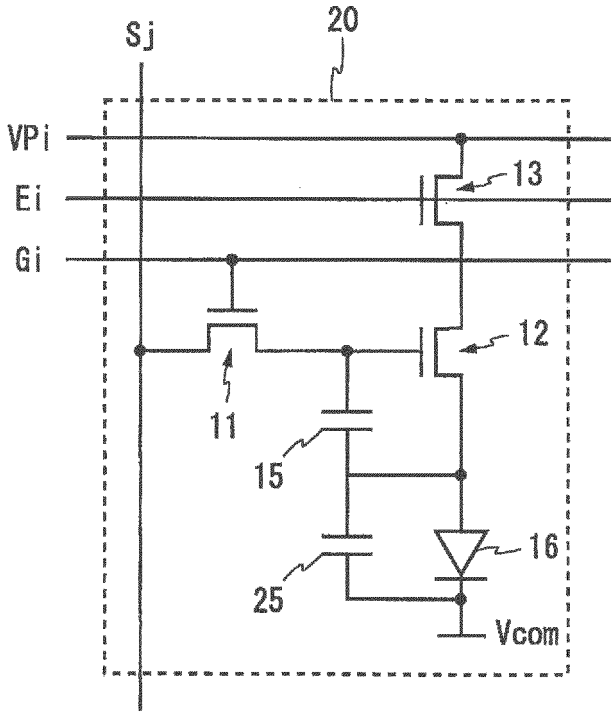


FIG. 21

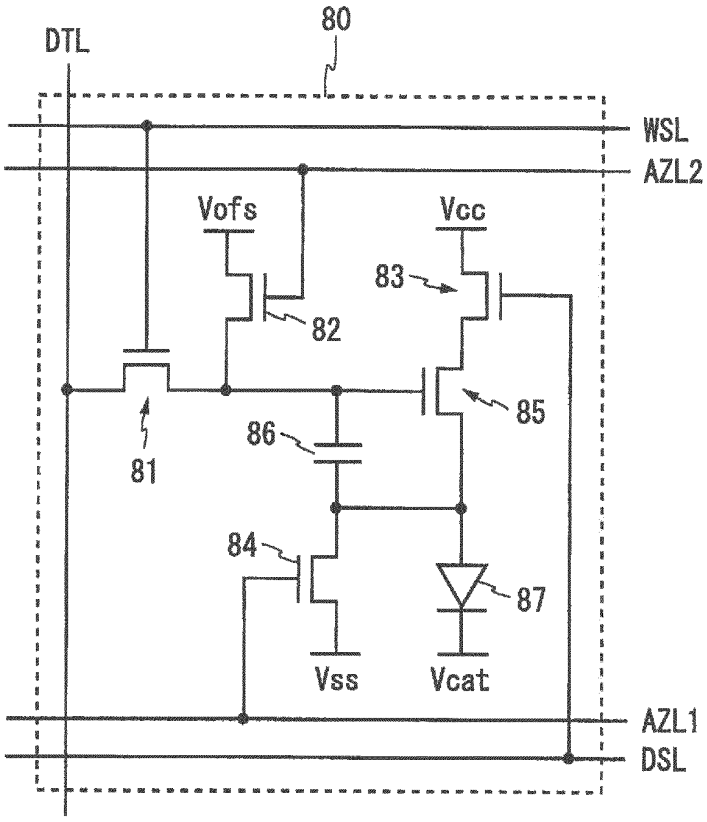
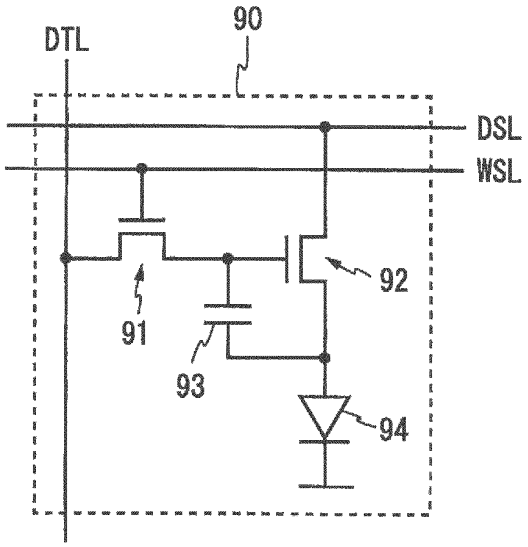

DTL
80
WSL
AZL2
Vofs
Vcc
83
82
85
86
81
84
87
Vss
Vcat
AZL1
DSL

FIG. 22


DTL
90
DSL
WSL
92
91
93
94

REFERENCES CITED IN THE DESCRIPTION

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- US 20100091207 A1 **[0011]**
- US 20090109146 A1 **[0012]**
- US 20090278771 A1 **[0013]**
- US 20070115225 A1 **[0014]**

专利名称(译)	显示装置及其驱动方法		
公开(公告)号	EP2595140B1	公开(公告)日	2020-06-10
申请号	EP2011806563	申请日	2011-06-01
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	KISHI NORITAKA NOGUCHI NOBORU		
发明人	KISHI, NORITAKA NOGUCHI, NOBORU		
IPC分类号	G09G3/3233 H01L27/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2300/0866 G09G2310/0205 G09G2310/0218 G09G2310/0256 G09G2320/0252 H01L27/3276 G09G3/3258 H01L27/3244 H01L27/3246 H01L27/326 H01L27/3262		
优先权	2010157625 2010-07-12 JP 2010202702 2010-09-10 JP		
其他公开文献	EP2595140A1 EP2595140A4		
外部链接	Espacenet		

摘要(译)

显示装置（100）包括：多个像素电路（10），耦合至多条扫描信号线Gi和多条控制线Ei的栅极驱动器电路（2），以及电源控制电路（4）。 经由公共电源线耦合到多条电源线VP i。 像素电路（10）分别包括有机EL元件，多个TFT和电容器，并且被控制为通过电源线VP i在帧的开始处集体接收初始化电位，此后立即共同进行阈值检测， 然后执行写入和发光操作。 因此，像素电路（10）的开口率可以保持较高，功率控制电路（4）通常仅具有一个输出缓冲器，因此其电路规模较小，仅通过电位驱动一次，从而功率 功耗低，并且阈值检测仅执行一次，因此可以确保在检测期间有足够的时间。

$$Vgs = \{C_{OLED} / (C_{OLED} + C_{st})\} \times (Vdat1 - Vref) + Vth \quad \cdots (1)$$