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(71) Applicant: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**
Atsugi-shi, Kanagawa-ken 243-0036 (JP)

(72) Inventors:
- **Inukai, Kazutaka**
  Kanagawa-ken 243-0036 (JP)
- **Osame, Mitsuaki**
  Kanagawa-ken 243-0036 (JP)
- **Iwabuchi, Tomoyuki**
  Kanagawa-ken 243-0036 (JP)

(74) Representative: **Grünecker, Kinkeldey,**
Stockmair & Schwanhäusser
Anwaltssozietät
Leopoldstrasse 4
80802 München (DE)

(54) **Method of driving EL display device and EL display device**

(57) An EL display device comprising a plurality of pixels (404), the pixels comprising EL elements (407), a plurality of source signal lines, a source signal line drive circuit (601), a first gate signal line drive circuit (605), and a second gate signal line drive circuit, wherein the source signal line drive circuit is configured to output any one bit of digital video signal among n bit of digital video signals to each of the plurality of source signal lines in each of (n + m) display periods in one frame period, with n and m being natural numbers, wherein the digital video signals are input from the plurality of source signal lines by inputting a first gate signal, light emitting or non-light emitting of the EL elements is selected by the digital video signals, the EL elements do not emit light when a second gate signal is input in the plurality of pixels, wherein the plurality of pixels are disposed in a matrix form, wherein the first gate signal line drive circuit is configured to input the first gate signal to each row of the plurality of pixels in turn, wherein the second gate signal line drive circuit is configured to input the second gate signal to each row of the plurality of pixels in turn, wherein the second gate signal line drive circuit is configured to input a second gate signal to a row of the plurality of pixels different from the p row to set the display period shorter than a period necessary to input the digital video signals to all the plurality of pixels while the first gate signal line drive circuit is configured to input the first gate signal to p row of the plurality of pixels, p being a natural number, in at least one display period of the (n + m) display periods, wherein n bit of digital video signals which the source signal line drive circuit inputs corresponds to i^{th} n bit of digital video signals, with i being a natural number, n or less in k with k being a natural number, more than 2 or more and (n + m)or less display periods of the display periods (n + m), and wherein k display periods does not continue, and the digital video signals which the source signal line drive circuit output correspond to j^{th} n bit of digital video signals, with j being different from i, and natural number, n or less, in a display period between the k display periods.

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(Cont. next page)

FIG. 1A

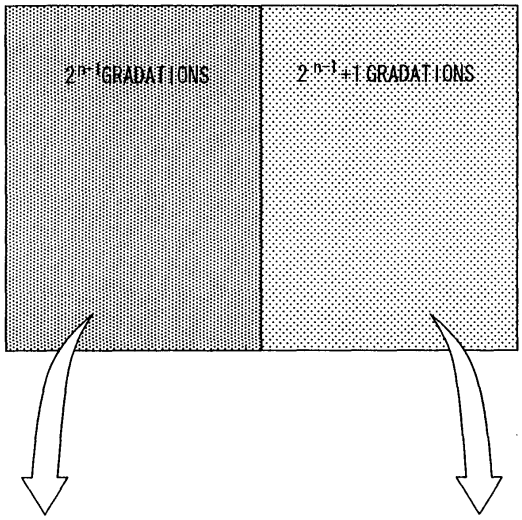
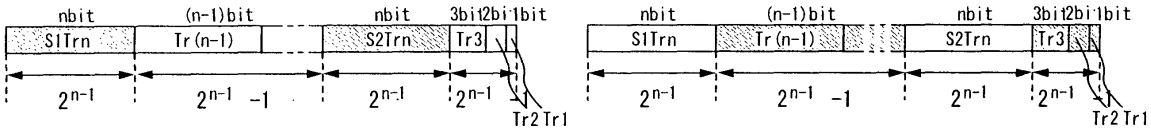

2^n-1 GRADATIONS
2^n-1+1 GRADATIONS

FIG. 1B


nbit
(n-1)bit
nbit
3bit
2bit
1bit
S1Trn
Tr(n-1)
S2Trn
Tr3
Tr2
Tr1
2^n-1
2^n-1 -1
2^n-1
2^n-1
2^n-1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 08 01 0199

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Y	JP 10 171401 A (FUJITSU LTD) 26 June 1998 (1998-06-26) * abstract; figure 3 *	1-11	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	6 August 2008	Harke, Michael

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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L : document cited for other reasons

& : member of the same patent family, corresponding document

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 08 01 0199

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	6 August 2008	Harke, Michael

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X : particularly relevant if taken alone
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& : member of the same patent family, corresponding document

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06-08-2008

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	驱动EL显示器件和EL显示器件的方法		
公开(公告)号	EP1970884A3	公开(公告)日	2008-09-24
申请号	EP2008010199	申请日	2001-09-04
[标]申请(专利权)人(译)	株式会社半导体能源研究所		
申请(专利权)人(译)	半导体能源研究所有限公司.		
当前申请(专利权)人(译)	半导体能源研究所有限公司.		
[标]发明人	INUKAI KAZUTAKA OSAME MITSUAKI IWABUCHI TOMOYUKI		
发明人	INUKAI, KAZUTAKA OSAME, MITSUAKI IWABUCHI, TOMOYUKI		
IPC分类号	G09G3/32 G09G3/30 G09F9/30 G09G3/20 H01L21/77 H01L21/84 H01L27/12 H01L27/32 H01L51/50 H05B33/14		
CPC分类号	G09G3/3266 G09G3/2022 G09G3/2033 G09G3/3275 G09G2300/0809 G09G2300/0842 G09G2310/0251 G09G2310/027 G09G2320/0247 G09G2320/0261 G09G2320/0266 H01L27/12 H01L27/1214		
优先权	2000267164 2000-09-04 JP		
其他公开文献	EP1970884A2		
外部链接	Espacenet		

摘要(译)

一种EL显示装置，包括多个像素（404），所述像素包括EL元件（407），多个源极信号线，源极信号线驱动电路（601），第一栅极信号线驱动电路（605），第二栅极信号线驱动电路，其中源极信号线驱动电路被配置为将n位数字视频信号中的任何一位数字视频信号输出到每个（n + m）的多个源极信号线中的每一个。 ）在一个帧周期中的显示周期，其中n和m是自然数，其中通过输入第一门信号从多个源信号线输入数字视频信号，选择EL元件的发光或不发光通过数字视频信号，当在多个像素中输入第二栅极信号时，EL元件不发光，其中多个像素以矩阵形式设置，其中第一栅极信号线驱动电路被配置为inp将第一栅极信号依次送到多个像素的每一行，其中第二栅极信号线驱动电路配置为输入第二栅极信号依次到多个像素的每一行，其中第二栅极信号线驱动电路被配置为将第二栅极信号输入到与p行不同的多个像素的行中，以将显示周期设置为短于将所述数字视频信号输入到所有所述多个像素所需的时段，同时所述第一栅极信号线驱动电路被配置为将所述第一栅极信号输入到所述多个像素中的p行，p为自然数，至少一个显示周期为（n + m）个显示周期，其中源信号线驱动电路输入的n位数字视频信号对应于第n位数字视频信号，其中i为自然数，n为k或者n为k是自然数，显示周期（n + m）的显示周期大于2或更多且（n + m）或更少，并且其中k个显示周期不继续，并且源信号线的数字视频信号驱动电路输出响应第j个n位数字视频信号，其中j与i不同，并且在k显示之间的显示周期内自然数n或更小周期。

FIG. 1A

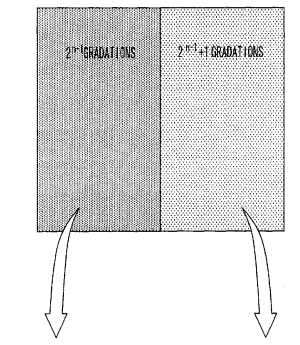

FIG. 1B