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(54) **Scan driving circuit and organic light emitting display using the same**

Zeilentreiberschaltung und organische lichtemittierende Anzeige damit

Circuit de commande de balayage et affichage électroluminescent organique l'utilisant

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Description

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a scan driving circuit and an organic light emitting display using the same.

2. Discussion of Related Art

[0002] In general, an active matrix type display device such as an organic light emitting display includes a pixel array arranged at intersections between data lines and scan lines in a matrix pattern.

[0003] The scan lines include horizontal lines (i.e., row lines) of a display region having a matrix of pixels, and sequentially provide a predetermined signal, namely, a scan signal from a scan driving circuit, to the pixel array.

[0004] FIG. 1 is a block diagram showing a conventional scan driving circuit. With reference to FIG. 1, the conventional scan driving circuit includes a plurality of stages ST1 to STn, which are dependently coupled with a start pulse SP input line. The plurality of stages ST1 to STn sequentially shift a clock signal C in response to a start pulse SP to generate output signals SO1 to SOn, respectively. In this case, each of second to n-th stages ST2 to STn receives and shifts an output signal of a previous stage as a start pulse.

[0005] Accordingly, the stages generate output signals SO1 to SOn in such a way that the start pulse is sequentially shifted, and provide the output signals to the pixel array.

[0006] FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1. FIG. 3 is a timing diagram of the stage shown in FIG. 2. Referring to FIG. 2 and FIG. 3, conventionally, each stage of a scan driving circuit uses a master-slave flip-flop. When a clock signal CLK is at a low level, such a flip-flop continues to receive an input and maintains a previous output.

[0007] In contrast to this, when the clock signal CLK is at a high level, the flip-flop maintains an input In received at an input terminal when the clock signal CLK is at the low level, and outputs the received input, but no longer receives the input In.

[0008] In the aforementioned circuit, an inverter included in the flip-flop has a problem in that a static current flows when an input thereof is at a low level. Furthermore, in the flip-flop, the number of inverters having received a high-level input is the same number as that of inverters having received a low-level input. Accordingly, the static current flows through a half of all the inverters in the flip-flop, thereby causing power consumption to be increased.

[0009] In addition, in the circuit of FIG. 2A, a voltage value due to a ratio of resistance (i.e., transistors M1' and M2') connected between a power supply VDD and a ground GND determines a high level of an output voltage OUT. Low level of the output voltage OUT is set to be greater than that of the ground GND by a threshold voltage of the transistor M2'.

[0010] By way of example, due to characteristic deviations of the transistors, since levels of an input voltage are different according to respective stages, in the case where the circuit of FIGs. 2 and 2A is used, the deviation occurs when the output voltage is at a high level, with the result that the circuit may be erroneously operated.

[0011] Moreover, the deviation in a low level of the output voltage causes a deviation in on-resistance of an input transistor of an inverter included in the circuit of FIG. 2 to occur, thereby weighting a deviation in a high level of the output voltage. In particular, since a panel of an organic light emitting display uses a transistor having a great characteristic deviation, such a problem is more serious.

[0012] Further, in the inverter, an electric current flows through an input transistor to charge an output terminal, whereas the electric current flows through a load transistor to discharge the output terminal. Upon a charge of the output terminal, a source-gate voltage of the load transistor is gradually reduced, and a discharge current is accordingly reduced rapidly. This causes the discharge efficiency to be deteriorated.

[0013] US2004/0227718 discloses a scan driving circuit comprising a plurality of stages, the plurality of stages being collectively adapted to receive four clock signals, wherein each of the plurality of stages has an input terminal and is respectively configured to receive three of the four clock signals, to receive and delay an input signal through the input terminal, and to output an output signal through an output terminal, wherein the output terminal of each of the plurality of stages except for a final stage is connected to the input terminal of a subsequent one of the stages, wherein each of the plurality of stages comprises:

> a switch coupled to the input terminal of the stage and to a second clock terminal, the switch being arranged to connect and disconnect the input terminal to and from a first node according to a second clock signal, the second clock signal being input through the second clock terminal.

SUMMARY OF THE INVENTION

[0014] Accordingly, a first aspect of the present invention provides a scan driving circuit as set out in claim 1. The scan driving circuit may be implemented with PMOS transistors or NMOS transistors, which switch an output voltage of the scan driving circuit from a positive source voltage to a negative source voltage. Preferred features are set out in claims 2 to 10. Acording to a second aspect of the invention there is provided an organic light emitting display as set out in claim 11.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] These and/or other aspects and features of the invention will become apparent and more readily appreciated from the following description of embodiments of the invention, taken in conjunction with the accompanying drawings of which:

[0016] FIG. 1 is a block diagram showing a conventional scan driving circuit;

[0017] FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1;

[0018] FIG. 2A is a circuit diagram of an inverter in the stage shown in FIG. 2;

[0019] FIG. 3 is a timing diagram of the stage shown in FIG. 2;

[0020] FIG. 4 is a block diagram showing an organic light emitting display according to an embodiment of the present invention;

[0021] FIG. 5 is a block diagram showing a construction of a scan driving circuit according to an embodiment of the present invention;

[0022] FIG. 6 is a circuit diagram showing a first embodiment of a stage of the scan driving circuit shown in FIG. 5;

[0023] FIG. 7 is a timing diagram showing a first embodiment of an input/output waveform of the stage shown in FIG. 6;

[0024] FIG. 8 is a circuit diagram of a stage of the scan driving circuit shown in FIG. 5;

[0025] FIG. 13 is a circuit diagram showing a sixth embodiment of a stage of the scan driving circuit shown in FIG. 5; and

[0026] FIG. 14 is a timing diagram of the stage shown in FIG. 13.

DETAILED DESCRIPTION

[0027] Hereinafter, embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being connected to a second element, the first element may be not only directly connected to the second element but also may be indirectly connected to the second element via a third element. Further, elements that are not essential to the complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0028] FIG. 4 is a block diagram showing an organic light emitting display according to an embodiment of the present invention. With reference to FIG. 4, the organic light emitting display includes a display region 30, a scan driving circuit 10, a data driving circuit 20, and a timing controller 50.

[0029] The display region 30 includes a plurality of pixels 40 formed at crossing areas of scan lines S1 to Sn, and data lines D1 to Dm. The scan driving circuit 10 drives the scan lines S1 to Sn. The data driving circuit 20 drives the data lines D1 to Dm. The timing controller 50 controls the scan driving circuit 10 and the data driving circuit 20.

[0030] The timing controller 50 generates a data drive control signal DCS and a scan drive control signal SCS according to externally supplied synchronous signals. The data drive control signal DCS generated by the timing controller 50 is provided to the data driving circuit 20, and the scan drive control signal SCS is provided to the scan driving circuit 10. Furthermore, the timing controller 50 provides externally supplied data Data to the data driving circuit 20.

[0031] The data driving circuit 20 receives the data drive control signal DCS from the timing controller 50. Upon the receipt of the data drive control signal DCS, the data driving circuit 20 generates data signals, and provides the generated data signals to the data lines D1 to Dm. In this embodiment, the data driving circuit 20 provides the generated data signals to the data lines D1 to Dm every one horizontal period.

[0032] The display region 30 receives a first power from a first power supply ELVDD and a second power from a second power supply ELVSS from an exterior source, and provides them to the pixels 40. Upon the receipt of the first power ELVDD and the second power ELVSS, the pixels 40 control an amount of current that flows into the second power supply ELVSS from the first power supply ELVDD through a light emitting element corresponding to the data signal, thus generating light corresponding to the data signal.

[0033] The scan driving circuit 10 generates a scan signal in response to a scan drive control signal SCS from the timing controller 50, and sequentially provides the generated scan signal to the scan lines S1 to Sn. That is, the scan driving circuit 10 sequentially generates the scan signal to drive the plurality of pixels, and provides the scan signal to the display region 30.

[0034] Hereinafter, a construction and an operation of the scan driving circuit of an organic light emitting display according to an embodiment of the present invention will be explained.

[0035] FIG. 5 is a block diagram showing a configuration of a scan driving circuit 30 according to an embodiment of the present invention. Referring to FIG. 5, the scan driving circuit includes n stages that are dependently coupled with a start pulse input line so as to drive an m x n pixel array.

[0036] First output lines of the first n stages are coupled with first n scan lines (i.e., row lines) included in the pixel array. A start pulse SP is supplied to a first stage. Output signals of first to n-1 th stages are provided to next stages as a start pulse, respectively. Each stage receives and operates according to a first clock signal CLK1, a second clock signal CLK2, and a third clock signal CLK3; the second clock signal CLK2, the third clock signal CLK3, and a fourth clock signal CLK4; the third clock signal CLK3, the fourth clock signal CLK4, and the first clock signal CLK1; or the fourth clock signal CLK4, the first clock signal CLK1, and the second clock signal CLK2. That is, each stage operates in response to three of the

four supplied clock signals: the first clock signal CLK1, the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4. Each stage includes a first clock terminal ck1, a second clock terminal ck2, and a third clock terminal ck3. Here, as shown, the first clock signal CLK1, the second clock signal CLK2, and the third clock signal CLK3 are supplied to the first clock terminal ck1, the second clock terminal ck2, and the third clock terminal ck3 of a (4k-3)-th stage, respectively. The second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4 are supplied to the first clock terminal ck1, the second clock terminal ck2, and the third clock terminal ck3 of a (4k-2)-th stage, respectively. The first clock signal CLK1, the third clock signal CLK3, and the fourth clock signal CLK4 are supplied to the third clock terminal ck3, the first clock terminal ck1, and the second clock terminal ck2 ofa(4k-1)-th stage, respectively. The first clock signal CLK1, the second clock signal CLK2, and the fourth clock signal CLK4 are supplied to the second clock terminal ck2, the third clock terminal ck3, and the first clock terminal ck1 of a (4k)-th stage, respectively. Here, k is a natural number.

[0037] Further, when the first stage outputs a signal in response to the first clock signal CLK1, the second clock signal CLK2, and the third clock signal CLK3, the second stage receives and operates according to the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4. When the second stage outputs a signal in response to the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4, the third stage receives and operates according to the third clock signal CLK3, the fourth clock signal CLK4, and the first clock signal CLK1. When the third stage outputs a signal in response to the third clock signal CLK3, the fourth clock signal CLK4, and the first clock signal CLK1, the fourth stage receives and operates according to the fourth clock signal CLK4, the first clock signal CLK1, and the second clock signal CLK2. That is, the first, second, third, and fourth stages sequentially output the signal to sequentially drive a display region of an organic light emitting display by lines.

[0038] An external control circuit (not shown) provides the input signals of the driving circuit, that is, a start pulse SP, the first to fourth clock signals CLK 1 to CLK4, and a supply voltage VDD.

[0039] FIG. 6 is a circuit diagram showing a first embodiment of a stage of the scan driving circuit shown in FIG. 5. In accordance with a first embodiment of the invention FIG. 7 is a timing diagram showing an input/output waveform of the stage shown in FIG. 6.

[0040] As shown in FIG. 6, in the first embodiment of the present invention, transistors included in each stage are all PMOS transistors. Each stage sequentially sends a low level output through the scan driving circuit. Namely, the scan driving circuit according to an embodiment of the present invention outputs a high level signal to a display region of an active matrix type display device such as an organic light emitting display for most of the time, and sequentially outputs a low level pulse through a plurality of stages as shown in FIG. 6 and FIG. 7.

[0041] Referring to FIG. 6, the stage includes a first PMOS transistor M1, a second PMOS transistor M2, a third PMOS transistor M3, a fourth PMOS transistor M4, a fifth PMOS transistor M5, and a first capacitor C 1. The first PMOS transistor M1 includes a gate coupled with a second clock terminal ck2, receives an output voltage Si of a previous stage or a first start pulse SP, and selectively transfers the output voltage Si of a previous stage or the first start pulse SP to a first node N1. The second PMOS transistor M2 includes a gate connected to the first node N1, and is coupled between the third clock terminal ck3 and a second node N2. The third PMOS transistor M3 includes a gate connected to the first clock terminal ck1, and is connected between a ground and a third node N3. The fourth PMOS transistor M4 includes a gate connected to the first node N1, and is connected between the first clock terminal ck1 and the third node N3. The fifth PMOS transistor M5 includes a gate connected to the third node N3, and is coupled between a power supply line VDD and the second node N2. The first capacitor C1 is connected between the first node N1 and the second node N2, and maintains a predetermined voltage.

[0042] Although it is shown that M3 is coupled to a ground, M3 may alternatively be coupled to a negative power supply VSS.

[0043] Hereinafter, through a circuit arrangement of (4k-3)-th stage among stages shown in FIG. 6, operation of the stages will be explained with specific reference to the first stage, the first stage having the first clock terminal ck1 connected to the first clock signal CLK1, the second clock terminal ck2 connected to the second clock signal CLK2, and the third clock terminal ck3 connected to the third clock signal CLK3.

[0044] With reference to FIGs. 6 and 7, each stage of the scan driving circuit may divide one period into a precharge period, an input period, an evaluation period, and a quiescent period according to the first clock signal CLK1, the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4. During the precharge period, a low level signal is inputted to the first clock terminal ck1 of the stage, and a high level signal is inputted to the second clock terminal ck2 and the third clock terminal ck3 to precharge a capacitor C 1 of the stage. During the input period, a low level signal is inputted to the second clock terminal ck2, and a high level signal is inputted to the first clock terminal ck1 and the third clock terminal ck3. Further, a start pulse SP or a scan signal Si of a previous stage is inputted through the input terminal to the first node N 1 and is stored in the capacitor C1. During the evaluation period, a low level signal is inputted to the third clock terminal ck3, and a high level signal is inputted to the first clock terminal ck1 and the second clock terminal ck2, so that the stage outputs a low level signal within a predetermined period. Further, a start pulse SP or a scan signal Si of a previous stage is inputted through the input terminal. During the

evaluation period, a low level signal is inputted to the third clock terminal ck3, and a high level signal is inputted through the first clock terminal ck1 and the second clock terminal ck2, so that the stage shifts and outputs a scan signal of a low level pulse by a predetermined time. In addition, the quiescent period is a time period when the fourth clock signal CLK4 which was not inputted to the stage has a low level.

[0045] During the precharge period, when the first clock signal CLK1 becomes a low level, the third PMOS transistor M3 is turned-on to make a voltage of the third node N3 a ground voltage. Accordingly, the fifth PMOS transistor M5 is turned-on to output a voltage of a power supply voltage VDD through an output terminal out, with the result that a high level voltage is outputted to the output terminal out. That is, a scan signal is outputted with a high level. Further, during the input period, the second clock signal CLK2 becomes a low level, the start pulse SP or the scan signal Si of a previous stage is transferred to the first node N1 through the first PMOS transistor M1, and the start pulse SP or the scan signal Si of a previous stage is stored in the capacitor C 1. At this time, because the start pulse SP or the scan signal Si of a previous stage is low, the second PMOS transistor M2 and the fourth PMOS transistor M4 are turned-on. Further, the first clock signal CLK1 becomes a high level to turn-off the third PMOS transistor M3. When the third PMOS transistor M3 is turned-off and the fourth PMOS transistor M4 is turned-on, a first clock signal CLK1 of a high level is transferred to the third node N3 to turn-off the fifth PMOS transistor M5. At this time, the second PMOS transistor M2 is turned-off, so that an output terminal outputs a high level signal according to a third clock signal CLK3 of a high level. Moreover, during the evaluation period, the third clock signal CLK3 becomes a low level to float the first PMOS transistor M1. This causes the capacitor C1 to maintain a low level signal, thereby turning-on the second PMOS transistor M2 and the fourth PMOS transistor M4. In contrast to this, the third PMOS transistor M3 and the fifth PMOS transistor M5 are turned-off. Consequently, a low level signal is outputted to the output terminal out according to the third clock signal CLK3 of a low level.

[0046] That is, the output terminal out outputs a high level voltage by a power supply line VDD during the precharge period, and maintains a high level voltage by the capacitor C1 during the input period. Further, during the evaluation period, a voltage corresponding to the third clock signal CLK3 of a low level is outputted. When the third clock signal CLK3 becomes a low level, a voltage of the output terminal out drops. In contrast to this, when the third clock signal CLK3 becomes a high level, the voltage of the output terminal out again becomes a high level. Accordingly, the output terminal out outputs a scan signal. Furthermore, during the quiescent period, the first clock signal CLK1, the second clock signal CLK2, and the third clock signal CLK3 are transferred with a high level, but the fourth clock signal CLK4 of a low level is not transferred to the stage, so that the stage does not operate in response to clock signals.

[0047] As a result, when a low level signal is not inputted to an input terminal in of each stage, the second PMOS transistor M2 is turned-off, so that the output terminal out maintains a high level signal. Thus, only when each stage receives the start pulse SP or a low level signal of a previous stage, it outputs a low level signal that results in a sequential output of the scan signal.

[0048] FIG. 8 is a circuit diagram showing a stage for the scan driving circuit shown in FIG. 5. Referring to FIG. 8, the stage includes a first PMOS transistor M1, a second PMOS transistor M2, a third PMOS transistor M3, a fourth PMOS transistor M4, a fifth PMOS transistor M5, and a capacitor C1.

[0049] The first PMOS transistor M1 transfers an input signal to the first node N1 in response to the second clock signal CLK2, and the second PMOS transistor M2 transfers the third clock signal CLK3 to the second node N2 corresponding to a voltage of the first node N1. The third PMOS transistor M3 transfers a ground voltage to a gate of the fifth transistor PMOS M5 in response to the first clock signal CLK1. A gate of the fourth PMOS transistor M4 is connected to the output terminal out, and the fourth transistor M4 transfers the first clock signal CLK1 to a gate of the fifth PMOS transistor M5 corresponding to a voltage of the output terminal out. Further, the fifth PMOS transistor M5 transfers a voltage of a power supply line VDD to the output terminal corresponding to a voltage of a gate thereof. Moreover, the capacitor C1 is connected between the first node N1 and the second node N2, and maintains a predetermined voltage.

[0050] The stage having the construction as described above receives and operates according to the first to third clock signals CLK1 to CLK3 shown in FIG. 7. During the precharge period, the fifth PMOS transistor M5 is turned-on in response to the first clock signal CLK1 to output a high level signal to the output terminal out by a voltage of the power supply line VDD. During the input period, the start pulse SP or a scan signal Si of a previous stage is stored in the capacitor C1 in response to the second clock signal CLK2. Next, the voltage stored in the capacitor C1 causes a voltage of the third clock signal CLK3 to be outputted, so that the output terminal out maintains a high level signal. At this time, when a voltage of the output terminal has a low level, the fourth PMOS transistor M4 transfers a high level signal to a gate of the fifth PMOS transistor M5, thereby preventing a voltage of the power supply line VDD from being transferred to the output terminal.

[0051] FIG. 13 is a circuit diagram showing a a stage for the scan driving circuit shown in FIG. 5 in accordance with a sixth embodiment of the invention. FIG. 14 is a timing diagram of the stage shown in FIG. 13. With reference to FIG. 13 and FIG. 14, the stage is constructed by NMOS transistors M6, M7, M8, M9, and M10. A stage of FIG. 13 has substantially the same construction as that of FIG. 6, and respective transistors perform sub-

stantially the same operation as that of FIG. 6. In other words, the transistors M6, M7, M8, M9, and M10 perform substantially the same functions as transistors M1, M2, M3, M4, and M5, respectively.

[0052] Since the scan driving circuit and an organic light emitting display using the embodiments according to the present invention switch an output voltage from a positive source voltage to a negative source voltage, an operation speed is increased. Furthermore, even if a clock signal transferred to the scan driving circuit is erroneously operated, a change of a waveform of a scan signal is not great.

[0053] Although certain embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in these embodiments without departing from the scope of the invention which is defined in the appended claims.

Claims

1. A scan driving circuit comprising a plurality of stages, the plurality of stages being collectively adapted to receive four clock signals, wherein each of the plurality of stages has an input terminal (in) and is respectively configured to receive three of the four clock signals (ck), to receive and delay an input signal through the input terminal (in), and to output an output signal through an output terminal (out), wherein the output terminal (out) of each of the plurality of stages except for a final stage is connected to the input terminal (in) of a subsequent one of the stages, wherein each of the plurality of stages comprises:

a switch (M1) coupled to the input terminal (in) of the stage and to a second clock terminal (ck2), the switch *being arranged to connect and disconnect the input terminal (in) to and from a first node (N1) according to a second clock signal, the second clock signal being input through the second clock terminal (ck2);
each of the plurality of stages being **characterised by**:

a switch section (M3-M5) coupled between the first node (N1) and the output terminal (out), the first clock signal being input through a first clock terminal (ck1); and
a storage section (M2) having a first terminal connected to the first node (N1) and a second terminal connected to a second node (N2), the second node (N2) being connected to the output terminal (out), for maintaining a voltage of the output terminal (out) for a predetermined time using a capacitor (C1) connected between the first node (N1) and the output terminal (out), and for transferring a voltage of a third clock signal to the output terminal (out), through a first transistor of said storage section (M2), according to the input signal sampled by the second clock signal, said sampled input signal being obtained from the first node (N1), the third clock signal being input through a third clock terminal (ck3);

wherein each switch section comprises:

a first transistor (M3) for transferring a second power supply voltage (ground) to a third node (N3), the gate of said first transistor being connected to the first clock terminal;
a second transistor (M4) having a gate terminal connected to the first node (N1) or to the output terminal (out) for transferring the voltage of the first clock signal to the third node (N3), wherein the third node (N3) is between the first transistor (M3) and second transistor (M4);
a third transistor (M5) including a gate connected to the third node (N3), the third transistor (M5) for transferring a first power supply voltage (V_{DD}) to the output terminal (out) according to a voltage of the third node (N3);
wherein the switch (M1), the first transistor (M2) of the storage section and the first, second and third transistors (M3, M4, M5) of the switch section are all PMOS transistors or all NMOS transistors.

2. A scan driving circuit as claimed in claim 1, wherein:

the first transistor (M3) includes a gate connected to the first clock terminal (ck1), a source connected to the second power supply voltage, and a drain connected to the third node (N3);
the second transistor (M4) includes a source connected to the first clock terminal (ck1), and a drain connected to the third node (N3);
the third transistor (M5) includes a source connected to the first power supply voltage (V_{DD}), and a drain connected to the output terminal (out).

3. A scan driving circuit as claimed in claim 1 or 2, wherein the second power supply voltage is a ground voltage.

4. A scan driving circuit as claimed in claim 1 or 2, wherein each storage section comprises:

a fourth transistor (M2) connected to the switch, the fourth transistor (M2) being for transferring the third clock (CLK3) to a second node (N2) according to a voltage of a first node (N1) that

received the input signal; and
wherein the capacitor (C1) is for maintaining a voltage between the first node (N1) and the second node (N2).

5. A scan driving circuit as claimed in any preceding claim, wherein the plurality of stages are adapted to operate during a precharge period, an input period, an evaluation period, and a quiescent period, wherein each of the plurality of stages is adapted to initialize the storage section during the precharge period, to receive and store a predetermined signal during the input period, to output a scan signal corresponding to the predetermined signal during the evaluation period, and not to operate in response to the first clock signal, the second clock signal, and the third clock during the quiescent period.

6. A scan driving circuit_as claimed in any of claims 1 to 5, wherein the plurality of stages are adapted to operate during a precharge period, an input period, and an evaluation period, wherein each of the plurality of stages is adapted to initialize the storage section and to output a high level voltage during the precharge period, to receive the input signal and to maintain the high level voltage during the input period, and to output a low level voltage during the evaluation period.

7. A scan driving circuit as claimed in claim 5 or 6, wherein each of the plurality of stages is adapted to operate in the input period when the previous one of the stages outputs a low level signal.

8. The scan driving circuit as claimed in any preceding claim, wherein the first clock (CLK1), the second clock (CLK2), and the third clock (CLK3) have the same period, but are shifted in phase from each other.

9. A scan driving circuit as claimed in any preceding claim, wherein the first power supply voltage (V_{DD}) is a voltage of a drive power source.

10. A scan driving circuit as claimed in any preceding claim wherein the switch is a first transistor (M1).

11. An organic light emitting display comprising:

a display region (30) having a plurality of pixels (40) for displaying an image;
a scan driving circuit (10) according to any preceding claim for transferring a scan signal to the display region; and
a data driving circuit (20) for transferring a data signal to the display region (30).

Patentansprüche

1. Zeilentreiberschaltung, umfassend eine Vielzahl von Stufen, wobei die Vielzahl von Stufen gemeinsam dafür eingerichtet ist, vier Taktsignale zu empfangen, wobei jede der Vielzahl von Stufen einen Eingangsanschluss (in) hat und jeweils dafür konfiguriert ist, drei der vier Taktsignale (ck) zu empfangen, über den Eingangsanschluss (in) ein Eingangssignal zu empfangen und zu verzögern und über einen Ausgangsanschluss (out) ein Ausgangssignal auszugeben, wobei der Ausgangsanschluss (out) jeder der Vielzahl von Stufen außer einer letzten Stufe mit dem Eingangsanschluss (in) einer nachfolgenden der Stufen verbunden ist, wobei jede der Vielzahl von Stufen umfasst:

einen Schalter (M1), der mit dem Eingangsanschluss (in) der Stufe und mit einem zweiten Taktanschluss (ck2) gekoppelt ist, wobei der Schalter dafür eingerichtet ist, den Eingangsanschluss (in) gemäß einem zweiten Taktsignal mit einem ersten Knoten (N1) zu koppeln und davon zu trennen, wobei das zweite Taktsignal über den zweiten Taktanschluss (ck2) eingegeben wird;
wobei jede der Vielzahl von Stufen **gekennzeichnet ist durch**:

einen Schalterabschnitt (M3-M5), der zwischen den ersten Knoten (N1) und den Ausgangsanschluss (out) gekoppelt ist, wobei das erste Taktsignal über einen ersten Taktanschluss (ck1) eingegeben wird; und
einen Speicherabschnitt (M2), der einen mit dem ersten Knoten (N1) verbundenen ersten Anschluss und einen mit einem zweiten Knoten (N2) verbundenen zweiten Anschluss aufweist, wobei der zweite Knoten (N2) mit dem Ausgangsanschluss (out) verbunden ist, um unter Verwendung eines Kondensators (C1), der zwischen den ersten Knoten (N1) und den Ausgangsanschluss (out) geschaltet ist, eine Spannung des Ausgangsanschlusses (out) für eine vorbestimmte Zeit beizubehalten und um eine Spannung eines dritten Taktsignals gemäß dem **durch** das zweite Taktsignal abgetasteten Eingangssignal über einen ersten Transistor des Speicherabschnitts (M2) zum Ausgangsanschluss (out) zu übertragen, wobei das abgetastete Eingangssignal vom ersten Knoten (N1) erlangt wird, wobei das dritte Taktsignal über einen dritten Taktanschluss (ck3) eingegeben wird;

wobei jeder Schalterabschnitt umfasst:

einen ersten Transistor (M3) zum Übertragen einer zweiten Versorgungsspannung (ground) zu einem dritten Knoten (N3), wobei das Gate des ersten Transistors mit dem ersten Taktanschluss verbunden ist;
einen zweiten Transistor (M4) mit einem Gateanschluss, der mit dem ersten Knoten (N1) oder mit dem Ausgangsanschluss (out) verbunden ist, zum Übertragen der Spannung des ersten Taktsignals zum dritten Knoten (N3), wobei der dritte Knoten (N3) zwischen dem ersten Transistor (M3) und dem zweiten Transistor (M4) ist; und
einen dritten Transistor (M5) mit einem Gate, das mit dem dritten Knoten (N3) verbunden ist, wobei der dritte Transistor (M5) zum Übertragen einer ersten Versorgungsspannung (V_{DD}) zum Ausgangsanschluss (out) gemäß einer Spannung des dritten Knotens (N3) dient;
wobei der Schalter (M1), der erste Transistor (M2) des Speicherabschnitts und der erste, zweite und dritte Transistor (M3, M4, M5) des Schalterabschnitts allesamt PMOS-Transistoren oder allesamt NMOS-Transistoren sind.

2. Zeilentreiberschaltung nach Anspruch 1, wobei:

der erste Transistor (M3) aufweist: ein Gate, das mit dem ersten Taktanschluss (ck1) verbunden ist, eine Source, die mit der zweiten Versorgungsspannung verbunden ist, und ein Drain, das mit dem dritten Knoten (N3) verbunden ist;
der zweite Transistor (M4) aufweist: eine Source, die mit dem ersten Taktanschluss (ck1) verbunden ist, und ein Drain, das mit dem dritten Knoten (N3) verbunden ist;
der dritte Transistor (M5) aufweist: eine Source, die mit der ersten Versorgungsspannung (V_{DD}) verbunden ist, und ein Drain, das mit dem Ausgangsanschluss (out) verbunden ist.

3. Zeilentreiberschaltung nach Anspruch 1 oder 2, wobei die zweite Versorgungsspannung eine Massespannung ist.

4. Zeilentreiberschaltung nach Anspruch 1 oder 2, wobei jeder Speicherabschnitt umfasst:

einen vierten Transistor (M2), der mit dem Schalter verbunden ist, wobei der vierte Transistor (M2) dazu dient, den dritten Takt (CLK3) gemäß einer Spannung eines ersten Knotens (N1), der das Eingangssignal empfangen hat, zu einem zweiten Knoten (N2) zu übertragen; und
wobei der Kondensator (C1) dazu dient, eine Spannung zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) beizubehalten.

5. Zeilentreiberschaltung nach einem der vorhergehenden Ansprüche, wobei die Vielzahl von Stufen dafür eingerichtet ist, während eines Vorladezeitabschnitts, eines Eingabezeitabschnitts, eines Bewertungszeitabschnitts und eines Ruhezeitabschnitts zu arbeiten, wobei jede der Vielzahl von Stufen dafür eingerichtet ist, während des Vorladezeitabschnitts den Speicherabschnitt zu initialisieren, während des Eingabezeitabschnitts ein vorbestimmtes Signal zu empfangen und zu speichern, während des Bewertungszeitabschnitts ein Zeilensignal, das dem vorbestimmten Signal entspricht, an den Ausgangsanschluss auszugeben, und während des Ruhezeitabschnitts als Antwort auf das erste Taktsignal, das zweite Taktsignal und das dritte Taktsignal nicht zu arbeiten.

6. Zeilentreiberschaltung nach einem der Ansprüche 1 bis 5, wobei die Vielzahl von Stufen dafür eingerichtet ist, während eines Vorladezeitabschnitts, eines Eingabezeitabschnitts und eines Bewertungszeitabschnitts zu arbeiten, wobei jede der Vielzahl von Stufen dafür eingerichtet ist, während des Vorladezeitabschnitts den Speicherabschnitt zu initialisieren und eine Hochpegelspannung auszugeben, während des Eingabezeitabschnitts das Eingangssignal zu empfangen und die Hochpegelspannung beizubehalten und während des Bewertungszeitabschnitts eine Tiefpegelspannung auszugeben.

7. Zeilentreiberschaltung nach Anspruch 5 oder 6, wobei jede der Vielzahl von Stufen dafür eingerichtet ist, im Eingabezeitabschnitt zu arbeiten, wenn die vorhergehende der Stufen ein Tiefpegelsignal ausgibt.

8. Zeilentreiberschaltung nach einem der vorhergehenden Ansprüche, wobei der erste Takt (CLK1), der zweite Takt (CLK2) und der dritte Takt (CLK3) die gleiche Periode haben, aber gegeneinander phasenverschoben sind.

9. Zeilentreiberschaltung nach einem der vorhergehenden Ansprüche, wobei die erste Versorgungsspannung (V_{DD}) eine Spannung einer Treiberstromversorgung ist.

10. Zeilentreiberschaltung nach einem der vorhergehenden Ansprüche, wobei der Schalter ein erster Transistor (M1) ist.

11. Organische Lichtemitteranzeige, umfassend:

einen Anzeigebereich (30) mit einer Vielzahl von Bildpunkten (40) zum Anzeigen eines Bildes;
eine Zeilentreiberschaltung (10) nach einem der vorhergehenden Ansprüche zum Übertragen eines Zeilensignals zum Anzeigebereich; und

eine Datentreiberschaltung (20) zum Übertragen eines Datensignals zum Anzeigebereich (30).

Revendications

1. Circuit de commande de balayage comprenant une pluralité d'étages, la pluralité d'étages étant conçue collectivement pour recevoir quatre signaux d'horloge, dans lequel chacun de la pluralité d'étages comporte une borne d'entrée (in) et est respectivement configuré pour recevoir trois des quatre signaux d'horloge (ck), pour recevoir et retarder un signal d'entrée par l'intermédiaire de la borne d'entrée (in), et pour délivrer un signal de sortie par l'intermédiaire d'une borne de sortie (out), dans lequel la borne de sortie (out) de chacun de la pluralité d'étages, à l'exception d'un étage final, est connectée à la borne d'entrée (in) d'un étage suivant parmi les étages, dans lequel chacun de la pluralité d'étages comprend :

un commutateur (M1) couplé à la borne d'entrée (in) de l'étage et à une deuxième borne d'horloge (ck2), le commutateur étant agencé pour connecter et déconnecter la borne d'entrée (in) à et d'un premier noeud (N1) conformément à un deuxième signal d'horloge, le deuxième signal d'horloge étant appliqué par l'intermédiaire de la deuxième borne d'horloge (ck2) ;
chacun de la pluralité d'étages étant **caractérisé par** :

une section de commutation (M3 à M5) couplée entre le premier noeud (N1) et la borne de sortie (out), le premier signal d'horloge étant appliqué par l'intermédiaire d'une première borne d'horloge (ck1) ; et
une section de mémorisation (M2) ayant une première borne connectée au premier noeud (N1) et une deuxième borne connectée à un deuxième noeud (N2), le deuxième noeud (N2) étant connecté à la borne de sortie (out), pour maintenir une tension de la borne de sortie (out) pendant un temps prédéterminé en utilisant un condensateur (C1) connecté entre le premier noeud (N1) et la borne de sortie (out), et pour transférer une tension d'un troisième signal d'horloge à la borne de sortie (out), par l'intermédiaire d'un premier transistor de ladite section de mémorisation (M2), conformément au signal d'entrée échantillonné par le deuxième signal d'horloge, ledit signal d'entrée échantillonné étant obtenu à partir du premier noeud (N1), le troisième signal d'horloge étant appliqué par l'intermédiaire d'une troisième borne d'horloge (ck3) ;

dans lequel chaque section de commutation comprend :

un premier transistor (M3) pour transférer une deuxième tension d'alimentation (masse) à un troisième noeud (N3), la grille dudit premier transistor étant connectée à la première borne d'horloge ;
un deuxième transistor (M4) ayant une borne de grille connectée au premier noeud (N1) ou à la borne de sortie (out) pour transférer la tension du premier signal d'horloge au troisième noeud (N3), dans lequel le troisième noeud (N3) est entre le premier transistor (M3) et le deuxième transistor (M4) ;
un troisième transistor (M5) ayant une grille connectée au troisième noeud (N3), le troisième transistor (M5) servant à transférer une première tension d'alimentation (V_{DD}) à la borne de sortie (out) conformément à une tension du troisième noeud (N3) ;
dans lequel le commutateur (M1), le premier transistor (M2) de la section de mémorisation et les premier, deuxième et troisième transistors (M3, M4, M5) de la section de commutation sont tous des transistors PMOS ou tous des transistors NMOS.

2. Circuit de commande de balayage selon la revendication 1, dans lequel :

le premier transistor (M3) comprend une grille connectée à la première borne d'horloge (ck1), une source connectée à la deuxième tension d'alimentation, et un drain connecté au troisième noeud (N3) ;
le deuxième transistor (M4) comprend une source connectée à la première borne d'horloge (ck1), et un drain connecté au troisième noeud (N3) ;
le troisième transistor (M5) comprend une source connectée à la première tension d'alimentation (V_{DD}), et un drain connecté à la borne de sortie (out).

3. Circuit de balayage selon la revendication 1 ou 2, dans lequel la deuxième tension d'alimentation est une tension de masse.

4. Circuit de commande de balayage selon la revendication 1 ou 2, dans lequel chaque section de commutation comprend :

un quatrième transistor (M2) connecté au commutateur, le quatrième transistor (M2) servant à transférer la troisième horloge (CLK3) à un

deuxième noeud (N2) conformément à une tension d'un premier noeud (N1) qui a reçu le signal d'entrée ; et
dans lequel le condensateur (C1) sert à maintenir une tension entre le premier noeud (N1) et le deuxième noeud (N2).

5. Circuit de commande de balayage selon l'une quelconque des revendications précédentes, dans lequel la pluralité d'étages sont conçus pour fonctionner pendant une période de précharge, une période d'entrée, une période d'évaluation et une période de repos, dans lequel chacun de la pluralité d'étages est conçu pour initialiser la section de mémorisation pendant la période de précharge, pour recevoir et mémoriser un signal prédéterminé pendant la période d'entrée, pour délivrer un signal de balayage correspondant au signal prédéterminé pendant la période d'évaluation, et pour ne pas fonctionner en réponse au premier signal d'horloge, au deuxième signal d'horloge et au troisième signal d'horloge pendant la période de repos.

6. Circuit de commande de balayage selon l'une quelconque des revendications 1 à 5, dans lequel la pluralité d'étages sont conçus pour fonctionner pendant une période de précharge, une période d'entrée et une période d'évaluation, dans lequel chacun de la pluralité d'étages est conçu pour initialiser la section de mémorisation et pour délivrer une tension de niveau haut pendant la période de précharge, pour recevoir le signal d'entrée et pour maintenir la tension de niveau haut pendant la période d'entrée, et pour délivrer une tension de niveau bas pendant la période d'évaluation.

7. Circuit de commande de balayage selon la revendication 5 ou 6, dans lequel chacun de la pluralité d'étages est conçu pour fonctionner dans la période d'entrée lorsque l'étage précédent parmi les étages délivre un signal de niveau bas.

8. Circuit de commande de balayage selon l'une quelconque des revendications précédentes, dans lequel la première horloge (CLK1), la deuxième horloge (CLK2) et la troisième horloge (CLK3) ont la même période, mais sont décalées en phase les unes par rapport aux autres.

9. Circuit de commande de balayage selon l'une quelconque des revendications précédentes, dans lequel la première tension d'alimentation (V_{DD}) est une tension d'une source de puissance de commande.

10. Circuit de commande de balayage selon l'une quelconque des revendications précédentes, dans lequel le commutateur est un premier transistor (M1).

11. Afficheur électroluminescent organique comprenant :

une région d'affichage (30) comportant une pluralité de pixels (40) pour afficher une image ;
un circuit de commande de balayage (10) selon l'une quelconque des revendications précédentes pour transférer un signal de balayage à la région d'affichage ; et
un circuit de commande de données (20) pour transférer un signal de données à la région d'affichage (30).

FIG. 1
(PRIOR ART)

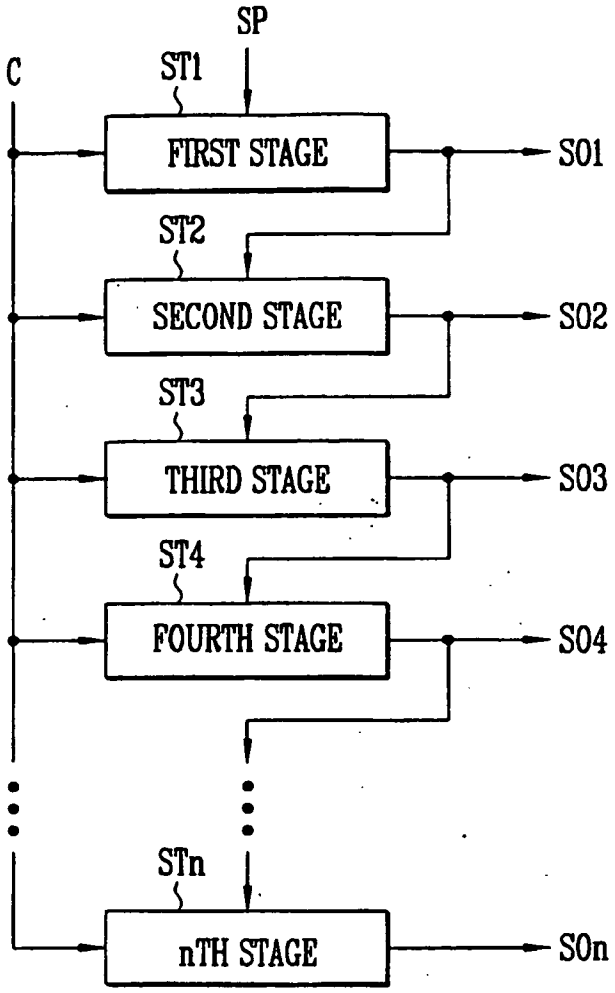


FIG. 2
(PRIOR ART)

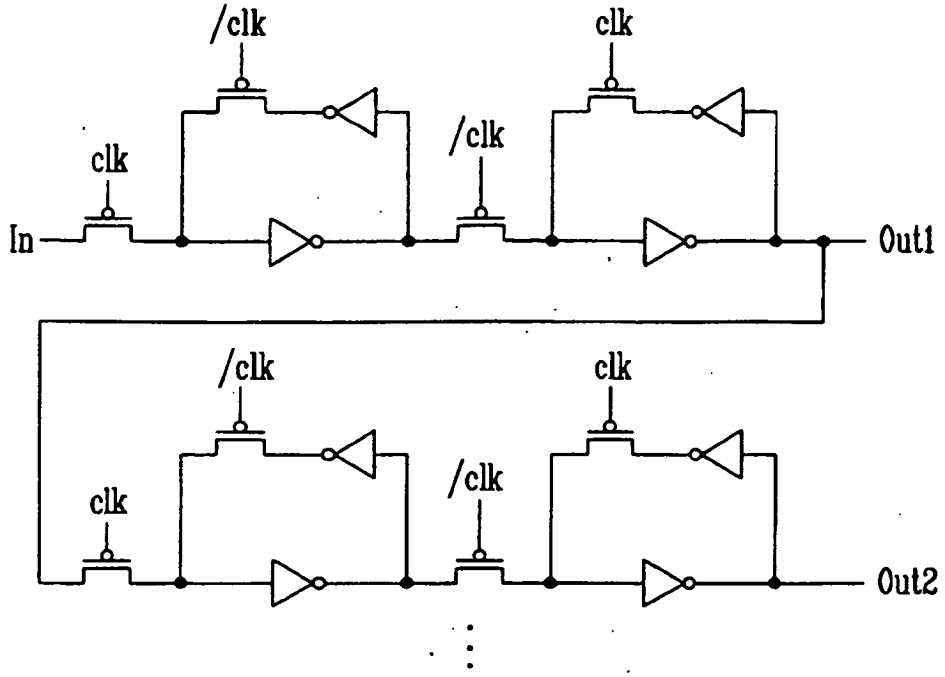


FIG. 2A
(PRIOR ART)

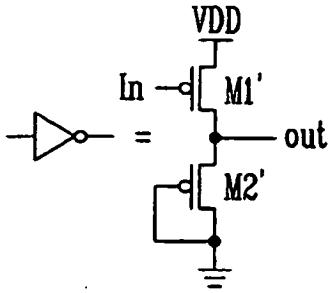


FIG. 3
(PRIOR ART)

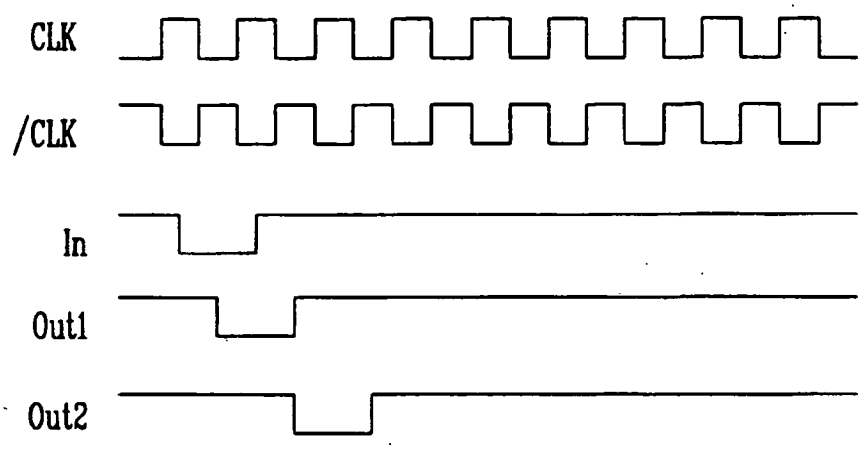


FIG. 4

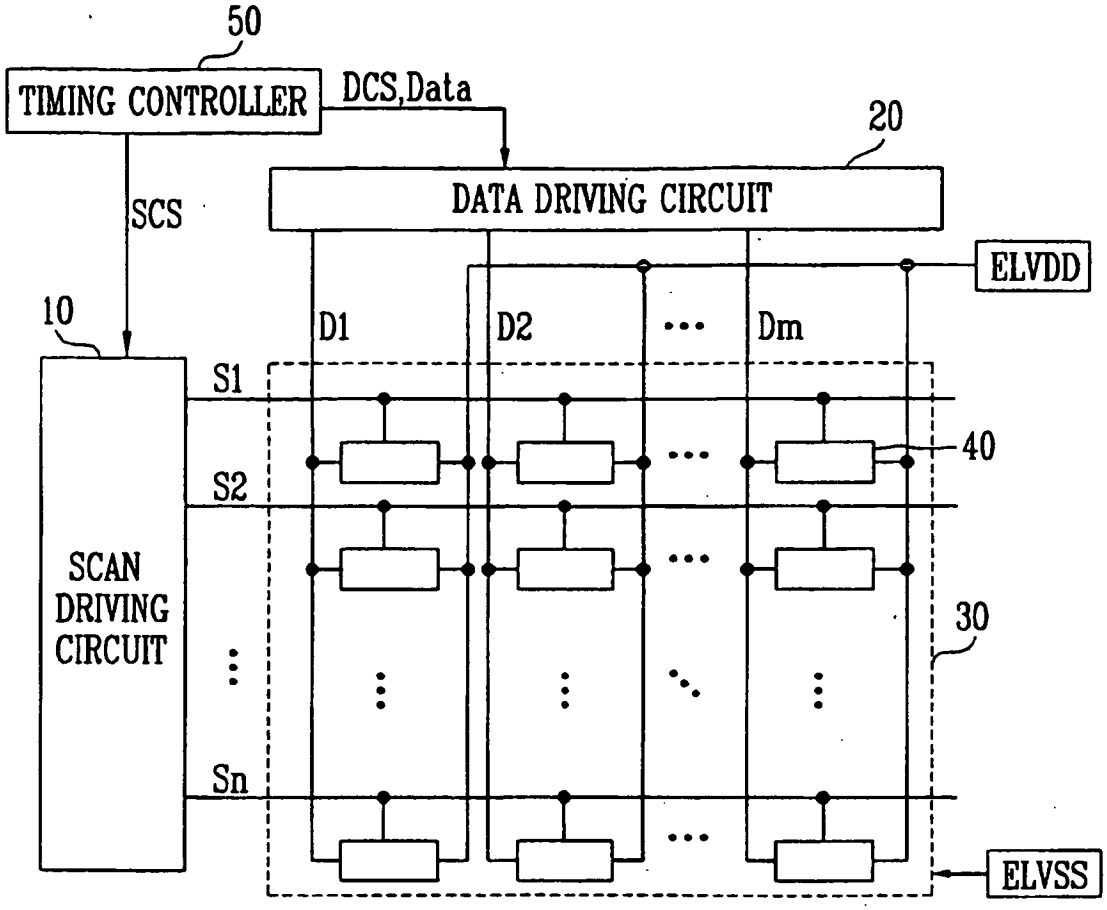

50
TIMING CONTROLLER
DCS,Data
20
DATA DRIVING CIRCUIT
SCS
ELVDD
10
D1
D2
Dm
S1
S2
40
SCAN DRIVING CIRCUIT
30
Sn
ELVSS

FIG. 5

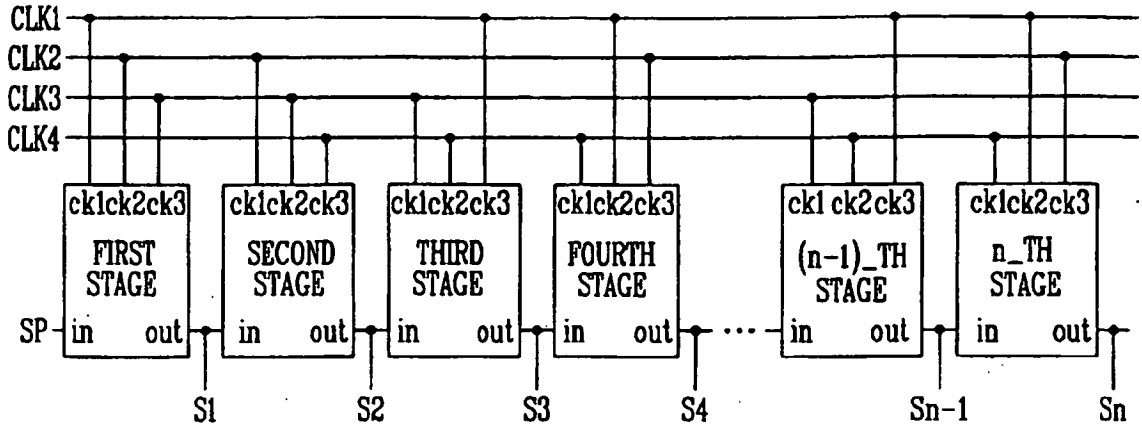

CLK1
CLK2
CLK3
CLK4
ck1ck2ck3
FIRST STAGE
SECOND STAGE
THIRD STAGE
FOURTH STAGE
(n-1)_TH STAGE
n_TH STAGE
SP
in
out
S1
S2
S3
S4
Sn-1
Sn

FIG. 6

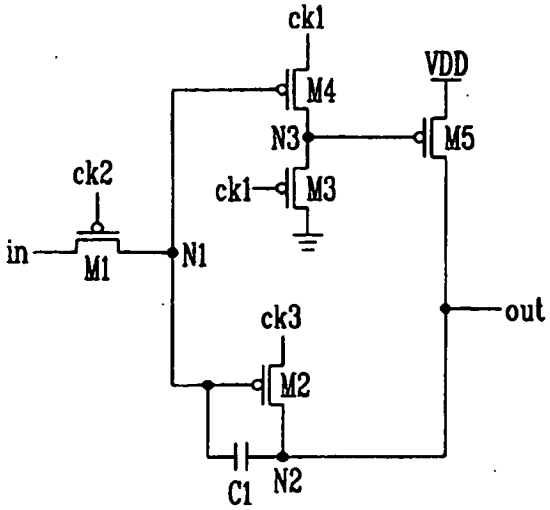

ck1
VDD
M4
N3
M5
ck2
ck1
M3
in
M1
N1
ck3
out
M2
C1
N2

FIG. 7

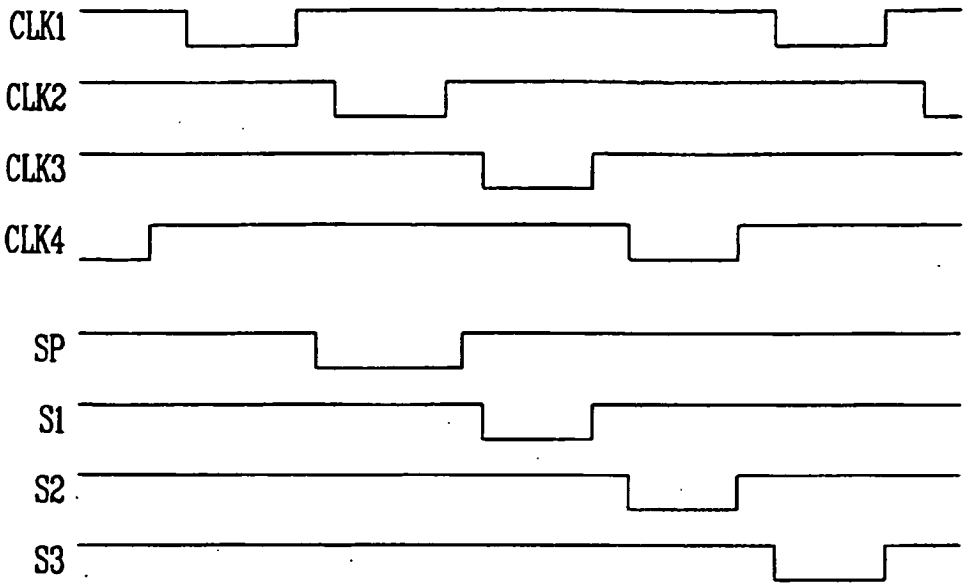

CLK1
CLK2
CLK3
CLK4
SP
S1
S2
S3

FIG. 8

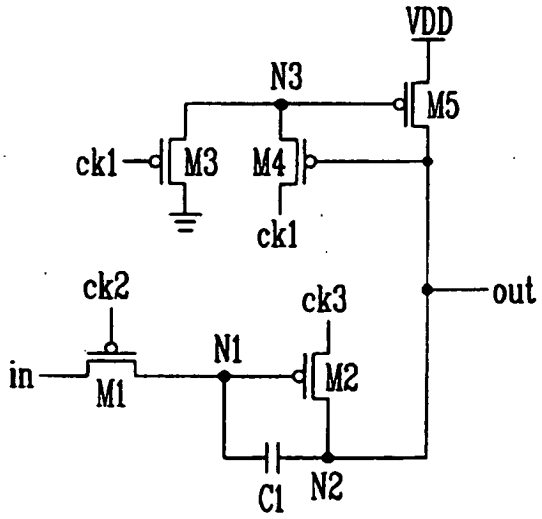

VDD
N3
M5
ck1
M3
M4
ck1
ck2
ck3
out
in
M1
N1
M2
C1
N2

FIG. 13

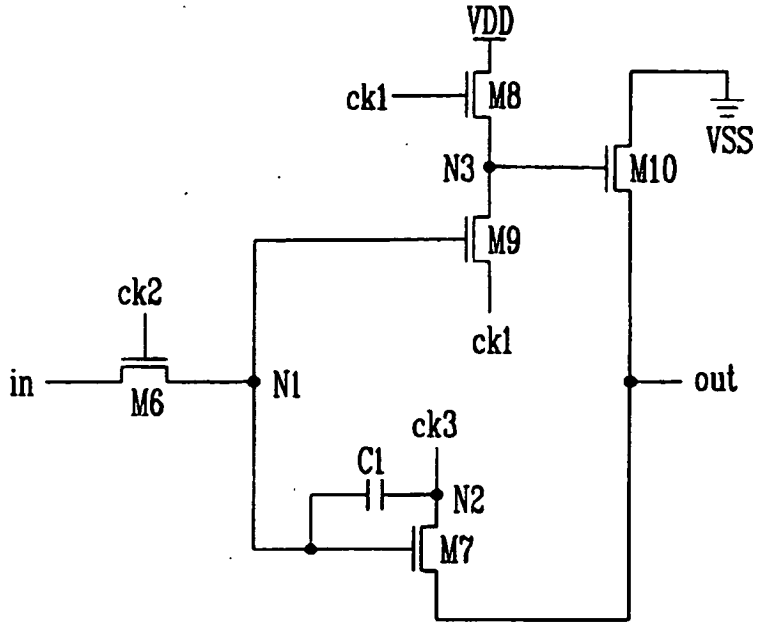
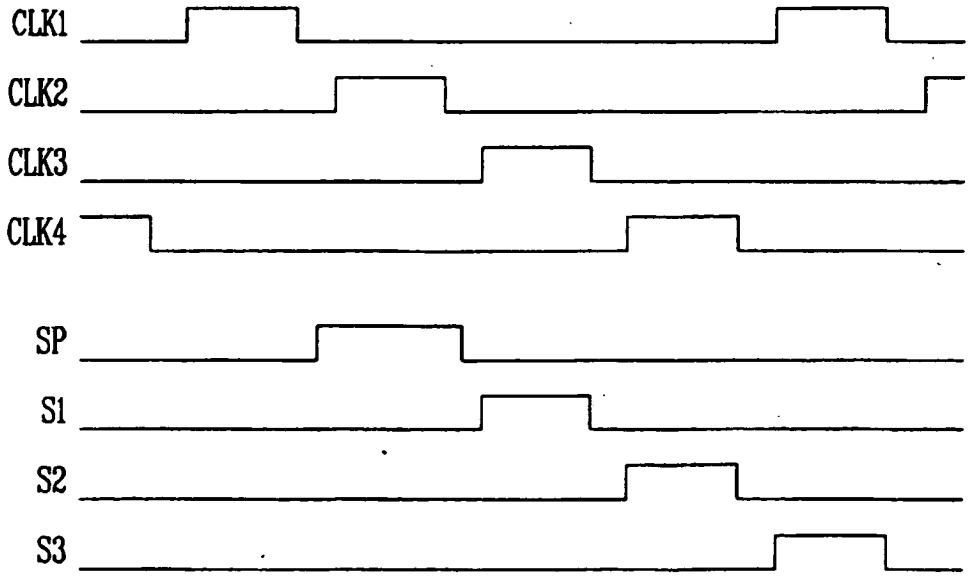

VDD
ck1
M8
VSS
N3
M10
M9
ck2
ck1
in
M6
N1
out
ck3
C1
N2
M7

FIG. 14


CLK1
CLK2
CLK3
CLK4
SP
S1
S2
S3

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20040227718 A **[0013]**

专利名称(译)	扫描驱动电路和使用其的有机发光显示器		
公开(公告)号	EP1847983B1	公开(公告)日	2012-01-25
申请号	EP2007251479	申请日	2007-04-03
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
[标]发明人	SHIN DONG YONG SAMSUNG SDI CO LTD		
发明人	SHIN, DONG YONG, SAMSUNG SDI CO., LTD		
IPC分类号	G09G3/32 G11C19/18		
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优先权	1020060034960 2006-04-18 KR		
其他公开文献	EP1847983A1		
外部链接	Espacenet		

摘要(译)

扫描驱动电路包括多个级。每级接收可以顺序产生的四个时钟信号中的三个，通过输入端子接收和延迟输入信号，并通过输出端子输出输出信号。每级的输入端连接到前一级的输出端。每个级包括晶体管，开关部分和存储部分。晶体管根据第二时钟信号关断/接通输入端子的连接。开关部分根据第一时钟信号将第一电压传送到输出端子，并根据输入信号防止第一电压传送到输出端子。存储部分将输出端子的电压保持预定时间，并根据输入信号将第三时钟信号的电压传送到输出端子。