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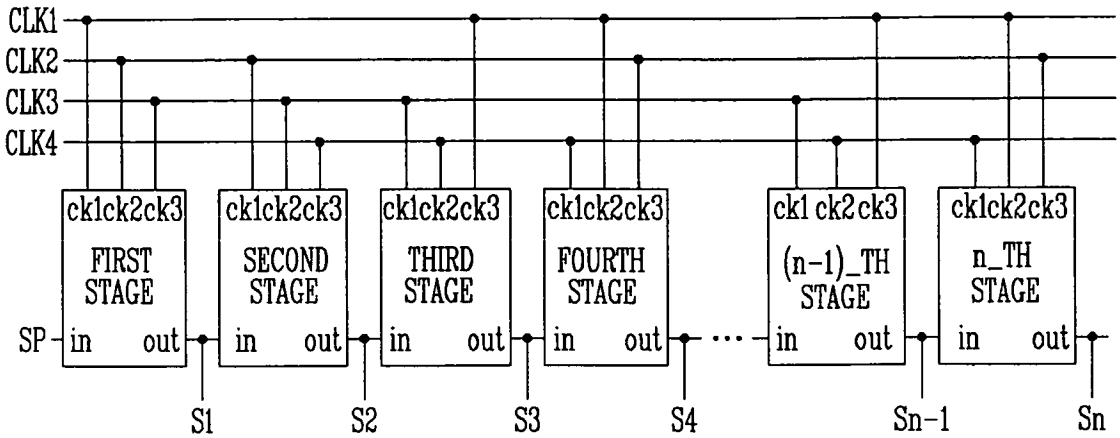
(54) Scan driving circuit and organic light emitting display using the same

(57) A scan driving circuit includes a plurality of stages. Each stage receives three of four clock signals that may be sequentially generated, receives and delays an input signal through an input terminal, and outputs an output signal through an output terminal. The input terminal of each stage is connected to the output terminal of a previous one of the stages. Each stage includes a transistor, a switch section, and a storage section. The transistor turns off/on a connection of the input terminal according to a second clock signal. The switch section transfers a first voltage to the output terminal according to a first clock signal and prevents the first voltage from being transferred to the output terminal according to the input signal. The storage section maintains a voltage of the output terminal for a predetermined time and transfers a voltage of a third clock signal to the output terminal according to the input signal.

FIG. 5



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Description

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a scan driving circuit and an organic light emitting display using the same.

2. Discussion of Related Art

[0002] In general, an active matrix type display device such as an organic light emitting display includes a pixel array arranged at intersections between data lines and scan lines in a matrix pattern.

[0003] The scan lines include horizontal lines (i.e., row lines) of a display region having a matrix of pixels, and sequentially provide a predetermined signal, namely, a scan signal from a scan driving circuit, to the pixel array.

[0004] FIG. 1 is a block diagram showing a conventional scan driving circuit. With reference to FIG. 1, the conventional scan driving circuit includes a plurality of stages ST1 to STn, which are dependently coupled with a start pulse SP input line. The plurality of stages ST1 to STn sequentially shift a clock signal C in response to a start pulse SP to generate output signals SO1 to SOn, respectively. In this case, each of second to n-th stages ST2 to STn receives and shifts an output signal of a previous stage as a start pulse.

[0005] Accordingly, the stages generate output signals SO1 to SOn in such a way that the start pulse is sequentially shifted, and provide the output signals to the pixel array.

[0006] FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1. FIG. 3 is a timing diagram of the stage shown in FIG. 2. Referring to FIG. 2 and FIG. 3, conventionally, each stage of a scan driving circuit uses a master-slave flip-flop. When a clock signal CLK is at a low level, such a flip-flop continues to receive an input and maintains a previous output.

[0007] In contrast to this, when the clock signal CLK is at a high level, the flip-flop maintains an input In received at an input terminal when the clock signal CLK is at the low level, and outputs the received input, but no longer receives the input In.

[0008] In the aforementioned circuit, an inverter included in the flip-flop has a problem in that a static current flows when an input thereof is at a low level. Furthermore, in the flip-flop, the number of inverters having received a high-level input is the same number as that of inverters having received a low-level input. Accordingly, the static current flows through a half of all the inverters in the flip-flop, thereby causing power consumption to be increased.

[0009] In addition, in the circuit of FIG. 2A, a voltage value due to a ratio of resistance (i.e., transistors M1' and M2') connected between a power supply VDD and a ground GND determines a high level of an output voltage OUT. Low level of the output voltage OUT is set to be greater than that of the ground GND by a threshold voltage of the transistor M2'.

[0010] By way of example, due to characteristic deviations of the transistors, since levels of an input voltage are different according to respective stages, in the case where the circuit of FIGs. 2 and 2A is used, the deviation occurs when the output voltage is at a high level, with the result that the circuit may be erroneously operated.

[0011] Moreover, the deviation in a low level of the output voltage causes a deviation in on-resistance of an input transistor of an inverter included in the circuit of FIG. 2 to occur, thereby weighting a deviation in a high level of the output voltage. In particular, since a panel of an organic light emitting display uses a transistor having a great characteristic deviation, such a problem is more serious.

[0012] Further, in the inverter, an electric current flows through an input transistor to charge an output terminal, whereas the electric current flows through a load transistor to discharge the output terminal. Upon a charge of the output terminal, a source-gate voltage of the load transistor is gradually reduced, and a discharge current is accordingly reduced rapidly. This causes the discharge efficiency to be deteriorated.

SUMMARY OF THE INVENTION

[0013] Accordingly, a first aspect of the present invention provides a scan driving circuit as set out in claim 1.. The scan driving circuit may be implemented with PMOS transistors or NMOS transistors, which switch an output voltage of the scan driving circuit from a positive source voltage to a negative source voltage. Preferred features are set out in claims 2 to 15. According to a second aspect of the invention there is provided an organic light emitting display as set out in claim 16.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] These and/or other aspects and features of the invention will become apparent and more readily appreciated from the following description of embodiments of the invention, taken in conjunction with the accompanying drawings of which:

[0015] FIG. 1 is a block diagram showing a conventional scan driving circuit;

[0016] FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1;

[0017] FIG. 2A is a circuit diagram of an inverter in the stage shown in FIG. 2;

[0018] FIG. 3 is a timing diagram of the stage shown in FIG. 2;

[0019] FIG. 4 is a block diagram showing an organic light emitting display according to an embodiment of the present invention;

[0020] FIG. 5 is a block diagram showing a construc-

tion of a scan driving circuit according to an embodiment of the present invention;

[0021] FIG. 6 is a circuit diagram showing a first embodiment of a stage of the scan driving circuit shown in FIG. 5;

[0022] FIG. 7 is a timing diagram showing a first embodiment of an input/output waveform of the stage shown in FIG. 6;

[0023] FIG. 8 is a circuit diagram showing a second embodiment of a stage of the scan driving circuit shown in FIG. 5;

[0024] FIG. 9 is a circuit diagram showing a third embodiment of a stage of the scan driving circuit shown in FIG. 5;

[0025] FIG. 10 is a circuit diagram showing a fourth embodiment of a stage of the scan driving circuit shown in FIG. 5;

[0026] FIG. 11 is a circuit diagram showing a fifth embodiment of a stage of the scan driving circuit shown in FIG. 5;

[0027] FIG. 12 is a timing diagram of the stage shown in FIG. 11;

[0028] FIG. 13 is a circuit diagram showing a sixth embodiment of a stage of the scan driving circuit shown in FIG. 5; and

[0029] FIG. 14 is a timing diagram of the stage shown in FIG. 13.

DETAILED DESCRIPTION

[0030] Hereinafter, embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being connected to a second element, the first element may be not only directly connected to the second element but also may be indirectly connected to the second element via a third element. Further, elements that are not essential to the complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0031] FIG. 4 is a block diagram showing an organic light emitting display according to an embodiment of the present invention. With reference to FIG. 4, the organic light emitting display includes a display region 30, a scan driving circuit 10, a data driving circuit 20, and a timing controller 50.

[0032] The display region 30 includes a plurality of pixels 40 formed at crossing areas of scan lines S1 to Sn, and data lines D1 to Dm. The scan driving circuit 10 drives the scan lines S1 to Sn. The data driving circuit 20 drives the data lines D1 to Dm. The timing controller 50 controls the scan driving circuit 10 and the data driving circuit 20.

[0033] The timing controller 50 generates a data drive control signal DCS and a scan drive control signal SCS according to externally supplied synchronous signals. The data drive control signal DCS generated by the timing controller 50 is provided to the data driving circuit 20, and the scan drive control signal SCS is provided to the scan driving circuit 10. Furthermore, the timing controller 50 provides externally supplied data Data to the data driving circuit 20.

[0034] The data driving circuit 20 receives the data drive control signal DCS from the timing controller 50. Upon the receipt of the data drive control signal DCS, the data driving circuit 20 generates data signals, and provides the generated data signals to the data lines D1 to Dm. In this embodiment, the data driving circuit 20 provides the generated data signals to the data lines D1 to Dm every one horizontal period.

[0035] The display region 30 receives a first power from a first power supply ELVDD and a second power from a second power supply ELVSS from an exterior source, and provides them to the pixels 40. Upon the receipt of the first power ELVDD and the second power ELVSS, the pixels 40 control an amount of current that flows into the second power supply ELVSS from the first power supply ELVDD through a light emitting element corresponding to the data signal, thus generating light corresponding to the data signal.

[0036] The scan driving circuit 10 generates a scan signal in response to a scan drive control signal SCS from the timing controller 50, and sequentially provides the generated scan signal to the scan lines S1 to Sn. That is, the scan driving circuit 10 sequentially generates the scan signal to drive the plurality of pixels, and provides the scan signal to the display region 30.

[0037] Hereinafter, a construction and an operation of the scan driving circuit of an organic light emitting display according to an embodiment of the present invention will be explained.

[0038] FIG. 5 is a block diagram showing a configuration of a scan driving circuit 30 according to an embodiment of the present invention. Referring to FIG. 5, the scan driving circuit includes n stages that are dependently coupled with a start pulse input line so as to drive an m x n pixel array.

[0039] First output lines of the first n stages are coupled with first n scan lines (i.e., row lines) included in the pixel array. A start pulse SP is supplied to a first stage. Output signals of first to n-1 th stages are provided to next stages as a start pulse, respectively. Each stage receives and operates according to a first clock signal CLK1, a second clock signal CLK2, and a third clock signal CLK3; the second clock signal CLK2, the third clock signal CLK3, and a fourth clock signal CLK4; the third clock signal CLK3, the fourth clock signal CLK4, and the first clock signal CLK1; or the fourth clock signal CLK4, the first clock signal CLK1, and the second clock signal CLK2. That is, each stage operates in response to three of the four supplied clock signals: the first clock signal CLK1, the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4. Each stage includes a first clock terminal ck1, a second clock terminal ck2, and a third clock terminal ck3. Here, as shown, the first clock signal CLK1, the second clock signal CLK2, and the third clock signal CLK3 are supplied to the first

clock terminal ck1, the second clock terminal ck2, and the third clock terminal ck3 of a (4k-3)-th stage, respectively. The second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4 are supplied to the first clock terminal ck1, the second clock terminal ck2, and the third clock terminal ck3 of a (4k-2)-th stage, respectively. The first clock signal CLK1, the third clock signal CLK3, and the fourth clock signal CLK4 are supplied to the third clock terminal ck3, the first clock terminal ck1, and the second clock terminal ck2 ofa(4k-1)-th stage, respectively. The first clock signal CLK1, the second clock signal CLK2, and the fourth clock signal CLK4 are supplied to the second clock terminal ck2, the third clock terminal ck3, and the first clock terminal ck1 of a (4k)-th stage, respectively. Here, k is a natural number.

[0040] Further, when the first stage outputs a signal in response to the first clock signal CLK1, the second clock signal CLK2, and the third clock signal CLK3, the second stage receives and operates according to the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4. When the second stage outputs a signal in response to the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4, the third stage receives and operates according to the third clock signal CLK3, the fourth clock signal CLK4, and the first clock signal CLK1. When the third stage outputs a signal in response to the third clock signal CLK3, the fourth clock signal CLK4, and the first clock signal CLK1, the fourth stage receives and operates according to the fourth clock signal CLK4, the first clock signal CLK1, and the second clock signal CLK2. That is, the first, second, third, and fourth stages sequentially output the signal to sequentially drive a display region of an organic light emitting display by lines.

[0041] An external control circuit (not shown) provides the input signals of the driving circuit, that is, a start pulse SP, the first to fourth clock signals CLK 1 to CLK4, and a supply voltage VDD.

[0042] FIG. 6 is a circuit diagram showing a first embodiment of a stage of the scan driving circuit shown in FIG. 5. In accordance with a first embodiment of the invention FIG. 7 is a timing diagram showing an input/output waveform of the stage shown in FIG. 6.

[0043] As shown in FIG. 6, in the first embodiment of the present invention, transistors included in each stage are all PMOS transistors. Each stage sequentially sends a low level output through the scan driving circuit. Namely, the scan driving circuit according to an embodiment of the present invention outputs a high level signal to a display region of an active matrix type display device such as an organic light emitting display for most of the time, and sequentially outputs a low level pulse through a plurality of stages as shown in FIG. 6 and FIG. 7.

[0044] Referring to FIG. 6, the stage includes a first PMOS transistor M1, a second PMOS transistor M2, a third PMOS transistor M3, a fourth PMOS transistor M4, a fifth PMOS transistor M5, and a first capacitor C 1. The first PMOS transistor M1 includes a gate coupled with a second clock terminal ck2, receives an output voltage Si of a previous stage or a first start pulse SP, and selectively transfers the output voltage Si of a previous stage or the first start pulse SP to a first node N1. The second PMOS transistor M2 includes a gate connected to the first node N1, and is coupled between the third clock terminal ck3 and a second node N2. The third PMOS transistor M3 includes a gate connected to the first clock terminal ck1, and is connected between a ground and a third node N3. The fourth PMOS transistor M4 includes a gate connected to the first node N1, and is connected between the first clock terminal ck1 and the third node N3. The fifth PMOS transistor M5 includes a gate connected to the third node N3, and is coupled between a power supply line VDD and the second node N2. The first capacitor C1 is connected between the first node N1 and the second node N2, and maintains a predetermined voltage.

[0045] Although it is shown that M3 is coupled to a ground, M3 may alternatively be coupled to a negative power supply VSS.

[0046] Hereinafter, through a circuit arrangement of (4k-3)-th stage among stages shown in FIG. 6, operation of the stages will be explained with specific reference to the first stage, the first stage having the first clock terminal ck1 connected to the first clock signal CLK1, the second clock terminal ck2 connected to the second clock signal CLK2, and the third clock terminal ck3 connected to the third clock signal CLK3.

[0047] With reference to FIGs. 6 and 7, each stage of the scan driving circuit may divide one period into a precharge period, an input period, an evaluation period, and a quiescent period according to the first clock signal CLK1, the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4. During the precharge period, a low level signal is inputted to the first clock terminal ck1 of the stage, and a high level signal is inputted to the second clock terminal ck2 and the third clock terminal ck3 to precharge a capacitor C 1 of the stage. During the input period, a low level signal is inputted to the second clock terminal ck2, and a high level signal is inputted to the first clock terminal ck1 and the third clock terminal ck3. Further, a start pulse SP or a scan signal Si of a previous stage is inputted through the input terminal to the first node N 1 and is stored in the capacitor C1. During the evaluation period, a low level signal is inputted to the third clock terminal ck3, and a high level signal is inputted to the first clock terminal ck1 and the second clock terminal ck2, so that the stage outputs a low level signal within a predetermined period. Further, a start pulse SP or a scan signal Si of a previous stage is inputted through the input terminal. During the evaluation period, a low level signal is inputted to the third clock terminal ck3, and a high level signal is inputted through the first clock terminal ck1 and the second clock terminal ck2, so that the stage shifts and outputs a scan signal of a low level pulse by a predetermined time. In addition, the quiescent period is a time period when the fourth clock signal CLK4 which was not inputted to the

stage has a low level.

[0048] During the precharge period, when the first clock signal CLK1 becomes a low level, the third PMOS transistor M3 is turned-on to make a voltage of the third node N3 a ground voltage. Accordingly, the fifth PMOS transistor M5 is turned-on to output a voltage of a power supply voltage VDD through an output terminal out, with the result that a high level voltage is outputted to the output terminal out. That is, a scan signal is outputted with a high level. Further, during the input period, the second clock signal CLK2 becomes a low level, the start pulse SP or the scan signal Si of a previous stage is transferred to the first node N1 through the first PMOS transistor M1, and the start pulse SP or the scan signal Si of a previous stage is stored in the capacitor C 1. At this time, because the start pulse SP or the scan signal Si of a previous stage is low, the second PMOS transistor M2 and the fourth PMOS transistor M4 are turned-on. Further, the first clock signal CLK1 becomes a high level to turn-off the third PMOS transistor M3. When the third PMOS transistor M3 is turned-off and the fourth PMOS transistor M4 is turned-on, a first clock signal CLK1 of a high level is transferred to the third node N3 to turn-off the fifth PMOS transistor M5. At this time, the second PMOS transistor M2 is turned-off, so that an output terminal outputs a high level signal according to a third clock signal CLK3 of a high level. Moreover, during the evaluation period, the third clock signal CLK3 becomes a low level to float the first PMOS transistor M1. This causes the capacitor C1 to maintain a low level signal, thereby turning-on the second PMOS transistor M2 and the fourth PMOS transistor M4. In contrast to this, the third PMOS transistor M3 and the fifth PMOS transistor M5 are turned-off. Consequently, a low level signal is outputted to the output terminal out according to the third clock signal CLK3 of a low level.

[0049] That is, the output terminal out outputs a high level voltage by a power supply line VDD during the precharge period, and maintains a high level voltage by the capacitor C1 during the input period. Further, during the evaluation period, a voltage corresponding to the third clock signal CLK3 of a low level is outputted. When the third clock signal CLK3 becomes a low level, a voltage of the output terminal out drops. In contrast to this, when the third clock signal CLK3 becomes a high level, the voltage of the output terminal out again becomes a high level. Accordingly, the output terminal out outputs a scan signal. Furthermore, during the quiescent period, the first clock signal CLK1, the second clock signal CLK2, and the third clock signal CLK3 are transferred with a high level, but the fourth clock signal CLK4 of a low level is not transferred to the stage, so that the stage does not operate in response to clock signals.

[0050] As a result, when a low level signal is not inputted to an input terminal in of each stage, the second PMOS transistor M2 is turned-off, so that the output terminal out maintains a high level signal. Thus, only when each stage receives the start pulse SP or a low level signal of a previous stage, it outputs a low level signal that results in a sequential output of the scan signal.

[0051] FIG. 8 is a circuit diagram showing a stage for the scan driving circuit shown in FIG. 5 according to a second embodiment of the invention. Referring to FIG. 8, the stage includes a first PMOS transistor M1, a second PMOS transistor M2, a third PMOS transistor M3, a fourth PMOS transistor M4, a fifth PMOS transistor M5, and a capacitor C1.

[0052] The first PMOS transistor M1 transfers an input signal to the first node N1 in response to the second clock signal CLK2, and the second PMOS transistor M2 transfers the third clock signal CLK3 to the second node N2 corresponding to a voltage of the first node N1. The third PMOS transistor M3 transfers a ground voltage to a gate of the fifth transistor PMOS M5 in response to the first clock signal CLK1. A gate of the fourth PMOS transistor M4 is connected to the output terminal out, and the fourth transistor M4 transfers the first clock signal CLK1 to a gate of the fifth PMOS transistor M5 corresponding to a voltage of the output terminal out. Further, the fifth PMOS transistor M5 transfers a voltage of a power supply line VDD to the output terminal corresponding to a voltage of a gate thereof. Moreover, the capacitor C1 is connected between the first node N 1 and the second node N2, and maintains a predetermined voltage.

[0053] The stage having the construction as described above receives and operates according to the first to third clock signals CLK1 to CLK3 shown in FIG. 7. During the precharge period, the fifth PMOS transistor M5 is turned-on in response to the first clock signal CLK1 to output a high level signal to the output terminal out by a voltage of the power supply line VDD. During the input period, the start pulse SP or a scan signal Si of a previous stage is stored in the capacitor C 1 in response to the second clock signal CLK2. Next, the voltage stored in the capacitor C 1 causes a voltage of the third clock signal CLK3 to be outputted, so that the output terminal out maintains a high level signal. At this time, when a voltage of the output terminal has a low level, the fourth PMOS transistor M4 transfers a high level signal to a gate of the fifth PMOS transistor M5, thereby preventing a voltage of the power supply line VDD from being transferred to the output terminal.

[0054] FIG. 9 is a circuit diagram showing a stage for of the scan driving circuit shown in FIG. 5 in accordance with a third embodiment of the invention. The stage shown in FIG. 9 has substantially the same construction and functions as those of FIG. 6. The difference of the stage of FIG. 9 from that of the FIG. 6 is that the sixth PMOS transistor M6 is connected to a source of the fourth PMOS transistor M6, and a power supply line VDD is connected to a source of the sixth PMOS transistor M6. Accordingly, when the third clock signal CLK3 has a low level, the fourth PMOS transistor M4 is turned-on, so that a voltage of the power supply line VDD is transferred to the third node N3 to turn-off the fifth PMOS transistor M5. In other words, the voltage of the power supply line VDD

which is not a clock signal, is transferred to a gate of the fifth PMOS transistor M5 to ensure a turning-off state of the fifth PMOS transistor M5. Accordingly, when the third clock signal CLK3 has a low level, the stage prevents a voltage of the power supply line VDD from being transferred to an output terminal through the fifth PMOS transistor M5. Thus, when the third clock signal CLK3 has a low level, the stage ensures a voltage of the output terminal to be dropped to a low level.

[0055] FIG. 10 is a circuit diagram showing a stage for the scan driving circuit shown in FIG. 5 in accordance with a fourth embodiment of the invention. With reference to FIG. 10, a stage of FIG. 10 has substantially the same construction and functions as those of FIG. 9. In particular, when the third clock signal CLK3 has a low level, a voltage of the power supply line VDD is transferred to the third node N3 in the same manner as that of FIG. 9. The difference of a stage of FIG. 10 from that of the FIG. 9 is that the third clock signal CLK3 is transferred to a gate of the fourth PMOS transistor M4, and a gate of the sixth PMOS transistor M6 is connected to the third node N3.

[0056] FIG. 11 is a circuit diagram showing a stage for the scan driving circuit shown in FIG. 5 in accordance with a fifth embodiment of the invention. With reference to FIG. 11, a stage of FIG. 11 has substantially the same construction and functions as those of FIG. 8 except that a source and a gate of a third PMOS transistor M3 receive the first clock signal CLK1. Accordingly, when the first clock signal CLK1 has a low level, the fifth PMOS transistor M5 is turned-on. Remaining operations of the stage shown in the FIG. 11 is the same as that of FIG. 8.

[0057] FIG. 12 is a timing diagram of the stage shown in FIG. 11. With reference to FIG. 12, signal waveforms of FIG. 12 are applicable to stages of FIG. 8 to FIG. 11. FIG. 11 shows an operation of the stage when at least two of the first to fourth clock signals CLK1 to CLK4 overlap with each other by external influences.

[0058] In FIG. 11, due to the second to fourth clock signals CLK2 to CLK4, the first and second clock signals CLK1 and CLK2, the second and third clock signals CLK2 and CLK3, and the third and fourth clock signals CLK3 and CLK4 overlap with each other. During the evaluation period among precharge period, the input period, the evaluation period, and the quiescent period, the scan signal operates corresponding to an operation of the third clock signal CLK3. During the quiescent period according to the fourth clock signal CLK4, the fourth clock signal CLK4 is not inputted to the stage, so that the fourth clock signal CLK4 does not influence an operation of the stage. Accordingly, an output scan signal of the stage varies depending on a waveform of the third clock signal CLK3. As a result, even if certain parts of respective clock signals overlap with each other, a waveform of the scan signal is not distorted.

[0059] However, after the evaluation period finishes without reaching the quiescent period in response to the fourth clock signal CLK4, when the precharge period again comes, a voltage of a drive power source is transferred to the output terminal out in response to the first clock signal CLK1, thereby distorting a waveform of the scan signal. This prevents a waveform of the scan signal during the quiescent period after the precharge period from being distorted.

[0060] FIG. 13 is a circuit diagram showing a a stage for the scan driving circuit shown in FIG. 5 in accordance with a sixth embodiment of the invention. FIG. 14 is a timing diagram of the stage shown in FIG. 13. With reference to FIG. 13 and FIG. 14, the stage is constructed by NMOS transistors M6, M7, M8, M9, and M10. A stage of FIG. 13 has substantially the same construction as that of FIG. 6, and respective transistors perform substantially the same operation as that of FIG. 6. In other words, the transistors M6, M7, M8, M9, and M10 perform substantially the same functions as transistors M1, M2, M3, M4, and M5, respectively.

[0061] Since the scan driving circuit and an organic light emitting display using the embodiments according to the present invention switch an output voltage from a positive source voltage to a negative source voltage, an operation speed is increased. Furthermore, even if a clock signal transferred to the scan driving circuit is erroneously operated, a change of a waveform of a scan signal is not great.

[0062] Although certain embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in these embodiments without departing from the scope of the invention which is defined in the appended claims.

Claims

1. A scan driving circuit comprising a plurality of stages, the plurality of stages being collectively adapted to receive four clock signals, wherein each of the plurality of stages is respectively configured to receive three of the four clock signals, to receive and delay an input signal through an input terminal, and to output an output signal through an output terminal, wherein the input terminal of each of the plurality of stages is connected to the output terminal of a previous one of the stages, wherein each of the plurality of stages comprises:

   a switch for turning on/off a connection of the input terminal according to a second clock signal, the second clock signal being input through a second clock terminal;
   a switch section for transferring a first voltage to the output terminal according to a first clock signal for preventing the first voltage from being transferred to the output terminal according to the input signal, the first clock signal being input through a first clock terminal; and

a storage section for maintaining a voltage of the output terminal for a predetermined time, and for transferring a voltage of a third clock signal among the clocks to the output terminal according to the input signal, the third clock signal being input through a third clock terminal.

2. A scan driving circuit as claimed in claim 1 wherein each switch section is for preventing the first voltage from being transferred to the output terminal according to the input signal.

3. A scan driving circuit as claimed in claim 1 or 2, wherein each storage section comprises:

a second transistor connected to the switch the second transistor being for transferring the third clock to a second node according to a voltage of a first node that received the input signal; and
a capacitor for maintaining a voltage between the first node and the second node.

4. A scan driving circuit as claimed in any preceding claim , wherein each switch section comprises:

a third transistor for transferring a second voltage to a third node according to a voltage of the first clock signal;
a fourth transistor for transferring the voltage of the first clock signal to the third node according to the input signal, wherein the third node is between the third transistor and fourth transistor;
a fifth transistor including a gate connected to the third node, the fifth transistor for transferring the first voltage to the output terminal according to a voltage of the third node.

5. A scan driving circuit as claimed in any one of claims 1 to 3, wherein the switch section comprises:

a third transistor including a gate connected to the first clock terminal, a source connected to a second voltage, and a drain connected to a third node;
a fourth transistor including a gate connected to the first node, a source connected to the first clock terminal, and a drain connected to the third node;
a fifth transistor including a gate connected to the third node, a source connected to the first voltage, and a drain connected to the output terminal.

6. A scan driving circuit as claimed in any one of claims 1 to 3, wherein each switch section comprises:

a third transistor including a gate connected to the first clock terminal, a source connected to a second voltage, and a drain connected to a third node;
a fourth transistor including a gate connected to a third node which is connected to the transistor, a source for receiving the first voltage, and a drain connected to the second node;
a fifth transistor including a gate connected to the third node, a source connected to the first voltage, and a drain connected to the output terminal; and
a sixth transistor including a gate connected to the third clock terminal and a source connected to the first voltage, the sixth transistor for transferring the first voltage to the source of the fourth transistor.

7. A scan driving circuit as claimed in any one of claims 1 to 1, wherein each switch section comprises:

a third transistor including a gate connected to the first clock terminal, a source connected to a second voltage, and a drain connected to a third node;
a fourth transistor including a gate connected to the third clock terminal, and a source for receiving the first voltage, and a drain connected to the third node; and
a fifth transistor including a gate connected to the third node, a source connected to the first voltage, and a drain connected to the output terminal; and
a sixth transistor including a gate connected to the first node which is connected to the switch and a source connected to the first voltage, the sixth transistor for transferring the first voltage to the source of the fourth transistor.

8. The scan driving circuit as claimed in any one of claim 1 to 3, wherein each switch section comprises:

a third transistor for transferring a second voltage to a third node according to a voltage of the first clock signal;
a fourth transistor including a gate connected to the output terminal, a source connected to the first clock terminal, and a drain connected to the third node; and
a fifth transistor including a gate connected to the third node, a source connected to the first voltage, and a drain connected to the output terminal.

9. The scan driving circuit as claimed in any one of claims 1 to 3, wherein the switch section comprises:

a third transistor including a gate and a source connected to the first clock terminal, and a drain connected to a third node;

a fourth transistor including a gate connected to the output terminal, a source connected to the first clock terminal, and a drain connected to the third node; and

a fifth transistor including a gate connected to the third node, a source connected to the first voltage, and a drain connected to the output terminal.

10. A scan driving circuit as claimed in any one of claims 4 to 9 , wherein the second voltage is a ground voltage.

11. A scan driving circuit as claimed in any preceding claim , wherein the plurality of stages are adapted to operate during a precharge period, an input period, an evaluation period, and a quiescent period, wherein each of the plurality of stages is adapted to initialize the storage section during the precharge period, to receive and store a predetermined signal during the input period, to output a scan signal corresponding to the predetermined signal during the evaluation period, and not to operate in response to the first clock signal, the second clock signal, and the third clock during the quiescent period.

12. An organic light emitting display as claimed in any of claims 1 to 10, wherein the plurality of stages are adapted to operate during a precharge period, an input period, and an evaluation period, wherein each of the plurality of stages is adapted to initialize the storage section and to output a high level voltage during the precharge period, to receive the input signal and to maintain the high level voltage during the input period, and to output a low level voltage during the evaluation period.

13. A scan driving circuit as claimed in claim 11 or 12, wherein each of the plurality of stages is adapted to operate in the input period when the previous one of the stages outputs a low level signal.

14. The scan driving circuit as claimed in any preceding claim , wherein the first clock, the second clock, and the third clock have the same period, but are shifted in phase from each other.

15. A scan driving circuit as claimed in any preceding claim , wherein the four clock signals have the same period, but are shifted in phase from each other.

16. A scan driving circuit as claimed in any preceding claim , wherein the first voltage is a voltage of a drive power source.

17. A scan driving circuit as claimed in any preceding claim wherein the switch is a first transistor.

18. An organic light emitting display comprising:

a display region having a plurality of pixels for displaying an image;

a scan driving circuit according to any preceding claim for transferring a scan signal to the display region; and

a data driving circuit for transferring a data signal to the display region.

FIG. 1
(PRIOR ART)

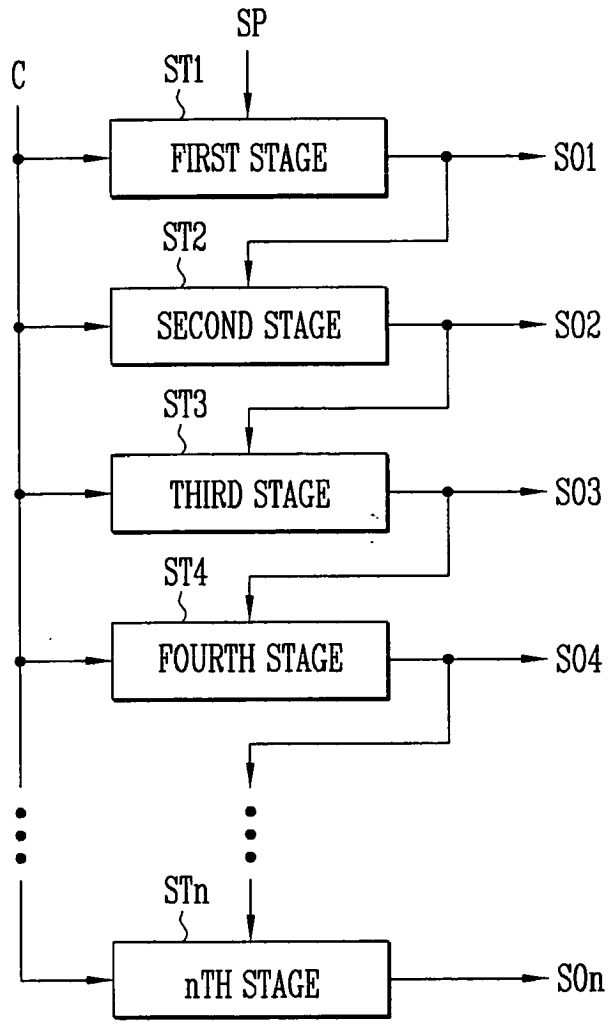


FIG. 2
(PRIOR ART)

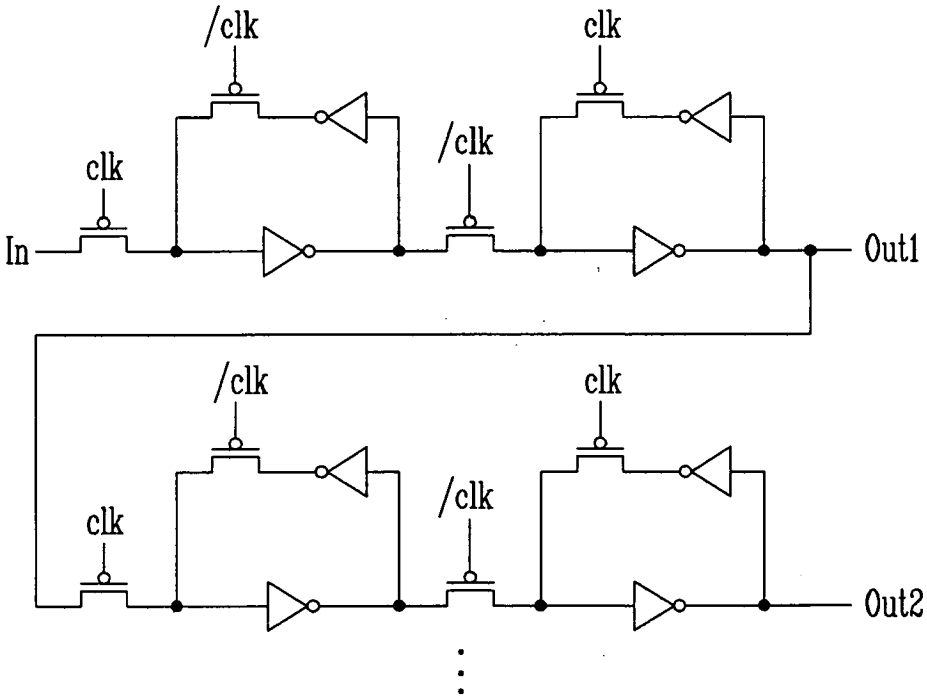


FIG. 2A
(PRIOR ART)

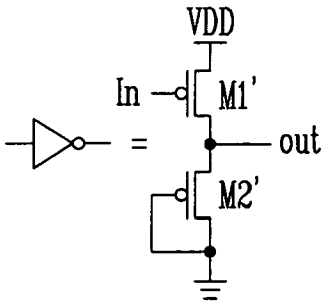


FIG. 3
(PRIOR ART)

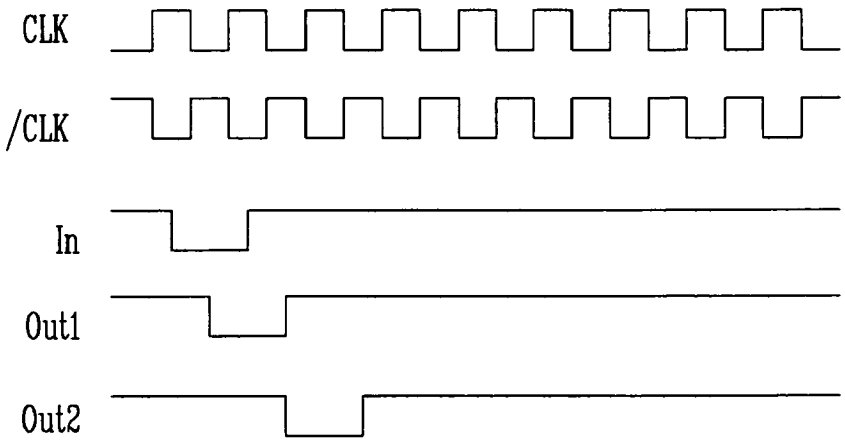


FIG. 4

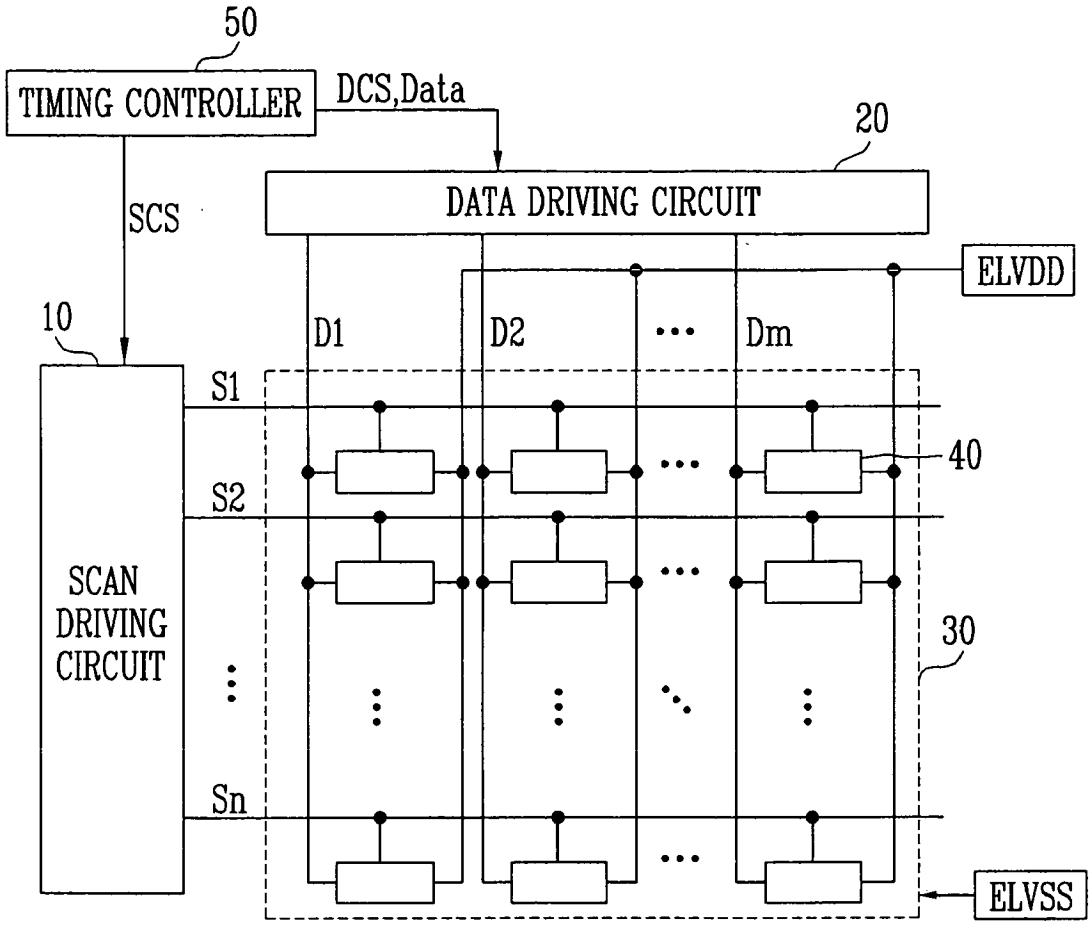

50
TIMING CONTROLLER
DCS,Data
20
DATA DRIVING CIRCUIT
SCS
ELVDD
10
D1
D2
Dm
S1
S2
40
SCAN DRIVING CIRCUIT
30
Sn
ELVSS

FIG. 5

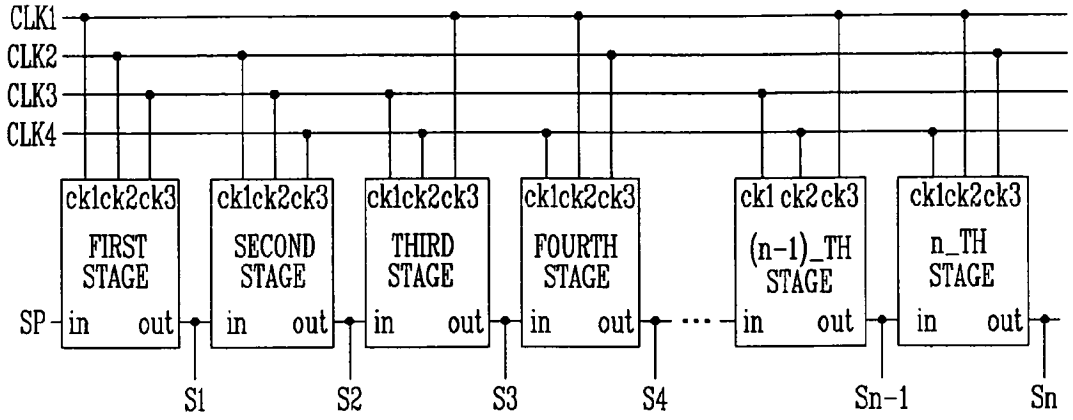

CLK1
CLK2
CLK3
CLK4
ck1ck2ck3
FIRST STAGE
SECOND STAGE
THIRD STAGE
FOURTH STAGE
(n-1)_TH STAGE
n_TH STAGE
SP
in
out
S1
S2
S3
S4
Sn-1
Sn

FIG. 6

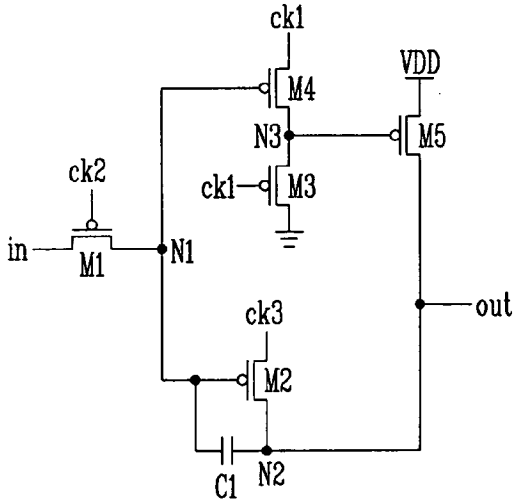

ck1
VDD
M4
N3
M5
ck2
ck1
M3
in
M1
N1
out
ck3
M2
C1
N2

FIG. 7

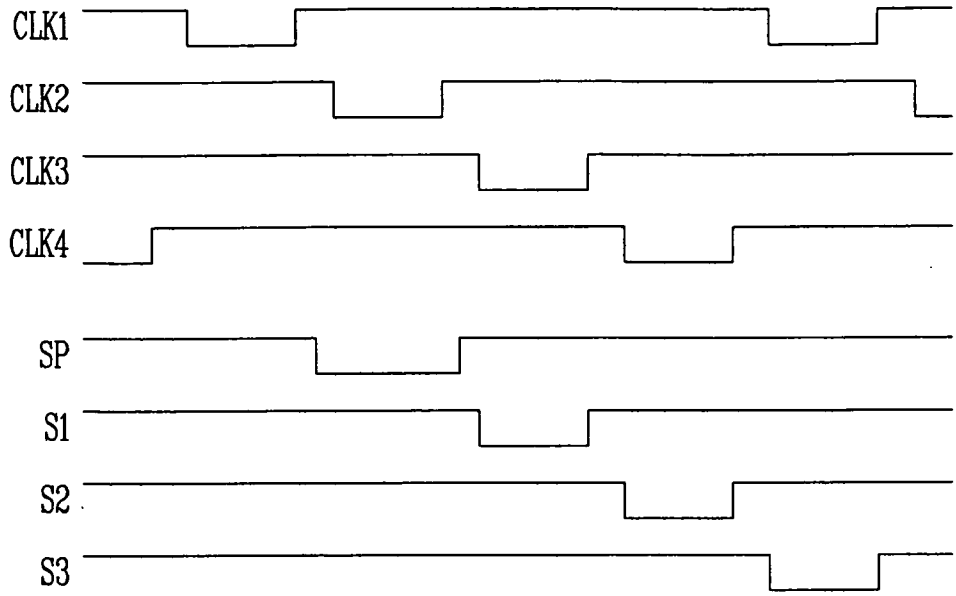

CLK1
CLK2
CLK3
CLK4
SP
S1
S2
S3

FIG. 8

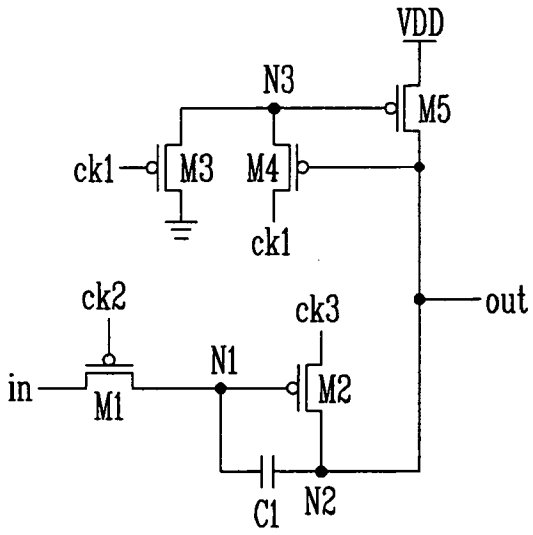

VDD
N3
M5
ck1
M3
M4
ck1
ck2
ck3
out
in
N1
M1
M2
C1
N2

FIG. 9

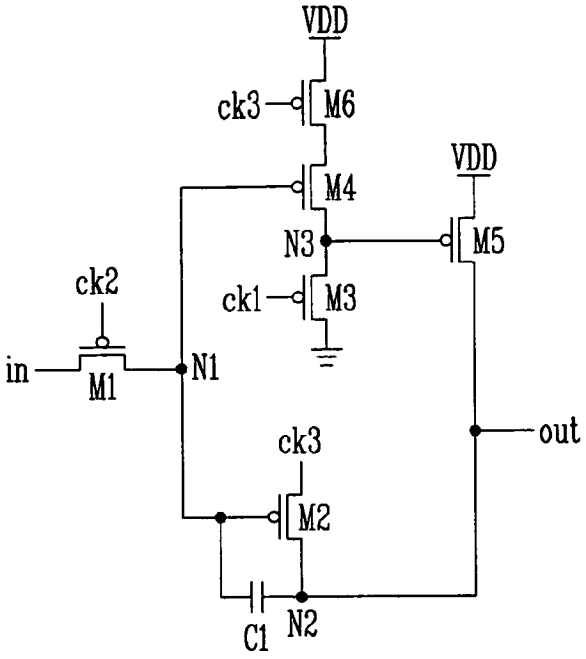

VDD
ck3
M6
VDD
M4
N3
M5
ck2
ck1
M3
in
M1
N1
out
ck3
M2
C1
N2

FIG. 10

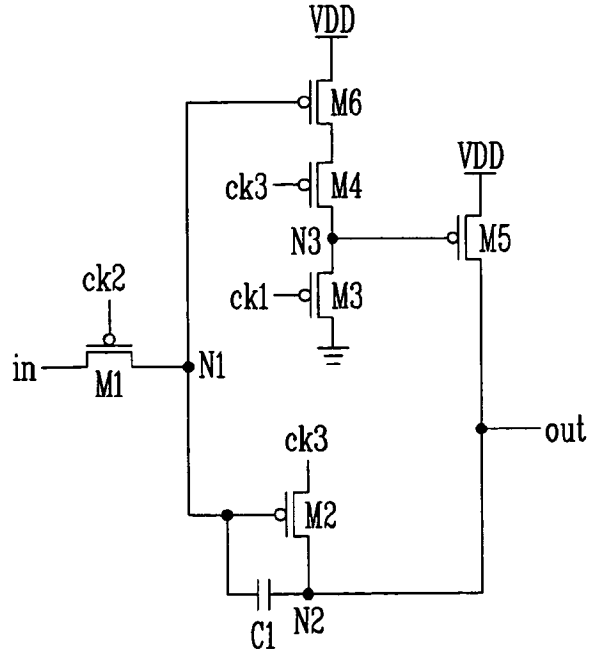

VDD
M6
VDD
ck3
M4
N3
M5
ck2
ck1
M3
in
M1
N1
out
ck3
M2
C1
N2

FIG. 11

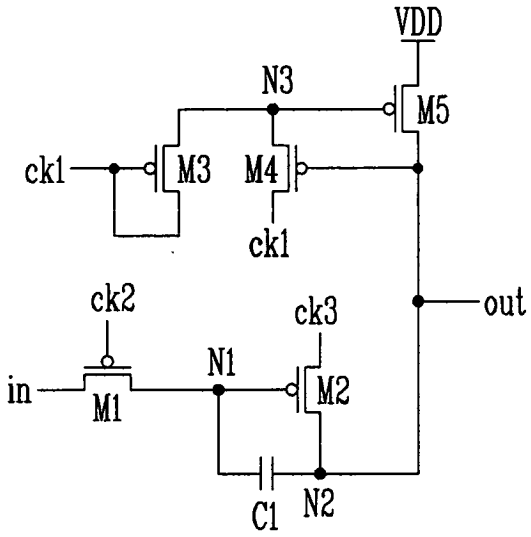

VDD
N3
M5
ck1
M3
M4
ck1
ck2
ck3
out
in
M1
N1
M2
C1
N2

FIG. 12

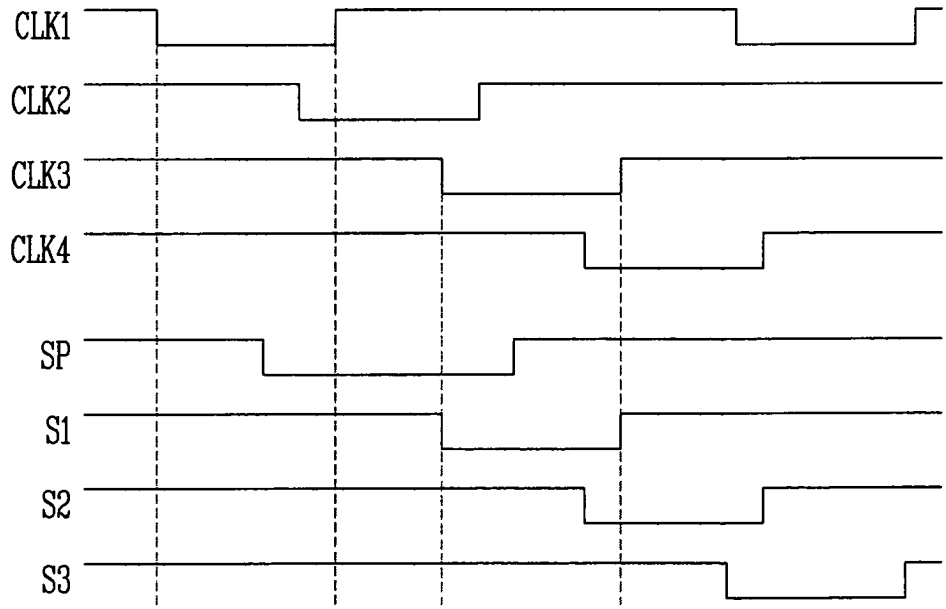

CLK1
CLK2
CLK3
CLK4
SP
S1
S2
S3

FIG. 13

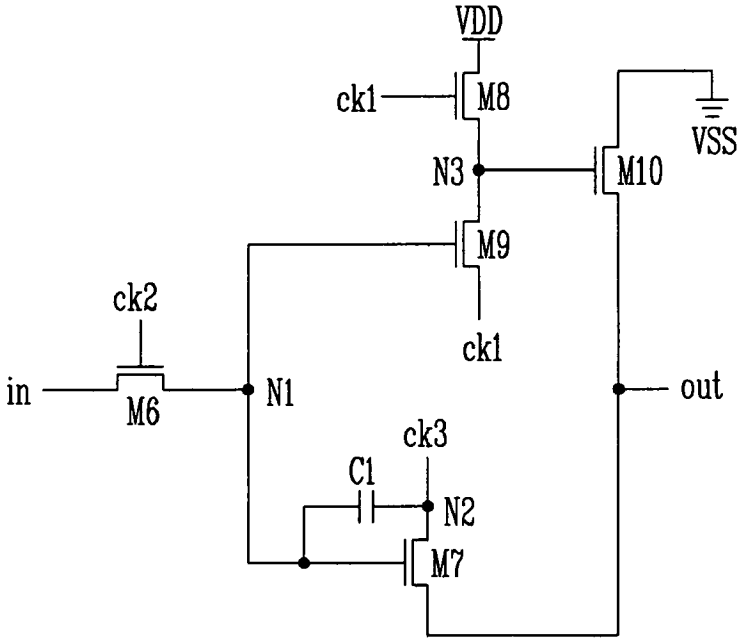
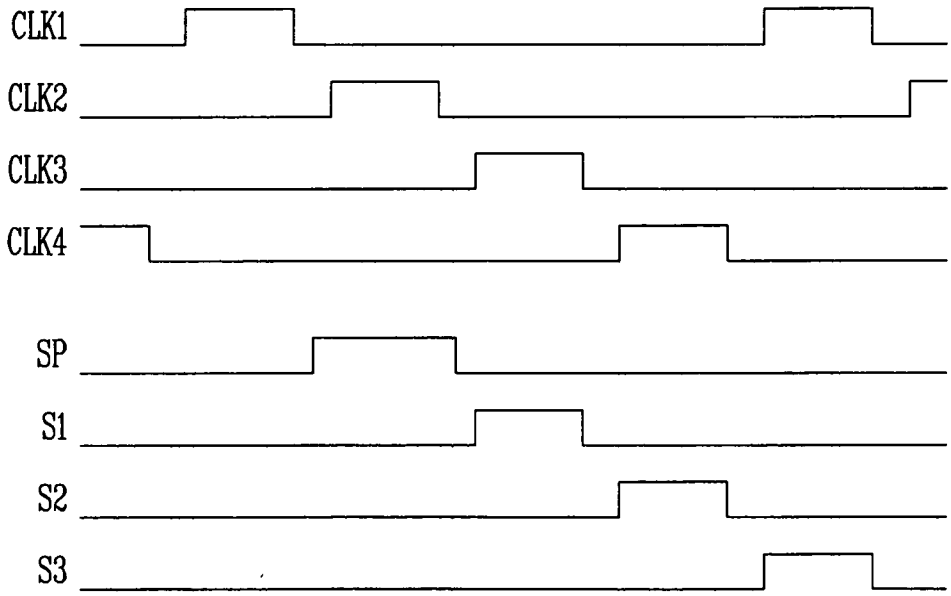

VDD
ck1
M8
VSS
N3
M10
M9
ck2
ck1
in
M6
N1
out
ck3
C1
N2
M7

FIG. 14


CLK1
CLK2
CLK3
CLK4
SP
S1
S2
S3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 07 25 1479

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2004/227718 A1 (PARK JAE-DEOK [KR]) 18 November 2004 (2004-11-18) * paragraphs [0061] - [0080] * * figures 1,6,7 *	1-3, 11-18	INV. G09G3/32 G11C19/18
X	JP 2005 251335 A (CASIO COMPUTER CO LTD) 15 September 2005 (2005-09-15) * abstract * * figures 1-4 *	1-3, 11-18	
X	GB 2 343 068 A (LG PHILIPS LCD CO LTD [KR]) 26 April 2000 (2000-04-26) * page 17, line 5 - page 20, line 10 * * figures 15-17 *	1-3, 11-18	

TECHNICAL FIELDS SEARCHED (IPC)

G11C
G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	22 June 2007	Ladiray, Olivier

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 07 25 1479

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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22-06-2007

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		JP 2000155550 A	06-06-2000

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	扫描驱动电路和使用其的有机发光显示器		
公开(公告)号	EP1847983A1	公开(公告)日	2007-10-24
申请号	EP2007251479	申请日	2007-04-03
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
[标]发明人	SHIN DONG YONG SAMSUNG SDI CO LTD		
发明人	SHIN, DONG YONG, SAMSUNG SDI CO., LTD		
IPC分类号	G09G3/32 G11C19/18		
CPC分类号	G09G3/3266 G09G3/20 G09G3/3208 G09G2310/0286 G09G2330/021 G11C19/184		
优先权	1020060034960 2006-04-18 KR		
其他公开文献	EP1847983B1		
外部链接	Espacenet		

摘要(译)

扫描驱动电路包括多个级。每级接收可以顺序产生的四个时钟信号中的三个，通过输入端子接收和延迟输入信号，并通过输出端子输出输出信号。每级的输入端连接到前一级的输出端。每个级包括晶体管，开关部分和存储部分。晶体管根据第二时钟信号关断/接通输入端子的连接。开关部分根据第一时钟信号将第一电压传送到输出端子，并根据输入信号防止第一电压传送到输出端子。存储部分将输出端子的电压保持预定时间，并根据输入信号将第三时钟信号的电压传送到输出端子。

FIG. 5