

(19)



(11)

EP 1 675 195 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
10.03.2010 Bulletin 2010/10

(51) Int Cl.:
H01L 51/05^(2006.01) H01L 27/00^(2006.01)

(43) Date of publication A2:
28.06.2006 Bulletin 2006/26

(21) Application number: **05108029.9**

(22) Date of filing: **01.09.2005**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK YU

(72) Inventors:
• **KIM, Bo-Sung**
Seoul (KR)
• **RYU, Min-Seong**
Suwon-si, Gyeonggi-do (KR)
• **HONG, Mun-Pyo**
Seongnam-si, Gyeonggi-do (KR)

(30) Priority: **17.12.2004 KR 2004108171**

(74) Representative: **Modiano, Micaela Nadia et al**
Modiano Josif Pisanty & Staub Ltd
Thierschstrasse 11
80538 München (DE)

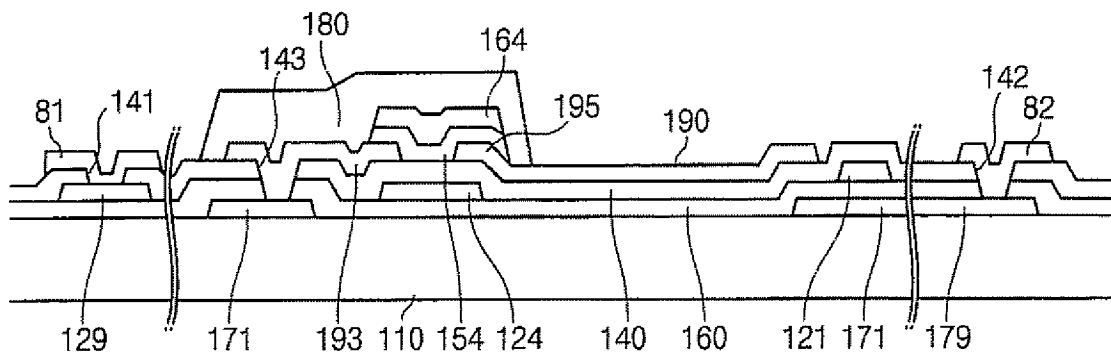
(71) Applicant: **Samsung Electronics Co., Ltd.**
Suwon-si, Gyeonggi-Do (KR)

(54) **Organic thin film transistor for an OLED display**

(57) A method of manufacturing a thin film transistor array panel is provided, the method includes: a substrate; a data line disposed on the substrate; an interlayer insulating layer disposed on the data line; a gate line disposed on the interlayer insulating layer and including a gate electrode; a gate insulating layer disposed on the gate line and the interlayer insulating layer, the gate insulating layer and the interlayer insulating film having a contact

hole exposing the data line; a first electrode disposed on the gate insulating layer and connected to the data line through the contact hole; a second electrode disposed opposite the first electrode with respect to the gate electrode; an organic semiconductor disposed on the first and the second electrodes and contacting the first and the second electrodes; and a passivation member disposed on the organic semiconductor.

Fig. 2



EP 1 675 195 A3



EUROPEAN SEARCH REPORT

 Application Number
 EP 05 10 8029

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2004/023447 A1 (HIRAKATA YOSHIHARU [JP] ET AL) 5 February 2004 (2004-02-05)	1,8,9	INV. H01L51/05 H01L27/00
Y	* paragraphs [0094] - [0116]; figures 9,14 *	2-7, 10-12	
Y	----- US 6 060 333 A (TANAKA TOSHIHIKO [JP] ET AL) 9 May 2000 (2000-05-09) * column 4, line 53 - column 6, line 5 *	2,3,6,7, 11	
Y	----- KYMISSIS IOANNIS ET AL: "Patterning pentacene organic thin film transistors" 1 May 2002 (2002-05-01), JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, AVS / AIP, MELVILLE, NEW YORK, NY, US, PAGE(S) 956 - 959 , XP012009376 ISSN: 1071-1023 * the whole document *	4,5,10, 12	
A	----- WO 2004/001855 A (CANON KK [JP]; UNNO AKIRA [JP]) 31 December 2003 (2003-12-31) * page 44, line 16 - page 45, line 8; figure 5 *	5,12	
A	----- DIMITRAKOPOULOS C D ET AL: "ORGANIC THIN-FILM TRANSISTORS: A REVIEW OF RECENT ADVANCES" IBM JOURNAL OF RESEARCH AND DEVELOPMENT, INTERNATIONAL BUSINESS MACHINES CORPORATION, NEW YORK, NY, US, vol. 45, no. 1, 1 January 2001 (2001-01-01), pages 11-27, XP001150345 ISSN: 0018-8646 * the whole document *	1,8,9	
A	----- US 5 705 826 A (ARATANI SUKEKAZU [JP] ET AL) 6 January 1998 (1998-01-06) * column 8, line 44 - column 9, line 8 *	6-8	TECHNICAL FIELDS SEARCHED (IPC) H01L
2 The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 1 February 2010	Examiner Persat, Nathalie
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

EPO FORM 1503 03.02 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 05 10 8029

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

01-02-2010

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004023447 A1	05-02-2004	NONE	
US 6060333 A	09-05-2000	US 6060338 A	09-05-2000
WO 2004001855 A	31-12-2003	AU 2003243002 A1	06-01-2004
		CN 1669154 A	14-09-2005
		EP 1532688 A1	25-05-2005
		JP 4136482 B2	20-08-2008
		JP 2004023021 A	22-01-2004
		US 2005247928 A1	10-11-2005
US 5705826 A	06-01-1998	JP 3246189 B2	15-01-2002
		JP 8018125 A	19-01-1996

专利名称(译)	用于OLED显示器的有机薄膜晶体管		
公开(公告)号	EP1675195A3	公开(公告)日	2010-03-10
申请号	EP2005108029	申请日	2005-09-01
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
当前申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
[标]发明人	KIM BO SUNG RYU MIN SEONG HONG MUN PYO		
发明人	KIM, BO-SUNG RYU, MIN-SEONG HONG, MUN-PYO		
IPC分类号	H01L51/05 H01L27/00		
CPC分类号	H01L27/283 H01L27/3244		
优先权	1020040108171 2004-12-17 KR		
其他公开文献	EP1675195A2		
外部链接	Espacenet		

摘要(译)

提供一种制造薄膜晶体管阵列面板的方法，该方法包括：基板；数据线设置在基板上；层间绝缘层设置在数据线上；栅极线，设置在层间绝缘层上并包括栅电极；栅极绝缘层设置在栅极线和层间绝缘层上，栅极绝缘层和层间绝缘膜具有暴露数据线的接触孔；第一电极，设置在栅极绝缘层上，并通过接触孔连接到数据线；第二电极相对于栅电极与第一电极相对设置；有机半导体，设置在第一和第二电极上并与第一和第二电极接触；钝化构件设置在有机半导体上。

Fig. 2

