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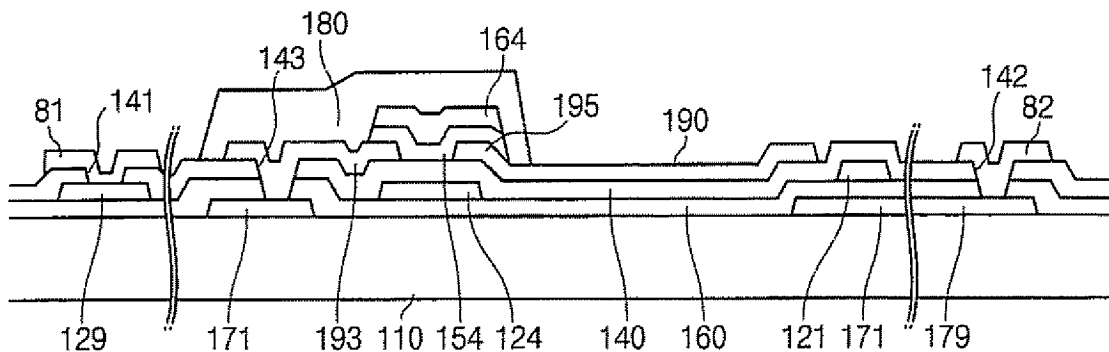
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(54) **Organic thin film transistor for an OLED display**

(57) A method of manufacturing a thin film transistor array panel is provided, the method includes: a substrate; a data line disposed on the substrate; an interlayer insulating layer disposed on the data line; a gate line disposed on the interlayer insulating layer and including a gate electrode; a gate insulating layer disposed on the gate line and the interlayer insulating layer, the gate insulating layer and the interlayer insulating film having a contact

hole exposing the data line; a first electrode disposed on the gate insulating layer and connected to the data line through the contact hole; a second electrode disposed opposite the first electrode with respect to the gate electrode; an organic semiconductor disposed on the first and the second electrodes and contacting the first and the second electrodes; and a passivation member disposed on the organic semiconductor.

Fig. 2



Description**BACKGROUND OF THE INVENTION****(a) Field of the Invention**

[0001] The present invention relates to an organic thin film transistor array panel and a manufacturing method thereof.

(b) Description of Related Art

[0002] Electric field effect transistors including organic semiconductors have been vigorously researched as driving devices for next generation display devices.

[0003] Organic semiconductors may be classified into low molecule compounds such as oligothiophene, pentacene, phthalocyanine, and C₆O; and high molecule compounds such as polythiophene and polythienylenevinylene.

[0004] The low molecule semiconductors have a high mobility in a range of about 0.05-1.5msV, and superior on/off current ratios. However, conventional processes for manufacturing organic thin film transistors (TFTs), including low molecule semiconductor compounds, can be complicated in that they require a low molecule semiconductor pattern be formed by using a shadow mask and vacuum deposition in order to avoid solvent-induced, in-plane expansion caused by organic solvents.

[0005] On the contrary, the organic thin film transistors based on the high molecular weight semiconductor materials show rather a low mobility in a range of about 0.001 - 0.1 cm²/Vs even though they have a merit for mass production due to their solution processibility, such as coating and inkjet printing process.

[0006] In addition, the organic semiconductor has a tendency to change its characteristics or to be damaged due to subsequent processing, thereby deteriorating the characteristics of organic TFTs.

SUMMARY OF THE INVENTION

[0007] A method of manufacturing a thin film transistor array panel is provided, the method includes: a substrate; a data line disposed on the substrate; an interlayer insulating layer disposed on the data line; a gate line disposed on the interlayer insulating layer and including a gate electrode; a gate insulating layer disposed on the gate line and the interlayer insulating layer, the gate insulating layer and the interlayer insulating film having a contact hole exposing the data line; a first electrode disposed on the gate insulating layer and connected to the data line through the contact hole; a second electrode disposed opposite the first electrode with respect to the gate electrode; an organic semiconductor disposed on the first and the second electrodes and contacting the first and the second electrodes; and a passivation member disposed on the organic semiconductor.

[0008] The first and the second electrodes may include indium tin oxide (ITO) and the second electrode may include a pixel electrode.

5 [0009] The organic thin film transistor array panel may further include an insulator disposed between the organic semiconductor and the passivation member. The insulator may include hydrocarbon based polymer including fluorine or parylene.

10 [0010] The interlayer insulating film may include silicon nitride (SiNx), polyacryl, polyimide, or benzocyclobutene

[0011] The gate insulating layer may include at least one selected from the group consisting of silicon dioxide, silicon nitride, maleimide-styrene, polyvinylphenol (PVP), and modified cyanoethyl pullulan (m-CEP).

15 [0012] The organic semiconductor may include at least one selected from the group consisting of: tetracene, pentacene, and derivatives thereof with substituent; oligothiophene including four to eight thiophenes connected at the positions 2, 5 of thiophene rings; perylenetetracarboxylic dianhydride (PTCDA), naphthalenetetracarboxylic dianhydride (NTCDA), and imide derivatives thereof; metallized phthalocyanine and halogenated derivatives thereof; co-oligomer and co-polymer of thienylene and vinylene; regioregular polythiophene; 20 perylene, coronene, and derivatives thereof with substituent; and aromatic and heteroaromatic ring of the above-described materials with at least one hydrocarbon chain having one to thirty carbon atoms.

25 [0013] A method for manufacturing an organic thin film transistor array panel is provided, which includes: forming a data line on a substrate; forming an interlayer insulating film on the data line; forming a gate line including on the interlayer insulating film; forming a gate insulating layer on the gate line and the interlayer insulating film, the gate insulating layer and the interlayer insulating film having a contact hole exposing the data line; forming first and second electrodes on the gate insulating layer, the first electrode connected to the data line through the contact hole and the second electrode separated from the first electrode; forming an organic semiconductor contacting the first and the second electrodes; and forming a passivation member on the organic semiconductor.

30 [0014] The method may further include: forming an insulator on the organic semiconductor and under the passivation member.

35 [0015] The first and the second electrodes may include ITO.

BRIEF DESCRIPTION OF THE DRAWINGS

40 [0016] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawing in which:

45 Fig. 1 is a layout view of an organic TFT array panel according to an embodiment of the present invention;

50 Fig. 2 is a cross-sectional view of the organic TFT

array panel shown in Fig. 1 taken along the line II-II'; Figs. 3, 5, 7, 9 and 11 are layout views of the organic TFT array panel shown Figs. 1 and 2 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention; Fig. 4 is a cross-sectional view of the TFT array panel shown in Fig. 3 taken along line IV-IV'; Fig. 6 is a cross-sectional view of the TFT array panel shown in Fig. 5 taken along line VI-VI'; Fig. 8 is a cross-sectional view of the TFT array panel shown in Fig. 7 taken along line VIII-VIII'; Fig. 10 is a cross-sectional view of the TFT array panel shown in Fig. 9 taken along line X-X'; Fig. 12 is a cross-sectional view of the TFT array panel shown in Fig. 11 taken along line XII-XII'; Fig. 13 is a layout view of an organic TFT array panel according to another embodiment of the present invention; and Fig. 14 is a cross-sectional view of the organic TFT array panel shown in Fig. 13 taken along line XIV-XIV'.

DETAILED DESCRIPTION OF EMBODIMENTS

[0017] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Like numerals refer to like elements throughout

[0018] In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0019] An organic TFT array panel according to an embodiment of the present invention will be described in detail with reference to Figs. 1 and 2.

[0020] Fig. 1 is a layout view of an organic TFT array panel according to an embodiment of the present invention and Fig. 2 is a cross-sectional view of the organic TFT array panel shown in Fig. 1 taken along the lines II-II'.

[0021] A plurality of data lines 171 are formed on an insulating substrate 110 such as transparent glass, silicone, or plastic.

[0022] The data lines 171 transmit data signals and extend substantially in the longitudinal direction. Each data line 171 includes an end portion 179 having a large area for contact with another layer or an external driving circuit. A data driving circuit (not shown) for generating the data signals may be mounted on a flexible printed circuit (FPC) film (not shown), which may be attached to the substrate 110, directly mounted on the substrate 110,

or integrated onto the substrate 110. The data lines 171 may extend to be connected to a driving circuit that may be integrated on the substrate 110.

[0023] The data lines 171 are preferably made of Al containing metal such as Al and Al alloy, Ag containing metal such as Ag and Ag alloy, Au containing metal such as Au and Au alloy, Cu containing metal such as Cu and Cu alloy, Mo containing metal such as Mo and Mo alloy, Cr, Ta or Ti. However, they may have a multi-layered structure including two conductive films (not shown) having different physical characteristics. One of the two films is preferably made of low resistivity metal including Al containing metal, Ag containing metal, and Cu containing metal for reducing signal delay or voltage drop. The other film is preferably made of material such as Mo containing metal, Cr, Ta, or Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). Good examples of the combination of the two films are a lower Cr film and an upper Al (alloy) film and a lower Al (alloy) film and an upper Mo (alloy) film. However, the data lines 171 may be made of various metals or conductors.

[0024] The data lines 171 have inclined edge profiles, and the inclination angles thereof range about 30-80 degrees.

[0025] An interlayer insulating film 160 is formed on the data lines 171. The interlayer insulating film 160 may be made of inorganic insulator or organic insulator. Examples of the inorganic insulator include silicon nitride (SiN_x) and silicon oxide (SiO_x), Examples of the organic insulator include polyacryl, polyimide, and benzocyclobutene (BCB; C₁₀H₈).

[0026] A plurality of gate lines 121 are formed on the interlayer insulating film 160.

[0027] The gate lines 121 transmit gate signals and extend substantially in a transverse direction. Each gate line 121 includes a plurality of gate electrodes 124 projecting upward and an end portion 129 having a large area for contact with another layer or an external driving circuit. A gate driving circuit (not shown) for generating the gate signals may be mounted on a FPC film (not shown), which may be attached to the substrate 110, directly mounted on the substrate 110, or integrated onto the substrate 110. The gate lines 121 may extend to be connected to a driving circuit that may be integrated on the substrate 110.

[0028] The gate lines 121 are preferably made of Al containing metal, Ag containing metal, Au containing metal, Cu containing metal, Mo containing metal, Cr, Ta, or Ti. However, they may have a multi-layered structure including two conductive films (not shown) having different physical characteristics. One of the two films is preferably made of low resistivity metal including Al containing metal, Ag containing metal, and Cu containing metal for reducing signal delay or voltage drop. The other film is preferably made of material such as Mo containing metal, Cr, Ta or Ti, which has good physical, chemical,

and electrical contact characteristics with other materials such as ITO or IZO. Good examples of the combination of the two films are a lower Cr film and an upper Al (alloy) film and a lower Al (alloy) film and an upper Mo (alloy) film. However, the gate lines 121 may be made of various metals or conductors.

[0029] The lateral sides of the gate lines 121 are inclined relative to a surface of the substrate 110, and the inclination angle thereof ranges about 30-80 degrees.

[0030] A gate insulating layer 140 is formed on the gate lines 121. The interlayer insulating film 160 may be made of inorganic insulator or organic insulator. Examples of the inorganic insulator include silicon nitride and silicon oxide that may have a surface treated with octadecyltrichloro-silane (OTS). Examples of the organic insulator include hydrocarbon based polymer including fluorine and parylene that can be deposited by chemical vapor deposition (CVD) in vacuum. Other examples of the organic insulator include maleimide-styrene, polyvinylphenol (PVP), and modified cyanoethyl pullulan (m-CEP).

[0031] Parylene shows excellent coating uniformity and great thickness varieties ranging from about 1,000 Å to several microns. Furthermore, parylene has very low permittivity to serve as an excellent insulator. Polymerized parylene is insoluble to almost all available organic solvents and has excellent chemical resistance. Since parylene can be deposited at room temperature, it gives no heat stress. Parylene is environment friendly since it is dry processed without solvent. Moreover, parylene requires no additive and thus there is no generated gas. In addition, the process for forming parylene film is simple to realize low manufacturing cost.

[0032] The gate insulating layer 140 has a plurality of contact holes 141 exposing the end portions 129 of the gate lines 121, and the gate insulating layer 140 and the interlayer insulating film 160 have a plurality of contact holes 142 and 143 exposing the end portions 179 of the data lines 171 and portions of the data lines 171, respectively,

[0033] A plurality of source electrodes 193, a plurality of pixel electrodes 190, and a plurality of contact assistants 81 and 82 are formed on the gate insulating layer 140. They are preferably made of ITO, particularly amorphous ITO. However, they may be other transparent conductor such as IZO or reflective conductor such as Ag, Al, or alloys thereof.

[0034] The source electrodes 193 are connected to the data lines 171 through the contact holes 143.

[0035] Each pixel electrode 190 includes a portion 195 disposed opposite a source electrode 193 with respect to a gate electrode 124, which is referred to as a drain electrode hereinafter. The pixel electrodes 190 overlap the gate lines 121 and the data lines 171 to increase the aperture ratio.

[0036] The contact assistants 81 and 82 are connected to the end portions 129 of the gate lines 121 and the end portions 179 of the data lines 171 through the contact holes 181 and 182, respectively. The contact assistants

81 and 82 protect the end portions 129 and 179 and enhance the adhesion between the end portions 129 and 179 and external devices.

[0037] A plurality of organic semiconductor islands 154 are formed on the source electrodes 193, the drain electrode 195, and the gate insulating layer 140. The semiconductor islands 154 are disposed on the gate electrodes 124 and contact the source electrodes 193 and the drain electrodes 195.

[0038] The organic semiconductor islands 154 may include a high molecular compound or a low molecular compound, which is soluble in an aqueous solution or organic solvent, and in this case, the organic semiconductor islands 154 can be formed by (inkjet) printing. However, the organic semiconductor islands 154 may be formed by deposition including spin coating and by lithography with or without etch and in this case, the partition 160 can be omitted.

[0039] The organic semiconductor islands 154 may be made of, or from derivatives of, tetracene or pentacene with substituent. Alternatively, the organic semiconductor islands 154 may be made of oligothiophene including four to eight thiophenes connected at the positions 2, 5 of thiophene rings.

[0040] The organic semiconductor islands 154 may be made of perylenetetracarboxylic dianhydride (PTCDA), naphthalene tetracarboxylic dianhydride (NTCDA), or their imide derivatives.

[0041] The organic semiconductor islands 154 may be made of metallized phthalocyanine or halogenated derivatives thereof. The metallized phthalocyanine may include Cu, Co, Zn, etc.

[0042] The organic semiconductor islands 154 may be made of co-oligomer or co-polymer of thienylene and vinylene. In addition, organic semiconductor islands 154 may be made of regioregular polythiophene.

[0043] The organic semiconductor islands 154 may be made of perylene, coronene or derivatives thereof with substituent.

[0044] The organic semiconductor islands 154 may be made of derivatives of aromatic or heteroaromatic ring of the above-described derivatives with at least one hydrocarbon chain having one to thirty carbon atoms.

[0045] A gate electrode 124, a source electrode 193, and a drain electrode 195 along with an organic semiconductor island 154 form an organic TFT Q having a channel formed in the organic semiconductor island 154 disposed between the source electrode 193 and the drain electrode 195.

[0046] The pixel electrodes 190 receive data voltages from the organic TFT Q and generate electric fields in cooperation with a common electrode (not shown) of an opposing display panel (not shown) supplied with a common voltage, which determine the orientations of liquid crystal molecules (not shown) of a liquid crystal layer (not shown) disposed between the two electrodes. A pixel electrode 190 and the common electrode form a capacitor referred to as a "liquid crystal capacitor," which stores

applied voltages after the organic TFT turns off.

[0047] A plurality of stoppers 164 are formed on the organic semiconductor islands 154. The stoppers 164 have substantially the same planar shape as the organic semiconductor islands 154. The stoppers 164 are preferably made of insulating material that can be dry processed and deposited under low temperature. An example of such a material is hydrocarbon based polymer including fluorine or parylene that can be formed at room temperature or low temperature. The stoppers 164 protect the organic semiconductor islands 154 from being damaged in the manufacturing process. The stoppers 164 may be omitted.

[0048] A plurality of passivation members 180 are formed on the organic TFTs Q and the stoppers 164. The passivation members 180 are preferably made of inorganic insulator such as silicon nitride or silicon oxide, organic insulator, or low dielectric insulator. The organic insulator and the low dielectric insulator preferably have dielectric constant less than about 4.0 and the low dielectric insulator includes a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD). The organic insulator for the passivation members 180 may have photosensitivity and the passivation members 180 may have a flat surface.

[0049] The operation of the above-described organic TFT will be described in detail.

[0050] The charge carriers, i.e., holes or electrons in the organic semiconductor islands 154 are uniformly distributed when no voltage is applied to the gate electrode 124 and there is no voltage difference between the source electrode 193 and the drain electrode 195. Upon the application of a voltage between the source electrode 193 and the drain electrode 195, an electrical current is generated in the organic semiconductor island 154 and the amount of the current is in proportion to the applied voltage when the applied voltage is small. Upon the application of a voltage to the gate electrode 124 (referred to as "gate voltage" hereinafter), the charge carriers move in response to an electric field generated by the gate voltage. Depending on the polarity of the gate voltage, the charge carriers move away from or close to the gate electrode 124 to form a depletion layer including no charge carrier or an accumulation layer full of charge carriers in the organic semiconductor island 154 near the gate insulator 140. Accordingly, the current flowing in the organic semiconductor island 154 can be controlled by controlling the magnitude and the polarity of the gate voltage.

[0051] Now, a method of manufacturing the TFT array panel shown in Figs. 1 and 2 according to an embodiment of the present invention will be described in detail with reference to Figs. 3-14 as well as Figs. 1 and 2.

[0052] A method of manufacturing the organic TFT array panel shown in Figs. 1 and 2 according to an embodiment of the present invention will be described with reference to Figs. 3-12 as well as Figs. 1 and 2.

[0053] Figs. 3, 5, 7, 9 and 11 are layout views of the

organic TFT array panel shown Figs. 1 and 2 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention, Fig. 4 is a cross-sectional view of the TFT array panel shown in Fig. 3 taken along line IV-IV', Fig. 6 is a cross-sectional view of the TFT array panel shown in Fig. 5 taken along line VI-VI', Fig. 8 is a cross-sectional view of the TFT array panel shown in Fig. 7 taken along line VIII-VIII', Fig. 10 is a cross-sectional view of the TFT array panel shown in Fig. 9 taken along line X-X', and Fig. 12 is a cross-sectional view of the TFT array panel shown in Fig. 11 taken along line XII-XII'.

[0054] Referring to Figs. 3 and 4, a conductive layer preferably made of Cr and having a thickness of about 2,000 Å is deposited on a substrate 110 and patterned by lithography and etch to form a plurality of data lines 171 including end portions 179.

[0055] Referring to Figs. 5 and 6, an interlayer insulating film 160 preferably made of SiN_x and having a thickness of about 2,000 Å is deposited. Thereafter, a conductive layer, which may include a lower Al-Nd film having a thickness of about 1,500 Å and an upper Mo film of about 300 Å, is deposited on the interlayer insulating film 160 and patterned by lithography and etch to form a plurality of gate lines 121 including gate electrodes 124 and end portions 129.

[0056] Referring to Figs. 7 and 8, a gate insulating layer 140 having a thickness of about 8,000 Å is deposited and the gate insulating layer 140 and the interlayer insulating film 160 are patterned to form a plurality of contact holes 141, 142 and 143 exposing the end portions 129 of the gate lines 121, the end portions 179 of the data lines 171, and portions of the data lines 171, respectively.

[0057] Referring to Figs. 9 and 10, an ITO layer having a thickness of about 400 Å is deposited on the gate insulating layer 140 and patterned by lithography and etch to form a plurality of source electrodes 193, a plurality of pixel electrodes 190 including drain electrodes 195, and a plurality of contact assistants 81 and 82.

[0058] The deposition of the ITO layer may be performed at a room temperature ranging about 20-35°C such that the sputtered ITO layer is an amorphous phase and has uniform film quality from the bottom to the top. The etching of the amorphous ITO layer may be made by wet etching preferably with a Cr etchant containing HNO₃, (NH₄)₂Ce(NO₃)₆, and H₂O, which is used for etching Cr and hardly affect the surface of the gate insulating layer 140 since it includes no hydrochloric acid. Annealing for converting the amorphous ITO into quasi-crystalline amorphous ITO may be added after the ITO layer is etched and the annealing may be performed at a temperature higher than about 180°C for about one to three hours. The quasi-crystalline amorphous ITO may provide excellent contact characteristics with an organic gate insulating layer 140.

[0059] Referring to Figs. 11 and 12, a plurality of organic semiconductor islands 154 preferably made of pentacene and having a thickness of about 800 Å and a plu-

rality of stoppers 164 are formed by molecular beam deposition, vapor deposition, vacuum sublimation, CVD, PECVD, reactive deposition, sputtering, spin coating, contact printing, inkjet printing, etc. with or without shadow mask.

[0060] Finally, an insulating layer having a thickness less than about one micron is deposited and patterned to form a plurality of passivation members 180 as shown in Figs. 1 and 2. The stoppers 164 protect the organic semiconductor islands 154 to prevent the organic semiconductor islands 154 from being damaged during the formation of the passivation members 180.

[0061] As described above, the data lines 171, the gate lines 121, the source electrodes 193, and the pixel electrodes 190 are formed before the organic semiconductor islands 154 are formed. Accordingly, the organic semiconductor islands 154 can avoid the damage caused by the formation of the elements 171, 121, 193 and 190, thereby securing the characteristics of the organic TFTs.

[0062] In addition, since the gate insulating layer 140 is formed after the data lines 171 and the gate lines 121 are formed, the gate insulating layer 140 can avoid the degradation of its surface characteristics that is important to the characteristics of the organic TFTs,

[0063] Now, an organic TFT according to another embodiment of the present invention will be described in detail with reference to Figs. 13 and 14.

[0064] Fig. 13 is a layout view of an organic TFT array panel according to another embodiment of the present invention, and Fig. 14 is a cross-sectional view of the organic TFT array panel shown in Fig. 13 taken along line XIV-XIV'.

[0065] As shown in Figs. 13 and 14, a layered structure of the organic TFT array panel according to this embodiment is almost the same as that shown in Figs. 1 and 2.

[0066] That is, a plurality of data lines 171 including end portions 179 are formed on a substrate 110, and an interlayer insulating film 160 is formed thereon. A plurality of gate lines 121 including gate electrodes 124 and end portions 129 are formed on the interlayer insulating film 160 and a gate insulating layer 140 is formed thereon. The gate insulating layer 140 has a plurality of contact holes 141 and the gate insulating layer 140 and the interlayer insulating film 160 have a plurality of contact holes 142 and 143. A plurality of source electrodes 193, a plurality of pixel electrodes 190, and a plurality of contact assistants 81 and 82 are formed on the gate insulating layer 140 and a plurality of organic semiconductor islands 154, a plurality of stoppers 164, and a plurality of passivation members 164 are sequentially formed thereon.

[0067] Unlike the organic TFT array panel shown in Figs. 1 and 2, a storage electrode line 131 is formed on the interlayer insulating film 160. The storage electrodes 131 are supplied with a predetermined voltage and extend substantially parallel to the gate lines 121. Each storage electrode 131 is disposed between two adjacent gate lines 121 and includes an expansion 137 expanding

upward and downward. However, the storage electrode lines 131 may have various shapes and arrangements.

[0068] The expansions 137 of the storage electrode lines 131 overlap the pixel electrode 190 to form additional capacitors referred to as "storage capacitors," which enhance the voltage storing capacity of the liquid crystal capacitors.

[0069] The data lines 171 are expanded near the contact holes 143 and the drain electrodes 195 project from the pixel electrodes 190.

[0070] Many of the above-described features of the organic TFT array panel and the manufacturing method thereof shown in Figs. 1-12 may be appropriate to the organic TFT array panel shown in Figs. 13 and 14 and the manufacturing method thereof.

[0071] In the above-described embodiments of the present invention, the organic semiconductor islands 154 and the gate insulating layer 140 is minimally exposed to lithography and etch to secure the characteristics of the organic TFTs. In addition, the gate insulating layer 140 contacts the source electrodes 193 and the pixel electrodes 190 preferably made of ITO, the contact characteristics of the gate insulating layer 140 is preserved.

[0072] Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

[0073] Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included for the sole purpose of increasing the intelligibility of the claims and accordingly such reference signs do not have any limiting effect on the scope of each element identified by way of example by such reference signs.

40 Claims

1. An organic thin film transistor array panel comprising:

- a substrate;
- a data line disposed on the substrate;
- an interlayer insulating layer disposed on the data line;
- a gate line disposed on the interlayer insulating layer and including a gate electrode;
- a gate insulating layer disposed on the gate line and the interlayer insulating layer, the gate insulating layer having a contact hole exposing the data line;
- a first electrode disposed on the gate insulating layer and connected to the data line through the contact hole;
- a second electrode disposed opposite the first

- electrode with respect to the gate electrode;
 an organic semiconductor disposed on the first
 and the second electrodes and contacting the
 first and the second electrodes; and
 a passivation member disposed on the organic
 semiconductor.
2. The organic thin film transistor array panel of claim
 1, wherein the first and the second electrodes com-
 prise ITO.
 3. The organic thin film transistor array panel of claim
 2, wherein the second electrode comprises a pixel
 electrode.
 4. The organic thin film transistor array panel of claim
 1, further comprising an insulator disposed between
 the organic semiconductor and the passivation
 member.
 5. The organic thin film transistor array panel of claim
 4, wherein the insulator comprises hydrocarbon
 based polymer including fluorine or parylene.
 6. The organic thin film transistor array panel of claim
 1, wherein the interlayer insulating film comprises
 silicon nitride (SiNx), polyacryl, polyimide, or benzo-
 cyclobutene.
 7. The organic thin film transistor array panel of claim
 1, wherein the gate insulating layer comprises at
 least one selected from the group consisting of sili-
 con dioxide, silicon nitride, maleimide-styrene, pol-
 yvinylphenol (PVP), and modified cyanoethyl pullu-
 lan (m-CEP).
 8. The organic thin film transistor array panel of claim
 1, wherein the organic semiconductor comprises at
 least one selected from the group consisting of:
 - tetracene, pentacene, and derivatives thereof
 with substituent;
 - oligothiophene including four to eight thi-
 ophenes connected at the positions 2, 5 of thi-
 ophene rings;
 - perylene-tetracarboxylic dianhydride (PTCDA),
 naphthalene-tetracarboxylic dianhydride (NTC-
 DA), and imide derivatives thereof;
 - metallized phthalocyanine and halogenated de-
 rivatives thereof;
 - co-oligomer and co-polymer of thienylene and
 vinylene;
 - regioregular polythiophene;
 - perylene, coronene, and derivatives thereof with
 substituent; and
 - aromatic and heteroaromatic ring of the above-
 described materials with at least one hydrocar-
 bon chain having one to thirty carbon atoms.
 9. A method for manufacturing an organic thin film tran-
 sistor array panel, the method comprising:
 - forming a data line on a substrate;
 - forming an interlayer insulating film on the data
 line;
 - forming a gate line including on the interlayer
 insulating film;
 - forming a gate insulating layer on the gate line
 and the interlayer insulating film, the gate insu-
 lating layer and the interlayer insulating film hav-
 ing a contact hole exposing the data line;
 - forming first and second electrodes on the gate
 insulating layer, the first electrode connected to
 the data line through the contact hole and the
 second electrode separated from the first elec-
 trode;
 - forming an organic semiconductor contacting
 the first and the second electrodes; and
 - forming a passivation member on the organic
 semiconductor.
 10. The method of claim 9, further comprising:
 - forming an insulator on the organic semiconduc-
 tor and under the passivation member.
 11. The method of claim 9, wherein the first and the sec-
 ond electrodes comprises ITO,
 12. The method of claim 10, wherein forming an insulator
 on the organic semiconductor and under the passi-
 vation member comprises:
 - forming an insulator comprising hydrocarbon
 based polymer including fluorine or parylene on
 the organic semiconductor and under the pas-
 sivation member.

Fig. 1

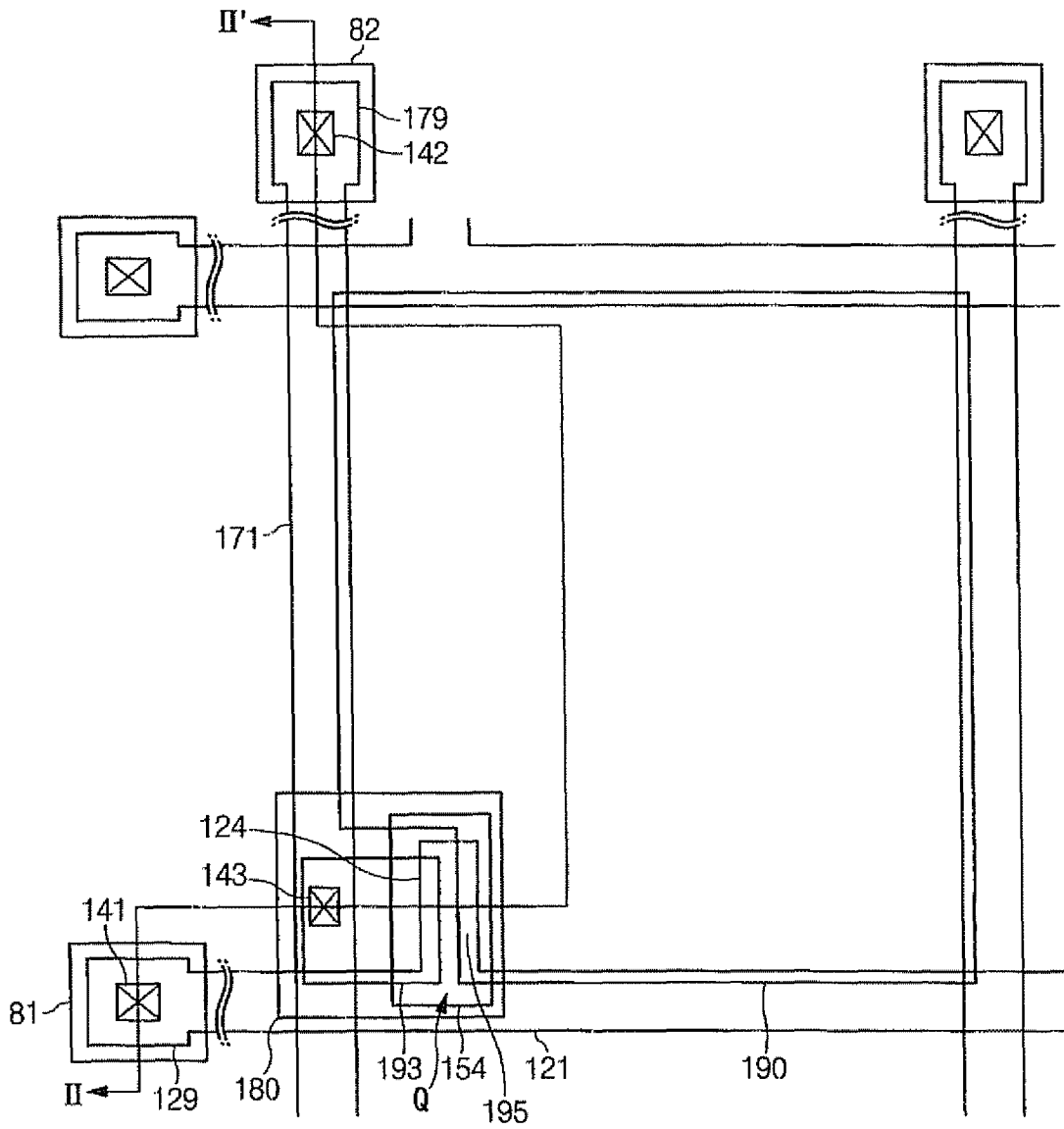


Fig. 2

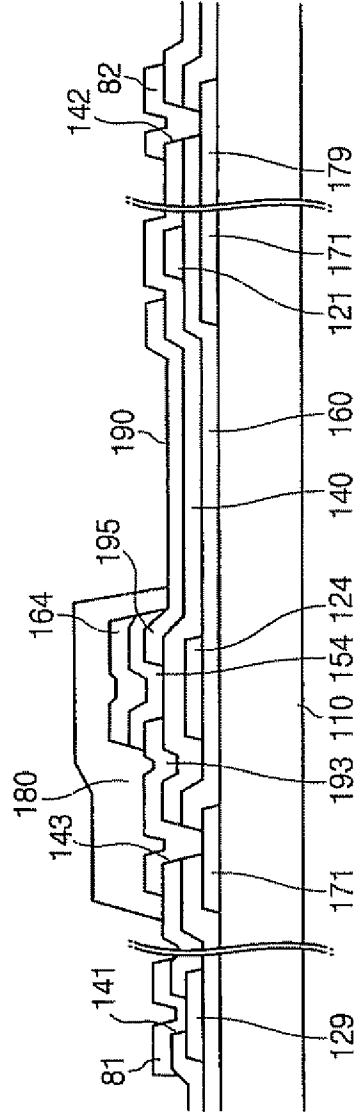


Fig. 3

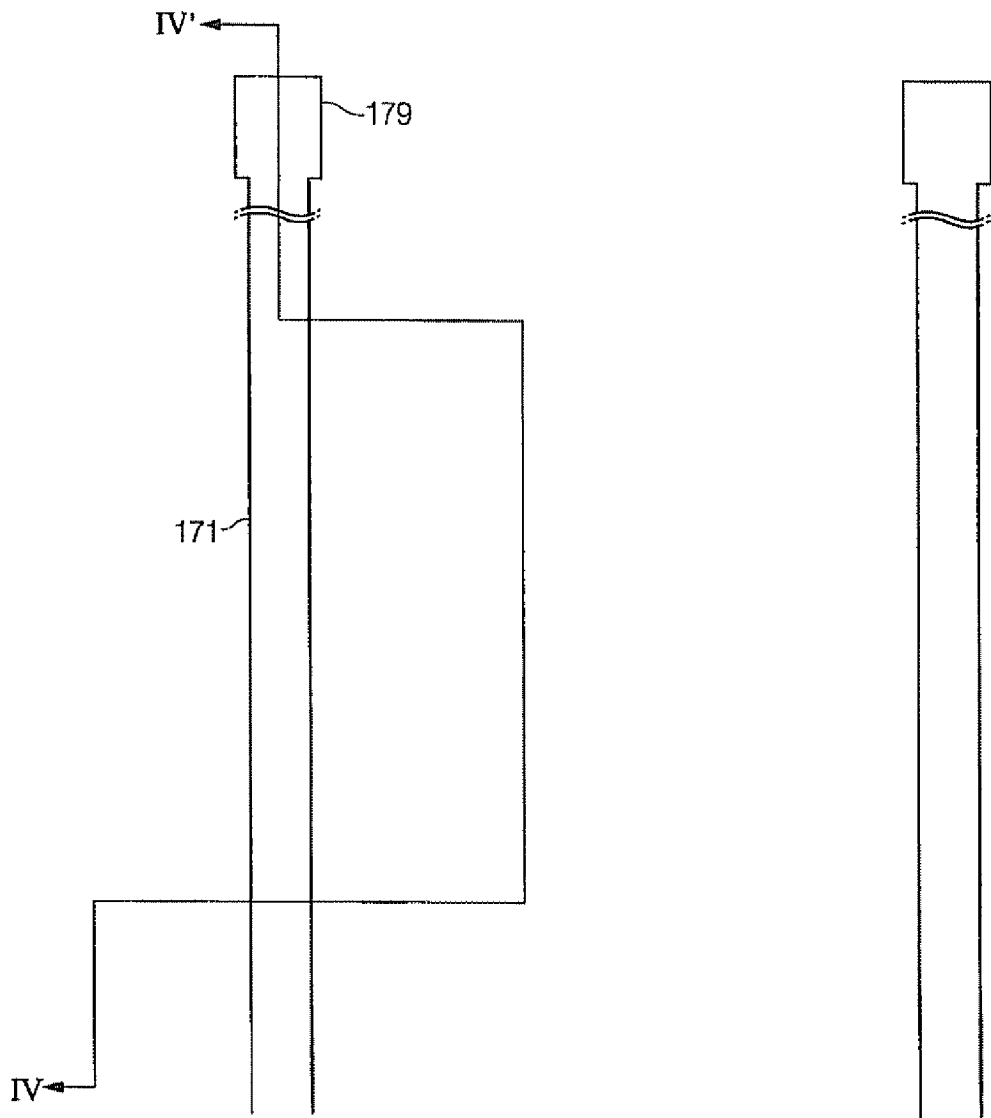


Fig. 4

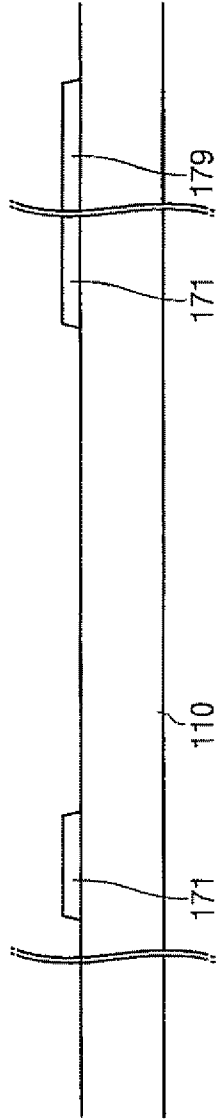


Fig. 5

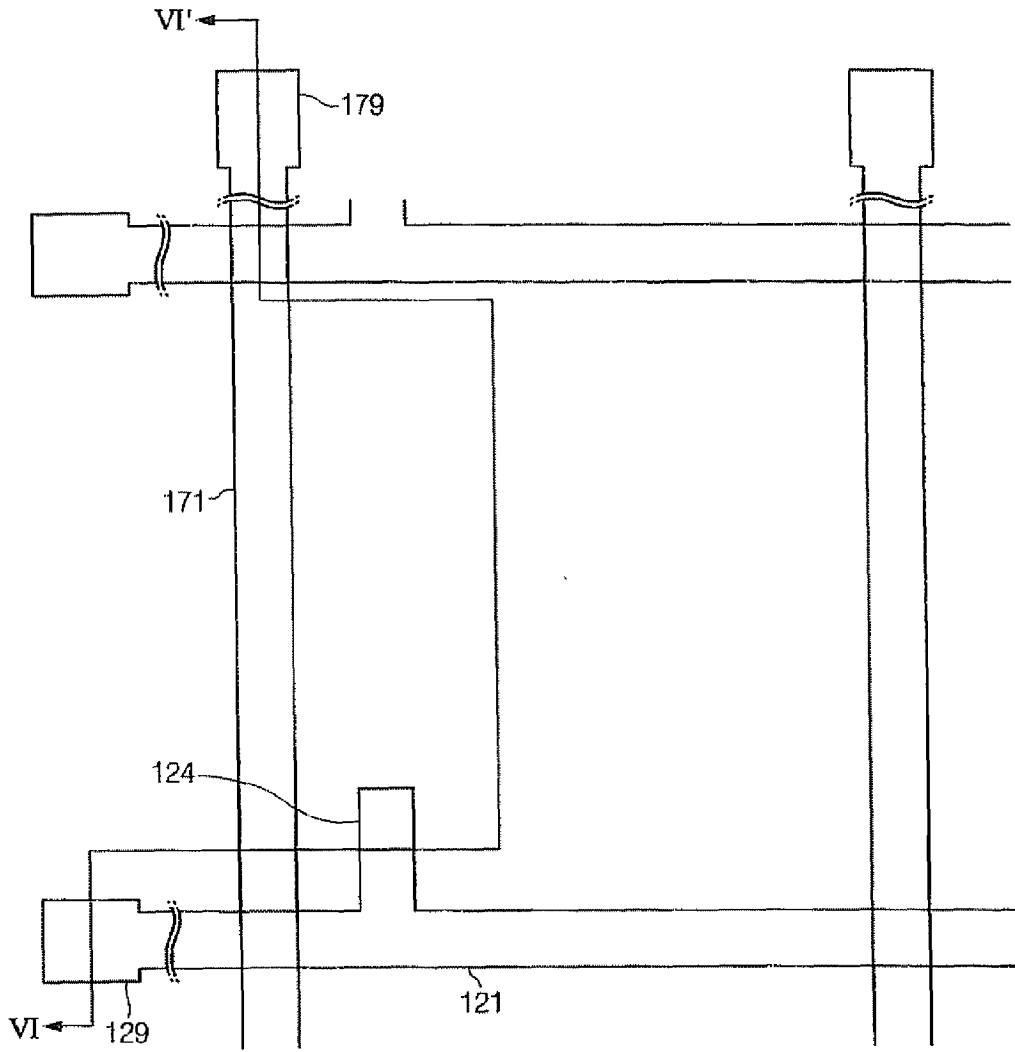


Fig. 6

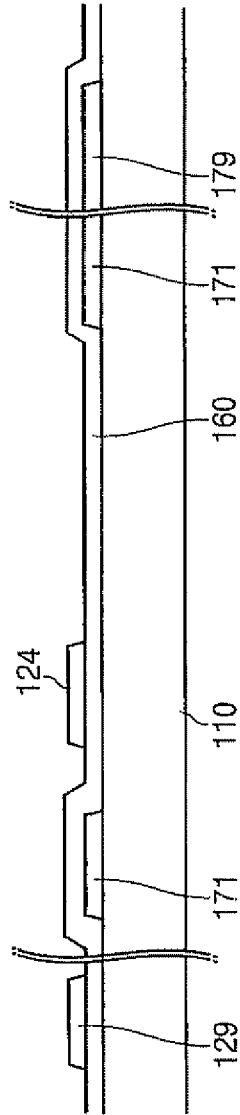


Fig. 7

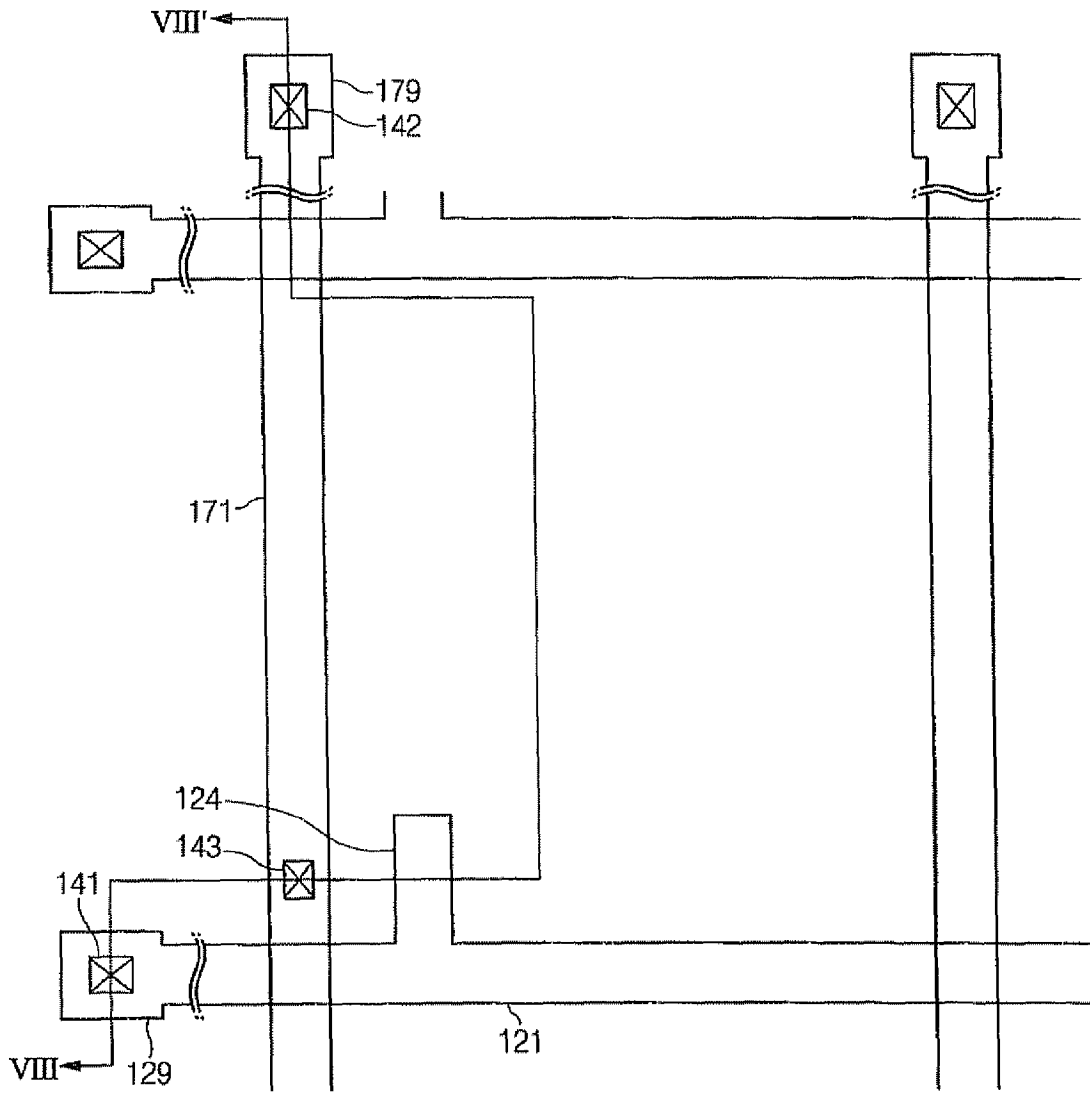


Fig. 8

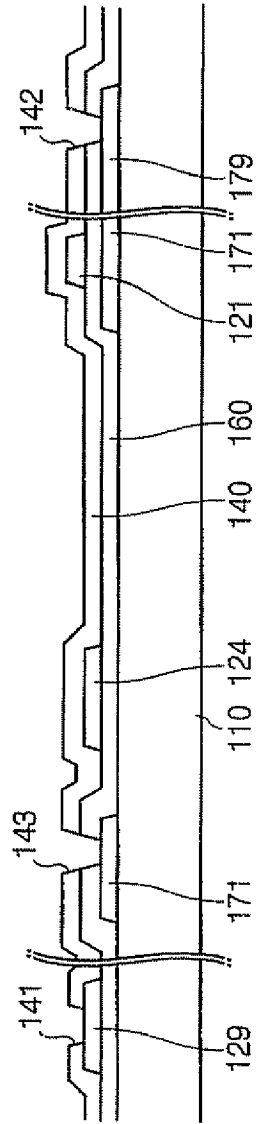


Fig. 9

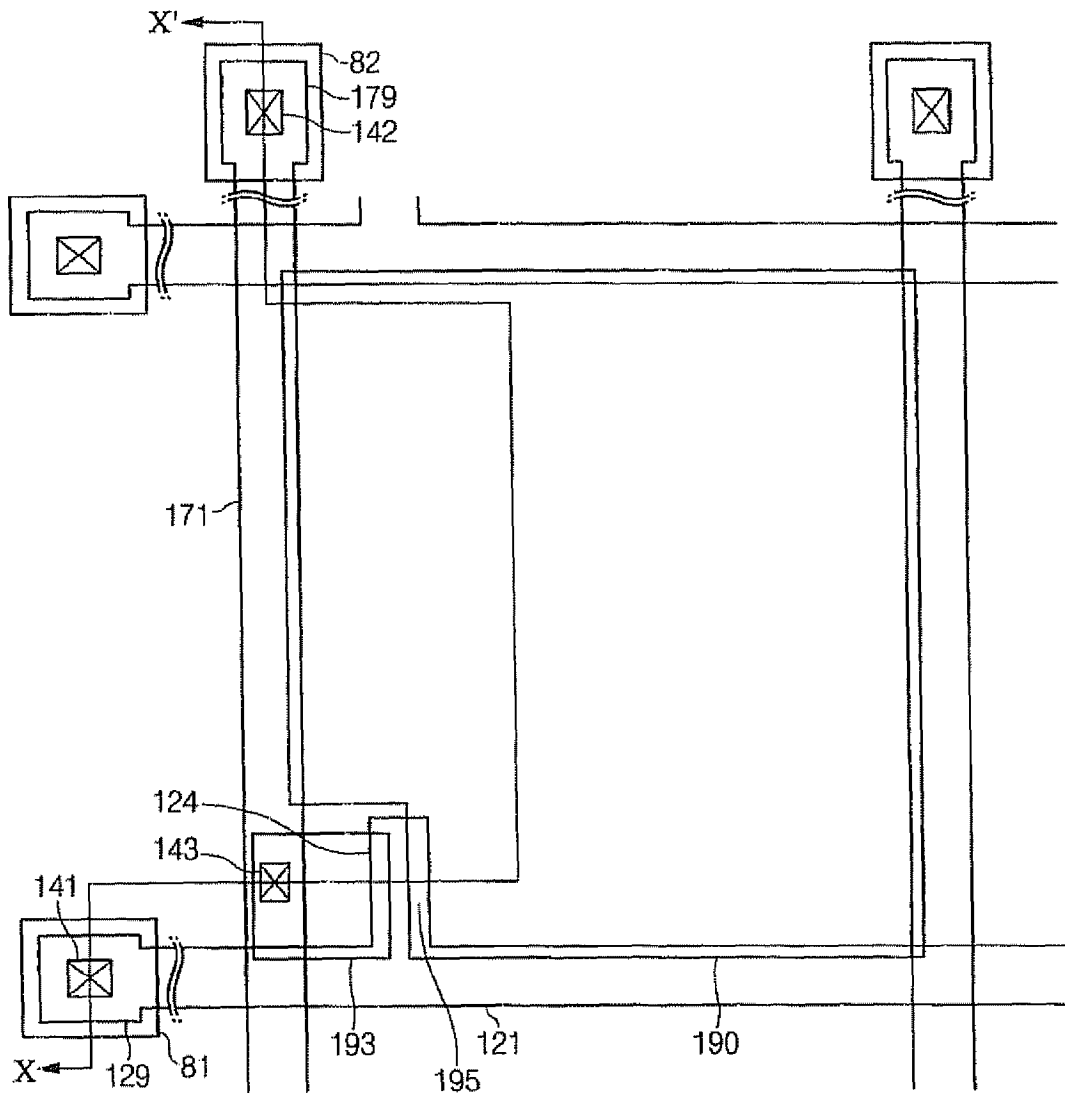


Fig. 10

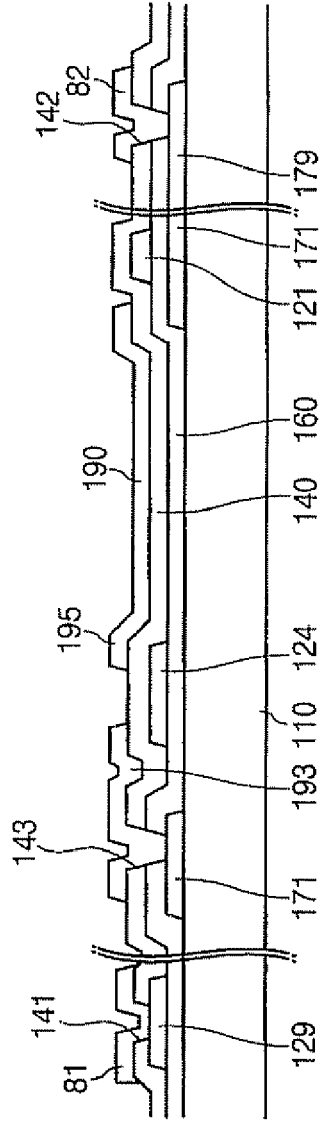


Fig. 11

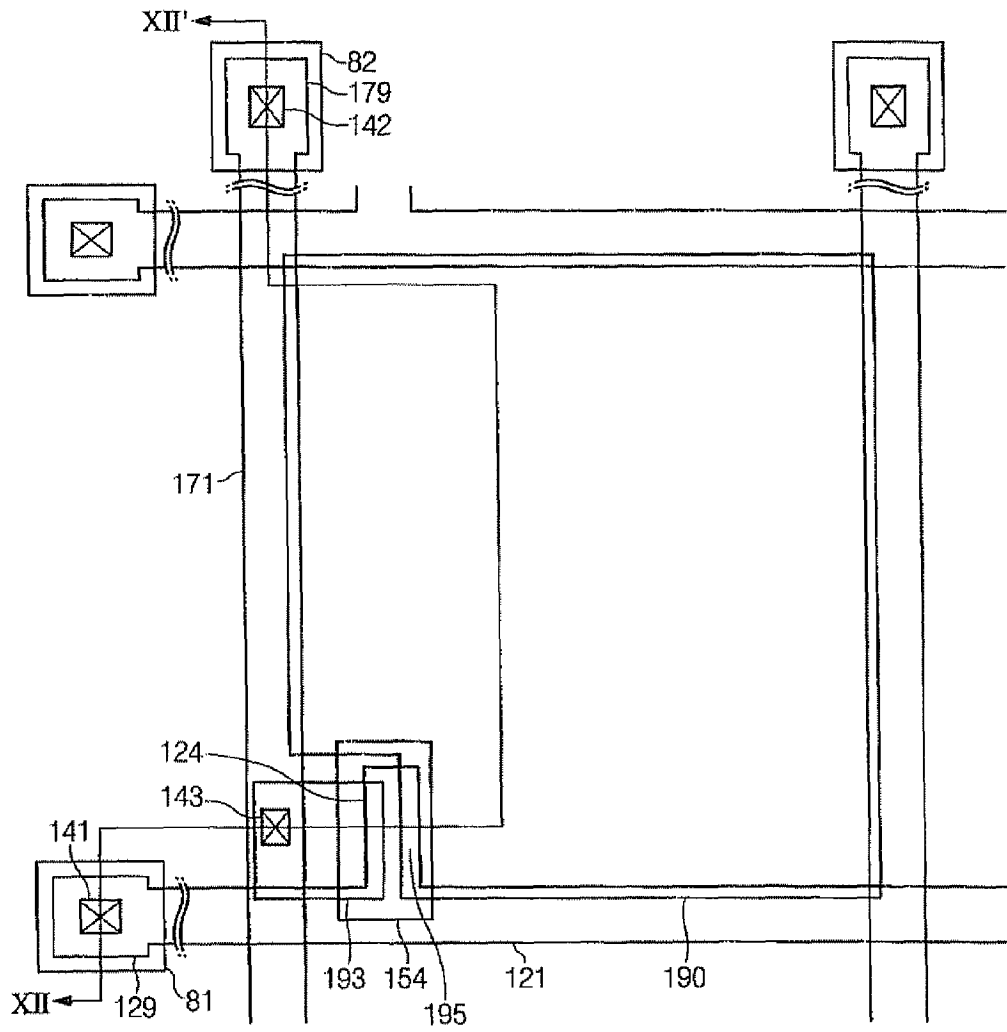


Fig. 12

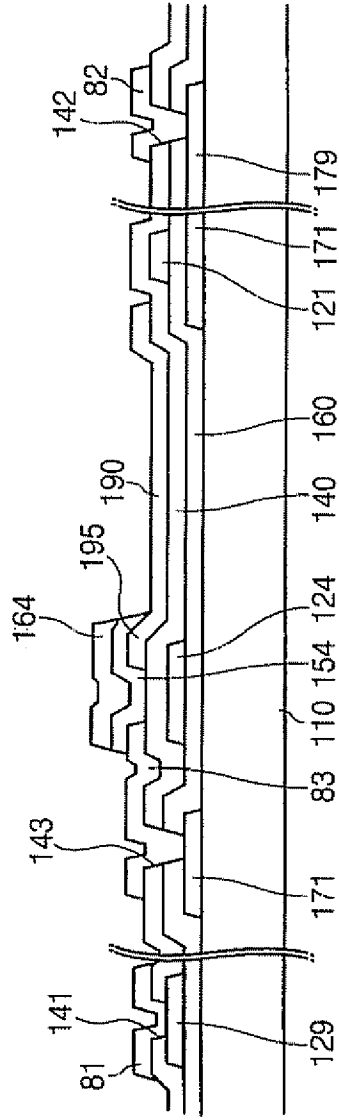


Fig. 13

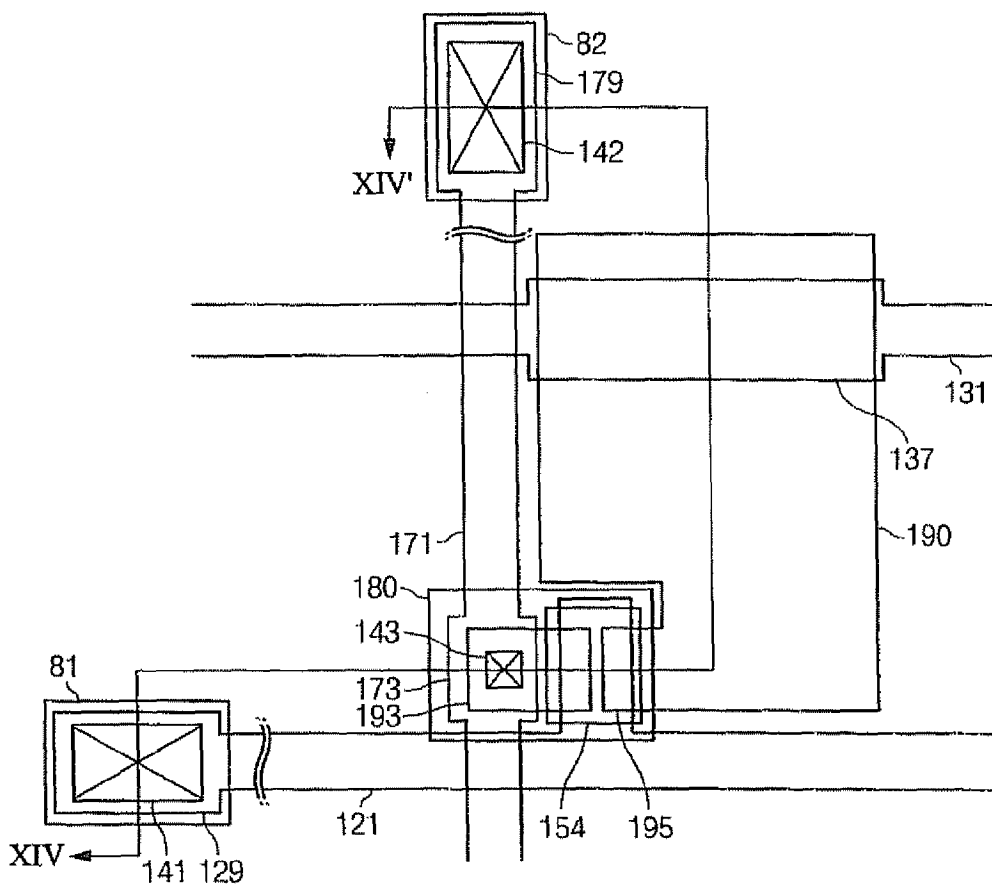
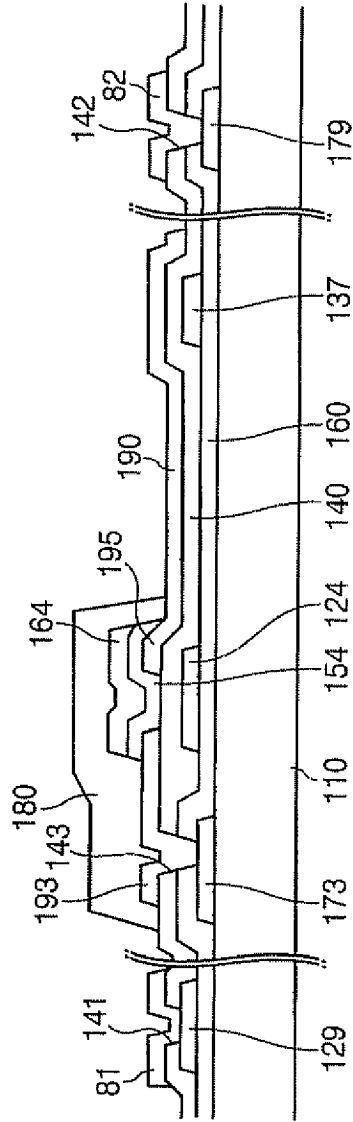


Fig. 14



专利名称(译)	用于OLED显示器的有机薄膜晶体管		
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当前申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
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摘要(译)

提供一种制造薄膜晶体管阵列面板的方法，该方法包括：基板；数据线设置在基板上；层间绝缘层设置在数据线上；栅极线，设置在层间绝缘层上并包括栅电极；栅极绝缘层设置在栅极线和层间绝缘层上，栅极绝缘层和层间绝缘膜具有暴露数据线的接触孔；第一电极，设置在栅极绝缘层上，并通过接触孔连接到数据线；第二电极相对于栅电极与第一电极相对设置；有机半导体，设置在第一和第二电极上并与第一和第二电极接触；钝化构件设置在有机半导体上。

Fig. 2

