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(54) OLED DISPLAY WITH PING PONG CURRENT DRIVING CIRCUIT AND SIMULTANEOUS SCANNING OF LINES

OLED-DISPLAY MIT PINGPONG-STROMANSTEUERSCHALTUNG UND GLEICHZEITIGEM SCANNEN VON LINIEN

SYSTEM D'AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE AVEC CIRCUIT DE COMMANDE DE COURANT EN MODE PING-PONG ET LE BALAYAGE SIMULTANÉE DES LIGNES

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Description

Technical Field

[0001] The present invention relates to a display drive apparatus, a display apparatus and a drive control method thereof, and more particularly to a display drive apparatus which can be applied to a display panel having a plurality of display pixels arranged therein, each display pixel comprising a current controlled type light emitting element which emits a light with a predetermined luminance gradation by supplying a current corresponding to display data thereto, and a display apparatus comprising the display drive apparatus, and a drive control method thereof.

Background Art

[0002] There has been conventionally known a light emitting element type display (a display apparatus) comprising a display panel in which display pixels each comprising a current controlled type light emitting element which emits a light with a predetermined luminance gradation in accordance with a current value of a drive current supplied thereto are two dimensionally arranged like an organic electroluminescence element (which will be referred to as an "organic EL element" hereinafter) or a light emitting diode (LED).

[0003] In particular, a light emitting element type display adopting an active matrix drive mode has a higher display response speed and no field angle dependence and can realize high luminance/high contrast, high definition of a display image quality, a reduction in power consumption and others as compared with a liquid crystal display apparatus (an LCD) which has greatly spread in recent years. Further, the light emitting element type display comprises light emitting element type display pixels and hence does not require a backlight like a liquid crystal display apparatus. Therefore, the light emitting element type display has very excellent characteristics that a further reduction in thickness and weight is possible, and it has been keenly studied and developed as a next-generation display.

[0004] FIG. 18 is a schematic view showing a structural example of a primary part of a light emitting element type display adopting an active matrix drive mode in a prior art.

[0005] FIG. 19 is an equivalent circuit diagram showing a structural example of a display pixel applied to the light emitting type display adopting the active matrix drive mode in the prior art.

[0006] As shown in FIG. 18, the light emitting element type display adopting the active matrix drive mode in the prior art has a structure comprising: a display panel 110P in which a plurality of display pixels EMP are arranged in a matrix form (n rows × m columns). Each display pixel EMP includes e.g., a later-described pixel drive circuit and a current controlled type light emitting element (e.g., an organic EL element) in the vicinity of each of intersections of a plurality of scanning lines SL and a plurality of data lines DL which are arranged to be substantially orthogonal to each other. A scanning driver 120P is connected to the scanning lines SL of the display panel 110P and sets the display pixels EMP in each row in a selected state by sequentially applying a scanning signal Vsel to each scanning line SL at a predetermined timing. A signal driver 200P is connected with the data lines DL of the display panel 110P, and fetches display data and supplies a gradation current Ipix corresponding to the display data to each data line DL at a predetermined timing.

[0007] In such a display, operating states of the scanning driver 120P and the signal driver 200P are controlled by, e.g., a scanning control signal, a data control signal and the like which are generated based on a timing signal supplied from the outside, and a gradation current corresponding to the display data is written in the display pixels in each row set in the selected state by application of the scanning signal. As a result, the respective display pixels emit lights with a predetermined luminance gradation, thereby displaying desired image information.

[0008] In such a light emitting element type display adopting the active matrix drive mode, various kinds of drive control mechanisms or control methods which control light emission of the above-described current controlled type light emitting elements have been proposed. For example, there has been known a display comprising a pixel drive circuit which is constituted of a plurality of switching means which control light emission of the light emitting elements as well as the light emitting elements in accordance with each display pixel constituting the display panel.

[0009] For example, as shown in FIG. 19, such a pixel drive circuit specifically comprises: a pixel drive circuit DP1; and an organic EL element OEL having an anode terminal connected to a drain terminal of a transistor Tr124 of the pixel drive circuit DP1 and a cathode terminal to which a ground potential is applied. The pixel drive circuit DP 1 includes in the vicinity of each intersection of a pair of scanning lines SL1 and SL2 arranged in parallel with each other and a data line DL: a first transistor Tr121 having a gate terminal connected to the scanning line SL1 and a source terminal and a drain terminal connected to the data line DL and a contact point N121; a second transistor Tr122 having a source terminal and a drain terminal connected to the contact point N121 and a contact point N122; a third transistor Tr123 having a gate terminal connected to the contact point N122, a drain terminal connected to the contact point N121, and a source terminal to which a high power supply voltage Vdd is applied; a fourth transistor Tr124 having a gate terminal connected to the contact point N122 and a source terminal to which the high power supply voltage Vdd is applied.

[0010] In this example, in FIG. 19, the first transistor Tr121 comprises an n-channel type field effect thin film transistor, and each of the second to fourth transistors Tr122 to Tr124 comprises a p-channel type field effect

thin film transistor. Furthermore, CP1 represents a parasitic capacitance formed between a gate and a source of the third and fourth transistors Tr123 and Tr124.

[0011] In the pixel drive circuit DP1 having such a configuration, the organic EL element OEL is subjected to a light emission control as follows by turning on/off the four transistors (switching means) comprising the transistors Tr121 to Tr124 at a predetermined timing.

[0012] That is, in the pixel drive circuit DP1, when the display pixel is set in the selected state by respectively applying a high-level scanning signal Vsel1 to the scanning line SL1 and a low-level scanning signal Vsel2 to the scanning line SL2 by the scanning drive 120P, the transistors Tr121, Tr122 and Tr123 are turned on, and the gradation current Ipix corresponding to display data which has been supplied to the data line DL by the signal driver 200P flows through the transistors Tr121 and Tr123. At this moment, since a part between the gate and the drain of the transistor Tr123 is electrically short-circuited by the transistors Tr122 and Tr123 operates in a saturated region. As a result, a current level of the gradation current Ipix is converted into a voltage level by the transistor Tr123, and a predetermined voltage is thereby generated between the gate and the source (a write operation). The transistor Tr124 is turned on in accordance with the voltage generated between the gate and the source of the transistor Tr123, and a predetermined drive current flows to the ground potential from the high power supply voltage Vdd through the transistor Tr124 and the organic EL element OEL, thereby emitting a light from the organic EL element (a light emitting operation).

[0013] Subsequently, when, e.g., the high-level scanning signal Vsel2 is applied to the scanning line SL2, the transistor Tr122 is turned off. As a result, the voltage generated between the gate and the source of the transistor Tr123 is held by the parasitic capacitance CP1. Then, when the low-level scanning signal Vsel1 is applied to the scanning line SL1, the transistor, Tr121 is turned off. As a result, the data line DL and the pixel drive circuit DP1 are electrically shut off. Consequently, the fourth transistor Tr124 continuously maintains the ON state by a potential difference based on the voltage held in the parasitic capacitance CP1, a predetermined drive current flows to the ground potential from the high power supply voltage Vdd through the transistor Tr124 and the organic EL element OEL, and hence the light emitting operation of the organic EL element OEL continues.

[0014] Here, the drive current supplied to the organic EL element OEL through the transistor Tr124 is controlled to have a current value based on a luminance gradation of the display data, and this light emitting operation is controlled to continue for, e.g., one frame period until a gradation current corresponding to the next display data is written in each display pixel.

[0015] The drive control method in the pixel drive circuit having such a circuit configuration supplies a gradation current having a specified current value corresponding to the display data to each display pixel (the gate terminal of the third transistor Tr123), and controls the drive current which is passed to the organic EL element based on a voltage held in accordance with the current value, thereby effecting the light emitting operation with a predetermined luminance gradation. Therefore, this method is called a current application mode (or a current specification mode).

[0016] Like FIG. 19, there has been also known a drive control method adopting a voltage application mode (or a voltage specification mode) which applies a gradation voltage having a specified voltage value corresponding to display data to each display pixel comprising a pixel drive circuit and an organic EL element, and controls a drive current which is passed to the organic EL element OEL in accordance with the voltage value of the gradation voltage, thereby effecting a light emitting operation with a predetermined luminance gradation. In a pixel drive circuit adopting such a voltage specification mode, irregularities or fluctuations (deterioration) are generated in element characteristics (a channel resistance of a transistor and others) of a switch element which has a selection function or a light emission drive function in dependence on an external environment (an ambient temperature and others), a utilization time and the like, a drive current is affected. Thus, the pixel drive circuit has a problem that desired light emission characteristics (display with a predetermined luminance gradation) cannot be stably realized for a long period in time. Alternatively, when each display pixel is finely formed in order to realize the high definition of the display panel, irregularities in operation characteristics (a current between the source and the drain of the transistor and others) of a switch element constituting the pixel drive circuit become large, and hence an appropriate gradation control cannot be performed. Accordingly, the pixel drive circuit has a drawback that generation of irregularities in light emission characteristics of each display pixel results in deterioration of a display image quality.

[0017] On the contrary, the pixel drive circuit adopting the current specification mode comprises a third transistor Tr123 (a current/voltage conversion transistor) which converts a current level of a gradation current corresponding to display data supplied to each display pixel into a voltage level and a fourth transistor Tr124 (a light emission drive transistor) which supplies a drive current having a predetermined current value to the organic EL element OEL. This pixel drive circuit can suppress an influence of irregularities in operation characteristics of the respective transistors Tr123 and Tr124 by setting a current value of a drive current supplied to the organic EL element OEL, and hence has an advantage that the problems of the pixel drive circuit adopting the voltage specification mode can be solved.

[0018] However, the pixel drive circuit adopting the current specification mode has the following problems.

[0019] In case of writing a gradation current based on display data having a lowest luminance or a relatively low luminance in each display pixel (at the time of low-

gradation display), a signal current having a small current value corresponding to a luminance gradation of display data must be supplied to each display pixel.

[0020] Here, since an operation of writing a gradation current in each display pixel corresponds to charging a capacitance component which is parasitic on the data line (a retention capacitance constituting a wiring capacitance and a display pixel) to a predetermined voltage, a wiring length of the data line becomes long due to, e.g., an increase in size of the display panel. Moreover, when the number of display pixels connected to this data line is increased, a time required to charges the data line becomes long as a current value of the gradation current becomes small, i.e., as display is effected with a lower gradation, and hence a time required for a write operation with respect to each display pixel is increased. The write operation with respect to each display pixel cannot be completed in a preset write time, and there occurs a so-called insufficient write state in which a stable state (a saturation state) is not reached. As a result, there is a display pixel which cannot emit a light with an appropriate luminance gradation corresponding to display data, resulting in deterioration in a display image quality.

[0021] Additionally, when the number of scanning lines arranged on the display panel is increased and a selection period (i.e., a write time) of each scanning line is set short in order to realize the high definition of the display panel, the sufficient write operation with respect to each display pixel cannot be performed as a current value of the gradation current is reduced, and the insufficient write state is generated, which leads to deterioration in a display image quality or a restriction in high definition of the display panel.

[0022] US 2003/132931 A1 discloses several modes of driving a display using different semiconductor circuit configurations connected to a source signal line for image signal output and gate signals for controlling the circuit operation. The image signal is input into a display row when the first gate signal of said row is selected. Here, the periods of the first gate signal of two adjacent row do not overlap. The second gate signal coincides with the light emitting period of the light emitting element.

[0023] WO 2004/086347 A, EP-A-0 837 445, and EP-A-1 207 511 relate to driving of a display device supplying gradation signals to the selected rows. At the same time, plurality of rows are selected in accordance with the structure of the display device that connects more rows to a single scanning line. The selection periods of two adjacent rows selected at the same time are fully overlapping. The selection periods of two adjacent rows that are not selected at the same time are not overlapping at all.

[0024] US 2003/001870 A1 relates to a display driving wherein the scanning lines are selected sequentially without overlapping periods between rows. The image data is then supplied as gradation voltage to output lines, in accordance with trigger pulses output to the trigger lines.

[0025] EP 0 911 796 A relates to driving a liquid crystal display. Pre-charging is applied to the pixels before writing the image signal therein. In particular, the signals V1 to V4 in Figure 3 are pre-charged in an initial period which causes the total pixel writing period to double. Thus the respective pulse pairs V1 and V2, V2 and V3, V3 and V4, etc. overlap in a half of their period.

Disclosure of Invention

[0026] In a display drive apparatus which drives display pixels of a display panel based on display data and a display apparatus comprising this display drive apparatus, the present invention has an advantage that occurrence of an insufficient write state in an operation of writing a gradation current in each display pixel can be suppressed and the high definition of the display panel can be excellently realized.

[0027] This is achieved by the features of the independent claims.

Brief Description of Drawings

[0028]

FIG. 1 is a schematic block diagram showing an entire configuration of a display apparatus according to a comparative example;

FIG. 2 is a structural view showing a part of the display apparatus according to the example depicted in FIG. 1;

FIG. 3 is a block diagram showing a structural example of a current generating section which can be applied to the display apparatus according to the example depicted in FIG. 1;

FIG. 4 is a circuit block diagram showing a structural example of a current holding/distributing section which can be applied to the display apparatus according to the example depicted in FIG. 1;

FIGS. 5A and 5B are conceptual views showing a schematic operation of the current holding/distributing section which can be applied to the example depicted in FIG. 1;

FIG. 6 is a timing chart illustrating a drive control operation (a drive control method) in the display apparatus according to the example depicted in FIG. 1;

FIG. 7 is a schematic structural view showing a primary part of another structural example of the display apparatus according to the example depicted in FIG. 1;

FIG. 8 is a schematic structural view showing a primary part of still another example of the display apparatus according to the example depicted in FIG. 1;

FIG. 9 is a structural view showing a part of an embodiment of a display apparatus according to the present invention;

FIG. 10 is a circuit block diagram showing a structural example of a current holding/distributing section which can be applied to the display apparatus ac-

cording to the embodiment depicted in FIG. 9;
FIGS. 11A and 11B are conceptual views showing a schematic operation of the current holding/distributing section which can be applied to the embodiment depicted in FIG. 9;
FIG. 12 is a timing chart showing a drive control method of the display apparatus according to the embodiment depicted in FIG. 9;
FIG. 13 is a schematic structural view showing a primary part of another structural example in the embodiment of the display apparatus according to the present invention;
FIG. 14 is a circuit block diagram showing a concrete circuit example of a display pixel which can be applied to the display apparatus according to the present invention;
FIGS. 15A and 15B are conceptual views showing a drive control operation of a pixel drive circuit according to the embodiment depicted in FIG. 9;
FIG. 16 is a schematic block diagram showing a structural example of the display apparatus to which a display pixel according to the embodiment depicted in FIG. 14 is applied;
FIG. 17 is a schematic block diagram showing still another structural example of the display apparatus to which the display pixel according to the embodiment depicted in FIG. 14 is applied;
FIG. 18 is a schematic view showing a structural example of a primary part of a light emitting element type display adopting an active matrix drive mode in a prior art; and
FIG. 19 is an equivalent circuit diagram showing a structural example of a display pixel applied to the light emitting element type display adopting the active matrix drive mode in the prior art.

Best Mode for Carrying Out the Invention

[0029] A display apparatus and a drive control method thereof according to the present invention will now be described hereinafter based on illustrated embodiments.

Comparative Example of Display Apparatus>

[0030] A schematic configuration of a display apparatus to which a display drive apparatus can be applied will be first described.

[0031] FIG. 1 is a schematic block diagram showing an entire configuration of a display apparatus according to a comparative example.

[0032] FIG. 2 is a structural view showing a primary part of the display apparatus according to this example.

[0033] As shown in FIG. 1, a display apparatus 100 roughly has a display panel 110A, a scanning driver (a selection circuit) 120A, a current generating section (a gradation signal generation circuit) 130, a current holding/distributing section (a current write circuit) 140A, a system controller 150 and a display signal generating section 160.

[0034] As shown in FIG. 2, the display panel 110A substantially has a plurality of display pixels EM which are two-dimensionally arranged (n rows $\times$ m columns) and connected to selection transistors Trsel. A plurality of scanning line groups SGi are arranged in accordance with the display pixels EM in a plurality of rows (two rows in this example) and in which a plurality of (two in this example) scanning lines SLia and SLib (i is a positive integer falling within a range of $1 \leqq i \leqq n'$, e.g., a divisor of the total number n of rows provided in the display panel 110A; n' and n are positive integers) are determined as one set. A plurality of data line groups DGj are arranged in accordance with the display pixels EM in each column corresponding to each scanning line groups SGi and in which a plurality of (two in this example) data lines DLja and DLjb (j is a positive integer falling within a range of $1 \leqq j \leqq m$; m is a positive integer and the total number of pixel columns set in the display panel 110) are determined as one set. Each display pixel EM is provided in the vicinity of each intersection of the scanning lines SLia and SLib constituting each scanning line group SGi and the data lines DLja and DLjb constituting each data line group DGj.

[0035] The scanning driver (the selection circuit) 120A is generally connected with the scanning line groups SGi of the display panel 110A, and sequentially applies a scanning signal Vsel to each scanning line group SGi at a predetermined timing to simultaneously set the display pixels EM corresponding to a plurality of rows (two rows in this example) connected to the scanning line group SGi.

[0036] The current generating section (the gradation signal generation circuit) 130 generally fetches display data corresponding to the display pixels corresponding to a plurality of rows (two rows in this example) of the scanning line group SGi supplied from the later-described display signal generating section 160, and sequentially supplies a signal current (a gradation signal) Ic for the plurality of corresponding rows to the current holding/distributing section 140A in time series.

[0037] The current holding/distributing section (the current write circuit) 140A is generally connected with each data line group DGj of the display panel 110A, distributes the signal current Ic corresponding to a plurality of rows (two rows in this example) sequentially supplied from the current generating section 130 in time series at a predetermined timing and holds this current in accordance with each row, and simultaneously supplies a gradation current Ipix based on the held signal current Ic to the display pixels EM in a plurality of rows (two rows in this embodiment). In this example, the current generating section 130 and the current holding/distributing section 140A constitute a signal driver 200A.

[0038] The system controller 150 generates and outputs a scanning control signal and a data control signal which control operating states of at least the scanning driver 120A, the current generating section 130 and the

current holding/distributing section 140A based on, e.g., a timing signal supplied from the display signal generating section 160.

[0039] The display signal generating section 160 generates display data (e.g., digital data) based on, e.g., a video signal supplied from the outside of the display apparatus 100 and supplies the display data to the current generating section 130, further generates or extracts a timing signal (a system clock or the like) which displays as an image the display data in the display panel 110A and supplies this timing signal to the system controller 150.

[0040] In the configuration shown in FIG. 2, as a structural example, the current holding/distributing section 140A is integrally formed with a pixel array on an insulating substrate BASE on which the plurality of display pixels EM (i.e., the pixel array) constituting the display panel 110A are formed. For example, the signal driver 200A may also have a conformation of a driver chip and be mounted (packaged) on the substrate BASE.

[0041] A concrete configuration of each structure will now be described.

(Display Panel)

[0042] For example, as shown in FIG. 2, the display panel 110A which can be applied to the display apparatus according to this example has a configuration in which each scanning line group SGi corresponding to two rows in which two diverging scanning lines SLia and SLib are determined as one set.and each data line group DGj corresponding to one pixel column in which two data lines DLja and DLjb are determined as one set are arranged to be orthogonal to each other. Each display pixel EM is connected to each intersection of each scanning line SLia and each data line DLja and an intersection of each scanning line SLib and each data line DLjb.

[0043] In this example, in the configuration shown in FIG. 2, the display pixels EM in odd-numbered rows are connected to the scanning line SLia in each scanning line group SGi, and the display pixels EM in even-numbered rows are connected to the scanning line SLib.

[0044] As shown in FIG. 2, as to the number of rows corresponding to the scanning lines constituting each scanning line group SGi, this example is not restricted to the configuration in which each scanning line group SGi corresponds to the display pixels EM for two rows. For example, it is possible to adopt a configuration in which each scanning line group SGi corresponds to the display pixels EM for k rows (k is a divisor of the total number n of rows provided in the display panel 110) and which has n/k sets (that is, n' sets mentioned above) of scanning line groups alternately, there may be used a configuration in which one (single) scanning line group is provided in accordance with rows (n rows) constituting the display panel 110A and all the display pixels EM for one screen are connected with the scanning line group in common, for example. In this case, all the display pixels EM for one screen are altogether set in a selected state by a single scanning signal output from the scanning driver 120A.

[0045] Each display pixel EM has a gate terminal connected with each scanning line SLia or SLib and a source terminal connected with a drain terminal of each selection transistor Trsel connected with each data line DLja or DLjb. Each display pixel EM includes a current controlled type light emitting element which emits a light with a predetermined luminance gradation based on a gradation current Ipix supplied from the current holding/distributing section 140 through each data line DLja or DLjb and the selection transistor Trsel.

[0046] In the display panel 110A having such a configuration, by applying a scanning signal Vsel to a specific scanning line group SGi from the later-described scanning driver 120A, the selection transistors Trsel connected to the plurality of (two) scanning lines SLia and SLib constituting the scanning line group SGi are simultaneously turned on, and the display pixels EM corresponding to the plurality of row (two rows) are altogether set in the selected state. In the state where the scanning signal Vsel is applied to the specific scanning line group SGi (the selected state), by supplying the gradation current Ipix corresponding to display data to each data line group DGj from the later-described current generating section 130 and the current holding/distributing section 140A all at once, the display data is written in the display elements EM corresponding to the plurality of rows (two rows) which are set in the selected state at the same time through the selection transistors Trsel which has been turned on. A concrete circuit example or a circuit operation of the display pixel EM including the selection transistor will be described later in detail.

(Scanning Driver)

[0047] The scanning driver 120A simultaneously sets the display pixels EM corresponding to the plurality of rows (two rows in this embodiment) connected to the scanning lines SLia and SLib constituting each scanning line group SGi in the selected state by executing the operation of sequentially applying the scanning signal Vsel which is in a selection level (e.g., a high level) to each scanning line group SGi based on a scanning control signal supplied from the system controller 150. That is, for example, as shown in FIG. 2, the scanning driver 120A comprises shift blocks SB1, SB2, ... SBi, ... SBn' each including a shift register and a buffer on a plurality of stages (in FIG. 2, n' = n/2; n is the total number of rows provided in the display panel 110A) in accordance with the respective scanning line groups SGi. A shift signal which is output while sequentially shifting from the upper part to the lower part of the display panel 110A by the shift registers is sequentially applied to each scanning line group SGi as the scanning signal Vsel having a predetermined selection level (a high level) through the buffers based on the scanning control signal (a scanning

start signal SST, a scanning clock signal SCK and the like) supplied from the later-described system controller 150.

[0048] As described above, for example, when there is adopted the configuration in which all the display pixels EM constituting the display panel 110A are connected to the single line group SGi, such shift blocks as shown in FIG. 2 are not necessary, and all the display pixels EM for one screen are altogether set in the selected state by applying the single scanning signal Vsel to the scanning line group SGi based on the scanning control signal at a predetermined timing.

(Current Generating Section)

[0049] The current generating section 130 sequentially fetches display data corresponding to the display pixels for the plurality of rows (two rows in this embodiment) in the data line group DGj corresponding to the scanning line group SGi supplied from the later-described display signal generating section 160 based on a data control signal fed from the system controller 150 at a predetermined timing to generate a signal current (a gradation signal) Ic having a current value corresponding to a gradation value of the display data, and sequentially supplies the signal current Ic for the plurality of rows to the current holding/distributing section 140A in accordance with each column in time series. The current generating section 130 sequentially and repeatedly executes this operation for one screen. The concrete configuration and operation of the current generating section 130 will be described later in detail.

(Current Holding/distributing Section)

[0050] The current holding/distributing section 140A sequentially fetches the signal current Ic for the plurality of rows corresponding to each scanning line group SGi supplied from the current generating section 130 in time series based on the data control signal fed from the system controller 150 at a predetermined timing, individually holds the signal current Ic in accordance with the plurality of display pixels EM in each column of each data line group DGj, and simultaneously supplies a gradation current Ipix based on the held signal current Ic to the display pixels EM for the plurality of rows (two rows in this embodiment) of each data line group DGj in accordance with a timing of setting each scanning line group SGi in the selected state by using the above-described scanning driver 120.

[0051] Specifically, for example, as shown in FIG. 2, the current holding/distributing section 140A comprises at least a plurality of current distribution circuits 141 each of which is provided in accordance with each data line group DGj arranged in the display panel 110A, and distributes the signal current Ic supplied from the current generating section 130 in time series in accordance with each of the plurality of (two in this embodiment) data lines DLja and DLjb of each data line group DGi, and a plurality of current holding circuits 142 each of which is provided to be connected with each data line group DGj arranged in the display panel 110A and holds the signal current Ic corresponding to the plurality of (two in this example) data lines distributed by the current distribution circuit 141 in parallel.

[0052] This current holding/distributing section 140A sequentially fetches the signal current Ic for the plurality of rows (two rows in this example) connected with the scanning lines SLia and SLib constituting each scanning line group SGi at a timing based on the data control signal, and distributes and holds the signal current Ic in accordance with each data line in each data line group SGi. The section 140A also generates a gradation current Ipix based on the held signal current Ic, and simultaneously supplies the gradation current Ipix to the display pixels EM for the plurality of rows (two rows in this embodiment) through each data line group DGi at a timing of setting the scanning line group SGi in the selected state. The concrete configuration and operation of the current holding/distributing section 140A will be described later in detail.

(System Controller)

[0053] The system controller 150 allows the scanning driver 120A, the current generating section 130 and the current holding/distributing section 140A to operate at a predetermined timing in order to generate/output the scanning signal Vsel, the signal current Ic and the gradation current Ipix by outputting the scanning control signal and the data control signal which control the operating states to the scanning driver 120A and the current generating section 130 and to the current holding/distributing section 140 through this current generating section 130, writes display data generated by the display signal generating section 160 in each display pixel EM to emit a light therefrom, and controls the display panel 110A to display predetermined image information based on a video signal.

(Display Signal Generating Section)

[0054] The display signal generating section 160 extracts a luminance gradation signal component from, e.g., a video signal supplied from the outside of the display apparatus 100, and supplies the luminance gradation signal component to the current generating section 130 as display data in accordance with each row of the display panel 110A. In this example, when the video signal includes a timing signal component which defines a display timing of image information like a television broadcast signal (a composite video signal), the display signal generating section 160 may have the function of extracting the luminance gradation signal component as well as a function of extracting a timing signal component and supplying it to the system controller 150. In this case,

the system controller 150 generates a scanning control signal and a data control signal which are supplied to the scanning driver 120A, the current generating section 130 or the current holding/distributing section 140 based on a timing signal supplied from the display signal generating section 160.

<Concrete Example of Current Generating Section>

[0055] A concrete structural example of the current generating section which can be applied to the display apparatus according to this example will now be described.

[0056] FIG. 3 is a block diagram showing a structural example of the current generating section which can be applied to the display apparatus according to this example.

[0057] For example, as shown in FIG. 3, the current generating section 130 has includes a shift resister circuit 131, a data resister circuit 132, a data latch circuit 133, a D/A converter 134, and a voltage-current conversing/current supply circuit 135. The shift register circuit 131 outputs a shift signal while sequentially shifting a sampling start signal STR based on a shift clock signal CLK supplied as a data control signal from the system controller 150. The data register circuit 132 sequentially fetches display data D0 to Dm (digital data) for one row supplied from the display signal generating section 160 based on an input timing of the shift signal. The data latch circuit 133 holds the display data D0 to Dm for one row fetched by the data register circuit 132 based on a data latch signal STB. The D/A converter 134 converts the held display data D0 to Dm into a predetermined analog signal voltage (a gradation voltage Vpix) based on gradation reference voltages V0 to Vp supplied from non-illustrated power supplying means. The voltage-current conversion/current supply circuit 135 which generates a signal current (a gradation signal) Ic corresponding to the display data converted into the analog signal voltage, and sequentially supplies to the current holding/distributing section 140A in time series a signal current Ic corresponding to the display pixels EM in each column for the plurality of rows connected to each scanning line group SGi based on an output enable signal OE supplied from the system controller 150 in accordance with each data line group DGj arranged in the display panel 110.

<Concrete Example of Current Holding/distributing Section>

[0058] A concrete example of the current holding/ distributing section which can be applied to the display apparatus according to this example will now be described.

[0059] FIG. 4 is a circuit block diagram showing a structural example of the current holding/distributing section which can be applied to the display apparatus according to this example.

[0060] In this example, just a structural example which can be applied to the display apparatus according to this embodiment is illustrated.

[0061] For example, as shown in FIG. 4, each current distribution circuit (a signal distributing section) 141 constituting the current holding/distributing section 140A comprises a switch transistor Tr41a and a switch transistor Tr41b. In the switch transistor Tr41a, the signal current Ic output from the current generating section 130 is supplied to one end side (a source terminal) of a current path, the other end side (a drain terminal) of the current path is connected with a first output contact point N41a extending to the current holding circuit 142, and a first current fetch signal WTodd supplied as a data control signal from the system controller 150 is applied to a control terminal (a gate terminal). In the switch transistor Tr41b, a signal current Ic output from the current generating section 130 is supplied to one end side (a source terminal) of a current path, the other end side (a drain terminal) of the current path is connected with a second output contact point N41b extending to the current holding circuit 142, and a second current fetch signal WTevn supplied as a data control signal is applied to a control terminal (a gate terminal).

[0062] Each current holding circuit 142 constituting the current holding/distributing section 140A has a configuration in which latch sections (signal holding/ outputting sections) 142a and 142c on two stages which are connected with the data line DLja in parallel in common and to which the signal current Ic output from the current distribution circuit 141 through the first output contact point N41a is supplied in common are provided in parallel with latch sections (signal holding/outputting sections) 142b and 142d on two stages which are connected with the data line DLjb in common and to which the signal current Ic output from the current distribution circuit 141 through the second output contact point N41b is supplied in common.

[0063] For example, as shown in FIG. 4, each latch section 142a (or 142c) comprises: a transistor Tr42a (or Tr42c) which has a current path (a source - a drain) connected between the output contact point N41a and the contact point N42a (or N42c) of the current distribution circuit 141 and has a control terminal (a gate) to which a first latch signal LCup (or a second latch signal LClw) is applied; a transistor Tr43a (or Tr43c) which has a current path connected between the contact point N42a (or N42c) and the contact point N43a (or N43c) and has a control terminal to which a first latch signal LCup (or a second latch signal LClw) is applied; a transistor Tr44a (or Tr44c) in which one end side of a current path is connected with the contact point N42a (or N42c) while a predetermined low-potential voltage (-Vcc) is applied to the other end side of the same and a control terminal is connected with the contact point N43a (or N43c); a transistor Tr45a (or Tr45c) in which one end side of a current path is connected with the contact point N42a (or N42c) while the other end side of the same is connected with the data line DLja and a second latch signal LClw (or a first latch

signal LCup) is applied to a control terminal; and a storage capacitance Ca (or Cc) connected between the contact point N43a (or N43c) and the low-potential voltage (-Vcc).

[0064] For example, as shown in FIG. 4, like the latch sections 142a and 142c, each latch section 142b (or 142d) mentioned above comprises: a transistor Tr42b (or Tr42d) in which a current path (a source - a drain) is connected between the output contact N41b of the current distribution circuit 141 and the contact point N42b (or N42d) and a first latch signal LCup (or a second latch signal LClw) is applied to a control terminal (a gate); a transistor Tr43b (or Tr43c) in which a current path is connected between the contact point N42b (or N42d) and the contact point N43b (or N43d) and a first latch signal LCup (or a second latch signal LClw) is applied to a control terminal; a transistor Tr44b (or Tr44d) in which one end side of a current path is connected with the contact point N42b (or N42d) while a predetermined low-potential voltage (-Vcc) is applied to the other end side of the same, and a control terminal is connected with the contact point N43b (or N43d) ; a transistor Tr45b (or Tr45d) in which one end side of a current path is connected with the contact point N42b (or N42d) while the other end side of the same is connected with the data line DLjb, and a second latch signal LClw (or a first latch signal LCup) is applied to a control terminal; and a storage capacitance Cb (or Cd) connected between the contact point N43b (or N43d) and the low-potential voltage (-Vcc).

[0065] In this example, although the respective transistors Tr41a, Tr41b in the current distribution circuit 141 according to this example and the respective transistors Tr42a to Tr45a, Tr42b to Tr45b, Tr42c to Tr45c and Tr42d to Tr45d in the current holding circuit 142 are not restricted to specific types, it is possible to apply an n-channel type field effect thin film transistor in which an amorphous silicon layer is a channel layer or a field effect thin film transistor in which a polysilicon layer is a channel layer, for example. In this case, as shown in FIG. 2, the current holding/distributing section 140A can be integrally formed with the pixel array on an insulating substrate BASE constituting the display panel 110A. Further, each of the storage capacitances Ca to Cd provided in the respective latch sections 142a to 142d may be a parasitic capacitance formed between the gate and the source of each of the transistors Tr44a to Tr44d or an individually provided capacitance element.

[0066] In the above-described current holding circuit 142, the storage capacitances Ca to Cd constitute the signal holding section and the charges storage circuit, and the transistors Tr44a to Tr44d and Tr45a to Tr45d constitute the gradation current outputting section.

<Operations of Current Holding/distributing Section>

[0067] Operations in the current holding/distributing section having such a configuration will now be described.

[0068] FIGS. 5A and 5B are conceptual views showing general operations of the current holding/distributing section which can be applied to this example.

[0069] In this example, of the latch sections 142a to 142d constituting each current holding circuit 142, the illustration and description will be given as to the side where the latch sections 142 and 142c are provided for the convenience' sake, but the same operations are executed on the side where the latch sections 142b and 142d are provided.

[0070] Operations in the current holding/distributing section 140A (the current distribution circuit 141 and the current holding circuit 142) according to this embodiment has: a current distributing operation of distributing a signal current (a gradation signal) Ic which is supplied from the current generating section 130 in time series and based on display data written in the display pixels for the plurality of rows (two rows in this embodiment) corresponding to the respective scanning lines SLia and SLib constituting the scanning line group SGi to the output contact point N41a side and the output contact point N41b side by the current distribution circuit 141; a current holding operation of fetching and holding the distributed signal current Ic in either the latch sections 142a and 142b or the latch sections 142c and 142d constituting the current holding circuit 142 in synchronization with the current distributing operation; and a current output operation of simultaneously outputting the gradation current Ipix based on the signal current Ic held in the current holding operation to the respective data lines DLja and DLjb constituting the data line group DGj from the other one of the latch sections 142a and 142b and the latch sections 142c and 142d constituting the current holding circuit 142 in synchronization with the current holding operation. The current holding operation and the current output operation are controlled to be alternately repeatedly executed between the latch sections 142a and 142b and the latch sections 142c and 142d constituting the current holding circuit 142 while repeating the current distributing operation in accordance with all the scanning line groups SGi in the display panel 110A.

[0071] That is, in a period where the signal current Ic supplied from the current generating section 130 based on the display data in accordance with each column is fetched and held on one latch section side constituting the current holding circuit 142, the gradation current Ipix is read and output from the other latch section side at the same time. Therefore, the operation of fetching the signal current Ic based on the display data and outputting the gradation current Ipix to the data line group DGj of each column is substantially executed.

[0072] Each of the operations will now be concretely described with reference to each circuit configuration of the current holding/distributing section.

(Current Distributing Operation)

[0073] In the current distributing operation, by selec-

tively setting first and second current fetch signals WTodd and WTevn supplied as data control signals from the system controller 150 to the high level in the current distribution circuit 141, one of the switches Tr41a and Tr41b is sequentially turned on, and the signal current Ic corresponding to the display pixels EM in each row is output from the current generating section 130 in time series in synchronization with the timing of turning on the switch. As a result, the signal current Ic is distributed in accordance with each row and output to the individual latch sections 142a and 142c or 142b and 142d constituting the later-described current holding section 142 through each output contact point N41a or N41b.

(Current Holding Operation/current Output Operation)

[0074] In the current holding circuit 142 (the latch sections 142a to 142d), by selectively setting first and second latch signals LCup and LClw supplied as data control signals from the system controller 150 to the high level, one (the latch sections 142a and 142b or the latch sections 142c and 142d) of the latch sections 142a and 142c connected with the output contact point N41a in parallel and the latch sections 142b and 142d connected with the output contact point N41b in parallel is set in a current holding operation state, and the remaining latch sections (the latch sections 142c and 142d or the latch sections 142a and 142b) are set in a later-described current output operation state.

[0075] In the current holding operation, as shown in FIG. 5A (the latch sections 142a and 142c alone are illustrated for the convenience's sake), the first latch signal LCup is set to the high level, and the second latch signal LClw is set to the low level. As a result, in the latch section 142a connected with the output contact point N41a, the transistors Tr42a, Tr43a and Tr44a are turned on, and the transistor Tr45a is turned off. At this time, since the part between the gate and the drain of the transistor Tr44a is electrically short-circuited by the transistor Tr43a, the transistor Tr44a operates in a saturation region. Consequently, the signal current Ic supplied from the current generating section 130 and output to the output contact point N41a through the switch Tr41a of the current distribution circuit 141 flows to the low-potential voltage (-Vcc) side through the transistors Tr42a and Tr44a of the latch section 142a, and a current level of the signal current Ic is converted into a voltage level between the gate and the source of the transistor Tr44a so that the signal current Ic is stored as the electric charges in the storage capacitance Ca.

[0076] In the current output operation, as shown in FIG. 5B, the first latch signal LCup is set to the low level, and the second latch signal LClw is set to the high level. As a result, the transistors Tr42a and Tr43a are turned off and the transistor Tr45a is turned on in the latch section 142a. At this time, a potential (a high voltage) based on the electric charges (the signal current Ic) stored in the storage capacitance Ca by the current holding operation is held in the contact point N43a, and hence the transistor Tr44a continues the ON operation. Consequently, the data line DLja arranged in the display panel 110 (not shown) is connected with the low-potential voltage (-Vcc) through the transistors Tr45a and Tr44a of the latch section 142a, and the gradation current Ipix flows in such a manner that it is drawn from the data line DLja side (i.e., the display pixel EM side) toward the latch section 142a (the current holding circuit 142).

[0077] Further, in a state where the first latch signal LCup is set to the low level and the second latch signal LClw is set to the high level (i.e., the current output operation state of the latch section 142a mentioned above), the transistors Tr42c and Tr43c are turned on, the part between the gate and the drain of the transistor Tr44c is electrically short-circuited by the transistor Tr43a so that the transistor Tr44c is turned on in the saturation region and the transistor Tr45c is turned off in the latch section 142c connected with the output contact point N41a in parallel. Therefore, the signal current Ic output to the output contact point N41a flows to the low-potential voltage (-Vcc) side through the transistors Tr42c and Tr44c of the latch section 142c, and a current level of the signal current Ic is converted into a voltage level between the gate and the source of the transistor Tr44c so that the signal current Ic is stored as the electric charges in the storage capacitance Cc.

[0078] That is, in a period that one of the latch sections 142a and 142c is set in the current holding operation state, the other one is simultaneously set in the current output operation state. Such an operation state is likewise executed in a combination of the non-illustrated latch sections 142b and 142d.

[0079] The description has been given as to the example where the function (a current polarity reversing section) which generates (converts a current direction) the negative gradation current Ipix corresponding to the signal current Ic with the positive polarity supplied from the current generating section 130 is provided and the gradation current Ipix is drawn from the data line (the display pixels) side in order to cope with the circuit configuration of the later-described pixel drive circuit provided to the display pixel EM in the current holding/distributing section 140A according to this example. However, the present invention is not restricted thereto, and it may have a configuration in which the gradation current Ipix with the positive polarity is generated and the gradation current Ipix is passed to the data line (the display pixels) in accordance with a circuit configuration of the display pixels EM.

[0080] It is to be noted that nearly all known current driver circuits (corresponding to the current generating section) which are distributed and available in the marketplace have a configuration of outputting the gradation signal (the signal current) Ic having the positive polarity, and hence the gradation current whose current direction is converted can be readily generated by known current drivers by applying the current holding/distributing section having the above-described configuration.

<Drive Control Method of Display Apparatus>

[0081] A drive control operation (a drive control method) in the display apparatus having the above-mentioned configuration will now be described.

[0082] FIG. 6 is a timing chart illustrating a drive control operation (a drive control method) in the display apparatus according to this example.

[0083] In this example, the description will be given with reference to each structure of the display apparatus described above.

[0084] In the display apparatus having the above-described structure, display data consisting of digital data which allows each display pixel (a light emitting element) EM constituting the display panel 110A to emit a light with a predetermined luminance gradation is first extracted from a video signal by using the display signal generating section 160, and the extracted display data is sequentially supplied to the current generating section 130 as serial data corresponding to each row of the display panel 110A.

[0085] The display data (the digital data) supplied to the current generating section 130 is converted into a signal current (a gradation signal) Ic corresponding to the display data at a timing based on a data control signal fed from the system controller 150, and output to the current holding/distributing section 140A provided in accordance with the data line group DGj of each column arranged in the display panel 110A.

[0086] In this example, the signal current Ic output from the current generating section 130 is output in time series in units of the data line group DGj corresponding to each column in the display panel 110A in accordance with each row for the respective display pixels EM connected to the respective data lines DLja and DLjb constituting the data line group DGj, for example.

[0087] As shown in FIG. 6, the current distributing operation is executed in the current holding/distributing section 140A. In the current distributing operation, the signal current Ic corresponding to the display pixels EM arranged in the plurality of rows (two rows in this embodiment) in accordance with each column is sequentially fetched, the transistors or switches Tr41a and Tr41b of the current distribution circuit 141 are selectively turned on at the timing based on data control signals (first and second current fetch signals WTodd and WTevn) supplied from the system controller 150, and the signal current Ic is sequentially supplied to the latch section 142a (or 142c) and the latch section 142b (or 142d) of the current holding circuit 142.

[0088] Then, in synchronization with this timing, the latch sections 142a and 142b of the current holding circuit 142 are set in the current holding operation state based on the data control signals (the first latch signal LCup at the high level and the second latch signal LClw at the low level) supplied from the system controller 150. As a result, only in a period that the signal current Ic is supplied to the respective latch sections 142a and 142b, the current holding operation is sequentially executed. In the current holding operation, the electric charges based on the signal current Ic corresponding to the display pixels EM in the respective rows (e.g., the first row and the second row) is stored in the respective storage capacitances Ca and Cb.

[0089] As shown,in FIG. 6, such a current distributing operation and current holding operation are alternately repeated in the latch sections 142a and 142b and the latch sections 142c and 142d with the signal levels of the first and second current fetch signals WTodd and WTevn and the first and second latch signals LCup and LClw being appropriately set. Consequently, the signal current Ic corresponding to the display pixels EM in the two rows based on the display data is sequentially held in each current holding circuit 142.

[0090] Subsequently, after the current holding operation, the latch sections 142a and 142b of the current holding circuit 142 are set in the current output operation state based on the data control signals (the first latch signal LCup at the low level and the second latch signal LClw at the high level) supplied from the system controller 150. As a result, the current output operation is executed in the respective latch sections 142a and 142b. In the current output operation, the gradation current Ipix based on the electric charges stored in the respective storage capacitances Ca and Cb is simultaneously supplied to the display pixels EM in the respective rows (e.g., the first row and the second row) through the respective data lines DLja and DLjb constituting the data line group DGj.

[0091] Therefore, the gradation current Ipix is output from the current holding/distributing section 140A through the data line group DGj of each column, and the scanning signal Vsel at the high level is applied to a specific scanning line group SGi from the scanning driver 120A at the timing based on the scanning control signal supplied from the system controller 150. As a result, all the selection transistors Trsel connected to the respective scanning lines SLia and SLib constituting this scanning line group SGi are turned on, the gradation current Ipix supplied to the display pixels EM in the plurality of rows (e.g., two rows including the first row and the second row) through the data lines DLja and DLjb of each data line group DGj is written in the respective display pixels EM, thereby executing the light emission operation with a predetermined luminance gradation based on the gradation current Ipix.

[0092] Furthermore, in the respective latch sections 142a and 142b, in a period where the current output operation is executed, as shown in FIG. 6, the latch sections 142c and 142d of the current holding circuit 142 are set in the current holding operation state based on the data control signals (the first latch signal LCup at the low level and the second latch signal LClw at the high level) supplied from the system controller 150. As a result, the current holding operation is sequentially executed. In this operation, the signal current Ic for each row continuously supplied from the current generating section 130 is

fetched in the respective latch sections 142c and 142d, and the electric charges based on the signal current Ic corresponding to the display pixels EM in the respective rows (e.g., the third row and the fourth row) are stored in the respective storage capacitances Cc and Cd.

[0093] Then, after the current output operation in the latch sections 142a and 142b, the system controller 150 again sets the first latch signal LCup to the high level and the second latch signal LClw to the low level. As a result, the latch sections 142a and 142b are again set in the current holding operation state. Consequently, the current output operation is executed in the respective latch sections 142a and 142b. In the current output operation, the electric charges based on the signal current Ic corresponding to the display pixels EM in the respective rows (e.g., the fifth row and the sixth row) are stored in the respective capacitances Ca and Cb.

[0094] Moreover, at this time, when the latch sections 142c and 142d of the current holding circuit 142 are set in the current output operation state, there is executed the current output operation in which the gradation current Ipix based on the electric charges stored in the respective storage capacitances Cc and Cd at the foregoing timing is simultaneously supplied to the display pixels EM in respective rows (e.g., the third row and the fourth row) through the respective data lines DLja and DLjb constituting the data line group DGj.

[0095] As a result, in the latch sections 142a and 142b and the latch sections 142c and 142d on the two stages constituting the respective current holding circuits 142 provided in accordance with respective columns in the current holding/distributing section 140A, the controls of simultaneously executing the current holding operation and the current output operation are alternately repeated in accordance with a predetermined operation cycle. Consequently, there is executed the operation in which the signal current Ic corresponding to the display data of each row output from the current generating section 130 is continuously fetched and held in the current holding circuit and simultaneously supplied to the display pixels in the plurality of rows as the gradation current Ipix.

[0096] Therefore, this example is configured in such a manner that the display pixels in a plurality of rows (two rows in this embodiment) are altogether set in the selected state by applying a single scanning signal from the scanning driver to the display panel in which the plurality of display pixels are two-dimensionally arranged and that display data corresponding to the display pixels in the plurality of rows is sequentially fetched and held by the signal driver and the gradation current corresponding to the plurality of rows is simultaneously supplied to the respective display pixels at a predetermined timing (e.g., one scanning period). Therefore, as compared with a known drive control method which applies one scanning signal to one scanning line, the number of scanning lines driven at a single scanning timing (the number of rows of the display pixels to be selected) becomes severalfold, and a time required to write the gradation current in the display pixels can be set to be substantially severalfold (twofold in this example).

[0097] Additionally, since the data lines arranged in each column are formed as a data line group in which a plurality of (two in this example) data lines are determined as one set, a capacitance component consisting of a holding capacitance which is parasitic to each data line and provided in each display pixel or a parasitic capacitance of a drive transistor can be greatly reduced (1/2 in this example) as compared with a configuration of a known display apparatus in which one data line is arranged in one column. Therefore, a time required to write the gradation current supplied to each data line in each display pixel can be reduced, or a delay of this write time can be suppressed.

[0098] As a result, a sufficiently long time to write display data in each display pixel can be assured. Therefore, when the display panel is increased in size or the high definition is realized, or even when an image is displayed with a low gradation, the wiring capacitance of the data lines can be satisfactorily charged to a predetermined voltage, thereby eliminating the insufficient write state of display data. Further, each display pixel can be allowed to emit a light with an appropriate luminance gradation corresponding to display data, and a luminance gradient (display irregularities) generated in the display panel can be greatly reduced, thereby improving the display image quality.

[0099] This example is configured in such a manner that the scanning lines arranged in the respective rows are formed of the scanning line group in which a plurality of (two in this example) scanning lines are determined as one set and that the display pixels for a plurality of rows (two rows in this example) are altogether set in the selected state by using a single scanning signal. Therefore, the number of scanning signals output from the scanning driver to the display panel can be greatly reduced (1/2 in this example), and the number of the connection terminals between the display panel and the scanning driver can be largely decreased (1/2 in this example). As a result, even if the high definition is realized in the display panel, an increase in number of the output terminals of a driver chip can be suppressed, and a pitch (a gap) between the terminals can be prevented from being small, thereby simplifying the positional accuracy in a connection step of the driver chip or reducing the number of steps.

[0100] Furthermore, when a field effect thin film transistor in which an amorphous silicon layer or a polysilicon layer is a channel layer is applied as each transistor constituting the current holding/ distributing section, the current holding/distributing section can be integrally formed with the display panel (the pixel array) on the same substrate, and an increase in the number of components can be suppressed, thereby keeping a product cost of the display apparatus down.

[0101] The above has described the example in which the scanning line group is arranged to correspond to the

display pixels in, e.g., two rows and the data line group corresponding to the display pixels in the two rows is arranged so that the display pixels in the two rows can be simultaneously set in the selected state by using a single scanning signal as the comparative example of the display apparatus. Another structural example of the display apparatus according to this example will now be described.

[0102] FIG. 7 is a schematic structural view showing a primary part of still another structural example of the display apparatus according to this comparative example.

[0103] FIG. 8 is a schematic structural view showing a primary part of yet another structural example of the display apparatus according to this comparative example.

[0104] That is, for example, as shown in FIG. 7, the display panel 110A may be configured to have each scanning line group SGi arranged to correspond to two or more rows (four rows) and each data line group DGj which comprises a plurality of (four) data lines DLja to DLjd whose number (four) corresponds to the plurality of rows and is arranged in accordance with each pixel row. Display pixels EM in the plurality of rows (four rows) can be simultaneously set in the selected state by using a single scanning signal Vsel.

[0105] Furthermore, as shown in FIG. 8, as a configuration (a layout format of scanning lines) of a scanning line group arranged to correspond to a plurality of rows, for example, one scanning line SLi may be drawn (turned) within the display panel 110A without divergence and connected to the display pixels EM in a plurality of rows (two rows) in common.

<Embodiment of Display Apparatus according to the invention>

[0106] An embodiment of a display apparatus according to the present invention will now be described with reference to the accompanying drawings.

[0107] FIG. 9 is a structural view showing a primary part of an embodiment of a display apparatus according to the present invention.

[0108] Here, structures equal to those in the comparative example are denoted by equal or like reference numerals, thereby eliminating the explanation thereof.

[0109] The display apparatus according to the above-mentioned comparative example comprises: the display panel in which each scanning line group SGi corresponding to a plurality of rows and each data line group DGj consisting of a plurality of data lines corresponding to the plurality of rows are arranged; and peripheral circuits (the scanning driver and the signal driver comprising the current generating section and the current holding/distributing section) corresponding to the display panel. The display apparatus according to the embodiment comprises: a display panel in which each scanning line provided in accordance with each row and each data line group consisting of a plurality of data lines corresponding to a plurality of rows are arranged; and peripheral circuits (a scanning driver and a signal driver comprising a current generating section and a current holding/distributing section) corresponding to the display panel.

[0110] As shown in FIG. 9, a display panel 110B according to this embodiment generally comprises: a plurality of display pixels EM which are two-dimensionally arranged (n rows $\times$ m columns) and connected to each other through selection transistors Trsel; a plurality of scanning lines SLq (q is a positive integer falling within a range of $1 \leqq q \leqq n$; n is a positive integer and the total number of pixel rows set in the display panel 110) arranged in accordance with the display pixels EM in respective rows; and a plurality of data line groups DGj which are arranged in accordance with the display pixels EM in respective columns and in which a plurality of (two in this embodiment) data lines DLja and DLjb (j is a positive integer falling within a range of $1 \leqq j \leqq m$; m is a positive integer and the total number of pixel columns set in the display panel 110) are determined as one set. Each display pixel EM is provided at each intersection of the scanning line SLq and the data lines DLja and DLjb constituting each data line group DGj.

[0111] The scanning driver (the selection circuit) 120B is generally connected with the scanning lines SLq in the display panel 110B, and sequentially applies a scanning signal Vsel to each scanning line SLq at a predetermined timing to sequentially set the display pixels EM in each row (one row) connected with the scanning line SLi in a selected state.

[0112] The current generating section 130 generally generates a signal current (a gradation signal) Ic having a current value corresponding to a luminance gradation value based on display data in accordance with the display data supplied from the display signal generating section 160.

[0113] The current holding/distributing section 140B is generally connected with each data line group DGj in the display panel 110B. The section 140B fetches the signal current Ic corresponding to a plurality of rows (two rows in this embodiment) supplied from the current generating section 130 in time series, and sequentially supplies a gradation current Ipix based on the signal current Ic to the display pixels EM in a plurality of rows (two rows in this embodiment) at a predetermined timing. In this embodiment, the current generating section 130 and the current holding/distributing section 140B constitute a signal driver 200B.

[0114] It is to be noted that, in the configuration shown in FIG. 9, the current holding/distributing section 140B is integrally formed with a pixel array on an insulating substrate BASE on which the plurality of display pixels EM (i.e., the pixel array) constituting the display panel 110B are formed as a structural example, but the present invention is not restricted thereto. For example, the signal driver 200B may have a conformation of a driver chip and mounted (packaged) on the substrate BASE. The detail will be described later.

[0115] A concrete configuration of each structure will

now be described.

(Display Panel)

[0116] For example, as shown in FIG. 9, the display panel 110 which can be applied to the display apparatus according to this embodiment has a configuration in which each scanning line SLq corresponding to each pixel row and each data line group DGj having two data lines DLja and DLjb determined as one set and corresponding to one pixel column are arranged to be orthogonal to each other and the display pixel EM is connected at each intersection of an odd-numbered scanning line SLi and the data line DLja in each column and at each intersection of an even-numbered scanning line SLi and the data line DLjb in each column.

[0117] In this embodiment, in the configuration depicted in FIG. 9, although the data line group DGj arranged in each column is configured with the two data lines DLja and DLjb being determined as one set, the present invention is not restricted thereto, and two or more data lines may be determined as one set. In this case, when the number of data lines constituting the data line group DGj is q (i.e., the number of the data lines DLj1 to DLjq is q), there is provided a configuration in which the display pixel EM is connected at each intersection of the scanning line in each row which can be calculated by dividing a line number by q with a remainder of 1 (each scanning line in the first, q+1th, 2q+1th, ... rows) and the first data line DLj1 in each column, the display pixel EM is connected at each intersection of the scanning line in each row which can be calculated in the same manner with a remainder of 2 (each scanning line in the second, q+2th, 2q+2th, ... rows) and the second data line DLj2 in each column, the display pixel and the data line are then connected in the same relationship, and the display pixel EM is connected at each intersection of the scanning line in each row which can be calculated in the same manner with a remainder of 0 (each scanning line in the qth, 2qth, 3qth, ... rows) and the qth (last) data line DLjq in each column.

[0118] Further, like the display pixel EM in FIG. 2, each display pixel EM generally has a configuration in which a gate terminal is connected with each scanning line SLi and a source terminal is connected with a drain terminal of the selection transistor Trsel connected to each data line DLja or DLjb, and comprises a current controlled type light emitting element which emits a light with a predetermined luminance gradation based on a gradation current Ipix supplied through the selection transistor Trsel.

[0119] In the display panel 110B having such a configuration, by applying a scanning signal Vsel to the scanning line SLi in a specific row from the later-described scanning driver 120B, the selection transistor Trsel connected with this scanning line SLi is turned on, and the display pixels EM in this row are altogether set in a selected state. In this selected state, when the gradation current Ipix corresponding to display data is simultaneously supplied to a specific data line in each data line group DGj, the display data is simultaneously written in the display pixels EM in this row set in the selected state through the selection transistors Trsel which has been turned on.

(Scanning Driver)

[0120] The scanning driver 120B sequentially executes an operation of applying the scanning signal Vsel at a selection level (e.g., a high level) to each scanning line SLq based on a scanning control signal supplied from the system controller 150 so that the display pixels EM in each row connected with each scanning line SLi are simultaneously set in the selected state and the display pixels EM in at least adjacent rows are simultaneously set in the selected state in a predetermined period. That is, as shown in, e.g., FIG. 9, the scanning driver 120 comprises shift blocks SB1, SB2, ..., SBi, ... SBn each comprising a shift register and a buffer on a plurality of stages (n stages in this embodiment) in accordance with respective scanning lines SLq. A shift signal which is output while sequentially shifting from the upper part toward the lower part in the display panel 110 by the shift registers is applied to each scanning line SLq through each buffer as a scanning signal Vsel having a predetermined selection level (a high level) based on scanning control signals (a scanning start signal SST, a scanning clock signal SCK and the like) supplied from the system controller 150. Here, in this embodiment, in the scanning driver having the above-described configuration, for example, a scanning clock signal SCK is set to a regular time width which sets the selected state (a selection time width for each row in which the scanning signal Vsel is applied) in a predetermined period (one horizontal scanning period) in accordance with each row and a scanning start signal SST is set to a selection time width for two rows (two horizontal scanning periods). As a result, the shift signal having the time width for two rows is shifted between the respective shift blocks SB1, SB2, ... SBi, ... SBn, and the scanning signal Vsel based on the shift signal is applied to at least adjacent scanning lines SLi in an overlapping manner in a predetermined period.

(Current Generating Section)

[0121] The current generating section 130 has the same configuration as that of the current generating section 130 in the first embodiment shown in FIG. 3, and sequentially and repeatedly executes an operation for one screen. In this operation, the current generating section 130 sequentially fetches at a predetermined timing display data corresponding to the display pixels in a plurality of rows (two rows in this embodiment) in each data line group DGj supplied from the display signal generating section 160 based on a data control signal fed from the system controller 150, generates a signal current (a gradation signal) Ic having a current value corresponding

to a luminance gradation value of the display data, and sequentially supplies the signal current Ic for a plurality of rows to the current holding/distributing section 140B in time series in accordance with each column.

(Current holding/distributing Section)

[0122] The current holding/distributing section 140B sequentially fetches and holds at a predetermined timing the signal current Ic for the plurality of rows corresponding to each data line group DGj supplied from the current generating section 130 in time series based on the data control signal fed from the system controller 150. The section 140B simultaneously supplies the signal current Ic as a gradation current Ipix to the display pixels EM in each row which are set in the selected state through each data line group DGj.

[0123] Specifically, for example, as shown in FIG. 9, the current holding/distributing section 140B comprises at least a plurality of current holding/distributing circuits 143 provided in accordance with the respective data line groups DGj arranged in the display panel 110B. Moreover, the current holding/distributing section 140B distributes and holds the signal current Ic supplied in time series from the current generating section 130 in accordance with each of the plurality of (two in this embodiment) data lines DLja and DLjb in each data line group DGj at a timing of setting each scanning line SLq in the selected state, and sequentially supplies the gradation current Ipix based on the held signal current Ic to the display pixels EM of the respective data lines DLja and DLjb.

[0124] It is to be noted that the concrete configuration and operation of the current holding/distributing section 140B will be described later in detail.

<Concrete Example of Current Holding/distributing Section>

[0125] A concrete example of the current holding/ distributing section which can be applied to the display apparatus according to this embodiment will now be described.

[0126] FIG. 10 is a circuit block diagram showing a structural example of the current holding/distributing section which can be applied to the display apparatus according to this embodiment.

[0127] It is to be noted that just a structural example which can be applied to the display apparatus according to this embodiment is described herein, and the present invention is not restricted to this example.

[0128] Each current holding/distributing circuit 143 constituting the current holding/holding section 140B is, as shown in, e.g., FIG. 10, configured to have a two-stage latch section comprising a holding section (a signal holding/outputting section) 143a connected with the data line DLja and a latch section (the signal holding/outputting section) 143b connected with the data line DLjb, these sections 143a and 143b being connected in parallel with the signal current Ic output from the current generating section 130 being supplied thereto in common. The data lines Dlja and DLjb constitutes each data line group DGj.

[0129] For example, as shown in FIG. 10, the current holding/distributing section 143a includes a transistor Tr46a in which the signal current Ic output from the current generating section 130 is supplied to one end side of a current path (a source or a drain), the other end side of the same is connected with a contact point N46a and a first current fetch signal WTodd is applied to a control terminal (a gate); a transistor Tr47a in which a current path is connected between the contact point N46a and a contact point N47a and the first current fetch signal WTodd is applied to a control terminal; a transistor Tr48a in which one end side of a current path is connected with the contact point N46a, the other end side of the same is connected with a low-potential voltage (-Vcc) and a control terminal is connected with the contact point N47a; a transistor Tr49a in which one end side of a current path is connected with the low-potential voltage (-Vcc), the other end side of the same is connected with the data line DLja and a control terminal is connected with the contact point N47a; and a storage capacitance Ce connected between the contact point N47a and the low-potential voltage (-Vcc).

[0130] Furthermore, the current holding/distributing section 143b also includes, as shown in, e.g., FIG. 10, a transistor Tr46b in which a signal current Ic output from the current generating section 130 is supplied to one end side of a current path (a source or a drain), the other end side of the same is connected with a contact point N46b and a second current fetch signal WTevn is applied to a control terminal (a gate); a transistor Tr47b in which a current path is connected between the contact point N46b and a contact point N47b and the second current fetch signal WTevn is applied to a control terminal; a transistor Tr48b in which one end side of a current path is connected with the contact point N46b, the other end side of the same is connected with a low-potential voltage (-Vcc) and a control terminal is connected with the contact point N47b; a transistor Tr49b in which one end side of a current path is connected with the low-potential voltage (-Vcc), the other end side of the same is connected with the data line DLjb and a control terminal is connected with the contact point N47b; and a storage capacitance Cf connected between the contact point N47b and the low-potential voltage (-Vcc).

[0131] Here, in the current holding/distributing section 140B according to this embodiment, for example, an n-channel type field effect thin film transistor in which an amorphous silicon layer is a channel layer or a field effect thin film transistor in which a polysilicon layer is a channel layer may be applied as each of the transistors Tr46a to Tr49a and Tr46b to Tr49b. In this case, as shown in FIG. 9, the current holding/distributing section 140B can be integrally formed with the pixel array on the insulating substrate BASE constituting the display panel 110B.

[0132] Additionally, each of the storage capacitances

Ce and Ce provided to the respective latch sections 142a and 143b may be a parasitic capacitance formed between the gate and the source of each of the transistors Tr49a and 49b or an individually provided capacitance element.

[0133] In the current holding/distributing circuit 143, the storage capacitances Ce and Cf constitute the signal holding section and the charges storage circuit according to the present invention, the transistors Tr46a, Tr47a, Tr46b and Tr47b constitute the signal distributing section according to the present invention, and the transistors Tr48a, Tr49a, Tr48b and Tr49b constitute the gradation current outputting section according to the present invention.

[0134] The invention in the current holding/distributing section having the above-described configuration will now be explained.

[0135] FIGS. 11A and 11B are conceptual views illustrating general operations of the current holding/ distributing section which can be applied to this embodiment.

[0136] The operation of the current holding/distributing section 140B (the current holding/distributing circuit 143) according to this embodiment has: a current holding/output operation of sequentially fetching the signal current Ic based on display data corresponding to the display pixels in two rows supplied from the current generating section in time series by the respective latch sections 143a and 143b of the current holding/distributing circuit 143, generating a gradation current Ipix based on the signal current (a gradation signal) Ic and individually outputting the generated current to the respective data lines Dlja and DLjb constituting the data line group DGj at a predetermined timing; and a current output holding operation of continuing output of the gradation current Ipix in the current holding/output operation for a predetermined period. The current holding/distributing section 140B is controlled to alternately repeat the current holding/output operation and the current output holding operation with partially overlapping periods between the latch sections 143a and 143b connected in parallel. As a result, output periods of the gradation current Ipix from the respective latch sections 143a and 143b in the current holding/output operation are set to partially overlap.

[0137] The operation will now be concretely described with reference to each circuit configuration in the current holding/distributing section.

[0138] In the current holding/distributing circuit 143 (the latch sections 143a and 143b), the first and second current fetch signals WTodd and WTevn supplied as data control signals from the system controller 150 are selectively set to a high level. As a result, one (the latch section 143a or 143b) of the latch sections 143a and 143b is set in the current holding/output operation state in which the signal current Ic is fetched and the gradation current Ipix corresponding to the signal current Ic is output, and the other latch section (the latch section 143b or 143a) is set in the current output holding operation state in which the output state of the gradation current Ipix in the current holding/output operation state with the foregoing timing is continued.

[0139] Specifically, in the current holding/output operation, as shown in FIG. 11A, the first current fetch signal WTodd is set to the high level, and the second current fetch signal WTevn is set to the low level. As a result, in the latch section 143a, the transistors Tr46a and Tr47a are turned on, the part between the gate and the drain of the transistor Tr48a is electrically short-circuited by the transistor Tr47a and hence the transistor Tr48a is turned on in a saturation region. As a result, the signal current (the gradation signal) Ic supplied from the current generating section 130 flows toward the low-potential voltage (-Vcc) side through the transistors Tr46a and Tr48a of the latch section 143a, and a current level of the signal current Ic is converted into a voltage level between the gate and the source of the transistor Tr48a so that the signal current Ic is stored as the electric charges in the storage capacitance Ce.

[0140] At this time, with storage of the electric charges in the storage capacitance Ce, the transistors Tr48a and Tr49a constituting a current mirror circuit are turned on by an increase in potential at the contact point N47a, and the gradation current Ipix having a predetermined current ratio set in the current mirror circuit with respect to the signal current Ic flows in such a manner that the gradation current Ipix is drawn from the data line DLja side toward the low-potential voltage (-Vcc), direction (i.e., from the display pixel EM side toward the latch section 143a) through the transistor Tr49a.

[0141] In the current output holding operation, as shown in FIG. 11B, the first current fetch signal WTodd is set to the low level, and the second current fetch signal WTevn is set to the high level. As a result, in the latch section 143a, the transistors Tr46a and Tr47a are turned off. At this time, since a potential (a high voltage) based on the electric charges (the signal current Ic) stored in the storage capacitance Ca is held in the contact point N47a by the current holding/output operation, the transistor Tr49a continues the ON state. Consequently, the operation state in which the gradation current Ipix is drawn from the data line DLja side toward the latch section 143a (the current holding/distributing circuit 143) is held.

[0142] Further, in the state where the first current fetch signal WTodd is set at the low level and the second current fetch signal WTevn is set at the high level (i.e., the current output holding operation state of the latch section 143a mentioned above), the transistors Tr46b and Tr47b are turned on, and the part between the gate and the drain of the transistor Tr48b is electrically short-circuited by the transistor Tr47b so that the transistor Tr48b is turned on a saturation region in the latch section 143b connected with the latch section 143a in parallel. Therefore, the current holding/output operation is executed. In this operation, the signal current Ic flows toward the low-potential voltage (-Vcc) side through the transistors Tr46b and Tr48b of the latch section 143b, and a current

level of the signal current Ic is converted into a voltage level between the gate and the source of the transistor Tr48b so that the signal current Ic is stored as the electric charges in the storage capacitance Cf. Further, the transistors Tr48b and Tr49b constituting the current mirror circuit are turned on with an increase in potential at the contact point N47b, and the gradation current Ipix having a predetermined current ratio with respect to the signal current Ic flows in such a manner that the gradation current Ipix is drawn from the data line DLjb side toward the low-potential voltage (-Vcc) side (i.e., from the display pixel EM side toward the latch section 143b) through the transistor Tr49b.

[0143] That is, in a period where one of the latch sections 143a and 143b is set in the current holding/output operation state, the other section is concurrently set in the current output holding operation state.

[0144] It is to be noted that the description has been given as to the example where the negative gradation current Ipix corresponding to the signal current Ic having the positive polarity supplied from the current generating section 130 is generated and the gradation current Ipix is drawn from the data line (the display pixel) side in the current holding/distributing section 140B in order to cope with the circuit configuration of the later-described pixel drive circuit provided in the display pixel EM. However, the current holding/ distributing section 140B may have a configuration in which the gradation current Ipix with the positive polarity is generated and passed to the data lines (the display pixels) in accordance with the circuit configuration of the display pixels EM.

<Drive Control Method of Display Apparatus>

[0145] A drive control operation in the display apparatus having the above-described configuration will now be explained.

[0146] FIG. 12 is a timing chart showing a drive control method of the display apparatus according to this embodiment.

[0147] In the display apparatus having the above-described configuration, display data consisting of digital data is first extracted from a video signal by the display signal generating section 160, the display data being used to allow each display pixel (a light emitting element) EM constituting the display panel 110B with a predetermined luminance gradation, the extracted display data is then sequentially supplied to the current generating section 130 as serial data corresponding to each row of the display panel 110B.

[0148] The display data supplied to the current generating section 130 is converted into a signal current (a gradation signal) corresponding to the display data at a timing based on a data control signal fed from the system controller 150, and output to the current holding/distributing section 140B provided in accordance with the data line group DGj of each column arranged in the display panel 110B.

[0149] In the current holding/distributing section 140B, as shown in FIG. 12, the latch section 143a of the current holding/distributing circuit 143 is set in the current holding/outputting operation state based on data control signals (a first current fetch signal WTodd at the high level and a second current fetch signal WTevn at the low level) supplied from the system controller 150. As a result, the current holding/ outputting operation is executed. In this operation, the signal current Ic corresponding to the display pixels EM for one row (e.g., the first row) in each column is fetched, and the electric charges based on the signal current Ic is stored in the storage capacitance Ce. At the same time, a gradation current Ipix having a predetermined current value is generated based on the electric charges stored in the storage capacitance Ce and a current ratio set by a current mirror circuit (the transistors Tr48a and Tr49a), and the generated gradation current Ipix is supplied to each display pixel EM in this row (the first row) through each data line DLja.

[0150] Subsequently, after the current holding/outputting operation, the latch section 143a of the current holding/distributing circuit 143 is set in the current output holding operation state based on data control signals (the first current fetch signal WTodd at the low level and the second current fetch signal WTevn at the high level) supplied from the system controller 150. As a result, the current output holding operation is executed. In this operation, the gradation current Ipix based on the electric charges (i.e., the signal current Ic) stored in the storage capacitance Ce is continuously supplied to each display pixel EM in this row (the first row) through each data line DLja in the latch section 143a.

[0151] On the other hand, as shown in FIG. 12, in the latch section 143a, in a period where the current output holding operation is executed, the latch section 143b of the current holding/distributing circuit 143 is set in the current holding/outputting operation based on data control signals (the first current fetch signal WTodd at the low level and the second current fetch signal WTevn at the high level) supplied from the system controller 150. As a result, the current holding/outputting operation is executed. In this operation, the signal current Ic for the next row (e.g., the second row) continuously supplied from the current generating section 130 is fetched in the latch section 143b, and the electric charges is stored in the storage capacitance Cf. At the same time, a gradation current Ipix having a predetermined current value is generated based on the electric charges stored in the storage capacitance Cf and a current ratio set by the current mirror circuit (the transistors Tr48b and Tr49b), and the generated gradation current Ipix is then supplied to each display pixel EM in this row (the second row).

[0152] Then, after the current output holding operation in the latch section 143a, the system controller 150 again sets the first current fetch signal WTodd to the high level and the second current fetch signal WTevn to the low level. As a result, the latch section 143a is again set in the current holding/outputting operation state. Conse-

quently, the current holding/outputting operation is executed. In this operation, the electric charges based on the signal current Ic for the next row (e.g., the third row) is stored in the storage capacitance Ce. At the same time, the gradation current Ipix based on the electric charges stored in the storage capacitance Ce and the current ratio set by the current mirror circuit is supplied to each display pixel EM in this row (the third row) through each data line DLja.

[0153] Furthermore, at this time, when the latch section 142b of the current holding/distributing section 143 is set in the current output holding operation state, the current output holding operation is executed. In this operation, the gradation current Ipix based on the electric charges stored in the storage capacitance Cf at the foregoing timing is supplied to each display pixel EM in a row which is a target of the current holding/outputting operation (the second row) through each data line DLjb.

[0154] As a result, in the current holding/distributing section 140B, the controls which concurrently execute the current holding/outputting operation and the current output holding operation are alternately repeated with predetermined operation cycles between the latch sections 143a and 143b on the two stages constituting each current holding/distributing circuit 143 provided in accordance with each column. As a result, there is executed the operation in which the signal current Ic corresponding to the display data of each row sequentially supplied from the current generating section 130 is continuously fetched and held in the current holding circuit and, at the same time, the signal current Ic is simultaneously supplied to the display pixels in each row as the gradation current Ipix.

[0155] Therefore, the gradation current Ipix is output from the current holding/distributing section 140B through the data line group DLj of each column, and the scanning signal Vsel at the high level is applied from the scanning driver 120 to at least adjacent scanning lines SLq at the timing based on the scanning control signal supplied from the system controller 150 in an overlapping manner during a predetermined period. As a result, the gradation current Ipix sequentially supplied through the data lines DLja and DLjb of each data line group DLj is written in the display pixels EM in a plurality of rows (e.g., two rows including the first row and the second row) corresponding to the respective scanning lines SLi, and a light emission operation is executed with a predetermined luminance gradation based on the gradation current Ipix.

[0156] As described above, in this embodiment, by applying the scanning signal to at least adjacent scanning lines in the display panel having the plurality of display pixels two-dimensionally arranged therein from the scanning driver in an overlapping manner in a predetermined period, the display pixels in each row are sequentially set in the selected state, and the display data corresponding to the display pixels in each row is sequentially fetched and held in each latch section by the signal driver. At the same time, the gradation current of each row is sequentially supplied to each display pixel. Therefore, the gradation current based on the display data can be simultaneously written in the display pixels in the plurality of rows with the simple structure including the latch sections corresponding to several data lines constituting the data line groups in respective rows, thereby setting the gradation current write time to be substantially long.

[0157] Specifically, as shown in FIG. 9, in the configuration where the data line group arranged in each column comprises two data lines and two latch sections are provided in the current holding/distributing section in accordance with each data line group, it is possible to set a period which is 1/2 of the period of selecting the display pixels in a specific row by the scanning period to overlap the period of selecting the display pixels in the next row. That is, it is possible to set the selection period to overlap in adjacent rows only in a period corresponding to the number of data lines constituting the data line group.

[0158] Further, like the comparative example, the number of the display pixels connected to each of the plurality of data lines constituting the data line group in each column can be greatly reduced to (1/2 in this embodiment) as compared with a known display apparatus in which one data line is arranged in one row. Therefore, a capacitance component consisting of a holding capacitance provided in the display element or a parasitic capacitance of the drive transistor can be reduced, and hence the time required to write the gradation current supplied to the data line in the display element can be decreased or a delay of this write time can be suppressed.

[0159] It is to be noted that this embodiment is configured in such a manner that the display data corresponding to the display pixels in each row is fetched and held in each latch section by the signal driver and, at the same time, the gradation current for each row is generated and sequentially supplied to each display pixel, and hence the latch operation in the current holding/distributing circuit (the latch section) must be rapidly executed. If the timing of the latch operation deviates due to a delay in signal or the like, there is a possibility that the display operation is obstructed.

[0160] Thus, in this embodiment, the latch operation of the display data (the signal current) in the current holding/distributing circuit (the latch section) is rapidly performed with a small current, and the current mirror circuit configuration is applied to an output stage for each data line. As a result, a current value (an absolute value) of the gradation current can be simply controlled to obtain a large current, and a delay in the latch operation can be suppressed.

[0161] As described above, in FIG. 9, each of the plurality of transistors constituting each current holding/distributing circuit 143A in the current holding/distributing section 140B comprises an n-channel type field effect thin film transistor in which an amorphous silicon semiconductor layer is a channel layer or a field effect thin

film transistor in which a polysilicon semiconductor layer is a channel layer, and this current holding/distributing section 140B is integrally formed with the pixel array on the insulating substrate BASE on which the plurality of display pixels EM constituting the display panel 110B are formed. However, the present invention is not restricted to this configuration.

[0162] For example, the present invention may have a conformation in which the signal driver including the current generating section and the current holding/ distributing section is an independent driver chip and this driver chip is mounted (packaged) on the substrate of the display panel.

[0163] A structural example in this case will now be briefly explained.

[0164] FIG. 13 is a schematic structural view showing a primary part of another structural example in the second embodiment of the display apparatus according to the present invention.

[0165] Here, structures equal to those in the foregoing structural example are denoted by like or equal reference numerals, thereby simplifying the explanation.

[0166] In FIG. 13, the signal driver 200C including the current holding/distributing section 140B and the current generating section 130 is configured as an independent driver chip. Here, the current holding/ distributing circuit 143 in FIG. 13 comprises a plurality of field effect transistors or the like formed on a single-crystal silicon substrate, for example. The driver chip constituting this signal driver 200C is configured to be mounted (packaged) on the substrate BASE constituting the display panel 110B.

<Concrete Circuit Example of Display Pixel>

[0167] A concrete circuit example of the display pixel which can be applied to the display apparatus according to the present invention will now be described with reference to the accompanying drawings.

[0168] FIG. 14 is a circuit block diagram showing a concrete circuit example of the display pixel which can be applied to the display apparatus according to the present invention.

[0169] FIGS. 15A and 15B are conceptual views showing drive control operations of the pixel drive circuit according to this embodiment.

[0170] FIG. 16 is a schematic block diagram showing a structural example of the display apparatus to which the display pixel according to this embodiment is applied.

[0171] FIG. 17 is a schematic block diagram showing another structural example of the display apparatus to which the display pixel according to this embodiment is applied.

[0172] As shown in FIG. 14, a display pixel EM' (a structure comprising the display pixel EM and the selection transistor Trsel described in connection with the comparative example) is generally configured to have: a pixel drive circuit DC which sets the display pixel EM' in a selected state based on a scanning signal Vsel applied from the scanning driver 120A or 120B, fetches a gradation current Ipix supplied from the current holding/distributing section 140A or 140B in the selected state, and passes a drive current corresponding to the gradation current Ipix to a light emitting element; and a current controlled type light emitting element comprising an EL element or an OEL element which emits a light with a predetermined luminance gradation based on the drive current supplied from the pixel drive circuit DC.

[0173] For example, as shown in FIG. 14, the pixel drive circuit DC comprises: an n-channel type transistor Tr11 in which a control terminal (a gate terminal) is connected to a scanning line SLi (corresponding to the scanning line SLia, and SLib or SLq constituting the scanning line group SGi described in conjunction with each of the foregoing examples and embodiments) and a current path (a source - a drain) is connected to a power supply line VL and a contact point N11; an n-channel type transistor Tr12 in which a control terminal is connected with the scanning line SLi and a current path is connected with a data line DLj (each data line DLja or DLjb constituting the data line group DGj described in conjunction with each of the foregoing examples and embodiments) and a contact point N12; an n-channel type transistor Tr13 in which a control terminal is connected with the contact point N11 and a current path is connected with the power supply line VL and the contact point N12; and a capacitor (a holding capacitance) Cs connected between the contact point N11 and the contact point N12. An anode terminal of an organic EL element OEL is connected to the contact point N12, and a cathode terminal of the same is connected to a ground terminal. Here, the capacitor Cs may be a parasitic capacitance formed between the gate and the' source of the transistor Tr13. Moreover, the transistor Tr12 corresponds to the selection transistor Trsel described in conjunction with each of the foregoing embodiments.

[0174] The light emission drive control of the light emitting element (the organic EL element OEL) in the pixel drive circuit DC having such a configuration is executed by, e.g., simultaneously setting the display pixels EM' in a plurality of rows in a selected state within one scanning period Tsc as one cycle so that the selected states of the display pixels overlap in a predetermined period, and setting a selection period (a write operation period) Tse in which a drive current Ipix corresponding to display data is written and held as a voltage component and a non-selection period (a light emitting operation period) Tnse in which a drive current corresponding to the display data is supplied to the organic EL element based on the voltage component written and held in the selection period Tse to emit a light with a predetermined luminance gradation (Tse = Tse + Tnse).

(Selection Period)

[0175] That is, in the selection period Tse for the display pixels EM', the display pixels EM' in a plurality of

rows are first simultaneously (or overlappingly in a predetermined period) to a selected state by applying a scanning signal Vsel at the high level to specific scanning lines SLi from the scanning driver and, at the same time, a power supply voltage Vsc at the low level is applied to the power supply line VL of the display pixels in the plurality of rows. Further, in synchronization with this timing, a gradation current Ipix having a negative polarity corresponding to display data of the display pixels EM' in the plurality of rows is supplied to each data line DLj from the current holding/distributing section.

[0176] As a result, as shown in FIG. 15A, the transistors Tr11 and Tr12 constituting the pixel drive circuit DC are turned on, and the power supply voltage Vsc at the low level is applied to the contact point N11 (that is, the gate terminal of the transistor Tr13 and one end of the capacitor Cs). Furthermore, the operation of drawing the gradation current Ipix toward the current holding/distributing section through the data line DL is performed. As a result, a voltage level whose potential is lower than the power supply voltage Vsc at the low level is applied to the contact point N12 (that is, the source terminal of the transistor Tr13 and the other end of the capacitor Cs).

[0177] In this manner, a potential difference is generated between the contact points N11 and N12 (between the gate and the source of the transistor Tr13). As a result, the transistor Tr13 is turned on, and a write current Ia corresponding to the gradation current Ipix flows toward the current holding/ distributing section from the power supply line VL through the transistor Tr13, the contact point N12, the transistor Tr12 and the data line DL.

[0178] At this time, the electric charges corresponding to the potential difference generated between the contact points N11 and N12 (between the gate and the source of the transistor Tr13) is stored in the capacitor Cs, and held (charged) as a voltage component. Moreover, the power supply voltage Vsc having a voltage level which is not greater than the ground potential is applied to the power supply line VL, and the write current Ia is controlled to flow in the direction of the data line DL. Therefore, a potential applied to an anode terminal (the contact point N12) of the organic EL element becomes lower than a potential (the ground potential) of the cathode terminal, and a reverse bias voltage is applied to the organic EL element OEL. Therefore, the drive current does not flow through the organic EL element OEL, and the light emitting operation is not carried out.

(Non-selection Period)

[0179] Subsequently, in the non-selection period Tnsec after completion of the selection period Tse, the scanning signal Vsel at the low level is applied to specific scanning lines SLi from the scanning driver so that the display pixels in a plurality of rows are set in a non-selected state, and the power supply voltage Vsc at the high level is applied to the power supply line VL of the display pixels in the plurality of rows. Further, in synchronization with this timing, the operation of drawing the gradation current Ipix by the current holding/distributing section is stopped.

[0180] As a result, as shown in FIG. 15B, the transistors Tr11 and Tr12 constituting the pixel drive circuit DC are turned off, and application of the power supply voltage Vsc to the contact point N11 (i.e., the gate terminal of the transistor Tr13 and one end of the capacitor Cs) is interrupted. Furthermore, application of the voltage level to the contact point N12 (i.e., the source terminal of the transistor Tr13 and the other end of the capacitor Cs) due to the operation of drawing the gradation current Ipix by the current holding/distributing section is interrupted. Therefore, the capacitor Cs holds the electric charges stored in the selection period.

[0181] When the capacitor Cs holds the charges voltage in the write operation in this manner, the potential difference between the contact points N11 and N12 (between the gate and the source of the transistor Tr13) is held, and hence the transistor Tr13 maintains the ON state. Moreover, since the power supply voltage Vsc having a voltage level higher than the ground potential is applied to the power supply line VL, the potential applied to the anode terminal (the contact point N12) of the organic EL element OEL becomes higher the potential (the ground potential) of the cathode terminal.

[0182] Therefore, a predetermined drive current Ib flows from the power supply line VL to the organic EL element OEL in a forward bias direction through the transistor Tr13 and the contact point N12, and the organic EL element OEL emits a light. Here, since the potential difference (the charges voltage) held by the capacitor Cs corresponds to a potential difference in case of passing a write current Ia corresponding to the gradation current Ipix in the transistor Tr13, the drive current Ib passed to the organic EL element OEL has the same current value as that of the write current Ia.

[0183] As a result, in the non-selection period Tnse after the selection period Tse, the drive current is continuously supplied through the transistor Tr13 based on the voltage component corresponding to the display data (the gradation current Ipix) written in the selection period Tse, and the organic EL element OEL continues the operation of emitting a light with the luminance gradation corresponding to the display data.

[0184] Then, the series of the operations mentioned above is sequentially repeatedly executed with respect to all the scanning lines SLi constituting the display panel 110A or 110B based on the drive control operation of the display apparatus mentioned above. As a result, the display data for one screen of the display panel is written, a light is emitted with a predetermined luminance gradation, and desired image information is displayed.

[0185] Here, in the image drive circuit DC according to this embodiment, since the transistors Tr11 to Tr13 can be constituted by using transistors having the same channel polarity (the n-channel type), it is possible to apply an n-channel type field effect thin film transistor in which

an amorphous silicon layer is a channel layer or a field effect thin film transistor in which a polysilicon layer is a channel layer like the circuit configuration of the current holding/ distributing sections (the current distribution circuit, the current holding circuit, and the current holding/distributing circuit) 140A and 140B. In this case, the current holding/distributing sections 140A and 140B and the display panels 110A and 110B can be integrally formed on the single insulating substrate. In particular, when the display panel and the current holding/distributing section are constituted by applying the n-channel type field effect thin film transistor using an amorphous silicon semiconductor layer, the field effect thin film transistor having stable operation characteristics can be relatively inexpensively manufactured by applying the established amorphous silicon manufacturing technique. Therefore, even if the high definition of the display panel is realized or the display panel is increased in size, the display apparatus having the good display image quality can be readily and excellently realized.

[0186] Here, as a configuration which applies a predetermined power supply voltage Vcs to the power supply line VL in the pixel drive circuit DC according to this embodiment, with respect to the configuration depicted in FIG. 2, as shown in, e.g., FIG. 16, it is possible to excellently apply a configuration in which a power supply drive 170A connected to each power supply line group VGi is provided in a peripheral area of the display panel 110C in which each power supply line group VGi comprising power supply lines VLia and VLib is arranged in parallel with the respective scanning lines SLia and SLib of each scanning line group SGi and, the power supply voltage Vcs having a predetermined voltage value is applied to each power supply line group VGi from the power supply driver 170A based on a power supply control signal fed from the system controller 150 in synchronization with a timing of outputting the scanning signal Vsel from the scanning driver 120A.

[0187] Further, with respect to the configuration depicted in FIG. 13, as shown in, e.g., FIG. 17, it is possible to excellently apply a configuration in which a power supply driver 170B connected with each power supply line VLi is provided in a peripheral area of the display panel 110D in which each power supply line VLi is arranged in parallel with each scanning line SLi in each row, and the power supply voltage Vcs having a predetermined voltage value is applied to each power supply line VLi from the power supply driver 170B based on a power supply control signal fed from the system controller 150 in synchronization with a timing of outputting the scanning signal Vsel from the scanning driver 120B.

[0188] It is to be noted that the description has been given as to the circuit configuration corresponding to the current application scheme which comprises three transistors as the pixel drive circuit DC and draws the gradation current Ipix in a direction of the current holding/distributing section (i.e., a direction of the signal driver) through the data line DLj in the display pixel EM', but the present invention is not restricted to this embodiment. It is possible to use the display apparatus comprising the pixel drive circuit to which at least the current application mode is applied and having another circuit configuration as long as the display apparatus has a light emission control transistor which controls supply of a drive current to the light emitting element and a write control transistor which controls a gradation current write operation, and holds the gradation current (the write current) corresponding to the display data and then turns on the light emission control transistor based on the gradation current to supply the gradation current, thereby allowing the light emitting element to emit a light with a predetermined luminance gradation. For example, the present invention may have a circuit configuration comprising, e.g., four transistors, or may have a circuit configuration which passes the gradation current in a direction of the display pixel (the pixel drive circuit) from the current holding/ distributing section side (i.e., the signal driver side) through the data line.

[0189] Furthermore, although the description has been given as to the configuration in which the organic EL element is applied as the light emitting element constituting the display pixel in the foregoing embodiments, the display apparatus according to the present invention is not restricted thereto. It is possible to excellently apply, e.g., a light emitting diode or any other light emitting element as well as the above-described organic EL element as long as it is a current controlled type light emitting element which emits a light with a predetermined luminance gradation in accordance with a current value of the drive current supplied thereto.

Claims

1. A display drive apparatus for driving a plurality of two-dimensionally arranged display pixels (EM) constituting a display panel (110B) based on display data, the display pixels (EM) being provided along a plurality of rows and columns, each of the display pixels (EM) including a light emitting element which emits a light by a supplied current, the display drive apparatus comprising at least:

   a current generation section (130) which generates a signal current (Ic) which controls a luminance gradation of each display pixel (EM), based on the display data;
   a selection circuit (120B) which sequentially sets each of the display pixels (EM) corresponding to each of said plurality of rows of the display panel (110B) in a selected state, during a selection period ; and
   a current write circuit (140B) which sequentially fetches the signal current (Ic) corresponding to the display pixels (EM) in each of the rows, and supplies a gradation current (Ipix) having a cur-

rent value based on the signal current (Ic) to the display pixels (EM) in each of the rows in accordance with the selection period for setting the selected state,

characterized in that

the selection circuit (120B) sets the selection period for setting the selected state to a period including a non-overlapping period and an overlapping period, wherein in the non-overlapping period, selection periods of adjacent two rows are not overlapped, and in the overlapping period, selection periods of said adjacent two rows are overlapped,

wherein the current generation section (130) has means for sequentially supplying the signal current (Ic) corresponding to two display pixels in each column of the display pixels corresponding to said adjacent two rows to the current write circuit (140B) in time series,

the current write circuit (140B) includes a plurality of current holding circuits (143) which are provided in accordance with respective columns of the display pixels (EM) in each of the rows, sequentially hold the signal current (Ic) supplied from the current generation section (130) in accordance with the timing of time-series supply, and sequentially supply as the gradation current (Ipix) a current having a current value based on the signal current (Ic) to said two display pixels of said two adjacent rows,

wherein each of the current holding circuits (143) includes two current holding/outputting sections (143a, 143b) corresponding to said two display pixels (EM) of said adjacent two rows,

wherein each of the current holding/outputting sections (143a, 143b) includes means which begins an output of the gradation current (Ipix) at the same time as the signal current (Ic) is supplied, and outputs the gradation current (Ipix) over the selection period of each row.

2. A display drive apparatus according to claim 1 wherein the selection circuit (120B) has means for sequentially applying a selection signal (Vsel) which sets the display pixels (EM) in each row in the selected state to the display pixels (EM) in each of the rows of the display panel (110B) with the overlapping periods, thereby sequentially setting the display pixels (EM) in each of the rows in the selected state with the overlapping periods.

3. A display apparatus for displaying image information based on display data, the display apparatus comprising:

a display panel (110B) comprising a plurality of two dimensionally arranged display pixel; and

the display drive apparatus for driving said display panel (110B) in accordance with any one of the claims 1 or 2, wherein the display data is supplied to said gradation signal generation unit (130).

4. A display apparatus according to claim 3, wherein the display panel comprises a plurality of scanning lines (SLq) arranged in a row direction and a plurality of data lines (DLja, DLjb) arranged in a column direction, and a plurality of display pixels (EM) arranged in a matrix form in the vicinity of intersections of the plurality of scanning lines (SLq) and the plurality of data lines (DLja, DLjb), wherein the plurality of data lines (DLja, DLjb) includes a plurality of data line groups (DGj) each of which has two data lines (Dlja, DLjb) corresponding to first and second scanning lines (SLq).

5. A display apparatus according to claim 4, wherein the selection circuit (120B) has means for sequentially applying a selection signal (Vsel) which sets the display pixels (EM) corresponding to each of the plurality of scanning lines (SLq) in the selected state, with the overlapping periods to sequentially set the display pixels (EM) corresponding to each of the plurality of scanning lines (SLq) in the selected state with the overlapping periods, and

the current write circuit (140B) has means for sequentially supplying the gradation current (Ipix) to each data line (DLja, DLjb) of each data line group (DGj) with the overlapping periods at the timing of applying the scanning signal (Vsel) by the selection circuit (120B).

6. A display apparatus according to claim 4, wherein the selection circuit (120B) has means for sequentially applying a selection signal (Vsel) which sets the display pixels (EM) corresponding to each of the plurality of scanning lines (SLq) in the selected state with the overlapping periods to sequentially set the display pixels (EM) corresponding to each of the plurality of scanning lines (SLq) in the selected state with the overlapping periods,

the gradation signal generation circuit (130) has means for sequentially supplying the gradation signal (Ic) corresponding to the plurality of display pixels (EM) corresponding to the plurality of specific scanning lines (SLq) in each data line (DIja, DLjb) of each data line group (DGj) to the current write circuit (140B) in time series, and

the current write circuit (140B) has a plurality of current holding circuits (143) each of which is provided in accordance with each data line group (DGj), sequentially holds the gradation signal (Ic) supplied from the gradation signal generation circuit (130) in accordance with the timing of time-series supply, and sequentially supplies as the gradation current (Ipix) a current having a current value corresponding to

the gradation signal (Ic) to each data line (DLja, DLjb) of each data line group (DGj) at the timing corresponding to application of the scanning signal (Vsel).

7. A display apparatus according to claim 6, wherein each current holding circuit (143) includes two current holding/outputting sections (143a, 143b) in accordance with each data line (DLja, DLjb) of each data line group (DGj), each of the current holding/outputting sections (143a, 143b) having:

a signal distributing section (Tr46a, Tr47a, Tr46b, Tr47b) which sequentially distributes the gradation signal (Ic) in accordance with each data line (DLja, DLjb) of each data line group (DGj) at the timing of the time-series supply;
a signal holding section (Ce, Cf) which holds the gradation signal (Ic) distributed by the signal distributing section; and
a gradation current outputting section (Tr48a, Tr49a, Tr48b, Tr49b) which outputs as the gradation current (Ipix) a current having a current value based on the gradation signal (Ic) held in the signal holding section,
wherein an operation of holding the gradation signal (Ic) distributed by the signal distributing section in the signal holding section in one of the current holding/outputting sections and outputting the gradation current (Ipix) based on the gradation signal (Ic) by the gradation current outputting section, and an operation of outputting the gradation current (Ipix) based on the gradation signal (Ic) held in the signal holding section by the gradation current outputting section in the other current holding/outputting section are controlled to be simultaneously executed in the overlapping periods.

8. A drive method of a display apparatus which displays image information based on display data, the display apparatus having a plurality of scanning lines (SLq) arranged in a row direction and a plurality of data lines (DLja, DLjb) arranged in a column direction, and a display panel (110B) having a plurality of display pixels (EM) which are arranged in the vicinity of intersections of the plurality of scanning lines (SLq) and the plurality of data lines (DLja, DLjb) and arranged in a matrix form, the drive method comprising at least the steps of:

generating a signal current (Ic) which controls a luminance gradation of each display pixel (EM), based on the display data;
setting the display pixels (EM) corresponding to each of the plurality of scanning lines (SLq) in a selected state, during a selection period;
fetching the signal current (Ic) corresponding to the display pixels (EM) corresponding to each of the plurality of scanning lines (SLq),
generating a gradation current (Ipix) having a current value based on the signal current (Ic), and supplying the gradation current (Ipix) to the display pixels (EM) corresponding to each of the plurality of scanning lines (SIq) in accordance with a selection period; and
allowing the display pixels (EM) in which the gradation current (Ipix) is supplied and written to operate with a display luminance based on a current value of the gradation current (Ipix),
characterized in that
in the step of setting the display pixels, the selection period for setting the selected state is set to a period including a non-overlapping period and an overlapping period, wherein
in the non-overlapping period, selection periods of adjacent two rows are not overlapped, and in the overlapping period, selection periods of said adjacent two rows are overlapped,
wherein in the step of generating a signal current (Ic), the signal current (Ic) corresponding to two display pixels in each column of the display pixels corresponding to said adjacent two sequentially supplying rows is sequentially supplied to a current write circuit (140B) in time series,
the current write circuit (140B) including a plurality of current holding circuits (143) which are provided in accordance with respective columns of the display pixels (EM) in each of the rows, sequentially hold the signal current (Ic) supplied from the current generation section (130) in accordance with the timing of time-series supply, and sequentially supply as the gradation current (Ipix) a current having a current value based on the signal current (Ic) to said two display pixels of said two adjacent rows,
wherein each of the current holding circuits (143) includes two current holding/outputting sections (143a, 143b) corresponding to said two display pixels (EM) of said adjacent two rows, and
wherein in the step of generating a gradation current (Ipix), an output of the gradation current (Ipix) begins at the same time as the signal current (Ic) is supplied, and the gradation current (Ipix) is output over the selection period of each row.

Patentansprüche

1. Anzeigetreibervorrichtung für das Treiben einer Vielzahl von zweidimensional angeordneten Anzeigebildpunkten (EM), die ein Anzeigepaneel (110B) bilden, basierend auf Anzeigedaten, wobei die Anzeigebildpunkte (EM) entlang einer Vielzahl von Reihen und Spalten vorgesehen sind, wobei jeder der Anzeigebildpunkte (EM) ein Lichtemissionselement

enthält, das Licht emittiert, wenn es mit Strom versorgt wird, wobei die Anzeigetreibervorrichtung wenigstens Folgendes umfasst:

einen Stromerzeugungsabschnitt (130), der einen Signalstrom (Ic), der eine Luminanzabstufung jedes Anzeigebildpunkts (EM) steuert, basierend auf den Anzeigedaten erzeugt,
eine Auswahlschaltung (120B), die sequentiell jeden der Anzeigebildpunkte (EM) in Entsprechung zu jeder aus der Vielzahl von Reihen des Anzeigepaneels (110B) in einen ausgewählten Zustand während einer Auswahlperiode setzt, und
eine Stromschreibschaltung (140B), die sequentiell den Signalstrom (Ic) in Entsprechung zu den Anzeigebildpunkten (EM) in jeder der Reihen abruft und einen Abstufungsstrom (Ipix) mit einem Stromwert basierend auf dem Signalstrom (Ic) zu den Anzeigebildpunkten (EM) in jeder der Reihen in Übereinstimmung mit der Auswahlperiode für das Setzen des ausgewählten Zustands zuführt,
dadurch gekennzeichnet, dass
die Auswahlschaltung (120B) die Auswahlperiode für das Setzen des ausgewählten Zustands zu einer Periode setzt, die eine nicht-überlappende Periode und eine überlappende Periode enthält, wobei in der nicht-überlappenden Periode Auswahlperioden von zwei benachbarten Reihen nicht überlappen und wobei in der überlappenden Periode Auswahlperioden der zwei benachbarten Reihen überlappen,
der Stromerzeugungsabschnitt (130) Einrichtungen zum sequentiellen Zuführen des Signalstroms (Ic) in Entsprechung zu zwei Anzeigebildpunkten in jeder Spalte der Anzeigebildpunkte in Entsprechung zu den zwei benachbarten Reihen zu der Stromschreibschaltung (140B) in einer Zeitreihe aufweist,
die Stromschreibschaltung (140B) eine Vielzahl von Stromhalteschaltungen (143) enthält, die in Übereinstimmung mit entsprechenden Spalten der Anzeigebildpunkte (EM) in jeder der Reihen vorgesehen sind, sequentiell den von dem Stromerzeugungsabschnitt (130) zugeführten Signalstrom (Ic) in Übereinstimmung mit dem Timing der Zeitreihen-Zufuhr halten und sequentiell als den Abstufungsstrom (Ipix) einen Strom mit einem Stromwert basierend auf dem Signalstrom (Ic) zu den zwei Anzeigebildpunkten der zwei benachbarten Reihen zuführen,
jede der Stromhalteschaltungen (143) zwei Strom-Halte-/Ausgabeabschnitte (143a, 143b) in Entsprechung zu den zwei Anzeigebildpunkten (EM) der zwei benachbarten Reihen enthält,
jeder der Strom-Halte-/Ausgabeabschnitte (143a, 143b) Einrichtungen enthält, die eine Ausgabe des Abstufungsstroms (Ipix) gleichzeitig zu der Zufuhr des Signalstroms (Ic) beginnen und den Abstufungsstrom (Ipix) über die Auswahlperiode jeder Reihe hinweg ausgeben.

2. Anzeigetreibervorrichtung nach Anspruch 1, wobei die Auswahlschaltung (120B) Einrichtungen zum sequentiellen Anlegen eines Auswahlsignals (Vsel) aufweist, die die Anzeigebildpunkte (EM) in jeder Reihe in den ausgewählten Zustand zu den Anzeigebildpunkten (EM) in jeder der Reihen des Anzeigepaneels (110B) mit den überlappenden Perioden setzen, um sequentiell die Anzeigebildpunkte (EM) in jeder der Reihen in den ausgewählten Zustand mit den überlappenden Perioden zu setzen.

3. Anzeigevorrichtung zum Anzeigen von Bildinformationen basierend auf Anzeigedaten, wobei die Anzeigevorrichtung umfasst:

ein Anzeigepaneel (110B), das eine Vielzahl von zweidimensional angeordneten Anzeigebildpunkten umfasst, und
die Anzeigetreibervorrichtung für das Treiben des Anzeigepaneels (110B) nach einem der Ansprüche 1 bis 2, wobei die Anzeigedaten zu der Abstufungssignal-Erzeugungseinheit (130) zugeführt werden.

4. Anzeigevorrichtung nach Anspruch 3, wobei das Anzeigepaneel eine Vielzahl von Abtastleitungen (SLq), die in einer Reihenrichtung angeordnet sind, und eine Vielzahl von Datenleitungen (DLja, DLjb), die in einer Spaltenrichtung angeordnet sind, sowie eine Vielzahl von Anzeigebildpunkten (EM), die in einer Matrixform in Nachbarschaft zu Kreuzungspunkten der Vielzahl von Abtastleitungen (SLq) und der Vielzahl von Datenleitungen (DLja, DLjb) angeordnet sind, umfasst, wobei die Vielzahl von Datenleitungen (DLja, DLjb) eine Vielzahl von Datenleitungsgruppen (DGj) enthält, von denen jede zwei Datenleitungen (DLja, DLjb) in Entsprechung zu ersten und zweiten Abtastleitungen (SLq) aufweist.

5. Anzeigevorrichtung nach Anspruch 4, wobei:

die Auswahlschaltung (120B) Einrichtungen zum sequentiellen Anlegen eines Auswahlsignals (Vsel) aufweist, die die Anzeigebildpunkte (EM) in Entsprechung zu jeder aus der Vielzahl von Abtastleitungen (SLq) in den ausgewählten Zustand mit den überlappenden Perioden setzt, um die Anzeigebildpunkte (EM) in Entsprechung zu jeder aus der Vielzahl von Abtastleitungen (SLq) in den ausgewählten Zustand mit den überlappenden Perioden zu setzen, und
die Stromschreibschaltung (140B) Einrichtungen zum sequentiellen Zuführen des Abstu-

fungsstroms (Ipix) zu jeder Datenleitung (DLja, DLjb) jeder Datenleitungsgruppe (DGj) mit den Überlappungsperioden mit dem Timing des Abtastsignals (Vsel) durch die Auswahlschaltung (120B) aufweist.

6. Anzeigevorrichtung nach Anspruch 4, wobei:

die Auswahlschaltung (120B) Einrichtungen zum sequentiellen Anlegen eines Auswahlsignals (Vsel) aufweist, die die Anzeigebildpunkte (EM) in Entsprechung zu jeder aus der Vielzahl von Abtastleitungen (SLq) in den ausgewählten Zustand mit den überlappenden Perioden setzen, um sequentiell die Anzeigebildpunkte (EM) in Entsprechung zu jeder aus der Vielzahl von Abtastleitungen (SLq) in den ausgewählten Zustand mit den überlappenden Perioden zu setzen,

die Abstufungssignal-Erzeugungsschaltung (130) Einrichtungen zum sequentiellen Zuführen des Abstufungssignals (Ic) in Entsprechung zu der Vielzahl von Anzeigebildpunkten (EM) in Entsprechung zu der Vielzahl von spezifischen Abtastleitungen (SLq) in jeder Datenleitung (DLja, DLjb) jeder Datenleitungsgruppe (DGj) zu der Stromschreibschaltung (140B) in einer Zeitreihe aufweist, und

die Stromschreibschaltung (140B) eine Vielzahl von Stromhalteschaltungen (143) aufweist, von denen jede in Übereinstimmung mit jeder Datenleitungsgruppe (DGj) vorgesehen ist, sequentiell das von der Abstufungssignal-Erzeugungsschaltung (130) zugeführte Abstufungssignal (Ic) in Übereinstimmung mit dem Timing der Zeitreihen-Zufuhr hält und sequentiell als den Abstufungsstrom (Ipix) einen Strom mit einem Stromwert in Entsprechung zu dem Abstufungssignal (Ic) zu jeder Datenleitung (DLja, DLjb) jeder Datenleitungsgruppe (DGj) mit dem Timing in Entsprechung zu dem Anlegen des Abtastsignals (Vsel) zuführt.

7. Anzeigevorrichtung nach Anspruch 6, wobei jede Stromhalteschaltung (143) zwei Strom-Halte-/Ausgabeabschnitte (143a, 143b) in Übereinstimmung mit jeder Datenleitung (DLja, DLjb) jeder Datenleitungsgruppe (DGj) enthält, wobei jeder der Strom-Halte-/Ausgabeabschnitte (143a, 143b) aufweist:

einen Signalverteilungsabschnitt (Tr46a, Tr47a, Tr46b, Tr47b), der sequentiell das Abstufungssignal (Ic) in Übereinstimmung mit jeder Datenleitung (DLja, DLjb) jeder Datenleitungsgruppe (DGj) mit dem Timing der Zeitreihen-Zufuhr verteilt,

einen Signalhalteabschnitt (Ce, Cf), der das durch den Signalverteilungsabschnitt verteilte Abstufungssignal (Ic) hält, und

einen Abstufungsstrom-Ausgabeabschnitt (Tr48a, Tr49a, Tr48b, Tr49b), der als den Abstufungsstrom (Ipix) einen Strom mit einem Stromwert basierend auf dem in dem Signalhalteabschnitt gehaltenen Abstufungssignal (Ic) ausgibt,

wobei eine Operation zum Halten des durch den Signalverteilungsabschnitt verteilten Abstufungssignals (Ic) in dem Signalhalteabschnitt in einem der Strom-Halte-/Ausgabeabschnitte und zum Ausgeben des Abstufungsstroms (Ipix) basierend auf dem Abstufungssignal (Ic) durch den Abstufungsstrom-Ausgabeabschnitt und eine Operation zum Ausgeben des Abstufungsstroms (Ipix) basierend auf dem in dem Signalhalteabschnitt gehaltenen Abstufungssignal (Ic) durch den Abstufungsstrom-Ausgabeabschnitt in dem anderen Strom-Halte-/Ausgabeabschnitt derart gesteuert werden, dass sie gleichzeitig in den überlappenden Perioden ausgeführt werden.

8. Treiberverfahren für eine Anzeigevorrichtung, die Bildinformationen basierend auf Anzeigedaten anzeigt, wobei die Anzeigevorrichtung eine Vielzahl von Abtastleitungen (SLq), die in einer Reihenrichtung angeordnet sind, und eine Vielzahl von Datenleitungen (DLja, DLjb), die in einer Spaltenrichtung angeordnet sind, sowie ein Anzeigepaneel (110b) mit einer Vielzahl von Anzeigebildpunkten (EM), die in Nachbarschaft zu Kreuzungspunkten der Vielzahl von Abtastleitungen (SLq) und der Vielzahl von Datenleitungen (DLja, DLjb) angeordnet sind und in einer Matrixform angeordnet sind, umfasst und wobei das Treiberverfahren wenigstens die folgenden Schritte umfasst:

Erzeugen eines Signalstroms (Ic), der eine Luminanzabstufung jedes Anzeigebildpunkts (EM) basierend auf den Anzeigedaten steuert,

Setzen der Anzeigebildpunkte (EM) in Entsprechung zu jedem aus der Vielzahl von Abtastleitungen (SLq) in einen ausgewählten Zustand während einer Auswahlperiode,

Abrufen des Signalstroms (Ic) in Entsprechung zu den Anzeigebildpunkten (EM) in Entsprechung zu jeder aus der Vielzahl von Abtastleitungen (SLq),

Erzeugen eines Abstufungsstroms (Ipix) mit einem Stromwert basierend auf dem Signalstrom (Ic), und Zuführen des Abstufungsstroms (Ipix) zu den Anzeigebildpunkten (EM) in Entsprechung zu jeder aus der Vielzahl von Abtastungsleitungen (SLq) in Übereinstimmung mit einer Auswahlperiode, und

Gestatten, dass die Anzeigebildpunkte (EM), in welchen der Abstufungsstrom (Ipix) zugeführt

und geschrieben wird, mit einer Anzeigeluminanz basierend auf einem Stromwert des Abstufungsstroms (Ipix) betrieben werden,
dadurch gekennzeichnet, dass
in dem Schritt zum Setzen der Anzeigebildpunkte die Auswahlperiode für das Setzen des ausgewählten Zustands auf eine Periode gesetzt ist, die eine nicht-überlappende Periode und eine überlappende Periode enthält, wobei in der nicht-überlappenden Periode Auswahlperioden von zwei benachbarten Reihen nicht überlappen und wobei in der überlappenden Periode Auswahlperioden der zwei benachbarten Reihen überlappen,
in dem Schritt zum Erzeugen eines Signalstroms (Ic) der Signalstrom (Ic) in Entsprechung zu zwei Anzeigebildpunkten in jeder Spalte der Anzeigebildpunkte in Entsprechung zu den benachbarten zwei sequentiell zuführenden Reihen sequentiell zu einer Stromschreibschaltung (140B) in einer Zeitreihe zugeführt wird,
die Stromschreibschaltung (140B) eine Vielzahl von Stromhalteschaltungen (143) enthält, die in Übereinstimmung mit entsprechenden Spalten der Anzeigebildpunkte (EM) in jeder der Reihen vorgesehen sind, sequentiell den von dem Stromerzeugungsabschnitt (130) zugeführten Signalstrom (Ic) in Übereinstimmung mit dem Timing der Zeitreihen-Zufuhr halten und sequentiell als den Abstufungsstrom (Ipix) einen Strom mit einem Stromwert basierend auf dem Signalstrom (Ic) zu den zwei Anzeigebildpunkten der zwei benachbarten Reihen zuführen,
jede der Stromhalteschaltungen (143) zwei Strom-Halte-/Ausgabeabschnitte (143a, 143b) in Entsprechung zu den zwei Anzeigebildpunkten (EM) der zwei benachbarten Reihen enthält, und
in dem Schritt zum Erzeugen eines Abstufungsstroms (Ipix) eine Ausgabe des Abstufungsstroms (Ipix) gleichzeitig zu der Zufuhr des Signalstroms (Ic) beginnt und der Abstufungsstrom (Ipix) über die Auswahlperiode jeder Reihe hinweg ausgegeben wird.

Revendications

1. Dispositif de commande d'affichage pour commander une pluralité de pixels d'affichage (EM) agencés de façon bidimensionnelle constituant un panneau d'affichage (110B), sur la base de données d'affichage, les pixels d'affichage (EM) étant disposés sur une pluralité de rangées et de colonnes, chacun des pixels d'affichage (EM) incluant un élément émetteur de lumière qui émet de la lumière au moyen d'un courant fourni, le dispositif de commande d'affichage comprenant au moins :

une section de génération de courant (130) qui génère un courant de signal (Ic) qui commande la gradation de luminance de chaque pixel d'affichage (EM), sur la base des données d'affichage ;
un circuit de sélection (120B) qui règle en séquence dans un état sélectionné chacun des pixels d'affichage (EM) correspondant à chaque rangée de ladite pluralité de rangées du panneau d'affichage (110B), pendant une période de sélection ; et
un circuit d'écriture de courant (140B) qui va chercher en séquence le courant de signal (Ic) correspondant aux pixels d'affichage (EM) dans chacune des rangées, et délivre aux pixels d'affichage (EM) dans chacune des rangées un courant de gradation (Ipix) ayant une valeur de courant basée sur le courant de signal (Ic), conformément à la période de sélection pour régler l'état sélectionné,
caractérisé en ce que
le circuit de sélection (120B) règle la période de sélection pour régler l'état sélectionné à une période incluant une période sans superposition et une période de superposition, dans lequel, pendant la période sans superposition, les périodes de sélection de deux rangées adjacentes ne sont pas superposées, et pendant la période de superposition, les périodes de sélection desdites deux rangées adjacentes sont superposées,
dans lequel la section de génération de courant (130) comporte un moyen pour délivrer en séquence en série dans le temps au circuit d'écriture de courant (140B) le courant de signal (Ic) correspondant aux deux pixels d'affichage dans chaque colonne de pixels d'affichage correspondant auxdites deux rangées adjacentes,
le circuit d'écriture de courant (140B) comporte une pluralité de circuits de retenue de courant (143) qui sont disposés conformément aux colonnes respectives de pixels d'affichage (EM) dans chacune des rangées, retiennent en séquence le courant de signal (Ic) délivré par la section de génération de courant (130) conformément au cadencement de la fourniture en série dans le temps, et fournissent en séquence auxdits deux pixels d'affichage desdites deux rangées adjacentes en tant que courant de gradation (Ipix) un courant ayant une valeur de courant basée sur le courant de signal (Ic),
dans lequel chacun des circuits de retenue de courant (143) comporte deux sections de retenue/sortie de courant (143a, 143b) correspondant auxdits deux pixels d'affichage (EM) desdites deux rangées adjacentes,
dans lequel chacune des sections de retenue/sortie de courant (143a, 143b) comporte un

moyen qui démarre la sortie du courant de gradation (Ipix) en même temps que le courant de signal (Ic) est délivré, et fournit en sortie le courant de gradation (Ipix) pendant la période de sélection de chaque rangée.

2. Dispositif de commande d'affichage selon la revendication 1, dans lequel le circuit de sélection (120B) comporte un moyen pour appliquer en séquence aux pixels d'affichage (EM) dans chacune des rangées du panneau d'affichage (110B) un signal de sélection (Vsel) qui règle dans l'état sélectionné les pixels d'affichage (EM) dans chaque rangée, avec les périodes de superposition, de façon à régler en séquence dans l'état sélectionné les pixels d'affichage (EM) dans chacune des rangées avec les périodes de superposition.

3. Dispositif d'affichage pour afficher des informations d'image sur la base de données d'affichage, le dispositif d'affichage comprenant :

un panneau d'affichage (110B) comprenant une pluralité de pixels d'affichage agencés de façon bidimensionnelle ; et
le dispositif de commande d'affichage pour commander ledit panneau d'affichage (110B) selon l'une quelconque des revendications 1 ou 2, dans lequel les données d'affichage sont délivrées à ladite unité de génération de signal de gradation (130).

4. Dispositif d'affichage selon la revendication 3, dans lequel le panneau d'affichage comprend une pluralité de lignes de balayage (SLq) agencées dans la direction des rangées et une pluralité de lignes de données (DLja, DLjb) agencées dans la direction des colonnes, et une pluralité de pixels d'affichage (EM) agencés sous forme matricielle au voisinage des intersections de la pluralité de lignes de balayage (SLq) et de la pluralité de lignes de données (DLja, DLjb), dans lequel la pluralité de lignes de données (DLja, DLjb) comporte une pluralité de groupes de lignes de données (DGj), dont chacun comporte deux lignes de données (DLja, DLjb) correspondant à des première et seconde lignes de balayage (SLq).

5. Dispositif d'affichage selon la revendication 4, dans lequel
le circuit de sélection (120B) comporte un moyen pour appliquer en séquence un signal de sélection (Vsel) qui règle dans l'état sélectionné les pixels d'affichage (EM) correspondant à chaque ligne de la pluralité de lignes de balayage (SLq), avec les périodes de superposition pour régler en séquence dans l'état sélectionné les pixels d'affichage (EM) correspondant à chaque ligne de la pluralité de lignes de balayage (SLq) avec les périodes de superposition, et le circuit d'écriture de courant (140B) comporte un moyen pour délivrer en séquence le courant de gradation (Ipix) à chaque ligne de données (DLja, DLjb) de chaque groupe de lignes de données (DGj), avec les périodes de superposition au moment de l'application du signal de balayage (Vsel) par le circuit de sélection (120B).

6. Dispositif d'affichage selon la revendication 4, dans lequel
le circuit de sélection (120B) comporte un moyen pour appliquer en séquence un signal de sélection (Vsel) qui règle dans l'état sélectionné les pixels d'affichage (EM) correspondant à chaque ligne de la pluralité de lignes de balayage (SLq), avec les périodes de superposition pour régler en séquence dans l'état sélectionné les pixels d'affichage (EM) correspondant à chaque ligne de la pluralité de lignes de balayage (SLq) avec les périodes de superposition,
le circuit de génération de signal de gradation (130) comporte un moyen pour délivrer en séquence en série dans le temps au circuit d'écriture de courant (140B) le signal de gradation (Ic) correspondant à la pluralité de pixels d'affichage (EM) correspondant à la pluralité de lignes de balayage spécifique (SLq) dans chaque ligne de données (DLja, DLjb) de chaque groupe de lignes de données (DGj), et
le circuit d'écriture de courant (140B) comporte une pluralité de circuits de retenue de courant (143), chacun d'entre eux étant fourni conformément à chaque groupe de lignes de données (DGj), retient en séquence le signal de gradation (Ic) délivré par le circuit de génération de signal de gradation (130) conformément au cadencement de la fourniture en série dans le temps, et fournit en séquence à chaque ligne de données (DLja, DLjb) de chaque groupe de lignes de données (DGj), en tant que courant de gradation (Ipix), un courant ayant une valeur de courant correspondant au signal de gradation (Ic), au moment correspondant à l'application du signal de balayage (Vsel).

7. Dispositif d'affichage selon la revendication 6, dans lequel chaque circuit de retenue de courant (143) comporte deux sections de retenue/sortie de courant (143a, 143b) conformément à chaque ligne de données (DLja, DLjb) de chaque groupe de lignes de données (DGj), chacune des sections de retenue/sortie de courant (143a, 143b) comportant :

une section de distribution de signal (Tr46a, Tr47a, Tr46b, Tr47b) qui distribue en séquence le signal de gradation (Ic) conformément à chaque ligne de données (DLja, DLjb) de chaque groupe de lignes de données (DGj), au moment de la fourniture en série dans le temps ;
une section de retenue de signal (Ce, Cf) qui retient le signal de gradation (Ic) distribué par la

section de distribution de signal ; et
une section de sortie de courant de gradation (Tr48a, Tr49a, Tr48b, Tr49b) qui délivre en sortie en tant que courant de gradation (Ipix) un courant ayant une valeur de courant basée sur le signal de gradation (Ic) retenu dans la section de retenue de signal,
dans lequel l'opération de retenue du signal de gradation (Ic) distribué par la section de distribution de signal dans la section de retenue de signal dans une des sections de retenue/sortie de courant et de fourniture en sortie du courant de gradation (Ipix) basé sur le signal de gradation (Ic) par la section de sortie de courant de gradation, et l'opération de fourniture en sortie du courant de gradation (Ipix) basé sur le signal de gradation (Ic) retenu dans la section de retenue de signal par la section de sortie de courant de gradation dans l'autre section de retenue/sortie de courant, sont commandées pour être exécutées simultanément pendant les périodes de superposition.

8. Procédé de commande d'un dispositif d'affichage qui affiche des informations d'image sur la base de données d'affichage, le dispositif d'affichage comportant une pluralité de lignes de balayage (SLq) agencées dans la direction des rangées et une pluralité de lignes de données (DLja, DLjb) agencées dans la direction des colonnes, et un panneau d'affichage (110B) comportant une pluralité de pixels d'affichage (EM) qui sont agencées au voisinage des intersections de la pluralité de lignes de balayage (SLq) et de la pluralité de lignes de données (DLja, DLjb), et agencées sous forme matricielle, le procédé de commande comprenant au moins les étapes consistant à :

générer un courant de signal (Ic) qui commande la gradation de luminance de chaque pixel d'affichage (EM), sur la base des données d'affichage ;
régler dans un état sélectionné les pixels d'affichage (EM) correspondant à chaque rangée de la pluralité de lignes de balayage (SLq), pendant une période de sélection ;
aller chercher le courant de signal (Ic) correspondant aux pixels d'affichage (EM) correspondant à chaque ligne de la pluralité de lignes de balayage (SLq),
générer un courant de gradation (Ipix) ayant une valeur de courant basée sur le courant de signal (Ic), et délivrer le courant de gradation (Ipix) aux pixels d'affichage (EM) correspondant à chaque ligne de la pluralité de lignes de balayage (Slq) conformément à une période de sélection ; et
permettre aux pixels d'affichage (EM) dans lesquels est fourni et écrit le courant de gradation (Ipix) de fonctionner avec une luminance d'affichage basé sur la valeur de courant du courant de gradation (Ipix),
caractérisé en ce que
à l'étape de réglage des pixels d'affichage, la période de sélection pour régler l'état sélectionné est réglée à une période incluant une période sans superposition et une période de superposition, dans lequel, pendant la période sans superposition, les périodes de sélection de deux rangées adjacentes ne sont pas superposées, et pendant la période de superposition, les périodes de sélection desdites deux rangées adjacentes sont superposées,
dans lequel à l'étape de génération d'un courant de signal (Ic), le courant de signal (Ic) correspondant aux deux pixels d'affichage dans chaque colonne de pixels d'affichage correspondant auxdites deux rangées adjacentes de fourniture en séquence est fourni en séquence à un circuit d'écriture de courant (140B) en série dans le temps,
le circuit d'écriture de courant (140B) incluant une pluralité de circuits de retenue de courant (143) qui sont disposés conformément aux colonnes respectives de pixels d'affichage (EM) dans chacune des rangées, retiennent en séquence le courant de signal (Ic) délivré par la section de génération de courant (130) conformément au cadencement de la fourniture en série dans le temps, et fournissent en séquence auxdits deux pixels d'affichage desdites deux rangées adjacentes en tant que courant de gradation (Ipix) un courant ayant une valeur de courant basée sur le courant de signal (Ic),
dans lequel chacun des circuits de retenue de courant (143) comporte deux sections de retenue/sortie de courant (143a, 143b) correspondant auxdits deux pixels d'affichage (EM) desdites deux rangées adjacentes, et
dans lequel à l'étape de génération d'un courant de gradation (Ipix), la sortie du courant de gradation (Ipix) commence en même temps que le courant de signal (Ic) est délivré, et le courant de gradation (Ipix) est fourni en sortie pendant la période de sélection de chaque rangée.

FIG.1

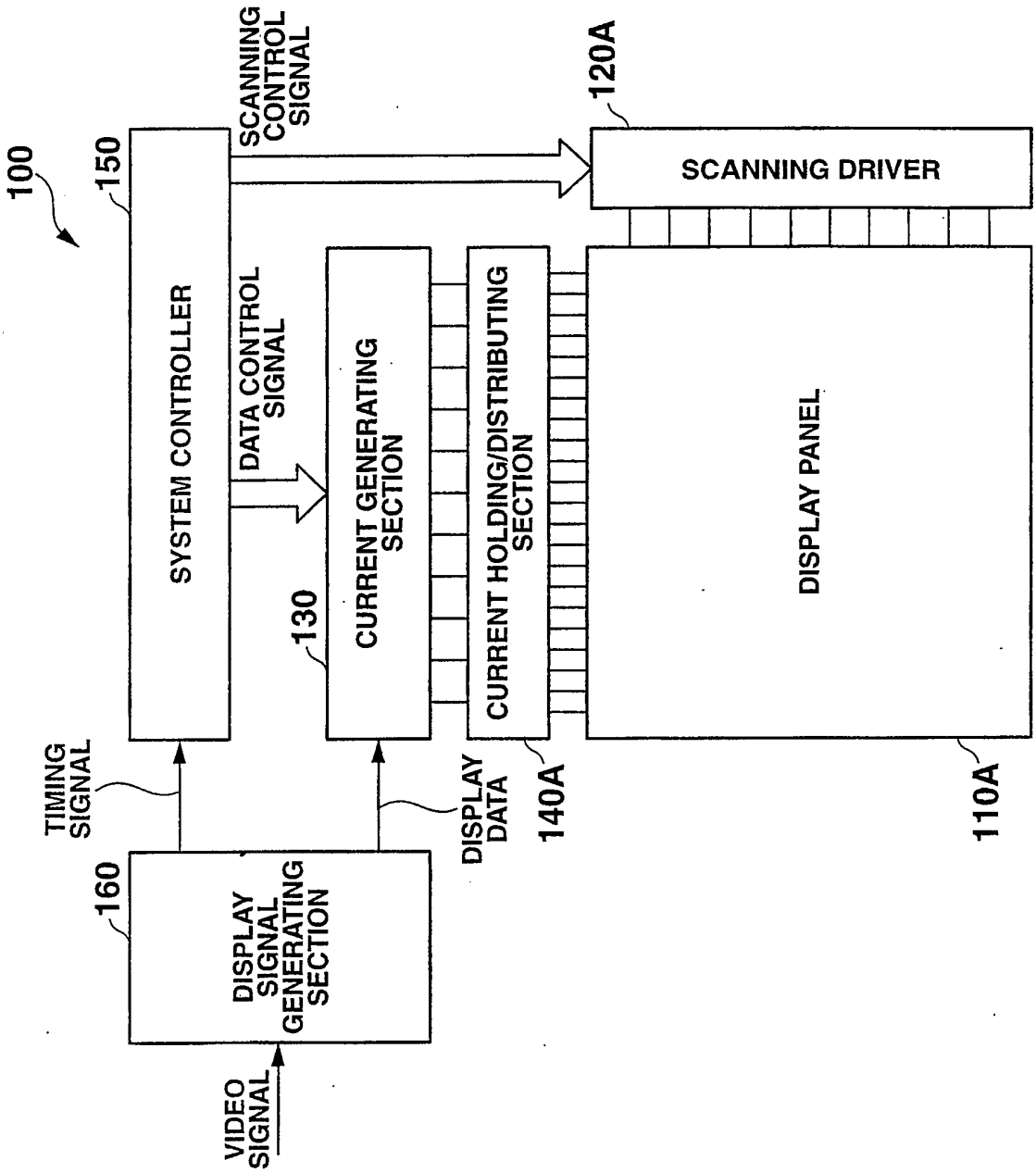

100
150
SYSTEM CONTROLLER
SCANNING CONTROL SIGNAL
120A
SCANNING DRIVER
DATA CONTROL SIGNAL
130
CURRENT GENERATING SECTION
CURRENT HOLDING/DISTRIBUTING SECTION
DISPLAY PANEL
TIMING SIGNAL
DISPLAY DATA
140A
110A
160
DISPLAY SIGNAL GENERATING SECTION
VIDEO SIGNAL

FIG.2

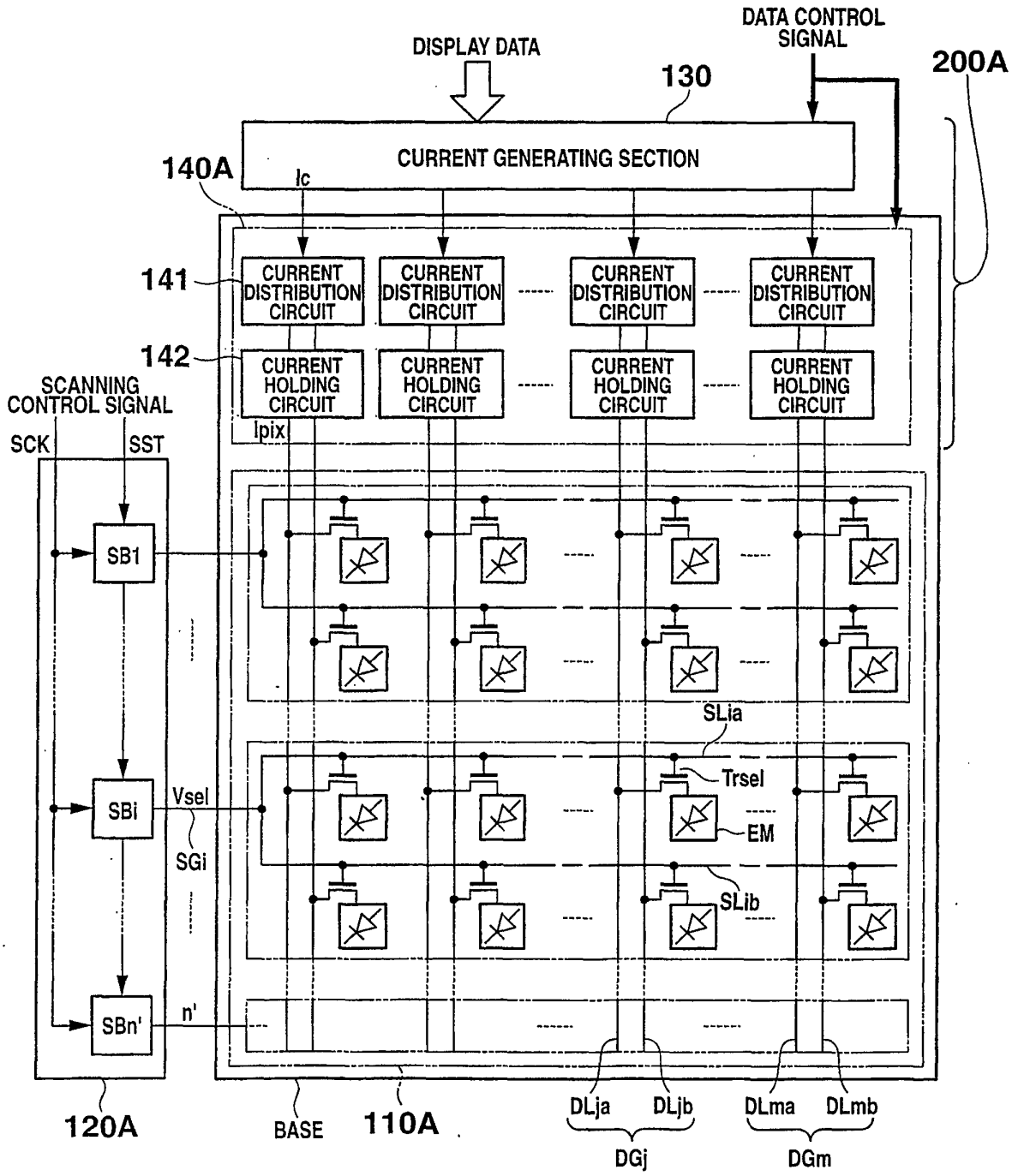

DISPLAY DATA
DATA CONTROL SIGNAL
200A
130
CURRENT GENERATING SECTION
140A
Ic
141
CURRENT DISTRIBUTION CIRCUIT
142
CURRENT HOLDING CIRCUIT
Ipix
SCANNING CONTROL SIGNAL
SCK
SST
SB1
SBi
SBn'
Vsel
SGi
n'
SLia
Trsel
EM
SLib
120A
BASE
110A
DLja
DLjb
DGj
DLma
DLmb
DGm

FIG.3

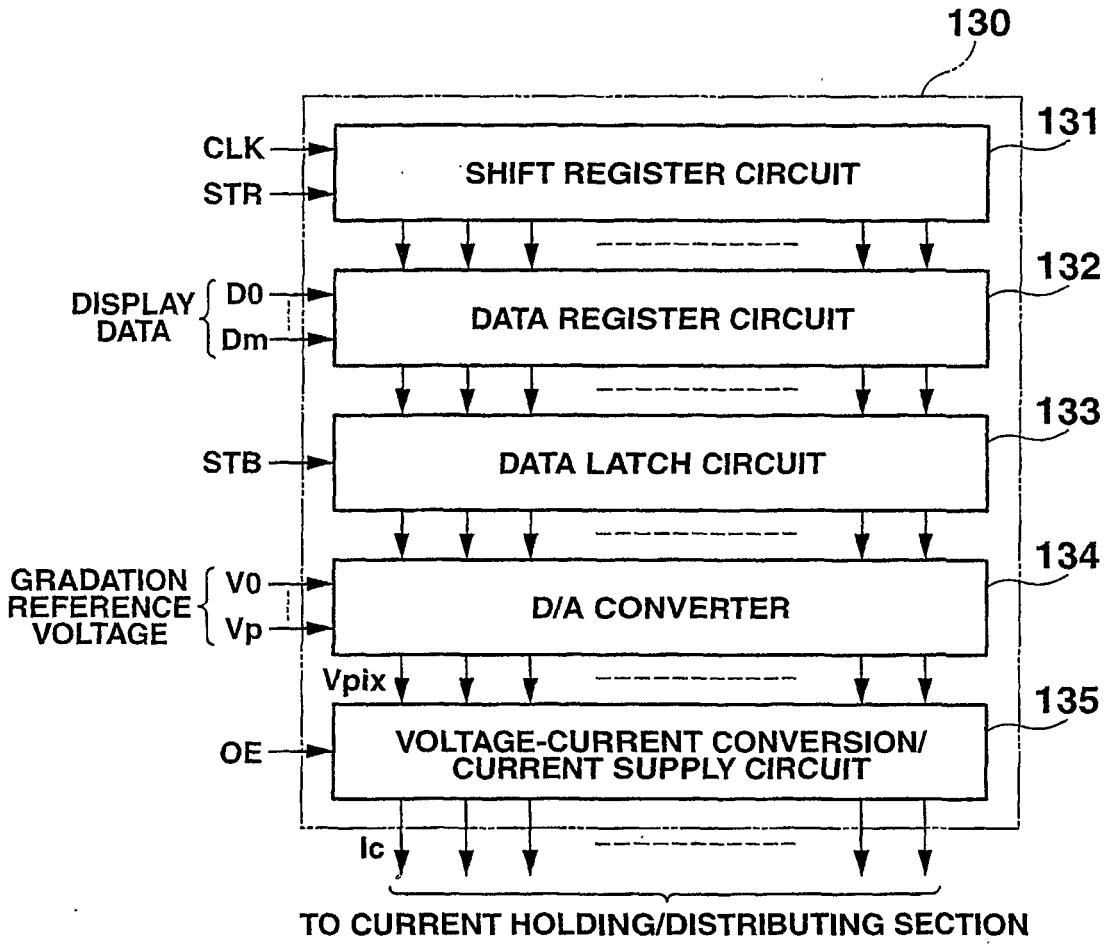

130
131
132
133
134
135
CLK
STR
SHIFT REGISTER CIRCUIT
DISPLAY DATA
D0
Dm
DATA REGISTER CIRCUIT
STB
DATA LATCH CIRCUIT
GRADATION REFERENCE VOLTAGE
V0
Vp
D/A CONVERTER
Vpix
OE
VOLTAGE-CURRENT CONVERSION/ CURRENT SUPPLY CIRCUIT
Ic
TO CURRENT HOLDING/DISTRIBUTING SECTION

FIG.4

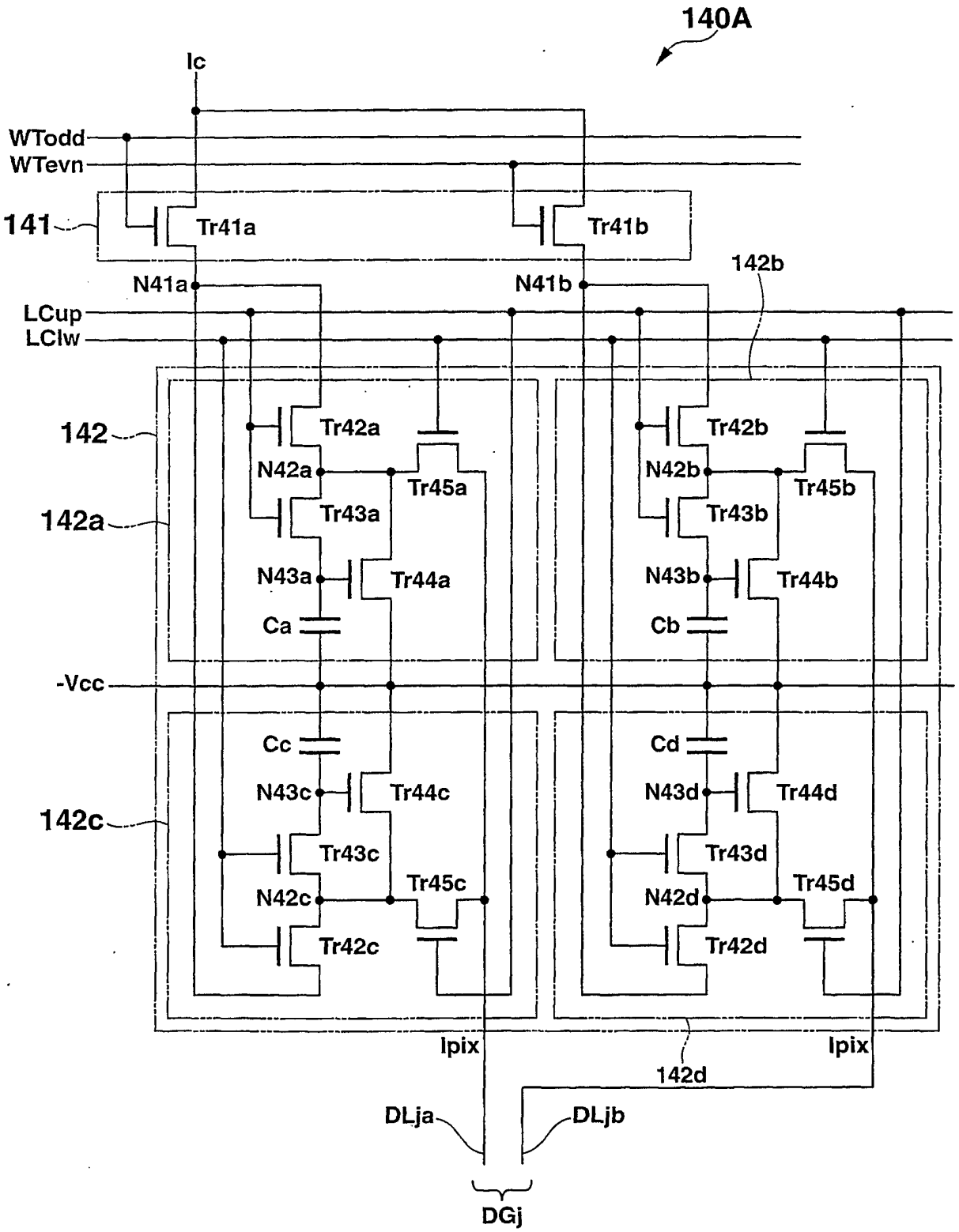

140A
Ic
WTodd
WTevn
141
Tr41a
Tr41b
N41a
N41b
142b
LCup
LClw
142
142a
Tr42a
N42a
Tr45a
Tr43a
N43a
Tr44a
Ca
Tr42b
N42b
Tr45b
Tr43b
N43b
Tr44b
Cb
-Vcc
142c
Cc
N43c
Tr44c
Tr43c
N42c
Tr45c
Tr42c
Cd
N43d
Tr44d
Tr43d
N42d
Tr45d
Tr42d
Ipix
Ipix
142d
DLja
DLjb
DGj

FIG.5B

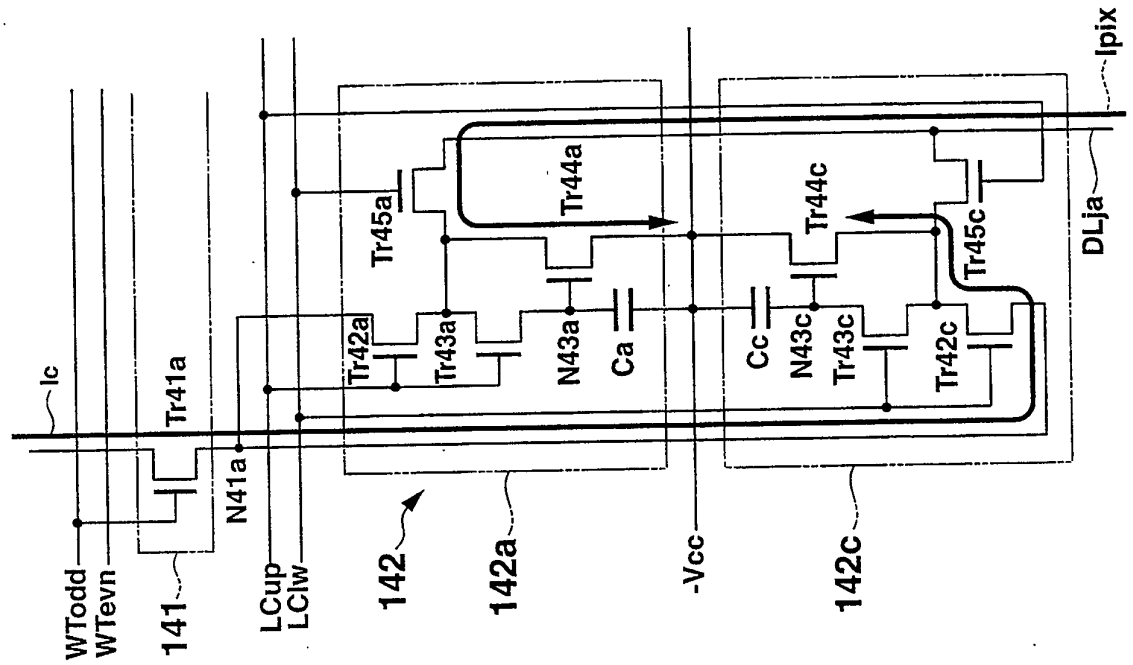

Ic
Tr41a
N41a
WTodd
WTevn
141
LCup
LClw
142
142a
-Vcc
142c
Tr45a
Tr44a
Tr42a
Tr43a
N43a
Ca
Cc
N43c
Tr43c
Tr42c
Tr44c
Tr45c
DLja
Ipix

FIG.5A

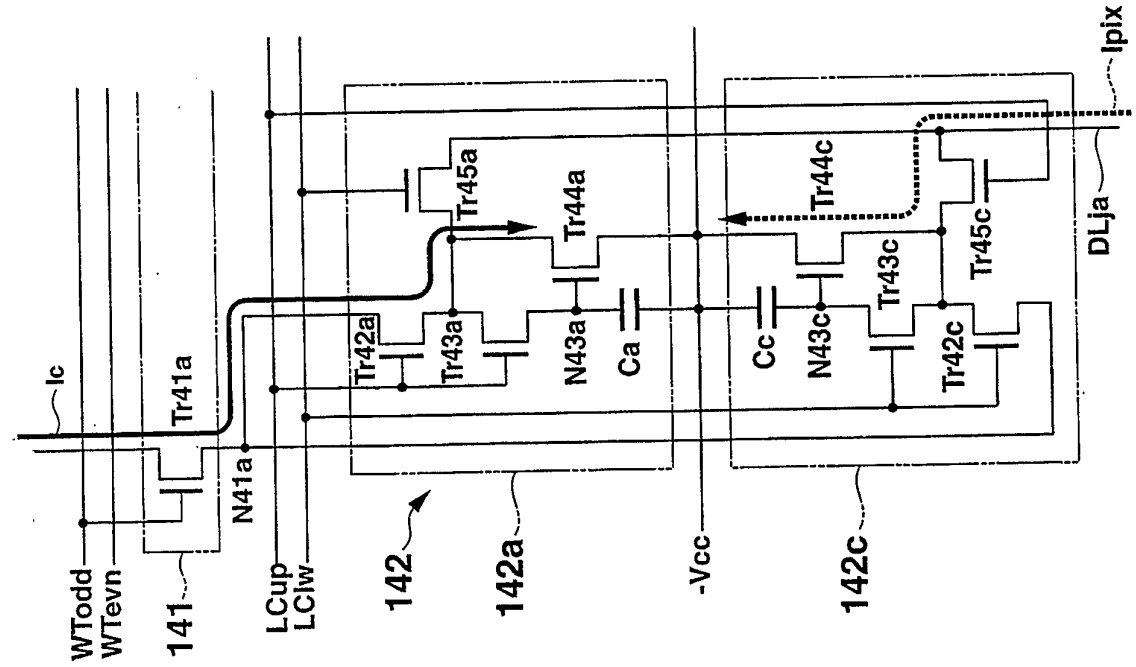

Ic
Tr41a
N41a
WTodd
WTevn
141
LCup
LClw
142
142a
-Vcc
142c
Tr45a
Tr44a
Tr42a
Tr43a
N43a
Ca
Cc
N43c
Tr43c
Tr42c
Tr44c
Tr45c
DLja
Ipix

FIG.6

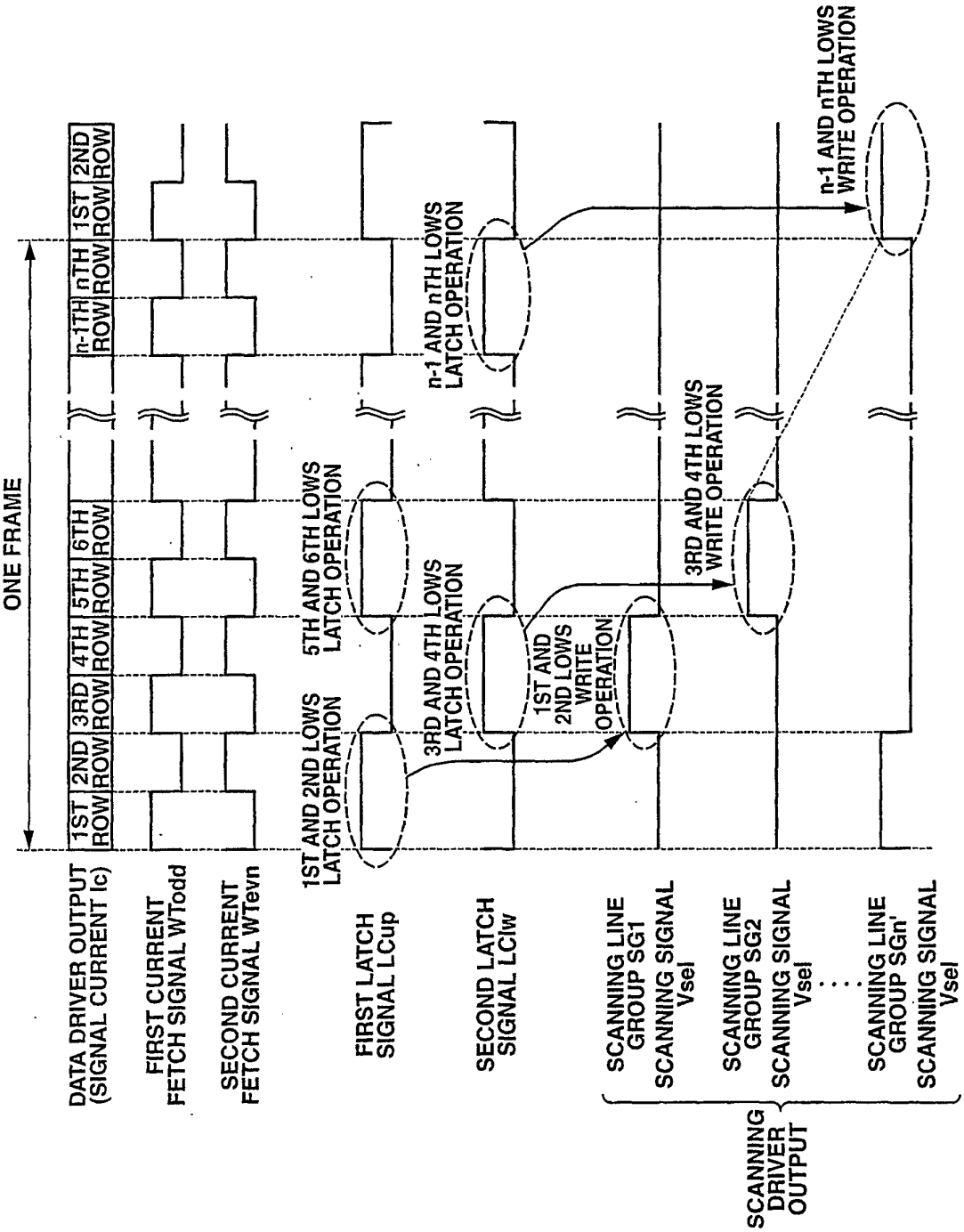

ONE FRAME
1ST ROW
2ND ROW
3RD ROW
4TH ROW
5TH ROW
6TH ROW
n-1TH ROW
nTH ROW
1ST ROW
2ND ROW
DATA DRIVER OUTPUT (SIGNAL CURRENT Ic)
FIRST CURRENT FETCH SIGNAL WTodd
SECOND CURRENT FETCH SIGNAL WTevn
1ST AND 2ND LOWS LATCH OPERATION
5TH AND 6TH LOWS LATCH OPERATION
3RD AND 4TH LOWS LATCH OPERATION
n-1 AND nTH LOWS LATCH OPERATION
FIRST LATCH SIGNAL LCup
SECOND LATCH SIGNAL LCIw
1ST AND 2ND LOWS WRITE OPERATION
3RD AND 4TH LOWS WRITE OPERATION
n-1 AND nTH LOWS WRITE OPERATION
SCANNING LINE GROUP SG1
SCANNING SIGNAL Vsel
SCANNING LINE GROUP SG2
SCANNING SIGNAL Vsel
SCANNING LINE GROUP SGn'
SCANNING SIGNAL Vsel
SCANNING DRIVER OUTPUT

FIG.7

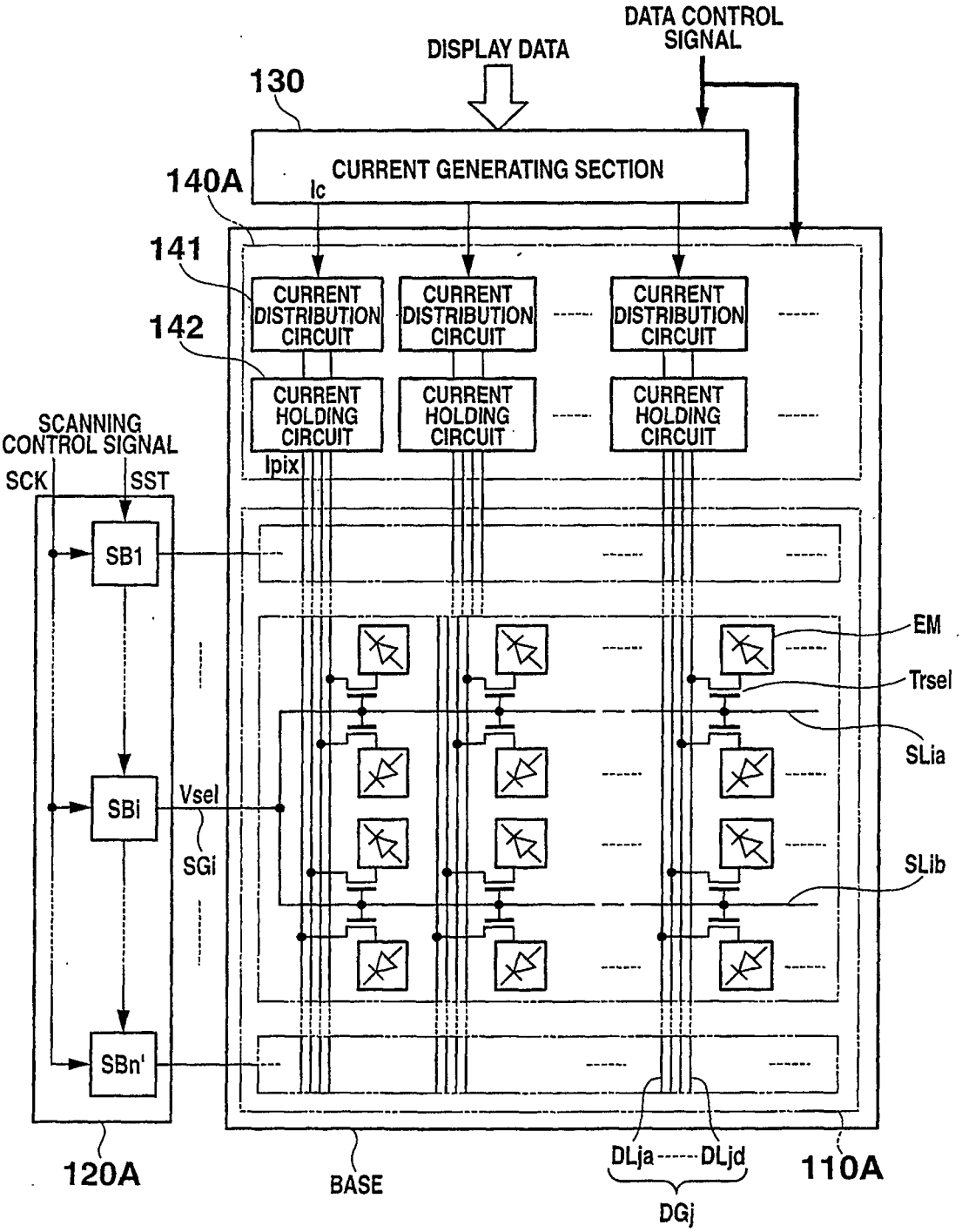

DATA CONTROL SIGNAL
DISPLAY DATA
130
CURRENT GENERATING SECTION
140A
Ic
141
142
CURRENT DISTRIBUTION CIRCUIT
CURRENT HOLDING CIRCUIT
Ipix
SCANNING CONTROL SIGNAL
SCK
SST
SB1
SBi
SBn'
Vsel
SGi
EM
Trsel
SLia
SLib
DLja
DLjd
DGj
120A
BASE
110A

FIG.8

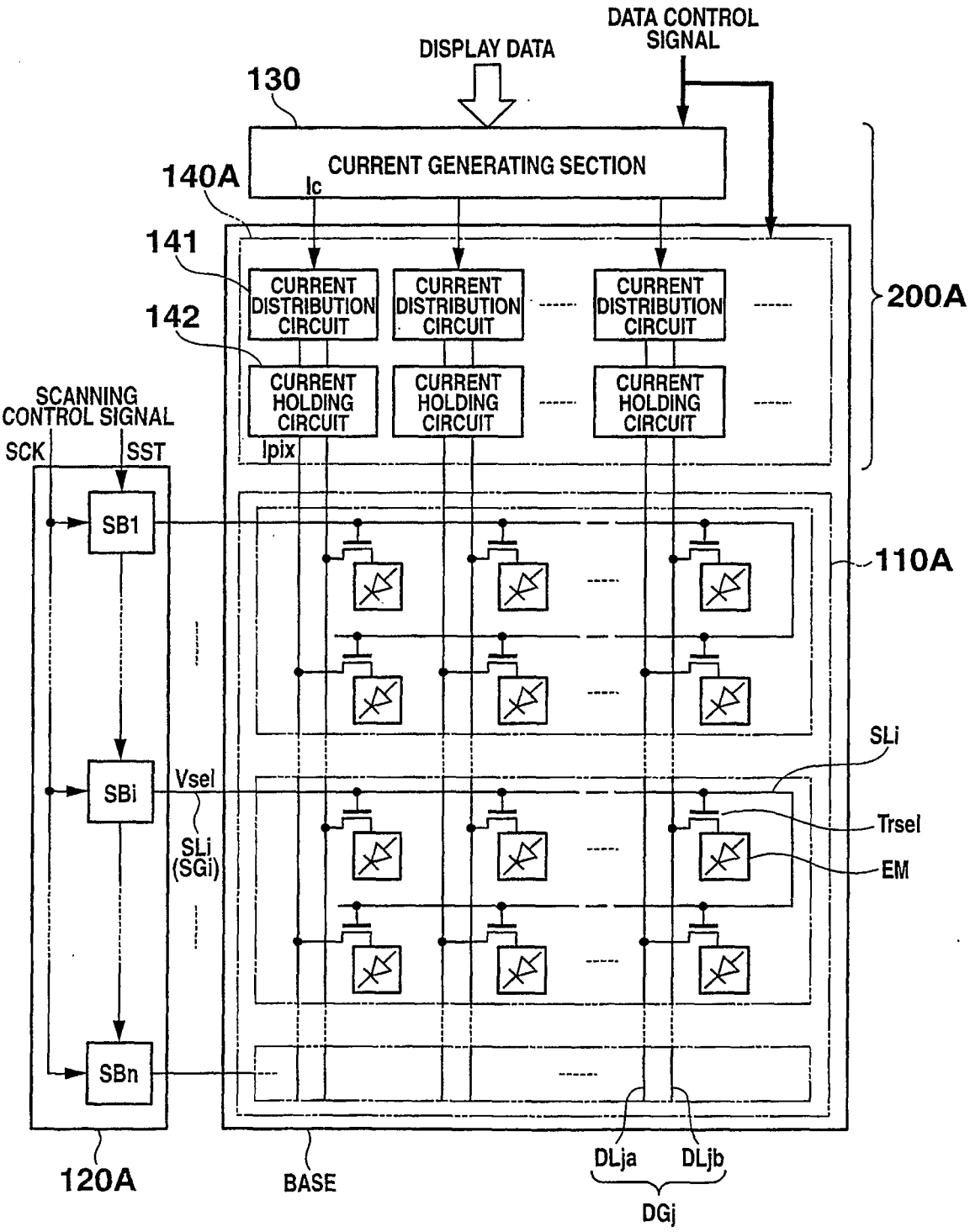

DISPLAY DATA
DATA CONTROL SIGNAL
130
CURRENT GENERATING SECTION
140A
Ic
141
142
CURRENT DISTRIBUTION CIRCUIT
CURRENT HOLDING CIRCUIT
200A
SCANNING CONTROL SIGNAL
SCK
SST
Ipix
SB1
SBi
SBn
110A
Vsel
SLi (SGi)
SLi
Trsel
EM
120A
BASE
DLja
DLjb
DGj

FIG.9

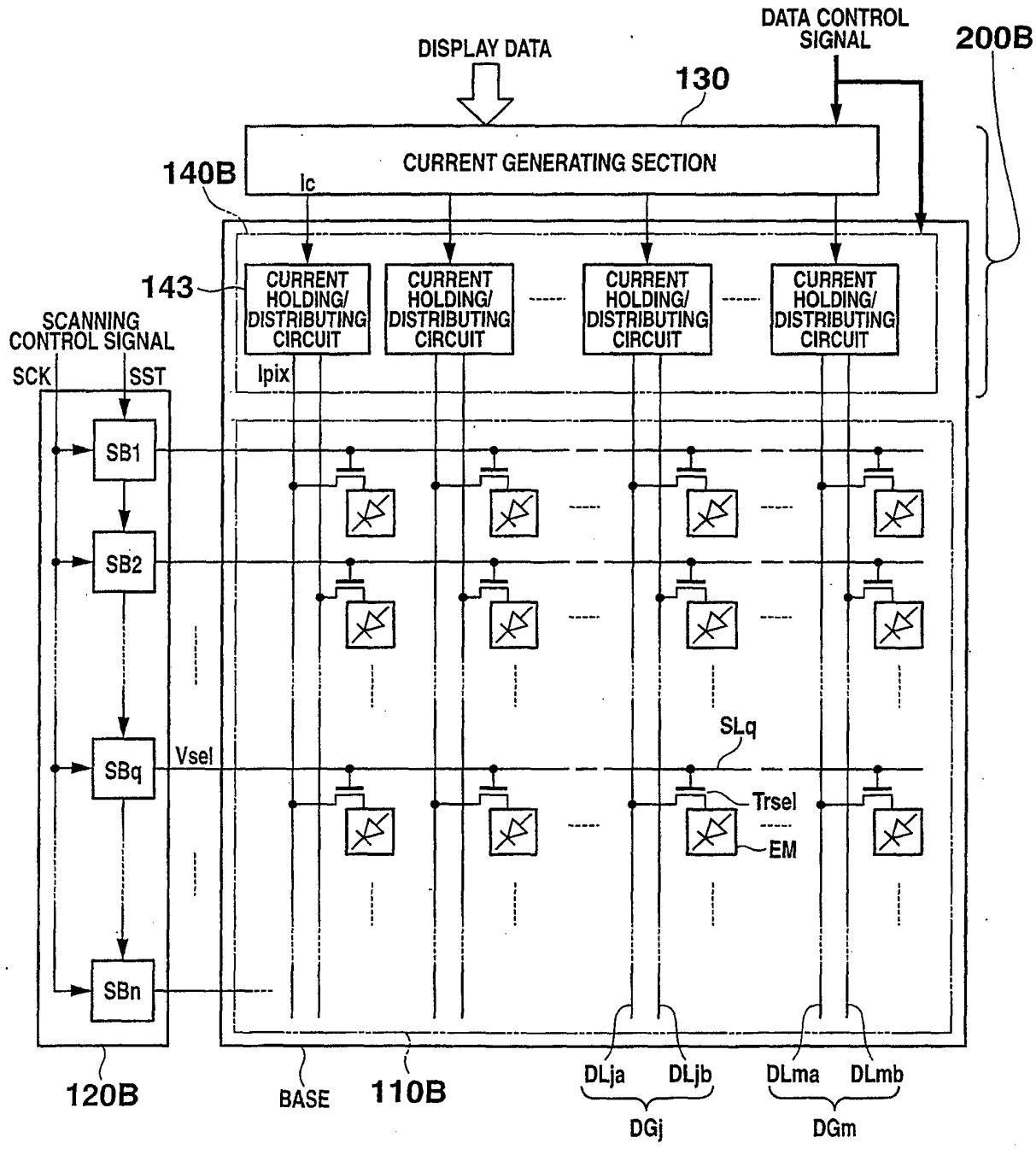

DISPLAY DATA
DATA CONTROL SIGNAL
200B
130
CURRENT GENERATING SECTION
140B
Ic
143
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
SCANNING CONTROL SIGNAL
SCK
SST
Ipix
SB1
SB2
SBq
SBn
Vsel
SLq
Trsel
EM
DLja
DLjb
DLma
DLmb
DGj
DGm
120B
BASE
110B

FIG.10

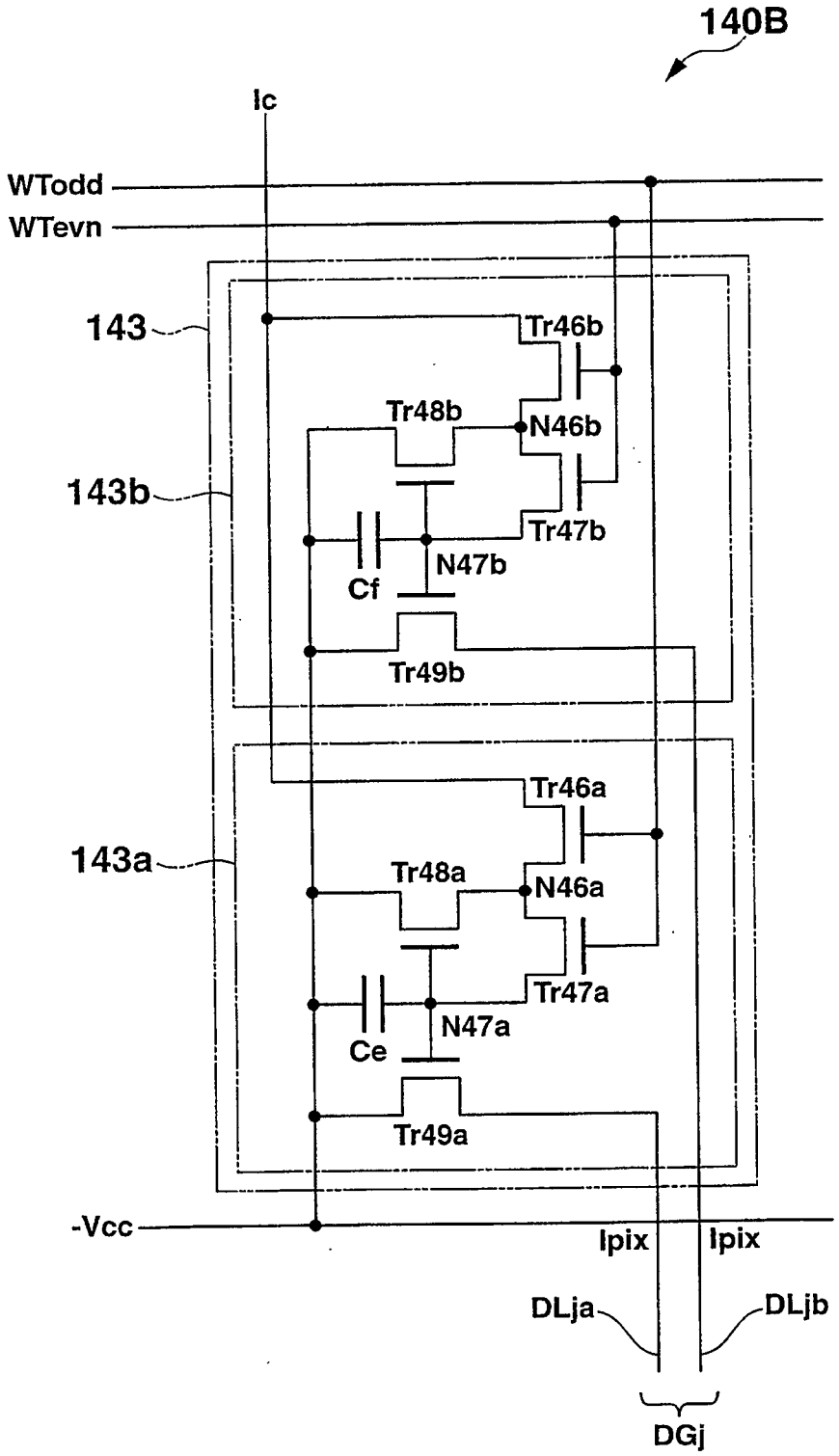

140B
Ic
WTodd
WTevn
143
143b
143a
Tr46b
Tr48b
N46b
Tr47b
Cf
N47b
Tr49b
Tr46a
Tr48a
N46a
Tr47a
Ce
N47a
Tr49a
-Vcc
Ipix
Ipix
DLja
DLjb
DGj

FIG.11B

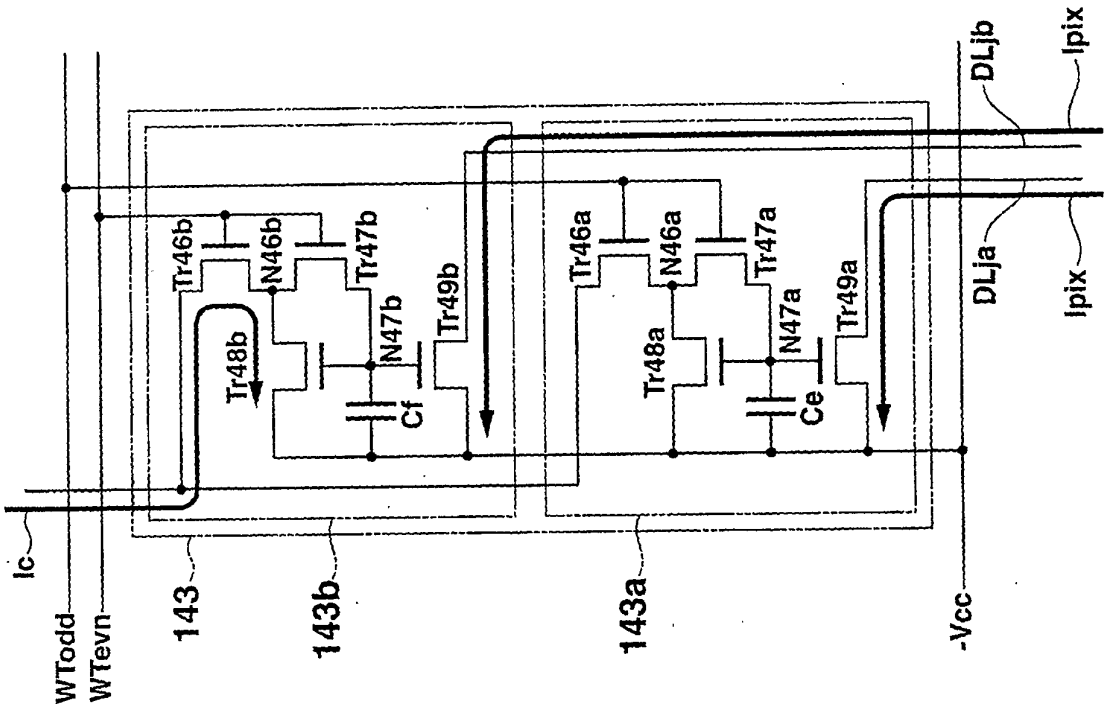


FIG.11A

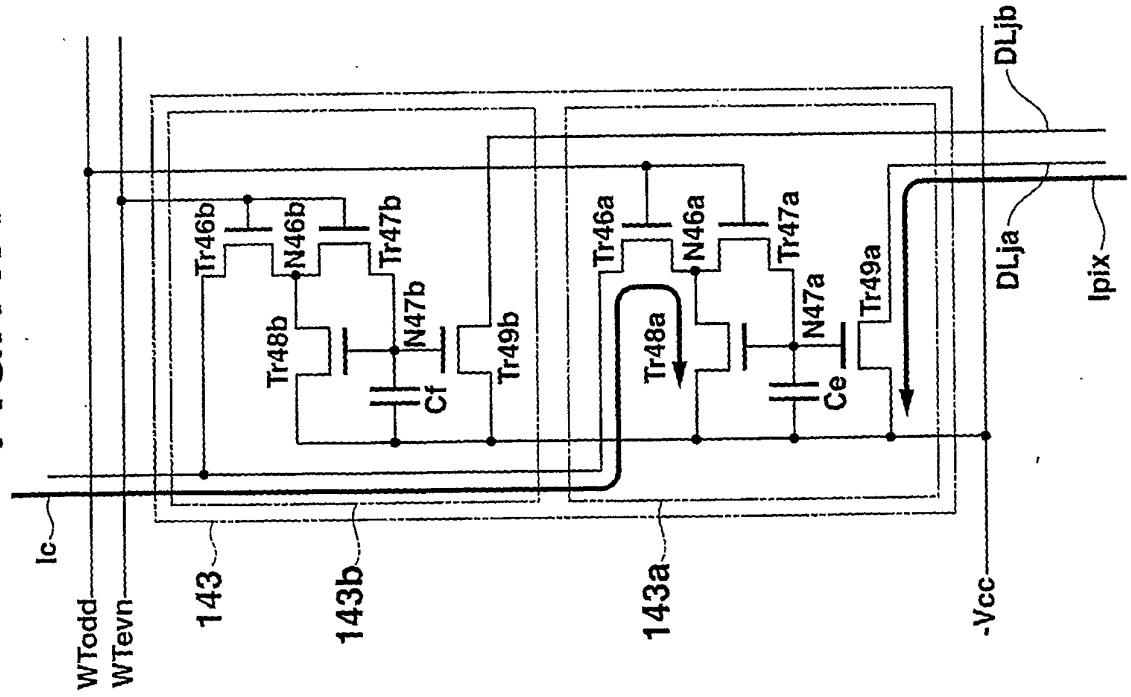


FIG.12

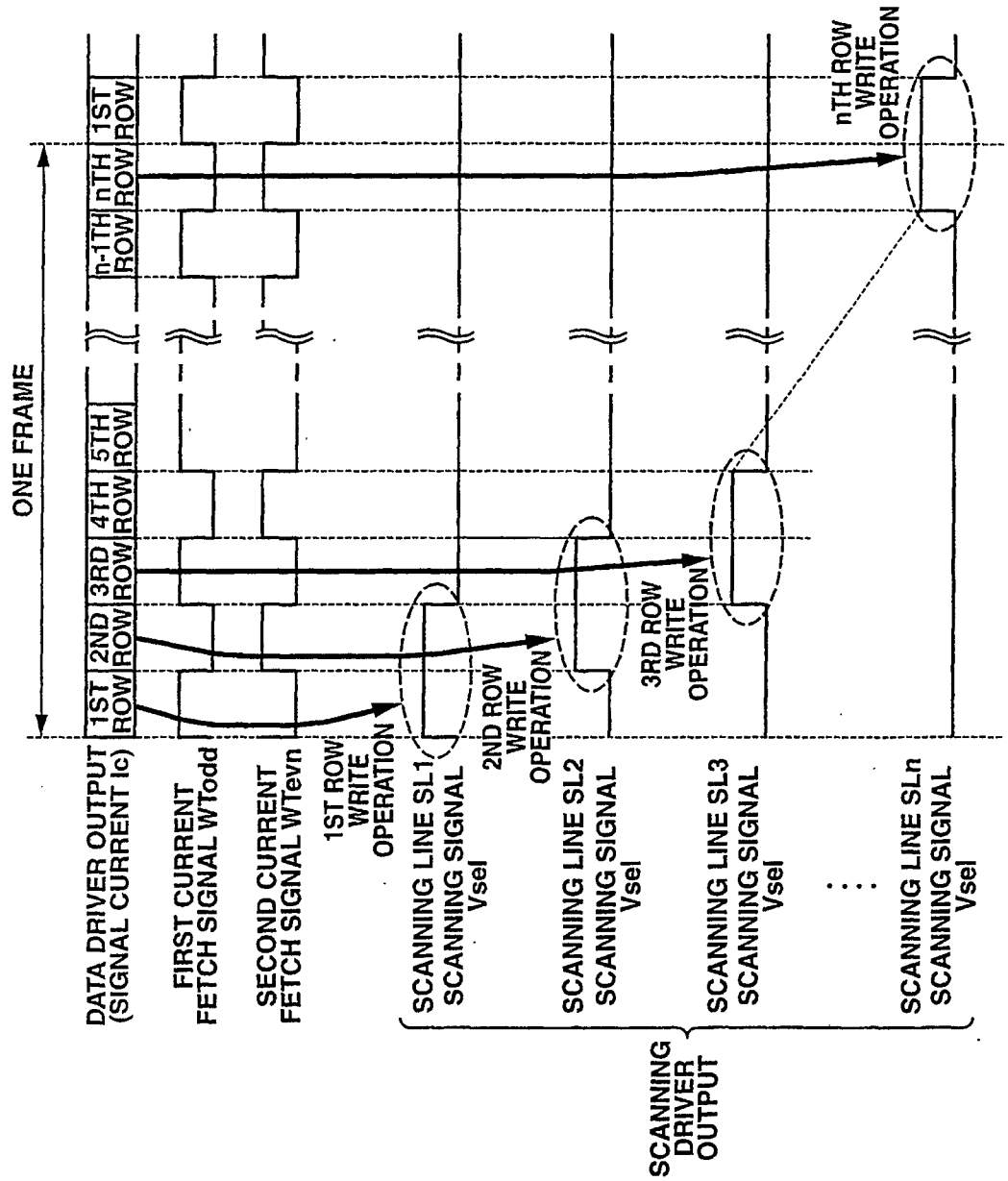

ONE FRAME
1ST ROW
2ND ROW
3RD ROW
4TH ROW
5TH ROW
n-1TH ROW
nTH ROW
1ST ROW
DATA DRIVER OUTPUT (SIGNAL CURRENT Ic)
FIRST CURRENT FETCH SIGNAL WTodd
SECOND CURRENT FETCH SIGNAL WTevn
1ST ROW WRITE OPERATION
2ND ROW WRITE OPERATION
3RD ROW WRITE OPERATION
nTH ROW WRITE OPERATION
SCANNING DRIVER OUTPUT
SCANNING LINE SL1 SCANNING SIGNAL Vsel
SCANNING LINE SL2 SCANNING SIGNAL Vsel
SCANNING LINE SL3 SCANNING SIGNAL Vsel
SCANNING LINE SLn SCANNING SIGNAL Vsel

FIG.13

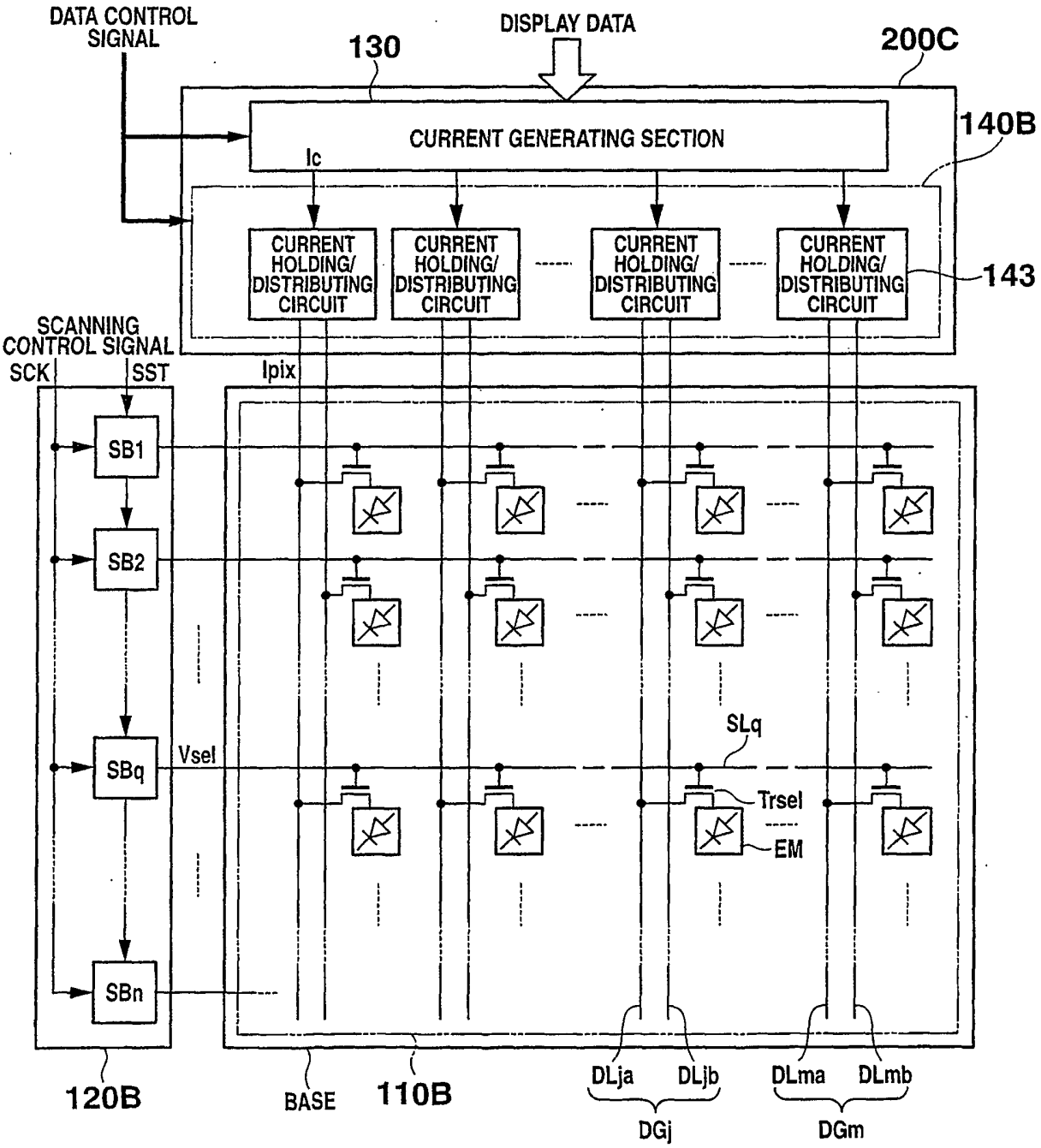

DATA CONTROL SIGNAL
DISPLAY DATA
130
200C
140B
CURRENT GENERATING SECTION
Ic
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
CURRENT HOLDING/ DISTRIBUTING CIRCUIT
143
SCANNING CONTROL SIGNAL
SCK
SST
Ipix
SB1
SB2
SBq
SBn
Vsel
SLq
Trsel
EM
120B
BASE
110B
DLja
DLjb
DLma
DLmb
DGj
DGm

FIG.14

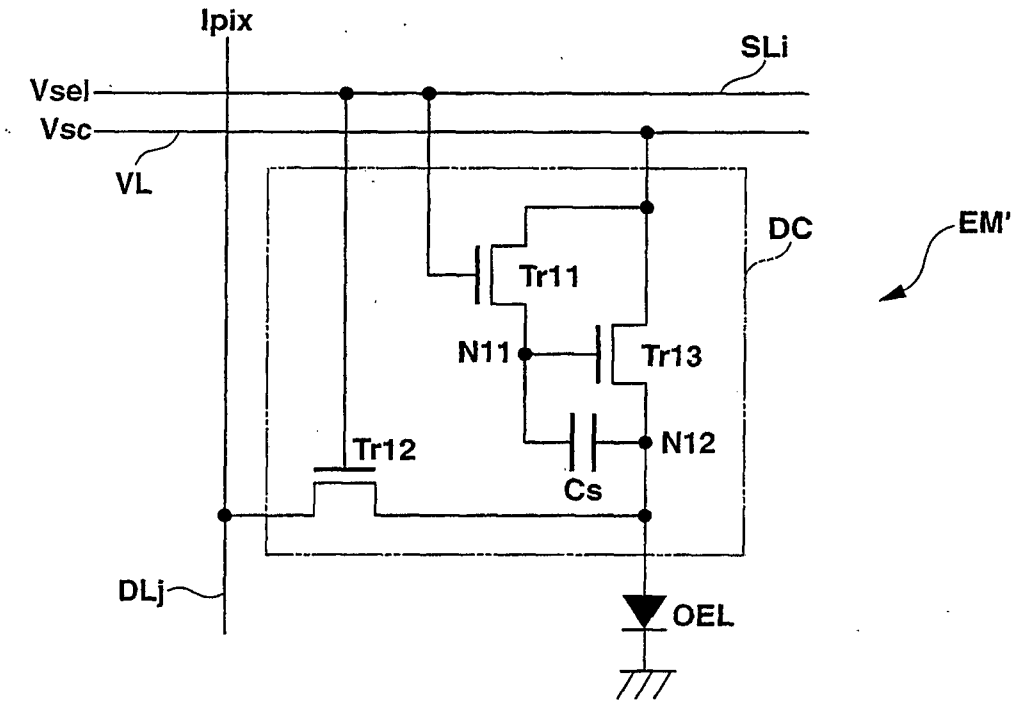


FIG.15A

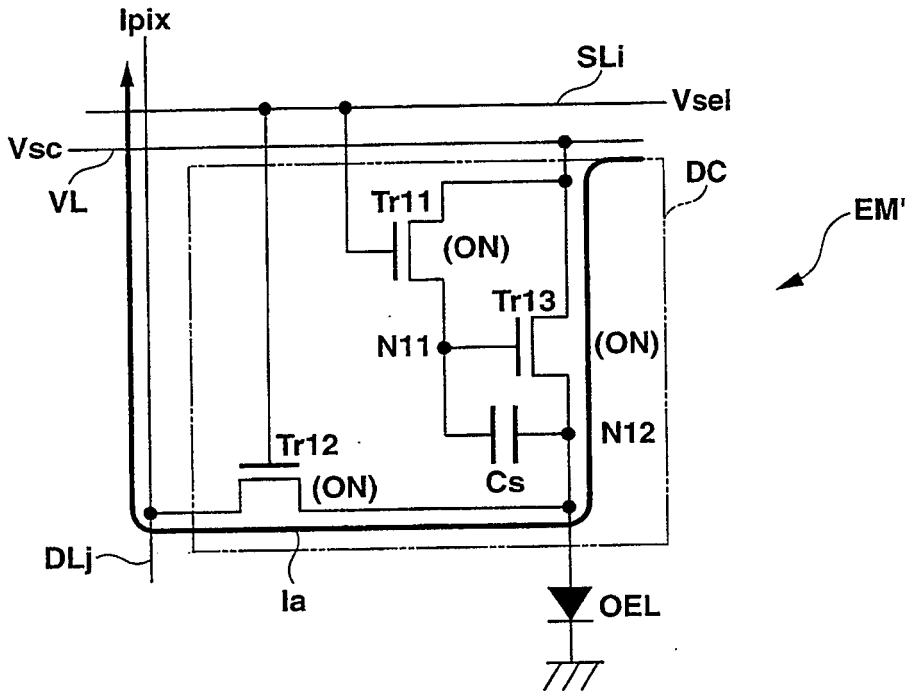


FIG.15B

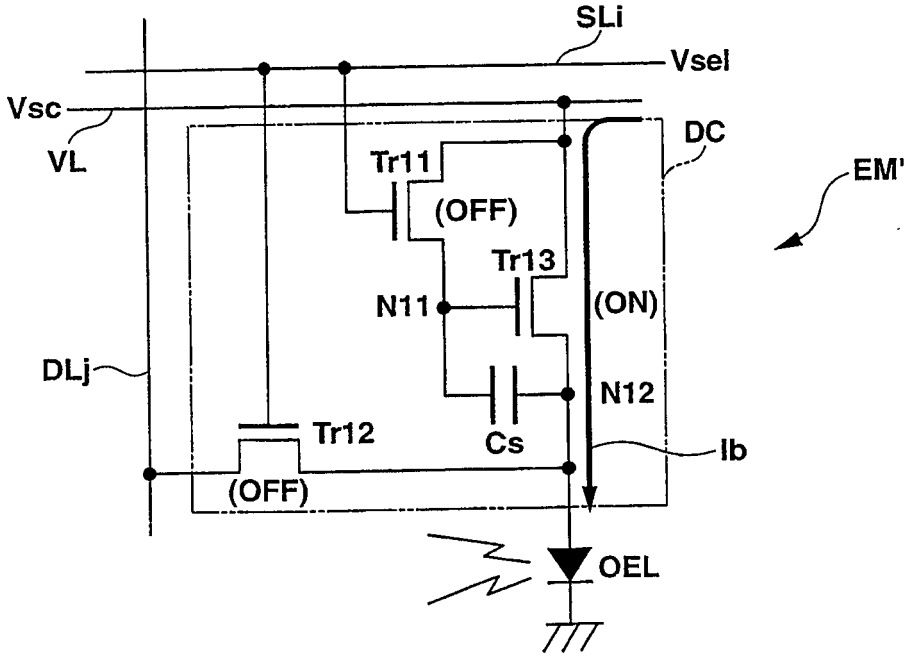


FIG.16

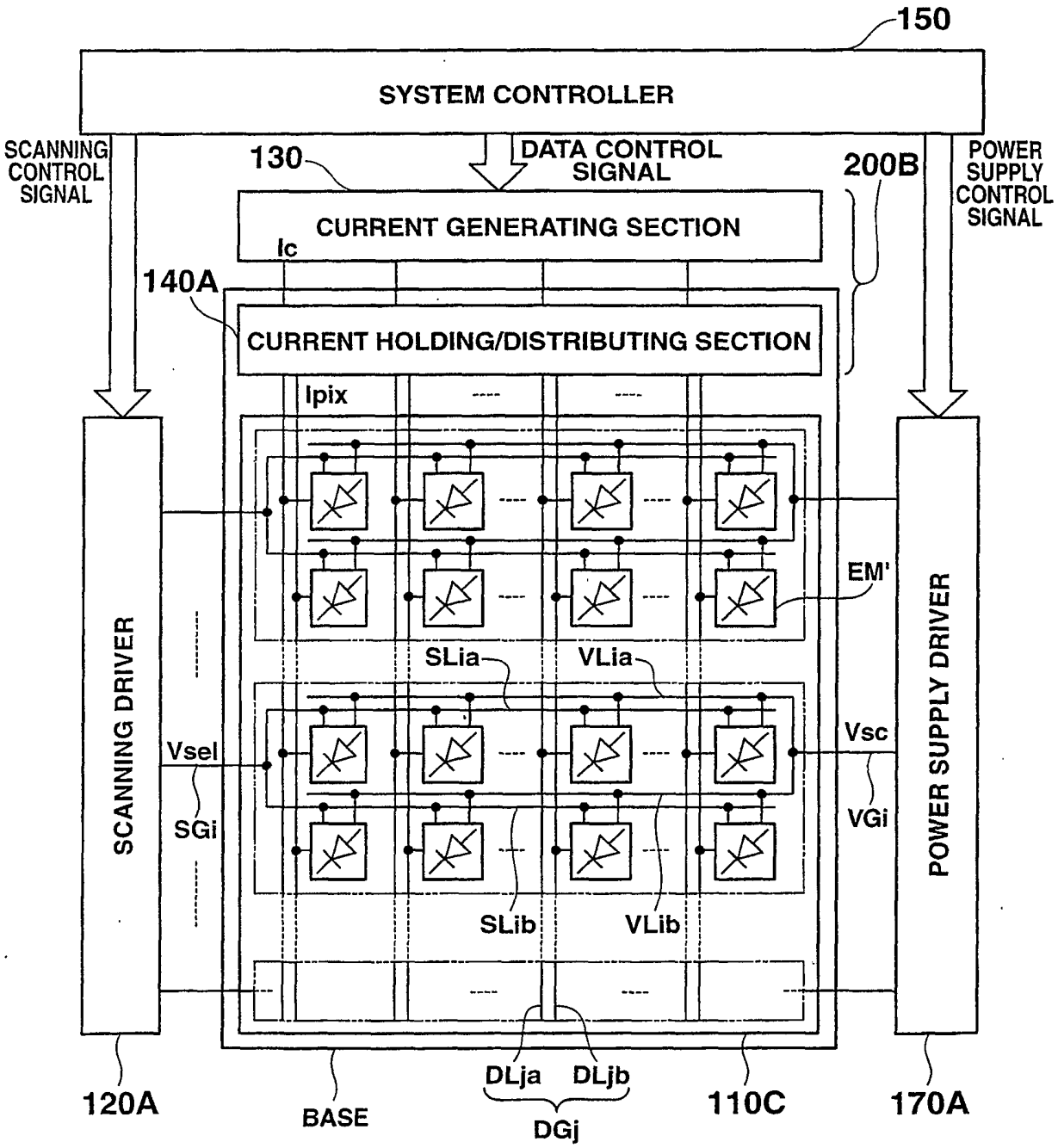

150
SYSTEM CONTROLLER
SCANNING CONTROL SIGNAL
130
DATA CONTROL SIGNAL
200B
POWER SUPPLY CONTROL SIGNAL
CURRENT GENERATING SECTION
Ic
140A
CURRENT HOLDING/DISTRIBUTING SECTION
Ipix
SCANNING DRIVER
POWER SUPPLY DRIVER
EM'
SLia
VLia
Vsel
SGi
Vsc
VGi
SLib
VLib
DLja
DLjb
DGj
120A
BASE
110C
170A

FIG.17

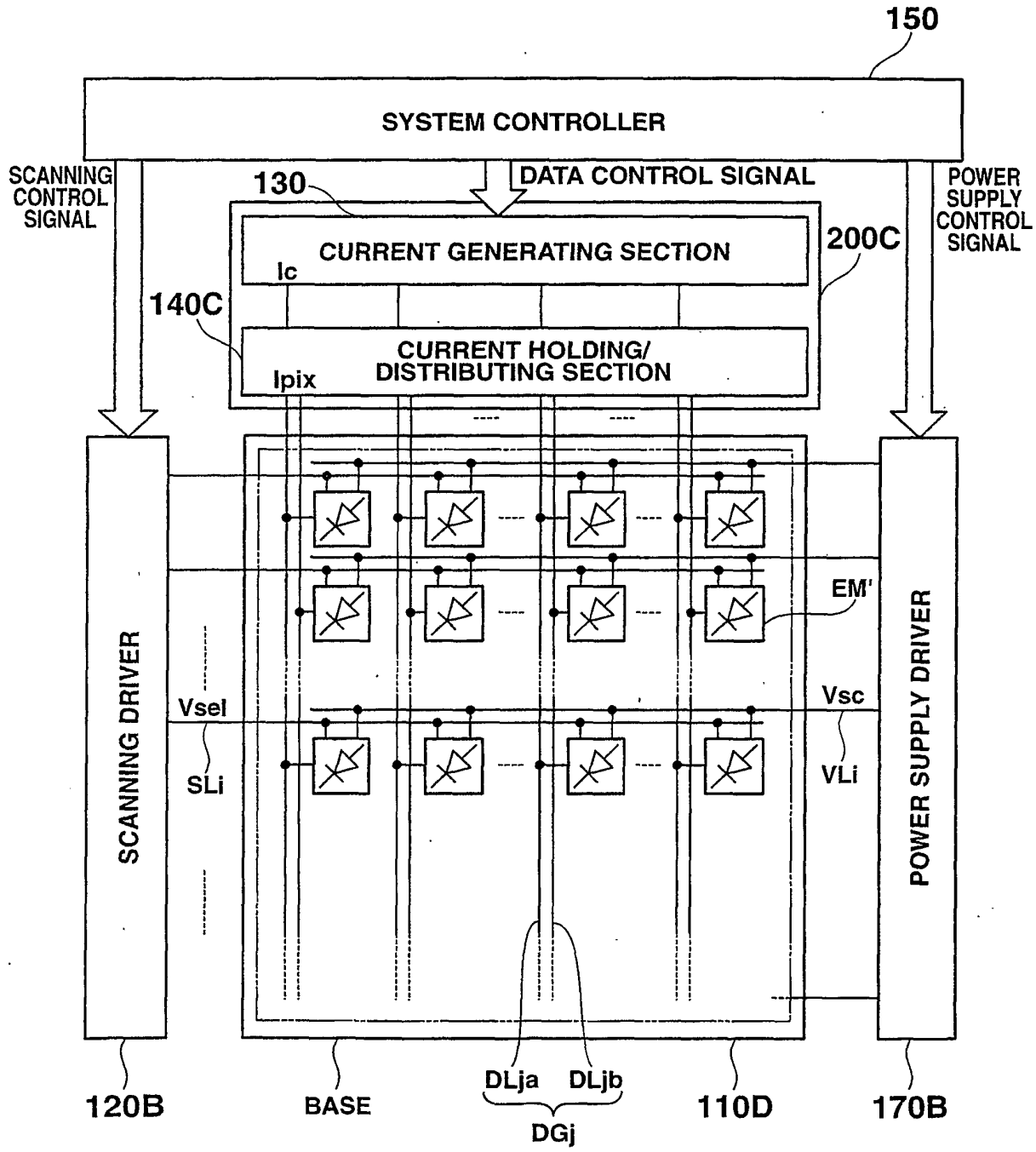

150
SYSTEM CONTROLLER
SCANNING CONTROL SIGNAL
130
DATA CONTROL SIGNAL
POWER SUPPLY CONTROL SIGNAL
CURRENT GENERATING SECTION
Ic
200C
140C
CURRENT HOLDING/ DISTRIBUTING SECTION
Ipix
SCANNING DRIVER
POWER SUPPLY DRIVER
EM'
Vsel
Vsc
SLi
VLi
DLja
DLjb
DGj
120B
BASE
110D
170B

FIG.18

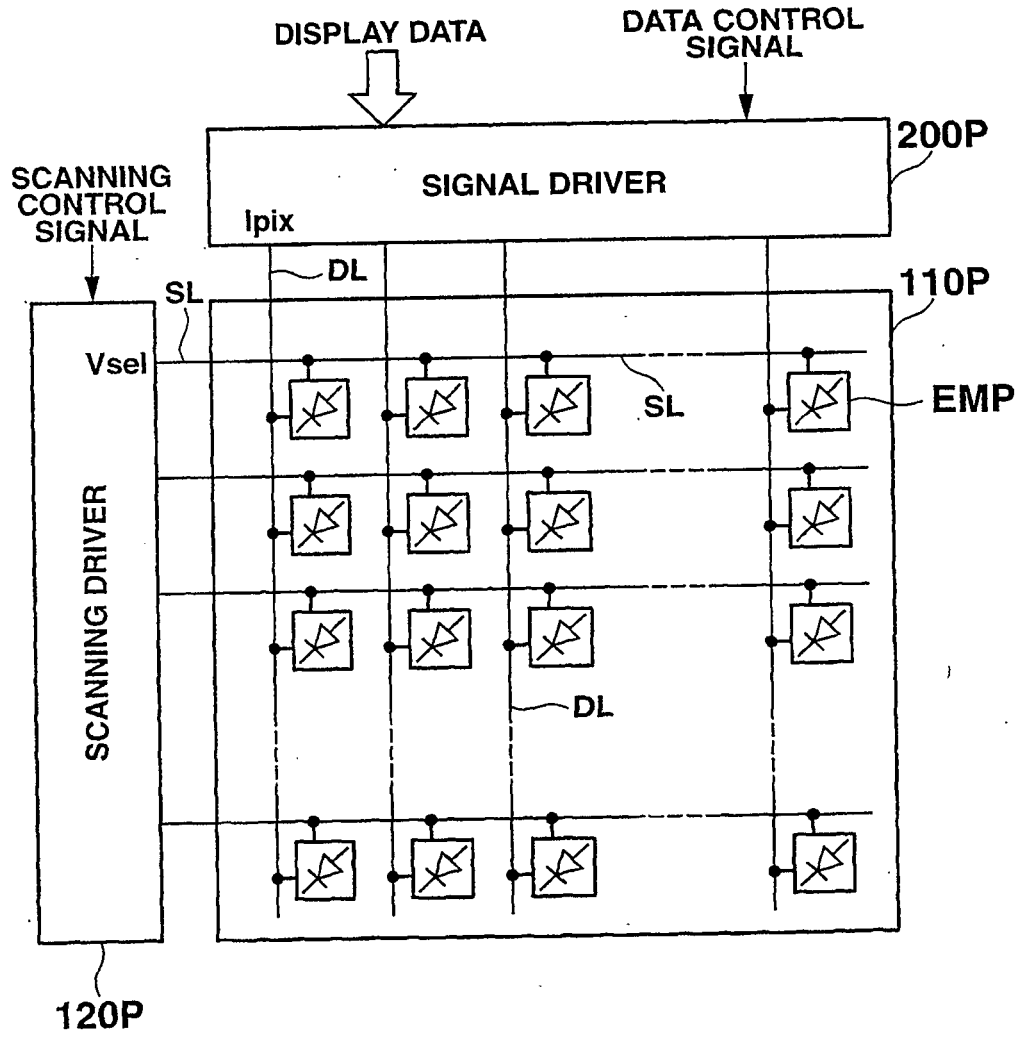
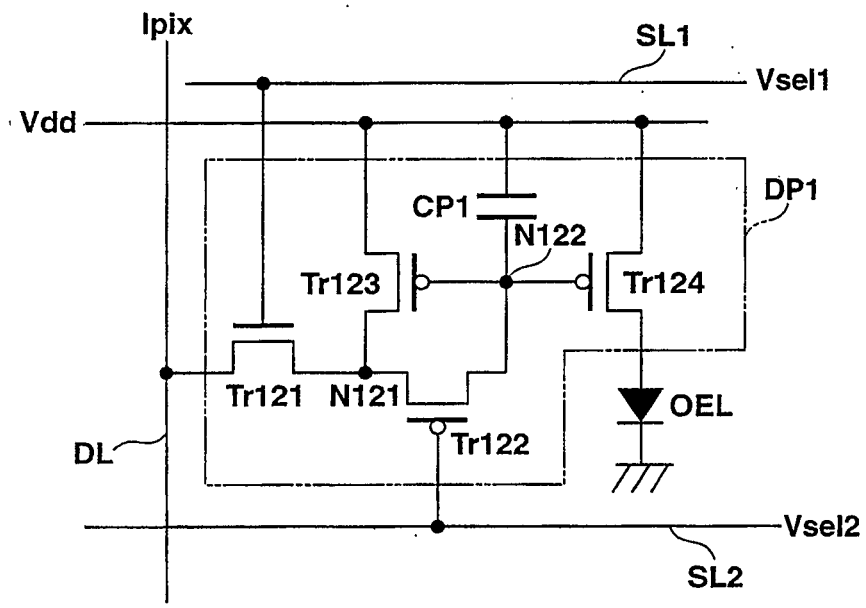

DISPLAY DATA
DATA CONTROL SIGNAL
200P
SIGNAL DRIVER
SCANNING CONTROL SIGNAL
Ipix
DL
110P
SL
Vsel
SL
EMP
SCANNING DRIVER
DL
120P

FIG.19


Ipix
SL1
Vsel1
Vdd
DP1
CP1
N122
Tr123
Tr124
Tr121
N121
OEL
Tr122
DL
Vsel2
SL2

REFERENCES CITED IN THE DESCRIPTION

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- EP 1207511 A **[0023]**
- US 2003001870 A1 **[0024]**
- EP 0911796 A **[0025]**

专利名称(译)	OLED显示屏采用乒乓电流驱动电路和同时扫描线路		
公开(公告)号	EP1649442B1	公开(公告)日	2016-01-20
申请号	EP2005745906	申请日	2005-05-26
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申请(专利权)人(译)	CASIO COMPUTER CO.，LTD.		
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发明人	SHIRASAKI, TOMOYUKI OZAKI, TSUYOSHI OGURA, JUN		
IPC分类号	G09G3/32 G09G3/36 G11C27/02		
CPC分类号	G11C27/028 G09G3/3225 G09G3/3266 G09G3/3283 G09G3/3648 G09G2300/0426 G09G2300/0842 G09G2300/0866 G09G2310/0205 G09G2310/0218 G09G2310/027 G09G2310/0297		
优先权	2004266441 2004-09-14 JP 2004160140 2004-05-28 JP		
其他公开文献	EP1649442A1		
外部链接	Espacenet		

摘要(译)

一种显示驱动装置，包括选择电路，该选择电路将所述显示面板的多个特定行中的显示像素设置在选择状态，同时所述行的选择信号至少彼此重叠。灰度信号生成电路生成灰度信号，该灰度信号基于显示数据控制每个OLED显示像素的亮度等级，并且以乒乓方式顺序地提供所生成的灰度信号。多个信号分配电路在时间序列供应的定时根据每列中的多个显示像素顺序地分配由灰度信号生成电路提供的灰度信号。多个电流保持电路分别保持分配的灰度信号，并同时将具有基于所保持的灰度信号的电流值的电流作为灰度电流提供给多个同时扫描的行中的显示像素。

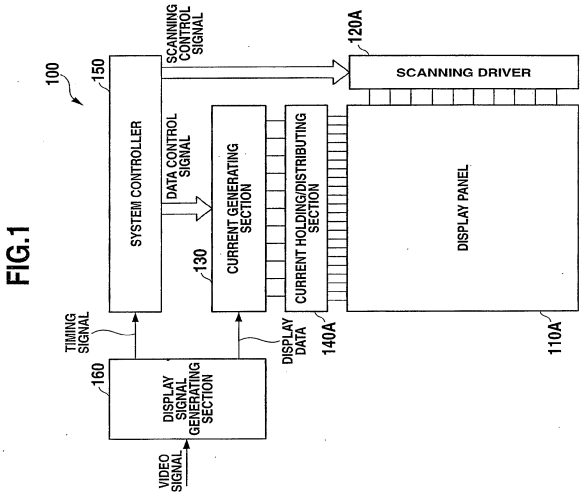

FIG.1