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(54) **ACTIVE-MATRIX DISPLAY, ACTIVE-MATRIX ORGANIC ELECTROLUMINESCENCE DISPLAY, AND METHODS FOR DRIVING THEM**

AKTIVMATRIXANZEIGE, ORGANISCHE AKTIVMATRIX-ELEKTRO-LUMINESZENZANZEIGE UND VERFAHREN ZU IHRER ANSTEUERUNG

AFFICHAGE A MATRICE ACTIVE, AFFICHAGE ELECTROLUMINESCENT ORGANIQUE A MATRICE ACTIVE ET PROCEDES DE COMMANDE DESDITS AFFICHAGES

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Description

TECHNICAL FIELD

[0001] The present invention relates to an active matrix type display device in accordance with the precharacterizing part of claim 1 and to a method of driving such an active matrix type display device in accordance with the precharacterizing part of method claim 8. An active matrix display device and a driving method of this kind are known from WO 99/65012.

BACKGROUND ART

[0002] Recently, in the display devices such as liquid crystal display (LCD) utilizing liquid crystalline cells as the display elements for respective pixels, plural pixels are arranged in the form of a matrix, and respective pixels are driven to display image such that the light intensity of each pixel is controlled in accordance with image information representing the image to be displayed. Such driving technique also applies to organic EL displays utilizing organic EL elements as the display elements for pixels.

[0003] Moreover, the organic EL displays have advantages over liquid crystal displays such that the organic EL displays have a higher visibility, need no backlighting, and have faster response to signals due to the fact that the organic EL displays are self-luminous using light-emitting elements as the display elements for pixels. The organic EL displays are quite different from liquid crystal displays in that organic EL element is current-controlled type one wherein luminance of each light-emitting element is controlled by the current flowing through it, while liquid crystal cell is voltage-controlled type one.

[0004] Like liquid crystal displays, organic EL displays can be driven in a simple (passive) matrix scheme and in an active matrix scheme. The former displays, however, have some difficult problems when used as a large-size high-precision display, though the display is simple in structure. To circumvent the problems, an active matrix control scheme has been developed in which the current flowing through a light-emitting element for each pixel is controlled by an active element, for example, a gate-insulated field effect transistor (typically a thin film transistor, TFT) also provided in the pixel.

[0005] Fig. 1 shows a conventional pixel circuit (circuit of a unit pixel) in an active matrix type organic EL display (for more details, see USP 5,684,365 and JP-A-H08-234683).

[0006] As is shown clearly in Fig. 1, the conventional pixel circuit includes an organic EL element 101 having an anode connected to a positive voltage supply Vdd, a TFT 102 having a drain connected to a cathode of the organic EL element 101 and a grounded source, a capacitor 103 connected between a gate of the TFT 102 and the ground, and a TFT 104 having a drain connected to the gate of the TFT 102, a source connected to a data line 106, and a gate connected to a scanning line 105.

[0007] Organic EL elements are often called organic light-emitting diodes (OLED) because they exhibit rectifying effects in many cases. Thus, the organic EL element is shown in Fig. 1 and other Figures as an OLED and indicated by a mark representing a diode. It should be understood, however, that in what follows the organic EL element is not required to have a rectification property.

[0008] Operations of the pixel circuit as shown above are as follows. First, the scanning line 105 is brought to a selective potential (a HIGH level in the example shown herein), and the data line 106 is supplied with a writing potential Vw to make the TFT 104 conductive, thereby charging or discharging the capacitor 103 and bringing the gate of the TFT 102 to the writing potential Vw. Next, the scanning line 105 is brought to a non-selective potential (which is a LOW level in this example). This status electrically isolates the scanning line 105 from the TFT 102. However, the gate potential of the TFT 102 is secured by the capacitor 103.

[0009] The current flowing through the TFT 102 and OLED 101 will reach a level that corresponds to the gate-source voltage Vgs, which causes the OLED 101 to be lucent with a luminance in accord with the current values thereof. In what follows an operation that transmits luminance information data, provided on the data line 106 by a selection of scanning line 105, into the pixel will be referred to as "writing". In the pixel circuit as shown in Fig. 1, once potential Vw is written to the OLED 101, such the OLED 101 will be lighted at a constant luminance until the next writing is made.

[0010] A plurality of such pixel circuits 111 (which may be simply referred to as pixels) can be arranged in the form of a matrix as shown in Fig.2 to form an active matrix type display (organic EL display) device, in which the pixels 111 are sequentially selected repeating the writing into the pixels 111 through data lines 114-1 - 115-m driven by voltage-driving-type data line drive circuit (voltage driver) 114 with scanning lines 112-1 - 112-n being sequentially selected by a scanning line drive circuit 113. In this example, pixels 111 are arranged in m (columns) by n (rows) matrix. It is a matter of course that in this case, there are m data lines and n scanning lines.

[0011] In a simple matrix type display device, each light-emitting element emits light only at the moment it is selected. In contrast, in an active matrix type display device, each light-emitting element can keep on emitting light after completion of the writing thereof. Accordingly, in the active matrix type display device, the peak luminance and peak current of light-emitting elements can be lower as compared with the simple matrix type display device, which is an advantage especially to a large size and/or high-precision display device.

[0012] In general, in the active matrix type organic EL

display device, TFTs (thin film transistor) formed on a glass substrate are used as active elements. However, amorphous silicon (non-crystalline silicon) and polysilicon (polycrystalline silicon) to be used for forming TFTs have poor crystallizing properties as compared with silicon single crystal. This implies that they have a poor conductivity and controllability, so that TFTs exhibit large fluctuations in characteristics.

[0013] Particularly, when a polysilicon TFT is formed on a relatively large glass substrate, in order to circumvent problems caused by thermal deformation of the glass substrate, a laser annealing technique is usually applied to the glass substrate after formation of an amorphous silicon film to crystallize the polysilicon TFT. However, uniform irradiation of laser light over a large area of the glass substrate is difficult, resulting in non-uniform crystallization of polysilicon at various points on the substrate. As a result, threshold value Vth of TFTs formed on the same substrate varies over several hundreds of mV, and at least I volt in some cases.

[0014] In such cases, if the same potential Vw is written to these pixels, the threshold values Vth will be different from one pixel to another. Consequently, current Ids flowing through the OLED (organic EL element) varies from one pixel to another and can deviate greatly from a desired level. One cannot then anticipate getting a high quality display. This is true not only with the threshold Vth but also with a fluctuation in the mobility μ of carriers in the same manner.

[0015] In order to alleviate the problem, the inventors of the present invention have proposed a pixel circuit as shown in Fig. 3 (See JP-A-H11-200843).

[0016] As is apparent from Fig. 3, this pixel circuit disclosed in the formerly filed Japanese Patent Application includes an OLED 121 having an anode connected with a positive voltage supply Vdd, a TFT 122 having a drain connected to a cathode of OLED 121 and a source connected to a reference potential or ground line (herein after simply referred to as ground), a capacitor 123 connected between a gate of the TFT 122 and the ground, TFT 124 having a drain connected to the data line 128 and a gate connected to a first scanning line 127A, respectively, a TFT 125 having a drain and a gate connected to a source of TFT 124 and a source connected to the ground, a TFT 126 having a drain connected to the drain and the gate of the TFT 125 and a source connected to the gate of the TFT 122, and a gate connected to the second scanning line 127B.

[0017] As shown in Fig. 3, the scanning line 127A is supplied with a timing signal scanA. The second scanning line 127B is supplied with a timing signal scanB. The data line 128 is supplied with an OLED luminance information (data). A current driver CS provides a bias current Iw to the data line 128 in accordance with active current data based on the OLED luminance information.

[0018] In the example shown herein, the TFTs 122 and 125 are N channel MOS transistors and the TFTs 124 and 126 are P channel MOS transistors. Figs. 4A-4D show timing charts for the pixel circuit in operation.

[0019] A definite difference between the pixel circuit shown in Fig. 3 and the one shown in Fig. 1 is as follows. In the pixel circuit shown in Fig. 1, luminance data is given to the pixels in the form of voltage, while in the pixel circuit shown in Fig. 3 luminance data is given to the pixels in the form of current. Corresponding operations are as follows.

[0020] First, in writing luminance information, scanning lines 127A and 127B shown in Figs. 4A and 4B are set to the selective status (status of selective potential, for which scanA and scanB are pulled down to LOW levels) and data line 128 is fed with a current Iw as shown in Fig. 4C which corresponds to the OLED luminance information shown in Fig. 4D. The current Iw flows through the TFT 125 via the TFT 124. The gate-source voltage generated in the TFT 125 is set to Vgs. Since the gate and the drain of the TFT 125 are short-circuited, the TFT 125 operates in the saturation region.

[0021] Hence, in accordance with a well-known MOS transistor formula, Iw is given by

$$Iw = \mu\ 1Cox1W1/L1/2(Vgs-Vth1)^2 \qquad (1)$$

where Vtl stands for the threshold of TFT 125, μ 1 for carrier mobility, Coxl for gate capacitance per unit area, W1 for channel width, and L1 for channel length.

[0022] Denoting the current flowing through the OLED 121 by Idrv, it is seen that the current Idrv is controlled by the TFT 122 connected in series with OLED 121. In the pixel circuit as shown in Fig. 3, since the gate-source voltage of the TFT 122 equals Vgs given by equation (1), Idrv is given by

$$Idrv = \mu\ 2Cox2W2/L2/2(Vgs-Vth2)^2 \qquad (2)$$

assuming that the TFT 122 operates in the saturation region.

[0023] Incidentally, it is known that a MOS transistor is generally operable in a saturation region under the following condition

$$|Vds|>|Vgs-Vt| \qquad (3)$$

Parameters appearing in the equations (2) and (3) are the same as in equation (1). Since the TFTs 125 and 122 are closely formed within the pixel, one may consider that practically

$$\mu 1 = \mu 2,\ Cox1 = Cox2,\ Vth1 = Vth2$$

[0024] Then, the following equation may be easily derived from the equations (1) and (2)

$$Idrv/Iw = (W2/W1)/(L2/L1) \quad (4)$$

[0025] That is, if carrier mobility μ, gate capacity per unit area Cox, and threshold Vth vary within the panel or vary from one panel to another, current Idrv flowing through the OLED 121 is exactly proportional to the writing current Iw, and hence the luminance of the OLED 121 can be precisely controlled. For example, if it is designed that W2 = W1 and L2 = L1, then Idrv/Iw = 1, which means that writing current Iw matches current Idrv that flows through the OLED 121, irrespective of variations in TFT properties.

[0026] It is possible to construct an active matrix type display device by arranging pixel circuits as described above and shown in Fig. 3 in the form of a matrix. A configuration example of such display device is shown in Fig. 5.

[0027] Referring to Fig. 5, provided to each current-writing type pixel circuit 211 arranged in a m (column) by n (row) matrix on a row by row basis are any of respective first scanning lines 212A-1 - 212A-n and any of respective second scanning lines 212B-1 - 212B-n. Further, each first scanning line 212A-1 - 212A-n is connected to the gate of the TFT 214 of Fig. 3, and each scanning line 212B-1 - 212B-n is connected to the gate of the TFT 126 of Fig. 3.

[0028] A first scanning line drive circuit 213A for driving the scanning lines 212A-1 - 212A-n is provided to the left of these pixels, and a second scanning line drive circuit 213B for driving the second scanning lines 212B-1 - 212B-n is provided to the right of the pixels. The first and the second scanning line drive circuits 213A and 213B consists of shift registers. The scanning line drive circuits 213A and 213B are provided with a common vertical start pulse VSP, and with vertical clock pulses VCKA and VCKB, respectively. The vertical clock pulse VCKA is slightly delayed with respect to the vertical clock pulse VCKB by means of a delay circuit 214.

[0029] Each of the pixel circuits 211 in each column is also connected to any of respective data lines 215-1 - 215-m. These data lines 215-1 - 215-m are connected at one end thereof to a current drive type data line drive circuit (current driver CS) 216. Luminance information is written to the respective pixels by the data line drive circuit 216 through the data lines 215-1 - 215-m.

[0030] Next, operations of the above active matrix type display device will be described. As the vertical start pulses VSP are fed to the first and the second scanning line drive circuit 213A and 213B, respectively, these scanning line drive circuits 213A and 213B begin shift operations upon receipt of the vertical start pulses VSP, sequentially output scanning pulses scanAl-scanAn and scanB1-scanBn in synchronism with the vertical clock pulses VCKA and VCKB to select scanning lines 212A-1 - 212A-n, and 212B-1 - 212B-n in sequence.

[0031] On the other hand, the data line drive circuit 216 drives the data lines 215-1 - 215-m according to current values determined by the luminance information. The current flows through the selected pixels that are connected to each of the scanning lines, to perform the writing operation on a scanning line basis. Each of these pixels starts emission of light with intensity in accord with the current values. It is noted that, as described previously, the vertical clock pulse VCKA is slightly behind the vertical clock pulse VCKB so that the scanning line 127B becomes non-selective ahead of the scanning line 127A, as seen in Fig. 3. At the point the scanning line 127B becomes non-selective, the luminance data is stored in the capacitor 123 within the pixel circuit, thereby maintaining constant luminance until new data is written into next frame.

[0032] In a case where a current mirror structure as shown in Fig. 3 is employed for the pixel circuit, a problem arises that the structure involves a larger number of transistors as compared with the one as shown in Fig. 1. That is, in the example shown in Fig. 1, each pixel is formed of two transistors, while, in the example shown in Fig. 3, each pixel requires four transistors.

[0033] Furthermore, in actuality, as disclosed in JP-A-11-200843, in many cases, a larger current Iw is needed for writing from data line as compared with the current Idrv flowing through a light-emitting element OLED. The reason for this is as follows. Current flowing through the light emitting element OLED is generally about a few μA even at the peak luminance. Hence, supposing gradation of 64 levels for the pixel, the magnitude of current in the neighborhood of the lowest gradation turns out to be several tens nA, which is however too small to be supplied correctly to the pixel circuit through a data line having a large capacitance.

[0034] This problem can be solved for a circuit shown in Fig. 3 by setting the factor (W2/W1)/(L2/L1) to a small value to thereby increase the writing current Iw in accordance with equation (4). To do this, however, it is necessary to make the ratio W1/L1 of TFT 125 large. In that case, since there are many limitations in reducing the channel length L1 as described later, the channel width W1 must be necessarily made larger, which results in a large TFT 125 occupying a large area of the pixel.

[0035] In the organic EL displays, when the dimensions of a pixel are generally fixed, this means that the area of light emitting section of the pixel must be reduced. This results in a loss of reliability of the pixel caused by increased current density, increased power consumption due to increased drive voltage, coarse graining of the pixels due to the decrease in the light emitting area, and the like, which prevent reduction of the pixel size, namely, hinders an improvement for a higher resolution.

[0036] For example, suppose that writing current on the order of a few μ A is preferred in the neighborhood of the lowest level of gradation. Then it is necessary to make the channel width W1 of the TFT 122 as 100 times larger than that of the TFT 122 if L1 = L2 is assumed. This is not the case if L1 < L2. However, there are limi-

tations on the reduction of the channel length L1 in view of withstand voltage of pixels and design rules.

[0037] Particularly in the current mirror constitution as shown in Fig. 3, it is preferred that L 1 = L2. This is because, considering the fact that the channel length greatly affects threshold value of a transistor, saturation characteristic in the saturation region thereof, and so on, it is advantageous to conform the TFTs 125 and 122 in the current mirror configuration by choosing L1 equal to L2 so that an exact proportional relationship of the current Idrv to the current Iw is established, which makes it possible to provide current of desired magnitude to the light emitting element OLED.

[0038] It is inevitable to have some fluctuations in the channel length during the manufacturing process of TFTs. Even then, if in design L1 equals L2 and the TFT 125 and TFT 122 are sufficiently close to each other, substantial equality L1 = L2 is guaranteed, should L1 and L2 deviate to some extent. As a result, the value of Idrv/Iw according to the equation (4) remains substantially constant in spite of the fluctuations.

[0039] On the other hand, if in design L1 < L2, but the actual channel lengths are shorter than the design lengths, then the shorter channel L1 will be more affected relatively than the other, rendering the ratio of L1 to L2 susceptible to the fluctuations during the manufacturing process and hence the ratio Idrv/Iw of equation (4). Consequently, dimensional fluctuations in channel length, if they occur on the same panel, can degrade the uniformity of an image formed.

[0040] Furthermore, in the circuit as shown in Fig. 3, it is necessary to made large the channel width of the TFT 124, serving as a switching transistor (hereinafter referred to as scanning transistor in some cases) connecting the data line to the TFT 125, because the writing current Iw flows through the TFT 124. This also causes a large pixel circuit occupying large area.

[0041] EP 1 061 497 AI discloses an image display apparatus including current controlled light-emitting elements and a driving method therefore, wherein each pixel includes a light-emitting element with a brightness value which varies depending upon an amount of current supplied thereto, a first TFT controlled by a scanning line for writing brightness information given thereto from a data line into the pixel and a second TFT for controlling the amount of current to be supplied to the light-emitting element corresponding to the brightness information written. Writing of the brightness information into each pixel is performed by applying an electrical signal corresponding to the brightness information to the data line while the scanning line is selected. The brightness information written in each pixel is held by the pixel also after the scanning line is placed into a non-selected state so that the light-emitting element can continue lighting with a brightness value corresponding to the brightness information held by the pixel.

[0042] WO 99/65012 cited above discloses an active matrix electroluminescent display device as well as a driving method therefore in accordance with the pre-characterizing parts of the independent claims 1 and 8, said prior art active matrix electroluminescent display device comprising:

a first scanning TFT for passing the current provided by the data line;

- conversion means, including a TFT-FET connected in diode configuration for converting the current provided from the data line into voltage;

a second scanning TFT for passing the voltage converted by the conversion means; hold means comprising a capacitor for holding the voltage converted by said conversion means, and
drive means for converting the voltage held in said hold means into a current and passing the converted current through an electro-optical element, said drive means and conversion means constituting a current mirror circuit. Further according to Fig. 5, item 20 of this document the conversion means is connected to the second scanning switch of all the pixels belonging to the same column.

[0043] It is an object of the invention to provide an active matrix type display device, and a method of driving this display device when pixel circuits are of writing current type, by realizing small pixel circuits occupying small areas to ensure a high resolution display and by realizing accurate current supply to each light emitting element.

DISCLOSURE OF THE INVENTION

[0044] According to a first aspect, the present invention provides a display device in accordance with that claimed in independent claim 1.

[0045] According to a second aspect, the present invention provides a method of driving a display device in accordance with that claimed in independent claim 8.

[0046] In the active matrix type display device having the above configuration which utilizes organic electroluminescent elements as the electro-optical elements, the first scanning switch and conversion part are possibly designed to have a large area due to the fact that they deal with a large current as compared with the electro-optical elements. It is noted that the conversion part is used only when luminance information is written, and that the first scanning switch collaborates with the second scanning switch to perform scanning in a row direction (for a selected row). Noting this feature, either or both of the first scanning switch and/or the conversion part may be shared between multiple pixels in a row direction, to thereby decrease the area of the pixel circuit occupying each pixel, which would be otherwise much larger. In addition, if the area of the pixel circuit occupying each pixel is the same, a degree of freedom of layout

design increases, so that current can be supplied to the electro-optical element more precisely.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047]

Fig. 1 is a circuit diagram of a conventional pixel circuit;

Fig. 2 is a block diagram showing a configuration example of a conventional active matrix type display device utilizing pixel circuits;

Fig. 3 is a circuit diagram of a current-writing type pixel circuit according to prior application;

Fig. 4A is a timing chart showing timing of signal scanA for a scanning line 127A of the current-writing type pixel circuit of Fig. 3;

Fig. 4B is a timing chart showing timing of signal scanB for scanning line 127B;

Fig. 4C is a timing chart showing active current data of the current driver CS;

Fig. 4D is a timing chart showing OLED luminance information;

Fig. 5 is a block diagram of an active matrix type display device utilizing current-writing type pixel circuits in accordance with prior application;

Fig. 6 is a circuit diagram showing an explanatory example of a current-writing type pixel circuit;

Fig. 7 is a cross sectional view of an exemplary organic EL element;

Fig. 8 is a cross sectional view of a pixel circuit for extracting light from the backside side of a substrate;

Fig. 9 is a cross sectional view of a pixel circuit for extracting light from the front surface side of a substrate;

Fig. 10 is a block diagram showing an active matrix type display device utilizing the current-writing pixel circuit according to the explanatory example;

Fig. 11 is a circuit diagram of a first pixel circuit obtained by modifying the explanatory example;

Fig. 12 is a circuit diagram of a second pixel circuit obtained by modifying the explanatory example;

Fig. 13 is a circuit diagram showing an embodiment of a current-writing type pixel circuit according to the invention;

Fig. 14 is a block diagram showing an active matrix type display device utilizing the embodiment of the current-writing pixel circuit according to the invention;

Fig. 15A is a timing chart showing timing of signal scanA (K of the current-writing type pixel circuit shown in Fig. 14);

Fig. 15B is a timing chart showing timing of signal scanA (K+ 1);

Fig. 15C is a timing chart showing timing of signal scanB (2K- 1);

Fig. 15D is a timing chart showing timing of scanning scanB (2K);

Fig. 15E is a timing chart showing timing of scanning scanB (2K+ 1);

Fig. 15F is a timing chart showing timing of scanning scanB (2K+2);

Fig. 15G is a timing chart showing active current data of the current driver CS; and

Fig. 16 is a circuit diagram of a modified pixel circuit obtained by modifying the embodiment of the invention.

EXPLANATORY EXAMPLE

[0048] Fig. 6 illustrates a circuit diagram of an explanatory example of a current-writing type pixel circuit for explaining basic principles, said explanatory example being not belonging to the invention as specified in the claims. In this example only two neighboring pixels (pixel 1 and 2) in a column are shown for simplicity's sake in drawing.

[0049] As shown in Fig. 6, the pixel circuit P1 of pixel 1 comprises OLED (organic EL element) 11-1 having an anode connected to a positive voltage supply Vdd, a TFT 12-1 having a drain connected to a cathode of the OLED 11-1 and a grounded source, a capacitor 13-1 connected to a gate of the TFT 12-1 and the ground (reference potential point), a TFT 14-1 having a drain connected to a data line 17 and a gate connected to a first scanning line 18A-1, respectively, a TFT 15-1 having a drain connected to a source of TFT 14-1, a source connected to the gate of the TFT 12-1, and a gate connected to a second scanning line 18B-1, respectively.

[0050] Similarly, the pixel circuit P2 of pixel 2 comprises OLED 11-2 having an anode connected to the positive voltage source Vdd, a TFT 12-2 having a drain connected to a cathode of the OLED 11-2 and a grounded source, a capacitor 13-2 connected to a gate of the TFT 12-2 and the ground, a TFT 14-2 having a drain connected to the data line 17, and a gate connected to a first scanning line 18A-2, respectively, a TFT 15-2 having a drain connected to a source of the TFT14-2, a source connected to the gate of the TFT 12-2, and a gate connected to a second scanning line 18B-2, respectively.

[0051] A so-called diode connection type TFT 16 whose drain and gate are short-circuited is shared between the pixel circuits P1 and P2 of the two pixels. That is, the drain and the gate of the TFT 16 are respectively connected to the source of the TFT 14-1 and the drain of the TFT 15-1 of the pixel circuit P1 and to the source of the TFT 14-2 and the drain of the TFT 15-2 of the pixel circuit P2, respectively. The source of the TFT 16 is grounded.

[0052] In the example shown herein, the TFTs 12-1 and 12-2 and the TFT 16 are N-channel MOS transistors, while the TFTs 14-1, 14-2, 15-1, and 15-2 are P-channel MOS transistors.

[0053] In the above arrangement of the pixel circuits P1 and P2, the TFTs 14-1 and 14-2 function as a first scanning switch for selectively supplying the TFT 16 with current Iw provided from the data line 17. The TFT 16 functions as a conversion part for converting the current Iw supplied from the data line 17 via the TFTs 14-1 and 14-2 into voltage and constitutes current mirror circuit together with the TFTs 12-1 and 12-2, which will be described later. The reason why the TFT 16 can be shared between the pixel circuits P1 and P2 is that the TFT 16 is used only at the moment of writing by the current Iw.

[0054] The TFTs 15-1 and 15-2 function as a second scanning switch for selectively supplying the capacitors 13-1 and 13-2 with the voltage converted by the TFT 16. The capacitors 13-1 and 13-2 function as hold parts for holding the voltages, which are converted from the current by the TFT 16 and supplied via the TFTs 15-1 and 15-2. The TFTs 12-1 and 12-2 function as drive parts for converting the voltages held in the respective capacitors 13-1 and 13-2 into respective currents and passing the converted currents through the OLED 11-1 and 11-2 to allow the OLED 11-1 and 11-2 to emit light. The OLEDs 11-1 and 11-2 are electro-optical elements whose luminance varies with the currents passing through them. Detailed structures of the OLEDs 11-1 and 11-2 will be described later.

[0055] Writing operations of the example of the pixel circuit described above for writing luminance data will now be described.

[0056] First, consider writing luminance data to the pixel 1. In this case, the current Iw is provided with the data line 17 in accordance with the luminance data with both of the scanning lines 18A-1 and 18B-1 being selected (in the example shown herein, scanning signals scanAl and scanB1 are both LOW levels). The current Iw is supplied to the TFT 16 via the currently conductive TFT 14-1. Because of the current Iw flowing through the TFT 16, voltage corresponding to the current Iw is generated on the gate of the TFT 16. This voltage is held in the capacitor 13-1.

[0057] This causes current to flow through the OLED 11-1 via the TFT 12-1 in response to the voltage held in the capacitor 13-1. Thus, an emission of light starts in the OLED 11-1. The writing of the luminance data to pixel 1 is completed when both the scanning lines 18A-1 and 18B-1 assume non-selective status (scanning signal scanA1 and scanB1 being pulled to HIGH levels). During the sequence of steps described above, scanning line 18B-2 stays in the non-selective status, so that OLED 11-2 of the pixel 2 keeps on emitting light with the luminance determined by the voltage held in the capacitor 13-2, without being affected by the writing to the pixel 1.

[0058] Next, consider writing luminance data to the pixel 2. This can be done by selecting both of the scanning lines 18A-2 and 18B-2 (with scanning signal scanA-2 and scanB-2 being LOW levels), and by supplying current Iw to the data line 17 in accordance with the luminance data. Because of the current Iw flowing through the TFT 16 via the TFT 14-2, voltage corresponding to the current Iw is generated on the gate of the TFT 16. This voltage is held in the capacitor 13-2.

[0059] Current corresponding to the voltage held in the capacitor 13-2 flows through the OLED 11-2 via the TFT 12-2, thereby causing the OLED 11-2 to emit light. During the sequence of the steps described above, scanning line 18B-1 maintains the non-selective status, so that OLED 11-1 of the pixel 1 continues light emission with the luminance determined by the voltage held in the capacitor 13-1, without being affected by the writing to the pixel 2.

[0060] That is, the two pixel circuits P1 and P2 of Fig. 6 behave in exactly the same way as the two pixel circuits of prior application as shown in Fig. 3. However, in the example the current-voltage conversion TFT 16 is shared between two pixels. Accordingly, one transistor may be omitted for every two pixels. As noted previously, the magnitude of the current Iw is extremely larger than the current flowing through the OLED. The current-voltage conversion TFT 16 must be large sized to directly deal with such large current Iw. Hence, it is possible to minimize that portion of the area occupied by the TFTs in the pixel circuits by configuring the current-voltage conversion TFT 16 to be shared between the two pixels as shown in Fig. 6.

[0061] As an example, a structure of the organic EL element will be described. Fig. 7 shows a cross section of an organic EL element. As apparent from Fig. 7, the organic EL element is formed of a substrate 21 made of, for example, a transparent glass, and a first electrode 22 made of transparent conductive layer (for example, anode) on the substrate 21. Further, on the first electrode 22, a positive hole carrier layer 23, a light emitting layer 24, electron carrier layer 25 and an electron injection layer 26 are deposited in order, thereby forming organic layers 27. Thereafter, a second metallic electrode (for example, cathode) 28 is formed on the organic layers 27. Applying DC voltage E across the first electrode 22 and the second electrode 28 causes the light emitting layer 24 to emit light when electrons and positive holes are recombined.

[0062] In the pixel circuit having such an organic EL element (OLED), TFTs formed on the glass substrate are used as active elements as previously described, for reasons as stated below.

[0063] Because the organic EL display device is a direct view type one, it is relatively large in size. Hence, due to limitations in cost and production capability, it is not realistic to use a single crystalline silicon substrate as the active element. Further, in order to allow the light to be emitted from the light emitting part, a transparent

conductive layer of indium tin oxide (ITO) is normally used as the first electrode (anode) 22 as shown in Fig. 7. Mostly, the ITO film is formed at a high temperature which is generally too high for the organic layer 27, and in such a case, the ITO layer must be formed before the organic layer 27 is formed. Hence, in general, the manufacture thereof proceeds as follows.

[0064] Manufacturing processes of TFT and organic EL element in the pixel circuits for use in the organic EL display device will be described below referring to the cross sectional view of Fig. 8.

[0065] First, a gate electrode 32, a gate insulation layer 33, and a semiconductor thin film 34 of amorphous (i.e. non-crystalline) silicon are formed in sequence through deposition and patterning of the respective layers, thereby forming a TFT on the glass substrate 31. On top of the TFT, an interlayer insulation film 35 is formed, and then a source electrode 36 and a drain electrode 37 are electrically connected to the source region (S) and the drain region (D) of the TFT across the interlayer insulation film 35. A further interlayer insulation film 38 is deposited thereon.

[0066] In some cases, the amorphous silicon may be transformed into polysilicon by a heat treatment such as laser annealing. In general, polysilicon has larger carrier mobility than amorphous silicon has, thereby permitting production of a TFT having a larger current drivability.

[0067] Next, a transparent electrode 39 of ITO is formed as the anode (corresponding to the first electrode 22 of Fig. 7) of the organic EL element (OLED). Then, an organic EI layer 40 (corresponding to the organic layer 27 of Fig. 7) is deposited thereon to form an organic EL element. Finally, a metallic layer (e.g. aluminum) is deposited, which will be later formed into the cathode 41 (corresponding to the second electrode 28 of Fig. 7).

[0068] In the arrangement described above, light is taken out from the backside (under side) of the substrate 31. Hence, it is necessary that the substrate 31 should be made of a transparent material (which is normally a glass). For this reason, a relatively large glass substrate 31 is used in an active matrix type organic EL display device, and as active elements, TFT that can be deposited on the substrate is usually used. An arrangement that light can be taken out from the front (upper) face of the substrate 31 has been recently adopted. A cross sectional view of such the arrangement is shown in Fig. 9. This arrangement differs from the one shown in Fig. 8 in that a metallic electrode 42, an organic EL layer 40, and a transparent electrode 43 are sequentially deposited on the interlayer insulation film 38, thereby forming an organic EL element.

[0069] As would be apparent from the above shown cross sectional view of the pixel circuit, in the active matrix type organic EL display device adapted to release light from the backside of the substrate 31, light emitting part of the organic EL element is positioned in vacant space between the TFTs after the TFTs are formed. This means that, if the transistors forming the pixel circuits are large, they occupy much of the area in the pixels, and lessen the area for the light emitting part.

[0070] In contrast, the pixel circuit of the example has the arrangement as shown in Fig. 6, in which the current-voltage conversion TFT 16 is shared between two pixels, the area occupied by the TFTs is decreased and hence the area for the light emitting parts can be increased accordingly. If the light emitting part is not increased, the size of the pixel may be decreased, so that a display device of a higher resolution can be realized.

[0071] Alternatively, in the circuit arrangement as shown in Fig. 6, one transistor can be omitted for every two pixels, which increases the degree of freedom in the layout design of the current-voltage conversion TFT 16. In this case, as described previously in connection with the related art, a large channel width W is allowed for the TFT 16, and thus, a high precision current mirror circuit can be designed without recklessly decreasing the channel length L.

[0072] In the circuit shown in Fig. 6, a pair of the TFT 16 and TFT 12-1 and a pair of the TFT 16 and TFT 12-2 form respective current mirrors, whose characteristics, e.g. threshold Vth, are preferably identical. Hence, the transistors forming the current mirrors are preferably disposed in close proximity to each other.

[0073] Although the TFT 16 is shared between the two pixels 1 and 2 in the circuit of Fig. 6, it will be apparent that the TFT 16 can be shared between more than two pixels. In this case, further reduction of the size of a pixel circuit and hence the occupied area in the pixel circuit, is possible. However, in a case where a current-voltage conversion transistor is shared between multiple pixels, it might be difficult to dispose all the OLED drive transistors (e.g. TFT 12-1 and TFT 12-2 of Fig. 6) close to that current-voltage conversion transistor (e.g. TFT 16 of Fig. 6).

[0074] As described above, an active matrix type display device, which is an active matrix type organic EL display device in the example shown herein, can be formed by arranging current-writing type pixel circuits in a matrix form. Fig. 10 is a block diagram showing such active matrix type organic EL display device.

[0075] As shown in Fig. 10, connected to each of current-writing type pixel circuits 51 arranged in m-by-n matrix are respective first scanning lines 52A-1 - 52A-n and respective second scanning lines 52B-1 - 52B-n in a row-by-row basis. In each pixel, the gate of the scanning TFT 14 (14-1, 14-2) of Fig. 6 is connected to any one of the first scanning lines 52A-1 - 52A-n, respectively, and the gate of the scanning TFT 15 (15-1, 15-n) of Fig. 6 is connected to any one of the second scanning lines 52B-1 - 52B-n, respectively.

[0076] Provided on the left side of the pixel section is a first scanning line drive circuit 53A for driving the scanning lines 52A-1 - 52A-n, and provided on the right side of the pixel section is a second scanning line drive circuit 53B for driving the second scanning lines 52B-1 - 52B-

n. The first and second scanning line drive circuits 53A and 53B are formed of shift registers. These scanning line drive circuits 53A and 53B are each supplied with a common vertical start pulse VSP and vertical clock pulses VCKA and VCKB. The vertical clock pulse VCKA is slightly delayed by a delay circuit 54 with respect to the vertical clock pulse VCKB.

[0077] Also, each pixel circuit 51 in a column is provided with any one of the respective data line 55-1 - 55-m. These data lines 55-1 - 55-m are connected at one end thereof to the current drive type data line drive circuit (current driver CS) 56. Luminance information is written to each pixel by the data line drive circuit 56 through the data lines 55-1 - 55-m.

[0078] Operations of the active matrix type organic EL display device described above will now be described. As a vertical start pulse VSP is fed to the first and the second scanning line drive circuits 53A and 53B, these scanning line drive circuits 53A and 53B start shifting operations upon receipt of the vertical start pulse VSP, thereby sequentially outputting scanning pulses scanA1-scanAn and scanB1-scanBn in synchronism with the vertical clock pulses VCKA and VCKB to sequentially select the scanning lines 52A-1 - 52A-n and 52B-1 - 52B-n.

[0079] On the other hand, the data line drive circuit 56 drives each of the data lines 55-1 - 55-m with current values in accordance with the pertinent luminance information. This current flows through the pixels that are connected to the scanning line selected, carrying out the current-writing operation by the scanning line. This causes each of the pixels to start emission of light with intensity in accordance with the current values. It is noted that since the vertical clock pulse VCKA slightly lag the vertical clock pulse VCKB, the scanning lines 18B-1 and 18B-2 become non-selective prior to the scanning lines 18A-1 and 18A-2, as shown in Fig. 6. At the point in time the scanning lines 18B-1 and 18B-2 have become non-selective, luminance data is held in the capacitor 13-1 and 13-2 within the pixel circuit, so that each pixel remains lighted at a constant luminance until new data is written into next frame.

FIRST MODIFICATION OF THE EXPLANATORY EXAMPLE

[0080] Fig. 11 is a circuit diagram showing a first modification of the pixel circuit in accordance with the explanatory example. Like reference numerals in Figs. 11 and 6 represent like or corresponding elements. Again, for simplicity of illustration, only two pixel circuits of two neighboring pixels (denoted as pixels 1 and 2) in a column are illustrated.

[0081] In the first modification, current-voltage conversion TFTs 16-1 and 16-2 are respectively provided in pixel circuits P1 and P2. This configuration apparently seems to be similar to the pixel circuit shown in Fig. 3 in connection with prior application. However, the pixel circuit is different from the one shown in Fig.3 in that the drain - gate couplings of the diode connected TFTs 16-1 and 16-2 are further coupled together for common use between the pixel circuits P1 and P2.

[0082] That is, in these pixel circuits P1 and P2, the sources of the TFTs 16-1 and 16-2 are grounded so that they are functionally equivalent to a single transistor element. Thus, the circuit shown in Fig. 11 having the drain-gate couplings of TFTs 16-1 and 16-2 commonly coupled is practically the same as the circuit shown in Fig. 6 having TFT16 shared between two pixels.

[0083] Because the TFTs 16-1 and 16-2 together are equivalent to a single transistor element, and because writing current Iw flows through the TFTs 16-1 and 16-2, the channel width of each of the TFTs 16-1 and 16-2 can be equal to the one to which the channel width of the current-voltage conversion TFT 125 of the pixel circuit shown in Fig. 3 in connection with the prior application is halved, as compared with the pixel circuit shown in Fig. 3 in connection with the prior application. As a result, the area occupied by the TFTs in the pixel circuit can be made smaller than that of the pixel circuits in connection with the prior application.

[0084] It will be apparent that the configuration described above in the first modification can be applied not only to two pixels but also to more than two pixels as in the first embodiment

SECOND MODIFICATION OF THE EXPLANATORY EXAMPLE

[0085] Fig. 12 shows a circuit diagram showing a second modification of a pixel circuit in accordance with the explanatory example. Like reference numerals in Figs. 12 and 6 represent like or corresponding elements. In this second modification also, only two neighboring pixels (pixels 1 and 2) in a column are shown for simplicity of illustration.

[0086] In the second modification, scanning line is (18-1 and 18-2) are respectively provided to each pixel one by one, so that the gates of the TFTs 14-1 and 15-1 are connected in common to the scanning line 18-1 while the gates of the scanning TFTs 14-2 and 15-2 are connected in common to the scanning line 18-2. In this respect, this modified pixel circuit differs from the one according to the first embodiment in which both of two scanning lines are provide to each pixel.

[0087] In operation, row-wise scanning is performed by a single scanning signal in the second modification, in contrast to the first embodiment where row-wise scanning is performed by a set of two scanning signals (A and B). However, the second modification is equivalent to the explanatory example not only in configuration of the pixel circuit but also in function thereof.

EMBODIMENT OF THE INVENTION

[0088] Fig. 13 is a circuit diagram showing an embod-

iment of a current-writing type pixel circuit according to the invention. Like reference numerals in Figs. 13 and 6 represent like or corresponding elements. Here, for simplicity of illustration, only two neighboring pixels (pixels 1 and 2) in a column are shown.

[0089] As compared to the explanatory example in which a current-voltage conversion TFT 16 is shared between two pixels, the pixel circuit of the embodiment has the first scanning TFT 14 serving as a first scanning switch also shared between two pixels. That is, regarding "A" group of scanning lines, one scanning line 18A is provided to every two pixels, and the gate of single scanning TFT 14 is connected to the scanning line 18A, and the source of the scanning TFT 14 is connected to the drain and the gate of the current-voltage conversion TFT 16 and to the drains of the scanning TFTs 15-1 and 15-2 serving as a second scanning switch.

[0090] The scanning line 18A of the "A" group shown in Fig. 13 is supplied with a timing signal scanA. The scanning line 18B-1 of B group is supplied with a timing signal scanB1, while the scanning line 18B-2 is supplied with a timing signal scanB-2. OLED luminance information (luminance data) is supplied to the data line 17. The current driver CS feeds bias current Iw to the data line 17 in accordance with active current data based on the OLED luminance information.

[0091] Writing operations of luminance data to a current-writing type pixel circuit in accordance with the embodiment described above will now be described.

[0092] First, consider writing luminance data to the pixel 1. In this case, the current Iw is provided with the data line 17 in accordance with the luminance data with both of the scanning lines 18A and 18B-1 being selected (in the example shown herein, scanning signals scanA and scanB1 are both LOW levels). The current Iw is supplied to the TFT 16 via the currently conductive TFT 14. Because of the current Iw flowing through the TFT 16, voltage corresponding to the current Iw is generated on the gate of the TFT 16. This voltage is held in the capacitor 13-1.

[0093] This causes current to flow through the OLED 11-1 via the TFT 12-1 in response to the voltage held in the capacitor 13-1. Thus, an emission of light starts in the OLED 11-1. The writing of the luminance data to pixel 1 is completed when both the scanning lines 18A and 18B-1 assume non-selective status (scanning signal scanA and scanB being pulled to HIGH levels). During the sequence of steps described above, scanning line 18B-2 stays in the non-selective status, so that OLED 11-2 of the pixel 2 keeps on emitting light with the luminance determined by the voltage held in the capacitor 13-2, without being affected by the writing to the pixel 1.

[0094] Next, consider writing luminance data to the pixel 2. This can be done by selecting both of the scanning lines 18A and 18B-2 (with scanning signal scanA and scanB-2 being LOW levels), and by supplying current Iw to the data line 17 in accordance with the luminance data. Because of the current Iw flowing through the TFT 16 via the TFT 14, voltage corresponding to the current Iw is generated on the gate of the TFT 16. This voltage is held in the capacitor 13-2.

[0095] Current that corresponds to the voltage held in the capacitor 13-2 flows through the OLED 11-2 via the TFT 12-2, thereby causing the OLED 11-2 to emit light. During the sequence of the steps described above, scanning line 18B-1 maintains the non-selective status, so that OLED 11-1 of the pixel 1 continues emitting light with the luminance determined by the voltage held in the capacitor 13-1, without being affected by the writing to the pixel 2.

[0096] Although the scanning line 18A must be selected during the writing to the pixels 1 and 2 as described above, the scanning line 18A may be reset to the non-selective status at a suitable timing after the completion of writing to the two pixels 1 and 2. Control of the scanning line 18A will now be described.

[0097] As described above, an active matrix type display device, which is an active matrix type organic EL display device in the example shown herein, can be formed by arranging the above pixel circuits in accordance with the embodiment in a matrix form. Fig. 14 is a block diagram showing such active matrix type organic EL display device. Like reference numerals in Figs. 14 and 10 represent like or corresponding elements.

[0098] In the active matrix type organic EL display device according to the embodiment, the first scanning lines 52A-1, 52A-2... are provided to each of the pixel circuits 51 arranged in a matrix of m columns by n rows, with one scanning line for every two rows (i.e. one scanning line for two pixels). Hence, the number of the first scanning lines 52A-1, 52A-2, ... is one half the number n of the pixels in a vertical direction (=n/2).

[0099] On the other hand, the second scanning lines 52B-1, 52B-2 ... are provided with one scanning line for each row. Hence, the number of the second scanning lines 52B-1, 52B-2, ... equals n. In each pixel, the gate of the scanning TFT 14 shown in Fig. 13 is connected to the first scanning lines 52A-1, 52A-2... respectively, and the gates of the scanning TFTs 15 (15-1 and 15-2) are connected to the second scanning lines 52B-1, 52B-2... respectively.

[0100] Figs. 15A-15G are timing charts each for writing operations in the above active matrix type organic EL display device. The timing charts represent writing operations for four pixels in the 2k-1st row through 2k+1st row (k being an integer) counting from top to bottom.

[0101] In writing to the pixels in the 2k-1st and 2kth rows, scanning signal scanA (k) is set to the selective status (which is LOW level in the example shown herein) as shown in Fig. 15A. During this period, selecting the scan signal scanB (2k-1) as shown in Fig. 15C and the scan signal scanB (2k) as shown in Fig. 15D in sequence allows the writing to the two pixels in these rows to be made. Next, in writing to the pixels in the rows 2k+1st and 2k+2nd, the scanning signal scanA (k+1) as

shown in Fig. 15B is set to the selective status (which is LOW level in the example shown herein). During this period, sequentially selecting the scanning signal scanB (2k+1) as shown in Fig. 15E and the scanning signal scanB (2k+2) as shown in Fig. 15F allows the writing to the two pixels in these rows to be accomplished. Fig. 15G shows active current data in the current driver CS 56.

[0102] As described above, in the pixel circuit in accordance with the embodiment, the scanning TFT 14 and the current-voltage conversion TFT 16 are shared between two pixels. Hence, the number of transistors per two pixels is six, which is less than that of the pixel circuit shown in Fig. 3 in connection with prior application by 2. Nevertheless, the inventive pixel circuit can attain the same writing operation as the pixel circuit in connection with the prior application.

[0103] It is noted that, like the current-voltage conversion TFT 16, in order for the scanning TFT 14 to deal with extremely large current Iw as compared with the current through the OLED (organic EL element), the TFT 14 must have large dimensions, and hence occupy a large area in the pixel. Therefore, the circuit configuration of the embodiment shown in Fig. 13 helps advantageously minimize the occupied area in the pixel circuit that is occupied by the TFTs, since not only the current-voltage conversion TFT 16 but also the scanning TFT 14 are shared between two pixels in this configuration. It is thus possible in the embodiment to attain much a higher resolution than the explanatory example by enlarging the dimensions of the light emitting part or reducing the pixel size.

[0104] Although, in the embodiment, the scanning TFT 14 and the current-voltage conversion TFT 16 are also shared between two pixels, it will be apparent that they can be shared between more than two pixel circuits. In that case, merits of reducing the number of the transistors are significant. However, sharing of the scanning TFT 14 between too many transistors will make it difficult to arrange so many OLED drive transistors (e. g. TFTs 12-1 and 12-2 of Fig. 13) close to the current-voltage conversion transistor (e.g. TFT 16 of Fig. 13) in each pixel circuit.

[0105] In the embodiment described herein, the scanning TFT 14 and the current-voltage conversion TFT 16 are shared between a multiplicity of pixels.

MODIFICATION OF THE EMBODIMENT

[0106] Fig. 16 is a circuit diagram showing a modification of the pixel circuit in accordance with the embodiment. Like reference numerals in Figs. 16 and 13 represent like or corresponding elements. Again, for simplicity of illustration, only two pixel circuits of two neighboring pixels (denoted by pixels 1 and 2) in a column are illustrated.

[0107] In the pixel circuit in accordance with this modification, pixel circuits P1 and P2 are respectively provided with the scanning TFTs 14-1 and 14-2 and the current-voltage conversion TFTs 16-1 and 16-2. Specifically, the gates of the respective scanning TFTs 14-1 and 14-2 are connected in common to the scanning line 18A. The respective drains and the gates of the diode-connected TFTs 16-1 and 16-2 are connected in common to each other between pixel circuits P1 and P2, and further connected to the sources of the scanning TFTs 14-1 and 14-2.

[0108] As is apparent from the above connection relationship, since the scanning TFTs 14-1 and 14-2 and the current-voltage conversion TFTs 16-1 and 16-2 are respectively connected in parallel, they are functionally equivalent to a single transistor element. In this regard, the circuit shown in Fig. 16 is substantially equivalent to the one shown in Fig. 13.

[0109] In the pixel circuit in accordance with this modification, the number of transistors is the same as that of transistors for two pixels of the pixel circuit shown in Fig. 3 in connection with the prior application. However, in this configuration, since writing current Iw flows through the TFT 14-1 and TFT 14-2, and through the TFTs 16-2 and 16-2, the channel width of these transistors can be equal to the one to which that of the pixel circuit in connection with the prior application is halved. Accordingly, as in the pixel circuit in accordance with the embodiment, the area occupied by the TFTs in the pixel circuit can be extremely reduced.

[0110] In the embodiment and its modification described above, the transistors forming current mirror circuits are presumably N-channel MOS transistors, and the scanning TFTs are p-channel MOS transistors. However, it should be understood that these embodiments have been presented for purposes of illustration and description, and not to limit the invention in the form disclosed.

Claims

1. An active matrix electroluminescent display device comprising a matrix array of electroluminescent electro optical elements (11-1, 11-2) arranged in rows and columns, including pixel circuits (P1, P2) adapted to provide a current arriving from a data line (17) to said electroluminescent electro optical elements whose luminance varies with the current passing therethrough, said pixel circuits (P1, P2) comprising:

   - a first scanning switch (14) for selectively passing the current provided from said data line (17);
   - a conversion means (16) for converting the current provided through said first scanning switch (14) into a voltage;
   - a second scanning switch (15, 15-1, 15-2) for selectively passing the voltage converted by

said conversion means (16);

- a hold means (13-1, 13-2) for holding the voltage supplied thereto through said second scanning switch (15-1, 15-2) and
- a drive means (12-1, 12-2) for converting the voltage held in said hold means (13-1, 13-2) into a current and providing the converted current to said electro-optical element (11-1, 11-2), wherein

said conversion means (16) is connected to the second scanning switch (15, 15-1. 15-2) of at least two separate pixel circuits (P1, P2) belonging to the same column and said first scanning switch (14) is connected to an electrode of said conversion means (16), **characterized in that** said first scanning switch (14) is provided in common for said at least two separate pixel circuits (P1, P2) belonging to the same column for feeding said current passed from the data line (17) through said conversion means (16) to said at least two separate pixel circuits (P1, P2).

2. The active matrix display device according to claim 1, wherein said first scanning switch (14) is provided in common for said pixel circuits (P1, P2) in two neighboring rows.

3. The active matrix display device according to claim 1, wherein

- said first scanning switch (14) includes a first FET (14) having a gate connected to a first scanning line (18 A);
- said conversion means (16) includes a second FET (16) having a drain and a gate thereof short circuited for generating voltage across the gate and the source thereof when current is supplied from the data line (17) via said first scanning switch (14);
- said second scanning switch includes a third FET (15-1, 15-2) having a gate connected to a second scanning line (18B-1, 18B-2);
- said hold means (13-1, 13-2) includes a capacitor for holding the voltage generated across said gate and source of said second FET (16) and supplied via said third FET effect transistor (15-1, 15-2); and
- said drive means (12-1, 12-2) includes a fourth FET (12-1, 12-2) connected in series with said electro-optical element (11-1, 11-2) for driving said electro-optical element in accordance with said voltage held in said capacitor of said hold means (13-1, 13-2).

4. The active matrix type display device according to claim 3, wherein said second (16) and fourth FET (12-1. 12-2) together constitute a current mirror circuit.

5. The active matrix type display device according to claim 3, wherein said first or second FET (14, 16) is a single transistor element.

6. The active matrix type display device according to claim 3, wherein said first or second FET (14-1, 14-2 or 16-1, 16-2) includes a multiplicity of transistor elements having said drains and gates connected together.

7. The active matrix type display device according to one of the claims 1 to 6. wherein said display device is an organic electroluminescent display device.

8. A method of driving an active matrix electroluminescent display device comprising a matrix array of electroluminescent electro optical elements (11-1, 11-2) arranged in rows and columns including pixel circuits (P1, P2) adapted to provide a current arriving from a data line (17) to said electroluminescent electro optical elements whose luminance varies with the current passing therethrough, said pixel circuits (P1, P2) comprising:

- a first scanning switch (14) for selectively passing the current provided from said data line (17);
- a conversion means (16) for converting the current provided through said first scanning switch (14) into a voltage;
- a second scanning switch (15, 15-1, 15-2) for selectively passing the voltage converted by said conversion means (16);
- a hold means (13-1, 13-2) for holding the voltage supplied thereto through said second scanning switch (15, 15-1, 15-2) and
- a drive means (12-1, 12-2) for converting the voltage held in said hold means (13-1, 13-2) into a current and passing the converted current through said electro-optical element (11-1, 11-2), wherein said first scanning switch (14) and said conversion means (16) are provided in common for at least two separate pixel circuits (P1, P2) belonging to the same column of the matrix display device, said first scanning switch (14) being connected to an electrode of the conversion means (16),

the method **characterized by** the step of

setting said first scanning switch (14) to a selective status and, during a period in which said first scanning switch (14) holds said selective status, sequentially switching to a selective status said second scanning switch (15-1) of said first pixel circuit (P1) and said second scanning switch (15-2) of said other pixel circuit (P2).

9. The method according to claim 8, wherein said active matrix type display device is an organic electroluminescent display device.

Patentansprüche

1. Elektrolumineszenz-Anzeigevorrichtung des Aktivmatrix-Typs, mit einer Matrixanordnung aus in Zeilen und Spalten angeordneten elektrooptischen Elektrolumineszenzelementen (11-1, 11-2) einschließlich Pixelschaltungen (P1, P2), die so beschaffen sind, dass sie einen von einer Datenleitung (17) ankommenden Strom für die elektrooptischen Elektrolumineszenzelemente, deren Luminanz sich mit dem durch sie fließenden Strom ändert, bereitstellen, wobei die Pixelschaltungen (P1, P2) versehen sind mit:

- einem ersten Abtastschalter (14), um den von der Datenleitung (17) bereitgestellten Strom wahlweise durchzulassen;
- einem Umsetzungsmittel (16), um den durch den ersten Abtastschalter (14) bereitgestellten Strom in eine Spannung umzusetzen;
- einem zweiten Abtastschalter (15, 15-1, 15-2), um die durch das Umsetzungsmittel (16) umgesetzte Spannung wahlweise durchzulassen;
- einem Haltemittel (13-1, 13-2), um die über den zweiten Abtastschalter (15-1, 15-2) gelieferte Spannung zu halten, und
- einem Treibermittel (12-1, 12-2), um die in dem Haltemittel (13-1, 13-2) gehaltene Spannung in einen Strom umzusetzen und um den umgesetzten Strom für das elektrooptische Element (11-1, 11-2) bereitzustellen, wobei

das Umsetzungsmittel (16) mit dem zweiten Abtastschalter (15, 15-1, 15-2) von wenigstens zwei getrennten Pixelschaltungen (P1, P2), die zu derselben Spalte gehören, verbunden ist und der erste Abtastschalter (14) mit einer Elektrode des Umsetzungsmittels (16) verbunden ist, **dadurch gekennzeichnet, dass** der erste Abtastschalter (14) gemeinsam für die wenigstens zwei getrennten Pixelschaltungen (P1, P2), die zu derselben Spalte gehören, vorgesehen ist, um den von der Datenleitung (17) durchgelassenen Strom über das Umsetzungsmittel (16) zu den wenigstens zwei getrennten Pixelschaltungen (P1, P2) zu liefern.

2. Anzeigevorrichtung des Aktivmatrix-Typs nach Anspruch 1, bei der der erste Abtastschalter (14) gemeinsam für die Pixelschaltungen (P1, P2) in zwei benachbarten Zeilen vorgesehen ist.

3. Aktivmatrix-Anzeigevorrichtung nach Anspruch 1, bei der:

- der erste Abtastschalter (14) einen ersten FET (14) aufweist, dessen Gate mit einer ersten Abtastzeile (18A) verbunden ist;
- das Umsetzungsmittel (16) einen zweiten FET (16) aufweist, dessen Drain und dessen Gate kurzgeschlossen sind, um über dem Gate und der Source hiervon eine Spannung zu erzeugen, wenn von der Datenleitung (17) über den ersten Abtastschalter (14) ein Strom geliefert wird;
- der zweite Abtastschalter einen dritten FET (15-1, 15-2) aufweist, dessen Gate mit einer zweiten Abtastzeile (18B-1, 18B-2) verbunden ist;
- das Haltemittel (13-1, 13-2) einen Kondensator aufweist, um die über dem Gate und der Source des zweiten FET (16) erzeugte und über den dritten FET (15-1, 15-2) gelieferte Spannung zu halten; und
- das Treibermittel (12-1, 12-2) einen vierten FET (12-1, 12-2) enthält, der mit dem elektrooptischen Element (11-1, 11-2) in Reihe geschaltet ist, um das elektrooptische Element in Übereinstimmung mit der Spannung, die in dem Kondensator des Haltemittels (13-1, 13-2) gehalten wird, anzusteuern.

4. Anzeigevorrichtung des Aktivmatrix-Typs nach Anspruch 3, bei der der zweite FET (16) und der vierte FET (12-1, 12-2) gemeinsam eine Stromspiegelschaltung bilden.

5. Anzeigevorrichtung des Aktivmatrix-Typs nach Anspruch 3, bei der der erste FET (14) oder der zweite FET (16) ein einzelnes Transistorelement ist.

6. Anzeigevorrichtung des Aktivmatrix-Typs nach Anspruch 3, bei der der erste FET (14-1, 14-2) oder der zweite FET (16-1, 16-2) mehrere Transistorelemente enthält, deren Drains und Gates miteinander verbunden sind.

7. Anzeigevorrichtung des Aktivmatrix-Typs nach einem der Ansprüche 1 bis 6, wobei die Anzeigevorrichtung eine organische Elektrolumineszenz-Anzeigevorrichtung ist.

8. Verfahren zum Ansteuern einer Elektrolumineszenz-Anzeigevorrichtung des Aktivmatrix-Typs, mit einer Matrixanordnung aus in Zeilen und Spalten angeordneten elektrooptischen Elektrolumineszenzelementen (11-1, 11-2), die Pixelschaltungen (P1, P2) enthalten, die so beschaffen sind, dass sie einen von einer Datenleitung (17) ankommenden Strom für die elektrooptischen Elektrolumineszenzelemente, deren Luminanz sich mit dem durch sie fließenden Strom ändert, bereitstellen, wobei die Pixelschaltungen (P1, P2) versehen sind mit:

- einem ersten Abtastschalter (14), um den von der Datenleitung (17) bereitgestellten Strom wahlweise durchzulassen;
- einem Umsetzungsmittel (16), um den über den ersten Abtastschalter (14) bereitgestellten Strom in eine Spannung umzusetzen;
- einem zweiten Abtastschalter (15, 15-1, 15-2), um die durch das Umsetzungsmittel (16) umgesetzte Spannung wahlweise durchzulassen;
- einem Haltemittel (13-1, 13-2), um die über dem zweiten Abtastschalter (15, 15-1, 15-2) gelieferte Spannung zu halten; und
- einem Treibermittel (12-1, 12-2), um die in dem Haltemittel (13-1, 13-2) gehaltene Spannung in einen Strom umzusetzen und um den umgesetzten Strom durch das elektrooptische Element (11-1, 11-2) durchzulassen, wobei der erste Abtastschalter (14) und das Umsetzungsmittel (16) für wenigstens zwei getrennte Pixelschaltungen (P1, P2), die zu derselben Spalte der Matrix-Anzeigevorrichtung gehören, gemeinsam vorgesehen sind, wobei der erste Abtastschalter (14) mit einer Elektrode des Umsetzungsmittels (16) verbunden ist, wobei das Verfahren **gekennzeichnet ist durch** den folgenden Schritt:

  Versetzen des ersten Abtastschalters (14) in einen ausgewählten Zustand und während einer Periode, in der der erste Abtastschalter (14) den ausgewählten Zustand beibehält, sequentielles Umschalten in einen ausgewählten Zustand des zweiten Abtastschalters (15-1) der ersten Pixelschaltung (P1) und des zweiten Abtastschalters (15-2) der anderen Pixelschaltung (P2).

9. Verfahren nach Anspruch 8, bei dem die Anzeigevorrichtung des Aktivmatrix-Typs eine organische Elektrolumineszenz-Anzeigevorrichtung ist.

Revendications

1. Dispositif d'affichage électroluminescent à matrice active comprenant un agencement en matrice d'organes (11-1, 11-2) électro-optiques électroluminescents agencés en rangées et colonnes, comprenant des circuits (P1, P2) de pixels adaptés pour fournir un courant arrivant depuis une ligne (17) de données jusqu'auxdits organes électro-optiques électroluminescents dont une luminance varie avec le courant qui y passe, lesdits circuits (P1, P2) de pixels comprenant :

- un premier interrupteur (14) à balayage pour faire passer de manière sélective le courant fourni depuis ladite ligne (17) de données ;
- un moyen (16) de conversion pour convertir le courant fourni au travers dudit premier interrupteur (14) à balayage en une tension ;
- un second interrupteur (15, 15-1, 15-2) à balayage pour faire passer de manière sélective la tension convertie par ledit moyen (16) de conversion ;
- un moyen (13-1, 13-2) de maintien pour maintenir la tension qui y est alimentée au travers dudit second interrupteur (15-1, 15-2) à balayage et
- un moyen (12-1, 12-2) d'entraînement pour convertir la tension maintenue dans ledit moyen (13-1, 13-2) de maintien en un courant et fournir le courant converti vers ledit organe (11-1, 11-2) électro-optique, dans lequel

ledit moyen (16) de conversion est connecté audit second interrupteur (15, 15-1, 15-2) à balayage d'au moins deux circuits (P1, P2) de pixels séparés appartenant à la même colonne et ledit premier interrupteur (14) à balayage est connecté à une électrode dudit moyen (16) de conversion, **caractérisé en ce que** ledit interrupteur (14) à balayage est mis à disposition en commun pour lesdits au moins deux circuits (P1, P2) de pixels séparés appartenant à la même colonne pour alimenter ledit courant passant depuis la ligne (17) de données au travers dudit moyen (16) de conversion jusqu'auxdits au moins deux circuits (P1, P2) de pixels séparés.

2. Dispositif d'affichage à matrice active selon la revendication 1, dans lequel ledit premier interrupteur (14) à balayage est mis à disposition en commun pour lesdits circuits (P1, P2) de pixels dans deux rangées voisines.

3. Dispositif d'affichage à matrice active selon la revendication 1, dans lequel

- ledit premier interrupteur (14) à balayage comprend un premier TEC (14) ayant une grille connectée à une première ligne (18A) de balayage ;
- ledit moyen (16) de conversion comprend un second TEC (16) ayant un drain et une grille de ce dernier court-circuités pour générer une tension sur la grille et la source de ce dernier lorsqu'un courant est alimenté depuis la ligne (17) de données par le biais dudit premier interrupteur (14) à balayage ;
- ledit second interrupteur à balayage comprend un troisième TEC (15-1, 15-2) ayant une grille connectée à une seconde ligne (18B-1, 18B-2) de balayage ;
- ledit moyen (13-1, 13-2) de maintien comprend un condensateur pour maintenir la tension gé-

nérée sur lesdites grille et source du second TEC (16) et alimentée par le biais dudit troisième transistor à effet de champ TEC (15-1, 15-2) ; et

- ledit moyen (12-1, 12-2) d'entraînement comprend un quatrième TEC (12-1, 12-2) connecté en série avec ledit organe (11-1, 11-2) électro-optique pour entraîner ledit organe électro-optique conformément à ladite tension maintenue dans ledit condensateur dudit moyen (13-1, 13-2) de maintien.

4. Dispositif d'affichage de type à matrice active selon la revendication 3, dans lequel ledit second (16) et quatrième (12-1, 12-2) TEC constituent ensemble un circuit miroir de courant.

5. Dispositif d'affichage de type à matrice active selon la revendication 3, dans lequel ledit premier ou second TEC (14, 16) est un organe de transistor simple.

6. Dispositif d'affichage de type à matrice active selon la revendication 3, dans lequel ledit premier ou second TEC (14-1, 14-2 ou 16-1, 16-2) comprend une multiplicité d'organes de transistor ayant lesdits drains et lesdites grilles connectés ensemble.

7. Dispositif d'affichage de type à matrice active selon l'une quelconque des revendications 1 à 6, dans lequel ledit dispositif d'affichage est un dispositif d'affichage électroluminescent organique.

8. Procédé d'entraînement d'un dispositif d'affichage électroluminescent à matrice active comprenant un agencement en matrice d'organes (11-1, 11-2) électro-optiques électroluminescents agencés en rangées et colonnes comprenant des circuits (P1, P2) de pixels adaptés pour fournir un courant arrivant depuis une ligne (17) de données jusqu'auxdits organes électro-optiques électroluminescents dont la luminance varie avec le courant y passant, lesdits circuits (P1, P2) de pixels comprenant :

- un premier interrupteur (14) à balayage pour faire passer de manière sélective le courant fourni depuis ladite ligne (17) de données ;
- un moyen (16) de conversion pour convertir le courant fourni au travers dudit premier interrupteur (14) à balayage en une tension ;
- un second interrupteur (15, 15-1, 15-2) à balayage pour faire passer de manière sélective la tension convertie par ledit moyen (16) de conversion ;
- un moyen (13-1, 13-2) de maintien pour maintenir la tension qui y est alimentée au travers dudit second interrupteur (15, 15-1, 15-2) à balayage et
- un moyen (12-1, 12-2) d'entraînement pour convertir la tension maintenue dans ledit moyen (13-1, 13-2) de maintien en un courant et faire passer le courant converti au travers dudit organe (11-1, 11-2) électro-optique, dans lequel ledit premier interrupteur (14) à balayage et ledit moyen (16) de conversion sont mis à disposition en commun pour au moins deux circuits (P1, P2) de pixels séparés appartenant à la même colonne du dispositif d'affichage à matrice, ledit premier interrupteur (14) à balayage étant connecté à une électrode du moyen (16) de conversion

le procédé étant **caractérisé en ce que** par l'étape consistant à :

régler ledit premier interrupteur (14) à balayage sur un état sélectif et, au cours d'une période durant laquelle ledit premier interrupteur (14) à balayage maintient ledit état sélectif, commuter de manière séquentielle vers un état sélectif ledit second interrupteur (15-1) à balayage dudit premier circuit (P1) de pixels et ledit second interrupteur (15-2) à balayage dudit autre circuit (P2) de pixels.

9. Procédé selon la revendication 8, dans lequel ledit dispositif d'affichage de type à matrice active est un dispositif d'affichage électroluminescent organique.

FIG. 1
(PRIOR ART)

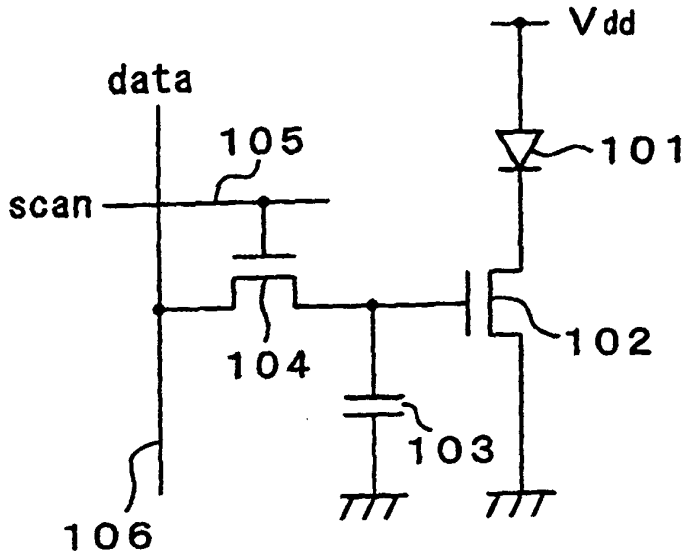


FIG. 3
(PRIOR ART)

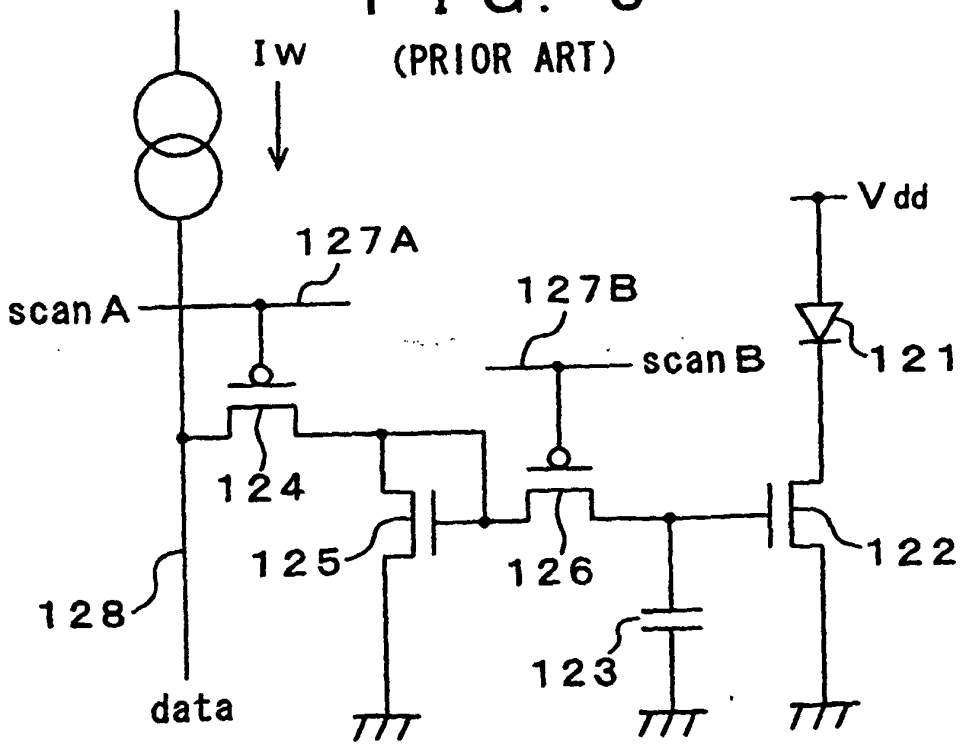
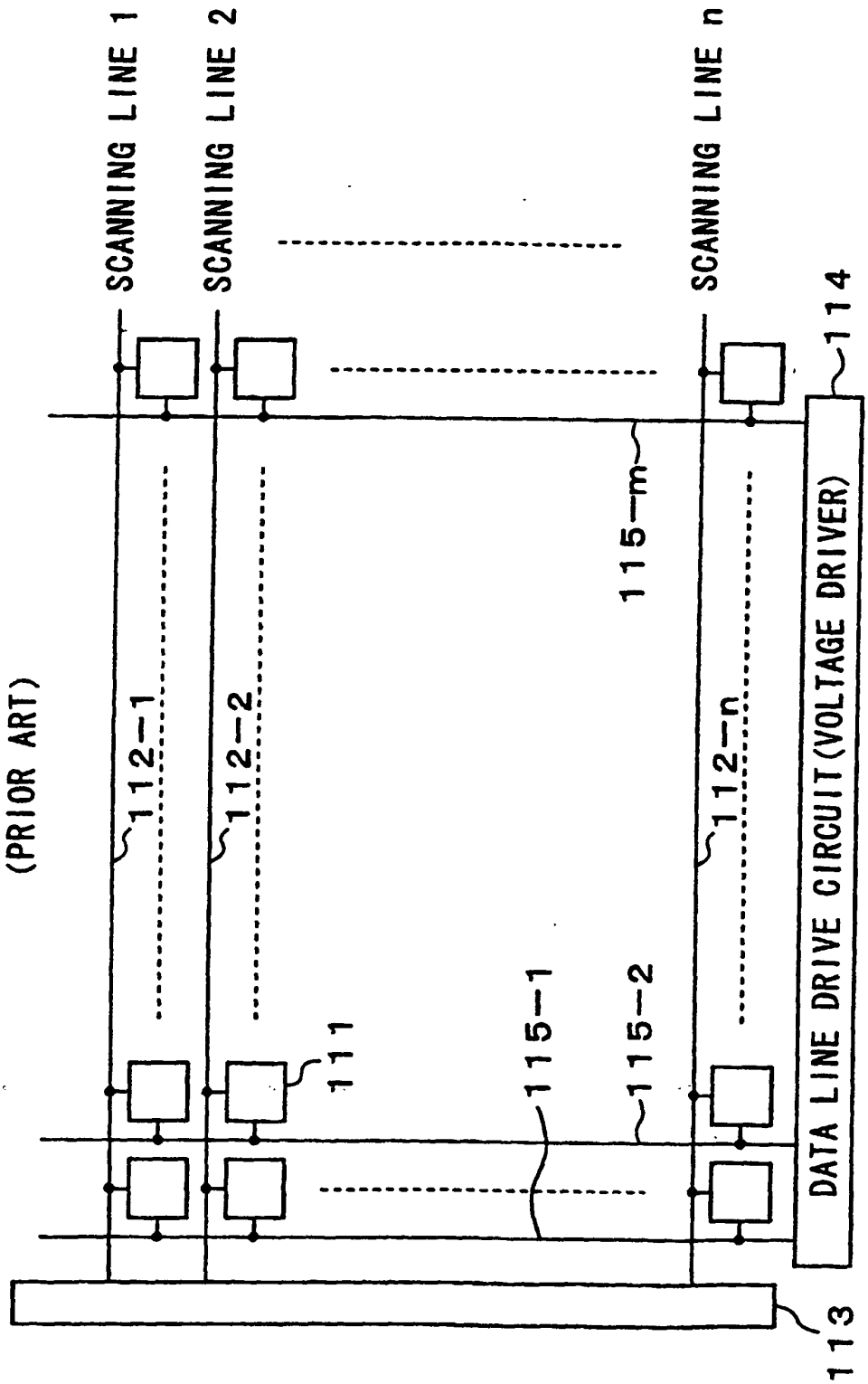


FIG. 2
(PRIOR ART)



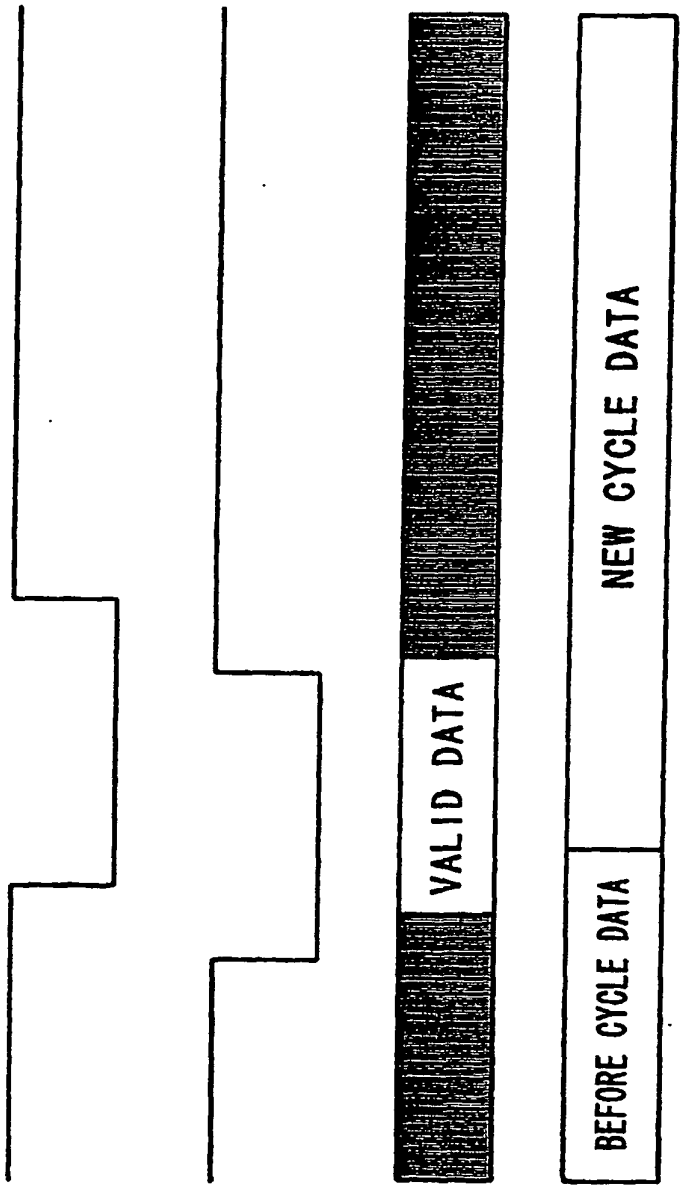


FIG. 4A (PRIOR ART)

FIG. 4B (PRIOR ART)

FIG. 4C (PRIOR ART)

FIG. 4D (PRIOR ART)

FIG. 5
(PRIOR ART)

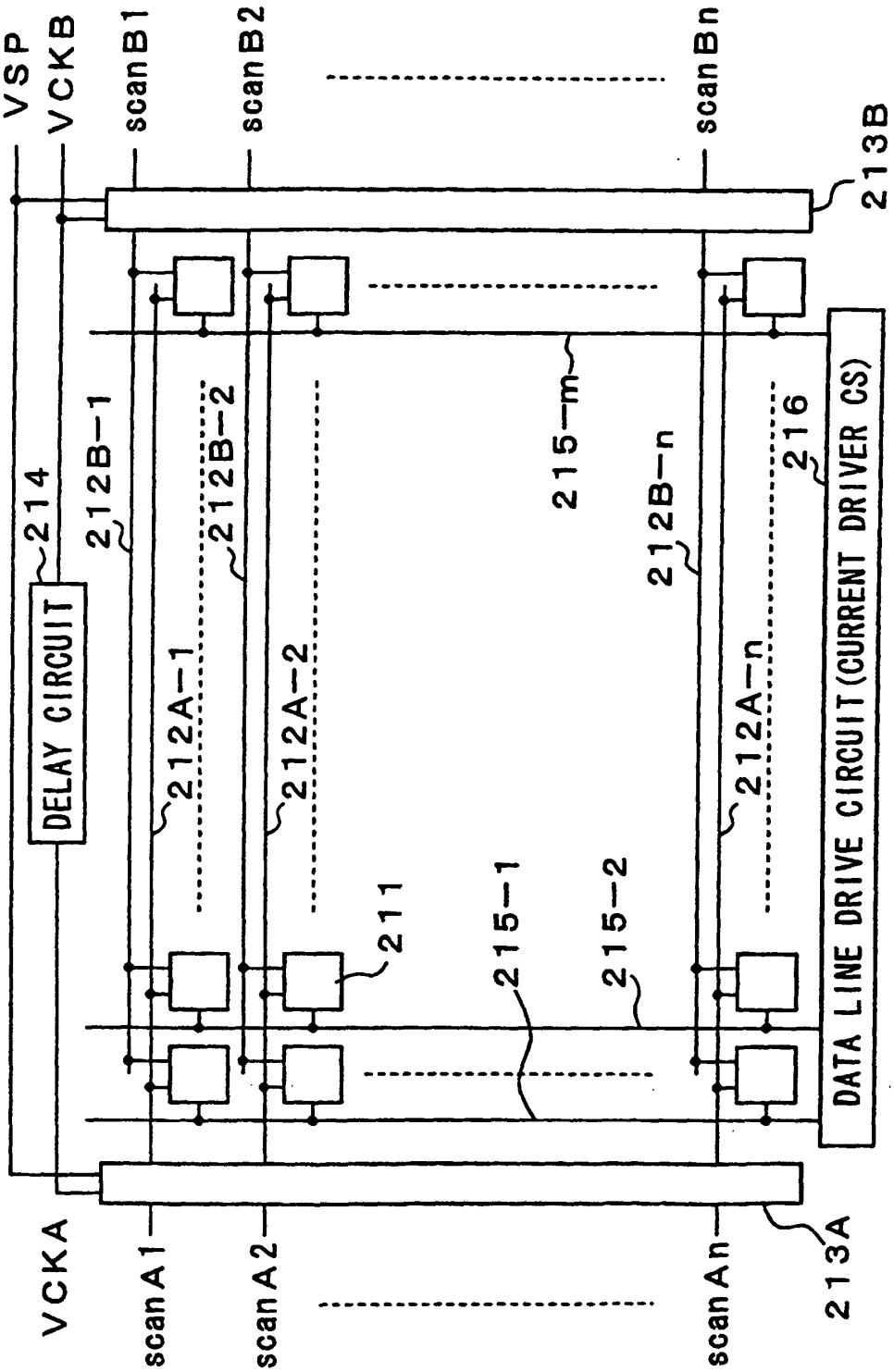


FIG. 6

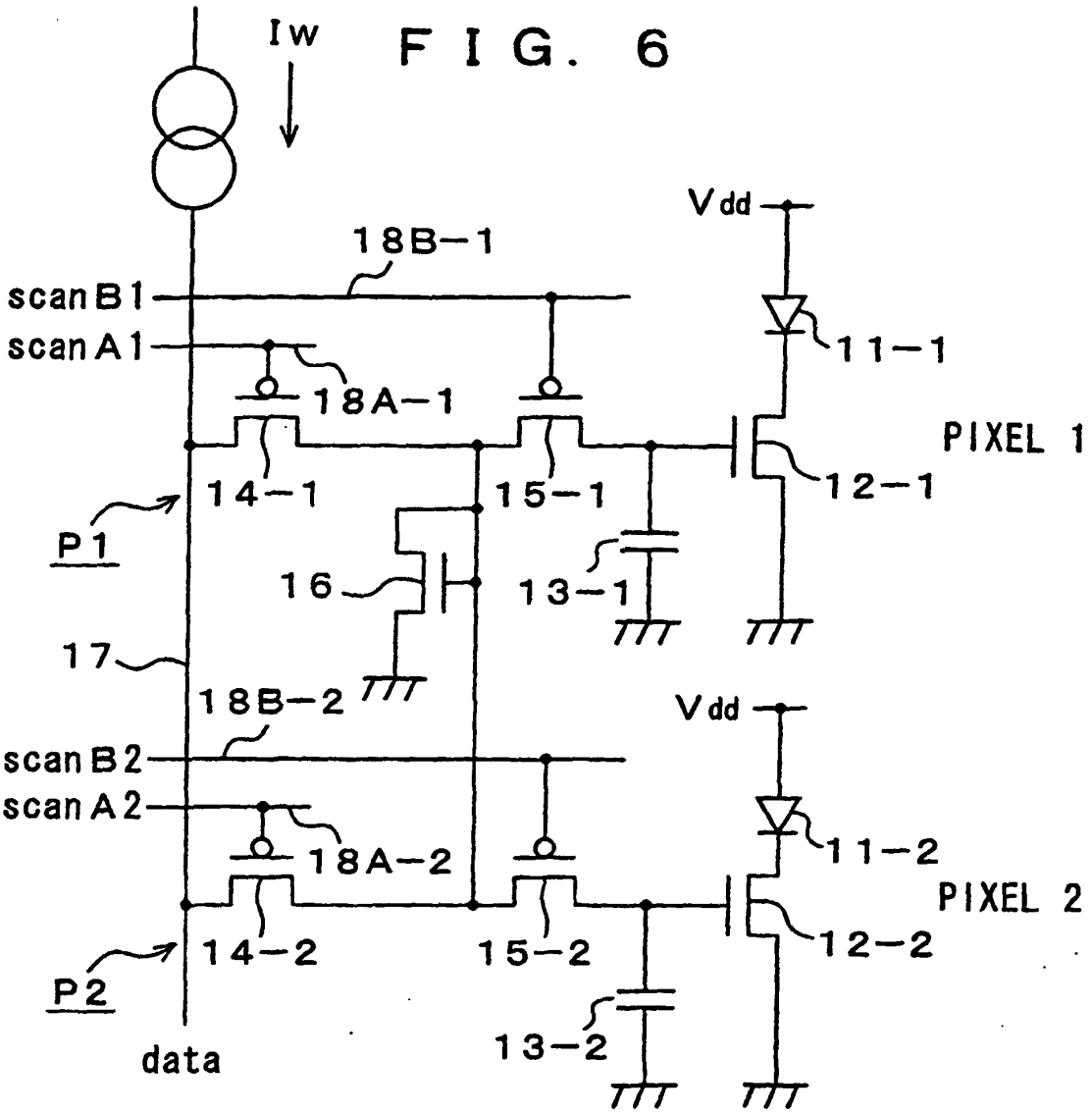

Iw
Vdd
18B-1
scanB1
scanA1
11-1
18A-1
PIXEL 1
14-1
15-1
12-1
P1
16
13-1
17
18B-2
Vdd
scanB2
scanA2
11-2
18A-2
PIXEL 2
14-2
15-2
12-2
P2
13-2
data

FIG. 7

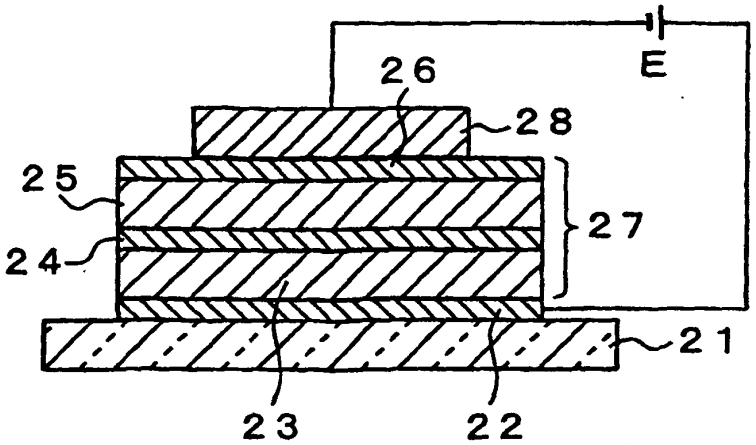

E
26
28
25
27
24
21
23
22

FIG. 8

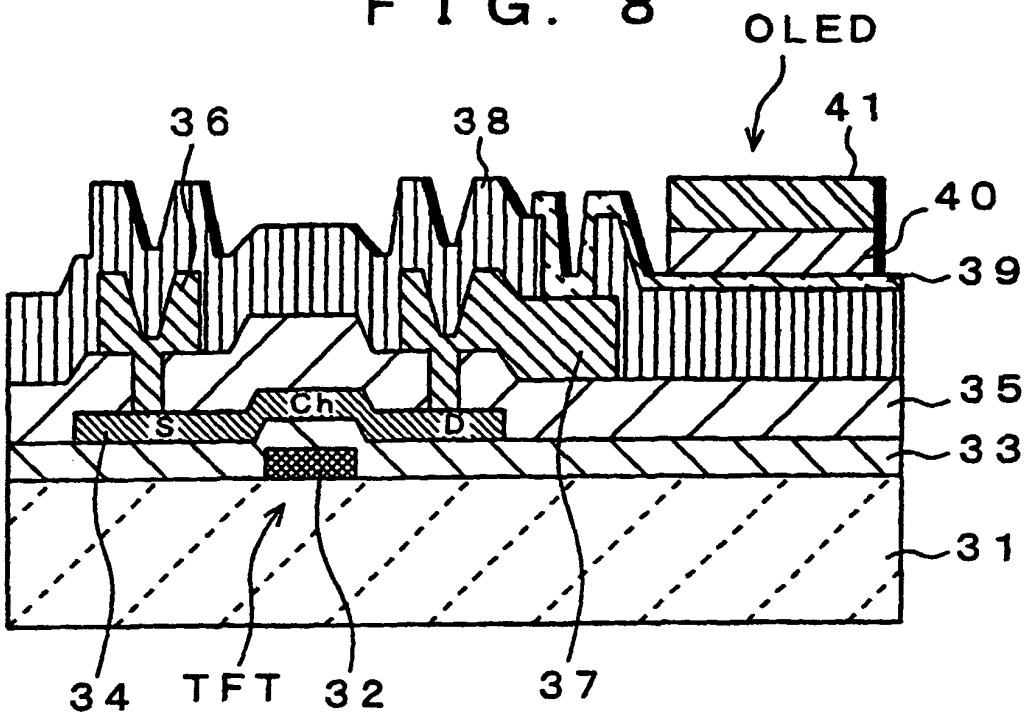

OLED
36
38
41
40
39
35
Ch
S
D
33
31
34
TFT
32
37

FIG. 9

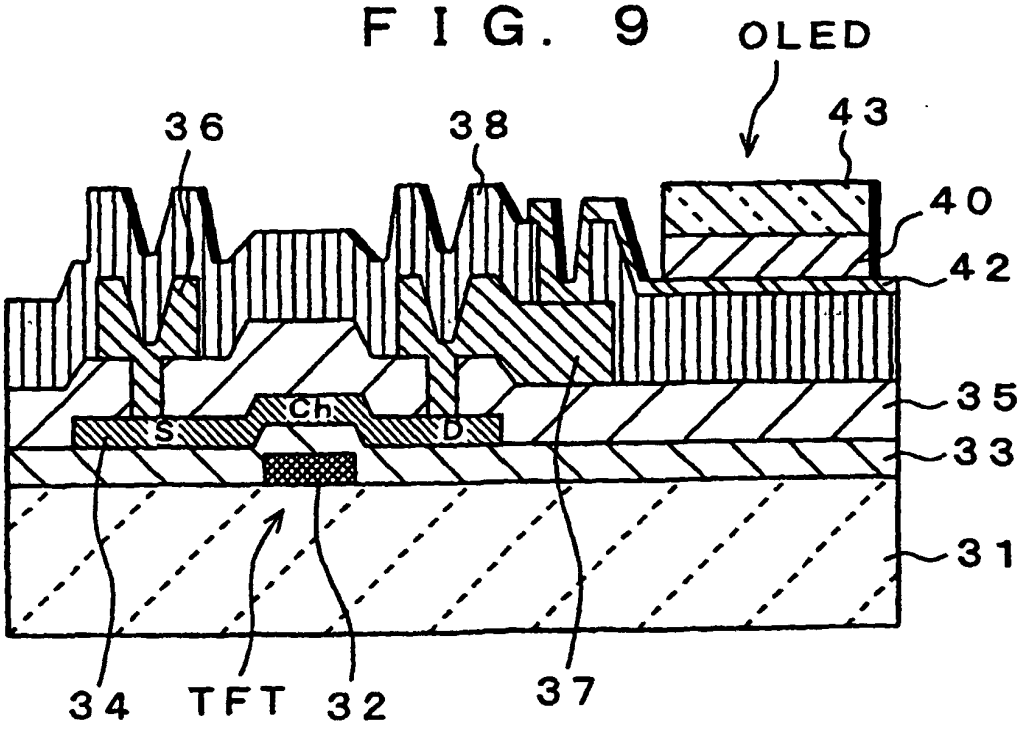

OLED
36
38
43
40
42
35
Ch
S
D
33
31
34
TFT
32
37

FIG. 10

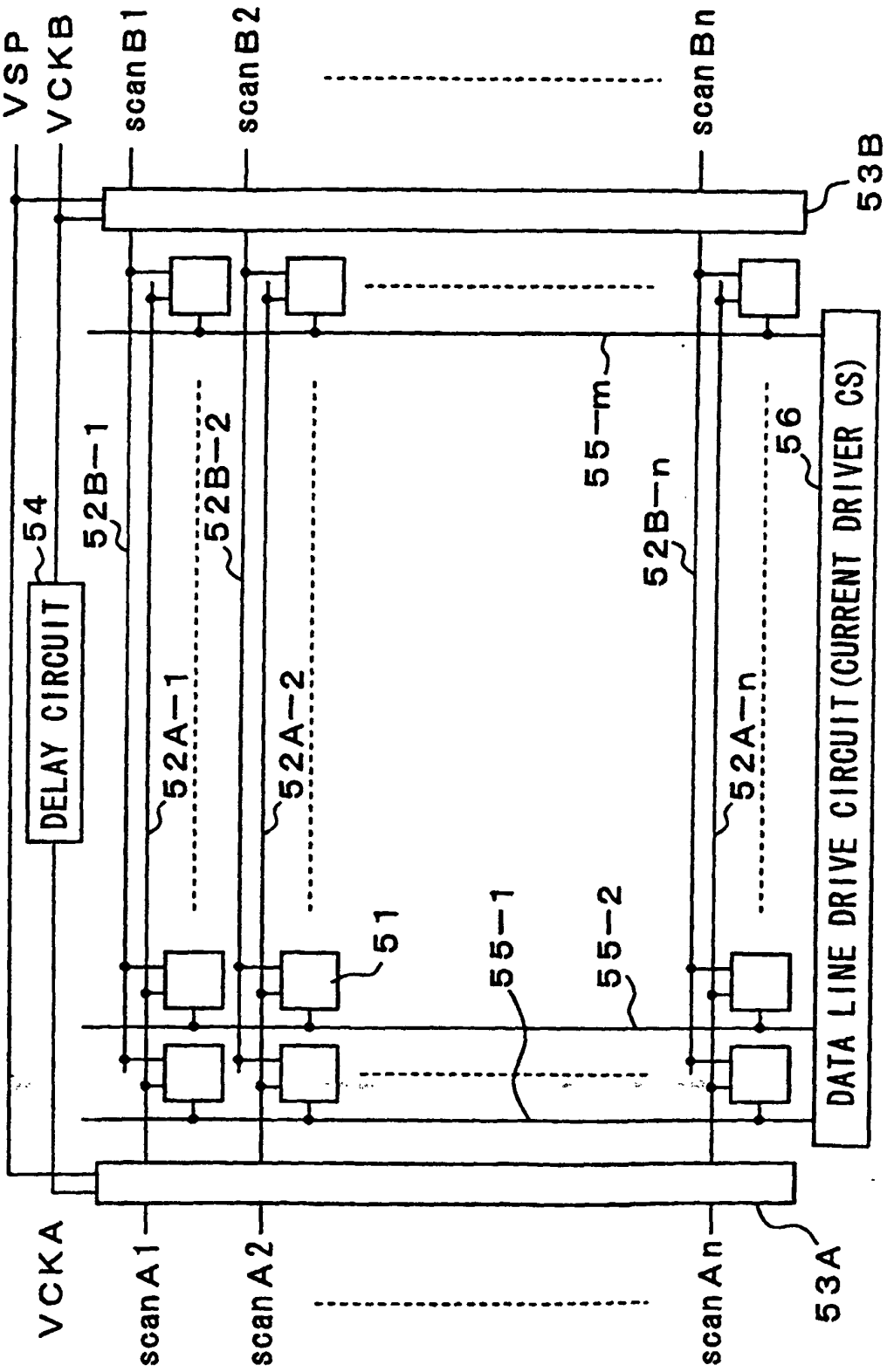

VSP
VCKB
scanB1
scanB2
scanBn
53B
54
DELAY CIRCUIT
52B-1
52B-2
52B-n
55-m
56
52A-1
52A-2
52A-n
51
55-1
55-2
DATA LINE DRIVE CIRCUIT (CURRENT DRIVER CS)
VCKA
scanA1
scanA2
scanAn
53A

FIG. 11

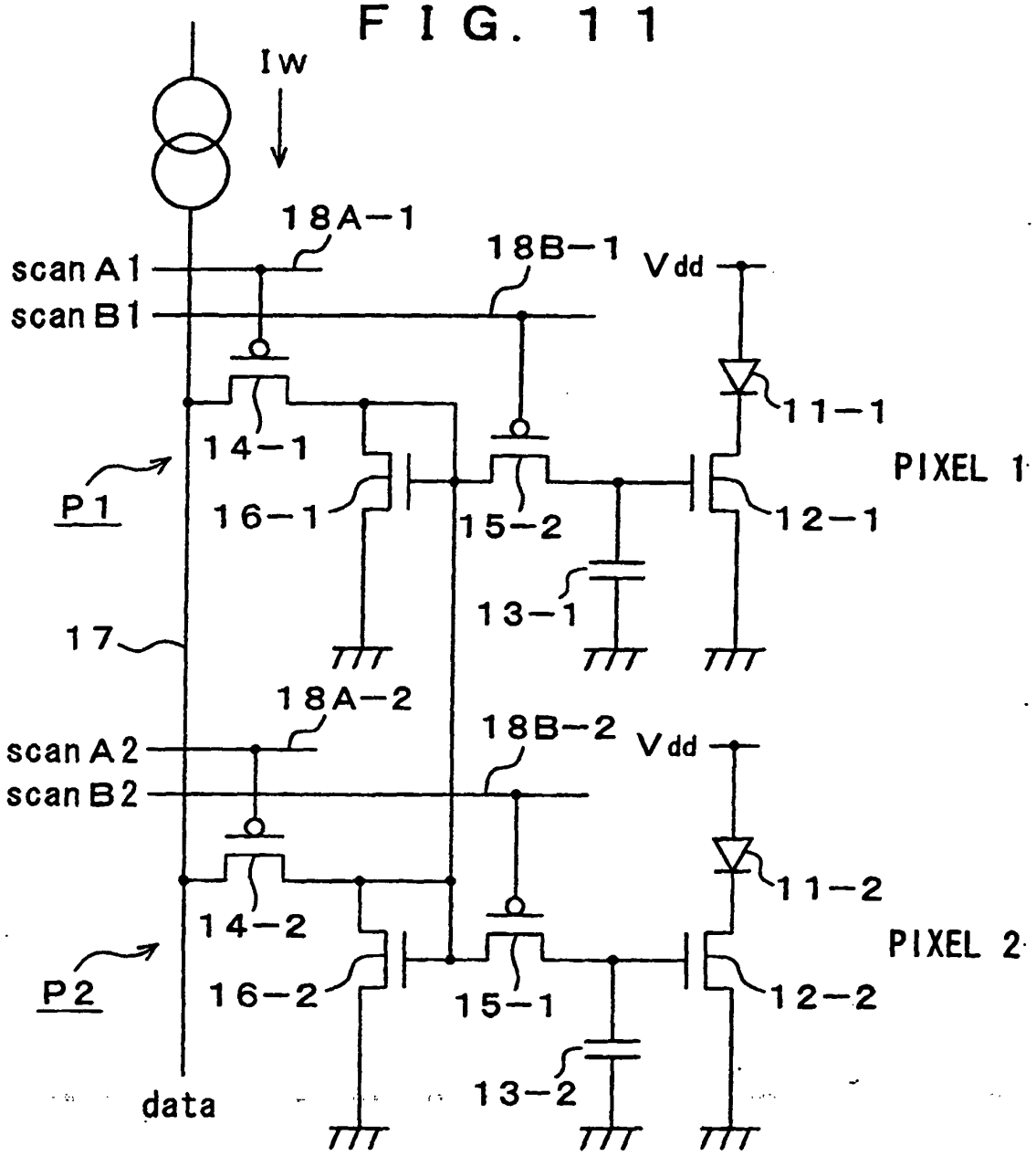

Iw
18A-1
18B-1
Vdd
scan A1
scan B1
11-1
14-1
PIXEL 1
P1
16-1
15-2
12-1
13-1
17
18A-2
18B-2
Vdd
scan A2
scan B2
11-2
14-2
PIXEL 2
P2
16-2
15-1
12-2
13-2
data

FIG. 12

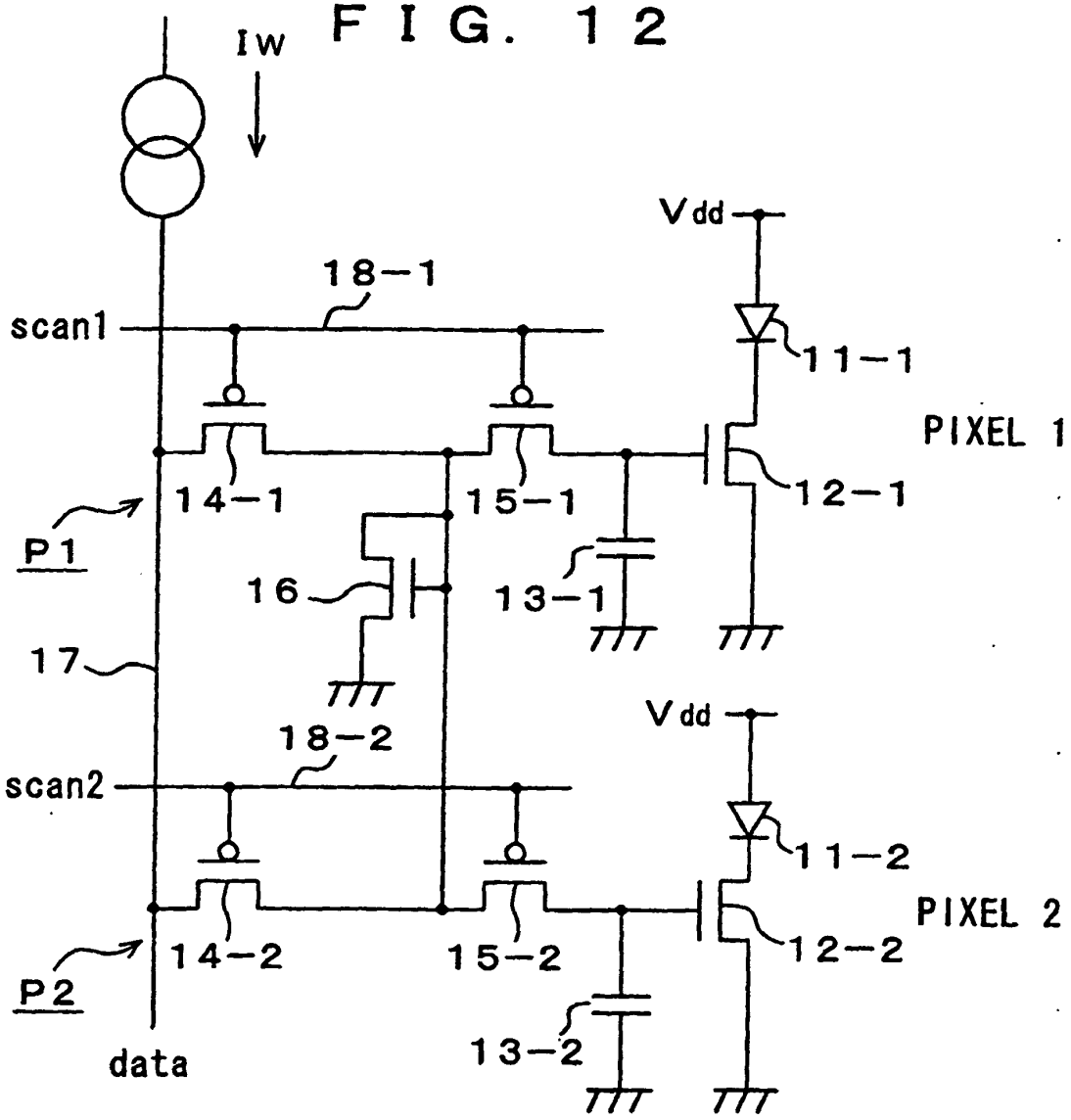

Iw
Vdd
18-1
scan1
11-1
PIXEL 1
14-1
15-1
12-1
P1
16
13-1
17
Vdd
18-2
scan2
11-2
PIXEL 2
14-2
15-2
12-2
P2
13-2
data

FIG. 13

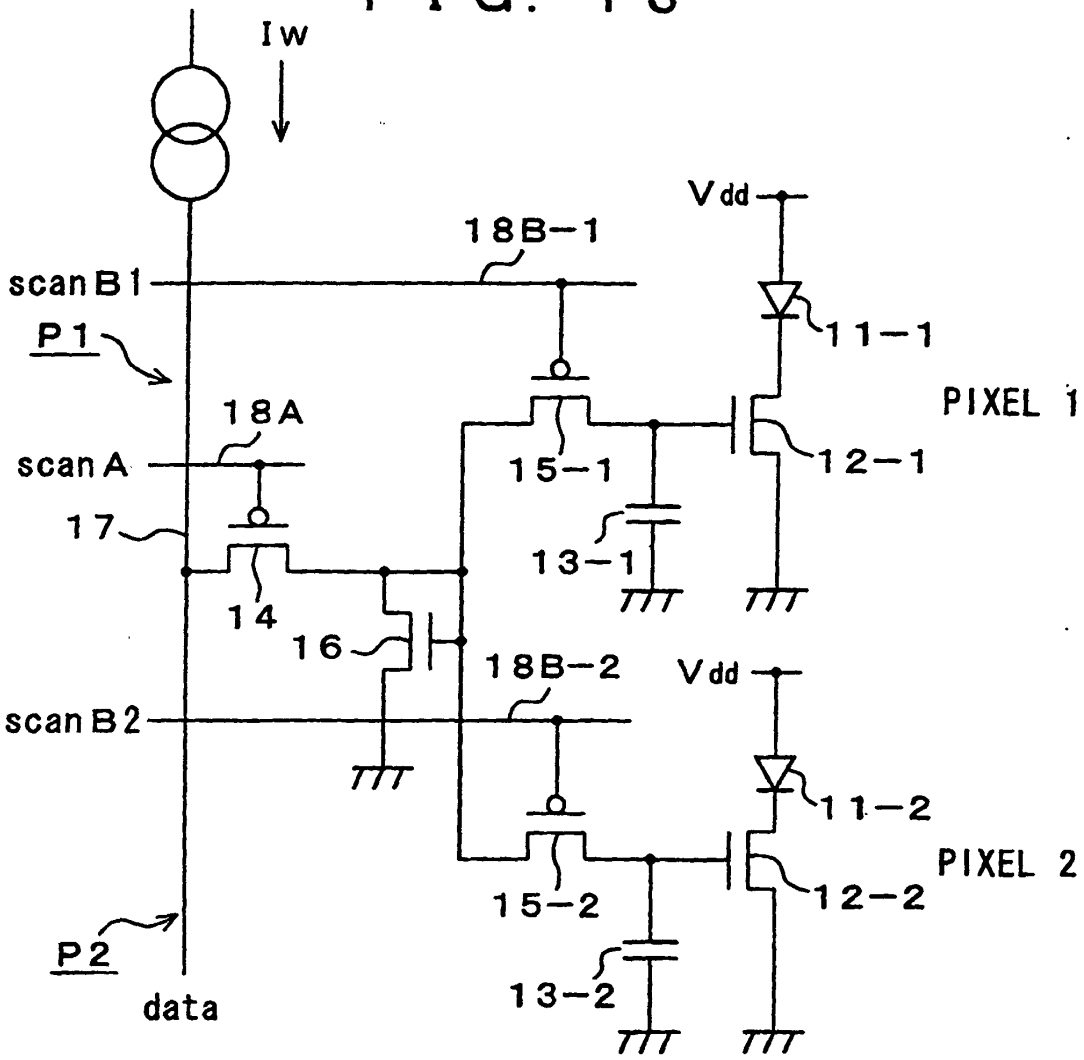
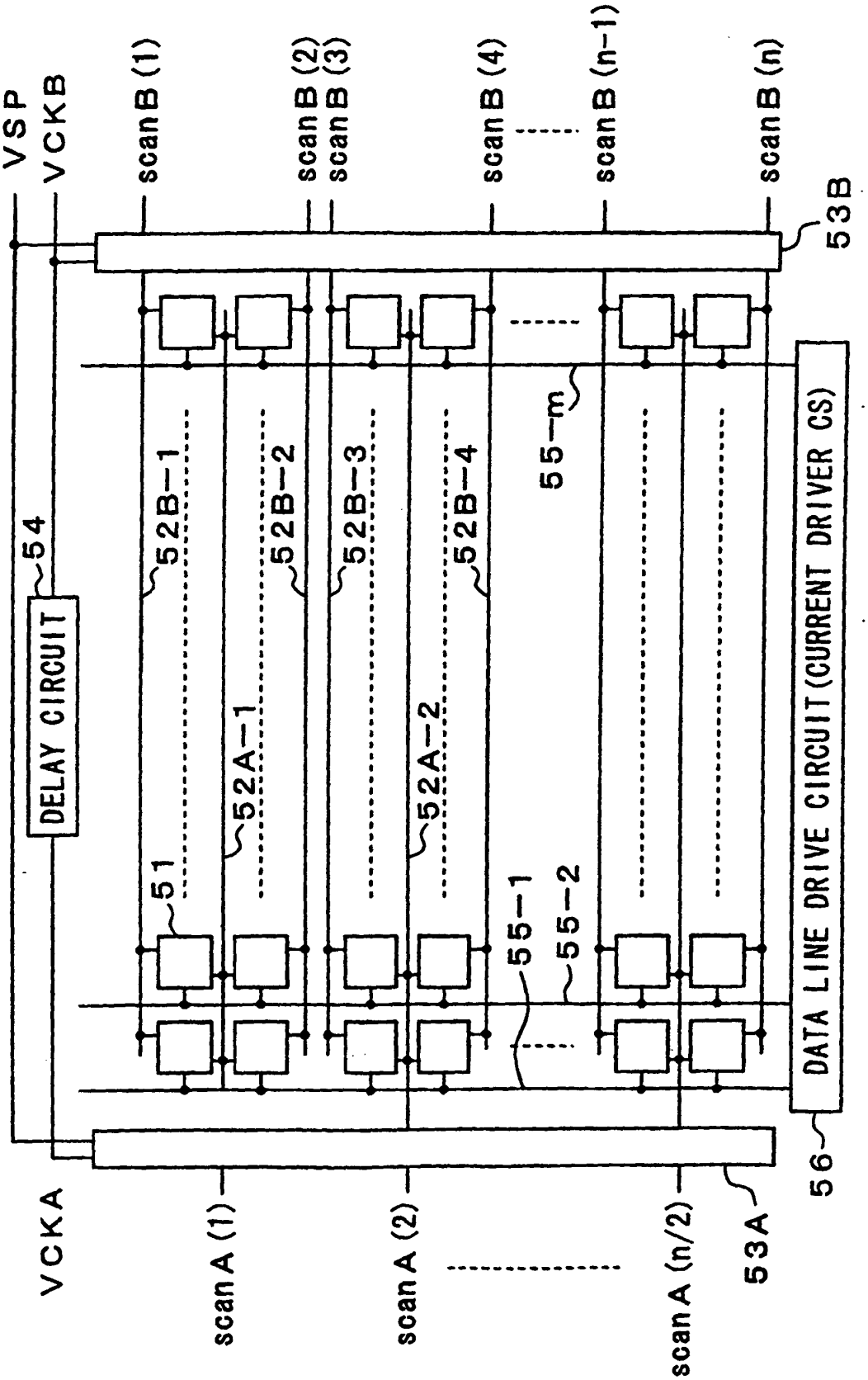

Iw
Vdd
18B-1
scanB1
P1
11-1
PIXEL 1
18A
scanA
15-1
12-1
17
13-1
14
16
18B-2
Vdd
scanB2
11-2
PIXEL 2
15-2
12-2
P2
13-2
data

FIG. 14


VSP
VCKB
scanB (1)
scanB (2)
scanB (3)
scanB (4)
scanB (n-1)
scanB (n)
53B
54
DELAY CIRCUIT
52B-1
52B-2
52B-3
52B-4
55-m
52A-1
52A-2
51
55-1
55-2
DATA LINE DRIVE CIRCUIT (CURRENT DRIVER CS)
56
VCKA
scanA (1)
scanA (2)
scanA (n/2)
53A

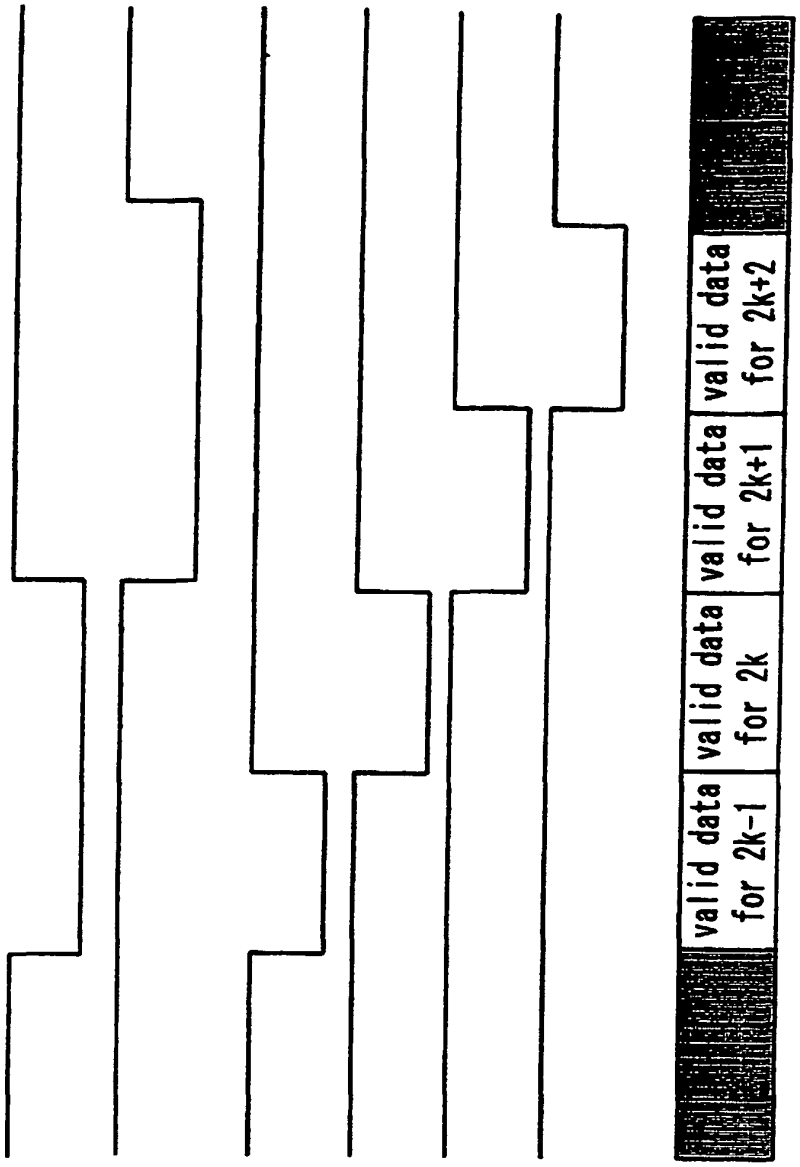


FIG. 15A scan A (k)

FIG. 15B scan A (k+1)

FIG. 15C scan B (2k-1)

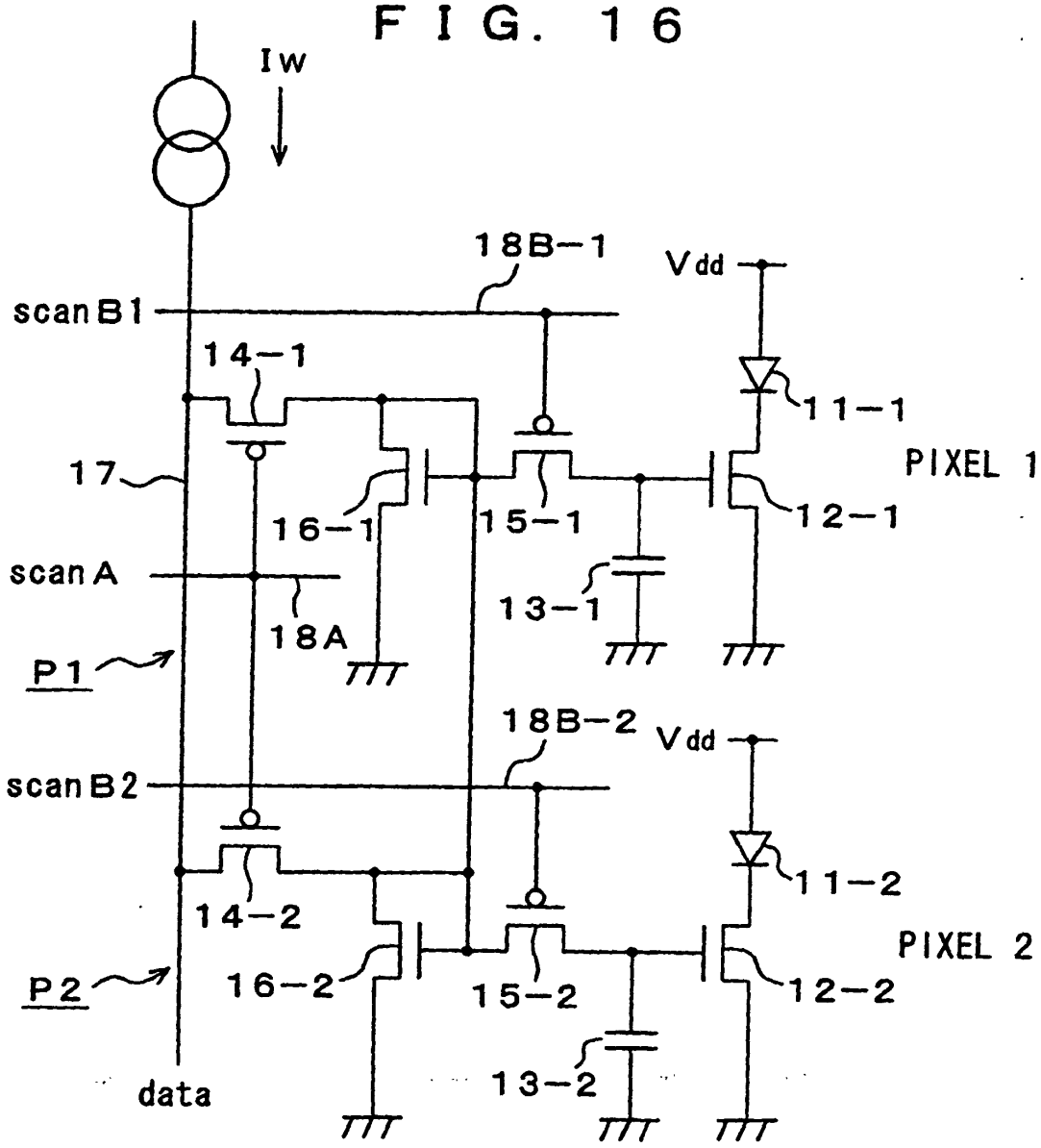
FIG. 15D scan B (2k)

FIG. 15E scan B (2k+1)

FIG. 15F scan B (2k+2)

FIG. 15G CURRENT FROM CS

FIG. 16


Iw
18B-1
Vdd
scanB1
14-1
11-1
17
PIXEL 1
16-1
15-1
12-1
scanA
13-1
18A
P1
18B-2
Vdd
scanB2
11-2
14-2
PIXEL 2
P2
16-2
15-2
12-2
13-2
data

专利名称(译)	有源矩阵显示器，有源矩阵有机电致发光显示器以及驱动它们的方法		
公开(公告)号	EP1353316B1	公开(公告)日	2005-11-09
申请号	EP2002729561	申请日	2002-01-11
[标]申请(专利权)人(译)	索尼公司		
申请(专利权)人(译)	索尼公司		
当前申请(专利权)人(译)	索尼公司		
[标]发明人	ASANO MITSURU C O SONY CORPORATION		
发明人	YUMOTO, AKIRA, C/O SONY CORPORATION ASANO, MITSURU, C/O SONY CORPORATION		
IPC分类号	H01L51/50 G09F9/30 G09G3/20 G09G3/30 G09G3/32 H01L27/32 H05B33/14 H05B33/08		
CPC分类号	G09G3/30 G09G3/3241 G09G3/3266 G09G2300/0465 G09G2300/0804 G09G2300/0842 G09G2310/0262		
优先权	2001006387 2001-01-15 JP		
其他公开文献	EP1353316A4 EP1353316A1		
外部链接	Espacenet		

摘要(译)

当制作电流写入型像素电路时，它涉及更多数量的晶体管，并且TFT占据像素电路的大部分区域。为了解决这个问题，两个像素电路（P1，P2）具有第一扫描TFT（14），电流 - 电压转换TFT（16），相应的第二扫描TFT（15-1,15-2），电容器（13-例如，在行方向上驱动包括两个像素的有机EL元件（11-2,11-2）的OLED的驱动TFT（12-1,12-2）。在每个像素电路中，与流过OLED（11-2,11-2）的电流和电流 - 电压转换TFT（16）相比，第一扫描TFT（14）处理大量电流（Iw）。 ）在两个像素之间共享。