(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 483 872 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
15.05.2019 Bulletin 2019/20

(51) Int Cl.:
G09G 3/3233 *(2016.01)*

(21) Application number: **18202278.0**

(22) Date of filing: **24.10.2018**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(30) Priority: **10.11.2017 KR 20170149552**

(71) Applicant: **LG Display Co., Ltd.**
SEOUL, 07336 (KR)

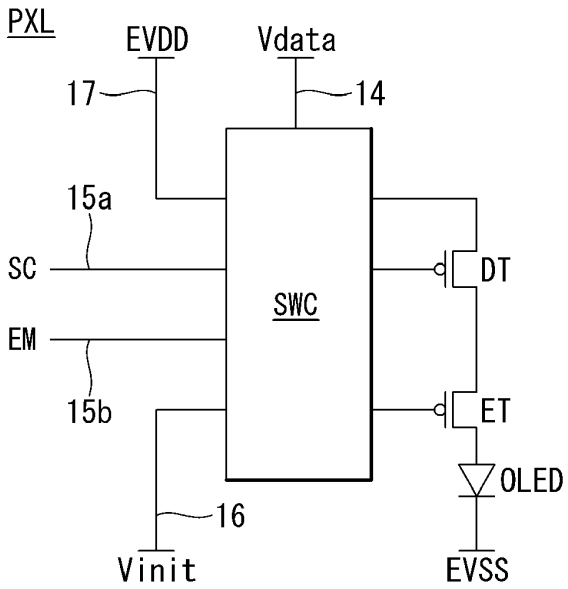
(72) Inventors:
- **RHA, Sunghoon**
  10845 Paju-si Gyeonggi-do (KR)
- **JEON, Changhoon**
  10845 Paju-si Gyeonggi-do (KR)
- **BAE, Hyungguk**
  10845 Paju-si Gyeonggi-do (KR)

(74) Representative: **Viering, Jentschura & Partner mbB**
Patent- und Rechtsanwälte
Am Brauhaus 8
01099 Dresden (DE)

(54) ELECTROLUMINESCENT DISPLAY DEVICE AND DRIVING METHOD OF THE SAME

(57) The electroluminescent display device according to the present disclosure comprises a plurality of pixels (PXL). Each of the plurality of pixels (PXL) comprises a driving element (DT) for generating a driving current, a light emitting element (OLED) for emitting light according to the driving current, an emission controlling element (ET) for controlling a flow of the driving current between the driving element (DT) and the light emitting element (OLED), and a switching circuit (SWC) for setting a first gate-source voltage of the driving element (DT) corresponding to the driving current based on a first data voltage (VI) during a first period and setting a second gate-source voltage of the driving element (DT) based on a second data voltage (Vk) different from the first data voltage (V1) during a second period following the first period, wherein the second gate-source voltage is different from the first gate-source voltage, and wherein during the second period the emission controlling element (ET) is turned off.

FIG. 3



EP 3 483 872 A1

Description

BACKGROUND

Field of the Technology

[0001] The present document relates to an electroluminescent display device and a method for driving the electroluminescent display device.

Discussion of the Related Art

[0002] The electroluminescent display device is classified into an inorganic light emitting display device and an organic light emitting display device according to the material of a light emitting layer. The organic light emitting display device of an active matrix type includes an organic light emitting diode OLED which emits light itself, and has the advantages of high response speed, high luminous efficiency, high luminance and wide viewing angle.

[0003] The organic light emitting display device arranges the pixels each of which includes the OLED in a matrix form and adjusts the luminance of the pixels according to gradation of image data. Each pixel includes a driving TFT (Thin Film Transistor), which controls the driving current flowing through the OLED according to the voltage between a gate electrode and a source electrode, and one or more switching TFTs for programming the voltage between the gate electrode and the source electrode of the driving TFT, and adjusts the display luminance by emitting the OLED with a luminance proportional to the driving current.

[0004] The driving characteristics of the pixel such as the threshold voltage of the driving TFT must be the same in all the pixels, in order to realize uniform image quality without luminance and color difference between pixels. However, there may be a deviation in the driving characteristics between pixels due to a process variation. In addition, as the driving time of a display device elapses, the deterioration progress speeds of pixels become different from each other, and the differences in the driving characteristics between pixels may become large. Such a driving characteristic deviation can change the amount of driving current flowing to the OLED, resulting in image quality irregularity between pixels.

[0005] In order to improve the image quality and lifetime of a display device, an internal compensation circuit for compensating for the differences in driving characteristics between pixels is applied to the organic light emitting display device. The internal compensation circuit may be implemented inside the pixel. The organic light emitting display device uses the compensation circuits implemented in pixels, to sample the gate-source voltage of the driving TFT which varies according to the threshold voltage of the driving TFT and compensate for the variation of the threshold voltage of the driving TFT based on the sampled voltage.

SUMMARY

[0006] The driving current determining the emitting luminescence of the OLED depends on the gate-source voltage of the driving TFT. The gate-source voltage of the driving TFT is updated every frame in accordance with the writing period of a data voltage. However, when same image is displayed on a pixel for a long time, a hysteresis phenomenon occurs because the gate-source voltage of the driving TFT included in the pixel does not change. Such the hysteresis phenomenon may induce a DC afterimage and lowers display quality. The longer the time during which the gate-source voltage of the driving TFT is maintained at a same value, the stronger the hysteresis phenomenon becomes.

[0007] Accordingly, an objective of the present disclosure is to provide an electroluminescent display device and a driving method for the same which can improve the hysteresis phenomenon of the driving TFT and enhance display quality.

[0008] Various embodiments of the present disclosure provide an electroluminescent display device and a method of driving an electroluminescent display device as described in the independent claims. Further embodiments are described in the dependent claims. An electroluminescent display device according to the present disclosure may comprise a plurality of pixels. Each of the plurality of pixels comprises a driving element for generating a driving current, a light emitting element for emitting light according to the driving current, an emission controlling element for controlling a flow of the driving current between the driving element and the light emitting element, and a switching circuit for setting a first gate-source voltage of the driving element corresponding to the driving current based on a first data voltage during a first period and setting a second gate-source voltage of the driving element based on a second data voltage different from the first data voltage during a second period following the first period, the second gate-source voltage being different from the first gate-source voltage, and during the second period the emission controlling element is turned off.

[0009] The second gate-source voltage may be for changing the on-biased state of the driving element to compensate a hysteresis phenomenon of the driving element, and the switching circuit may set the second gate-source voltage a plurality of times based on a plurality of data voltages including the second data voltage during the second period.

[0010] The driving element may become a first on-biased state by the first gate-source voltage and become a second

on-biased state by the second gate-source voltage, and the first on-biased state and the second on-biased state may be different from each other.

[0011] The second data voltage may be applied to another pixel during the second period, and a first gate-source voltage of a driving element included in the another pixel may be set according to the second data voltage.

[0012] During the emission controlling element is turned on within the first period, the light emitting element may emit light by the driving current applied through the emission controlling element, and the first and second periods may be included in one frame.

[0013] The electroluminescent display device may further comprise a source driver for generating the first data voltage to supply to a data line connected to the plurality of pixels within the first period, and generating the second data voltage to supply the data line within the second period; and a gate driver for generating a first pulse of a first scan signal synchronized with the first data voltage to supply to a first gate line connected to the plurality of pixels within the first period, generating a second pulse of a first scan signal synchronized with the second data voltage to supply to the first gate line within the second period, and generating a first pulse of a second scan signal synchronized with the second data voltage to supply to a second gate line connected to the plurality of pixels within the second period.

[0014] A gate electrode, a first electrode and a second electrode of the driving element may be respectively connected to a second node, a first node and a third node, the emission controlling element may be connected between the third node and a fourth node, the light emitting element may be connected between the fourth node and an input terminal of a low potential power voltage, and the switching circuit may be connected to the data line through which the first and second data voltages are supplied, a first power line through which an initializing voltage is supplied, and a second power line through which a high potential power voltage is supplied.

[0015] The switching circuit may comprise a first switching element connected between the first node and the data line, a second switching element connected between the first node and the second power line, a third switching element connected to the second node and the third node, a fourth switching element connected to the second node and the first power line, a fifth switching element connected to the fourth node and the first power line and a storage capacitor connected between the second power line and the second node.

[0016] The fourth switching element may be switched according to an (n-1)th scan signal, the first, third and fifth switching elements may be switched according to an nth scan signal, the nth scan signal being later than the (n-1)th scan signal in their phases of an on period, the emission controlling element and the second switching element may be switched according to an nth emission signal, the (n-1)th scan signal and the nth scan signal may be respectively input as an on level in the first period and the second period sequentially, and the nth emission signal may be input as an off level in the first and second periods and input as the on level in a third period between the first period and the second period.

[0017] The present disclosure also provides a method of driving an electroluminescent display device equipped with a plurality of pixels, each of the plurality of pixels comprising a driving element for generating a driving current, a light emitting element for emitting light according to the driving current and an emission controlling element for controlling a flow of the driving current between the driving element and the light emitting element, the method comprising: setting a first gate-source voltage of the driving element corresponding to the driving current based on a first data voltage during a first period; and setting a second gate-source voltage of the driving element based on a second data voltage different from the first data voltage during a second period following the first period, the second gate-source voltage being different from the first gate-source voltage, and during the second period the emission controlling element is turned off.

[0018] The second gate-source voltage may be for changing the on-biased state of the driving element to compensate a hysteresis phenomenon of the driving element, and the setting a second gate-source voltage of the driving element may include setting the second gate-source voltage a plurality of times based on a plurality of data voltages including the second data voltage during the second period.

[0019] The driving element may become (in other words, assume) a first on-biased state by the first gate-source voltage and may become (in other words, assume) a second on-biased state by the second gate-source voltage, and the first on-biased state and the second on-biased state may be different from each other.

[0020] The second data voltage may be applied to another pixel during the second period, and a first gate-source voltage of a driving element included in the another pixel may be set according to the second data voltage.

[0021] during the emission controlling element is turned on within the first period, the light emitting element may emit light by the driving current applied through the emission controlling element, and the first and second periods may be included in one frame.

[0022] The method may further comprise: generating the first data voltage to supply to a data line connected to the plurality of pixels within the first period, and generating the second data voltage to supply the data line within the second period; generating a first pulse of a first scan signal synchronized with the first data voltage to supply to a first gate line connected to the plurality of pixels within the first period; and generating a second pulse of the first scan signal synchronized with the second data voltage to supply to the first gate line within the second period, and generating a first pulse of a second scan signal synchronized with the second data voltage to supply to a second gate line connected to the plurality of pixels within the second period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a block diagram illustrating an electroluminescent display device according to an embodiment of the present disclosure.
FIG. 2 is a diagram illustrating a pixel array of an electroluminescent display device according to an embodiment of the present disclosure.
FIG. 3 is a diagram schematically showing an equivalent circuit of the pixel shown in FIG. 2.
FIG. 4 is a waveform diagram showing an example of the multi-scan driving method for improving hysteresis phenomenon.
Fig. 5 is a waveform diagram showing another example of the multi-scan driving method for improving hysteresis phenomenon.
FIG. 6 shows that an afterimage is improved according to the multi-scan driving method.
FIG. 7 specifically shows the equivalent circuit of the pixel shown in FIG. 2.
FIG. 8 is a waveform diagram showing driving signals input to the pixel of FIG. 7 and potential changes of specific pixel nodes according to the driving signals.
FIG. 9A is an equivalent circuit diagram showing the operation of the pixel during a first initializing period of FIG. 8.
FIG. 9B is an equivalent circuit diagram showing the operation of the pixel during a first sampling period of FIG. 8.
FIG. 9C is an equivalent circuit diagram showing the operation of the pixel during an emission period of FIG. 8.
FIG. 9D is an equivalent circuit diagram showing the operation of the pixel during a second initializing period of FIG. 8.
FIG. 9E is an equivalent circuit diagram showing the operation of the pixel during a second sampling period of FIG. 8.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0024] The advantages and features of the present disclosure and methods of accomplishing the same may be understood more readily by reference to the following detailed descriptions of exemplary embodiments and the accompanying drawings. The present disclosure may, however, be embodied in many different forms and should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the present disclosure to those skilled in the art, and the present disclosure is defined by the appended claims.

[0025] The shapes, sizes, percentages, angles, numbers, etc. shown in the figures to describe the exemplary embodiments of the present disclosure are merely examples and not limited to those shown in the figures. Like reference numerals denote like elements throughout the specification. In describing the present disclosure, detailed descriptions of related well-known technologies will be omitted to avoid unnecessary obscuring the present disclosure. When the terms 'comprise', 'have', 'consist of' and the like are used, other parts may be added as long as the term 'only' is not used. The singular forms may be interpreted as the plural forms unless explicitly stated.

[0026] The elements may be interpreted to include an error margin even if not explicitly stated.

[0027] When the position relation between two parts is described using the terms 'on', 'over', 'under', 'next to' and the like, one or more parts may be positioned between the two parts as long as the term 'immediately' or 'directly' is not used.

[0028] It will be understood that, although the terms first, second, etc., may be used to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element referred to below may be a second element within the scope of the present disclosure.

[0029] Like reference numerals denote like elements throughout the specification.

[0030] The features of various exemplary embodiments of the present disclosure may be combined with one another either partly or wholly, and may technically interact or work together in various ways. The exemplary embodiments may be carried out independently or in combination with one another.

[0031] In this specification, the pixel circuit formed on the substrate of a display panel may be implemented by a TFT of a p-type MOSFET structure, but the present disclosure is not limited thereto. The TFT or the transistor is the element of 3 electrodes including a gate, a source and a drain. The source is an electrode for supplying a carrier to the transistor. Within the TFT the carrier begins to flow from the source. The drain is an electrode from which the carrier exits the TFT. That is, the flow of carriers in the MOSFET is from the source to the drain. In the case of a P-type MOSFET (PMOS), since the carrier is the hole, the source voltage has a voltage higher than the drain voltage so that holes can flow from the source to the drain. In the P-type MOSFET, a current direction is from the source to the drain because holes flow from the source to the drain. It should be noted that the source and drain of the MOSFET are not fixed. For example, the source and drain of the MOSFET may vary depending on the applied voltage. Therefore, in the description of the

present disclosure, one of the source and the drain is referred to as a first electrode, and the other one of the source and the drain is referred to as a second electrode.

[0032] Hereinafter, various embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. The component names used in the following description are selected in consideration of facilitating the specification, and may be different from the parts names of actual products. In the following embodiments, an electroluminescent display device will be described mainly with respect to an organic light emitting display device including organic light emitting material. However, the present disclosure is not limited to the organic light emitting display device, but may be applied to an inorganic light emitting display device including inorganic light emitting material.

[0033] FIG. 1 is a block diagram illustrating an electroluminescent display device according to an embodiment of the present disclosure, FIG. 2 is a diagram illustrating a pixel array of an electroluminescent display device according to an embodiment of the present disclosure, and FIG. 3 is a diagram schematically showing an equivalent circuit of the pixel shown in FIG. 2.

[0034] Referring to FIGS. 1 to 3, the electroluminescent display device according to the present disclosure comprises a display panel 10 equipped with pixels PXL, driving circuits 12 and 13 for driving the signal lines connected to the pixels PXL, and a timing controller 11 for controlling the driving circuits 12 and 13.

[0035] The driving circuits 12 and 13 write input image data DATA to the pixels PXL of the display panel 10. The driving circuits 12 and 13 comprise a source driver 12 for driving the data lines 14 connected to the pixels PXL and a gate driver 13 for driving the gate lines 15 connected to the pixels PXL.

[0036] A plurality of data lines 14 and a plurality of gate lines 15 cross each other on the display panel 10, and the pixels PXL are arranged in a matrix form. The pixels PXL may comprise an organic light emitting diode OLED. The OLED that emits light by itself includes an anode electrode, a cathode electrode, and organic compound layers formed therebetween. The organic compound layers include a hole injection layer HIL, a hole transport layer HTL, an emission layer EML, an electron transport layer ETL, and an electron injection layer EIL. When a driving voltage is applied to the anode electrode and the cathode electrode, holes passing through the HTL and electrons passing through the ETL are transferred to the EML to form excitons. As a result, the light emitting layer EML generates visible light.

[0037] The display panel 10 may include a display area AA equipped with a pixel array and a non-display area outside of the display area AA. The pixel array is provided with a plurality of horizontal pixel lines L1 to L4 as shown in FIG. 2, and a plurality of pixels PXL adjacent horizontally and connected to the gate lines 15 are disposed on each of the horizontal pixel lines L1 to L4. Here, each of the horizontal pixel lines L1 to L4 is not a physical signal line, but means a pixel group of one line, which is implemented by horizontally neighboring pixels PXL. The pixel array may include a first power line (hereinafter referred to as an initializing power line) 16 for supplying an initializing voltage Vinit to the pixels PXL and a second power line (hereinafter referred to as a high potential power line) 17 for supplying a high potential power voltage EVDD to the pixels PXL. The pixels PXL may be connected to a low potential power voltage EVSS. Each of the gate lines 15 may include a first gate line 15a for supplying a scan signal SC and a second gate line 15b for supplying an emission signal EM.

[0038] Each of the pixels PXL may be one of a red pixel, a green pixel, a blue pixel and a white pixel. The red pixel, the green pixel, the blue pixel, and the white pixel may constitute one unit pixel for color implementation. The color implemented in the unit pixel may be determined according to the emission ratio of the red pixel, the green pixel, the blue pixel, and the white pixel. Each of the pixels PXL may be connected to one data line 14, at least one first gate line 15a, one second gate line 15b, the initializing power line 16, the high potential power line 17, etc. Each pixel PXL may be further connected to a first gate line 15a disposed in a previous horizontal pixel line. Each pixel disposed in a nth horizontal pixel line L(n) is supplied with a nth scan signal SC(n) and a nth emission line EM(n) assigned to the nth horizontal pixel line L(n) and a (n-1)th scan signal SC(n-1) assigned to a (n-1)th horizontal pixel line L(n-1). However, gate lines connected to each pixel PXL and gate signals may vary depending on the circuit configuration of the pixel PXL.

[0039] Each pixel PXL may comprise a driving TFT DT for generating a driving current, an OLED for emitting light according to the driving current and a switching circuit SWC for programing a voltage between a gate and a source of the driving TFT DT, as shown in FIG. 3. Each pixel PXL may further comprise an emission controlling TFT ET for turning on/off a current flow between the driving TFT DT and the OLED for PWM (Pulse Width Modulation) driving. The PWM driving is to control the emission duty of the OLED in one frame to remove flicker and afterimage in a low gradation representation. An off period of the emission controlling TFT ET for PWM driving may be determined according to a predetermined PWM duty ratio.

[0040] Each of the pixels PXL may change the on-biased state of the driving TFT DT at least once within the off period of the emission controlling TFT ET so that the level of the hysteresis phenomenon can be reduced. For this purpose, each of the pixels PXL may change the gate-source voltage of the driving TFT DT equal to or more than twice in one frame based on a multi-scan driving method.

[0041] The source driver 12 converts input image data DATA received from the timing controller 11 every frame into data voltages Vdata, and then supplies the data voltages to the data lines 14. The source driver 12 uses a digital-to-analog converter ADC converting the input image data DATA into gamma compensation voltages to output the data

voltages Vdata.

[0042] A multiplexer may be disposed between the source driver 12 and the data lines 14 of the display panel 10. The multiplexer distributes the data voltages output through one output channel to the plurality of the data lines, thereby reducing the number of the output channels of the source driver 12 to the number of the data lines. The multiplexer may be omitted depending on the resolution or purpose of display devices.

[0043] The source driver 12 may further comprise a power generating unit. The power generating unit may generate an initializing voltage Vinit to supply to the initializing power line 16 and generate a high potential power voltage EVDD to supply to the high potential power line 17. The power generating unit may further generate a low potential power voltage EVSS. The power generating unit may be mounted outside the source driver 12 and then be connected to the source driver 12 via a conductive film, etc. The initializing voltage Vinit may be designed to be within considerably lower voltage ranges than the operation voltage of the OLED, in order to preventing the OLED from unnecessarily emitting light during an initializing period and a sampling period.

[0044] The gate driver 13 may comprise a first gate driver for generating the scan signals SC(1)~SC(4) of FIG. 2 and a second gate driver for generating the emission signals EM(1)~EM(4).

[0045] The first gate driver includes stages as many as the horizontal pixel lines L1~L4 and outputs the scan signals SC(1)~SC(4) under the control of the timing controller 11. The first gate driver may be implemented by a shift register and sequentially supply the scan signals SC(1)~SC(4) to first gate lines 15a(1)~15a(4) through a plurality of first output nodes. The first gate driver may sequentially supply the scan signals SC(1)~SC(4) to the first gate lines 15a(1)~15a(4) a plurality of times in one frame the according to a multi-scan driving method.

[0046] The second gate driver includes stages as many as the horizontal pixel lines L1~L4 and outputs the emission signals EM(1)~EM(4) under the control of the timing controller 11. The second gate driver may be implemented by a shift register and sequentially supply the emission signals EM(1)~EM(4) to second gate lines 15b(1)~15b(4) through a plurality of second output nodes.

[0047] To simplify the configuration of the gate driver 13, each of the first output nodes may be commonly connected to two adjacent horizontal pixel liens. In order to drive the pixels PXL in FIG. 7, two scan signals having different on-timings are necessary. For example, if an (n-1)th scan signal SC(n-1) and a nth scan signal SC(n) are used as two scan signals applied to the pixels of a nth horizontal pixel line Ln, one gate driver may be omitted so an advantage occurs of simplifying the configuration of the gate driver 13. In this case, since the (n-1)th scan signal SC(n-1) and the nth scan signal SC(n) are sequentially output from one gate driver, the pulse widths of the two scan signals are same but the phases are different from each other

[0048] The gate drive 13 may be directly formed on a non-display area of the display panel 10 with the pixel array through the process of a gate-driver in panel GIP, but is not limited thereto. The gate driver 13 may be manufactured in an IC type and then bonded to the display panel 10 through a conductive film.

[0049] The timing controller 11 receives digital data DATA of input image and timing signals synchronized with the digital data from a host system. The timing signals includes a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a dot clock signal DCLK, and a data enable signal DE. The host system may be one of a television system, a set-top box, a navigation system, a DVD player, a Blu-ray player, a personal computer, a home theater system and a phone system.

[0050] The timing controller 11 may multiply an input frame frequency by i (i is a positive integer larger than 0) times and control the operation timings of the driving circuits 12 and 13 at a frame frequency of the input frame frequency x i Hz. The input frame frequency is 60Hz in the NTSC (National Television Standards Committee) scheme and 50Hz in PAL (Phase-Alternating Line) scheme.

[0051] The timing controller 11 generates the data control signal DDC for controlling the operation timings of the source driver 12 and the gate control signal GDC for controlling the operation timings of the gate driver 13, based on the timing signals received from the host system.

[0052] The data control signal DDC includes a source start pulse, a source sampling clock, a source output enable signal, and the like. The source start pulse controls the sampling start timing of the source driver 12. The source sampling clock is a clock signal that shifts data sampling timings. If the signal transmitting interface between the timing controller 11 and the source driver 12 is a mini-LVDS (Low Voltage Differential Signaling) interface, the source start pulse and the source sampling clock may be omitted.

[0053] The gate control signal GDC includes a gate start pulse, a gate shift clock, a gate output enable signal, and the like. In case of the GIP circuit, the gate output enable signal may be omitted. The gate start pulse is generated at the beginning of a frame period every frame period, and input to a shift register of each gate driver 13. The gate start pulse controls the start timing, at which the scan signals and the emission signals are output, every frame period. The gate shift clock is input to a shift register of the gate driver 13 to control the shift timings of the gate signals.

[0054] Fig. 4 is a waveform diagram showing an example of the multi-scan driving method for improving hysteresis phenomenon and Fig. 5 is a waveform diagram showing another example of the multi-scan driving method for improving hysteresis phenomenon.

[0055] The on-biased state of the driving TFT DT may be implemented by the gate-source voltage of the driving TFT DT satisfying a conducting condition. Each pixel PXL may be further supplied with the data voltage assigned to another pixel within an off-state duration of the emission controlling TFT ET, in order for the on-biased state to be changed at least one time in one frame. For this, each pixel PXL may be applied with two or more data voltages in the multi-scan method such as FIGS. 4 and 5.

[0056] Referring to FIG. 4, for the multi-scan driving, each of the scan signals SC(1)~SC(n) may be input as an on level ON twice within one frame. In this case, each of the scan signals SC(1)~SC(n) includes a first pulse of a scan signal corresponding to a first on level ON and a second pulse of the scan signal corresponding to a second on level ON. At this time, each of the emission signals is input as an on level ON between the first pulse of the scan signal and the second pulse of the scan signal, and input as an off level OFF while overlapping the first pulse of the scan signal and the second pulse of the scan signal. The off level periods OFF of the emission signals EM(1)~EM(n) correspond to the off period of the emission controlling TFT ET.

[0057] Referring to FIG. 4, the example, in which a pixel A is driven according to a first scan signal SC(1) and a first emission signal EM(1) and a pixel B is driven according to a second scan signal SC(2) and a second emission signal EM(2), is described as follows. The pixel A and the pixel B are connected to a same data line 14.

[0058] Referring to FIG. 4, in the pixel A, a first gate-source voltage of the driving TFT DT is set based on a first data voltage V1 in a first period and a second gate-source voltage of the driving TFT DT may be set based on a second data voltage Vk different from the first data voltage V1 in a second period, following the first period, during which the emission controlling TFT ET is turned off. Here, the first gate-source voltage is for generating a driving current emitting the OLED in the pixel A, and the second gate-source voltage is for changing the on-biased state of the driving TFT DT in the pixel A to lower the hysteresis phenomenon. The emission controlling TFT ET is turned on in the first period, and the OLED emits light by the driving current during the emission controlling TFT ET is turned on. The first and second periods are included in one frame period.

[0059] Referring to FIG. 4, the source driver 12 generates the first data voltage V1 to supply to the data lines 14 connected to the pixels A and B in the first period, and generates the second data voltage Vk to supply to the data lines 14 connected to the pixels A and B in the second period. And, the gate driver 13 generates a first pulse of a first scan signal (P1 of SC(1)) synchronized with the first data voltage V1 to supply to the first gate line connected to the pixel A in the first period, and generates a second pulse of the first scan signal (P2 of SC(1)) synchronized with the second data voltage Vk to supply to the first gate line in the second period. Also, the gate driver 13 generates a first pulse of a second scan signal (P1' of SC(k)) synchronized with the second data voltage Vk to supply to a second gate line connected to the pixel B in the second period.

[0060] So, the second data voltage Vk is input to the pixel A and the pixel B simultaneously in the second period. In the case of the pixel A, the second gate-source voltage of the driving TFT DT is set according to the second data voltage Vk. On the other hand, in the case of the pixel B, the first gate-source voltage of the driving TFT DT is set according to the second data voltage Vk.

[0061] With respect to all pixels, the period becomes short during which a first on-biased state in accordance with the first gate-source voltage is changed into a second on-biased state in accordance with the second gate-source voltage within one frame. Accordingly, since the time that the gate-source voltage of the driving TFT DT remains the same becomes short, the hysteresis phenomenon can be alleviated.

[0062] Meanwhile, referring to FIG. 5, each of the scan signals SC(1)~SC(n) may be input while having the on level ON three times within one frame, for the multi-scan driving. In this case, each of the scan signals SC(1)~SC(n) includes a first pulse of a scan signal corresponding to a first on level ON, a second pulse of the scan signal corresponding to a second on level ON and a third pulse of the scan signal corresponding to a third on level ON. At this time, each of the emission signals EM(1)~EM(n) is input as an on level ON between the first pulse of the scan signal and the second pulse of the scan signal, and input as an off level OFF while overlapping the first pulse of the scan signal, the second pulse of the scan signal and the third pulse of the scan signal. The off period of the emission controlling TFT ET becomes the off level OFF period of the emission signals EM(1)~EM(n).

[0063] Referring to FIG. 5, the example, in which a pixel A is driven according to a first scan signal SC(1) and a first emission signal EM(1), a pixel B is driven according to a second scan signal SC(i) and a second emission signal EM(i) and a pixel C is driven according to a third scan signal SC(j) and a third emission signal EM(j), is described as follows. The pixels A, B and C are connected to a same data line 14.

[0064] Referring to FIG. 5, in the pixel A, a first gate-source voltage of the driving TFT DT is set based on a first data voltage V1 in a first period, a second gate-source voltage of the driving TFT DT may be set two times based on second data voltages Vi and Vj different from the first data voltage V1 in a second period during which the emission controlling TFT ET is turned off. Here, the first gate-source voltage is for generating a driving current emitting the OLED in the pixel A, and the second gate-source voltage is for changing the on-biased state of the driving TFT DT in the pixel A to lower the hysteresis phenomenon. And, the second gate-source voltage is different from the first gate-source voltage. Setting the second gate-source voltage multiple times also has the advantage that the response speed is improved. Since the

emission controlling TFT ET is turned on in the first period, the OLED emits light by the driving current during the emission controlling TFT ET is turned on. The first and second periods are included in one frame period.

[0065] Referring to FIG. 5, the source driver 12 generates the first data voltage V1 to supply to the data lines 14 connected to the pixels A, B and C in the first period, and generates the second data voltages Vi and Vj to supply to the data lines 14 connected to the pixels A, B and C in the second period. And, in the first period, the gate driver 13 generates a first pulse of a first scan signal (P1 of SC(1)) synchronized with the first data voltage V1 to supply to the first gate line connected to the pixel A. In the second period, the gate driver 13 also generates a second pulse of the first scan signal (P2 of SC(1)) synchronized with the second data voltage Vi to supply to the first gate line and then generates a third pulse of the first scan signal (P3 of SC(1)) synchronized with the second data voltage Vj to supply to the first gate line in the second period. Also, in the second period, the gate driver 13 generates a first pulse of a second scan signal (P1' of SC(i)) synchronized with the second data voltage Vi to supply to a second gate line connected to the pixel B and then generates a first pulse of a third scan signal (PI" of SC(j)) synchronized with the second data voltage Vj to supply to a third gate line connected to the pixel C.

[0066] So, the second data voltage Vi is input to the pixel A and the pixel B simultaneously in the second period. In the case of the pixel A, the second gate-source voltage of the driving TFT DT is set according to the second data voltage Vi. On the other hand, in the case of the pixel B, the first gate-source voltage of the driving TFT DT is set according to the second data voltage Vi.

[0067] Also, the second data voltage Vj is input to the pixels A, B and C simultaneously in the second period. In the case of the pixels A and B, the second gate-source voltage of the driving TFT DT is set according to the second data voltage Vj. On the other hand, in the case of the pixel C, the first gate-source voltage of the driving TFT DT is set according to the second data voltage Vj.

[0068] With respect to all pixels, the period, during which a first on-biased state in accordance with the first gate-source voltage is changed into a second on-biased state in accordance with the second gate-source voltage within one frame, becomes shorter than FIG. 4. Accordingly, since the time that the gate-source voltage of the driving TFT DT remains the same becomes short, the hysteresis phenomenon can be alleviated.

[0069] FIG. 6 shows that an afterimage is improved according to the multi-scan driving method.

[0070] The degree of the hysteresis phenomenon is proportional to the time during which the gate-source voltage of the driving TFT is maintained. If the image such as FIG. 6A is displayed for a long time, the afterimage such as FIG. 6B appears. When the threshold voltage of the driving TFT is compensated in each pixel, the hysteresis phenomenon causes a mis-compensation and induces a DC afterimage to reduce display quality. If the time that the gate-source voltage of the driving TFT is maintained is reduced within one frame through the multi-scan driving such as FIGS. 4 and 5 of the present disclosure, the DC afterimage can be remarkably reduced and the display quality can be improved as shown in FIG. 6C. According to the present description, by also applying the data voltage applied to a second pixel to the driving TFT of a first pixel during the emission controlling TFT is turned off within one frame, the hysteresis phenomenon of the driving TFT of the first pixel can be effectively improved without an additional increase in driving time.

[0071] FIG. 7 specifically shows the equivalent circuit of the pixel shown in FIG. 2.

[0072] Referring to FIG. 7, the pixel PXL according to one embodiment of the present disclosure comprises an OLED, a plurality of TFTs (T1~T5, ET, DT) and a storage capacitor Cst. The TFTs (T1~T5, ET, DT) may be implemented by LTPS TFTs of a PMOS type having good response characteristics. But, the technical idea of the present description is not limited thereto. For example, some TFTs connected to the gate electrode of the driving TFT DT among switching TFTs (T1~T5) may be implemented by oxide TFTs of a NMOS type having good off-current characteristics, and the remaining TFTs may be implemented as LTPS TFTs of a PMOS type having good response characteristics.

[0073] Hereinafter, the connection structure of one pixel PXL arranged on an nth horizontal pixel line will be described in detail.

[0074] The OLED is a device which emits light according to the driving current input from the driving TFT DT. The anode electrode of the OLED is connected to fourth node N4, and the cathode electrode of the OLED is connected to the input terminal of the low potential voltage EVSS. An organic compound layer is provided between the anode electrode and the cathode electrodes.

[0075] The driving TFT DT is a device which generates the driving current flowing through the OLED according to a first gate-source voltage within a first period. During a second period during which the emission controlling TFT ET is turned off, the driving TFT DT compensates for the hysteresis phenomenon according to a second gate-source voltage different from the first gate-source voltage. The driving TFT DT includes a gate electrode connected to a second node N2, a first electrode connected to a first node N1, and a second electrode connected to a third node N3.

[0076] The emission controlling TFT ET is a device which is connected between the third node N3 and a fourth node N4 and switched according to an nth emission signal EM(n). The emission controlling TFT ET controls the driving current so that the OLED can be repeatedly turned on and off with a constant emission duty ratio. The gate electrode of the emission controlling TFT ET is connected to an nth second gate line 15b(n) to which an nth emission signal EM(n) is applied, a first electrode of the emission controlling TFT ET is connected to the third node N3 and a second electrode

of the emission controlling TFT ET is connected to the fourth node N4.

[0077] The first switching TFT T1 is connected between the data line 14 and the first node N1 and switched according to an nth scan signal SC(n). The gate electrode of the first switching TFT T1 is connected to the nth first gate line 15a(n) to which the nth scan signal SC(n) is applied, a first electrode of the first switching TFT T1 is connected to the data line 14 and a second electrode of the first switching TFT T1 is connected to the first node N1.

[0078] The second switching TFT T2 is connected between the high potential power line 17 and the first node N1 and switched according to the nth emission signal EM(n). The gate electrode of the second switching TFT T2 is connected to the nth second gate line 15b(n) to which the nth emission signal EM(n) is applied, a first electrode of the second switching TFT T2 is connected to the high potential power line 17, and a second electrode of the second switching TFT T2 is connected to the first node N1.

[0079] The third switching TFT T3 is connected between the second node N2 and the third node N3 and switched according to the nth scan signal SC(n). The gate electrode of the third switching TFT T3 is connected to the nth first gate line 15a(n) to which the nth scan signal SC(n) is applied, a first electrode of the third switching TFT T3 is connected to the third node N3, and a second electrode of the third switching TFT T3 is connected to the second node N2.

[0080] The fourth switching TFT T4 is connected between the second node N2 and the initializing power line 16, and switched according to an (n-1)th scan signal SC(n-1). The gate electrode of the fourth switching TFT T4 is connected to an (n-1)th first gate line 15a(n-1) to which the (n-1)th scan signal SC(n-1) is applied, a first electrode of the fourth switching TFT T4 is connected to the second node N2, and a second electrode of the fourth switching TFT T4 is connected to the initializing power line 16.

[0081] The fifth switching TFT T5 is connected between the fourth node N4 and the initializing power line 16, and switched according to the nth scan signal SC(n). The gate electrode of the fifth switching TFT T5 is connected to the nth first gate line 15a(n) to which the nth scan signal SC(n) is applied, a first electrode of the fifth switching TFT T5 is connected to the fourth node N4, and a second electrode of the fifth switching TFT T5 is connected to the initializing power line 16.

[0082] The storage capacitor Cst is connected between the high potential power line 17 and the second node N2.

[0083] Meanwhile, the third and fourth switching TFTs T3 and T4 may be designed as a dual gate configuration in order to suppress a leakage current occurring when turned off. In the dual gate configuration, two gate electrodes are connected to each other in order to have a same potential. Because the channel length of the dual gate configuration becomes longer than that of a single gate configuration, an off resistance is increased and an off current is reduced, which ensure the stability of operation.

[0084] FIG. 8 is a waveform diagram showing driving signals input to the pixel of FIG. 7 and potential changes of specific pixel nodes according to the driving signals. And, FIGS. 9A to 9E show the operation states of the pixel during the first initializing period, a first sampling period, an emission period, a second initializing period and a second sampling period of FIG. 8.

[0085] Referring to FIG. 8, a first frame period for driving each pixel PXL disposed on an nth horizontal pixel line Ln may comprise a first initializing period IP1, a first sampling period SP1 following the first initializing period, an emission period EP following the first sampling period, a second initializing period IP2 following the emission period, and a second sampling period SP2 following the second initializing period. Here, the first initializing period IP1, the first sampling period SP1 and the emission period EP may be included in the first period described in the embodiments of FIGS. 4 and 5 and claims, and the second initializing period IP2 and the second sampling period SP2 may be included in the second period described in the embodiments of FIGS. 4 and 5 and claims.

[0086] Referring to FIG. 8, in the first initializing period IP1, the (n-1)th scan signal SC(n-1) is input as an on level ON, and the nth scan signal SC(n) and the nth emission signal EM(n) are input as an off level OFF. The first initializing period IP1 is for resetting the second node N2 by the initializing voltage Vinit before the first sampling period SP1.

[0087] Referring to FIG. 9A, during the first initializing period IP1, the fourth switching TFT T4 is turned on responding to the (n-1)th scan signal SC(n-1) of an on level ON. The initializing voltage Vinit is applied to the node N2 by the turn-on operation of the fourth switching TFT T4, so that the gate potential of the drive TFT DT is reset to the initializing voltage Vinit.

[0088] Referring to FIG. 9A, during the first initializing period IP1, the first, third and fifth switching TFTs T1, T3 and T3 are turned off responding to the nth scan signal SC(n) of an off level OFF, and the second switching TFT T2 and the emission controlling TFT ET are turned off responding to the nth emission signal EM(n) of an off level OFF.

[0089] Referring to FIG. 8, during the first sampling period SP1, the nth scan signal SC(n) is input as the on level ON and the (n-1)th scan signal SC(n-1) and the nth emission signal EM(n) are input as the off level OFF. The first sampling period SP1 is for sampling the threshold voltage of the driving TFT DT.

[0090] Referring to FIG. 9B, during the first sampling period SP1, the first, third and fifth switching TFTs T1, T3 and T5 are turned on responding to the nth scan signal SC(n). The potential of the first node N1 is changed into a data voltage Vx due to the turning on of the first switching TFT T1. The gate electrode and the second electrode of the driving TFT DT are short-circuited by the turning on of the third switching TFT T3, so the driving TFT DT is diode-connected. If

a current flows through the driving TFT DT with being diode-connected, the threshold voltage of the driving TFT DT is sampled and stored at the second node N2 and the third node N3. That is, the potential of the second node N2 and the third node N3 becomes (Vx-Vth). The gate-source voltage Vgs of the driving TFT DT is the voltage between the first node N1 and the second node N2. So, during the first sampling period SP1, the first gate-source voltage of the driving TFT DT becomes the threshold voltage of the driving TFT DT.

[0091] Referring to FIG. 9B, during the first sampling period SP1, the potential of the fourth node N4 is reset to the initializing voltage Vinit by the turning on of the fifth switching TFT T5 so unnecessary emission of the OLED can be prevented.

[0092] Referring to FIG. 9B, during the first sampling period SP1, the fourth switching TFT T4 is turned off responding to the (n-1)th scan signal SC(n-1) of the off level OFF, and the second switching TFT T2 and the emission controlling TFT ET maintain their turn-off states responding to the nth emission signal EM(n) of the off level OFF.

[0093] Referring to FIG. 8, during the emission period EP, the (n-1)th scan signal SC(n-1) and the nth scan signal SC(n) are input as the off level OFF, and the nth emission signal EM(n) is input as the on level ON. The emission period EP is for setting the first gate-source voltage of the driving TFT DT corresponding to a driving current based on a data voltage Vx. And the emission period EP is for emitting the OLED according to the driving current flowing through the driving TFT DT.

[0094] Referring to FIG. 9C, during the emission period EP, the second switching TFT T2 and the emission controlling TFT ET are turned on responding to the nth emission signal EM(n) of the on level ON. During the emission period EP, the potential of the first node N1 is changed from the data voltage Vx to the high potential power voltage EVDD by the turning on of the second switching TFT T2. During the emission period EP, the potential of the second node N2 maintains (Vdata-Vth) which is stored in the first sampling period SP1 by the storage capacitor Cst. So, during emission period EP, the first gate-source voltage Vgs1 of the driving TFT DT becomes (EVDD-Vx+Vth), and a driving current corresponding thereto flows the driving TFT DT. This driving current is applied to the OLED via the emission controlling TFT ET.

[0095] The driving current Ioled flowing to the OLED during the emission period EP is expressed as a function independent of the threshold voltage of the driving TFT DT as shown in the following Equation 1.

[Equation 1]

$$\begin{aligned} \text{Ioled} &= K(Vgs - |Vth|)^2 \\ &= K(EVDD - \{Vx - |Vth|\} - |Vth|)^2 \\ &= K(EVDD - Vx)^2 \end{aligned}$$

[0096] Here, K is a constant value determined by the mobility, the channel ratio, parasitic capacity, etc. of the driving TFT DT.

[0097] Referring to FIG. 9C, during the emission period EP, the fourth switching TFT T4 maintains its turn-off state in response to the (n-1)th scan signal SC(n-1) of the off level OFF. And, during the emission period EP, the first, third and fifth switching TFTs T1, T3 and T5 are turned off in response to the nth scan signal SC(n) of the off level OFF.

[0098] Referring to FIG. 8, in the second initializing period IP2, the (n-1)th scan signal SC(n-1) is input as the on level ON, and the nth scan signal SC(n) and the nth emission signal EM(n) are input as the off level OFF. The second initializing period IP2 is for resetting the second node N2 to the initializing voltage Vinit prior to the second sampling period SP2.

[0099] Referring to FIG. 9D, during the second initializing period IP2, the fourth switching TFT T4 is turned on in response to the (n-1)th scan signal SC(n-1) of the on level ON. The initializing voltage Vinit is applied to the second node N2 by turning on the fourth switching TFT T4 and the gate potential of the driving TFT DT is reset again to the initializing voltage Vinit.

[0100] Referring to FIG. 9D, during the second initializing period IP2, the first, third and fifth switching TFTs T1, T3 and T5 are turned off in response to the nth scan signal SC(n) of the off level OFF, and the second switching TFT T2 and the emission controlling TFT ET are turned off in response to the nth emission signal EM(n) of the off level OFF.

[0101] Referring to FIG. 8, in the second sampling period SP2, the nth scan signal SC(n) is input as the on level ON, and the (n-1)th scan signal SC(n-1) and the nth emission signal EM(n) are input as the off level OFF. The second sampling period SP2 is for setting the second gate-source voltage Vgs2 of the driving TFT DT based on a data voltage Vx and another data voltage Vy (which is the data voltage applied to another pixel), in order to compensate for the hysteresis phenomenon of the driving TFT DT.

[0102] Referring to FIG. 9E, during the second sampling period SP2, the first, third and fifth switching TFTs T1, T3 and T5 are turned on in response to the nth scan signal SC(n) of the on level ON. The potential of the first node N1 is

changed intro a data voltage Vy owing to the turning on of the first switching TFT T1. And the gate electrode and the second electrode of the driving TFT DT are short-circuited by the turning on of the third switching TFT T3, so the driving TFT DT is diode-connected. If a current flows through the driving TFT DT with being diode-connected, the threshold voltage of the driving TFT DT is sampled and stored at the second node N2 and the third node N3. That is, the potential of the second node N2 and the third node N3 becomes (Vy-Vth). The gate-source voltage Vgs of the driving TFT DT is the voltage between the first node N1 and the second node N2. So, during the second sampling period SP2, the first gate-source voltage of the driving TFT DT gradually converges to the threshold voltage of the driving TFT DT. This voltage is different from the first gate-source voltage Vgs1 (EVDD-Vx+Vth) of the emission period EP described above and contributes to lowering the level of the hysteresis phenomenon of the driving TFT DT.

[0103] Referring to FIG. 9E, during the second sampling SP2, the fourth switching TFT T4 is turned off in response to the (n-1)th scan signal SC(n-1) of the off level OFF, and the second switching TFT T2 and the emission controlling TFT ET maintain their turn-off states in response to the nth emission signal EM(n) of the off level OFF.

[0104] As described above, according to the electroluminescent display device of the present disclosure, during the turning off period of an emission controlling element within one frame, the on-biased state of a driving element is changed by applying, to a pixel, the data voltage input to another pixel in the multi-scan driving method. Since the time that the gate-source voltage of the driving element is maintained within one frame is reduced, the electroluminescent display device of the present disclosure may improve the level of the hysteresis phenomenon of the driving element and the DC afterimage included from the hysteresis phenomenon, thereby raising a display quality.

[0105] Throughout the description, it should be understood by those skilled in the art that various changes and modifications are possible without departing from the technical principles of the present disclosure. Therefore, the technical scope of the present disclosure is not limited to the detailed descriptions in this specification but should be defined by the scope of the appended claims.

Claims

1. An electroluminescent display device, comprising:

a plurality of pixels (PXL),
wherein each pixel (PXL) of the plurality of pixels (PXL) comprises:

a driving element (DT) for generating a driving current;
a light emitting element (OLED) for emitting light according to the driving current;
an emission controlling element (ET) for controlling a flow of the driving current between the driving element (DT) and the light emitting element (OLED); and
a switching circuit (SWC) for setting a first gate-source voltage of the driving element (DT) corresponding to the driving current based on a first data voltage (V1) during a first period and setting a second gate-source voltage of the driving element (DT) based on a second data voltage (Vk) different from the first data voltage (V1) during a second period following the first period,
wherein the second gate-source voltage is different from the first gate-source voltage, and
wherein during the second period the emission controlling element (ET) is turned off.

2. The electroluminescent display device of claim 1, wherein the second gate-source voltage is for changing the on-biased state of the driving element (DT) to compensate a hysteresis phenomenon of the driving element (DT), and wherein the switching circuit (SWC) is adapted to set the second gate-source voltage a plurality of times based on a plurality of data voltages including the second data voltage (Vk) during the second period.

3. The electroluminescent display device of claim 2, wherein the driving element (DT) becomes a first on-biased state by the first gate-source voltage and becomes a second on-biased state by the second gate-source voltage, and the first on-biased state and the second on-biased state are different from each other.

4. The electroluminescent display device of claim 2 or 3, wherein the second data voltage (Vk) is applied to another pixel (PXL) during the second period, and a first gate-source voltage of a driving element (DT) included in the another pixel (PXL) is set according to the second data voltage (Vk).

5. The electroluminescent display device of claim 4, wherein during the emission controlling element (ET) is turned on within the first period, the light emitting element (OLED) emits light by the driving current applied through the emission controlling element (ET), and the first and second periods are included in one frame.

6. The electroluminescent display device of any one of claims 1 to 5, further comprising:

a source driver (12) for generating the first data voltage (V1) to supply to a data line (14) connected to the plurality of pixels (PXL) within the first period, and generating the second data voltage (Vk) to supply the data line (14) within the second period; and
a gate driver (13) for generating a first pulse (P1) of a first scan signal (SC(1)) synchronized with the first data voltage (V1) to supply to a first gate line connected to the plurality of pixels (PXL) within the first period, generating a second pulse (P2) of the first scan signal (SC(1)) synchronized with the second data voltage (Vk) to supply to the first gate line within the second period, and generating a first pulse (P1') of a second scan signal (SC(i)) synchronized with the second data voltage (Vk) to supply to a second gate line connected to the plurality of pixels (PXL) within the second period.

7. The electroluminescent display device of any one of claims 1 to 6, wherein a gate electrode, a first electrode and a second electrode of the driving element (DT) are respectively connected to a second node (N2), a first node (N1) and a third node (N3),
wherein the emission controlling element (ET) is connected between the third node (N3) and a fourth node (N4),
wherein the light emitting element (OLED) is connected between the fourth node (N4) and an input terminal of a low potential power voltage (EVSS), and
wherein the switching circuit (SWC) is connected to the data line (14) through which the first and second data voltages (VI, Vk) are supplied, a first power line (16) through which an initializing voltage (Vinit) is supplied, and a second power line (17) through which a high potential power voltage (EVDD) is supplied.

8. The electroluminescent display device of claim 7, wherein the switching circuit (SWC) comprises:

a first switching element (T1) connected between the first node (N1) and the data line;
a second switching element (T2) connected between the first node (N1) and the second power line (17);
a third switching element (T3) connected to the second node (N2) and the third node (N3);
a fourth switching element (T4) connected to the second node (N2) and the first power line (16);
a fifth switching element (T5) connected to the fourth node (N4) and the first power line (16); and
a storage capacitor (Cst) connected between the second power line (17) and the second node (N2).

9. The electroluminescent display device of claim 8, wherein the fourth switching element (T4) is switched according to an (n-1)th scan signal (SC(n-1)),
wherein the first, third and fifth switching elements (T1, T3 and T5) are switched according to an nth scan signal (SC(n)), the nth scan signal (SC(n)) being later than the (n-1)th scan signal (SC(n-1)) in their phases of an on period,
wherein the emission controlling element (ET) and the second switching element (T2) are switched according to an nth emission signal (EM(n)),
wherein the (n-1)th scan signal (SC(n-1)) and the nth scan signal (SC(n)) are respectively input as an on level in the first period and the second period sequentially, and
wherein the nth emission signal (EM(n)) is input as an off level in the first and second periods and is input as the on level in a third period between the first period and the second period.

10. A method of driving an electroluminescent display device equipped with a plurality of pixels (PXL), each of the plurality of pixels (PXL) comprising a driving element (DT) for generating a driving current, a light emitting element (OLED) for emitting light according to the driving current and an emission controlling element (ET) for controlling a flow of the driving current between the driving element (DT) and the light emitting element (OLED), the method comprising:

setting a first gate-source voltage of the driving element (DT) corresponding to the driving current based on a first data voltage (V1) during a first period; and
setting a second gate-source voltage of the driving element (DT) based on a second data voltage (Vk) different from the first data voltage (V1) during a second period following the first period,
wherein the second gate-source voltage is different from the first gate-source voltage, and
wherein during the second period the emission controlling element (ET) is turned off.

11. The method of claim 10, wherein the second gate-source voltage is for changing the on-biased state of the driving element (DT) to compensate a hysteresis phenomenon of the driving element (DT), and
wherein the setting a second gate-source voltage of the driving element (DT) includes setting the second gate-

source voltage a plurality of times based on a plurality of data voltages including the second data voltage (Vk) during the second period.

12. The method of claim 11, wherein the driving element (DT) becomes a first on-biased state by the first gate-source voltage and becomes a second on-biased state by the second gate-source voltage, and the first on-biased state and the second on-biased state are different from each other.

13. The method of claim 12, wherein the second data voltage (Vk) is applied to another pixel (PXL) during the second period, and a first gate-source voltage of a driving element (DT) included in the another pixel (PXL) is set according to the second data voltage (Vk).

14. The method of claim 13, wherein during the emission controlling element (ET) is turned on within the first period, the light emitting element (OLED) emits light by the driving current applied through the emission controlling element (ET), and the first and second periods are included in one frame.

15. The method of claim 10, further comprising:

generating the first data voltage (V1) to supply to a data line (14) connected to the plurality of pixels (PXL) within the first period, and generating the second data voltage (Vk) to supply the data line (14) within the second period;
generating a first pulse (P1) of a first scan signal (SC(1)) synchronized with the first data voltage (V1) to supply to a first gate line connected to the plurality of pixels (PXL) within the first period; and
generating a second pulse (P2) of the first scan signal (SC(1)) synchronized with the second data voltage (Vk) to supply to the first gate line within the second period, and generating a first pulse (P1') of a second scan signal (SC(i)) synchronized with the second data voltage (Vk) to supply to a second gate line connected to the plurality of pixels (PXL) within the second period.

FIG. 1

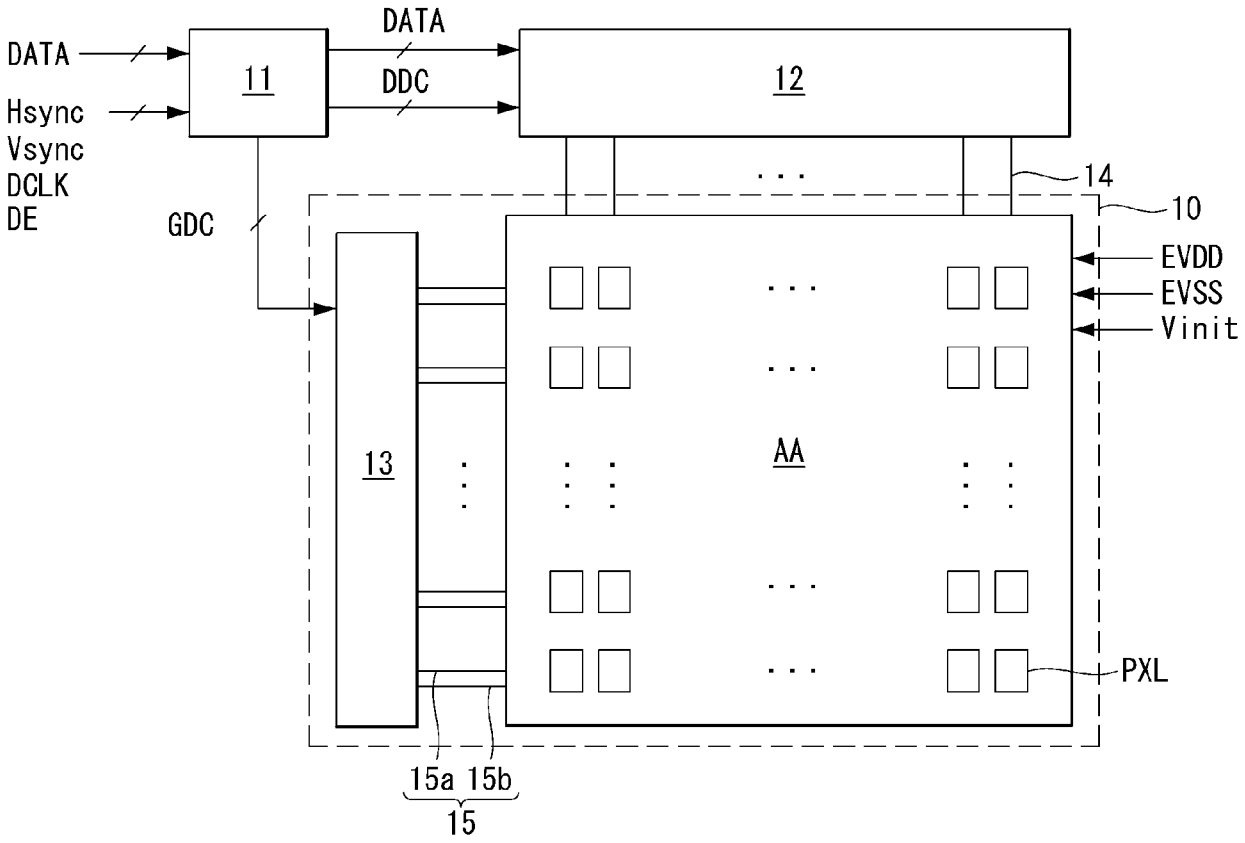

DATA
Hsync
Vsync
DCLK
DE
11
DATA
DDC
12
14
10
GDC
13
AA
EVDD
EVSS
Vinit
PXL
15a 15b
15

FIG. 2

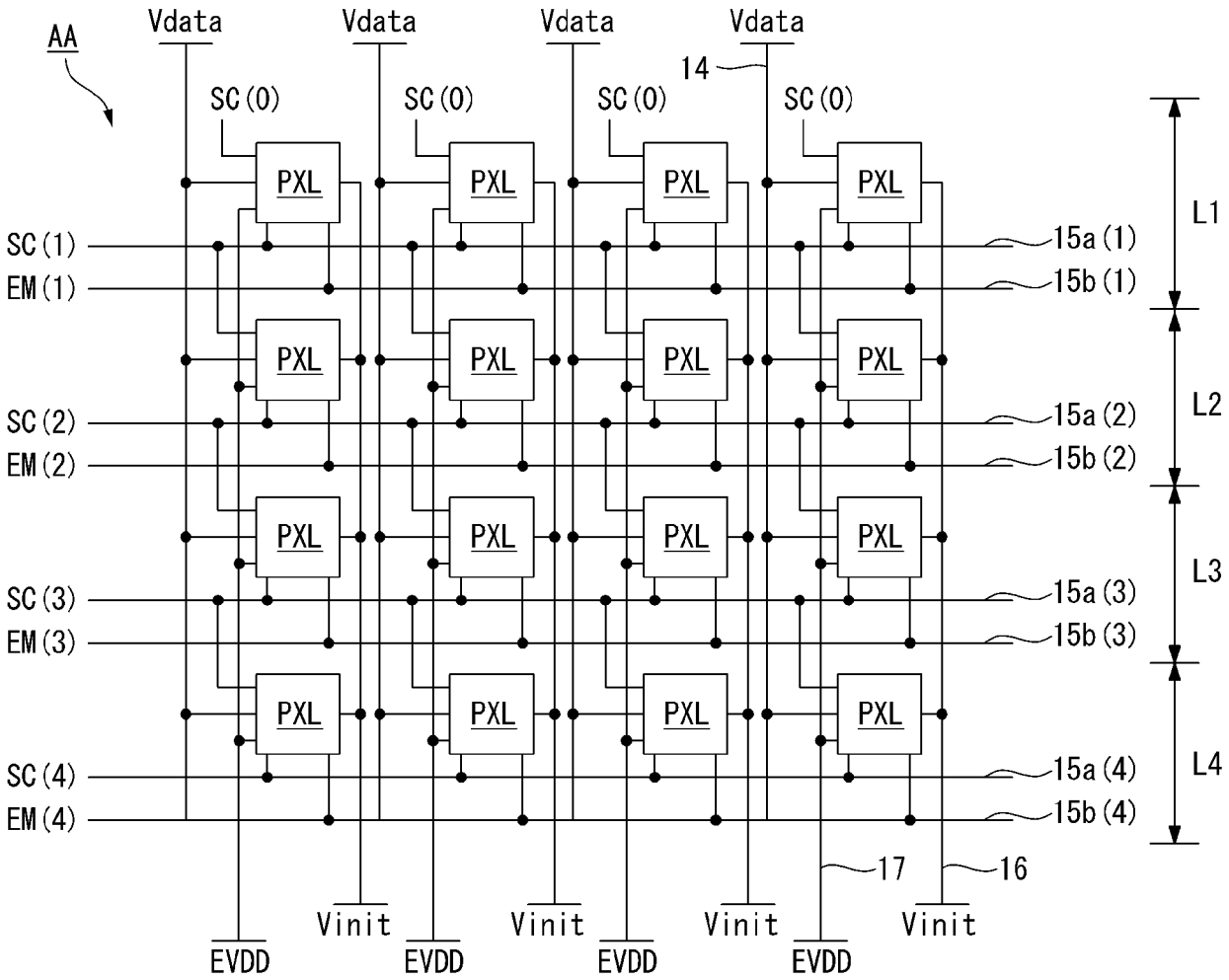

AA
Vdata
Vdata
Vdata
Vdata
14
SC (0)
SC (0)
SC (0)
SC (0)
PXL
SC (1)
EM (1)
SC (2)
EM (2)
SC (3)
EM (3)
SC (4)
EM (4)
15a (1)
15b (1)
15a (2)
15b (2)
15a (3)
15b (3)
15a (4)
15b (4)
L1
L2
L3
L4
17
16
Vinit
EVDD

FIG. 3

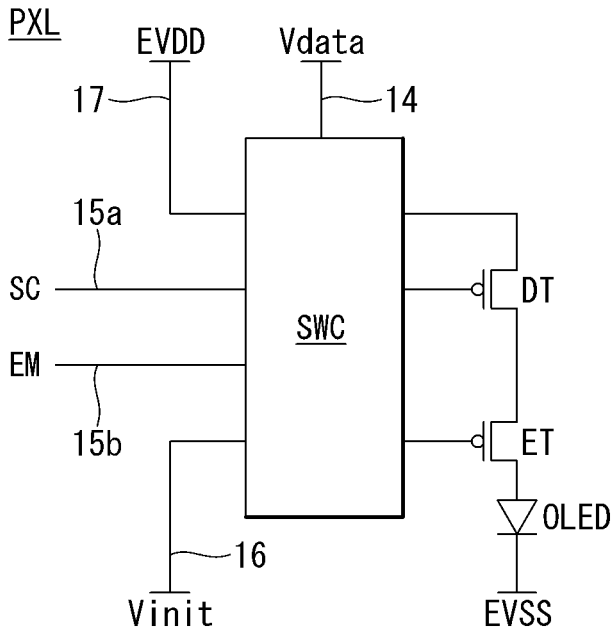


FIG. 4

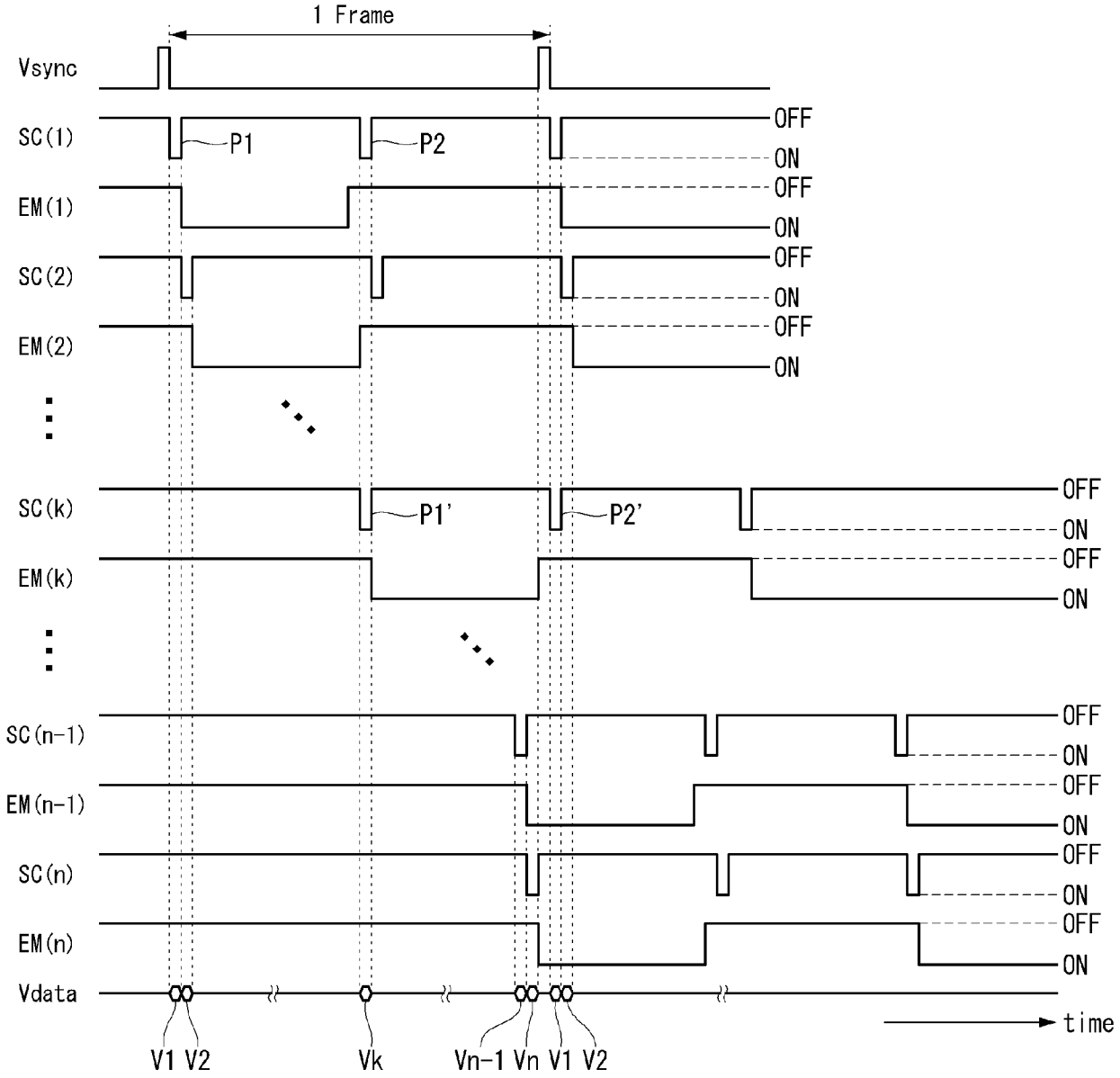

1 Frame
Vsync
SC(1)
P1
P2
EM(1)
SC(2)
EM(2)
SC(k)
P1'
P2'
EM(k)
SC(n-1)
EM(n-1)
SC(n)
EM(n)
Vdata
OFF
ON
V1 V2
Vk
Vn-1 Vn V1 V2
time

FIG. 5

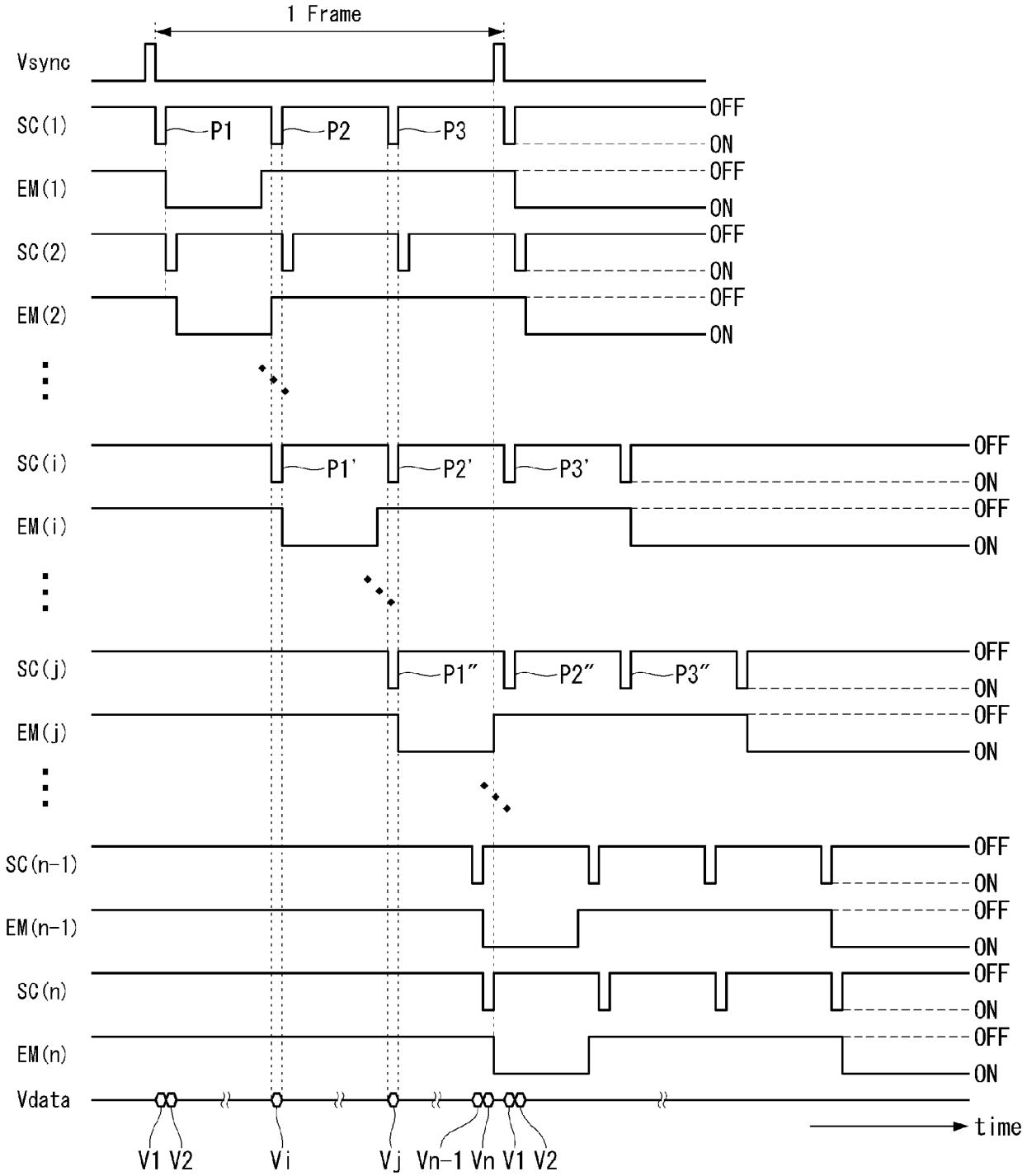

1 Frame
Vsync
SC(1)
P1
P2
P3
OFF
ON
EM(1)
SC(2)
EM(2)
SC(i)
P1'
P2'
P3'
EM(i)
SC(j)
P1"
P2"
P3"
EM(j)
SC(n-1)
EM(n-1)
SC(n)
EM(n)
Vdata
V1 V2
Vi
Vj
Vn-1 Vn V1 V2
time

FIG. 6

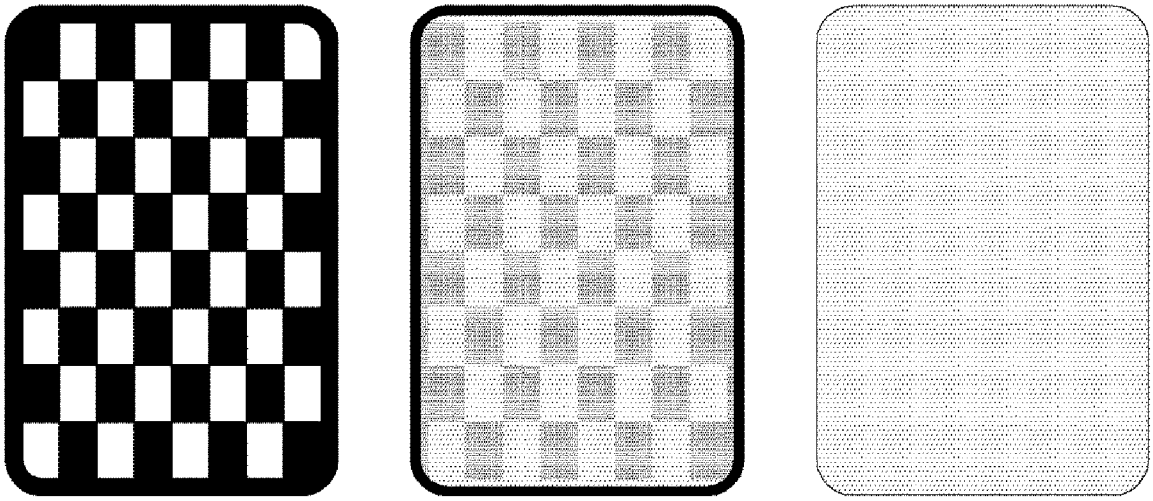


FIG. 7

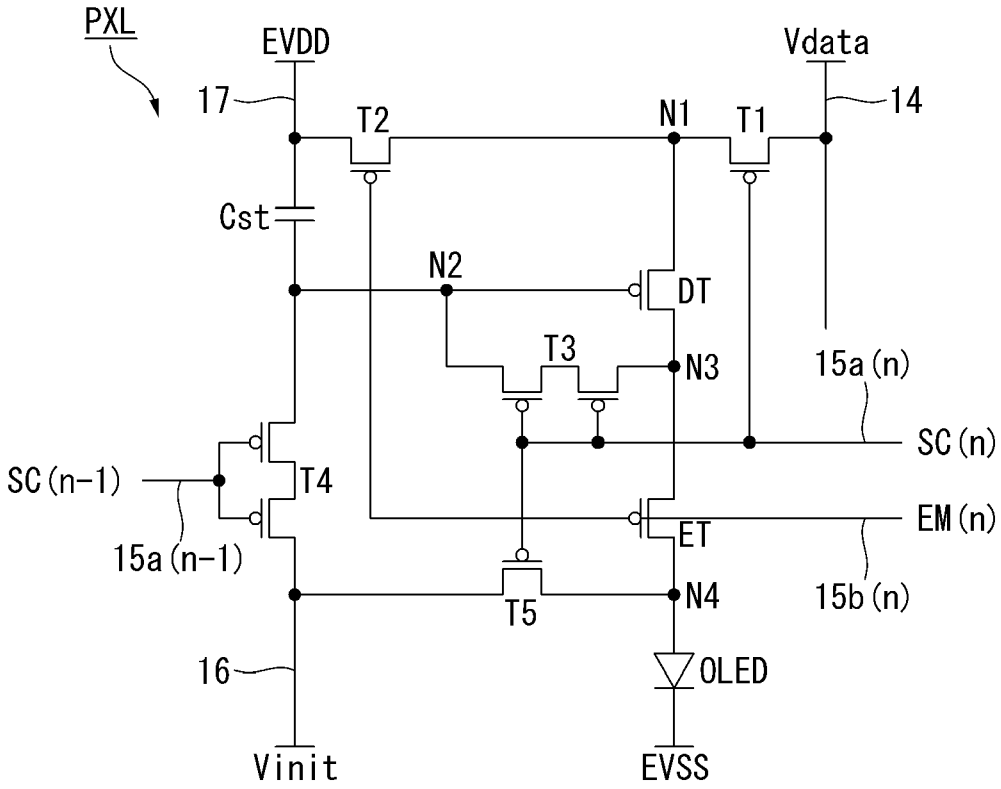

PXL
EVDD
Vdata
17
T2
N1
T1
14
Cst
N2
DT
T3
N3
15a(n)
SC(n)
SC(n-1)
T4
EM(n)
ET
15a(n-1)
T5
N4
15b(n)
16
OLED
Vinit
EVSS

FIG. 8

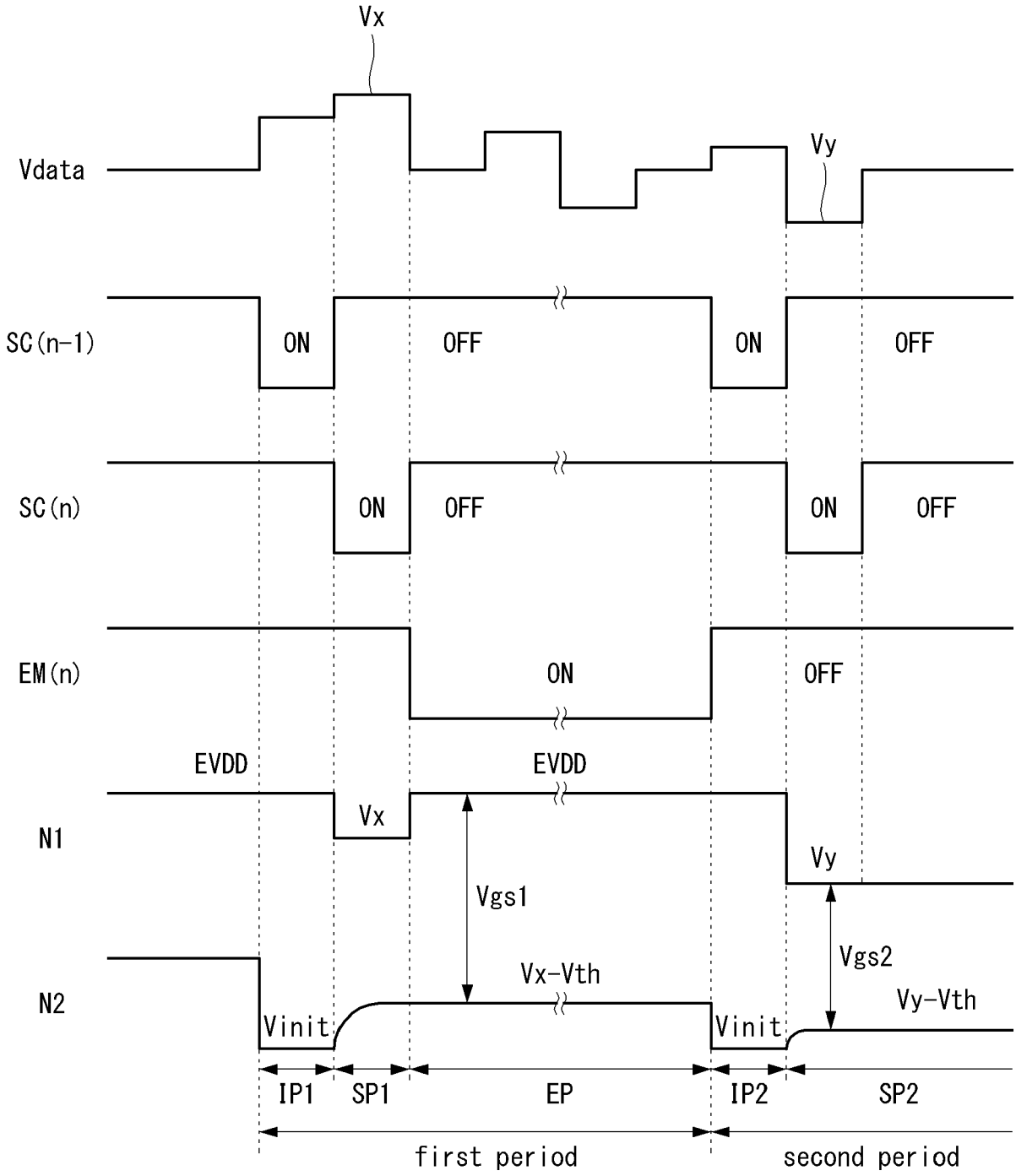

Vx
Vdata
Vy
SC(n-1)
ON
OFF
ON
OFF
SC(n)
ON
OFF
ON
OFF
EM(n)
ON
OFF
EVDD
EVDD
N1
Vx
Vy
Vgs1
Vgs2
N2
Vx-Vth
Vy-Vth
Vinit
Vinit
IP1
SP1
EP
IP2
SP2
first period
second period

FIG. 9A

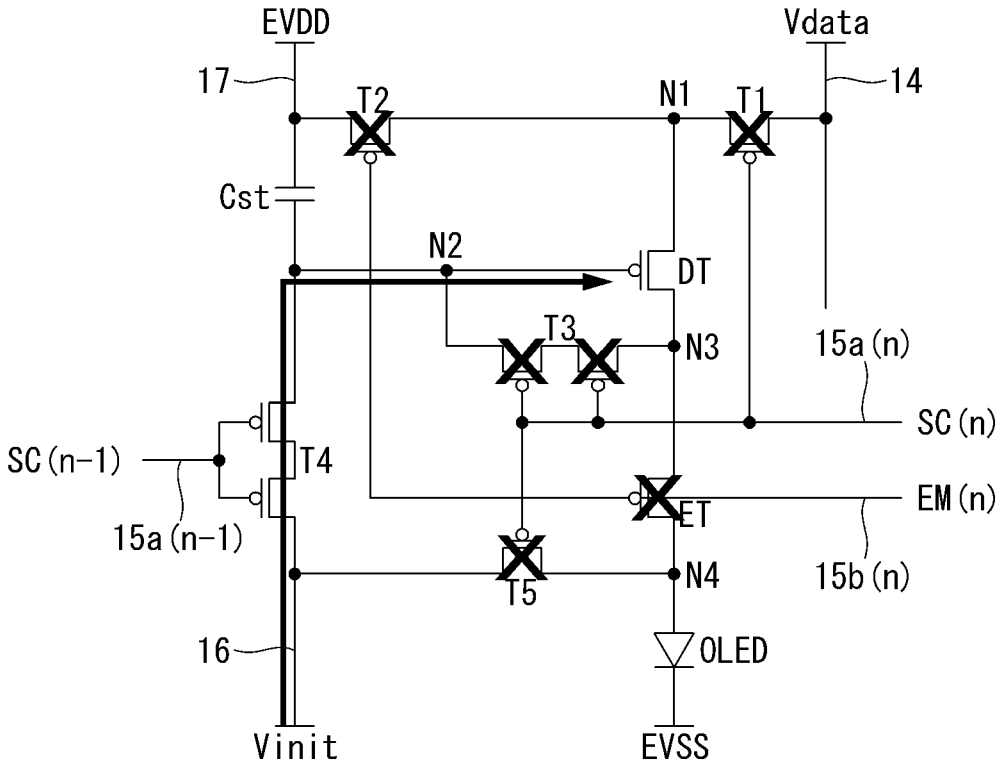

EVDD
Vdata
17
14
T2
N1
T1
Cst
N2
DT
T3
N3
15a(n)
SC(n)
SC(n-1)
T4
EM(n)
ET
15a(n-1)
T5
N4
15b(n)
16
OLED
Vinit
EVSS

FIG. 9B

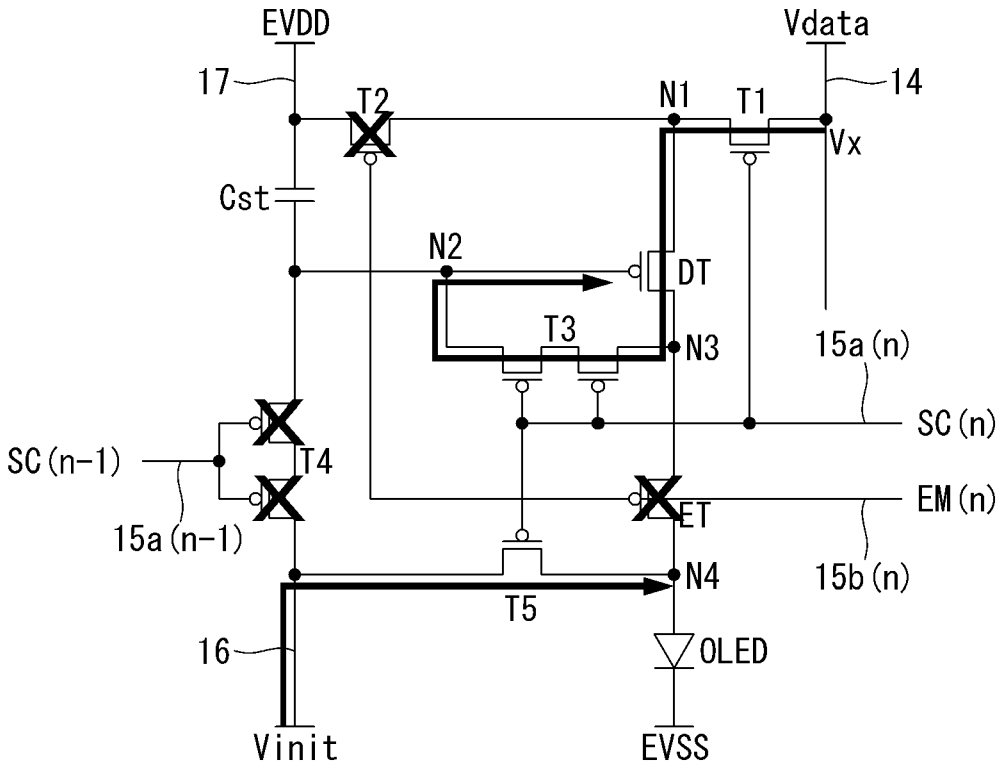

EVDD
Vdata
17
T2
N1
T1
14
Vx
Cst
N2
DT
T3
N3
15a(n)
SC(n)
SC(n-1)
T4
EM(n)
ET
15a(n-1)
N4
15b(n)
T5
16
OLED
Vinit
EVSS

FIG. 9C

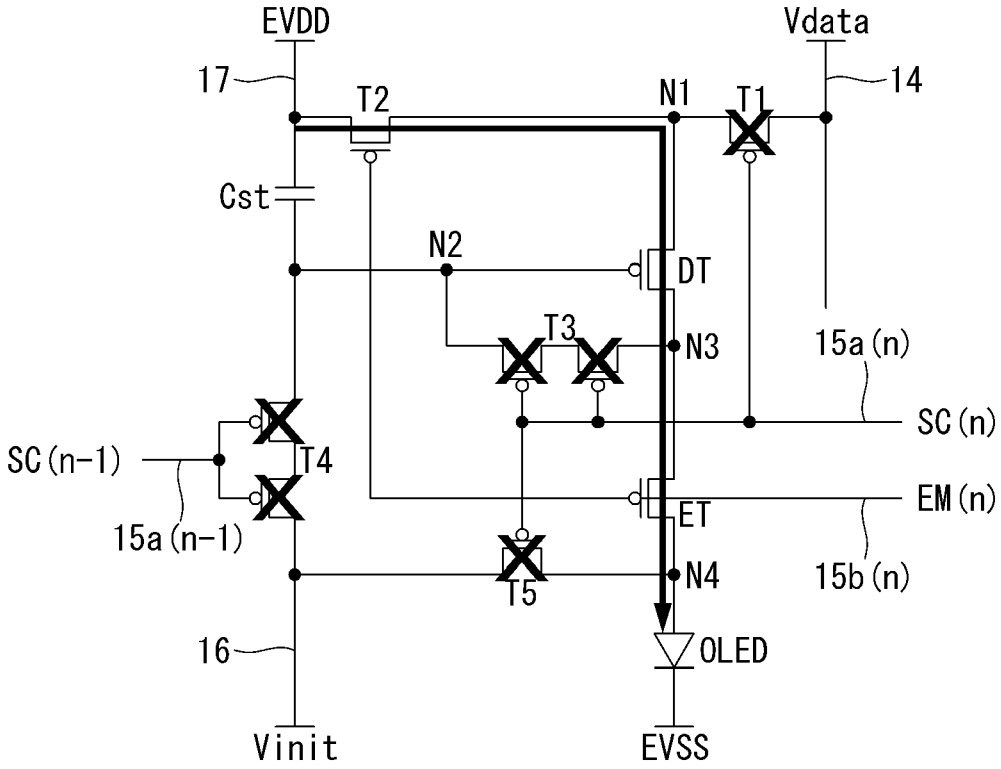

EVDD
Vdata
17
T2
N1
T1
14
Cst
N2
DT
T3
N3
15a(n)
SC(n)
SC(n-1)
T4
EM(n)
ET
15a(n-1)
T5
N4
15b(n)
16
OLED
Vinit
EVSS

FIG. 9D

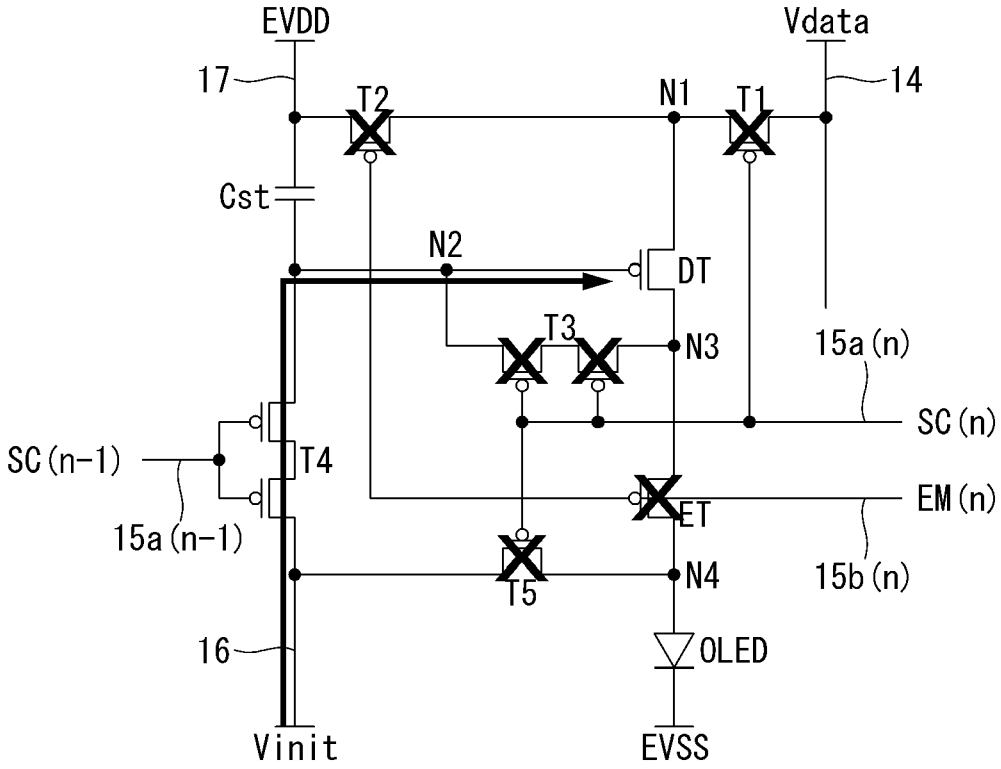
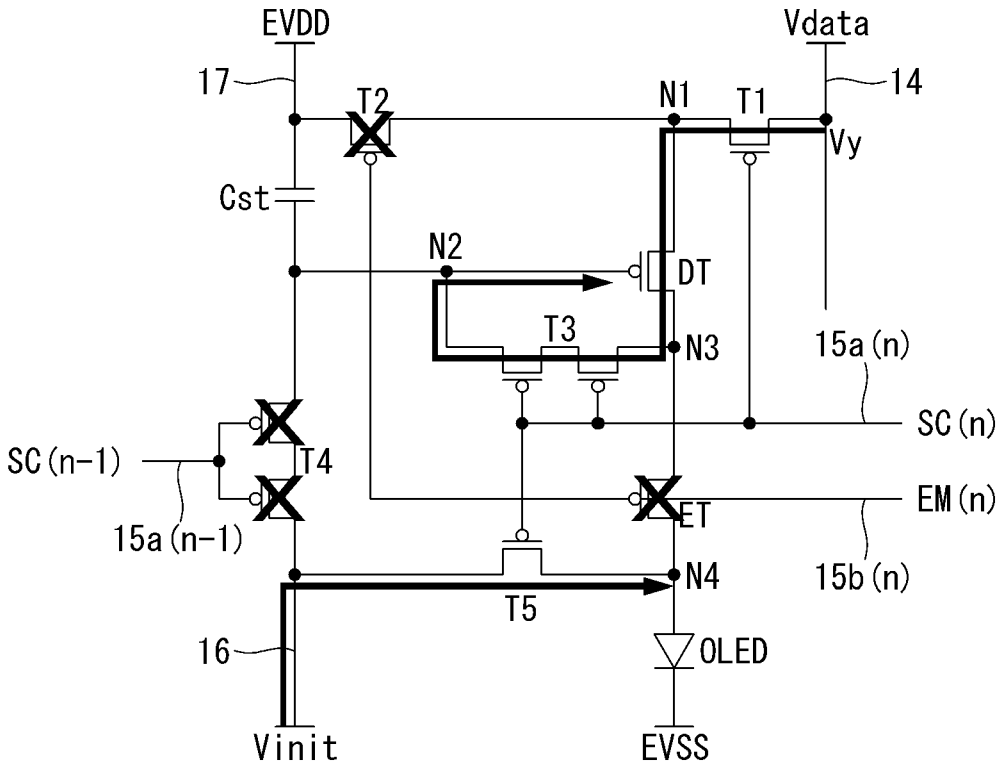

EVDD
Vdata
17
14
T2
N1
T1
Cst
N2
DT
T3
N3
15a(n)
SC(n)
SC(n-1)
T4
EM(n)
ET
15a(n-1)
T5
N4
15b(n)
16
OLED
Vinit
EVSS

FIG. 9E


EVDD
Vdata
17
T2
N1
T1
14
Vy
Cst
N2
DT
T3
N3
15a(n)
SC(n)
SC(n-1)
T4
EM(n)
ET
15a(n-1)
N4
15b(n)
T5
16
OLED
Vinit
EVSS

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 18 20 2278

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2015/187270 A1 (LEE SEUNG-KYU [KR] ET AL) 2 July 2015 (2015-07-02) * paragraphs [0025], [0042] - [0056], [0061] - [0063], [0108] - [0118], [0132] - [0140], [0143] - [0147]; figures 1-4I * -----	1-15	INV. G09G3/3233

TECHNICAL FIELDS SEARCHED (IPC)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	30 November 2018	Demin, Stefan

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 18 20 2278

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

30-11-2018

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015187270 A1	02-07-2015	KR 20150076868 A	07-07-2015
		US 2015187270 A1	02-07-2015

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	电致发光显示装置及其驱动方法		
公开(公告)号	EP3483872A1	公开(公告)日	2019-05-15
申请号	EP2018202278	申请日	2018-10-24
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	RHA SUNGHOON JEON CHANGHOON BAE HYUNGGUK		
发明人	RHA, SUNGHOON JEON, CHANGHOON BAE, HYUNGGUK		
IPC分类号	G09G3/3233		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0861 G09G2310/0262 G09G2320/043 G09G3/325 G09G3/3266 G09G3/3291 G09G2320/0204 G09G2320/0257 G09G2320/064		
优先权	1020170149552 2017-11-10 KR		
外部链接	Espacenet		

摘要(译)

根据本公开的电致发光显示装置包括多个像素（PXL）。多个像素（PXL）中的每一个包括用于产生驱动电流的驱动元件（DT），用于根据驱动电流发光的发光元件（OLED），用于控制流动的发光控制元件（ET）。驱动元件（DT）和发光元件（OLED）之间的驱动电流，以及用于基于第一驱动元件设置与驱动电流对应的驱动元件（DT）的第一栅-源电压的开关电路（SWC）在第一周期期间的数据电压（VI）和在第一周期之后的第二周期期间基于与第一数据电压（V1）不同的第二数据电压（Vk）设置驱动元件（DT）的第二栅极-源极电压其中，第二栅极-源极电压不同于第一栅极-源极电压，并且其中在第二时段期间，发射控制元件（ET）截止。

FIG. 3