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(54) **ERROR COMPENSATOR AND ORGANIC LIGHT EMITTING DISPLAY DEVICE USING THE SAME**

FEHLERKOMPENSATOR UND ORGANISCHE LICHTEMITTIERENDE ANZEIGEEINHEIT DAMIT

COMPENSATEUR D'ERREUR ET DISPOSITIF D'AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE UTILISANT CELUI-CI

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Description

[0001] The following description relates to an error compensator and an organic light emitting display device using the same.

[0002] Various types of flat panel display devices have been developed which reduce weight and volume as compared with cathode ray tubes. These flat panel display devices include a liquid crystal display, a field emission display, a plasma display panel, an organic light emitting display device, and the like.

[0003] Among these flat panel display devices, the organic light emitting display device displays images using organic light emitting diodes that emit light through recombination of electrons and holes. The organic light emitting display device has a fast response speed and is driven with low power consumption.

[0004] US 2002/190193 and US2001/008422 disclose devices providing error compensation.

[0005] According to the invention, there is provided an error compensator according to claim 1, and a sensing unit that includes the error compensator according to claim 4.

[0006] Aspects of embodiments of the present invention are directed toward an error compensator that can improve image quality and an organic light emitting display device using the same. Aspects of embodiments are directed toward an error compensator and an organic light emitting display device using the same, which can exactly extract information on the degradation of an organic light emitting diode and the threshold voltage of a driving transistor.

[0007] Embodiments also provide an error compensator and an organic light emitting display device using the same, which can exactly extract information on the degradation of an organic light emitting diode and the threshold voltage of a driving transistor, in which data is changed using extracted information, so that it is possible to display an image with improved image quality, regardless of the degradation of an organic light emitting diode and the threshold voltage of a driving transistor.

[0008] According to an embodiment of the present invention, an organic light emitting display device is provided to include: pixels each having a driving transistor and an organic light emitting diode; and a sensing unit extracting at least one of a first information including the threshold voltage of the driving transistor or a second information including the degradation of the organic light emitting diode from a pixel of the pixels, wherein the sensing unit includes: an amplifier amplifying a voltage corresponding to the at least one of the first information or the second information; and an error compensator compensating for error components of elements included in the amplifier and the error compensator.

[0009] The error components may include offset characteristics, noises and line resistances of the elements. The amplifier may include a first transistor having a second electrode coupled to the pixel, having a first electrode coupled to a ground power source, and having a gate electrode coupled to the second electrode so that current flows from the pixel to the ground power source; a second transistor coupled in the form of a current mirror to the first transistor; and a current supply unit supplying a reference current to the first transistor. The second transistor may be formed to have a channel width wider than that of the first transistor. The reference current may be set to have a current value lower than that of a second current to be flowed in the second transistor, the second current mirroring a first current supplied to the first transistor. A common terminal of the current supply unit and the second transistor may be coupled to the error compensator.

[0010] The amplifier may further include a first switch SW20 positioned between the gate electrode and the second electrode of the first transistor; a second switch SW21 coupled between the ground power source and the gate electrodes of the eleventh and second transistors; and a third switch SW22 coupled between the pixel and the common terminal of the current supply unit and the second transistor. The first switch SW20 may be turned on during a period in which the first information is extracted, and the second and third switches SW21, SW22 may be turned on during a period in which the second information is extracted.

[0011] The error compensator may be an error compensator as described below.

[0012] According to an embodiment of the present invention, an error compensator includes a first operational amplifier (OP-AMP) and a second OP-AMP; a first switch and a first capacitor, coupled in parallel between a first input terminal and an output terminal of the first OP-AMP; a second switch coupled between a first input terminal and an output terminal of the second OP-AMP; a third switch coupled between the first input terminal and the amplifier; a fourth switch coupled between an external analog-digital converter and the output terminal of the second OP-AMP; a first storage unit coupled between the output terminal of the first OP-AMP and the first input terminal of the second OP-AMP; and a second storage unit coupled between the first input terminal and the output terminal of the second OP-AMP.

[0013] A first reference power source may be supplied to a second input terminal of the first OP-AMP, and a second reference power source may be supplied to a second input terminal of the second OP-AMP. The first storage unit may include a fifth switch, a third capacitor and a sixth switch, coupled in series between the output terminal of the first OP-AMP and the first input terminal of the second OP-AMP; and a seventh switch, a fourth capacitor and an eighth switch, coupled in parallel to the fifth switch, the third capacitor and the sixth switch between the output terminal of the first OP-AMP and the first input terminal of the second OP-AMP. The fifth and sixth switches may be turned on during a first period in the period in which the first and second switches are turned on, and the seventh and eighth switches may be

turned on during a second period not overlapping with the first period in the period in which the first and second switches are turned on. The fourth switch may also be set to be in a turn-on state during the first and second periods.

[0014] The second storage unit may include a second capacitor coupled between tenth and eleventh nodes; a ninth switch coupled between the eleventh node and the first input terminal of the second OP-AMP; a tenth switch coupled between the tenth node and the output terminal of the second OP-AMP; an eleventh switch coupled between the tenth node and the first input terminal of the second OP-AMP; and a twelfth switch coupled between the eleventh node and the output terminal of the second OP-AMP. The fifth switch, the sixth switch, the ninth switch and the tenth switch may be turned on during a third period in the period in which the third switch is turned on, and the seventh switch, the eighth switch, the eleventh switch and the twelfth switch may be turned on during a fourth period not overlapping with the third period in the period in which the third switch is turned on. The fourth period may be set to be longer than the third period.

[0015] The fourth switch, the eleventh switch and the twelfth switch may be turned on during a period posterior to the fourth period.

[0016] The organic light emitting display device may further include a data driver supplying a data signal to data lines coupled to the pixels; a scan driver supplying a scan signal to scan lines coupled to the pixels; and a timing controller changing bits of data supplied from the outside thereof and provides the data driver with the changed bits, corresponding to the at least one of the first information or the second information. The sensing unit may further include an analog-digital converter converting a voltage supplied from the error compensator into a digital value; and a memory storing the digital value, and providing the stored value to the timing controller so that the bits of the data are changed. Each pixel may include a transistor coupled between the sensing unit and a common node between the driving transistor and the organic light emitting diode, and turned on during the period in which the at least one of the first information or the second information is extracted.

[0017] In the error compensator and the organic light emitting display device according to an embodiment of the present invention, error components of external compensation elements are removed using an error compensator, and accordingly, it is possible to exactly extract information corresponding to the threshold voltage of a driving transistor and the degradation of an organic light emitting diode included in each pixel.

[0018] The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention, and, together with the description, serve to explain the principles of the present invention.

FIG. 1 is a circuit diagram illustrating a pixel of a related art organic light emitting display device.

FIG. 2 is a block diagram illustrating an organic light emitting display device according to an embodiment of the present invention.

FIG. 3 is a circuit diagram illustrating a pixel according to an embodiment of the present invention.

FIG. 4 is a block diagram illustrating an embodiment of a sensing unit shown in FIG. 2.

FIG. 5 is a circuit diagram illustrating an embodiment of an amplifier shown in FIG. 4.

FIG. 6 is a circuit diagram illustrating an embodiment of a current supply unit shown in FIG. 5.

FIG. 7 is a circuit diagram illustrating an error compensator according to an embodiment of the present invention.

FIG. 8 is a waveform diagram illustrating an operation process of the error compensator shown in FIG. 7.

FIG. 9 is a circuit diagram illustrating another embodiment of the amplifier.

FIG. 10 is a waveform diagram illustrating an operation process of the amplifier shown in FIG. 9.

[0019] Referring to FIG. 1, the pixel 4 of the related art organic light emitting display device includes an organic light emitting diode OLED, and a pixel circuit 2 coupled to a data line Dm and a scan line Sn so as to control the organic light emitting diode OLED.

[0020] An anode electrode of the organic light emitting diode OLED is coupled to the pixel circuit 2, and a cathode electrode of the organic light emitting diode OLED is coupled to a second power source ELVSS. When a scan signal is supplied to the scan line Sn, the pixel circuit 2 controls the amount of current supplied to the organic light emitting diode OLED, corresponding to a data signal supplied to the data line Dm. To this end, the pixel circuit 2 includes a second transistor M2 coupled between a first power source ELVDD and the organic light emitting diode OLED, a transistor M1 coupled with the transistor M2, the data line Dm and the scan line Sn, and a storage capacitor Cst coupled between a gate electrode and a first electrode of the transistor M2.

[0021] A gate electrode of the transistor M1 is coupled to the scan line Sn, and a first electrode of the transistor M1 is coupled to the data line Dm. A second electrode of the transistor M1 is coupled to one terminal of the storage capacitor Cst. Here, the first electrode is referred to as any one of source and drain electrodes, and the second electrode is set as an electrode different from the first electrode. For example, if the first electrode is referred to as a source electrode, then the second electrode is referred as a drain electrode. When the scan signal is supplied to the scan line Sn, the transistor M1 coupled to the scan line Sn and the data line Dm is turned on to supply the data signal supplied from the data line Dm to the storage capacitor Cst. In this case, the storage capacitor Cst charges to a voltage corresponding to the data signal.

[0022] The gate electrode of the transistor M2 is cou-

pled to the one terminal of the storage capacitor Cst, and the first electrode of the transistor M2 is coupled to the other terminal of the storage capacitor Cst and the first power source ELVDD. A second electrode of the transistor M2 is coupled to the anode electrode of the organic light emitting diode OLED. The transistor M2 controls the amount of current flowing from the first power source ELVDD to the second power source ELVSS via the organic light emitting diode OLED, corresponding to the voltage stored in the storage capacitor Cst.

[0023] In this case, the organic light emitting diode OLED generates light corresponding to the amount of current supplied from the transistor M2.

[0024] However, the organic light emitting display device has a problem in that an image with uniform luminance is not displayed by degradation of the organic light emitting diode OLED and a variation in threshold voltage of the transistor M2. In order to solve such a problem, there has been proposed a method of compensating for the degradation of the organic light emitting diode OLED and the threshold voltage of the transistor M2 from the outside of the pixel 4. However, in the method of compensating for the degradation and the threshold voltage from the outside using micro-current flowing in the pixel 4, exact information is not extracted by offsets and noises of elements included in an external compensation circuit, and therefore, exact compensation is not made.

[0025] FIG. 2 is a block diagram illustrating an organic light emitting display device according to an embodiment of the present invention.

[0026] Referring to FIG. 2, the organic light emitting display device according to this embodiment includes a pixel unit 130 having pixels 140 positioned at intersection portions (crossing regions) of scan lines S1 to Sn and data lines D1 to Dm, a scan driver 110 driving the scan lines S1 to Sn, a data driver 120 driving the data lines D1 to Dm, a control line driver 160 driving control lines CL1 to CLn, and a timing controller 150 controlling the scan driver 110, the data driver 120 and the control line driver 160.

[0027] The organic light emitting display device according to this embodiment further includes a sensing unit 170 extracting threshold voltage information of a driving transistor and/or degradation information of an organic light emitting diode included in each pixel 140, using feedback lines F1 to Fm.

[0028] The pixel unit 130 includes the pixels 140 positioned at intersection portions (crossing regions) of the scan lines S1 to Sn and the data lines D1 to Dm. Each pixel 140 provides the sensing unit 170 with the threshold voltage information of the driving transistor and/or the degradation information of the organic light emitting diode during a sensing period. Each pixel 140 receives a data signal input during a driving period, and generates light with a set or predetermined luminance while controlling the amount of current supplied from a first power source ELVDD to a second power source ELVSS via the organic light emitting diode, corresponding to the received data signal.

[0029] The scan driver 110 supplies a scan signal to the scan lines S1 to Sn. For example, the scan driver 110 progressively supplies the scan signal to the scan lines S1 to Sn during the sensing and driving periods.

[0030] The data driver 120 receives a second data data2 supplied during the driving period, and generates a data signal using the supplied second data data2. The data signal generated in data driver 120 is supplied to the data lines D1 to Dm in synchronization with the scan signal. The data driver 120 may supply a specific data signal in synchronization with the scan signal during the sensing period. Here, the specific data signal is used to extract threshold voltage information of the driving transistor included in each pixel 140, and may be set to any one of various gray scale values.

[0031] The control line driver 160 supplies a control signal to the control lines CL1 to CLn during the sensing period. For example, the control line driver 160 may progressively supply a control signal to the control lines CL1 to CLn during the sensing period. If the data signal is progressively supplied to the control lines CL1 to CLn, pixels 140 for each horizontal line are coupled to the feedback lines F1 to Fm.

[0032] The sensing unit 170 extracts threshold voltage information of the driving transistor and/or degradation information of the organic light emitting diode from each pixel 140 during the sensing period. For example, the sensing unit 170 may extract threshold voltage information and/or degradation information of the pixels 140 for each horizontal line, corresponding to the control signal supplied to the control lines CL1 to CLn.

[0033] The timing controller 150 controls the scan driver 110, the data driver 120 and the control line driver 160. The timing controller 150 receives threshold voltage information and/or degradation information supplied from the sensing unit 170, and generates a second data data2 by changing a first data data1, corresponding to the supplied information.

[0034] FIG. 3 is a circuit diagram illustrating a pixel according to an embodiment of the present invention. For convenience of illustration, a pixel coupled to an m-th data line Dm and an n-th scan line Sn is shown in FIG. 3.

[0035] Although the pixel 140 having three transistors M1 to M3 and one capacitor Cst has been illustrated in FIG. 3, the present invention is not limited thereto. Practically, in the present invention, the pixel 140 may be selectively implemented as any one of various circuits currently known in the art, which can be electrically coupled to the sensing unit 170.

[0036] Referring to FIG. 3, the pixel 140 according to this embodiment includes an organic light emitting diode OLED, and a pixel circuit 142 controlling the amount of current supplied to the organic light emitting diode OLED.

[0037] An anode electrode of the organic light emitting diode OLED is coupled to the pixel circuit 142, and a cathode electrode of the organic light emitting diode OLED is coupled to the second ELVSS. The organic light

emitting diode OLED generates light with a set or predetermined luminance, corresponding to current supplied from the pixel circuit 142.

[0038] The pixel circuit 142 supplies a set or predetermined current to the organic light emitting diode OLED, corresponding to a data signal. To this end, the pixel circuit 142 includes first to third transistors M1 to M3 and a storage capacitor Cst.

[0039] A first electrode of the first transistor M1 (driving transistor) is coupled to the first power source ELVDD, and a second electrode of the first transistor M1 is coupled to the anode electrode of the organic light emitting diode OLED. The first transistor M1 controls the amount of current supplied to the organic light emitting diode OLED, corresponding to the voltage applied to a first node N1.

[0040] A first electrode of the second transistor M2 is coupled to the data line Dm, and a second electrode of the second transistor M2 is coupled to the first node N1. A gate electrode of the second transistor M2 is coupled to the scan line Sn. When a scan signal is supplied to the scan line Sn, the second transistor M2 is turned on to electrically couple the data line Dm and the first node N1 to each other.

[0041] A first electrode of the third transistor M3 is coupled to the anode electrode of the organic light emitting diode OLED, and a second electrode of the third transistor M3 is coupled to a feedback line Fm. A gate electrode of the third transistor M3 is coupled to a control line CLn. When a control signal is supplied to the control line CLn, the third transistor M3 is turned on to electrically couple the feedback line Fm and the anode electrode of the organic light emitting diode OLED to each other.

[0042] The storage capacitor Cst is coupled between the first power source ELVDD and the first node N1. The storage capacitor Cst stores a voltage corresponding to the data signal.

[0043] FIG. 4 is a block diagram illustrating an embodiment of the sensing unit shown in FIG. 2. For convenience of illustration, only one channel is shown in FIG. 4.

[0044] Referring to FIG. 4, the sensing unit 170 according to this embodiment includes an amplifier 180, an error compensator 190, an analog-digital converter (hereinafter, referred to as an "ADC") 200 and a memory 210. Here, the amplifier 180, the error compensator 190 and the like are formed for each channel, i.e., each of the feedback lines F1 to Fm. The ADC 200 may be formed for each channel or may be formed to share a plurality of channels. The memory 210 is commonly coupled to all the channels, so as to store threshold voltage information and/or degradation information extracted from each channel.

[0045] The amplifier 180 amplifies voltage (and/or current) extracted from each pixel 140. Practically, the amplifier 180 amplifies micro-voltage (and/or current) from each pixel 140 and supplies the amplified micro-voltage (and/or current) to the error compensator 190.

[0046] The error compensator 190 removes an error component (an offset characteristic, noise, resistive component, etc.) so that desired information can be extracted. Practically, the error compensator 190 supplies only desired information to the ADC 200 by removing an error component caused by internal circuits of the amplifier 180. In this case, all error components caused by circuits between the pixel 140 and the ADC 200, including an error component included in the information (voltage and/or current) amplified in the amplifier 180, can be removed, and accordingly, it is possible to improve the reliability of the extracted information. The error compensator also compensates for errors that would otherwise be introduced by its internal circuitry.

[0047] The ADC 200 converts, into a digital value, information supplied from the error compensator 190, e.g., analog voltage including threshold voltage information of the driving transistor and/or degradation information of the organic light emitting diode included in each pixel.

[0048] The digital value converted in the ADC 200 is stored in the memory 210. Practically, a digital value (threshold voltage information and/or degradation information) corresponding to each pixel is stored in the memory 210. The digital value stored in the memory 210 is supplied to the timing controller 150. The timing controller 150 generates the second data data2 by changing bits of the first data data1 so that the threshold voltage information of the driving transistor and/or the degradation information of the organic light emitting diode is included in each pixel, using the digital value stored in the memory 210.

[0049] FIG. 5 is a circuit diagram illustrating an embodiment of the amplifier shown in FIG. 4. Although transistors M11 and M12 are implemented as NMOS transistors in FIG. 5, the present invention is not limited thereto.

[0050] Referring to FIG. 5, the amplifier 180 includes a current supply unit 182, a fourth transistor M11 and a fifth transistor M12.

[0051] A second electrode of the fourth transistor M11 is coupled to the pixel 140, and a first electrode of the fourth transistor M11 is coupled to a ground power source GND. A gate electrode of the fourth transistor M11 is coupled to its own second electrode. That is, the fourth transistor M11 is diode-coupled so that current can flow from the pixel 140 to the ground power source GND.

[0052] The fifth transistor M12 is coupled between the current supply unit 182 and the ground power source GND. A gate electrode of the fifth transistor M12 is coupled to the gate electrode of the fourth transistor M11. That is, the fifth transistor M12 is coupled in the form of a current mirror to the fourth transistor M11. A common node of the fifth transistor M12 and the current supply unit 182 is coupled to the error compensator 190.

[0053] In the present invention, the fifth transistor M12 is formed to have a channel width wider than that of the fourth transistor M11 so that the amount of current can be amplified. For example, the fifth transistor M12 may be set so that the channel width of the fifth transistor M12 is i (i is an integer exceeding 1) times wider than that of

the fourth transistor M11.

[0054] The current supply unit 182 supplies a set or predetermined reference current iref to the fifth transistor M12. Here, the reference current iref is set to have a previously fixed current value in the design process of the current supply unit 182. For example, the reference current iref is set to have a current value lower than that of current iM12 flowing through the fifth transistor M12.

[0055] An operation process of the amplifier will be described in more detail. A specific data signal is supplied to the data lines D1 to Dm, corresponding to the scan signal progressively supplied to the scan lines S1 to Sn during the sensing period. A control signal is progressively supplied to the control lines CL1 to CLn during the sensing period. The voltage of the second power source ELVSS is controlled during the sensing period so that current does not flow in the organic light emitting diode OLED. Practically, in an embodiment of the present invention, the configuration in which the current provided to the sensing unit 170 via the first transistor M1 during the sensing period is applicable to all various types of configurations currently known in the art.

[0056] The specific data signal is supplied to the pixel circuit 142. If the third transistor M3 is turned on, a first current, i.e., pixel current itft is supplied from the first transistor M1 to the amplifier 180. Here, the pixel current itft is determined, corresponding to the threshold voltage and mobility of the first transistor M1 included in each pixel.

[0057] The first current itft supplied from the pixel circuit 142 is supplied to the ground power source GND via the diode-coupled eleventh transistor M11. In this case, the second current iM12, which is i times greater than the pixel current itft, flows through the fifth transistor M12 coupled in the form of the current mirror to the fourth transistor M11. Since the second current iM12 is set to be greater than the reference current iref, a third current iout is supplied from the error compensator 190.

[0058] Here, the reference current iref is set (or predetermined) to have a low current value, corresponding to the specific data signal. Then, the third current iout is set to have a current value higher than that of the first current itft. That is, the amplifier 180 generates the third current iout that is a high current value, using the first current itft that is a micro-current.

[0059] FIG. 6 is a circuit diagram illustrating an embodiment of the current supply unit shown in FIG. 5.

[0060] Referring to FIG. 6, the current supply unit 182 according to this embodiment includes a plurality of current sources Is, and a switch SW coupled between each current source Is and a third power source VDD.

[0061] The current source Is supplies a set current. The switch SW is coupled between the third power source VDD and each current power source Is so as to control whether the current is supplied from the current source Is. Practically, the turn-on/turn-off of the switch SW is controlled so that a desired reference current iref can be supplied, in consideration of characteristics of a panel, etc.

[0062] FIG. 7 is a circuit diagram illustrating an error compensator according to an embodiment of the present invention.

[0063] Referring to FIG. 7, the error compensator 190 according to this embodiment includes a first operational amplifier (OP-AMP) 192, a second OP-AMP 194, a first switch SW1, a second switch SW2, a third switch SW3, a fourth switch SW4, a first capacitor C1, a first storage unit 196 and a second storage unit 198.

[0064] A first input terminal (negative input terminal: -) of the first OP-AMP 192 is coupled to the amplifier 180 via the third switch SW3, and a second input terminal (positive input terminal: +) of the first OP-AMP 192 receives a first reference voltage Vref1. A first output terminal of the first OP-AMP 192 is coupled to the first storage unit 196. The first OP-AMP 192 provides the first storage unit 196 with the voltage input from the amplifier 180 while being operated as a buffer or integrator.

[0065] The first switch SW1 is coupled between the first input terminal (-) and the first output terminal of the first OP-AMP 192. In a case where the first switch SW1 is turned on, the first OP-AMP 192 is driven as a buffer. In a case where the first switch SW1 is turned off, the first OP-AMP 192 is driven as an integrator. To this end, the first capacitor C1 is coupled in parallel to the first switch SW1 between the first input terminal (-) and the first output terminal of the first OP-AMP 192.

[0066] The third switch SW3 is coupled between the first input terminal (-) of the first OP-AMP 192 and the amplifier 180. The third switch SW3 controls the electrical coupling between the first OP-AMP 192 and the amplifier 180 while being turned on and turned off.

[0067] In addition, when the third switch SW3 is turned on, the third current iout described above is supplied to the amplifier 180. Here, the third current iout is supplied from a virtual current source (or voltage source). The first OP-AMP 192 inversely amplifies a voltage corresponding to the third current iout and provides the inversely amplified voltage to the first storage unit 196.

[0068] A first input terminal (-) of the second OP-AMP 194 is coupled to the first storage unit 196, and a second input terminal (+) of the second OP-AMP 194 receives a second reference voltage Vref2. A second output terminal of the second OP-AMP 194 is coupled to the ADC 200 via the fourth switch SW4. The second OP-AMP 194 supplies the voltage provided from the first storage unit 196 to the ADC 200 while being operated as a buffer or integrator.

[0069] The second switch SW2 is coupled between the first input terminal (-) and the second output terminal of the second OP-AMP 194. In a case where the second switch SW2 is turned on, the second OP-AMP 194 is driven as a buffer. In a case where the second switch SW2 is turned off, the second OP-AMP 194 is driven as an integrator. Meanwhile, in an embodiment of the present invention, the first and second reference voltages Vref1 and Vref2 are experimentally determined as refer-

ence voltages for inversion amplification, in consideration of the characteristics of the panel.

[0070] The fourth switch SW4 is coupled between the second output terminal of the second OP-AMP 194 and the ADC 200. The fourth switch SW4 controls the electrical coupling between the second OP-AMP 194 and the ADC 200 while being turned on and turned off.

[0071] The first storage unit 196 is coupled between the first output terminal and the first input terminal (-) of the first OP-AMP 192. Error component existing between the third switch SW3 and the ADC 200, e.g., offsets, line resistances, noises and element characteristics of the first and second OP-AMPs 192 and 194 are stored in the first storage unit 196. To this end, the first storage unit 196 includes a fifth switch SW5, a third capacitor C3 and a sixth switch SW6, which are coupled in parallel between the first output terminal and the first input terminal (-) of the first OP-AMP 192, and a seventh switch SW7, a fourth capacitor C4 and an eighth switch SW8, which are coupled in parallel to the fifth switch SW5, the third capacitor C3 and the sixth switch SW6 between the first output terminal and the first input terminal (-) of the first OP-AMP 192.

[0072] The fifth and sixth switches SW5 and SW6 store an error component in the third capacitor C3 while being simultaneously turned on. The seventh and eighth switches SW7 and SW8 store an error component in the fourth capacitor C4 while being turned on at a time different from that when the fifth switch SW5 is turned on.

[0073] The second storage unit 198 stores a voltage corresponding to the third current iout, except the error component stored in the first storage unit 196 and the error component of the amplifier 180 (circuit characteristics and error components for amplification). To this end, the first storage unit 196 includes a second capacitor C2, and ninth to twelfth switches SW9 to SW12.

[0074] The second capacitor C2 is coupled between tenth and eleventh nodes N10 and N11. The second capacitor C2 stores a specific voltage except error components.

[0075] The eleventh switch SW11 is coupled between the tenth node N10 and the first input terminal (-) of the second OP-AMP 194. The twelfth switch SW12 is coupled between the eleventh node N11 and the second output terminal of the second OP-AMP 194. The eleventh and twelfth switches SW11 and SW12 store a predetermined voltage in the second capacitor C2 while being simultaneously turned on and turned off.

[0076] The ninth switch SW9 is coupled between the eleventh node N11 and the first input terminal (-) of the second OP-AMP 194. The tenth switch SW10 is coupled between the tenth node N10 and the second output terminal of the second OP-AMP 194. The ninth and tenth switches SW9 and SW10 store a set voltage in the second capacitor C2 while being simultaneously turned on and turned off. Here, the turn-on periods of the ninth and eleventh switches SW9 and SW11 do not overlap with each other.

[0077] FIG. 8 is a waveform diagram illustrating an operation process of the error compensator shown in FIG. 7.

[0078] Referring to FIG. 8, the first switch SW1, the second switch SW2, the fourth switch SW4, the fifth switch SW5 and the sixth switch SW6 are turned on during a first period T1.

[0079] If the fourth switch SW4 is turned on, the ADC 200 and the second output terminal of the second OP-AMP 194 are electrically coupled to each other.

[0080] If the first switch SW1 is turned on, the first OP-AMP 192 is coupled in the form of a buffer. Then, the first reference voltage Vref1 is applied to the first output terminal of the first OP-AMP 192 due to virtual ground characteristics of the OP-AMP.

[0081] If the second switch SW2 is turned on, the second OP-AMP 194 is coupled in the form of a buffer. Then, the second reference voltage Vref2 is applied to the second output of the second OP-AMP 194 due to the virtual ground characteristics of the OP-AMP.

[0082] If the fifth switch SW5 is turned on, the first output terminal of the first OP-AMP 192 and one terminal of the third capacitor C3 are electrically coupled to each other. If the sixth switch SW6 is turned on, the second output terminal of the second OP-AMP 194 and the other terminal of the third capacitor C3 are electrically coupled to each other. In this case, the third capacitor C3 ideally stores a voltage corresponding to the difference between the first and second reference voltages Vref1 and Vref2. However, practically, a set voltage including error components (e.g., offsets, line resistances, noises and element characteristics of the OP-AMPs) is stored in the third capacitor C3. Practically, error components from the third switch SW3 to the ADC 200 are stored in the form of voltage in the third capacitor C3 during the first period T1.

[0083] The first switch SW1, the second switch SW2, the fourth switch SW4, the seventh switch SW7 and the eighth switch SW8 are turned on during a second period T2.

[0084] If the first switch SW1 is turned on, the first reference voltage Vref1 is applied to the first output terminal of the first OP-AMP 192. If the second switch SW2 is turned on, the second reference voltage Vref2 is applied to the second output terminal of the second OP-AMP 194.

[0085] If the seventh switch SW7 is turned on, the first output terminal of the first OP-AMP 192 and one terminal of the fourth capacitor C4 are electrically coupled to each other. If the eighth switch SW8 is turned on, the other terminal of the fourth capacitor C4 and the second output terminal of the second OP-AMP 194 are electrically coupled to each other. In this case, a set voltage including an error component of the error compensator 190 is charged in the fourth capacitor C4. For example, the same voltage as that of the third capacity C3 is stored in the fourth capacitor C4. Subsequently, for convenience of illustration, it is assumed that the same voltage is stored in the third and fourth capacitors C3 and C4.

[0086] The third switch SW3, the fifth switch SW5, the

sixth switch SW6, the ninth switch SW9 and the tenth switch SW10 are turned on during a third period T3. The third period is set to be a short time period so that only the error component of the amplifier 180 is supplied to the error compensator 190. In other words, the third switch SW3 is instantaneously turned on and then turned off so that the voltage corresponding to the third current iout is not applied to the first input terminal (-) of the first OP-AMP 192.

[0087] Then, a set voltage including the error component of the amplifier 180 is applied to the first input terminal (-) of the first OP-AMP 192 during the third period T3. The first OP-AMP 192 inversely amplifies a predetermined voltage and supplies a first voltage to the first output terminal of the first OP-AMP 192 while being driven as an integrator during the third period T3.

[0088] The first voltage output to the first output terminal of the first OP-AMP 192 is supplied to the first input terminal (-) of the second OP-AMP 194 by coupling of the third capacitor C3. In this case, the first voltage is changed into a second voltage, corresponding to the voltage stored in the third capacitor C3. Here, an error component of the error compensator 190 is additionally included in the second voltage. Meanwhile, since the ninth and tenth switches SW9 and SW10 are turned on, the second voltage is stored in the second capacitor C2. Subsequently, for convenience of illustration, it is assumed that when the eleventh node N11 is coupled to the first input terminal (-) of the second OP-AMP 194, a voltage in the reverse direction is stored in the second capacitor C2. In addition, it is assumed that when the tenth node N10 is coupled to the first input terminal (-) of the second OP-AMP 194, a voltage in the forward direction is stored in the second capacitor C2. In this case, the second voltage in the reverse direction is stored in the second capacitor C2 during the third period T3.

[0089] Subsequently, the third switch SW3, the seventh switch SW7, the eighth switch SW8, the eleventh switch SW11 and the twelfth switch SW12 are turned on during a fourth period T4. Here, the fourth period T4 is set to a period wider than the third period T3.

[0090] If the third switch SW3 is turned on during the fourth period T4, a third voltage corresponding to the third current iout is applied to the first input terminal (-) of the first OP-AMP 192. Here, the fourth period T4 is set to a sufficiently wide time so that the third voltage can be stably applied. The first OP-AMP 192 inversely amplifies the third voltage and supplies the inversely amplified voltage to the first output terminal of the first OP-AMP 192 while being driven as an integrator during the fourth period T4. The voltage supplied to the first output terminal of the first OP-AMP 192 is changed into a fourth voltage by coupling of the fourth capacitor C4 so that the fourth voltage is supplied to the first input terminal (-) of the second OP-AMP 194. In this case, the eleventh and twelfth switches SW11 and SW12 are turned on, and hence the fourth voltage in the forward direction is stored in the second capacitor C2.

[0091] Meanwhile, the error components are offset by the second voltage in the reverse direction, stored in the second capacitor C2 during the third period T3, and the fourth voltage in the forward direction, stored in the second capacitor C2 during the fourth period T4. In other words, a set voltage corresponding to the third current iout is charged in the second capacitor C2 during the fourth period T4, regardless of the error components of the amplifier 180 and the error compensator 190.

[0092] Subsequently, the fourth switch SW4, the eleventh switch SW11 and the twelfth switch SW12 are turned on during a fifth period T5. If the fourth switch SW4 is turned on, the ADC 200 and the second output terminal of the second OP-AMP 194 are electrically coupled to each other. If the eleventh switch SW11 is turned on, the tenth node N10 is coupled to the first input terminal (-) of the second OP-AMP 194. If the twelfth switch SW12 is turned on, the eleventh node N11 is coupled to the second output terminal of the second OP-AMP 194. Then, the second OP-AMP 194 supplies, to the ADC 200, a set voltage corresponding to the set voltage stored in the second capacitor C2. The ADC 200 converts a set voltage supplied thereto into a digital value, and stores the converted digital value in the memory 210.

[0093] Practically, in an embodiment of the present invention, the threshold voltage and mobility information of the driving transistor included in each pixel 140 is extracted by repeating the aforementioned procedure during the sensing period. As described above, in an embodiment of the present invention, only pure information from which the error components of the amplifier 180 and the error compensator 190 are removed may be extracted, and accordingly, the accuracy of compensation can be improved. In addition, the error compensator 190 according to this embodiment is used to extract only a desired voltage by removing error components, and can be applied to various circuits for amplifying a predetermined current and/or voltage.

[0094] FIG. 9 is a circuit diagram illustrating another embodiment of the amplifier. In FIG. 9, components identical to those of FIG. 5 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0095] Referring to FIG. 9, the amplifier 180 according to this embodiment includes a current supply unit 182, a fourth transistor M11', a fifth transistor M12', a thirteenth switch SW20, a fourteenth switch SW21 and a fifteenth switch 22.

[0096] The fourth transistor M11' is coupled between the pixel 140 and the ground power source GND. The thirteenth switch SW20 is formed between the pixel 140 and a gate electrode of the fourth transistor M11'. When the thirteenth switch SW20 is turned on, the fourth transistor M11' is diode-coupled so that current can flow from the pixel 140 and the ground power source GND.

[0097] The fifth transistor M12' is coupled between the current supply unit 182 and the ground power source GND. A gate electrode of the fifth transistor M12' is coupled to the gate electrode of the fourth transistor M11'.

That is, the fifth transistor M12' is coupled in the form of a current mirror to the fourth transistor M11'.

[0098] The fourteenth switch SW21 is coupled between the gate electrode of the fourth transistor M11' and the ground power source GND. If the fourteenth switch SW21 is turned on, the ground power source GND is supplied to the gate electrodes of the fourth and fifth transistors M11' and M12', and accordingly, the fourth and fifth transistors M11' and M12' are turned off.

[0099] The fifteenth switch SW22 is formed between the pixel 140 and a common terminal of the current supply unit 182 and the error compensator 190. If the fifteenth switch SW22 is turned on, the pixel 140, the current supply unit 182 and the error compensator 190 are electrically coupled to one another.

[0100] FIG. 10 is a waveform diagram illustrating an operation process of the amplifier shown in FIG. 9.

[0101] Referring to FIG. 10, it is assumed that the third transistor M3 included in the pixel 140 is first turned on during the sensing period.

[0102] The thirteenth switch SW20 is turned on during a period in which the threshold voltage information of the first transistor M1 is extracted in the sensing period. If the thirteenth switch SW20 is turned on, the fourth transistor M11' is diode-coupled. In this case, the amplifier 180 shown in FIG. 9 is driven identically to the amplifier 180 shown in FIG. 4, and therefore, its detailed description will be omitted.

[0103] The fourteenth and fifteenth switches SW21 and SW22 are turned on during a period in which the degradation information of the organic light emitting diode OLED is extracted in the sensing period. If the fourteenth switch SW21 is turned on, the fourth and fifth transistors M11' and M12' are turned off.

[0104] If the fifteenth switch SW22 is turned on, the reference current iref from the current supply unit 182 is supplied to the second power source ELVSS via the anode electrode of the organic light emitting diode OLED. In this case, a set voltage corresponding to the reference current iref is applied to the organic light emitting diode OLED.

[0105] The resistance is changed corresponding to the degree of degradation of the organic light emitting diode OLED, and accordingly, degradation information is included in the set voltage applied to the organic light emitting diode OLED, corresponding to the reference current iref. The set voltage applied to the organic light emitting diode OLED is supplied to the error compensator 190.

[0106] That is, the amplifier 180 according to this embodiment can extract the degradation information of the organic light emitting diode OLED and the threshold voltage information of the first transistor M1 from the pixel 140 while being driven as a current source or current sink source. In addition, the operation process of the error compensator 190 is identical to that described above, and therefore, its detailed description will be omitted.

[0107] While the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

[0108] In the claims, it will be understood that the first and second transistors M11, M12 are referred to in the description as fourth and fifth transistors M11, M12. It will further be understood that the first to third switches SW20 - SW22 are referred to in the description as thirteenth to fifteenth switches SW20 - SW22.

Claims

1. An error compensator adapted to receive an input signal at its input and to provide an error compensated signal at its output, the error compensator comprising:

a first operational amplifier (192) and a second operational amplifier (194);
a first switch (SW1) and a first capacitor (C1), connected in parallel between a first input terminal and an output terminal of the first operational amplifier (192);
a second switch (SW2) connected between a first input terminal and an output terminal of the second operational amplifier (194);
a third switch (SW3) connected between the first input terminal of the first operational amplifier and the input of the error compensator;
a fourth switch (SW4) connected between the output terminal of the second operational amplifier (194) and the output of the error compensator;
a first storage unit (196) connected between the output terminal of the first operational amplifier (192) and the first input terminal of the second operational amplifier (194); and
a second storage unit (198) connected between the first input terminal and the output terminal of the second operational amplifier (194),

wherein the first storage unit (196) includes:

a fifth switch (SW5), a third capacitor (C3) and a sixth switch (SW6), coupled in series between the output terminal of the first operational amplifier (192) and the first input terminal of the second operational amplifier (194); and
a seventh switch (SW7), a fourth capacitor (C4) and an eighth switch (SW8), coupled in parallel to the fifth switch (SW5), the third capacitor (C3) and the sixth switch (SW6), between the output terminal of the first operational amplifier and the first input terminal of the second operational amplifier,
wherein the fifth and sixth switches (SW5 and

SW6) are configured to be turned on during a first period in the period in which the first and second switches (SW1 and SW2) are turned on, and the seventh and eighth switches (SW7 and SW8) are configured to be turned on during a second period not overlapping with the first period in the period in which the first and second switches (SW1 and SW2) are turned on and/or wherein the fourth switch (SW4) is configured to be also set to be in a turn-on state during the first and second periods; and

wherein the second storage unit (198) includes:

a second capacitor (C2) coupled between first and second nodes (N10 and N11); a ninth switch (SW9) coupled between the second node and the first input terminal of the second operational amplifier (194);
a tenth switch (SW10) coupled between the first node and the output terminal of the second operational amplifier (194);
an eleventh switch (SW11) coupled between the first node and the first input terminal of the second operational amplifier (194); and a twelfth switch (SW12) coupled between the second node and the output terminal of the second operational amplifier (194).

2. The error compensator of claim 1, wherein a first reference power source is connected to a second input terminal of the first operational amplifier (192), and a second reference power source is connected to a second input terminal of the second operational amplifier (194).

3. The error compensator of claim 1, wherein the fifth switch (SW5), the sixth switch (SW6), the ninth switch (SW9) and the tenth switch (SW10) are configured to be turned on during a third period in the period in which the third switch (SW3) is turned on, and the seventh switch (SW7), the eighth switch (SW8), the eleventh switch (SW11) and the twelfth switch (SW12) are configured to be turned on during a fourth period not overlapping with the third period in the period in which the third switch (SW3) is turned on, wherein the fourth period may be set to be longer than the third period and/or wherein the fourth switch (SW4), the eleventh switch (SW11) and the twelfth switch (SW12) are configured to be turned on during a period after the fourth period.

4. A sensing unit (170) comprising an amplifier (180), an error compensator (190) according to any one of the preceding claims and an analog to digital converter (200), wherein the output of the amplifier is connected to the input of the error compensator (190) and the output of the error compensator (190) is connected to the input of the analog to digital converter (200).

5. A sensing unit according to claim 4, further comprising a memory (210) connected to the output of the analog to digital converter.

6. A system comprising a pixel (140) and a sensing unit (170) according to claim 5, wherein the amplifier (180) is connected to the pixel (140) and the memory (210) is arranged to store threshold voltage information and/or degradation information extracted from the pixel.

Patentansprüche

1. Fehlerkompensator, der zum Empfangen eines Eingangssignals an seinem Eingang und zum Bereitstellen eines fehlerkompensierten Signals an seinem Ausgang angepasst ist, der Fehlerkompensator umfassend:

einen ersten Operationsverstärker (192) und einen zweiten Operationsverstärker (194);
einen ersten Schalter (SW1) und einen ersten Kondensator (C1), die parallel zwischen einem ersten Eingangsanschluss und einem Ausgangsanschluss des ersten Operationsverstärkers (192) geschaltet sind;
einen zweiten Schalter (SW2), der zwischen einem ersten Eingangsanschluss und einem Ausgangsanschluss des zweiten Operationsverstärkers (194) geschaltet ist;
einen dritten Schalter (SW3), der zwischen dem ersten Eingangsanschluss des ersten Operationsverstärkers und dem Eingang des Fehlerkompensators geschaltet ist;
einen vierten Schalter (SW4), der zwischen dem Ausgangsanschluss des zweiten Operationsverstärkers (194) und dem Ausgang des Fehlerkompensators geschaltet ist;
eine erste Speichereinheit (196), die zwischen dem Ausgangsanschluss des ersten Operationsverstärkers (192) und dem ersten Eingangsanschluss des zweiten Operationsverstärkers (194) geschaltet ist; und
eine zweite Speichereinheit (198), die zwischen dem ersten Eingangsanschluss und dem Ausgangsanschluss des zweiten Operationsverstärkers (194) geschaltet ist,

wobei die erste Speichereinheit (196) enthält:

einen fünften Schalter (SW5), einen dritten Kondensator (C3) und einen sechsten Schalter (SW6), die in Reihe zwischen dem Ausgangsanschluss des ersten Operationsverstärkers

(192) und dem ersten Eingangsanschluss des zweiten Operationsverstärkers (194) gekoppelt sind; und

einen siebten Schalter (SW7), einen vierten Kondensator (C4) und einen achten Schalter (SW8), die parallel zu dem fünften Schalter (SW5), dem dritten Kondensator (C3) und dem sechsten Schalter (SW6) zwischen dem Ausgangsanschluss des ersten Operationsverstärkers und dem ersten Eingangsanschluss des zweiten Operationsverstärkers gekoppelt sind, wobei die fünften und sechsten Schalter (SW5 und SW6) so konfiguriert sind, dass sie während eines ersten Zeitraums in dem Zeitraum eingeschaltet sind, in dem die ersten und zweiten Schalter (SW1 und SW2) eingeschaltet sind, und die siebenten und achten Schalter (SW7 und SW8) so konfiguriert sind, dass sie während eines zweiten Zeitraums, der sich mit dem ersten Zeitraum nicht überschneidet, in dem Zeitraum eingeschaltet sind, in dem die ersten und zweiten Schalter (SW1 und SW2) eingeschaltet sind, und/oder wobei der vierte Schalter (SW4) so konfiguriert ist, dass er während des ersten und zweiten Zeitraums ebenfalls in einen eingeschalteten Zustand versetzt ist; und

wobei die zweite Speichereinheit (198) enthält:

einen zweiten Kondensator (C2), der zwischen ersten und zweiten Knoten (N10 und N11) gekoppelt ist;

einen neunten Schalter (SW9), der zwischen dem zweiten Knoten und dem ersten Eingangsanschluss des zweiten Operationsverstärkers (194) gekoppelt ist;

einen zehnten Schalter (SW10), der zwischen dem ersten Knoten und dem Ausgangsanschluss des zweiten Operationsverstärkers (194) gekoppelt ist;

einen elften Schalter (SW11), der zwischen dem ersten Knoten und dem ersten Eingangsanschluss des zweiten Operationsverstärkers (194) gekoppelt ist; und

einen zwölften Schalter (SW12), der zwischen dem zweiten Knoten und dem Ausgangsanschluss des zweiten Operationsverstärkers (194) gekoppelt ist.

2. Fehlerkompensator nach Anspruch 1, wobei eine erste Referenzstromquelle mit einem zweiten Eingangsanschluss des ersten Operationsverstärkers (192) verbunden ist und eine zweite Referenzstromquelle mit einem zweiten Eingangsanschluss des zweiten Operationsverstärkers (194) verbunden ist.

3. Fehlerkompensator nach Anspruch 1, wobei der fünfte Schalter (SW5), der sechste Schalter (SW6), der neunte Schalter (SW9) und der zehnte Schalter (SW10) so konfiguriert sind, dass sie während eines dritten Zeitraums in dem Zeitraum eingeschaltet sind, in dem der dritte Schalter (SW3) eingeschaltet ist, und der siebte Schalter (SW7), der achte Schalter (SW8), der elfte Schalter (SW11) und der zwölfte Schalter (SW12) so konfiguriert sind, dass sie während eines vierten Zeitraums, der sich mit dem dritten Zeitraum nicht überschneidet, in dem Zeitraum eingeschaltet sind, in dem der dritte Schalter (SW3) eingeschaltet ist, wobei der vierte Zeitraum länger als der dritte Zeitraum eingestellt sein kann und/oder wobei der vierte Schalter (SW4), der elfte Schalter (SW11) und der zwölfte Schalter (SW12) so konfiguriert sind, dass sie während eines Zeitraums nach dem vierten Zeitraum eingeschaltet sind.

4. Sensoreinheit (170), umfassend einen Verstärker (180), einen Fehlerkompensator (190) nach einem der vorhergehenden Ansprüche und einen Analog-Digital-Wandler (200), wobei der Ausgang des Verstärkers mit dem Eingang des Fehlerkompensators (190) verbunden ist und der Ausgang des Fehlerkompensators (190) mit dem Eingang des Analog-Digital-Wandlers (200) verbunden ist.

5. Sensoreinheit nach Anspruch 4, ferner umfassend einen Speicher (210), der mit dem Ausgang des Analog-Digital-Wandlers verbunden ist.

6. System, umfassend ein Pixel (140) und eine Sensoreinheit (170) nach Anspruch 5, wobei der Verstärker (180) mit dem Pixel (140) verbunden ist und der Speicher (210) dazu angeordnet ist, aus dem Pixel extrahierte Schwellenspannungsinformationen und/oder Degradationsinformationen zu speichern.

Revendications

1. Compensateur d'erreur adapté pour recevoir un signal d'entrée au niveau de son entrée et pour fournir un signal à compensation d'erreur au niveau de sa sortie, le compensateur d'erreur comprenant :

un premier amplificateur opérationnel (192) et un deuxième amplificateur opérationnel (194) ;

un premier commutateur (SW1) et un premier condensateur (C1) reliés en parallèle entre une première borne d'entrée et une borne de sortie du premier amplificateur opérationnel (192) ;

un deuxième commutateur (SW2) relié entre une première borne d'entrée et une borne de sortie du deuxième amplificateur opérationnel (194) ;

un troisième commutateur (SW3) relié entre la première borne d'entrée du premier amplificateur opérationnel et l'entrée du compensateur

d'erreur ;
un quatrième commutateur (SW4) relié entre la borne de sortie du deuxième amplificateur opérationnel (194) et la sortie du compensateur d'erreur ;
une première unité de stockage (196) reliée entre la borne de sortie du premier amplificateur opérationnel (192) et la première borne d'entrée du deuxième amplificateur opérationnel (194) ; et
une deuxième unité de stockage (198) reliée entre la première borne d'entrée et la borne de sortie du deuxième amplificateur opérationnel (194),

dans lequel la première unité de stockage (196) comporte :

un cinquième commutateur (SW5), un troisième condensateur (C3) et un sixième commutateur (SW6) couplés en série entre la borne de sortie du premier amplificateur opérationnel (192) et la première borne d'entrée du deuxième amplificateur opérationnel (194) ; et
un septième commutateur (SW7), un quatrième condensateur (C4) et un huitième commutateur (SW8) couplés en parallèle au cinquième commutateur (SW5), au troisième condensateur (C3) et au sixième commutateur (SW6) entre la borne de sortie du premier amplificateur opérationnel et la première borne d'entrée du deuxième amplificateur opérationnel,
dans lequel les cinquième et sixième commutateurs (SW5 et SW6) sont configurés pour être passants pendant une première période dans la période dans laquelle les premier et deuxième commutateurs (SW1 et SW2) sont passants, et les septième et huitième commutateurs (SW7 et SW8) sont configurés pour être passants pendant une deuxième période qui ne se chevauche pas avec la première période dans la période dans laquelle les premier et deuxième commutateurs (SW1 et SW2) sont passants et/ou dans lequel le quatrième commutateur (SW4) est configuré pour être également mis dans un état passant pendant les première et deuxième périodes ; et

dans lequel la deuxième unité de stockage (198) comporte :

un deuxième condensateur (C2) couplé entre des premier et deuxième noeuds (N10 et N11) ;
un neuvième commutateur (SW9) couplé entre le deuxième noeud et la première borne d'entrée du deuxième amplificateur opérationnel (194) ;
un dixième commutateur (SW10) couplé entre le premier noeud et la borne de sortie du deuxième amplificateur opérationnel (194) ;
un onzième commutateur (SW11) couplé entre le premier noeud et la première borne d'entrée du deuxième amplificateur opérationnel (194) ; et
un douzième commutateur (SW12) couplé entre le deuxième noeud et la borne de sortie du deuxième amplificateur opérationnel (194).

2. Compensateur d'erreur de la revendication 1, dans lequel une première source d'alimentation de référence est reliée à une deuxième borne d'entrée du premier amplificateur opérationnel (192), et une deuxième source d'alimentation de référence est reliée à une deuxième borne d'entrée du deuxième amplificateur opérationnel (194).

3. Compensateur d'erreur de la revendication 1, dans lequel le cinquième commutateur (SW5), le sixième commutateur (SW6), le neuvième commutateur (SW9) et le dixième commutateur (SW10) sont configurés pour être passants pendant une troisième période dans la période dans laquelle le troisième commutateur (SW3) est passant, et le septième commutateur (SW7), le huitième commutateur (SW8), le onzième commutateur (SW11) et le douzième commutateur (SW12) sont configurés pour être passants pendant une quatrième période qui ne se chevauche pas avec la troisième période dans la période dans laquelle le troisième commutateur (SW3) est passant, dans lequel la quatrième période peut être réglée pour être plus longue que la troisième période et/ou dans lequel le quatrième commutateur (SW4), le onzième commutateur (SW11) et le douzième commutateur (SW12) sont configurés pour être passants pendant une période après la quatrième période.

4. Unité de détection (170) comprenant un amplificateur (180), un compensateur d'erreur (190) selon l'une quelconque des revendications précédentes et un convertisseur analogique-numérique (200), où la sortie de l'amplificateur est reliée à l'entrée du compensateur d'erreur (190) et la sortie du compensateur d'erreur (190) est reliée à l'entrée du convertisseur analogique-numérique (200).

5. Unité de détection selon la revendication 4, comprenant en outre une mémoire (210) reliée à la sortie du convertisseur analogique-numérique.

6. Système comprenant un pixel (140) et une unité de détection (170) selon la revendication 5, dans lequel l'amplificateur (180) est relié au pixel (140) et la mémoire (210) est conçue pour stocker des informations de tension de seuil et/ou des informations de dégradation extraites du pixel.

FIG. 1

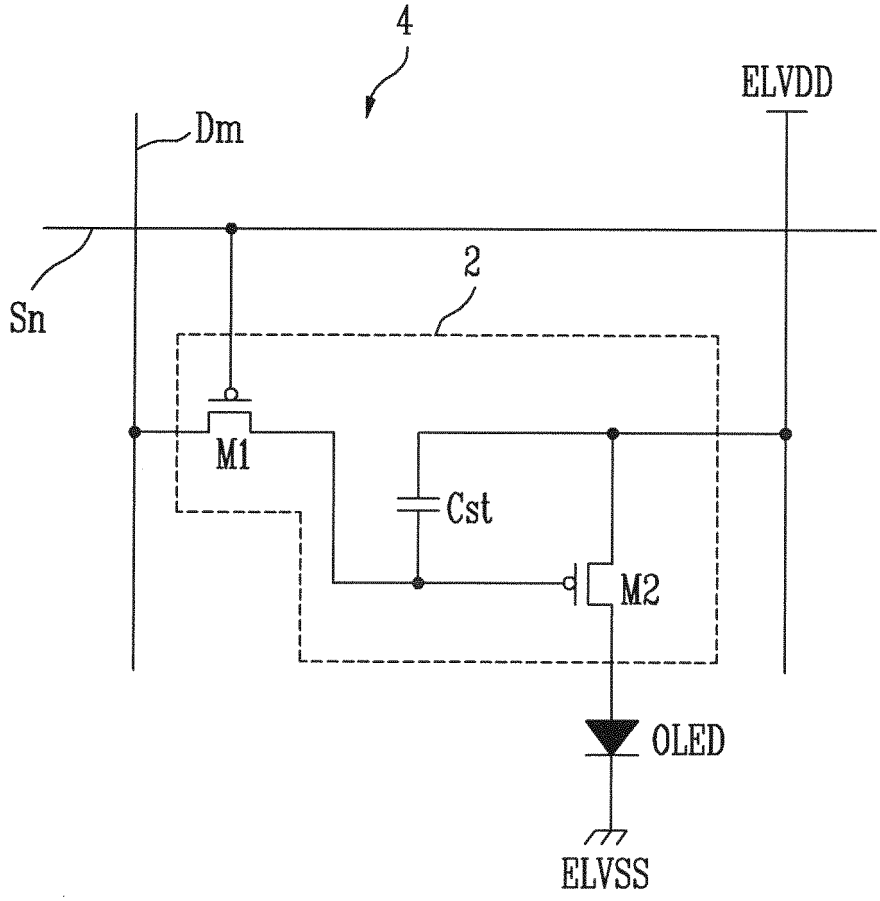


FIG. 2

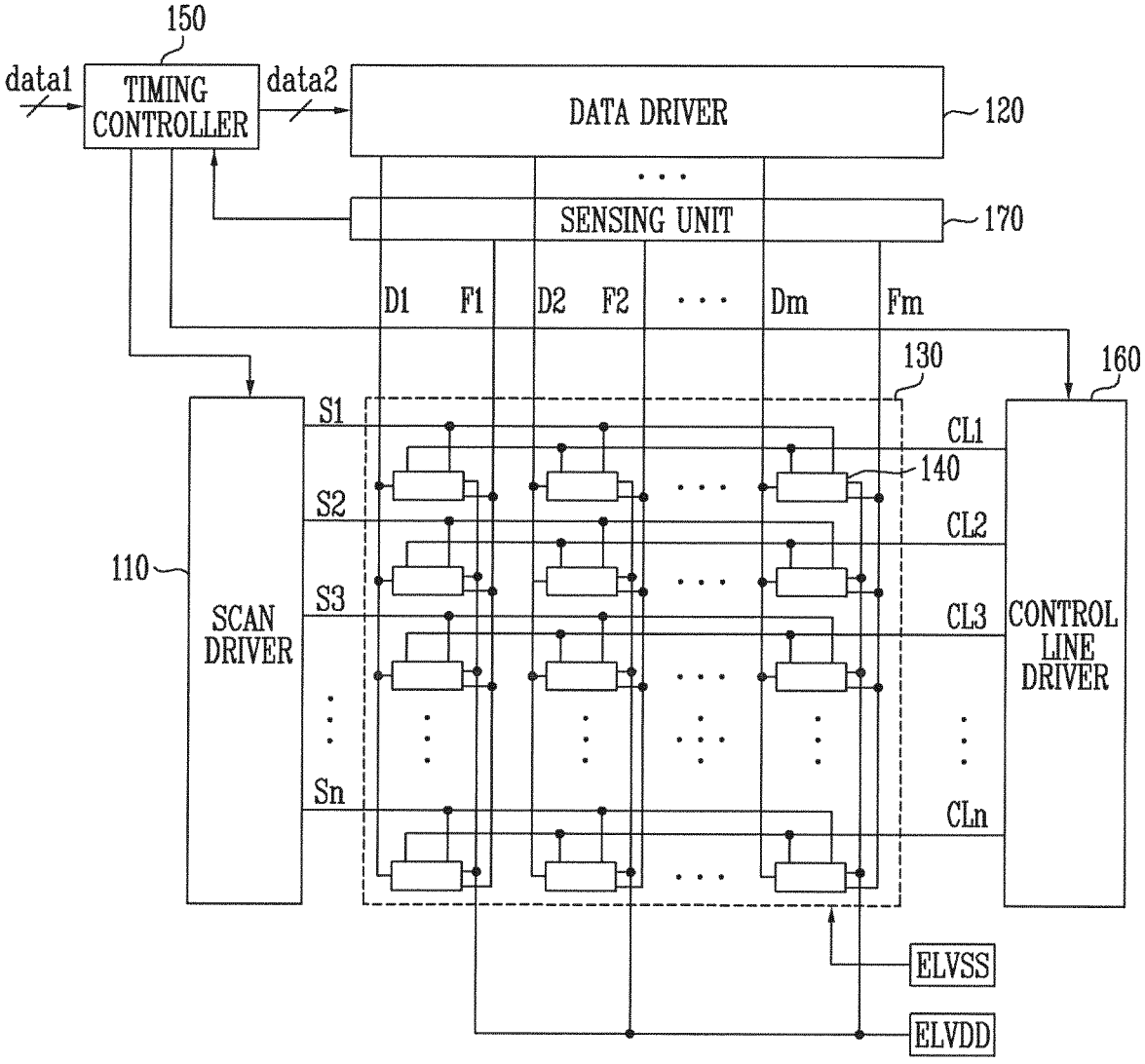

150
data1
TIMING CONTROLLER
data2
DATA DRIVER
120
SENSING UNIT
170
D1
F1
D2
F2
Dm
Fm
130
160
S1
S2
S3
Sn
CL1
CL2
CL3
CLn
140
110
SCAN DRIVER
CONTROL LINE DRIVER
ELVSS
ELVDD

FIG. 3

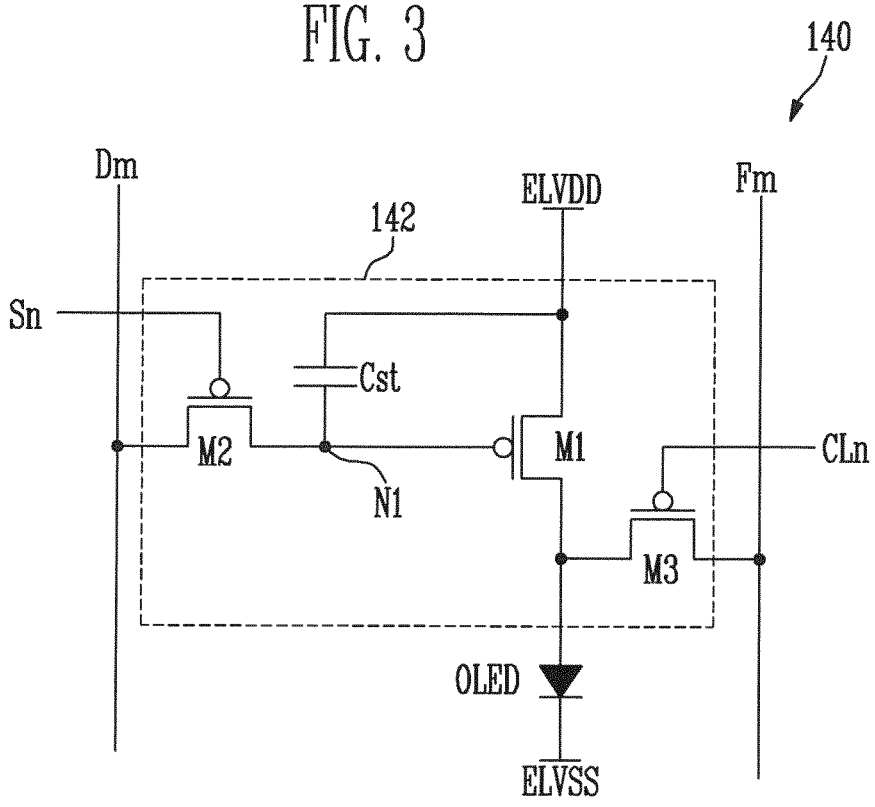

140
Dm
ELVDD
Fm
142
Sn
Cst
M2
M1
CLn
N1
M3
OLED
ELVSS

FIG. 4

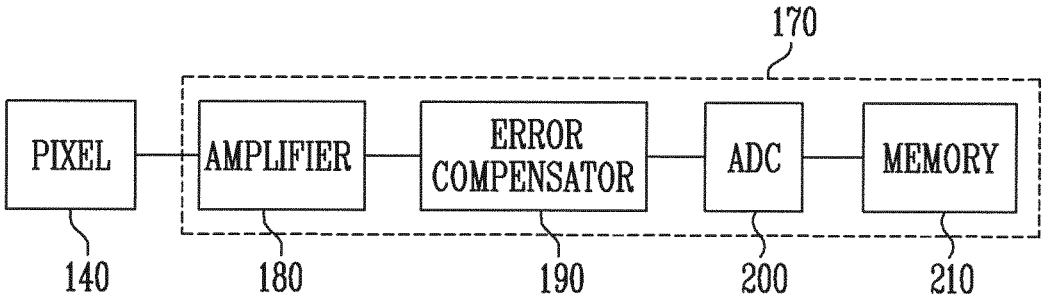

170
PIXEL
AMPLIFIER
ERROR COMPENSATOR
ADC
MEMORY
140
180
190
200
210

FIG. 5

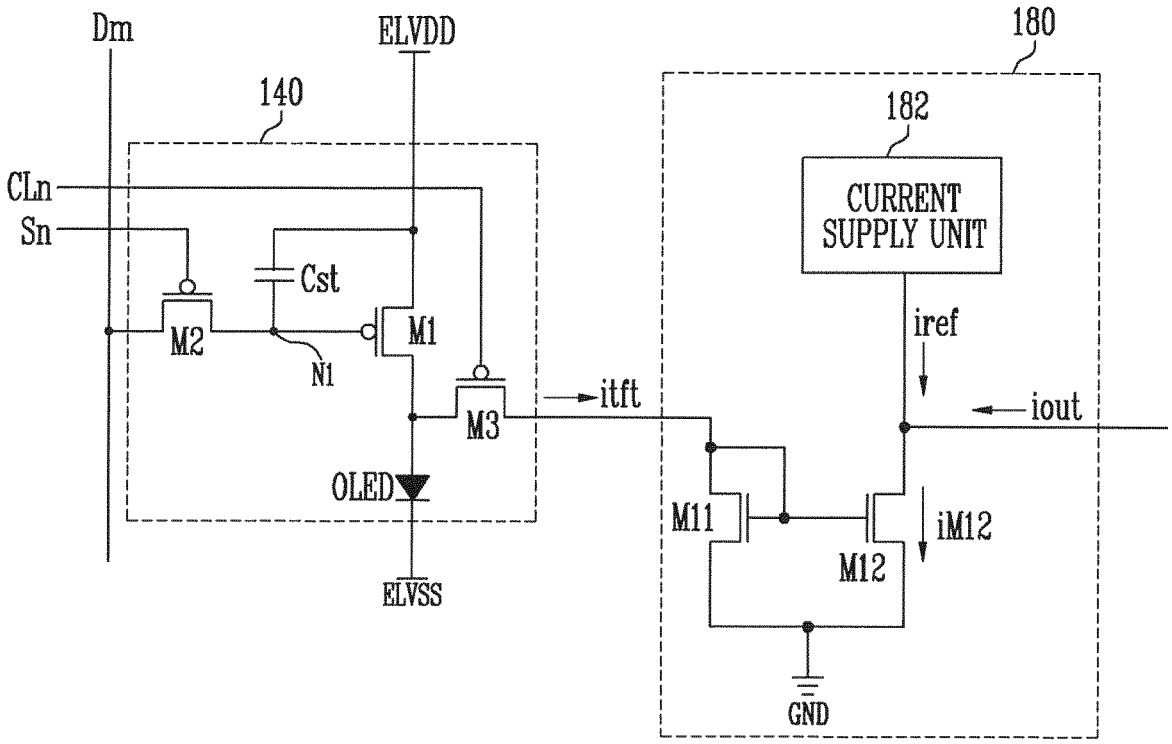

Dm
ELVDD
180
140
182
CLn
Sn
CURRENT SUPPLY UNIT
Cst
iref
M2
M1
N1
itft
iout
M3
OLED
M11
iM12
M12
ELVSS
GND

FIG. 6

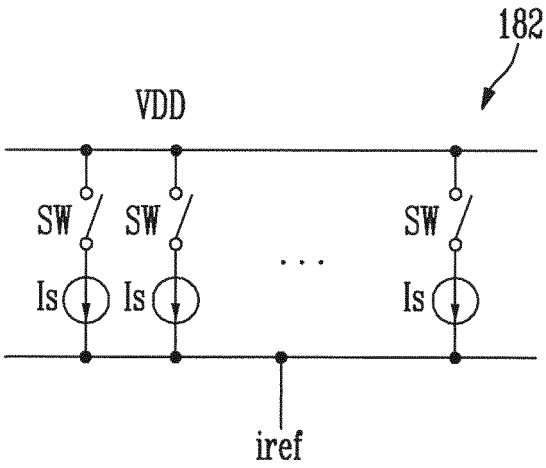

182
VDD
SW
SW
SW
Is
Is
Is
iref

FIG. 7

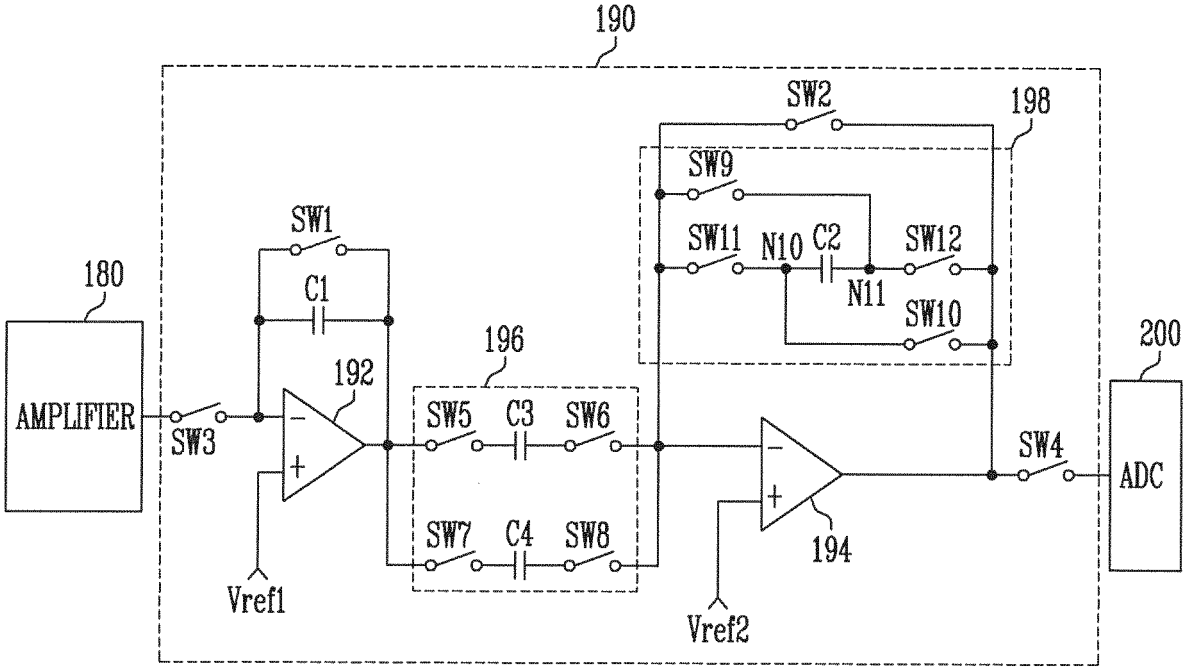

190
198
SW2
SW9
SW1
SW11
N10
C2
SW12
N11
SW10
180
C1
196
200
AMPLIFIER
192
SW3
SW5
C3
SW6
SW4
ADC
SW7
C4
SW8
194
Vref1
Vref2

FIG. 8

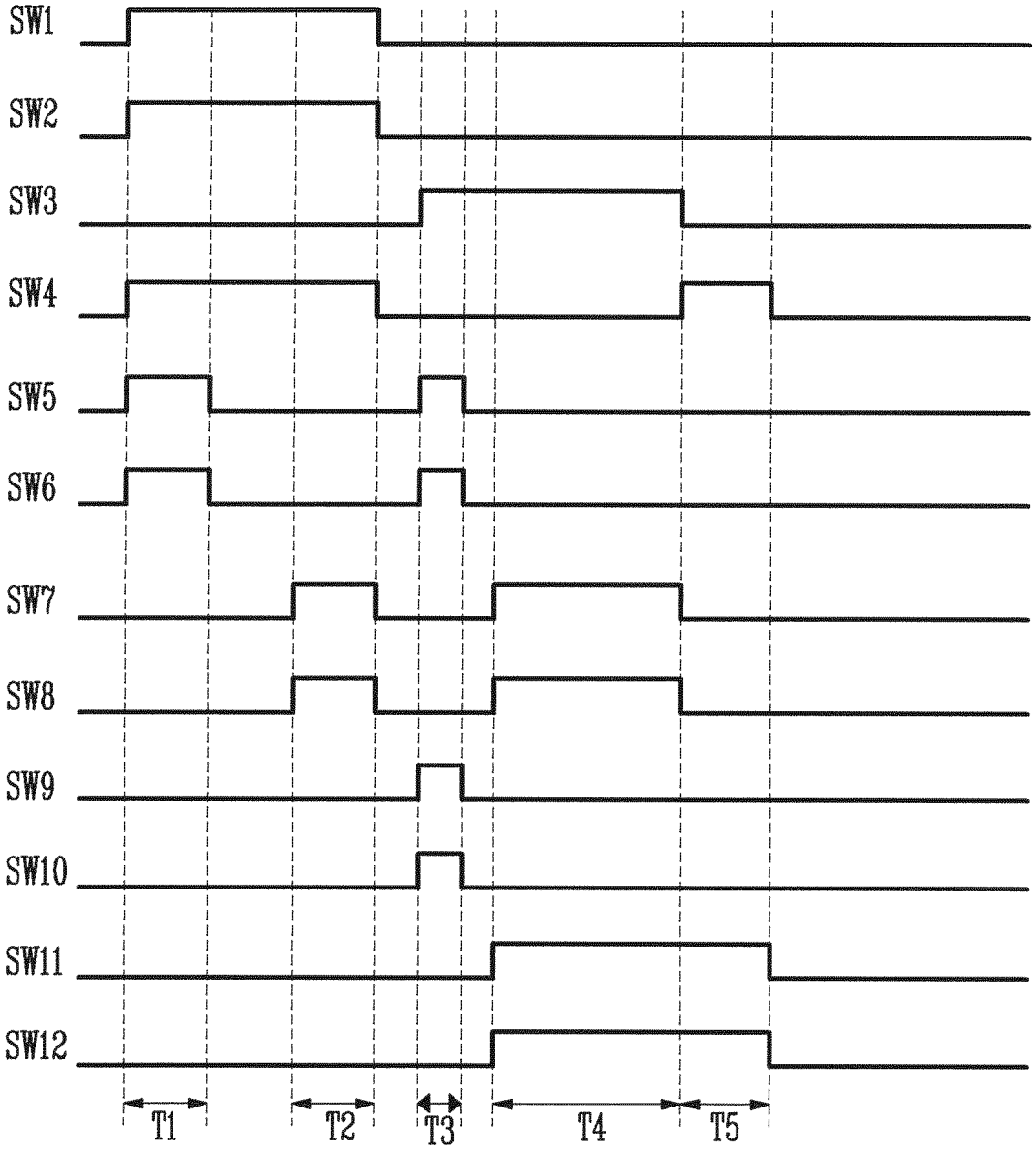


FIG. 9

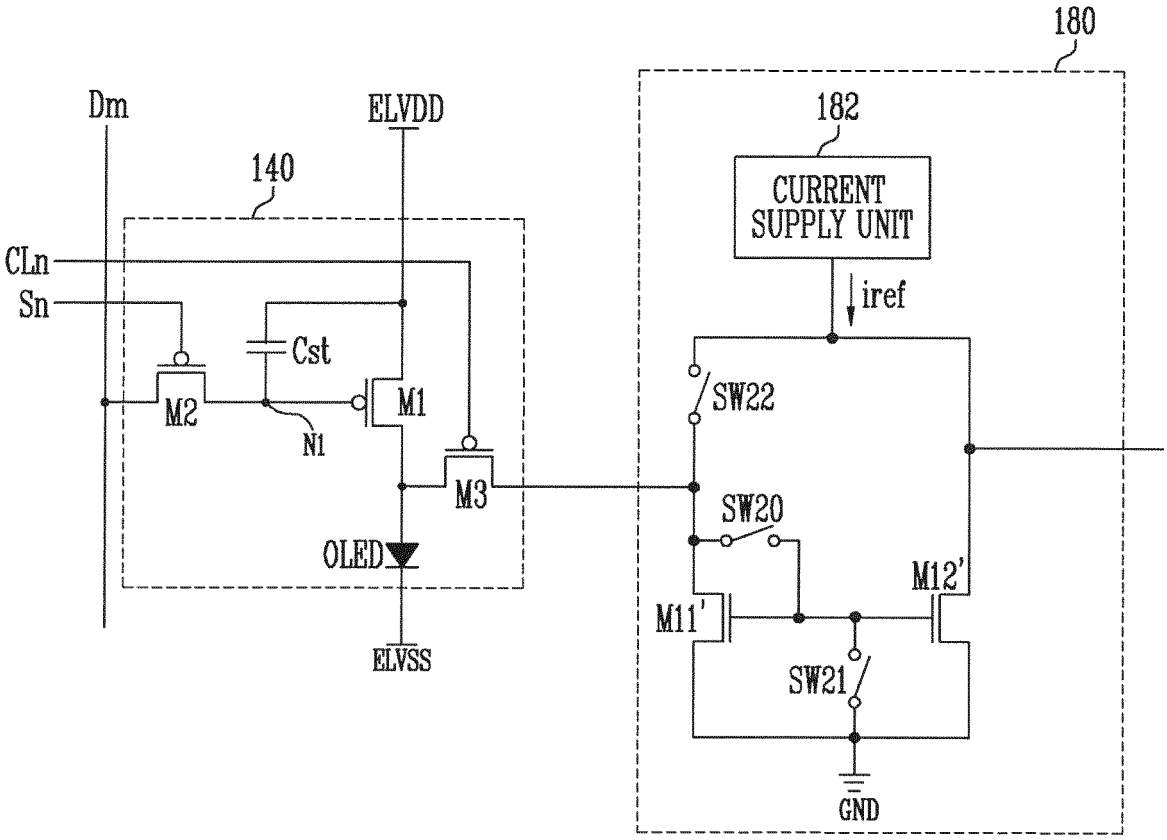
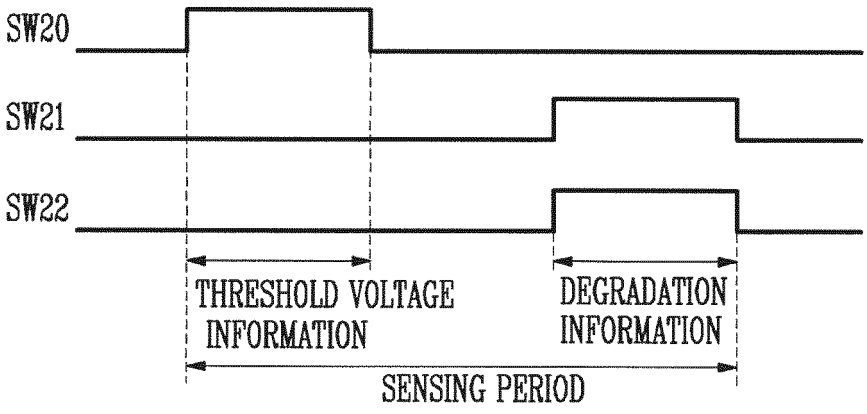

180
182
CURRENT SUPPLY UNIT
iref
Dm
ELVDD
140
CLn
Sn
Cst
M2
M1
N1
M3
OLED
ELVSS
SW22
SW20
M12'
M11'
SW21
GND

FIG. 10


SW20
SW21
SW22
THRESHOLD VOLTAGE INFORMATION
DEGRADATION INFORMATION
SENSING PERIOD

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2002190193 A **[0004]**
- US 2001008422 A **[0004]**

专利名称(译)	误差补偿器和使用其的有机发光显示装置		
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优先权	1020120139059 2012-12-03 KR		
其他公开文献	EP3079143A1		
外部链接	Espacenet		

摘要(译)

一种误差补偿器和使用该误差补偿器的有机发光显示装置。有机发光显示装置包括每个都具有驱动晶体管和有机发光二极管的像素;以及感测单元，从像素的像素提取包括驱动晶体管的阈值电压的第一信息或包括有机发光二极管的劣化的第二信息中的至少一个。在有机发光显示装置中，感测单元包括放大器，放大与第一信息或第二信息中的至少一个相对应的电压;以及误差补偿器，补偿包括在放大器和误差补偿器中的元件的误差分量。

FIG. 1