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(54) **Organic light emitting display comprising an emission driver**

Organische lichtemittierende Anzeige mit einem Emissionstreiber

Affichage électroluminescent organique utilisant un module de commande d'émission

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Description

BACKGROUND

Field

[0001] The field relates to an emission driver and an organic light emitting display using the same, and more particularly to an emission driver and an organic light emitting display using the same for supplying a light emitting control signal to a light emitting control line.

Description of the Related Technology

[0002] Recently, various flat panel displays of reduced weight and volume, which are unfavorable in a cathode ray tube, have been developed. The flat panel display can take the form of, for example, a liquid crystal display, a field emission display, a plasma display panel and an organic light emitting display, etc.

[0003] The organic light emitting display displays an image using an organic light emitting diode (OLED) generating light by recombination of electrons and holes. The organic light emitting display has quick response speed and is driven with low power consumption. A general organic light emitting display supplies current corresponding to data signals to an organic light emitting diode using driving transistors formed in pixels to allow the organic light emitting diode to generate light.

[0004] Such a conventional organic light emitting display includes a data driver that supplies data signals to data lines, a scan driver that sequentially supplies scan signals to scan lines, an emission driver that supplies light emitting signals to light emitting control lines, and a pixel unit that includes a plurality of pixels coupled to the data lines, the scan lines, and the light emitting lines.

[0005] The pixels included in the pixel unit are selected, when the scan signals are supplied to the scan lines, to be supplied with the data signals from the data lines. The pixels supplied with the data signals illuminate, while generating light having a predetermined brightness corresponding to the data signals. Herein, the light emitting time of the pixels is controlled by the light emitting control signals supplied from the light emitting control lines. In general, the light emitting control signals are supplied while the data signals are supplied to the pixels, to set the pixels as a non-light emitting state.

[0006] Herein, in order for the organic light emitting display to be stably driven, the light emitting control signals should be supplied for an initial driving period before the pixels of the pixel unit normally emits light to set the pixels as a non-light emitting state. However, an output of a conventional emission driver is set as an unknown state during an initial driving period thereof. In other words, during the initial driving period, the light emitting control signals are supplied to some light emitting control lines, and the light emitting control signals are not supplied to the other light emitting control lines. Herein, light

emitting is generated in some pixels coupled to the light emitting control lines not supplied with the light emitting control signals, and a problem arises that quality is, accordingly, deteriorated.

5 **[0007]** EP 1763 003 A2 and US 2007/0046608 A1 show circuits for an emission control driver of an OLED display device. However, a problem of these circuits is that initial states of some internal nodes may not be defined to the effect that proper functioning of the circuits
10 may not be guaranteed under all circumstances.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

15 **[0008]** For these reasons the invention provides the organic light emitting display of claim 1. Preferred embodiments are subject of the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

20 **[0009]** The accompanying drawings, together with the specification illustrate exemplary embodiments, and, together with the description, serve to explain certain inventive principles.

[0010] FIG. 1 illustrates an organic light emitting display according to an embodiment;

25 **[0011]** FIG. 2 illustrates the emission driver of FIG. 1;

[0012] FIG. 3 is a waveform view showing a normal driving process of a stage of an emission driver;

30 **[0013]** FIG. 4 is a circuit view showing a stage of FIG. 2 in detail;

[0014] FIGS. 5a to 5d are circuit views showing an operation process of a stage by the waveform view of FIG. 3;

[0015] FIG. 6 is a waveform view showing an initial control signal supplied during an initial driving period; and

35 **[0016]** FIG. 7 is a circuit view showing an operation process of a stage by the waveform view of FIG. 6.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

40 **[0017]** Hereinafter, certain exemplary embodiments will be described with reference to the accompany drawings. Herein, when a first element is described as being coupled to a second element, the first element may be not only directed coupled to the second element but may
45 be also be indirectly coupled to the second element via a third element. Further, some of the elements that are not essential to the complete understanding of the invention are omitted for clarity. Also, like reference numerals generally refer to like elements throughout.

[0018] Hereinafter, embodiments which can carried out by those skilled in the art, will be described with reference to the accompanying FIGS. 1 to 7.

50 **[0019]** FIG. 1 illustrates an organic light emitting display according to one embodiment. In FIG. 1, although a scan driver 10 and an emission driver 30 are illustrated as separated from each other, the emission driver 30 may be included in the scan driver 10.

[0020] Referring to FIG. 1, the organic light emitting display includes: a pixel unit 40 including a plurality of pixels coupled to scan lines S1 to Sn, data lines D1 to Dm, and light emitting control lines E1 to En, a scan driver 10 that drives the scan lines S1 to Sn, a data driver 20 that drives the data lines D1 to Dm, an emission driver 30 that drives the light emitting control lines E1 to En, and a timing controller 60 that controls the scan driver 10, the data driver 20, and the emission driver 30.

[0021] The scan driver 10 sequentially supplies scan signals to the scan lines S1 to Sn, while being controlled by the timing controller 60. As a result, pixels 50 coupled to the scan lines S1 to Sn are sequentially selected.

[0022] The data driver 20 supplies data signals to the data lines D1 to Dm, while being controlled by the timing controller 60. The data driver 20 supplies the data signals to the data lines D1 to Dm while the scan signals are supplied. As a result, the data signals are supplied to the selected pixels 50 by the scan signals, and the pixels 50 each are charged with voltage corresponding to the data signals supplied thereto.

[0023] The emission driver 30 sequentially supplies light emitting control signals to the light emitting control lines E1 to En, while being controlled by the timing controller 60. For example, the emission driver 30 supplies the light emitting control signals so that the pixels 50 do not emit light during the period that the data signals are being supplied to each pixel 50. The emission driver 30 supplies the light emitting control signals to the light emitting control lines E1 to En during an initial driving period that power is supplied to the emission driver 30, to set the pixels 50 to a non-light-emitting state. If the pixels are set to a non-light-emitting state during the initial driving period, the deterioration of display quality due to abnormal light emitting can be prevented.

[0024] The pixel unit 40 includes a plurality of pixels 50 arranged in a matrix. The respective pixels 50 supply current corresponding to the data signals to a second power supply ELVSS from a first power supply ELVDD via an organic light emitting diode (not shown) to generate light having a brightness corresponding to the current. Pixels 50 are set as a non-light-emitting state when the light emitting signals are supplied thereto.

[0025] FIG. 2 is a schematic view showing the emission driver of FIG. 1.

[0026] Referring to FIG. 2, an emission driver 30 of the present invention includes stages 321, 322, ... coupled to respective light emitting control signals E1 to En. The respective stages 321, 322, ... are driven by two clock signals.

[0027] Timing controller 60 supplies four clock signals Clk1, Clk1b, Clk2, and Clk2b and starting signals SP to the emission driver 30. The first clock signal Clk1 and the inverted first clock signal Clk1b are supplied to odd stages 321, 323, 325 ..., and the second clock signal Clk2 and the inverted second clock signal Clk2b are supplied to even stages 322, 324, The starting signals SP are supplied to the first stage 321 and the second stage 322.

Herein, as shown in FIG. 3, the first clock signal Clk1 and the second clock signal Clk2 have the same period and are supplied to be overlapped by 1/4 periods at their high levels (or low levels).

[0028] An output of an i^{th} (i is a natural number) stage 32i is supplied to an $i+2^{\text{nd}}$ stage 32i+2 via an inverter IN. For example, the output of a first stage 321 is supplied to the third stage 323 via the inverter IN, and the output of the third stage 323 is supplied to the fifth stage 325 via the inverter IN. Accordingly, the odd stages 323, 325, ... are supplied with the output of odd stages. The output of the second stage 322 is supplied to the fourth stage 324 via the inverter IN, and the output of the fourth stage 324 is supplied to the sixth stage via the inverter IN. Accordingly, the even stages 324, ... are supplied with the output of even stages.

[0029] FIG. 4 illustrates an embodiment of a circuit for the respective stages. For convenience, a first stage 321 coupled to a first clock signal Clk1 and an inverted first clock signal Clk1b will be described in FIG. 4.

[0030] Referring to FIG. 4, a first stage 321 includes an input unit 34 that supplies any of a first signal and a second signal according to clock signals Clk1 and Clk1b and starting signals SP, an output unit 36 that controls whether light emitting control signals are generated or not according to the first signal or the second signal supplied from the input unit 34, and an initial driving controller 38 that controls the light emitting signals to be supplyable during an initial driving period.

[0031] The input unit 34 includes a first transistor M1 coupled to a third power supply VDD and a first input terminal, a third transistor M3 coupled to the first input terminal and a second input terminal, a second transistor M2 coupled to the third transistor M3 and a third input terminal, and a first capacitor C1 coupled between a gate electrode of the second transistor M2 and a first electrode (source electrode) thereof.

[0032] A first electrode of the first transistor M1 is coupled to the third power supply VDD and a gate electrode thereof is coupled to the first input terminal. Herein, the first input terminal is a terminal supplied with the first clock signal clk1. A second electrode (drain electrode) of the first transistor M1 is coupled to a first node N1. The first transistor M1 is turned on when the first clock signal Clk1 is at a low level, to supply voltage of the third power supply VDD to the first node N1.

[0033] A first electrode of the second transistor M2 is coupled to the first node N1, and a second electrode thereof is coupled to the third input terminal. Herein, the third input terminal is supplied with the inverted first clock signal clk1b. A gate electrode of the second transistor M2 is coupled to a first electrode of the third transistor M3. As described above, the second transistor M2 is turned on or turned off according to the voltage charged in the first capacitor C1.

[0034] The first electrode of the third transistor M3 is coupled to the gate electrode of the second transistor M2, and a second electrode thereof is coupled to the

second input terminal. The second input terminal is supplied with the starting signals SP or light emitting control signals inverted from a previous stage. A gate electrode of the third transistor M3 is coupled to the first input terminal. The third transistor M3 is turned on when the first clock signal Clk1 is at a low level.

[0035] The first capacitor C1 is coupled to the gate electrode of the second transistor M2 and the first electrode thereof. The first capacitor C1 is charged with voltage, which can turn on the second transistor M2 when the third transistor M3 is turned on and the starting signals SP are supplied to the second input terminal. It is not charged with voltage otherwise.

[0036] The output unit 36 outputs the light emitting signals (high level) in the case where the second signals (low level) are supplied to the first node N1, and it does not output the light emitting signals in other case (that is, when the first signal (high level) is supplied to the first node N1).

[0037] To this end, the output unit 36 includes a fourth transistor M4 coupled to the third power supply VDD, a sixth transistor M6, an eighth transistor M8, a fifth transistor M5 coupled to a fourth power supply VSS, a seventh transistor M7, a ninth transistor M9, and a second capacitor C2 coupled between a gate electrode of the ninth transistor M9 and a first electrode thereof.

[0038] A first electrode of the fourth transistor M4 is coupled to the third power supply VDD, and a second electrode thereof is coupled to the second node N2. A gate electrode of the fourth transistor M4 is coupled to the first node N1.

[0039] A first electrode of the fifth transistor M5 is coupled to the second node N2, and a second electrode thereof is coupled to the fourth power supply VSS. A gate electrode of the fifth transistor M5 is coupled to the first input terminal.

[0040] A first electrode of the sixth transistor M6 is coupled to the third power supply VDD, and a second electrode thereof is coupled to a first electrode of the seventh transistor M7. A gate electrode of the sixth transistor M6 is coupled to the second node N2.

[0041] The first electrode of the seventh transistor M7 is coupled to the second electrode of the sixth transistor M6, and a second electrode thereof is coupled to the fourth power supply VSS. A gate electrode of the seventh transistor M7 is coupled to the first node N1.

[0042] A first electrode of the eighth transistor M8 is coupled to the third power supply VDD, and a second electrode thereof is coupled to the light emitting control line E1. A gate electrode of the eighth transistor M8 is coupled to the second electrode of the sixth transistor M6.

[0043] A first electrode of the ninth transistor M9 is coupled to the light emitting control line E1, and a second electrode thereof is coupled to the fourth power supply VSS. The gate electrode of the ninth transistor M9 is coupled to the second node N2.

[0044] The second capacitor C2 is coupled between the gate electrode of the ninth transistor M9 and the first

electrode thereof. The second capacitor C2 controls a turn-on and a turn-off of the ninth transistor M9.

[0045] The initial driving controller 38 controls the light emitting control signals to be supplied to the light emitting control line E1 during an initial driving period. The initial driving controller 38 is driven during the initial driving period and not driven during a normal driving period that the pixels 50 are driven. The initial driving controller 38 includes a tenth transistor M10 and an eleventh transistor M11.

[0046] A first electrode of the tenth transistor M10 is coupled to the third power supply VDD, and a second electrode thereof is coupled to the gate electrode of the second transistor M2. A gate electrode of the tenth transistor M10 is coupled to a fourth input terminal input with initial control signals RS (active low level signal). The tenth transistor M10 is turned on when the initial control signals RS are supplied, and is turned off when the initial control signals RS are not supplied. In this embodiment, the input unit 34, the output unit 36, and the initial driving controller 38 use only the same type of transistors, pMOS transistors. In other embodiments other transistors may be used, or multiple types may be used.

[0047] A first electrode of the eleventh transistor M11 is coupled to the first node N1, and a second electrode thereof is coupled to the fourth power supply VSS. A gate electrode of the eleventh transistor M11 is coupled to the fourth input terminal. The eleventh transistor M11 is turned on when the initial control signals are supplied, and is turned off when the initial control signals are not supplied.

[0048] FIG. 3 is a waveform view showing a normal driving process of a stage during a normal driving period. During the normal driving period, the tenth transistor M10 and the eleventh transistor M11 maintain in a turn-off state.

[0049] With reference to FIGS. 3 and 4, first a clock signal Clk1 is set as a low level and an inverted first clock signal Clkb1 is set as a high level during a first period T1. In this case, as shown in FIG. 5a, a first transistor M1 and a third transistor M3 are turned on by the first clock signal Clk1.

[0050] Because the first transistor M1 is on, the voltage of a first node N1 rises to the voltage of a third power supply VDD. Accordingly, the voltage of a first signal (high level) is applied to the first node N1. Because the third transistor M3 is turned on, the gate electrode voltage of the second transistor M2 falls to a low level because of the starting signal SP supplied during the first period T1. In this case, the first capacitor C1 is charged with a voltage of a difference between the voltage of the third power supply VDD applied to the first node N1 and the low level voltage applied to a gate electrode of a second transistor M2.

[0051] Because the second transistor M2 is turned on, the voltage of the inverted first clock signal Clkb1 is supplied to the first node N1. Herein, a voltage level of the inverted first clock signal Clkb1 is set as a high level. For

example, the high level voltage of the inverted first clock signal Clk1b may be set to be the same as the voltage of the third power supply VDD. Then, even when the first transistor M1 and the second transistor M2 are simultaneously turned on, the voltage of the first node N1 can be stably maintained at the same high level.

[0052] When the voltage of the first signal is applied to the first node N1, a fourth transistor M4 and a seventh transistor M7 are turned off. Meanwhile, although the first clock signal Clk1 maintains a low level, a fifth transistor M5 maintains a turn-off state because of the voltage stored in a second capacitor C2. (The charging process of voltage in the second capacitor C2 will be described later.) The second capacitor C2 is charged with voltage of more than $VDD - (VSS + |V_{th5}|)$. Therefore, voltage of a first electrode of the fifth transistor M5 is less than $|V_{th5}|$ higher than the voltage of the first clock signal Clk1 and accordingly, the fifth transistor M5 maintains a turn-off state.

[0053] The sixth transistor M6 is turned on by voltage applied to a second node N2 (that is, voltage because of the second capacitor C2), as shown in FIG. 5b. When the sixth transistor M6 is turned on, the voltage of the third power supply VDD is supplied to the gate electrode of the eighth transistor M8. Accordingly, the eighth transistor M8 is off.

[0054] The ninth transistor M9 maintains a turn-on state because of the voltage charged in the second capacitor C2 and accordingly, the light emitting control line E maintains output voltage of a fourth power supply VSS. Herein, the second capacitor C2 is charged with voltage of more than $VDD - (VSS + |V_{th5}|)$ so that voltage of the light emitting control line E is pulled-down to the voltage of the fourth power supply VSS.

[0055] Thereafter, during a second period T2, the first clock signal Clk1 is set as a high level and the inverted clock signal Clk1b is set as a low level.

[0056] Because the first clock signal Clk1 is set as a high level, the first transistor M1, the third transistor M3, and the fifth transistor M5 are turned off, as shown in FIG. 5c. The second transistor M2 is still on because of the voltage charged in the first capacitor C1 during a previous period. Because the second transistor M2 is on, the voltage of the first node N1 falls to a level of the inverted first clock signal Clk1b (for example, the fourth power supply VSS), that is, a low level.

[0057] Because the voltage of a second signal (low level) is applied to the first node N1, the fourth transistor M4 and the seventh transistor M7 are turned on. Because the fourth transistor M4 is turned on, the voltage of the second node N2 rises to the voltage of the third power supply VDD. As a result, the sixth transistor M6 and the ninth transistor M9 are turned off. Because the seventh transistor M7 is on, the voltage of the gate electrode of the eighth transistor M8 falls to the voltage of the fourth power supply VSS so that the eighth transistor M8 is turned on. Because the eighth transistor M8 is on, the voltage of the third power supply VDD is supplied to the

light emitting control line E1. Accordingly, during the second period T2, the light emitting control signals are supplied to the light emitting control line E1. During the second period T2, the voltage of the third power supply VDD is supplied across the second capacitor C2 so that the second capacitor C2 is not charged with voltage.

[0058] During a third period T3, the first clock signal Clk1 is set as a low level, and the inverted first clock signal Clk1b is set as a high level.

[0059] Accordingly, during the third period T3, the first transistor M1, the third transistor M3, and the fifth transistor M5 are turned on by the first clock signal Clk1, as shown in FIG. 5d. Because the first transistor M1 is turned on, the voltage of the first node N1 rises to the voltage of the third power supply VDD. In other words, the voltage of the first signal (high level) is applied to the first node N1.

[0060] Because the third transistor M3 is turned on, and the starting signals SP maintains voltage at high level (for example, the voltage of the third power supply VDD), the second transistor M2 is off. The voltage at both terminals of the first capacitor C1 are the voltage of the third power supply VDD so that the first capacitor C1 is not charged. In this embodiment, the first capacitor C1 is charged with a predetermined voltage only in the period where the starting signals SP are set as a low level, and is not charged with voltage otherwise.

[0061] The second transistor M2 is turned off, the voltage of the first signal is applied to the first node N1, and the inverted first clock signal Clk1b maintains a high level. Therefore, although the first node N1 maintains the voltage of the first signal, current is prevented from flowing via the second transistor M2 and power consumption is therefore reduced.

[0062] When the fifth transistor M5 is on, the voltage of the second node N2 is pulled down to voltage of $VSS + |V_{th5}|$. ($|V_{th5}|$ is threshold voltage of the fifth transistor M5). After the voltage of the second node N2 is pulled-down to the voltage of $VSS + |V_{th5}|$, the fifth transistor M5 is switched into a turn-off state. Accordingly, the second capacitor C2 is charged with the voltage of more than $VDD - (VSS + |V_{th5}|)$ because of the voltage of $VSS + |V_{th5}|$ applied to the second node N2 and the third power VDD applied to the light emitting control line E1.

[0063] The fourth transistor M4 and the seventh transistor M7 are turned off by the voltage of the first signal applied to the first node N1, and the sixth transistor M6 and the ninth transistor M9 are turned on by the voltage charged in the second capacitor C2.

[0064] Because the sixth transistor is turned on, the voltage of the third power supply VDD is applied to the gate electrode of the eighth transistor M8 so that the eighth transistor M8 is turned off. Because the ninth transistor M9 is on, the voltage of the light emitting control line D1, maintaining a high state during the second period T2, falls to the voltage of the fourth power supply VSS. At this time, the fifth transistor is set as a turn-off state (accordingly, N2 is in a floating state) so that the voltage charged in the second capacitor C2 is maintained and

accordingly, the voltage of the light emitting control line E1 is pulled down to the voltage of the fourth power supply VSS.

[0065] Thereafter, the voltage of only the first signal (high level) is applied to the first node N1 before the starting signals SP are supplied again. In other words, the first capacitor C1 is not charged with voltage before the starting signals SP are supplied again, and accordingly the second transistor M2 maintains a turn-off state. As a result, the ninth transistor M9 supplies the voltage of the fourth power supply VSS to the light emitting control line E1 during the remainder of the frame period, because of the voltage charged in the second capacitor C2.

[0066] FIG. 6 illustrates an initial control signal supplied during an initial driving period.

[0067] Referring to FIG. 6, an initial control signal RS (low level) is supplied during an initial driving period and the initial control signal RS is not supplied during a normal driving period.

[0068] Because the initial control signal RS is supplied during the initial driving period, the tenth transistor M10 and the eleventh transistor M11 are turned on, as shown in FIG. 7. Because the tenth transistor M10 is on, the voltage of a third power supply VDD is supplied to the gate electrode of the second transistor M2 and accordingly, the second transistor M2 is turned off.

[0069] Because the eleventh transistor M11 is on, the voltage of the fourth power supply VSS is supplied to the first node N1. In other words, a second signal is supplied to the first node N1. Because the second signal is supplied to the first node N1, the fourth transistor M4 and the seventh transistor M7 are turned on.

[0070] Because the fourth transistor M4 is turned on, the voltage of the third power supply VDD is supplied to a second node N2 so that a sixth transistor M6 is turned off. Because the seventh transistor M7 is turned on, the voltage of the fourth power supply VSS is supplied to the gate electrode of the eighth transistor M8 so that the eighth transistor M8 is turned on. Because the eighth transistor M8 is turned on, the voltage of the third power supply VDD is supplied to the light emitting control line E1.

[0071] As described above, during the initial driving period, the initial driving controller 38 is controlled to supply the light emitting control signals to the all light emitting control lines E1 to En. Then, light emitting of the pixels 50 during the initial driving period can be prevented, making it possible to improve display quality.

Claims

1. An organic light emitting display, comprising:

a pixel unit (40) including a plurality of pixels (50) positioned adjacent to intersection portions of light emitting control lines (E1, E2, En), scan lines (S1, S2, Sn), and data lines (D1, D2, Dm);
a scan driver (10) configured to drive the scan

lines (S1, S2, Sn);

a data driver (20) configured to drive the data lines (D1, D2, Dm);

an emission driver (30); and

a controller adapted to drive the emission driver (30) in an initial driving period and a normal driving period subsequent to the initial driving period, wherein the emission driver (30) comprises:

a plurality of stages (321, 322, 323, 324, 325), each of which being coupled to one of a plurality of light emitting control lines (E1, E2, En) and comprising:

an input unit (34) configured to supply one of a first signal and a second signal to a first node (N1); and

an output unit (36) configured to output a voltage at a first level when the second signal is input to the first node (N1) and configured to output a voltage at a second level when the first signal is input to the first node (N1),

wherein the input unit (34) comprises a first transistor (M1) coupled between a first power supply (VDD) adapted to provide a first power supply voltage and a first node (N1), wherein the first transistor (M1) has a gate electrode coupled to a first input terminal (1);

a second transistor (M2) coupled between the first node (N1) and a third input terminal (3);

a first capacitor (C1) coupled between a gate electrode of the second transistor (M2) and the first node (N1); and
a third transistor (M3) coupled between the gate electrode of the second transistor (M2) and a second input terminal (2) and having a gate electrode coupled to the first input terminal (1), and
wherein the output unit (36) comprises

a fourth transistor (M4), a sixth transistor (M6) and an eighth transistor (M8) each coupled to the first power supply (VDD);

a fifth transistor (M5) coupled between a second power supply (VSS) and the fourth transistor (M4), the second power supply being adapted to provide a second power supply voltage lower than the first power supply voltage;

a seventh transistor (M7) coupled between the second power supply (VSS) and the sixth transistor (M6);

a ninth transistor (M9) coupled between the second power supply (VSS) and the eighth transistor (M8); and

a second capacitor (C2) coupled between a gate electrode of the ninth transistor (M9) and a common node between the ninth transistor (M9) and the eighth transistor (M8),

the emission driver being **characterised by** an initial driving controller (38) configured to supply the second signal to the first node (N1) during the initial driving period and comprising:

a tenth transistor (M10) coupled between a gate electrode of the second transistor (M2) and the first power supply (VDD) and having a gate electrode coupled to a fourth input terminal (4); and

an eleventh transistor (M11) coupled between the first node (N1) and the second power supply (VSS) and having a gate electrode coupled to the fourth input terminal (4),

wherein the controller is further adapted to supply the fourth input terminal (4) with an initial control signal during the initial driving period and to thereby turn on the tenth transistor (M10) and the eleventh transistor (M11).

2. The organic light emitting display as claimed in claim 1, wherein the first level is a voltage level higher than the voltage of the second level.
3. The organic light emitting display as claimed in one of the preceding claims, wherein the first input terminal (1) is supplied with a first clock signal (clk1), and the third input terminal (3) is supplied with an inverted first clock signal (clk1b).
4. The organic light emitting display according to claim 3, wherein the second input terminal (2) is supplied with an output signal of a previous stage or a starting signal (sp).
5. The organic light emitting display according to one of the preceding claims, wherein the initial driving controller (38) is adapted to supply the voltage of the second power supply (4) to the first node (N1) during the initial driving period.
6. The organic light emitting display according to one of the preceding claims, wherein the each stage (321, 322, 323, 324, 325) comprises only a single type of transistor.

Patentansprüche

1. Organische lichtemittierende Anzeige, aufweisend:

5 eine Pixeleinheit (40), die eine Vielzahl von Pixeln (50) aufweist, die benachbart zu Schnittabschnitten von Lichtemissionskontrollleitungen (E1, E2, En), Ansteuerleitungen (S1, S2, Sn) und Datenleitungen (D1, D2, Dm) angeordnet sind;
 10 einen Ansteuertrieb (10), der zur Ansteuerung der Ansteuerleitungen (S1, S2, Sn) konfiguriert ist;
 15 einen Datentreiber (20), der zur Ansteuerung der Datenleitungen (D1, D2, Dm) konfiguriert ist;

einen Emissionstreiber (30); und
 eine Steuerung, die zur Ansteuerung des Emissionstreibers (30) in einer Anfangsansteuerperiode und einer an die Anfangsansteuerperiode anschließenden normalen Ansteuerperiode ausgebildet ist, wobei der Emissionstreiber (30) aufweist:

eine Vielzahl von Stufen (321, 322, 323, 324, 325), von denen jede mit einer aus einer Vielzahl von Lichtemissionskontrollleitungen (E1, E2, En) gekoppelt ist und Folgendes aufweist:

30 eine Eingabeeinheit (34), die zum Anlegen eines ersten Signals oder eines zweiten Signals an einen ersten Knoten (N1) konfiguriert ist; und
 eine Ausgabeeinheit (36), die konfiguriert ist, eine Spannung mit einem ersten Pegel auszugeben, wenn das zweite Signal in den ersten Knoten (N1) eingegeben wird, und konfiguriert ist, eine Spannung mit einem zweiten Pegel auszugeben, wenn das erste Signal in den ersten Knoten (N1) eingegeben wird,
 40 wobei die Eingabeeinheit (34) einen ersten Transistor (M1) aufweist, der zwischen eine erste Spannungsversorgung (VDD), die zur Bereitstellung einer ersten Versorgungsspannung ausgebildet ist, und einen ersten Knoten (N1) gekoppelt ist, wobei der erste Transistor (M1) eine Gate-Elektrode aufweist, die mit einem ersten Eingangsanschluss (1) gekoppelt ist;
 45 einen zweiten Transistor (M2), der zwischen den ersten Knoten (N1) und einen dritten Eingangsanschluss (3) gekoppelt ist;
 einen ersten Kondensator (C1), der zwischen eine Gate-Elektrode des zweiten Transistors (m2) und den ersten Knoten (N1) gekoppelt ist; und
 50 einen dritten Transistor (M3), der zwischen

die Gate-Elektrode des zweiten Transistors (M2) und einen zweiten Eingangsanschluss (2) gekoppelt ist und eine Gate-Elektrode aufweist, die mit dem ersten Eingangsanschluss (1) gekoppelt ist, und
 wobei die Ausgangseinheit (36) einen vierten Transistor (M4), einen sechsten Transistor (m6) und einen achten Transistor (m8) aufweist, die jeweils mit der ersten Spannungsversorgung (VDD) gekoppelt sind;
 einen fünften Transistor (M5), der zwischen eine zweite Spannungsversorgung (VSS) und den vierten Transistor (M4) gekoppelt ist, wobei die zweite Spannungsversorgung zur Bereitstellung einer zweiten Versorgungsspannung ausgebildet ist, die niedriger als die erste Versorgungsspannung ist;
 einen siebten Transistor (M7), der zwischen die zweite Spannungsversorgung (VSS) und den sechsten Transistor (M6) gekoppelt ist;
 einen neunten Transistor (M9), der zwischen die zweite Spannungsversorgung (VSS) und den achten Transistor (M8) gekoppelt ist; und
 einen zweiten Kondensator (C2), der zwischen eine Gate-Elektrode des neunten Transistors (M9) und einen gemeinsamen Knotenpunkt zwischen dem neunten Transistor (M9) und dem achten Transistor (M8) gekoppelt ist,
 wobei der Emissionstreiber durch eine Steuerung (38) einer Anfangsansteuerung **gekennzeichnet** ist, die konfiguriert ist, während der Anfangsansteuerperiode das zweite Signal an den ersten Knoten (N1) anzulegen, und Folgendes aufweist:

einen zehnten Transistor (M10), der zwischen eine Gate-Elektrode des zweiten Transistors (M2) und die erste Spannungsversorgung (VDD) gekoppelt ist und eine Gate-Elektrode aufweist, die mit einem vierten Eingangsanschluss (4) gekoppelt ist; und
 einen elften Transistor (M11), der zwischen den ersten Knoten (N1) und die zweite Spannungsversorgung (VSS) gekoppelt ist und eine Gate-Elektrode aufweist, die mit dem vierten Eingangsanschluss (4) gekoppelt ist,
 wobei die Steuerung weiterhin ausgebildet ist, während der Anfangsansteuerperiode den vierten Eingangsanschluss (4) mit einem Anfangssteuersignal zu versorgen, so dass der zehnte Transistor (M10) und der elfte Transistor (M11) eingeschaltet werden.

2. Organische lichtemittierende Anzeige nach Anspruch 1, wobei der erste Pegel ein Spannungspegel ist, der höher als die Spannung des zweiten Pegels ist.
3. Organische lichtemittierende Anzeige nach einem der vorhergehenden Ansprüche, wobei der erste Eingangsanschluss (1) mit einem ersten Taktsignal (clk1) versorgt wird und der dritte Eingangsanschluss (3) mit einem invertierten ersten Taktsignal (clk1b) versorgt wird.
4. Organische lichtemittierende Anzeige nach Anspruch 3, wobei der zweite Eingangsanschluss (2) mit einem Ausgangssignal einer vorhergehenden Stufe oder einem Startsignal (sp) versorgt wird.
5. Organische lichtemittierende Anzeige nach einem der vorhergehenden Ansprüche, wobei die Steuerung (38) der Anfangsansteuerung ausgebildet ist, während der Anfangsansteuerperiode den ersten Knoten (N1) mit der Spannung der zweiten Spannungsversorgung (4) zu versorgen.
6. Organische lichtemittierende Anzeige nach einem der vorhergehenden Ansprüche, wobei jede Stufe (321, 322, 323, 324, 325) nur einen einzigen Transistortyp aufweist.

Revendications

1. Dispositif d'affichage à émission de lumière organique, comprenant :
 - une unité de pixels (40) comprenant une pluralité de pixels (50) positionnés au voisinage de parties d'intersection de lignes de commande d'émission de lumière (E1, E2, En), de lignes de balayage (S1, S2, Sn) et de lignes de données (D1, D2, Dm) ;
 - un dispositif d'attaque de balayage (10) configuré de façon à attaquer les lignes de balayage (S1, S2, Sn) ;
 - un dispositif d'attaque de données (20) configuré de façon à attaquer les lignes de données (D1, D2, Dm) ;
 - un dispositif d'attaque d'émission (30) ; et
 - un dispositif de commande adapté de façon à attaquer le dispositif d'attaque d'émission (30) lors d'une période d'attaque initiale et d'une période d'attaque normale suivant la période d'attaque initiale, le dispositif d'attaque d'émission (30) comprenant :
 - une pluralité d'étages (321, 322, 323, 324, 325), chacun d'entre eux étant couplé à l'une d'une pluralité de lignes de commande

d'émission de lumière (E1, E2, En) et comprenant :

une unité d'entrée (34) configurée de façon à délivrer l'un d'un premier signal et d'un deuxième signal à un premier noeud (N1) ; et
 une unité de sortie (36) configurée de façon à délivrer en sortie une tension à un premier niveau lorsque le deuxième signal est entré sur le premier noeud (N1) et configurée de façon à délivrer en sortie une tension à un deuxième niveau lorsque le premier signal est entré sur le premier noeud (N1),
 l'unité d'entrée (34) comprenant un premier transistor (M1) couplé entre une première alimentation (VDD) adaptée de façon à délivrer une première tension d'alimentation et un premier noeud (N1), le premier transistor (M1) comportant une électrode de grille couplée à une première borne d'entrée (1) ;
 un deuxième transistor (M2) couplé entre le premier noeud (N1) et une troisième borne d'entrée (3) ;
 un premier condensateur (C1) couplé entre une électrode de grille du deuxième transistor (M2) et le premier noeud (N1) ; et
 un troisième transistor (M3) couplé entre l'électrode de grille du deuxième transistor (M2) et une deuxième borne d'entrée (2) et comportant une électrode de grille couplée à la première borne d'entrée (1), et
 l'unité de sortie (36) comprenant un quatrième transistor (M4), un sixième transistor (M6) et un huitième transistor (M8) chacun couplé à la première alimentation (VDD) ;
 un cinquième transistor (M5) couplé entre une deuxième alimentation (VSS) et le quatrième transistor (M4), la deuxième alimentation étant adaptée de façon à délivrer une deuxième tension d'alimentation inférieure à la première tension d'alimentation ;
 un septième transistor (M7) couplé entre la deuxième alimentation (VSS) et le sixième transistor (M6) ;
 un neuvième transistor (M9) couplé entre la deuxième alimentation (VSS) et le huitième transistor (M8) ; et
 un deuxième condensateur (C2) couplé entre une électrode de grille du neuvième transistor (M9) et un noeud commun entre le neuvième transistor (M9)

et le huitième transistor (M8),

le dispositif d'attaque d'émission étant **caractérisé par** un dispositif de commande d'attaque initiale (38) configuré de façon à délivrer le deuxième signal au premier noeud (N1) durant la période d'attaque initiale, et comprenant :

un dixième transistor (M10) couplé entre une électrode de grille du deuxième transistor (M2) et la première alimentation (VDD), et comportant une électrode de grille couplée à une quatrième borne d'entrée (4) ; et
 un onzième transistor (M11) couplé entre le premier noeud (N1) et la deuxième alimentation (VSS), et comportant une électrode de grille couplée à la quatrième borne d'entrée (4),
 le dispositif de commande étant de plus adapté de façon à délivrer à la quatrième borne d'entrée (4) un signal de commande initial durant la période d'attaque initiale, et à rendre ainsi passants le dixième transistor (M10) et le onzième transistor (M11).

2. Dispositif d'affichage à émission de lumière organique selon la revendication 1, dans lequel le premier niveau est un niveau de tension supérieur à la tension du deuxième niveau.
3. Dispositif d'affichage à émission de lumière organique selon l'une des revendications précédentes, dans lequel il est délivré à la première borne d'entrée (1) un premier signal d'horloge (clk1), et il est délivré à la troisième borne d'entrée (3) un premier signal d'horloge inversé (clk1b).
4. Dispositif d'affichage à émission de lumière organique selon la revendication 3, dans lequel il est délivré à la deuxième borne d'entrée (2) un signal de sortie d'un étage précédent ou un signal de démarrage (sp).
5. Dispositif d'affichage à émission de lumière organique selon l'une des revendications précédentes, dans lequel le dispositif de commande d'attaque initiale (38) est adapté de façon à délivrer la tension de la deuxième alimentation (4) au premier noeud (N1) durant la période d'attaque initiale.
6. Dispositif d'affichage à émission de lumière organique selon l'une des revendications précédentes, dans lequel chaque étage (321, 322, 323, 324, 325) ne comprend qu'un seul type de transistor.

FIG. 1

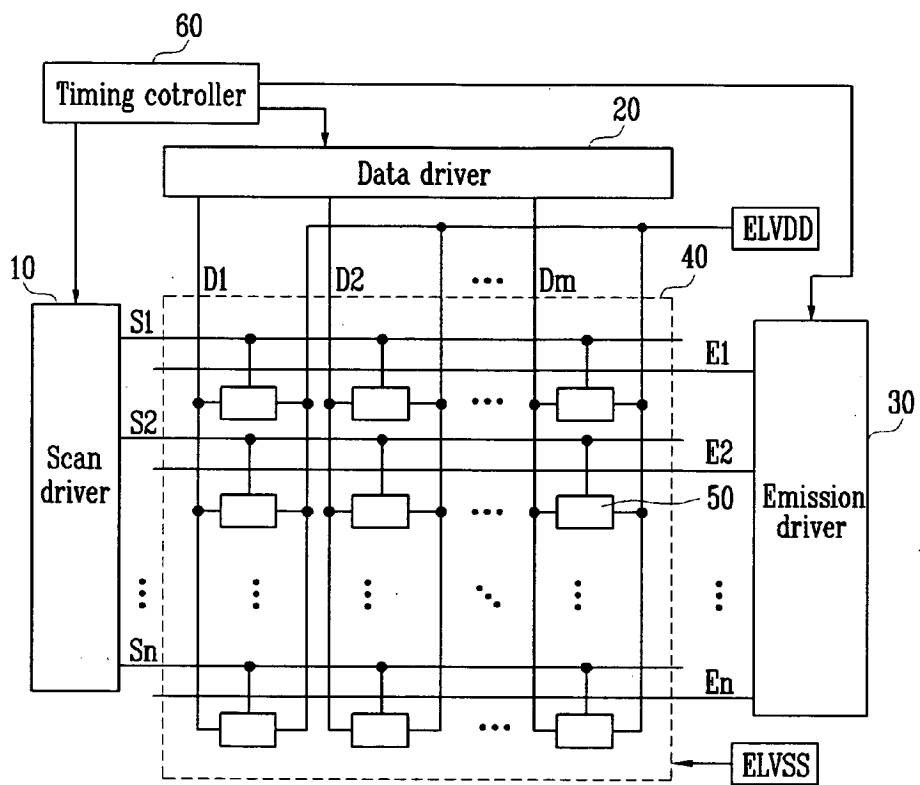


FIG. 3

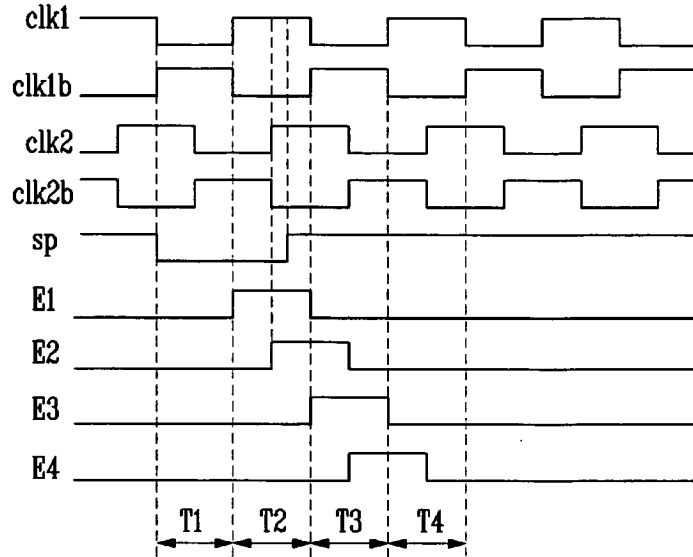


FIG. 4

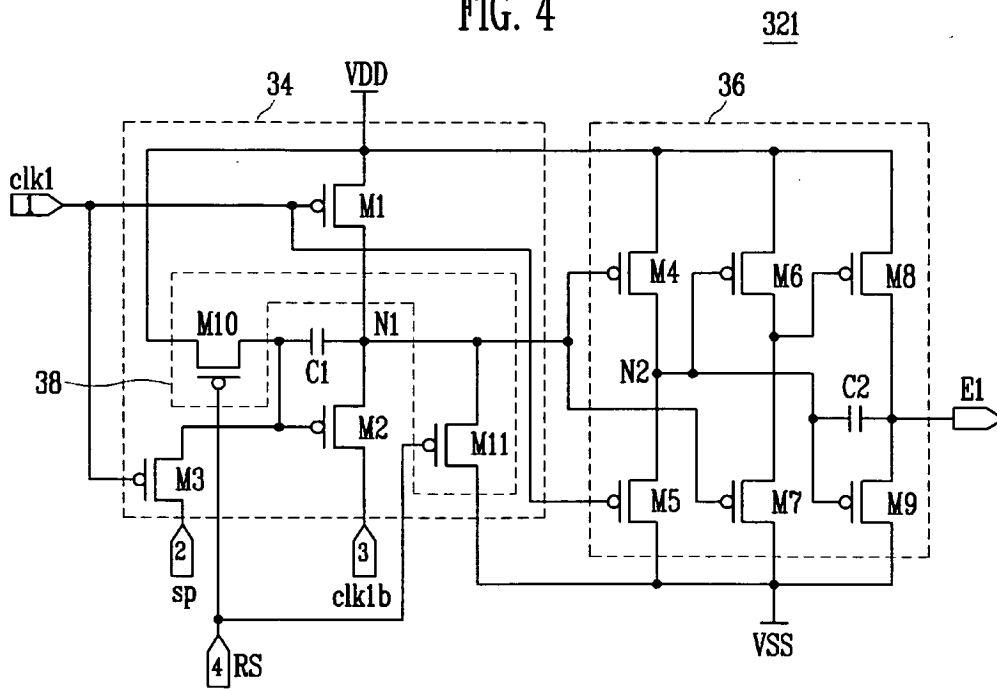


FIG. 5A

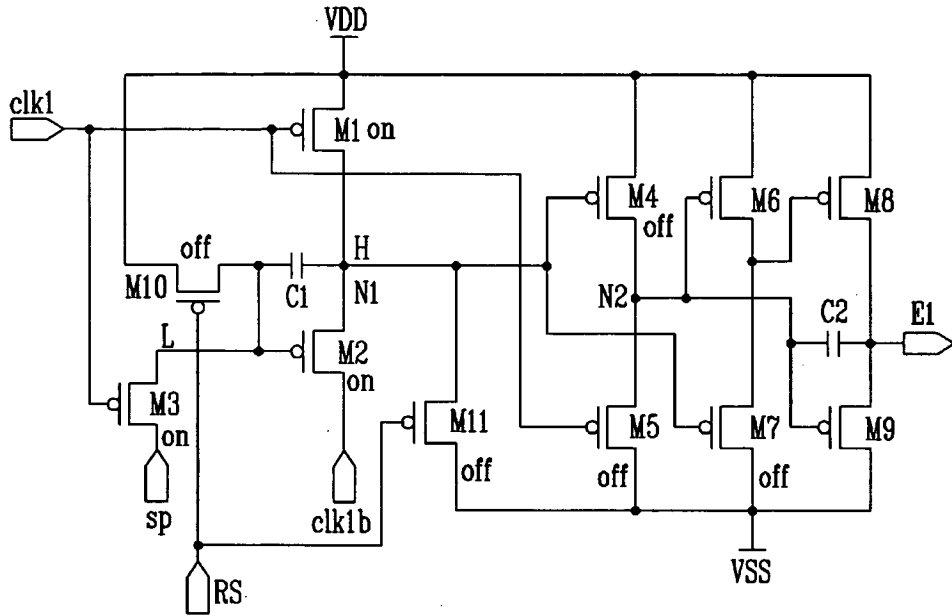


FIG. 5B

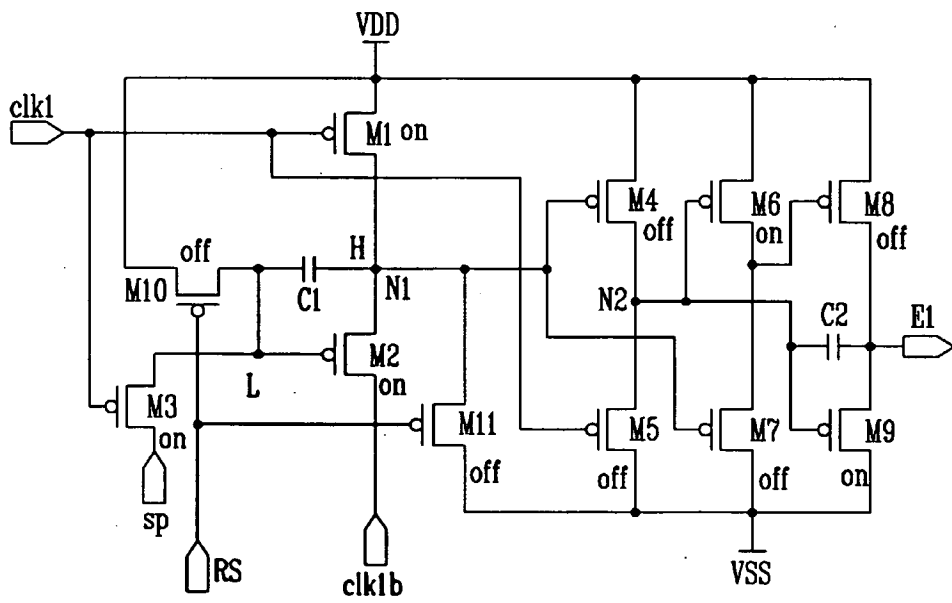


FIG. 5C

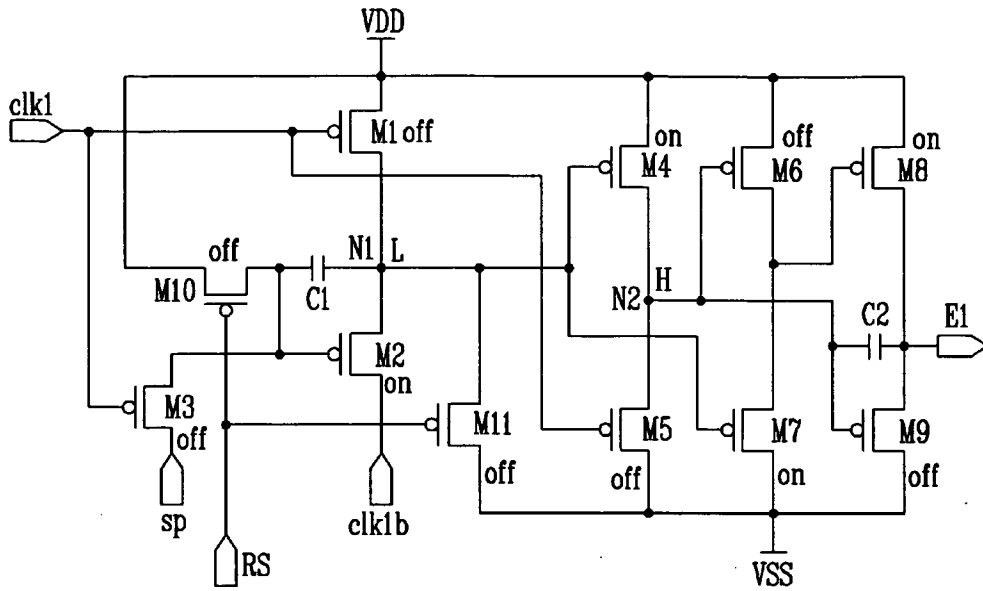


FIG. 5D

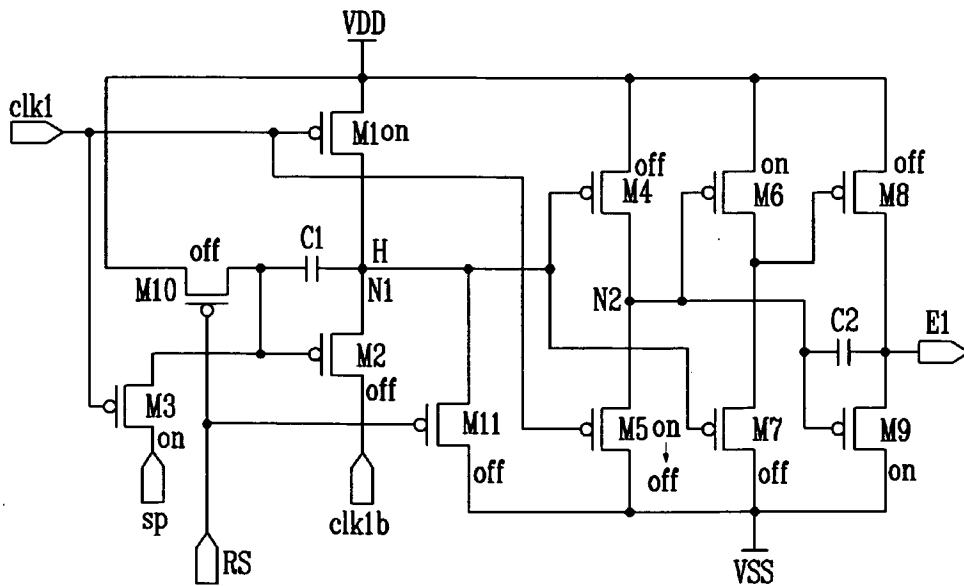


FIG. 6

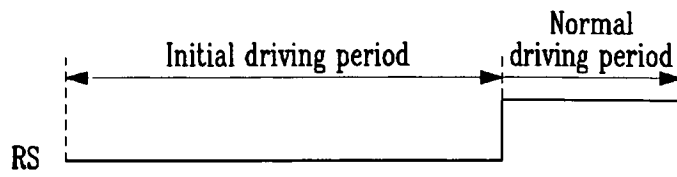
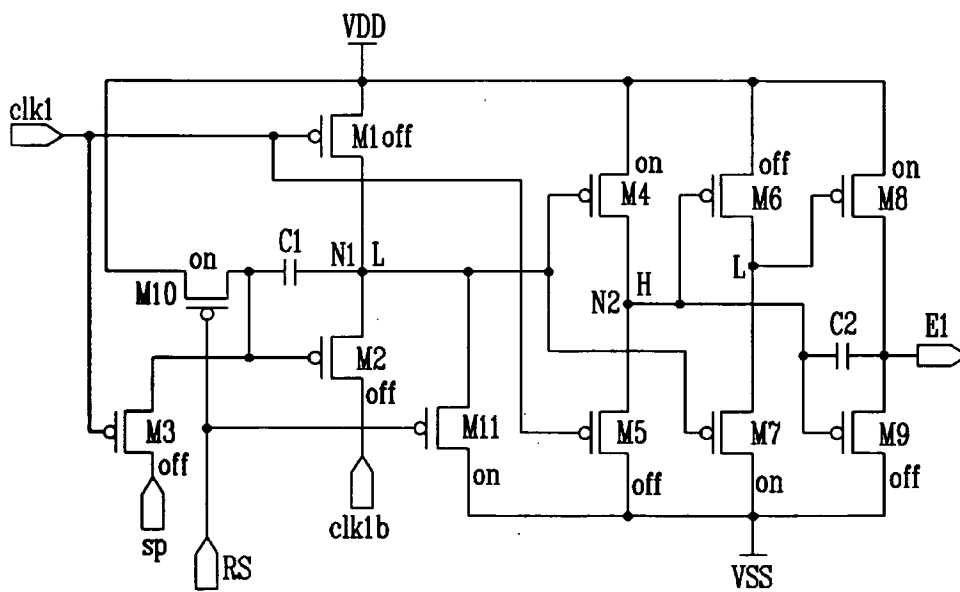


FIG. 7



REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	包含发射驱动器的有机发光显示器		
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摘要(译)

公开了一种防止有机发光二极管的不必要照射的有机发光显示器。显示器具有发射驱动器，其在初始化时段期间全局关闭所有像素，并且允许在其他时间期间的正常操作。

