

(19)



(11)

EP 2 067 135 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:

01.08.2018 Bulletin 2018/31

(51) Int Cl.:

G09G 3/3275 ^(2016.01) **G09G 3/3233** ^(2016.01)

(21) Application number: **07828894.1**

(86) International application number:

PCT/JP2007/069154

(22) Date of filing: **25.09.2007**

(87) International publication number:

WO 2008/038819 (03.04.2008 Gazette 2008/14)

(54) **DISPLAY DRIVING APPARATUS AND METHOD FOR DRIVING DISPLAY DRIVING APPARATUS,
AND DISPLAY APPARATUS AND METHOD FOR DRIVING DISPLAY APPARATUS**

ANZEIGENANTRIEBSVORRICHTUNG UND VERFAHREN ZUM ANTREIBEN EINER
ANZEIGENANTRIEBSVORRICHTUNG SOWIE ANZEIGEVORRICHTUNG UND VERFAHREN ZUM
ANTREIBEN EINER ANZEIGEVORRICHTUNG

APPAREIL DE COMMANDE D’AFFICHAGE ET PROCÉDÉ DE COMMANDE DE L’APPAREIL DE
COMMANDE D’AFFICHAGE, ET DISPOSITIF D’AFFICHAGE ET PROCÉDÉ DE COMMANDE DU
DISPOSITIF D’AFFICHAGE

(84) Designated Contracting States:
DE FR GB

(30) Priority: **25.09.2006 JP 2006258717**
26.03.2007 JP 2007078963

(43) Date of publication of application:
10.06.2009 Bulletin 2009/24

(73) Proprietor: **Solas OLED Ltd**
County Roscommon (IE)

(72) Inventor: **OGURA, Jun**
Hamura-shi
Tokyo 205-8555 (JP)

(74) Representative: **Peterreins Schley**
Patent- und Rechtsanwälte
Hermann-Sack-Strasse 3
80331 München (DE)

(56) References cited:
EP-A- 1 191 512 WO-A-2005/069267
WO-A-2006/000101 US-A1- 2004 239 596
US-A1- 2005 088 103 US-A1- 2005 269 958

EP 2 067 135 B1

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

Technical Field

5 **[0001]** The present invention relates to a display driving apparatus and a method for driving a display driving apparatus as well as a display apparatus and a method for driving a display apparatus.

Background Art

10 **[0002]** There exists a display apparatus that includes a display panel in which current driving-type light-emitting elements (e.g., organic electroluminescence (EL) element, inorganic EL elements, light-emitting diodes (LED)) are arranged in a matrix manner.

[0003] For example, Unexamined Japanese Patent Application KOKAI Publication No. H8-330600 discloses an active matrix-type driving display apparatus that is current-controlled by a voltage signal. This driving display apparatus is structured so that a current control thin film transistor and a switching thin film transistor are provided for each pixel. The current control thin film transistor flows current in an organic EL element when a voltage signal corresponding to image data is applied to a gate, and the switching thin film transistor turns ON or OFF the supply of the voltage signal to the gate of the current control thin film transistor. The driving display apparatus disclosed by Unexamined Japanese Patent Application KOKAI Publication No. H 8-330600 controls the brightness when an organic EL element emits light by controlling a voltage value of the voltage signal applied to the gate of the current control thin film transistor.

20 **[0004]** However, a threshold voltage of a transistor generally varies as time passes. Thus, in the case of the driving display apparatus of Unexamined Japanese Patent Application KOKAI Publication No. H 8-330600, a threshold voltage of a current control thin film transistor for supplying current to an organic EL element varies as time passes, which causes a variation in a value of current flowing in the organic EL element. As a result, there is a risk that brightness during the light emission by the organic EL element may vary.

25 **[0005]** Patent document US 2005/0088103 relates to a pixel driving circuit having the capability of taking into account the variation in threshold voltage of the transistor driving the light emitting device. More specifically, as can be seen in Fig. 1, the pixel driving circuit includes three switches 25, 26 and 27, a capacitor 24, an adder 23 and a digital to analog converter 22. Upon receiving video signal data, a driving voltage is generated by means of the digital to analog converter 22. The generated driving voltage is corrected by means of adder 23 thanks to the addition of a correction voltage stored in capacitor 24. More specifically, a precharge voltage is applied to the pixel driving circuit by means of switch 27; subsequently, a response voltage is read and stored by means of capacitor 24 and switch 25. The correction voltage consists in the current threshold voltage of the driving transistor. More specifically, by waiting until the correction voltage converges to the value of the threshold voltage, the correction circuit is capable of directly reading the actual threshold voltage of the driving transistor; add the actual threshold voltage to the driving voltage obtained through the digital to analogue converter 22 by means of adder 23; and apply the corrected driving voltage by means of switch 26.

Disclosure of Invention

40 **[0006]** The present invention has been made in view of the above disadvantage. It is an objective of the invention to provide a display apparatus in which a light-emitting element displays an image with an appropriate gradation level even when variation is caused in a threshold voltage of a transistor for supplying light-emitting current to the light-emitting element.

[0007] The above mentioned object is achieved by the teaching of the independent claims.

45 **[0008]** According to the present invention, even when variation is caused in a threshold voltage of a transistor for supplying a light-emitting current to an organic EL element, the light-emitting element can emit light with desired brightness of gradation level.

Brief Description of Drawings

50 **[0009]** These objects and other objects and advantages of the present invention will become more apparent upon reading of the following detailed description and the accompanying drawings in which:

Fig. 1 illustrates the main structure of a display pixel used in a display apparatus according an embodiment not forming part of the present invention;

Fig. 2 illustrates a signal waveform in the respective operations of a display pixel;

Fig. 3A illustrates an operation status in a writing operation of a display pixel;

Fig. 3B illustrates an equivalent circuit in a writing operation of a display pixel;

Fig. 4A shows an example of an operating characteristic of a driving transistor in a writing operation of a display pixel;
Fig. 4B shows an example of a relation between the driving current of an organic EL element and a driving voltage in a writing operation;

Fig. 5A illustrates an operation status in a retention operation of a display pixel;

Fig. 5B illustrates an equivalent circuit in a retention operation of a display pixel;

Fig. 6 illustrates an operating characteristic of a driving transistor in a retention operation of a display pixel;

Fig. 7A illustrates an operation status in a light-emitting operation of a display pixel;

Fig. 7B illustrates an equivalent circuit in a light-emitting operation of a display pixel;

Fig. 8A shows an example of an operating characteristic of a driving transistor in a light-emitting operation of a display pixel;

Fig. 8B shows an example of a load characteristic of the organic EL element in a light-emitting operation;

Fig. 9 is a block diagram showing the structure of the display apparatus in Embodiment 1;

Fig. 10 shows the structure of the main part of the data driver and the display pixel (pixel driving circuit, light-emitting element) in Embodiment 1;

Fig. 11 shows the respective steps from a selection operation to a light-emitting operation;

Fig. 12 illustrates a timing chart in a driving control of the display apparatus;

FIG. 13 illustrates a timing diagram in the selection operation of the display apparatus;

Fig. 14 illustrates operation statuses of the data driver and the display pixel in the precharge operation;

Fig. 15 illustrates the operation statuses of the data driver and the display pixel in the reading operation of a reference voltage;

Fig. 16 illustrates the operation statuses of the data driver and the display pixel in the writing operation of the display apparatus;

Fig. 17 illustrates the operation statuses of the data driver and the display pixel in the retention operation of the display apparatus;

Fig. 18 illustrates the operation statuses of the data driver and the display pixel in the light-emitting operation of the display apparatus;

Fig. 19 shows an example of a voltage applied to the data line in the selection period;

Fig. 20 illustrates a relation between an elapsed time and a potential change of a source terminal of a driving transistor during a transient response period;

Fig. 21 illustrates a relation between a threshold voltage of a driving transistor and a difference to a reference voltage;

Fig. 22 shows an example of a circuit structure of a data driver;

Fig. 23 shows a characteristic when a digital voltage of a digital-analog converter used as a data driver is converted to an analog voltage;

Fig. 24 illustrates an operation timing in a method for driving a display apparatus including a display zone of this embodiment;

Fig. 25 illustrates the structure of the main part of a data driver and a display pixel of Embodiment 2 (pixel driving apparatus, light-emitting element);

Fig. 26A illustrates an equivalent circuit including a capacity component parasitic on the pixel driving circuit;

Fig. 26B illustrates an equivalent circuit corresponding to the capacity component C_s shown in Fig. 27A;

Fig. 27A illustrates an equivalent circuit in a writing operation of a display pixel in Embodiment 2 not forming part of the present invention;

Fig. 27B illustrates an equivalent circuit in a light-emitting operation of a display pixel in Embodiment 2 not forming part of the present invention;

Fig. 27C illustrates an equivalent circuit corresponding to the capacity component $C_{gd13'}$ shown in Fig. 27B;

Fig. 27D illustrates an equivalent circuit corresponding the capacity component C_s'' shown in Fig. 27B;

Fig. 28A illustrates the first model for describing law of conservation of charge amount;

Fig. 28B illustrates the second model for describing law of conservation of charge amount;

Fig. 29A illustrates a model for describing a status in which charge is retained in a display pixel when a high level selection signal is applied thereto;

Fig. 29B illustrates a model for describing a status in which charge is retained in a display pixel when a low level selection signal is applied thereto;

Fig. 30A illustrates a voltage in the equivalent circuit in a selection step;

Fig. 30B illustrates a voltage in the equivalent circuit in a not-selected status switching step;

Fig. 31A illustrates a voltage change when the selection step (writing operation) shifts to the not-selected status;

Fig. 31B illustrates a voltage change in the not-selected status retention step;

Fig. 32A illustrates a voltage in the equivalent circuit of the not-selected status retention step;

Fig. 32B illustrates a voltage in the equivalent circuit of the power source voltage switching step;

Fig. 32C illustrates a voltage in the equivalent circuit of the light-emitting step;

Fig. 33 illustrates a voltage in the equivalent circuit during a writing operation;

Fig. 34 illustrates a relation between input data and a data voltage and an original gradation level voltage in a writing operation;

Fig. 35 illustrates a relation between input data and a compensated gradation level voltage and a threshold voltage in a writing operation;

Fig. 36A illustrates the first example of a relation between input data and a light emission driving current and a threshold voltage in a light-emitting operation;

Fig. 36B illustrates the second example of a relation between input data and a light emission driving current and a threshold voltage in a light-emitting operation;

Fig. 37A illustrates the first example of a relation between the input data and the light emission driving current and variation in the threshold voltage in a light-emitting operation;

Fig. 37B illustrates the second example of a relation between the input data and the light emission driving current and variation in the threshold voltage in a light-emitting operation;

Fig. 37C illustrates the third example of a relation between the input data and the light emission driving current and variation in the threshold voltage in a light-emitting operation;

Fig. 38A illustrates the first example of the relation between the input data and the light emission driving current and the threshold voltage when a "γ effect" is not provided;

Fig. 38B illustrates the second example of the relation between the input data and the light emission driving current and the threshold voltage when a "γ effect" is not provided;

Fig. 39 illustrates a relation between a constant and input data set to cause the effect of the present invention;

Fig. 40 illustrates a relation between a voltage and a current of the organic EL element used for a test for checking the effect of the present invention; and

Fig. 41 illustrates a relation between an in-channel parasitic capacitance and a voltage of a transistor used for a display pixel (pixel driving circuit).

Best Mode for Carrying Out the Invention

[0010] Hereinafter, a display apparatus and a display driving apparatus according to an embodiment of the present invention will be described. This embodiment is an example in which the display apparatus of the present invention is a display apparatus 1 using a current driving-type light-emitting element to display an image. This light-emitting element may be an arbitrary light-emitting element. However, the following will describe a case where the light-emitting element is an organic EL element.

[0011] First, a display pixel PIX of the display apparatus 1 of this embodiment will be described. As shown in Fig. 1, the display pixel PIX includes a pixel driving circuit DC and an organic EL element OLED. The pixel driving circuit DC has a transistor T1, a transistor T2, and a capacitor Cs. The transistor T1 and the transistor T2 may have arbitrary element structures and characteristics. However, the following will describe a case where the transistor T1 and the transistor T2 are n channel-type thin film transistors.

[0012] The transistor T1 is an n channel-type thin film transistor (hereinafter referred to as "driving transistor") for driving the organic EL element OLED to emit light. The driving transistor T1 is structured so that a drain terminal is connected to a power source terminal TMv, a source terminal is connected to a contact point N2, and a gate terminal is connected to a contact point N1. This power source terminal TMv is applied with a power source voltage Vcc having different voltage values depending on an operation status of the pixel driving circuit DC.

[0013] The transistor T2 is an n channel-type thin film transistor that is hereinafter referred to as a "retention transistor". The retention transistor T2 is structured so that a drain terminal is connected to the power source terminal TMv (a drain terminal of the driving transistor T1), a source terminal is connected to the contact point N1, and a gate terminal is connected to the control terminal TMh. The control terminal TMh is applied with a retention control signal Shld.

[0014] The capacitor Cs is connected between the gate terminal and the source terminal of the driving transistor T1 (between the contact point N1 and the contact point N2). The capacitor Cs may be parasitic capacitance formed between the gate and source terminals of the driving transistor T1 or also may be the parasitic capacitance connected with a capacitive element in parallel thereto.

[0015] The organic EL element OLED is an organic EL element that emits light with a gradation level depending on supplied current. The organic EL element OLED is structured so that an anode terminal is connected to the contact point N2 and a cathode terminal TMc is applied with a reference voltage Vss. This reference voltage Vss has a fixed value. A data terminal TMd is connected to the contact point N2 is applied with a data voltage Vdata corresponding to the gradation level value of display data.

[0016] Next, a method for controlling the display pixel PIX having the above structure will be described.

[0017] The pixel driving circuit DC applies a voltage corresponding to the gradation level value of display data to the capacitor Cs to charge the capacitor Cs (hereinafter referred to as a "writing operation"). After the writing operation, the

capacitor Cs retains the written voltage (hereinafter referred to as a "retention operation"). Based on the charging voltage retained by the capacitor Cs, gradation level current corresponding to the gradation level of the display data flows in the organic EL element OLED and the organic EL element OLED emits light (hereinafter referred to as a "light-emitting operation"). The brightness of the light emitted by the organic EL element OLED corresponds to the gradation level of the display data.

[0018] As shown in Fig. 2, the pixel driving circuit DC sequentially performs the above-described writing operation, retention operation, and light-emitting operation. The following will describe conditions required for the display pixel PIX to perform the respective operations.

(Writing operation)

[0019] In the writing operation, the capacitor Cs is written with a voltage corresponding to the gradation level value of the display data. During the writing operation, the organic EL element OLED is in a light-off status in which the organic EL element OLED does not emit light. During the writing operation by the pixel driving circuit DC, the driving transistor T1 shows an operating characteristic illustrated in Fig. 4A,

[0020] In Fig. 4A, a characteristic line SPw, shown by a solid line, shows a relation between the drain-source voltage Vds and a drain-source current Ids in an initial state in which the n channel-type thin film transistor used as the driving transistor T1 is diode-connected. A point PMw on the characteristic line SPw is an operation point of the driving transistor T1. A characteristic line SPw2 shown by a broken line in Fig. 4A, shows a relation between the drain-source voltage Vds and the drain-source current Ids when the driving transistor T1 has a characteristic change due to its driving history. As shown in Fig. 4A, the drain-source voltage Vds is a sum of a threshold voltage Vth and a voltage Veff_gs, as shown in the following formula (1).

$$V_{ds}=V_{th}+V_{eff_gs} \quad (1)$$

[0021] When the drain-source voltage Vds exceeds the threshold voltage Vth (a threshold voltage between a gate and a source = a threshold voltage between a drain and a source), the drain-source current Ids nonlinearly increases with an increase of the drain-source voltage Vds as shown by the characteristic line SP2. Thus, Veff_gs in Fig. 4A represents a voltage effectively forming the drain-source current Ids.

[0022] During the writing operation shown in Fig. 2, the driving current and the driving voltage of the organic EL element OLED show the characteristic shown in Fig. 4B. In Fig. 4B, the characteristic line SPe shown by the solid line shows a relation in an initial state between a driving voltage Voled applied between an anode and a cathode of the organic EL element OLED and a driving current Ioled flowing between the anode and the cathode. When the driving voltage Voled exceeds the threshold voltage Vth_oled, the driving current Ioled nonlinearly increases with an increase of the driving voltage Voled as shown by the characteristic line SPe. In Fig. 4B, a characteristic line SPe2 represents an example of a relation between the driving voltage Voled and the driving current Ioled when the characteristic changes in accordance with the driving history of the organic EL element OLED.

[0023] As shown in Fig. 3A, during the writing operation, the control terminal TMh of the retention transistor T2 is applied with a retention control signal Shld of an ON-level (high level H) to turn ON the retention transistor T2. As a result, the connection (short-circuiting) between the gate and the drain of the driving transistor T1 is established to cause the driving transistor T1 to be in a diode-connected state. The power source terminal TMv is applied with the first power source voltage Vccw for a writing operation and the data terminal TMd is applied with a data voltage Vdata corresponding to the gradation level value of the display data.

[0024] Then, the drain and source of the driving transistor T1 have therebetween current Ids corresponding to the potential difference between the drain and the source (Vccw - Vdata) (hereinafter referred to as "expected value current"). The data voltage Vdata is set to include this expected value current Ids as a voltage value required for obtaining a current value that is required for the organic EL element OLED to emit light with an appropriate brightness depending on the gradation level value of the display data. At this timing, as mentioned above short-circuiting is caused between the gate and the drain of the driving transistor T1 and the drain of the driving transistor T1 is in a diode-connected status. Thus, as shown in Fig. 3B, the drain-source voltage Vds of the driving transistor T1 equals the gate-source voltage Vgs and is represented by the following formula (2). It is noted that the capacitor Cs is written (or charged) with this gate-source voltage Vgs.

$$V_{ds}=V_{gs}=V_{ccw}-V_{data} \quad (2)$$

[0025] Next, the first power source voltage V_{ccw} will be described. The driving transistor T1 is an n channel-type transistor. Thus, in order to flow the drain-source current I_{ds} of the driving transistor T1 the gate potential must be higher than the source potential (positive potential). As shown in Fig. 3B, the gate potential equals the drain potential (the first power source voltage V_{ccw}) and the source potential equals the data voltage V_{data} . Thus, to flow the drain-source current I_{ds} , the following formula (3) must be established.

$$V_{data} < V_{ccw} \quad (3)$$

[0026] In order for the organic EL element OLED to be in a light-off state, a difference between a voltage of the anode terminal of the organic EL element OLED and a voltage of the cathode terminal T_{Mc} must be equal to or less than the light-emitting threshold voltage V_{th_oled} of the organic EL element OLED. As shown in Fig. 3B, the contact point N2 is connected to the anode terminal of the organic EL element OLED. The contact point N2 is connected to the data terminal T_{Md} and is applied with the data voltage V_{data} . On the other hand, the cathode terminal T_{Mc} is applied with the reference voltage V_{ss} having a fixed value.

[0027] Therefore, in order to cause the organic EL element OLED to be in a light-off state in the in a writing operation, a difference between the data voltage V_{data} and the reference voltage V_{ss} must be equal to or less than the light-emitting threshold voltage V_{th_oled} of the organic EL element OLED. In this case, the contact point N2 has the potential V_{data} ; therefore the following formula (4) must be statisified in order for the organic EL element OLED to be in a light-off state during the writing operation. It is noted that, when the reference voltage V_{ss} is set to a ground potential of 0V, the formula (4) can be represented by the following formula (5).

$$V_{data} - V_{ss} = V_{th_oled} \quad (4)$$

$$V_{data} = V_{th_oled} \quad (5)$$

[0028] Thus, in order to cause the capacitor C_s to be written with the gate-source voltage V_{gs} of the driving transistor T1 and to cause the organic EL element OLED not to emit light off during a writing operation, a relation shown in the following formula (6) based on the above-described formula (2) and formula (5) must be established.

$$V_{ccw} - V_{gs} = V_{th_oled} \quad (6)$$

[0029] Then, the relation of the formula (1) established for the gate-source voltage V_{gs} when the driving transistor Tr1 is diode-connected ($V_{gs} = V_{ds} = V_{th} + V_{eff_gs}$) is substituted into the formula (6) to provide the following formula (7).

$$V_{ccw} = V_{th_oled} + V_{th} + V_{eff_gs} \quad (7)$$

[0030] When voltage $V_{eff_gs} = 0$ is established at which the drain-source current I_{ds} is formed, the formula (7) is represented by the following formula (8). As shown by this formula (8), during a writing operation, the first power source voltage V_{ccw} at a writing level must have a value that is equal to or lower than the sum of the light-emitting threshold voltage V_{th_oled} and the threshold voltage V_{th} of the driving transistor T1 (a gate-source threshold voltage=a drain-source threshold voltage).

$$V_{ccw} = V_{th_oled} + V_{th} \quad (8)$$

[0031] Generally, the characteristic of the driving transistor T1 of Fig. 4A and the characteristic of the organic EL element shown in Fig. 4B change in accordance with the driving history. The following will describe an influence of the change in the characteristic of the driving transistor T1 and the organic EL element OLED in accordance with the driving history in a writing operation.

[0032] First, the characteristic of the driving transistor T1 will be described. As shown in Fig. 4A, the threshold voltage V_{th} of the driving transistor T1 in the initial state increases in accordance with the driving history, by a threshold voltage change amount ΔV_{th} . When the threshold voltage varies in accordance with the driving history, the characteristic line

becomes a characteristic line SPw2 line obtained by substantially translating the initial characteristic line SPw to a higher voltage side. In this case, in order to obtain gradation level current (drain-source current I_{ds}) in accordance with the gradation level value of the display data, the data voltage V_{data} must be increased by the threshold voltage change amount ΔV_{th} .

[0033] Next, the following will describe an influence of the change in the characteristic of the organic EL element OLED during a writing operation. Generally, the organic EL element has resistance that increases in accordance with the driving history. As shown in Fig. 4B, in the characteristic line SPe2 after a change in the resistance of the organic EL element OLED, a rate at which the driving current I_{oled} increases with regards to an increase in the driving voltage V_{oled} (increase rate) decreases when compared with the initial characteristic line SPe before the resistance change.

[0034] In order to allow the organic EL element OLED to emit light with an appropriate brightness depending on the gradation level value of the display data even when the resistance is high, the driving current I_{oled} in accordance with the gradation level value must be supplied to the organic EL element OLED. In order to supply such a driving current I_{oled} , the driving voltage V_{oled} must be increased by a difference between the voltage corresponding to the necessary driving current I_{oled} for the gradation level in the characteristic line SPe2 and the voltage corresponding to the necessary driving current I_{oled} for the gradation level in the characteristic line SPe. It is noted that this difference voltage reaches the maximum value ΔV_{oled_max} when the driving current I_{oled} is the maximum value I_{oled_max} . When the writing operation is completed to satisfy the above-described conditions, the display pixel PIX carries out a retention operation.

(Retention operation)

[0035] During the retention operation, as shown in Fig. 5A, the control terminal TMh is applied with the retention control signal Shld of an OFF level (low level L). As a result, the retention transistor T2 is turned OFF to block electric connection between the gate and the drain of the driving transistor T1. Thus, the diode connection of the driving transistor T1 is cancelled to stop the charging of the capacitor Cs. As shown in Fig. 5B, the capacitor Cs retains the drain-source voltage V_{ds} of the driving transistor T1 (=gate-source voltage V_{gs}) charged during the writing operation.

[0036] The relation between the drain-source voltage V_{ds} and the drain-source current I_{ds} when the diode connection of the driving transistor T1 is cancelled follows the characteristic line SPh shown by the solid line in Fig. 6. The gate-source voltage V_{gs} in this case is maintained to have a fixed value (e.g., a value of a voltage retained by the capacitor Cs during the retention operation).

[0037] The characteristic line SPw in Fig. 6 is substantially the same as the characteristic line SPw during the writing operation shown in Fig. 4A and shows the characteristic when the driving transistor T1 is diode-connected. An intersecting point of the characteristic line SPh and the characteristic line SPw is at the operation point PMh during the retention. The characteristic line SPo in Fig. 6 is obtained by deducting the threshold voltage V_{th} from the voltages V_{gs} of the characteristic line SPw. At the intersecting point Po of the characteristic line SPo and the characteristic line SPh, the drain-source voltage V_{ds} has a pinch-off voltage V_{po} .

[0038] When the driving transistor T1 operates in accordance with the characteristic line SPh, a zone within which the drain-source voltage V_{ds} changes from 0V to a pinch-off voltage V_{po} is an unsaturated zone. In the unsaturated zone, the drain-source current I_{ds} increases with an increase of the drain-source voltage V_{ds} . A zone within which the voltage V_{ds} is equal to or higher than the pinch-off voltage V_{po} is a saturated zone. In the saturated zone, there is substantially no change in the drain-source current I_{ds} even when the drain-source voltage V_{ds} increases.

[0039] It is noted that the retention control signal Shld may be switched from an ON-level to an OFF level when the power source voltage V_{cc} is switched from the first power source voltage V_{ccw} for a writing operation to the second power source voltage V_{cce} for a light-emitting operation (when the retention operation is switched to the light-emitting operation). When the retention operation is completed in the manner described above, the display pixel PIX carries out a light-emitting operation.

(Light-emitting operation)

[0040] As shown in Fig. 7A, during a light-emitting operation, after the above-described retention operation, such that the diode connection of the driving transistor T1 remains cancelled. The power source terminal TMv is applied with the second power source voltage V_{cce} for a light-emitting operation as the terminal voltage V_{cc} instead of the first power source voltage V_{ccw} for a writing operation. This second power source voltage V_{cce} has a higher potential than that of the first power source voltage V_{ccw} .

[0041] As a result, as shown in Fig. 7B, the current I_{ds} in accordance with the value of the gate-source voltage V_{gs} flows between the drain and source of the driving transistor T1. This current I_{ds} is supplied to the organic EL element OLED to allow the organic EL element OLED to emit light with a brightness in accordance with the value of the current I_{ds} . During the light-emitting operation, the current I_{ds} can be maintained at a fixed level by maintaining the gate-source voltage V_{gs} at a fixed level. Thus, a voltage retained by the capacitor Cs (a voltage applied to the capacitor Cs from a

retention operation period to a light-emitting operation period) may be applied between the gate and the source for example.

[0042] During the light-emitting operation, when the gate-source voltage V_{gs} is fixed, the organic EL element OLED operates based on a load line SPe shown by the solid line in Fig. 8A. The load line SPe represents an inverted relation between the driving voltage V_{oled} and the driving current I_{oled} of the organic EL element OLED with regards to a value of a potential difference ($V_{cce} - V_{ss}$) between the power source terminal TMv and the cathode terminal TMc of the organic EL element OLED as reference. In Fig. 8A, the characteristic line SPh is substantially the same as the characteristic line SPh shown in Fig. 6 during the retention operation.

[0043] As shown in Fig. 8A, when processing proceeds from the retention operation to the light-emitting operation, the operation point of the driving transistor T1 moves from the operation point PMh during the retention operation to an operation point PMe during the light-emitting operation (an intersecting point during the retention operation of the characteristic line SPh and the load line SPe of the organic EL element OLED). As shown in Fig. 8A, this operation point PMe is a point at which a potential difference ($V_{cce} - V_{ss}$) between the power source terminal TMv and the cathode terminal TMc of the organic EL element is distributed between the drain and the source of the driving transistor T1 and between the anode and the cathode of the organic EL element OLED. Specifically, at the operation point PMe during the light-emitting operation, the voltage V_{ds} is applied between the drain and the source of the driving transistor T1 and the driving voltage V_{oled} is applied between the anode and the cathode of the organic EL element OLED as shown in Fig. 7B.

[0044] When the expected value current I_{ds} flowing between the drain and the source of the driving transistor T1 during the writing operation is equal to the driving current I_{oled} supplied to the organic EL element OLED during the light-emitting operation, the organic EL element OLED emits light having a brightness depending on the gradation level value of the display data. To realize this, the operation point PMe of the driving transistor T1 during the light-emitting operation must be maintained within the saturated zone shown in Fig. 8A.

[0045] On the other hand, the driving voltage V_{oled} of the organic EL element OLED has the maximum value V_{oled_max} when the highest display gradation level is reached. Specifically, in order to allow the organic EL element OLED to emit light with brightness depending on the gradation level value of the display data, the second power source voltage V_{cce} for a light-emitting operation may be set to satisfy a relation shown in the following formula (9). It is noted that the left-hand side of the formula (9) represents a voltage applied between the above-described power source terminal TMv and the cathode terminal TMc of the organic EL element OLED. When the reference voltage V_{ss} applied to the cathode terminal of the organic EL element OLED is set to have the ground potential of 0V, the formula (9) can be represented by the following formula (10).

$$V_{cce} - V_{ss} = V_{po} + V_{oled_max} \quad (9)$$

$$V_{cce} = V_{po} + V_{oled_max} \quad (10)$$

[0046] Next, the following will describe an influence of a change in the characteristic of the organic EL element OLED during the light-emitting operation.

[0047] As shown in Fig. 4B, the organic EL element OLED has higher resistance in accordance with the driving history and as a result the increase rate of the driving current I_{oled} with respect to the driving voltage V_{oled} decreases. Then, the load line SPe of the organic EL element OLED more gently inclines as shown by $SPe2$ and $SPe3$ in Fig. 8B. Specifically, the load line of the organic EL element OLED changes in accordance with the driving history to cause a change in the load line from SPe through $SPe2$ to $SPe3$. As a result, the operation point of the driving transistor T1 changes on the characteristic line SPh from PMe through $PMe2$ to $PMe3$.

[0048] When the operation point of the driving transistor T1 exists in the saturated zone (PMe to $PMe2$), the driving current I_{oled} maintains a value of the expected value current I_{ds} during the writing operation. When the operation point exists in the unsaturated zone (when the operating point moves from $PMe2$ to $PMe3$, for example) however, the driving current I_{oled} decreases and is lower than the expected value current I_{ds} during the writing operation. The decrease in the driving current I_{oled} causes the light-emitting element to emit light with a gradation level lower than the brightness corresponding to the gradation level value of the display data.

[0049] In the example of Fig. 8B, the pinch-off point Po exists at a boundary between the unsaturated zone and the saturated zone. Thus, a potential difference between the operation point PMe and the pinch-off point Po during the light-emitting operation functions, when the organic EL element has higher resistance, as a compensation margin for maintaining a driving current I_{oled} during the light-emitting operation. In other words, a compensation margin corresponding to the current value of the driving current I_{oled} functions as a potential difference on the characteristic line SPh between

a pinch-off point trajectory SPo and the load line SPe of the organic EL element. It is noted that the compensation margin decreases with an increase of the driving current I_{oled}. The compensation margin increases when a voltage increases that is applied between the power source terminal TMv and the cathode terminal TMc of the organic EL element OLED (V_{cce} - V_{ss}) increases.

[0050] In the above-described illustrative embodiment, a transistor voltage is used to control brightness of the respective light-emitting elements (hereinafter referred to as "voltage gradation level control"). Then, the data voltage V_{data} is set based on initial characteristics of the previously determined transistor drain-source voltage V_{ds} and the drain-source current I_{ds}. However, the data voltage V_{data} set based on the method as described above causes an increase in the threshold voltage V_{th} in accordance with the driving history. Thus, the driving current supplied to the light-emitting element fails to correspond to the display data (data voltage) and thus the light-emitting element does not emit light with preferred brightness. When the transistor is an amorphous transistor in particular, the element characteristic remarkably varies.

[0051] In an n-channel-type amorphous silicon transistor, a driving history or temporal change causes carrier trap to a gate insulating film. This carrier trap offsets a gate field and the characteristic between the drain-source voltage V_{ds} and the drain-source current I_{ds} have an increased threshold voltage V_{th}. In the example of Fig. 4A, during the writing operation, the threshold voltage V_{th} shifts from the characteristic SPw in an initial state to the characteristic SPw2 at a higher voltage. When the drain-source voltage V_{ds} is fixed in this case, the drain-source current I_{ds} decreases and the light-emitting element has reduced brightness. It is noted that the amorphous transistor in the example shown in Fig. 4A is designed to have a gate insulating film thickness of 300nm (3000Å), a channel width of 500μm, a channel length of 6.28μm, and a threshold voltage of 2.4V.

[0052] When the element characteristic of the transistor varies, the threshold voltage V_{th} mainly increases. After the variation in the element characteristic, the characteristic line SPw2 showing the relation between the drain-source voltage V_{ds} and the drain-source current I_{ds} is a substantial translation of the characteristic line SPw in the initial state. Thus, a characteristic substantially corresponding to the varied characteristic line SPw2 can be obtained by adding a fixed voltage (hereinafter referred to as "OFFSET voltage V_{ofst}") corresponding to the change amount ΔV_{th} of the initial threshold voltage V_{th} to the drain-source voltage V_{ds} of the initial characteristic line SPw. Specifically, during an operation for writing the display data to the pixel driving circuit DC, the source terminal of the driving transistor T1 (contact point N2) is applied with a voltage obtained by the drain-source voltage V_{ds} on the characteristic line SPw with and an OFFSET voltage V_{ofst} (hereinafter referred to as "compensated gradation level voltage V_{pix}").

[0053] By doing this, a change in the element characteristic due to the variation in the threshold voltage V_{th} can be compensated. Specifically, the light emission driving current I_{em} having a value depending on display data can be supplied to the organic EL element OLED. The organic EL element OLED having received the light emission driving current I_{em} emits light with brightness in accordance with the display data.

(Embodiment 1)

[0054] The following section will describe the display apparatus 1 of Embodiment 1 for displaying an image by the above-described display pixel PIX. First, the structure of the display apparatus 1 will be described. As shown in Fig. 9, the display apparatus 1 includes: a display zone 11; a selection driver 12; a power source driver 13; a data driver (display driving apparatus) 14; a controller 15; a display signal generation circuit 16; and a display panel 17.

[0055] The display zone 11 includes: a plurality of selection lines L_s; a plurality of data lines L_d; and a plurality of display pixels PIX. The respective selection lines L_s are arranged in the row direction of the display zone 11 (left-and-right direction in Fig. 9). The respective selection lines L_s are parallel to one another. The respective data lines L_d are arranged in the column direction of the display zone 11 (up-and-down direction in Fig. 9). The respective data lines L_d are parallel to one another. The respective display pixels PIX are arranged in the vicinity of the respective intersecting points of the respective selection lines L_s and the respective data lines L_d and in a lattice-like manner in "n" rows × "m" columns (n and m are a positive integer).

[0056] The selection driver 12 supplies a selection signal S_{sel} to the respective selection lines L_s with a predetermined timing. This selection signal S_{sel} is a signal for instructing the capacitor C_s with regards to the display pixel PIX to which a voltage corresponding to the gradation level value of the display data should be written. The selection driver 12 may be structured by any of an Integrated Circuit (IC) chip or a transistor.

[0057] The power source driver 13 supplies, with a predetermined timing, the power source voltage V_{cc} of the predetermined voltage level to a plurality of power source voltage lines L_v arranged in the selection line L_s in parallel with the selection line L_s.

[0058] The data driver (display driving apparatus) 14 applies, with a predetermined timing, the compensated gradation level voltage V_{pix} (e.g., V_{pix}(i), V_{pix}(i+1)) to the respective data lines L_d.

[0059] The controller 15 generates, based on a timing signal supplied from the display signal generation circuit 16, a signal for controlling the operations of the respective members to supply the signal to the respective members. For

example, the controller 15 supplies a selection control signal for controlling the operation of the selection driver 12, a power source control signal for controlling the operation of the power source driver 13, and a data control signal for controlling the operation of the data driver 14.

[0060] The display signal generation circuit 16 generates display data (data for brightness) based on a video signal inputted from the exterior of the display apparatus 1 to supply the display data to the data driver 14. The display signal generation circuit 16 also extracts, based on the generated display data, a timing signal (e.g., system clock) for displaying an image in the display zone 11 to supply the timing signal to the controller 15. This timing signal also may be generated by the display signal generation circuit 16.

[0061] The display panel 17 is a board having thereon the display zone 11, the selection driver 12, and the data driver 14. This board also may have thereon the power source driver 13. The display panel 17 also may have thereon a part of the data driver 14 and the remaining part of the data driver may be provided at the exterior of the display panel 17. In this case, a part of the data driver 14 in the display panel 17 may include an IC chip or a transistor.

[0062] The display panel 17 has, at the center thereof, the display panel 17 in which the respective display pixels PIX are arranged in a lattice-like manner. The respective display pixels PIX are divided into a group positioned at an upper zone of the display zone 11 and a group positioned at a lower zone. The display pixels PIX included in each group are connected to branched power source voltage lines Lv, respectively. It is noted that the group at the upper zone in Embodiment 1 includes the first to $(n/2)$ th display pixels PIX (" n " is an even number). The group at the lower zone includes the $(n/2+1)$ to " n "th display pixels PIX.

[0063] The respective power source voltage lines Lv in the group at the upper zone are connected to the first power source voltage line Lv1. The respective power source voltage lines Lv in the group at the lower zone are connected to the second power source voltage line Lv2. The first power source voltage line Lv1 and the second power source voltage line Lv2 are connected to the power source driver 13 in an independent manner. Thus, the power source voltage Vcc is commonly applied to the first to $(n/2)$ th display pixels PIX via the first power source voltage line Lv1. The $(n/2+1)$ to " n "th display pixels PIX are commonly applied with the power source voltage Vcc via the second power source voltage line Lv2. The power source driver 13 applies the power source voltage Vcc via the first power source voltage line Lv1 at a timing different from a timing at which the power source driver 13 applies the power source voltage Vcc via the second power source voltage line Lv2.

[0064] The display pixel PIX shown in Fig. 9 includes, as shown in Fig. 10, the pixel driving circuit DC and the organic EL element OLED. The pixel driving circuit DC has a transistor Tr11, a selection transistor Tr12, a driving transistor Tr13, and a capacitor Cs. This transistor Tr11 corresponds to the retention transistor T2 shown in Fig. 1 and the driving transistor Tr13 corresponds to the driving transistor T1 shown in Fig. 1. It is noted that the respective transistors Tr11 to Tr13 may be an arbitrary type of transistor but the respective transistors Tr11 to Tr13 in the following description are all an n channel-type field effect-type transistor.

[0065] The retention transistor Tr11 is a transistor for diode connection of the driving transistor Tr13. The retention transistor Tr11 is structured so that a gate terminal is connected to the selection line Ls, a drain terminal is connected to the power source voltage line Lv, and a source terminal is connected to the contact point N11. The selection line Ls is applied with the selection signal Ssel. This selection signal Ssel is identical with the retention control signal Shld shown in Fig. 2.

[0066] The selection transistor Tr12 shown in Fig. 10 is structured so that a gate terminal is connected to the selection line Ls, a source terminal is connected to the data line Ld, and a drain terminal is connected to the contact point N12. This contact point N12 corresponds to the contact point N2 shown in Fig. 1. The driving transistor Tr13 is structured so that a gate terminal is connected to the contact point N11, a drain terminal is connected to the power source voltage line Lv, and a source terminal is connected to the contact point N12. The contact point N11 corresponds to the contact point N1 shown in Fig. 1.

[0067] The capacitor Cs is an identical as that shown in Fig. 1. The capacitor Cs shown in Fig. 10 is connected between the contact point N11 and the contact point N12 (between the gate and the source of the driving transistor Tr13). The organic EL element OLED is structured so that an anode terminal is connected to the contact point N12 and the cathode terminal TMc is applied with a fixed reference voltage Vss.

[0068] During the writing operation, the compensated gradation level voltage Vpix corresponding to the gradation level value of the display data is applied to the capacitor Cs in the pixel driving circuit DC. Then, the compensated gradation level voltage Vpix, the reference voltage Vss, and the power source voltage Vcc (Vc_{ce}) having a high potential applied to the power source voltage line Lv for a light-emitting operation satisfy the relations of the above-described formulae (3) to (10). Thus, during the writing operation, the organic EL element OLED is in a light-off status. It is noted that pixel driving circuit DC is not limited to the structure shown in Fig. 10 and also may have any structure so long as that structure has elements corresponding to the respective elements shown in Fig. 1 and has a current path of the driving transistor T1 that has thereon current driving-type light-emitting elements OLED arranged in series. The light-emitting element is not limited to the organic EL element OLED and also may be other current driving-type light-emitting element such as a light-emitting diode.

[0069] The selection driver 12 includes, for example, a shift register and an output circuit section (output buffer). The shift register sequentially outputs, based on the selection control signal from the controller 15, shift signals corresponding to selection lines Ls of the respective rows. The output circuit section converts the level of this shift signal to a predetermined selected level (high level H or low level L). After the conversion, the output circuit section sequentially outputs the converted shift signals to the selection lines Ls of the respective rows as the selection signals Ssel.

[0070] For example, during a selection period Tsel shown in Fig. 13 (a period including a precharge period Tpre, a transient response period Ttrs, and a writing period Twrt), the selection driver 12 supplies the selection signal Ssel of a high level to the selection lines Ls of the respective rows connected with the display pixels PIX. The selection driver 12 supplies the selection signal Ssel to the selection line Ls in each row with a predetermined timing to sequentially set the display pixel PIX in each row to a selected status. The selection driver 12 may include a transistor that is the same as those of the respective transistors Tr11 to Tr13 in the pixel driving circuit DC.

[0071] During the selection period Tse, the power source driver 13 applies, based on the power source control signal from the controller 15, the power source voltage Vcc of a low potential (=Vccw) to the respective power source voltage lines Lv. During the light-emitting period, the power source driver 13 applies the power source voltage Vcc of a high potential (=Vcce) to the respective power source voltage lines Lv. In the example of Fig. 9, the power source driver 13 applies, during the operation of the display pixels PIX included in the group at the upper zone, the power source voltage Vcc to these display pixels PIX via the first power source voltage line Lv1. The power source driver 13 also applies, during the operation of the display pixels PIX included in the group at the upper zone, the power source voltage Vcc to these display pixels PIX via the second power source voltage line Lv2.

[0072] The lower source driver 13 may include a timing generator and an output circuit section. The timing generator generates, based on a power source control signal from the controller 15, timing signals corresponding to the respective power source voltage lines Lv. The timing generator is a shift register that sequentially outputs a shift signal for example. The output circuit section converts a timing signal to a predetermined voltage level (voltage values Vccw and Vcce) to apply the power source voltage Vcc suitable for this voltage level to the respective power source voltage lines Lv. When the number of the power source voltage lines Lv is small, the power source driver 13 may be provided in the controller 15 instead of the display panel 17.

[0073] The data driver (display driving apparatus) 14 generates a signal voltage (original gradation level voltage Vorg) corresponding to the display data (brightness corresponding to an emitting color) for each display pixel PIX supplied from the display signal generation circuit 16 for compensation. By the compensation of the original gradation level voltage Vorg, the data driver 14 generates a compensated gradation level voltage Vpix corresponding to the element characteristic (threshold voltage) of the driving transistor Tr13 provided in each display pixel PIX. After the generation, the data driver 14 applies the compensated gradation level voltage Vpix to the respective display pixels PIX via the data line Ld.

[0074] As shown in Fig. 10, the data driver 14 includes: a resistor 141, a gradation level voltage generator 142, a voltage converter 143, a voltage calculator 144, and changing-over switches SW1 to SW3. The gradation level voltage generator 142, the voltage calculator 144, and the changing-over switches SW1 to SW3 are provided in the data line Ld of each column and are provided in a quantity of "m" in the entire data driver 14.

[0075] A voltage reader 145 includes the voltage converter 143 and the changing-over switch SW2. The voltage converter 143 and the changing-over switch SW2 are connected to the data line Ld. It is noted that wiring resistances and capacities from the data line Ld to the respective changing-over switches SW1 to SW3 are structured so as to be equal to one another. Thus, a voltage drop due to the data line Ld is substantially equal to any of the respective changing-over switches SW1 to SW3.

[0076] The resistor 141 has a shift register and a data register. The shift register sequentially outputs a shift signal based on a data control signal from the controller 15. The data register acquires, based on the outputted shift signal, data for brightness of the gradation level to transfer the data to the gradation level voltage generators 142 provided in the respective columns in a parallel manner. The data register acquires data for gradation level by acquiring data corresponding to the display pixels PIX in one row on the display zone 11.

[0077] The gradation level voltage generator 142 generates and outputs the original gradation level voltage Vorg. This original gradation level voltage Vorg is a voltage that has a value corresponding to display data for each display pixel PIX and that shows brightness of the gradation level of each organic EL element OLED. It is noted that the original gradation level voltage Vorg is applied between an anode and a cathode of the organic EL element OLED and thus does not depend on the threshold voltage Vth of the transistor Tr13. When the driving transistor Tr13 operates based on the characteristic line SPw shown in Fig. 4A, the gradation level voltage generator 142 outputs, to the data line Ld, an absolute voltage value obtained by adding this original gradation level voltage Vorg to the threshold voltage Vth ($|Vorg+Vth|$). Then, by the potential difference between the power source voltage line Lv and the data line Ld, current for allowing the organic EL element OLED to emit light with brightness depending on the display data flows in the transistor Tr13.

[0078] During the writing operation, when current flows from the power source voltage line Lv to the data line Ld, the gradation level voltage generator 142 calculates a value obtained by multiplying, with -1, a voltage having a sum of the

original gradation level voltage Vorg and the threshold voltage Vth to output the value. When current flows from the data line Ld to the power source voltage line Lv, the gradation level voltage generator 142 directly outputs the voltage having the sum of the original gradation level voltage Vorg and the threshold voltage Vth without multiplying the voltage with a coefficient. It is noted that the original gradation level voltage Vorg is set to have a higher voltage with an increase of gradation level of display data.

[0079] The gradation level voltage generator 142 also may include, for example, a Digital to Analogue Converter (DAC) and an output circuit. The DAC converts, based on a gradation level reference voltage supplied from a power supply section (not shown), a digital signal voltage of display data to an analog signal voltage. It is noted that this gradation level reference voltage is a reference voltage based on the values of gradation level. The output circuit outputs, with a predetermined timing, the analog signal voltage converted by the DAC as the original gradation level voltage Vorg.

[0080] The voltage converter 143 applies the predetermined precharge voltage to the data line Ld. After the application, after a transient response period (natural relaxation period), the voltage of the capacitor Cs (reference voltage Vref) is read via the data line Ld.

[0081] After the reading, the voltage converter 143 determines a coefficient a to estimate a threshold voltage of the transistor Tr13 after the characteristic variation. Next, the voltage converter 143 multiplies the coefficient a with the reference voltage Vref to generate the first compensation voltage a·Vref to output the first compensation voltage a·Vref to the voltage calculator 144.

[0082] In the example of Fig. 10, current flowing in the data line Ld during the writing operation is set to flow from the data line Ld to the data driver 14. Thus, the first compensation voltage a·Vref is set so that $a \cdot V_{ref} < V_{ccw} - V_{th1} - V_{th2}$ is established. In this formula, Vth1 represents a threshold voltage of the transistor Tr13 and Vth2 represents a threshold voltage of the transistor Tr12. Then, current flows from the power source voltage line Lv via the drain and source of the transistor Tr13, the drain and source of the transistor Tr12, and the data line Ld.

[0083] The voltage calculator 144 performs addition and subtraction of the original gradation level voltage Vorg from the gradation level voltage generator 142, the first compensation voltage a·Vref from the voltage converter 143, and the previously-set second compensation voltage Vofst. When the gradation level voltage generator 142 includes the DAC, the addition and subtraction processings are performed for analog signals. It is noted that the second compensation voltage Vofst is determined based on an output variation characteristic of the threshold voltage Vth of the transistor Tr13 for example. Next, the voltage calculator 144 outputs the voltage obtained by addition and subtraction as the compensated gradation level voltage Vpix to the data line Ld. During the writing operation, voltage calculator 144 determines the compensated gradation level voltage Vpix so as to satisfy the following formula (11) for example.

$$V_{pix} = a \cdot V_{ref} - V_{org} + V_{ofst} \quad (11)$$

[0084] The respective changing-over switches SW1 to SW3 switches ON and OFF based on the data control signal from the controller 15, respectively. The changing-over switch SW1 turns ON or OFF the application by the voltage calculator 144 of the compensated gradation level voltage Vpix to the data line Ld. The changing-over switch SW2 turns ON or OFF an operation in which the voltage converter 143 reads a voltage of the data line Ld. The changing-over switch SW3 turns ON or OFF the application of the precharge voltage Vpre to the data line Ld.

[0085] The controller 15 controls the selection driver 12, the power source driver 13, and the data driver 14 to operate the respective drivers with a predetermined timing. The selection driver 12 sequentially sets the display pixel PIX to the selected status. The power source driver 13 applies the power source voltage Vcc to the respective power source voltage lines Lv. The data driver 14 applies the compensated gradation level voltage Vpix to the respective display pixels PIX.

[0086] The pixel driving circuits DC of the respective display pixels PIX performs a series of driving control operations under the control by the controller 15. This driving control operation including: a compensated gradation level voltage setting operation (precharge operation, transient response, reference voltage reading operation); a writing operation; a retention operation; and a light-emitting operation. By the driving control operation, the pixel driving circuit DC causes the display zone 11 to display image information based on a video signal.

[0087] The display signal generation circuit 16 extracts gradation level signals included in the video signal inputted from the exterior of the display apparatus 1. After the extraction, the display signal generation circuit 16 supplies the gradation data signals to the data driver 14 with regards to every one row of the display zone 11. When the video signal includes a timing signal defining the timing at which the image is to be displayed, the display signal generation circuit 16 may extract the timing signal to output the timing signal to the controller 15. Then, the controller 15 outputs the respective control signals to the respective drivers based on the timing defined by the timing signal.

(Method for driving display apparatus)

[0088] Next, a method for driving the display apparatus 1 will be described. It is noted that the following section will represent the respective display pixels PIX placed at positions (i, j) on the display zone 11 (n rows × m columns) by display pixels PIX (i, j) ($1 \leq i \leq n$, $1 \leq j \leq m$).

[0089] As shown in Fig. 11, the method for driving the display apparatus 1 of Embodiment 1 including: a selection step, a not-selected status switching step, a not-selected status retention step, a power source voltage switching step, and a light-emitting step. The respective steps are operations carried out in the respective display pixels PIX so that the respective display pixels PIX in the entire display zone 11 independently perform the operations of the respective steps. This selection step is a step for carrying out an operation shown in Fig. 13 (precharge operation, compensated gradation level voltage setting operation, writing operation). The not-selected status retention step is a step for performing the retention operation shown in Fig. 2. The light-emitting step is a step for performing the light-emitting operation shown in Fig. 2.

[0090] As shown in Fig. 12, the display apparatus 1 repeats a series of operations with a predetermined cycle period Tcyc. The cycle period Tcyc is a period required for one display pixel PIX to display one pixel of an image of one frame for example. In Embodiment 1, the cycle period Tcyc is a period required for the display pixels PIX for one row to display an image of one row of video frames.

[0091] First, in the compensation period Tdet in the selection period Tsel, a precharge operation is performed. In the precharge operation, the voltage converter 143 applies the predetermined precharge voltage Vpre to data line Ld of the respective columns. As a result, the precharge current Ipre from the power source voltage line Lv flows in the respective rows to the data line Ld. Thereafter, as shown in Fig. 13, the changing-over switch SW3 is turned OFF and the application of the precharge voltage Vpre by the voltage converter 143 is stopped. As a result, the precharge operation is completed. It is noted that a timing at which the application of the precharge voltage Vpre is completed is included in the compensation period Tdet.

[0092] When the read timing t1 shown in Fig. 13 has passed since the stoppage of the application of the precharge voltage Vpre, the voltage converter 143 reads a reference voltage Vref(t1).

[0093] In the compensated gradation level voltage setting operation, the gradation level voltage generator 142 generates the original gradation level voltage Vorg corresponding to the display data supplied from the display signal generation circuit 16. The voltage calculator 144 compensates the original gradation level voltage Vorg generated by the gradation level voltage generator 142 to generate the compensated gradation level voltage Vpix. When the voltage calculator 144 generates the compensated gradation level voltage Vpix, the compensated gradation level voltage setting operation is completed. Thereafter, the writing operation is performed.

[0094] In the writing operation, the voltage calculator 144 applies the compensated gradation level voltage Vpix to the respective data lines Ld. As a result, the writing current (the drain-source current Ids of the transistor Tr13) flows in the capacitor Cs.

[0095] In the retention operation, a voltage depending on the written compensated gradation level voltage Vpix (charge enough to flow writing current) written by a writing operation between the gate and the source of the transistor Tr13 is charged in the capacitor Cs and is retained. Hereinafter, a period during which the retention operation is performed will be referred to as a "retention period Thld".

[0096] In the light-emitting operation, as shown in Fig. 12, based on the charging voltage retained by the capacitor Cs, the light emission driving current Iem (e.g., Iem(i), Iem(i+1)) is supplied to the organic EL element OLED. The organic EL element OLED emits light with gradation level depending on display data. Hereinafter, a period during which the light-emitting operation is performed will be referred to as a "light-emitting period Tem". During the light-emitting period Tem, the light emission driving current Iem desirably equals to the drain-source current Ids of the transistor Tr13.

[0097] Hereinafter, the respective operations during the above-described selection operation will be described by an example of the display pixels PIX in the "i"th row. The reference voltage reading operation and the compensated gradation level voltage generation operation are performed during the election period Tsel for the display pixels PIX in the "i"th row now being processed.

[0098] As shown in Fig. 13, a period during which the precharge operation is performed during the compensation period Tdet will be referred to as a "precharge period Tpre". During this precharge period Tpre, the power source voltage line Lv is applied with the power source voltage Vccw. The voltage converter 143 applies the predetermined precharge voltage Vpre to the respective data lines Ld. As a result, the drain-source current Ids depending on the precharge voltage Vpre flows in the transistor Tr13 of the respective display pixels PIX arranged in a specific row (e.g., the "i"th row). The capacitor Cs accumulates charge depending on the precharge voltage Vpre.

[0099] As shown in Fig. 13, when the precharge operation is completed, the display driving apparatus DC turns OFF the changing-over switch SW3 to stop the application of the precharge voltage Vpre. After the completion of the precharge operation, a transient response is started. Thus, a timing at which the precharge operation is completed will be hereinafter referred to as "transient response start timing t0". Hereinafter, a period from the start of the transient response to the

completion will be referred to as a "transient response period Ttrs".

[0100] During the transient response period Ttrs, the data driver 14 performs the reference voltage reading operation. After the time since the transient response start timing t0 has passed and the read timing t1 is reached, the voltage converter 143 reads, via data line Ld, the charging voltage of the capacitor Cs retained between the gate and the source of the transistor Trl3. The read charging voltage is the reference voltage Vref(tl) shown in Fig. 13.

[0101] Next, during the compensation period Tdet shown in Fig. 13, the pixel driving circuit DC performs the compensated gradation level voltage generation operation. In the compensated gradation level voltage generation operation, the voltage calculator 144 sets the compensated gradation level voltage Vpix based on the reference voltage Vref(tl).

[0102] As shown in Fig. 14, during the precharge period Tpre, the power source driver 13 applies the power source voltage Vcc of the writing operation level (=the first power source voltage Vccw = reference voltage Vss) to the power source voltage line Lv connected to the display pixels PIX in the "i"th row. The selection driver 12 applies the selection signal Ssel of the selected level (high level) to the selection line Ls of the "i"th row. The display pixels PIX in the "i"th row are set to the selected status.

[0103] Then, in the respective display pixels PIX of the "i"th row, the respective transistors Tr11 are turned ON and the respective driving transistors Tr13 are in a diode-connected status. As a result, the power source voltage Vcc(=Vccw) is applied to the drain terminal and the gate terminal driving transistor Trl3 (contact point N11; one end of the capacitor Cs). The transistor Tr12 is also turned ON and the source terminal of the transistor Trl3 (contact point N12; the other end of the capacitor Cs) is electrically connected to the data lines Ld of the respective columns.

[0104] In synchronization with this timing, the controller 15 supplies a data control signal. As shown in Fig. 13, the data driver 14 turns OFF the changing-over switch SW1 to ON and turns ON the changing-over switches SW2 to SW3. As a result, the predetermined precharge voltage Vpre is applied to the respective capacitors Cs via the respective data lines Ld.

[0105] During the application of the precharge voltage Vpre, the maximum value of the threshold voltage of the driving transistor Tr13 after the variation in the element characteristic is a sum of the initial threshold voltage Vth0 and the maximum value ΔVth_max of the variation value ΔVth of the threshold voltage. The maximum value of the drain-source voltage of the transistor Tr12 is a sum of the initial drain-source voltage Vds12 and the maximum value ΔVds12_max of the variation value ΔVds12 of the drain-source voltage Vds12 due to increased resistance of the transistor Tr12. It is also assumed that a voltage drop due to the selection transistor Tr12 shown in Fig. 14 and the wiring resistance from the power source voltage line Lv to the data line Ld except for the selection transistor Tr12 is Vvd. Then, the precharge voltage Vpre is set to satisfy the following formula (12). It is noted that the potential difference (Vccw-Vpre) shown at the left-hand side of the formula (12) is a voltage applied to the selection transistor Tr12 and the driving transistor Tr13.

$$V_{ccw}-V_{pre}=(V_{th0}+\Delta V_{th_max})+(V_{ds12}+\Delta V_{ds12_max})+V_{vd} \quad (12)$$

[0106] The selection signal Ssel outputted to the selection line Ls is a positive voltage during the compensation period Tdet and is a negative voltage during periods other than the compensation period Tdet. Then, a voltage applied to the gate terminal of the transistor Tr12 is not remarkably close to the positive voltage. Thus, the maximum value ΔVds12_max of the variation value ΔVds12 the drain-source voltage is so small that the maximum value ΔVds12_max of can be ignored when compared with the maximum value ΔVth_max of the variation value ΔVth of the threshold voltage of the driving transistor Tr13. Thus, the formula (12) can be represented by the following formula (12a).

$$V_{ccw}-V_{pre}=(V_{th0}+\Delta V_{th_max})+V_{ds12}+V_{vd} \quad (12a)$$

[0107] Specifically, a voltage depending on the value of the precharge voltage Vpre is applied between both ends of the capacitor Cs (the gate and the source of the transistor Trl3). The voltage applied to the capacitor Cs is higher than the threshold voltage Vth after the variation in the element characteristic of the driving transistor Tr13. Thus, as shown in Fig. 14, the driving transistor Tr13 is turned ON to flow the precharge current Ipre depending on this voltage between the drain and the source of the transistor Tr13. Thus, both ends of the capacitor Cs immediately accumulates the charge based on this precharge current Ipre (voltage based on the precharge voltage Vpre).

[0108] The pixel driving apparatus DC owned by the display pixel PIX has a structure shown in Fig. 10. Thus, in order to flow the precharge current Ipre from the data line Ld in the data driver direction, the precharge voltage Vpre is set to have a negative potential to the power source voltage Vccw of the writing operation level (low level) (Vpre<Vccw=0).

[0109] In the precharge operation, it is assumed that a signal applied to the source terminal of the transistor Trl3 is a current signal. In this case, a risk is caused where the wiring capacity and wiring resistance owned by the data line Ld and/or the capacity component included in the pixel driving apparatus DC may delay a change in a potential (charging

voltage) in the capacitor Cs. However, the precharge voltage V_{pre} applied in Embodiment 1 is a voltage signal and thus the can be quickly charged with the capacitor Cs during the initial precharge period T_{pre} . Then, as shown in Fig. 13, the charging voltage of the capacitor Cs is rapidly close to the precharge voltage V_{pre} to subsequently gradually converge to the precharge voltage V_{pre} within the remaining period of the precharge period T_{pre} .

[0110] It is noted that, during the precharge period T_{pre} , the voltage of the precharge voltage V_{pre} applied to the anode terminal of the organic EL element OLED (contact point N12) is set to be lower than the reference voltage V_{ss} applied to the cathode terminal TMc. The power source voltage V_{ccw} is set to be equal to or lower than the reference voltage V_{ss} . Thus, the organic EL element OLED is not in a positive bias status and thus has no current therein. Thus, during the precharge period T_{pre} , the organic EL element OLED does not emit light.

[0111] During the transient response period T_{trs} after the precharge period T_{pre} (natural relaxation period), the data driver 14 maintains, as shown in Fig. 13, the changing-over switch SW1 in an OFF status and maintains the changing-over switch SW2 in an ON status. The data driver 14 switches the changing-over switch SW3 from ON to OFF. This blocks the application of the precharge voltage V_{pre} to the data line Ld and the display pixels PIX in the "i"th row in the selected status (pixel driving circuit DC).

[0112] Then, as shown in Fig. 15, the transistors Tr11 and Tr12 maintains an ON status. An electric connection between the pixel driving circuit DC and the data line Ld is maintained but an application of the voltage to the data line Ld is blocked. Thus, the other terminal side of the capacitor Cs (contact point N12) is set to have high impedance.

[0113] The gate and the source of the transistor Tr13 (both ends of the capacitor Cs) have therebetween, by the above-described precharge operation, a potential difference that is equal to or higher than the threshold voltage after the variation of the transistor Tr13 ($V_{th0} + \Delta V_{th_max}$). Thus, as shown in Fig. 15, the transistor Tr13 maintains an ON status and a transient current I_{ref} flows from the power source voltage line Lv via the transistor Tr13. During the transient response period T_{trs} (natural relaxation period), as shown in Fig. 13, the source terminal side of the transistor Tr13 (contact point N12; the other end of the capacitor Cs) has a gradually-increasing potential toward the potential of the drain terminal side (power source voltage line Lv side). In accordance with this, the data line Ld electrically connected via the transistor Tr12 also has a gradually-increasing potential.

[0114] During the transient response period T_{trs} , a part of the charge accumulated in the capacitor Cs is discharged. Thus, the gate-source voltage V_{gs} of the transistor Tr13 declines. Thus, the potential of the data line Ld changes from the precharge voltage V_{pre} to converge to the threshold voltage after the variation in the transistor Tr13 ($V_{th0} + \Delta V_{th}$). If the transient response period T_{trs} is too long, the potential difference ($V_{ccw} - V(t)$) changes to converge to ($V_{th0} + \Delta V_{th}$). The mark " $V(t)$ " represents a potential in the data line Ld changing with the time "t" and equals, as shown in Fig. 13, to the precharge voltage V_{pre} when the precharge period T_{pre} is completed. When the transient response period T_{trs} is too long however, the selection period T_{sel} increases and thus the display characteristic (a video display characteristic in particular) remarkably deteriorates.

[0115] To prevent this, in Embodiment 1, the transient response period T_{trs} is set so that the gate-source voltage V_{gs} of the transistor Tr13 is shorter than a period during which the potential converges to the threshold voltage after the variation ($V_{th} + \Delta V_{th}$). The transient response period T_{trs} is suitably set so that the pixel driving circuit DC can perform the precharge operation and the writing operation during the selection period T_{sel} . Specifically, a timing at which the transient response period T_{trs} is completed (reference voltage read timing) is set to a specific timing in a status in which the gate-source voltage V_{gs} of the transistor Tr13 is changing. It is noted that the organic EL element OLED does not emit light even during the transient response period T_{trs} . The reason is that a value of a voltage applied to the contact point N12 at the anode terminal side of the organic EL element OLED is lower than the reference voltage V_{ss} applied to the cathode terminal TMc and thus a positive bias status is not provided.

[0116] Next, the reference voltage reading operation will be described. This reference voltage reading operation is identical with the operation shown in Fig. 13. Specifically, at the read timing t_1 , the voltage converter 143 reads the potential of the data line Ld (reference voltage $V_{ref}(t_1)$) connected thereto via the changing-over switch SW2 shown in Fig. 15. The reference voltage read timing t_1 is a timing at which the transient response period T_{trs} is completed. Specifically, the transient response period T_{trs} shown in Fig. 13 is equal to (the reference voltage read timing t_1) - (transient response start timing t_0).

[0117] As shown in Fig. 15, the data line Ld is connected to the source terminal (contact point N12) of the driving transistor Tr13 via the selection transistor Tr12 set to an ON status. The reference voltage $V_{ref}(t_1)$ read by the voltage converter 143 is a function of the time "t" and is determined based on a voltage corresponding to the gate-source voltage V_{gs} of the transistor Tr13.

[0118] During the transient response period T_{trs} , this voltage V_{gs} is different depending on the threshold voltage V_{th} of the transistor Tr13 or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$). Thus, the threshold voltage V_{th} or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$) can be substantially identified based on the change in the gate-source voltage V_{gs} . Then, with an increase of a variation amount ΔV_{th} of the threshold voltage, a ratio of the change in the gate-source voltage V_{gs} declines.

[0119] In the transistor Tr13, the variation amount ΔV_{th} increases with an increase of the variation of the threshold

voltage V_{th} and the reference voltage $V_{ref}(t)$ also decreases. Thus, based on the reference voltage $V_{ref}(t)$, the threshold voltage V_{th} or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$) of the transistor $Tr13$ can be identified.

[0120] The reference voltage V_{can} can be represented by the following (13). It is noted that $V_{gs}(t_0)$ shown in the formula (13) represents a gate-source voltage of the transistor $Tr13$ at the read timing $t_1(t_1)$. The mark "VR" represents a sum of the voltage drop V_{ds12} due to the source-drain resistance of the transistor $Tr12$ and a voltage drop due to the wiring resistance V_{vd} .

$$V_{ccw} - V_{ref}(t) = V_{gs}(t) + VR \quad (13)$$

[0121] Specifically, during a period from an arbitrary timing (t_0) during the transient response period T_{trs} to a timing (t_1) at which the transient response period T_{trs} is completed, a potential change in the data line Ld ($V_{ref}(t_1) - V_{ref}(t_0)$) depends on a change in the gate-source voltage of transistor $Tr13$ ($V_{gs}(t_1) - V_{gs}(t_0)$). The threshold voltage V_{th} of the transistor $Tr13$ is identified based on this change amount.

[0122] The voltage converter 143 retains the read reference voltage $V_{ref}(t)$ via a buffer. Then, the voltage converter 143 inversely amplifies the reference voltage V_{ref} to convert the voltage level to output the result as "the first compensation voltage $a \cdot V_{ref}$ ". Then, the reference voltage reading operation is completed and the pixel driving circuit DC performs an operation for writing display data.

[0123] Next, this writing operation will be described. During the writing operation, the controller 15 supplies a data control signal to the changing-over switches $SW1$ to $SW3$ included in the voltage reader 145 shown in Fig. 10. As a result, as shown in Fig. 16, the changing-over switch $SW1$ is turned ON and the changing-over switches $SW2$ to $SW3$ are turned OFF. This provides an electric connection between the data line Ld and the voltage calculator 144. The power source driver 13 outputs the first power source voltage V_{ccw} for a writing operation.

[0124] Next, display data from the display signal generation circuit 16 shown in Fig. 9 is transferred, via the resistor 141, to the gradation level voltage generators 142 provided in the respective columns (the respective data lines Ld). The gradation level voltage generator 142 acquires, from the transferred display data, gradation level values of the display pixel PIX (display pixel PIX set to a selected status) to be subjected to the writing operation. Then, the gradation level voltage generator 142 determines whether the gradation level values have the 0th gradation level or not.

[0125] When the gradation level values have the 0th gradation level, the gradation level voltage generator 142 outputs, to the voltage calculator 144, a predetermined gradation level voltage (a gradation level voltage) V_{zero} for causing the organic EL element OLED to perform a no-light-emitting operation (or a black display operation). This black gradation level voltage V_{zero} is applied to the data line Ld via the changing-over switch $SW1$ shown in Fig. 16. Then, the voltage calculator 144 does not perform a compensation processing based on the reference voltage V_{ref} (compensation processing for compensating the variation of the threshold voltage V_{th} of the transistor $Tr13$). The black gradation level voltage V_{zero} is set to ($-V_{zero} < V_{th} - V_{ccw}$). Then, the diode-connected transistor $Tr13$ has the gate-source voltage $V_{gs} (= V_{ccw} - V_{zero})$ lower than the threshold voltage V_{th} or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$) to result in $V_{gs} < V_{th}$. It is noted that the black gradation level voltage V_{zero} suppresses the variation of the respective threshold voltages of the transistors $Tr12$ and $Tr13$ and thus $V_{zero} = V_{ccw}$ is desirably established.

[0126] On the other hand, when the gradation level values does not have the 0th gradation level, the gradation level voltage generator 142 generates the original gradation level voltage V_{org} having a voltage value suitable for the gradation level values to output the original gradation level voltage V_{org} to the voltage calculator 144. The voltage calculator 144 uses the first compensation voltage $a \cdot V_{ref}$ shown in Fig. 16 outputted from the voltage converter 143 to compensate this original gradation level voltage V_{org} so as to have a voltage value suitable for the variation of the threshold voltage V_{th} of the transistor $Tr13$.

[0127] Then, the voltage calculator 144 calculates the compensated gradation level voltage V_{pix} so that the original gradation level voltage V_{org} , the first compensation voltage $a \cdot V_{ref}$, and the second compensation voltage V_{fst} to satisfy the above-described formula (11). It is noted that the second compensation voltage V_{fst} is calculated based on a variation characteristic of the threshold voltage V_{th} of the transistor $Tr13$ (a relation between the threshold voltage V_{th} and the reference voltage V_{ref}) for example. The original gradation level voltage V_{org} is a positive voltage having an increasing potential with an increase of the gradation level of the display data.

[0128] The voltage calculator 144 applies the generated compensated gradation level voltage V_{pix} to the data line Ld via the changing-over switch $SW1$. The coefficient a of the first compensation voltage $a \cdot V_{ref}$ is a positive value while the second compensation voltage V_{fst} is a positive value depending on the design of the transistor $Tr13$ ($-V_{fst} < 0$). The compensated gradation level voltage V_{pix} is set to have a relatively negative potential based on the power source voltage V_{cc} of a writing operation level ($= V_{ccw} = \text{reference voltage } V_{ss}$) as reference. Thus, the compensated gradation level voltage V_{pix} declines toward a negative potential with an increase of a gradation level (and the voltage signal has an increasing amplitude).

[0129] The source terminal (contact point N12) of the transistor Tr13 included in the display pixel PIX set to the selected status is applied, based on the compensation voltage ($a \cdot V_{ref} + V_{ofst}$) depending on the threshold voltage V_{th} or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$) of the transistor Tr13, with the compensated gradation level voltage V_{pix} for which the original gradation level voltage V_{org} is compensated. Thus, the voltage V_{gs} depending on the compensated gradation level voltage V_{pix} is applied between the gate the source of the transistor Tr13 (both ends of the capacitor Cs). In the writing operation as described above, instead of flowing current suitable for display data in the gate terminal and the source terminal of the transistor Tr13 to set a voltage, a desired voltage is directly applied to the gate terminal and the source terminal. Thus, potentials of the respective terminals and contact points can be quickly set to a desired status.

[0130] It is noted that, during the writing period T_{wrt} , the compensated gradation level voltage V_{pix} applied to the anode terminal of the organic EL element OLED is set to be lower than the reference voltage V_{ss} applied to the cathode terminal TMc. Thus, the organic EL element OLED is in a reverse bias status and thus does not emit light. Then, the writing operation is completed and the display apparatus 1 performs a retention operation.

[0131] Next, this retention operation will be described. As shown in Fig. 12, during the retention period T_{hld} , the selection driver 12 applies the selection signal Ssel of a not-selected level (low level) to the selection line Ls of the "i"th row. As a result, the retention transistor Tr11 is turned OFF as shown in Fig. 17 to cancel the diode-connected status of the driving transistor Tr13. The selection signal Ssel of the not-selected level also turns OFF the selection transistor Tr12 shown in Fig. 17 to block an electric connection between the source terminal of the transistor Tr13 (contact point N12) and the data line Ld. Then, a voltage for which the threshold voltage V_{th} or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$) is compensated is retained between the gate and the source of the transistor Tr13 of the "i"th row (both ends of the capacitor Cs).

[0132] As shown in Fig. 12, during the retention period T_{hld} , the selection driver 12 applies the selection signal Ssel of the selected level (high level) to the selection line Ls of the (i+1)th row. As a result, the display pixel PIX of the (i+1)th row is set to the selected status. Thereafter, until the selection period T_{sel} of the final row for a single group is completed, the respective rows are subjected to the above-described compensated gradation level voltage setting operation and writing operation. Then, the selection driver 12 applies, with different timings, the selection signal Ssel of the selected level to the selection lines Ls of the respective rows. It is noted that, as shown in Fig. 24, the display pixels PIX of the respective rows for which the compensated gradation level voltage setting operation and the writing operation are already completed continuously perform the retention operation until the display pixels PIX of all rows are written with the compensated gradation level voltage V_{pix} (a voltage depending on the display data).

[0133] This retention operation is performed between the writing operation and the light-emitting operation when all display pixels PIX in the respective groups are driven and controlled to emit light simultaneously for example. In this case, as shown in Fig. 24, the retention periods T_{hld} are different for the respective rows. In the example of Fig. 17, the changing-over switches SW1 to SW3 are all OFF. However, as shown in Fig. 12, when the display pixels PIX in the "i"th row perform retention operation (the retention period T_{hld} of the "i"th row), the display pixels PIX after the (i+1)th row simultaneously perform the compensated gradation level voltage setting operation and the writing operation. Thus, the respective changing-over switches SW1 to SW3 are individually switching controlled at a predetermined timing during every selection period T_{sel} of the display pixels PIX of the respective rows. Then, the retention operation is completed and the display pixels PIX perform the light-emitting operation.

[0134] Next, this light-emitting operation will be described. As shown in Fig. 12, during the light-emitting operation (light-emitting period T_{em}), the selection driver 12 applies the selection signal Ssel of the not-selected level (low level) to the selection lines Ls of the respective rows (e.g., the "i"th row and the (i+1)th row). As shown in Fig. 18, the power source driver 13 applies, to the power source voltage line Lv, the power source voltage V_{cc} of the light-emitting operation level (the second power source voltage V_{cce}). This second power source voltage V_{cce} is a positive voltage having a higher potential than that of the reference voltage V_{ss} ($V_{cce} > V_{ss}$).

[0135] The second power source voltage V_{cce} is set so that the potential difference ($V_{cce} - V_{ss}$) is higher than a sum of the saturated voltage of the transistor Tr13 (pinch-off voltage V_{po}) and the driving voltage V_{oled} of the organic EL element OLED. Thus, as shown in the examples shown in Fig. 7 and Fig. 8, the transistor Tr13 operates in a saturated zone. The anode of the organic EL element OLED (contact point N12) is applied with a positive voltage depending on the voltage written by the writing operation between the gate and the source of the transistor Tr13 ($V_{ccw} - V_{pix}$). On the other hand, the cathode terminal TMc is applied with the reference voltage V_{ss} (e.g., ground potential) and thus the organic EL element OLED is in a reverse bias status.

[0136] As shown in Fig. 18, the power source voltage line Lv flows the light emission driving current I_{em} via the transistor Tr13 into the organic EL element OLED. This light emission driving current I_{em} has a current value depending on the compensated gradation level voltage V_{pix} . Thus, the organic EL element emits light with desired brightness of the gradation level. It is noted that the organic EL element OLED continues a light-emitting operation in the next cycle period T_{cyc} until the power source driver 13 starts the application of the power source voltage V_{cc} of the writing operation level ($=V_{ccw}$).

(Method for driving display apparatus)

[0137] Next, a method for driving the above-described display apparatus 1 will be described. An example of Fig. 19 shows a voltage change in the data line Ld. In this case, the respective transistors of the pixel driving circuit DC are an amorphous silicon transistor. The voltage and the power source voltage Vcc of the data line Ld are set so that current flowing in the pixel driving circuit DC is drawn into the data driver 14. The precharge voltage Vpre is set to -10V. The selection period Ttrs is set to 35 μ sec, the precharge period Tpre is set to 10 μ sec, the transient response period Ttrs is set to 15 μ sec, and the writing period Twrt is set to 10 μ sec, respectively. This selection period Ttrs=35 μ sec corresponds to a selection period allocated to the respective scanning lines when the display zone 11 has 480 scanning lines (selection lines) and the frame rate is 60fps.

[0138] In the driving control operation of the display apparatus 1, the precharge operation, the reference voltage reading operation, and the writing operation are sequentially performed during the selection period Tsel.

[0139] In the precharge operation, the data driver 14 turns ON the changing-over switch SW3. As a result, the data line Ld is applied with the precharge voltage Vpre of a negative voltage (-10V). Then, the data line voltage sharply declines as shown in Fig. 19. Thereafter, the data line voltage gradually converges to the precharge voltage Vpre in accordance with the wiring capacity of the data line Ld and a time constant due to the wiring resistance. By this change in the data line voltage, the gate-source voltage Vgs corresponding to the precharge voltage Vpre is applied between the gate and the source of the transistor Tr13 in a row set to the selected status.

[0140] Thereafter, at the transient response start timing t0, the data driver 14 turns OFF the changing-over switch SW3. This blocks the application of the precharge voltage Vpre to the data line Ld and the impedance is increased. However, the gate-source voltage Vgs is retained between the gate and the source of the transistor Tr13 due to the charging voltage of the capacitor Cs. Thus, the transistor Tr13 maintains the ON status. Thus, the transient current Ids flows between the drain and the source of the transistor Tr13.

[0141] While the transient current Ids flowing therebetween, the potential of the drain-source voltage Vds declines and the potential of the gate-source voltage Vgs equal to that of this voltage Vds also declines. Then, the voltage Vgs changes toward the threshold voltage Vth or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$) of the transistor Tr13. Thus, the potential of the source terminal of the transistor Tr13 (contact point N12) gradually increases as time passes.

[0142] In the driving control operation of Embodiment 1, current flowing in the display pixel (pixel driving circuit) is drawn from the data line Ld into the data driver 14. Thus, the data line Ld is set to have a negative voltage lower than that of the power source voltage Vcc. In this case, the higher gate-source voltage Vgs the transistor Tr13 has, the higher threshold voltage Vth or threshold voltage after the variation ($V_{th0} + \Delta V_{th}$) the transistor Tr13 has, as shown in Fig. 19.

[0143] In the transient response status, the gate-source voltage Vgs of the transistor Tr13 increases, as time passes, toward the threshold voltage Vth or the threshold voltage after the variation ($V_{th0} + \Delta V_{th}$). Thereafter, this voltage Vgs changes to converge to the threshold voltage Vth as shown by the characteristic lines ST1 and ST2 shown in Fig. 20. The transient response period Ttrs is set to be shorter than a period during which the voltage Vgs converges to the threshold voltage Vth.

[0144] Then, with regards to a change in the data line voltage per hour, an increase in the gate-source voltage Vgs is higher as the threshold voltage Vth has a lower absolute value. As the threshold voltage Vth has a higher absolute value, an increase in the gate-source voltage Vgs is lower. In the case of the threshold voltage Vth(L) close to the initial status, the variation ΔV_{th} is small and thus an increase in the voltage Vgs significantly changes (characteristic line ST1). When the variation ΔV_{th} is large on the other hand, an increase in the voltage Vgs gently changes (characteristic line ST2). In the example of Fig. 20, the characteristic lines ST1 and ST2 are used to detect the reference voltage Vref before the voltage Vgs converges to the threshold voltage Vth. After the detection, changes in the respective characteristic lines ST1 and ST2 can be identified to estimate, based on the changes thereof, the threshold voltages Vth(L) and Vth(H) as a converge voltage. As described above, the reference voltage Vref is a function of the transient response period Ttrs and the threshold voltage Vth of the transistor Tr13.

[0145] Next, the following section will describe a relation between the threshold voltage of the driving transistor Tr13 and the reference voltage Vref. The following example will assume, as in the example shown in Fig. 19, that the precharge voltage Vpre is -10V. The transient response period Ttrs is set to 15 μ sec.

[0146] The transistor Tr13 is set to have, as a driving capability, a constant K for calculating the saturated current Ids between the drain and the source ($=K \times (W/L) \times (V_{gs} - V_{th})^2$) of 7.5×10^{-9} and a ratio between the channel width W and the length L of 80/6.5. The resistance between the source and the drain of the selection transistor Tr12 is set to 13MO and a pixel content Cs+Cpix as a sum of the capacitor Cs and the pixel parasitic capacitance Cpix is set to 1pF. The parasitic capacitance Cpara of the data line Ld is set to 10pF and the wiring resistance Rdata of the data line Ld is set to 10kO.

[0147] In this case, the transistor Tr13 has a relation between the threshold voltage Vth (initial threshold voltage V_{th0} +threshold voltage change amount ΔV_{th}) and the reference voltage Vref having a characteristic shown in Fig. 21. Specifically, the lower the threshold voltage Vth is, the higher the reference voltage Vref is. The higher the threshold

voltage V_{th} is, the lower the reference voltage V_{ref} is. This characteristic is substantially linear and thus a relation between the reference voltage V_{ref} and the threshold voltage V_{th} can be represented by a linear function $y=a \cdot x+b$ as shown by the following formula (14). This slope "a" is substantially equals to "a" shown in the above-described formula (11). In the example of Fig. 21, the value of "a" is substantially 2. V_{ofst} represents the threshold voltage V_{th} (theoretical value) when the reference voltage V_{ref} is 0 that is a unique voltage value set based on verify conditions.

$$V_{th} = -a \cdot V_{ref} - V_{ofst} \quad (14)$$

[0148] In the writing operation, the data line L_d is applied with the compensated gradation level voltage V_{pix} . As shown in Fig. 19, the data line voltage sharply increases to subsequently converge toward the compensated gradation level voltage V_{pix} . Thus, in a row set to the selected status, the gate-source voltage V_{gs} depending on the compensated gradation level voltage V_{pix} is retained between the gate and the source of the transistor $Tr13$ (both ends of the capacitor C_s). The voltage calculator 144 adds and subtracts the original gradation level voltage V_{org} , the first compensation voltage $a \cdot V_{ref}$, and the second compensation voltage V_{ofst} to generate this compensated gradation level voltage V_{pix} . The original gradation level voltage V_{org} is set to a voltage value depending on the display data (data for brightness and color) in an initial status. In the initial status, the threshold voltage V_{th} does not vary. Thus, the compensated gradation level voltage V_{pix} can be represented by the following formula (15).

$$V_{pix} = V_{org} + V_{th} \quad (15)$$

[0149] When the formula (15) is substituted into the formula (14), the above-described formula (11) is obtained. The voltage calculator 144 can add and subtract the respective voltages based on the formula (11) to generate the compensated gradation level voltage V_{pix} having a value subjected to a compensation processing in accordance with the variation ΔV_{th} of the threshold voltage. When the organic EL element OLED does not emit light, it is preferred that the formula (15) is not used and the compensated gradation level voltage V_{pix} can be set to the power source voltage V_{cc} (=the second power source voltage V_{cce} of the light-emitting operation level).

[0150] Next, a specific structure of the data driver 14 for realizing the above-described method for driving a display apparatus will be described. As shown in Fig. 22, the data driver 14 mainly includes the gradation level voltage generator 142, the voltage converter 143, the voltage calculator 144, and the changing-over switches $SW1$ to $SW3$. The data line L_d has parasitic capacitance C_{para} and wiring resistance R_{data} .

[0151] The gradation level voltage generator 142 includes a digital-analog voltage converter V-DAC (hereinafter referred to as "DA converter"). In this embodiment, this DA converter V-DAC has a voltage conversion characteristic shown in Fig. 23. The DA converter V-DAC converts data for gradation level (digital signal) supplied from the display signal generation circuit 16 to an analog signal voltage. The converted analog signal voltage is the original gradation level voltage V_{org} . The DA converter V-DAC outputs this original gradation level voltage V_{org} to the voltage converter 143.

[0152] It is noted that, in the example of Fig. 23, the drain-source current I_{ds} of the transistor $Tr13$ substantially in proportional to a digital input gradation level. Thus, the organic EL element OLED has the light-emitting brightness substantially in proportional to the value of flowing current (or current density) and is displayed with gradation level linear with regard to the digital input.

[0153] The voltage converter 143 shown in Fig. 22 includes a plurality of voltage follower-type amplification circuits and a plurality of inverted amplification circuits. In the amplification circuit, a + side input terminal of an operational amplifier $OP1$ is connected to the data line L_d via the changing-over switch $SW2$. An output terminal of the operational amplifier $OP1$ is connected to a - side input terminal of the operational amplifier $OP1$.

[0154] In the inverted amplification circuit, the + side input terminal of the operational amplifier $OP2$ is connected to the reference voltage. The - side input terminal of the operational amplifier $OP2$ is connected, via the resistance $R1$, the output terminal of the operational amplifier $OP1$ and is connected, via the resistance $R2$, the output terminal of the operational amplifier $OP2$.

[0155] The amplification circuit having the operational amplifier $OP1$ retains the voltage level of a reference voltage V_{ref} . It is noted that the retention capacity C_f is a capacity to retain the voltage level of the reference voltage V_{ref} .

[0156] The inverted amplification circuit inverts the voltage polarity of the reference voltage V_{ref} . The inverted amplification circuit also amplifies, in accordance with a voltage amplification rate determined based on a ratio between the resistances $R2$ and $R1$ ($R2/R1$), the voltage ($-V_{ref}$) having an inverted polarity. The voltage $[-(R2/R1) \cdot V_{ref}]$ obtained after the amplification is the above-described first compensation voltage. The ratio $R2/R1$ corresponds to the slope "a" shown in the formula (14). The inverted amplification circuit also outputs the first compensation voltage $[-(R2/R1) \cdot V_{ref}]$ to the

voltage calculator 144.

[0157] The voltage calculator 144 includes an adder circuit. This adder circuit has the operational amplifier OP3 shown in Fig. 22. The + side input terminal of the operational amplifier OP3 is applied with the reference voltage via the resistance R. This + side input terminal is connected to an external input terminal of the second compensation voltage Vofst via another resistance R. On the other hand, the - side input terminal is connected to the output terminal of the operational amplifier OP2 via the resistance R. This side input terminal is connected to the DA converter V-DAC via another resistance R and is connected to the output terminal of the operational amplifier OP3 via another resistance R.

[0158] The voltage calculator 144 adds and subtracts the original gradation level voltage Vorg, the first compensation voltage $[-(R2/R1) \cdot V_{ref}]$ and the second compensation voltage Vofst to generate the compensated gradation level voltage Vpix. The voltage calculator 144 outputs this compensated gradation level voltage Vpix to the data line Ld via the changing-over switch SW1.

[0159] The respective changing-over switches SW1 to SW3 include a transistor switch. The respective changing-over switches SW1 to SW3 are turned ON or OFF based on the data control signal supplied from the controller 15 (any of switching control signals OUT, REF, PRE). This turns ON or OFF the connection between the data driver 14 (the voltage calculator 144, the voltage converter 143, an external input terminal of the precharge voltage Vpre) and the data line Ld.

(Method for driving display apparatus)

[0160] Next, a driving method that is characteristic for the display apparatus 1 will be described. As shown in Fig. 9, the respective display pixels PIX of Embodiment 1 are divided to a group provided at the upper zone of the display zone 11 and a group provided at the lower zone of the display zone 11. The display pixels PIX include in the respective groups are applied with independent power source voltages Vcc via different power source voltage lines Lv1 and Lv2, respectively. Thus, the display pixels PIX in a plurality of rows included in the respective groups simultaneously perform a light-emitting operation.

[0161] The following section will describe a timing at which the display pixels PIX operate in the driving method as described above. The following section will assume that the display zone 11 shown in Fig. 9 includes display pixels in 12 rows and the respective display pixels are divided to a group of the first to sixth rows (a group provided at the upper zone of the display zone 11) and a group of the seventh to twelfth rows (a group provided at the lower zone of the display zone 11). As shown in Fig. 24, First, the display pixels PIX of the respective rows are caused to sequentially perform the compensated gradation level voltage setting operation (precharge operation, transient response, reference voltage reading operation) and the writing operation. When the writing operation is completed, all display pixels PIX in the group are caused to simultaneously emit light with gradation level depending on the display data. This light-emitting operation is sequentially repeated for the respective groups. As a result, data for one screen is displayed on the display zone 11.

[0162] For example, the respective display pixels PIX of the group of the first to sixth rows are applied, via the first power source voltage line Lv1, with the power source voltage Vcc having a low potential ($=V_{ccw}$). Then, the compensated gradation level voltage setting operation, the writing operation, and the retention operation are repeatedly performed for the respective rows starting from the first row to the sixth row. With regards to the display pixels PIX of the respective rows, the voltage calculator 144 acquires, from the voltage converter 143, the first compensation voltage $a \cdot V_{ref}$ corresponding the threshold voltage Vth of to the driving transistor Tr13. The display pixels PIX are written with the compensated gradation level voltage Vpix. The display pixels PIX in a row for which the writing operation is completed are then subjected to the retention operation.

[0163] At a timing at which the writing operation to the display pixels PIX in the sixth row is completed, the power source driver 13 applies a high potential power source voltage $V_{cc}(=V_{cce})$ to the respective display pixels PIX via the first power source voltage line Lv1. As a result, based on gradation level depending on the display data (compensated gradation level voltage Vpix) written to the respective display pixels PIX, all display pixels PIX included in this group (the first to sixth rows) are caused to simultaneously emit light. The display pixels of this group continuously emit light until the display pixels PIX in the first row are set to the next compensated gradation level voltage Vpix. A period during which the display pixels of this group continuously emit light until the display pixels PIX in the first row are set to the next compensated gradation level voltage Vpix is the light-emitting period Tem of the first to sixth rows. It is noted that this driving method causes the display pixels PIX in the sixth row (the final row of the group of the upper zone) to emit light without performing the retention operation after the writing operation.

[0164] On the other hand, at a timing at which the writing operation to the respective display pixels PIX of the group of the first to sixth rows is completed, the power source driver 13 applies the power source voltage $V_{cc}(=V_{ccw})$ for the writing operation to the respective display pixels PIX in the group of the seventh to twelfth rows via the second power source voltage line Lv2. Then, operations substantially the same as the above-described operations for the group of the first to sixth rows (the compensated gradation level voltage setting operation, the writing operation, and the retention operation) are repeated for the respective rows starting from the seventh row to the twelfth row. It is noted that, during these operations, display pixels in the group of the first to sixth rows continuously emit light.

[0165] At a timing at which the writing operation to the display pixels PIX in the twelfth row is completed, the power source driver 13 applies the power source voltage $V_{cc}(=V_{cce})$ for the light-emitting operation to the respective display pixels PIX. As a result, the display pixels PIX in six rows of this group (the seventh to twelfth rows) are caused to emit light simultaneously. Then, at a timing at which the writing operation to the display pixels PIX in all rows of each group is completed, all display pixels PIX in the group can be caused to emit light simultaneously. During display pixels in the respective rows in each group are set with a compensated gradation level voltage and during the writing current I_{ds} is flowing therein, the respective display pixels in the group can be controlled not to emit light.

[0166] In the example of Fig. 24, the display pixels PIX in twelve rows are divided to two groups and a control is performed by which the data driver 14 causes the respective groups to emit light with different timings. Thus, a ratio between one frame period T_{fr} and a period during which black display is caused by a no-light-emitting operation (hereinafter referred to as "black insertion rate") can be set to 50%. Generally, in order to allow a person to clearly visually recognize video without feeling indistinctiveness or blur, this black insertion rate should be 30% or more. Thus, this driving method can display data with a relatively favorable display picture quality.

[0167] It is noted that display pixels in the respective rows may be also divided to three or more groups instead of two groups. Rows included in the respective groups are not limited to continuous rows and also may be divided to a group of odd-numbered rows and a group of even-numbered rows. The power source voltage line L_v also may be connected to the respective rows instead of being connected to divided groups. In this case, the respective power source voltage lines can be independently applied with the power source voltage V_{cc} so that the display pixels PIX in the respective rows can individually emit light.

[0168] As described above, according to Embodiment 1 of the present invention, during the writing period T_{wrt} of display data, the compensated gradation level voltage V_{pix} is directly applied between the gate and the source of the driving transistor Tr_{13} and a desired voltage is retained in the capacitor C_s . This compensated gradation level voltage V_{pix} has a voltage value for which the display data and the variation of the element characteristic of the driving transistor are compensated. As a result, the light emission driving current I_{em} flowing in the light-emitting element (organic EL element OLED) can be controlled based on the compensated gradation level voltage V_{pix} and the light-emitting element can emit light with desired brightness of the gradation level. Specifically, voltage specification (voltage application) can be used to control the display gradation level of the light-emitting element.

[0169] Thus, the gradation data signal depending on the display data (compensated gradation level voltage) can be written, within the predetermined selection period T_{sel} , to the respective display pixels in a quick and secure manner. In this manner, the display apparatus 1 of the present invention can suppress insufficient writing of display data and can allow display pixels to emit light with preferred gradation level depending on the display data.

[0170] It is noted that Embodiment 1 can use the voltage specification (voltage application) to control the display gradation level of the light-emitting element for any of a case where the display zone has a larger size, a case where the display zone has a smaller size, a case where data of a low gradation level is displayed, and a case where current flowing in display pixels in a small display zone is small. In this regard, the gradation level control method of the present invention is advantageous over a method for using current specification for flowing current depending on display data to perform a writing operation (or to retain a voltage depending on display data) to control a gradation level.

[0171] According to Embodiment 1, prior to writing display data to the pixel driving circuit DC owned by the display pixel PIX, the first compensation voltage is acquired for which the original gradation level voltage V_{org} is compensated in accordance with the variation in the threshold voltage V_{th} of the driving transistor Tr_{13} . Thereafter, the writing operation is used to generate a gradation data signal (compensated gradation level voltage V_{pix}) compensated based on this compensation voltage and an unique voltage value (the second compensation voltage) set based on the verify conditions to apply the gradation data signal to the light-emitting EL element OLED. As a result, the variation in the threshold voltage is compensated and the respective display pixels (light-emitting elements) emit light with appropriate brightness of the gradation level depending on the display data. This can suppress the dispersion of the light-emitting characteristics of the respective display pixels PIX.

gradation data signal According to Embodiment 1, a gradation data signal (compensated gradation data signal) outputted from the data driver 14 is a voltage signal. Thus, even when the transistor Tr_{13} has the drain-source current I_{ds} having a small value during the writing operation, the gate-source voltage V_{gs} depending on this current I_{ds} can be quickly set. This is different from a method for directly controlling the current value of the drain-source current I_{ds} of the transistor Tr_{13} to control the gradation level of the pixel. Thus, during the selection period T_{sel} , the compensated gradation level voltage V_{pix} can be written between the gate and source of the transistor Tr_{13} and the capacitor C_s . This eliminates a need in the structure of the pixel driving circuit DC structure for a memorization means (e.g., frame memory) for storing compensation data for generating the compensated gradation level voltage V_{pix} for example.

[0172] According to the driving method of Embodiment 1, even when a plurality of display pixels have different threshold voltages V_{th} , the respective threshold voltages V_{th} are estimated based on the reference voltage V_{ref} to compensate the respective threshold voltages V_{th} . As a result, a plurality of pixels can be caused to operate with an identical light-emitting characteristic (e.g., identical brightness). For example, it is assumed that the display pixel A has the transistor

Tr13 having a threshold voltage V_{th_A} and the display pixel B has the transistor Tr13 having a threshold voltage V_{th_B} . Based on the formula (14), the threshold voltage of the driving transistor Tr13 is compensated. It is also assumed that current flowing between the drain and source of the respective display pixels is I_A and I_B . In the saturated zone, I_A and I_B are represented by the following formulae (16) and (17), respectively. It is noted that "K" in the formulae (16) and (17) represents a coefficient.

$$I_A = K \{ (V_{org} + V_{th_A}) - V_{th_A} \}^2 = K \cdot \{ V_{org} \}^2 \quad (16)$$

$$I_B = K \{ (V_{org} + V_{th_B}) - V_{th_B} \}^2 = K \cdot \{ V_{org} \}^2 \quad (17)$$

[0173] As described above, this method can compensate not only an influence by the threshold voltage change amount ΔV_{th} of the driving transistor Tr13 but also an influence by the dispersion of threshold value characteristics among the respective transistors. Thus, according to Embodiment 1, even when the threshold voltage of the display pixel A is different from the threshold voltage of the display pixel B in an initial status in which there is substantially no variation ΔV_{th} in the threshold voltage V_{th} , variation in the threshold voltages of the respective driving transistors Tr13 owned by the respective display pixels is compensated to provide a uniform display characteristic.

(Embodiment 2)

[0174] In the voltage specification-type gradation level control method according to Embodiment 1, the original gradation level voltage V_{org} is compensated based on the reference voltage V_{ref} to generate the compensated gradation level voltage V_{pix} . Then, this compensated gradation level voltage V_{pix} is applied to the respective display pixels PIX. The gradation level control method shown in Embodiment 1 is based on an assumption that an influence by the capacity component parasitic on the display pixel PIX can be sufficiently suppressed by the capacitor C_s connected between the gate and the source of the driving transistor Tr13. This method is also based on an assumption that, even when the power source voltage V_{cc} is switched from the writing level to the light-emitting level, there is no variation in the writing voltage retained in the capacitor C_s .

[0175] However, a mobile electronic apparatus such as a mobile phone frequently requires a smaller panel size and a fine picture quality. Such a requirement may prevent the storage capacitor of the capacitor C_s from being set to be higher than the parasitic capacitance of the display pixel PIX. In this case, when variation is caused in a writing voltage charged in the capacitor C_s at the start of the light-emitting operation, this causes variation in the gate-source voltage V_{gs} of the driving transistor Tr13. This causes variation in the light emission driving current I_{em} to prevent the respective display pixels from emitting light with brightness depending on display data.

[0176] In order to avoid this problem, instead of using the compensated gradation level voltage V_{pix} to compensate the variation in the threshold voltage V_{th} of the driving transistor Tr13, a value of the light emission driving current I_{em} may be compensated. The following section will describe the display apparatus 1 of Embodiment 2 not forming part of the present invention for performing the operation as described above.

[0177] First, the structure of the display apparatus 1 of Embodiment 2 will be described. The display apparatus 1 of Embodiment 2 has the same basic structure as those shown in Fig. 9 and Fig. 10. Specifically, as shown in Fig. 25, the display pixel PIX of Embodiment 2 is substantially the same as that of Embodiment 1. The pixel driving circuit DC owned by the display pixel PIX includes: the driving transistor Tr13 connected to the light-emitting element OLBD in series; the selection transistor Tr12; and the retention transistor Tr11 for diode connection of the driving transistor Tr13.

[0178] In Embodiment 2, the data driver (display driving apparatus) 14 has the structure shown in Fig. 25 instead of the structure shown in Fig. 10.

[0179] As in Embodiment 1, the gradation level voltage generator 142 of Embodiment 2 generates the original gradation level voltage V_{org} to output the original gradation level voltage V_{org} . With regards to this original gradation level voltage V_{org} , the unique voltage characteristic of the pixel driving circuit (driving transistor Tr13) is compensated in order to allow a light-emitting element to emit light with desired brightness of the gradation level.

[0180] The data driver 14 (display driving apparatus) includes, instead of the voltage converter 143 shown in Fig. 10, an adder section (voltage reader) 146 and a converter 147. The data driver 14 also includes, instead of the voltage calculator 144 shown in Fig. 10, an inversion calculator (compensated gradation data signal generator) 148. The data driver 14 also includes a changing-over switch SW4. It is noted that the adder section 146 and the changing-over switch SW2 will be collectively called as "voltage reader 149". The combination of the adder section 146, the converter 147, the inversion calculator 148, and the changing-over switch SW4 is provided in an amount of "n" in the data line L_d of each column, respectively.

[0181] The adder section (voltage reader) 146 applies the predetermined precharge voltage V_{pre} to the data line L_d . After the predetermined transient response period T_{trs} (natural relaxation period), the adder section 146 reads the reference voltage V_{ref} . The adder section 146 outputs, to the converter 147, a voltage ($V_{ref}+V_{ofst}$) obtained by adding a previously set OFFSET voltage V_{ofst} to the reference voltage V_{ref} .

[0182] The converter 147 multiplies the voltage ($V_{ref}+V_{ofst}$) outputted from the adder section 146 with the predetermined coefficient a . This coefficient a is used to estimate the threshold voltage V_{th} after the variation of the characteristic of the transistor Tr_{13} . After the multiplication, the converter 147 outputs the resultant voltage $a(V_{ref}+V_{ofst})$ to the inversion calculator 148. It is noted that the voltage $a(V_{ref}+V_{ofst})$ generated by the converter 147 can be represented, as shown in the following formula (21), by a predetermined multiple β of the threshold voltage V_{th} . It is noted that the " βV_{th} " will be called as "compensation voltage" hereinafter.

$$\beta V_{th}=a \cdot (V_{ref}+V_{ofst}) \quad (21)$$

[0183] The inversion calculator 148 adds the original gradation level voltage V_{org} from the gradation level voltage generator 142 to the compensation voltage βV_{th} from the converter 147 to generate the compensated gradation level voltage (compensated gradation data signal) V_{pix} . When the gradation level voltage generator 142 includes a DA converter at this stage, the inversion calculator 148 adds the original gradation level voltage V_{org} to the compensation voltage βV_{th} in the form of an analog signal. Then, the inversion calculator 148 charges the generated compensated gradation level voltage V_{pix} in the capacitor C_s via the data line L_d (writing operation). It is noted that Embodiment 2 also allows, in order to flow writing current from the data line L_d into the data driver 14 during the writing operation to the display pixel PIX , the inversion calculator 148 to set the compensated gradation level voltage V_{pix} to a negative polarity. Then, the compensated gradation level voltage V_{pix} is set to satisfy the following formula (22). It is noted that, in the formula (22), $\beta > 1$, original gradation level voltage $V_{org} > 0$, and $V_{in} < 0$ are established.

$$V_{pix}=-V_{in}=-V_{org}-\beta V_{th} \quad (22)$$

[0184] The changing-over switch SW_4 is connected between the output terminal of the inversion calculator 148 and a power source terminal for applying the black gradation level voltage V_{zero} . It is noted that the changing-over switch SW_4 desirably has resistance and capacity equal to those of the respective changing-over switches SW_1 to SW_3 . The changing-over switch SW_4 is turned ON or OFF based on the data control signal from the controller 15. Based on this, the changing-over switch SW_4 controls the application to the data line L_d of the black gradation level voltage V_{zero} .

[0185] When the gradation level are the 0th gradation level (or when the organic EL element OLED does not emit light), the gradation level voltage generator 142 does not output the original gradation level voltage V_{org} . Then, the black gradation level voltage V_{zero} is applied to the output terminal of the inversion calculator 148 via the changing-over switch SW_4 . The formula (22) can be represented by the following formula (23). Specifically, the display driving apparatus 14 of Embodiment 2 has the above-described structure to compensate the unique voltage characteristic of the pixel driving circuit (driving transistor Tr_{13}) and to generate the compensated gradation level voltage V_{pix} for causing the light-emitting element OLED to emit light with desired brightness of the gradation level voltage V_{pix} to the capacitor C_s .

$$V_{pix}=-V_{in}=V_{zero}=V_{th} \quad (23)$$

(Method for driving display apparatus)

[0186] Next, a method for driving the display apparatus 1 of Embodiment 2 will be described. As in Embodiment 1, Embodiment 2 also firstly performs an operation for setting a compensated gradation level voltage. The adder section 146 applies the predetermined precharge voltage V_{pre} to the data lines L_d on the respective columns. As a result, the adder section 146 flows the precharge current I_{pre} from the power source voltage line L_v into the data lines L_d of the respective rows. Thereafter, the adder section 146 stops the application of the precharge voltage V_{pre} . After the stoppage, after the transient response period T_{trs} , the adder section 146 reads the reference voltage $V_{pre}(t_0)$. As in Embodiment 1, this transient response period T_{trs} is set to be shorter than a period during which the gate-source voltage V_{gs} of the transistor Tr_{13} converges to the threshold voltage after the variation ($V_{th}+\Delta V_{th}$).

[0187] Next, the inversion calculator 148 compensates the original gradation level voltage V_{org} based on the com-

compensation voltage BV_{th} set based on the reference voltage V_{ref} . The inversion calculator 148 generates the compensated gradation level voltage V_{pix} shown in the formula (22) to apply the compensated gradation level voltage V_{pix} to the respective data lines L_d . Then, the writing current I_{wrt} based on this compensated gradation level voltage V_{pix} flows in the respective display pixels PIX . This writing current I_{wrt} corresponds to the drain-source current I_{ds} of the transistor $Tr13$.

[0188] Thus, Embodiment 2 sets, in order to compensate the writing current I_{wrt} , the voltage V_{gs} so that gate-source voltage V_{gs} of the driving transistor $Tr13$ satisfy the following formula (24). In the formula (24), V_{d0} represents a voltage among the voltages V_{gs} applied to the gate and the source of the transistor $Tr13$ during the writing operation that changes in accordance with the specified gradation level (digital bit). In the formula (24), γV_{th} represents a voltage depending on the threshold voltage V_{th} . This V_{d0} corresponds to the first compensation voltage and γV_{th} corresponds to the second compensation voltage. It is noted that the constant γ in the formula (24) is defined by the following formula (25).

$$V_{gs}=0-(-V_d)=V_{d0}+\gamma V_{th} \quad (24)$$

$$\gamma=1+(C_{gs11}+C_{gd13})/C_s \quad (25)$$

[0189] By satisfying the formula (24), Embodiment 2 can use the compensated gradation level voltage V_{pix} to compensate the light emission driving current I_{em} flowing from the transistor $Tr13$ into the organic EL element OLED during the light-emitting operation. Embodiment 1 is different from Embodiment 2 in that the compensated gradation level voltage V_{pix} had compensated the variation in the threshold voltage V_{th} of the transistor $Tr13$. It is noted that C_{gs11} in the formula (25) is a parasitic capacitance between the contact point $N11$ and the contact point $N13$ as shown in Fig. 27A. C_{gd13} represents a parasitic capacitance between the contact point $N11$ and the contact point $N14$, C_{para} represents a parasitic capacitance of the data line L_d , and C_{pix} represents a parasitic capacitance of the organic EL element OLED.

[0190] In the above-described a method for driving a display apparatus, the shift from a writing operation to a light-emitting operation causes the selection signal S_{sel} applied to the selection line L_s to be switched from the a high level to a low level and also causes the power source voltage V_{cc} applied to the power source voltage line L_v to be switched from a low level to a high level. This causes a risk of variation in the gate-source voltage (a voltage retained in the capacitor C_s) V_{gs} of the driving transistor $Tr13$. In Embodiment 2, this voltage V_{gs} is set to satisfy the formula (24) to compensate the writing current I_{wrt} .

[0191] Then, the gate-source voltage V_{gs} for specifying the light emission driving current I_{em} flowing in the organic EL element OLED during a light-emitting operation is introduced. It is noted that the following section assumes that the power source voltage $V_{cc}(=V_{ccw})$ during the writing operation is a ground potential GND. As shown in Fig. 27A, during the writing operation, the display pixel PIX is applied with the selection signal S_{sel} of the selected level (high level) ($=V_{sh}$) and the power source voltage $V_{cc}(=V_{ccw}=GND)$ for a writing operation. The inversion calculator 148 applies the compensated gradation level voltage $V_{pix}(=-V_{in})$ having a negative polarity lower than that of the power source voltage $V_{ccw}(=GND)$ to the display pixel PIX .

[0192] As a result, the transistor $Tr11$ and selection transistor $Tr12$ are turned ON and the gate of the driving transistor $Tr13$ (contact point $N11$) is applied with the power source voltage $V_{ccw}(=GND)$ and the source (contact point $N12$) of the transistor $Tr13$ is applied with the compensated gradation level voltage V_{pix} having a negative polarity. As a result, a potential difference is caused between the gate and the source of the transistor $Tr13$ to turn ON the transistor $Tr13$. Then, the writing current I_{wrt} flows from the power source voltage line L_v applied with the power source voltage V_{ccw} into the data line L_d . The V_{gs} (writing voltage V_d) depending on the value of this writing current I_{wrt} is retained in the capacitor C_s formed between the gate and the source of the transistor $Tr13$.

[0193] It is noted that $C_{gs11'}$ shown in Fig. 27A is an effective parasitic capacitance that is caused between the gate and the source of the transistor $Tr11$ when the gate voltage (selection signal S_{sel}) of the transistor $Tr11$ changes from a high level to a low level. C_{gd13} is a parasitic capacitance caused between the gate and the drain of the transistor $Tr13$ when a source-drain voltage of the driving transistor $Tr13$ is in a saturated zone.

[0194] On the other hand, as shown in Fig. 27B, during the light-emitting operation, the selection line L_s is applied with the selection signal S_{sel} of the voltage ($-V_{sl}<0$) of the not-selected level (low level) and is applied with the power source voltage V_{cc} for light emission having a high potential ($=V_{cce}$; 12-15V for example). The selection transistor $Tr12$ is turned OFF to block the application by the inversion calculator 148 of the compensated gradation level voltage $V_{pix}(=-V_{in})$ to the data line L_d .

[0195] By applying the election signal S_{sel} having the voltage V_{sel} to the selection line L_s , the transistor $Tr11$ is turned OFF to block the application of the power source voltage V_{cc} to the gate of the transistor $Tr13$ (contact point $N11$) and to block the application of the compensated gradation level voltage V_{pix} to the source of the transistor $Tr13$ (contact

point N12). Then, a potential difference ($0 - (-V_d) = V_d$) caused between the gate and the source of the transistor Tr13 during a writing operation is retained in the capacitor Cs. Thus, the gate-source potential difference V_d is maintained and the transistor Tr13 maintains an ON status. As a result, the light emission driving current I_{em} in accordance with the gate-source voltage $V_{gs}(=V_d)$ flows from the power source voltage line L_v to the organic EL element OLED. Then, the organic EL element OLED emits light with brightness depending on a value of this current I_{em} .

[0196] It is noted that a voltage V_{oel} at the contact point N12 shown in Fig. 27B represents a voltage of the organic EL element OLED during the light-emitting operation (hereinafter referred to as "light-emitting voltage"). C_{gs11} is a parasitic capacitance caused between the gate and the source when the gate voltage of the transistor Tr11 (selection signal Ssel) has a low level ($-V_{sl}$). It is noted that a relation between C_{gs11}' of Fig. 27A and C_{gs11} of Fig. 27B is represented by the following formula (26). It is noted that the voltage V_{shl} in the formula (26) represents a potential difference ($V_{sh} - (-V_{sl})$) between the high level (V_{sh}) and the low level ($-V_{sl}$) of the selection signal Ssel.

$$C_{gs11}' = C_{gs11} + (1/2) \times C_{ch11} \times V_{sh} / V_{shl} \quad (26)$$

[0197] At the shift from the writing operation to the light-emitting operation, the voltage levels of the selection signal Ssel and the power source voltage V_{cc} are switched. Then, during the writing operation, the voltage $V_{gs}(=V_d)$ retained between the gate and the source of the transistor Tr13 varies in accordance with the formula (27). In the formula (27), c_{gd} , c_{gs} , and c_{gs}' represent values obtained by normalizing the respective parasitic capacitances C_{gd} , C_{gs} , and C_{gs}' by the capacity of the capacitor and $c_{gd} = C_{gd}/C_s$, $c_{gs} = C_{gs}/C_s$, and $c_{gs}' = C_{gs}'/C_s$ are established. It is noted that a characteristic according to which the voltage V_{gs} varies in accordance with a change in the voltage applied to the pixel driving circuit DC is called as "a voltage characteristic unique to the pixel driving circuit DC".

$$V_{gs} = \{V_d - (c_{gs} + c_{gd}) \cdot V_{oel}\} / (1 + c_{gs} + c_{gd}) + (c_{gd} \cdot V_{cce} - c_{gs}' \cdot V_{shl}) / (1 + c_{gs} + c_{gd}) \quad (27)$$

[0198] The formula (27) is introduced by applying "law of conservation of charge amount" before and after the switching of a control voltage (selection signal Ssel, power source voltage V_{cc}) applied to the pixel driving circuit DC. As shown in Fig. 28A and Fig. 28B, a voltage applied to one end of the capacity components (capacities C_1 and C_2) connected in series is changed from V_1 to V_1' . Then, the charge amounts Q_1 and Q_2 of the respective capacity components before the change and the charge amounts Q_1' and Q_2' of the respective capacity components after the change can be represented by the following formulae (28a) to (28d).

$$Q_1 = C_1(V_1 - V_2) \quad (28a)$$

$$Q_2 = C_2 V_2 \quad (28b)$$

$$Q_1' = C_1(V_1' - V_2') \quad (28c)$$

$$Q_2' = C_2 V_2' \quad (28d)$$

[0199] Based on the formulae (28a) to (28d), $-Q_1 + Q_2 = -Q_1' + Q_2'$ is calculated, the potentials V_2 and V_2' at a connection point of the capacity components C_1 and C_2 is represented by the following formula (29).

$$V_2' = V_2 - \{C_1 / (C_1 + C_2)\} \cdot (V_1 - V_1') \quad (29)$$

[0200] Next, the following section will describe the potential V_{n11} at the gate (contact point N11) of the transistor Tr13 when the relations shown in the above-described formulae (28a) to (28d) and (29) are applied to the display pixel PIX (the pixel driving circuit DC and the organic EL element OLED) and the selection signal Ssel is switched.

[0201] In this case, the equivalent circuits shown in Figs. 26, 28A, and 28B can be substituted by the equivalent circuits shown in Figs. 29A and 30B. In the example of Fig. 29A, the selection line Ls is applied with the selection signal Ssel of the selected level (high level voltage Vsh) and the power source voltage line Lv is applied with the power source voltage Vcc(=Vccw) having a low potential. In the example of Fig. 29B, the selection line Ls is applied with the selection signal Ssel of the not-selected level (low level voltage Vsl). The power source voltage line Lv is applied with the power source voltage Vcc(=Vccw) having a low potential.

[0202] During the application of the selection signal Ssel of the selected level (Vsh), charge amounts retained in the respective capacity components Cgs11, Cgs11b, Cds13, and Cpix and the capacitor Cs shown in Fig. 29A are represented by the following formulae (30a) to (30d). When the selection signal Ssel of the not-selected level (Vsl) is applied, charge amounts retained in the respective capacity components Cgs11, Cgs11b, Cds13, and Cpix and capacitor Cs shown in Fig. 29B are represented by the following formulae (30e) to (30h). The capacity component Cgs11b shown between the contact points N11 and N13 shown in Fig. 29B is the gate-source parasitic capacitance Cgso11 other than the in-channel capacity of the transistor Tr11. The capacity component Cgs11b between the contact points N11 and N13 shown in Fig. 29A is a sum of a value of (Cgs1 = Cch11/2 + Cgs11) obtained by multiplying the channel capacity Cch11 of the transistor Tr11 with 1/2 and Cgs11(=Cgso11).

$$Q1=0 \quad (30a)$$

$$Q2=Cs \cdot Vd \quad (30b)$$

$$Q3=-Cpix \cdot Vd \quad (30c)$$

$$Q4=Cgs11b \cdot Vsh \quad (30d)$$

$$Q1'=Cgd13 \cdot V1 \quad (30e)$$

$$Q2'=Cs \cdot (V - V1) \quad (30f)$$

$$Q3'=-Cpix \cdot V \quad (30g)$$

$$Q4'=Cgs11 \cdot Vsh \cdot (V1 - Vsl) \quad (30h)$$

[0203] When the law of conservation of charge amount is applied in the examples of Fig. 29A and Fig. 29B, a relation of the respective charges at the contact point N11 and at the contact point N12 are represented by the following formulae (31a) and (31b).

$$-Q1+Q2-Q4=-Q1'+Q2'-Q4' \quad (31a)$$

$$-Q2+Q3=-Q2'+Q3' \quad (31b)$$

[0204] When the formulae (31a) to (31b) are applied to the above-described formula (30a) to (30d), the potential Vn11 at the contact point N11 and the potential Vn12 at the contact point N12 are represented by the following formulae (32a) and (32b). It is noted that Cgs11' and D shown in the formulae (32a) and (32b) are defined by the following formulae (33a) and (33b), respectively.

$$V_{n11} = -V_1 = -(C_{gs11}' \cdot C_{pix} + C_{gs11}' \cdot C_s) \cdot V_{shl} / D \quad (32a)$$

$$V_{n12} = -V = -V_d - (C_{gs11}' \cdot C_s) \cdot V_{shl} / D \quad (32b)$$

$$C_{gs11}' = C_{gs11} + (C_{ch11}' \cdot C_s) / (2 \cdot V_{shl}) \quad (33a)$$

$$D = C_{gd13} \cdot C_{pix} + C_{gd13} \cdot C_s + C_{gs11} \cdot C_{pix} + C_{gs11} \cdot C_s + C_s \cdot C_{pix} \quad (33b)$$

[0205] The following section will describe a case where the method for introducing the potential as described above are applied to the respective steps from the writing operation to the light-emitting operation according to Embodiment 2 and the method for driving the display apparatus 1 in Embodiment 2. The method for driving the display apparatus 1 of Embodiment 2 is identical as that shown in the example of Fig. 11 and includes a selection step, a not-selected status switching step, a not-selected status retention step, a power source voltage switching step, and a light-emitting step.

[0206] Specifically, in Embodiment 2, the selection step is a step to send the selection signal Ssel of the selected level to the display pixel PIX to select the display pixel PIX to write a voltage in accordance with the display data to the capacitor Cs owned by the display pixel PIX. The not-selected status switching step is a step to cause the respective display pixels PIX selected in the selection step to be in a not-selected status. The not-selected status retention step is a step in which a capacitor Cs is retained in the capacitors Cs of the display pixels PIX caused to be in a not-selected status by the switching step. The power source voltage switching step is a step in which the power source voltage Vcc applied to the driving transistor Tr13 connected to the capacitor that has retained the charging voltage in the not-selected status is switched from the writing operation level (low potential) to the light-emitting operation level (high potential). The light-emitting step is a step in which a light-emitting element is caused to emit light with brightness depending on display data.

[0207] First, the following section will describe a voltage change at each point when the selection step shifts to the not-selected status switching step. Before the shift, as shown in Fig. 30A, the transistor Tr11 and the transistor Tr12 are ON by the application of the selection signal (Vsh) of a high potential and the writing current Iwrt flows between the drain and the source of the transistor Tr13. The contact point N11 has a potential of Vccw (ground potential) and the contact point N12 has a potential of -Vd.

[0208] When the selection signal Ssel of the not-selected level is applied to the transistor Tr11 and is applied to the transistor Tr12 in this status, the transistor Tr11 and the transistor Tr12 are switched from ON to OFF as shown in Fig. 30B. It is defined that the contact point N11 after the switching has a potential of -V1 and the contact point N12 after the switching has a potential of -V. When the selection signal Ssel is switched from a positive potential of high level (Vsh) to a negative potential of a low level (-Vsl), the gate-source voltage Vgs' of the driving transistor Tr13 changes by ΔV_{gs} from Vd. Then, the voltage Vgs' after the switching (writing voltage (i.e., a potential difference between the potential Vn11 of the contact point N11 and the potential Vn12 of the contact point N12)) is represented by the following formula (34).

$$\begin{aligned} V_{gs}' &= V_{n11} - V_{n12} = -V_1 - (-V) = V - V_1 \\ &= V_d - (C_{gs11}' \cdot C_{pix} / D) \cdot V_{shl} = V_d - \Delta V_{gs} \end{aligned} \quad (34)$$

[0209] This voltage shift ΔV_{gs} is represented by $C_{gs11}' \cdot C_{pix} \cdot V_{shl} / D$. The capacity component Cs' between the contact points N11 and N12 at the not-selected switching step is a parasitic capacitance component formed at a part other than the gate-source capacity of the transistor Tr13. In the formulae (32a), (32b), (33a), and (33b), "Cs" is a sum of the capacity component Cs', the gate-source voltage parasitic capacitance Cgso13 other than the in-channel capacity of the transistor Tr13, and the in-channel gate-source capacity of the transistor Tr13 in the saturated zone. This in-channel gate-source capacity is 2/3 of the channel capacity Cch1 of the transistor Tr13. Thus, Cs shown in formula (32a), (32b), (33a), (33b) can be calculated as shown below.

$$C_s = C_s' + C_{gs013} + (2/3) \cdot C_{ch13}$$

[0210] In the saturated zone, the in-channel gate-drain capacity can be assumed as 0. Thus, only C_{gd13} is a gate-drain capacity C_{gs013} other than the in-channel capacity of the transistor $Tr13$. In the formula (34), C_{gs11}' is a sum of the gate-source parasitic capacitance C_{gs011} other than the in-channel capacity of the transistor $Tr11$ and the in-channel gate-source capacity of the transistor $Tr11$ when $V_{ds}=0$. This in-channel gate-source capacity is an integration value of 1/2 of the channel capacity C_{ch11} of the transistor $Tr11$ and a voltage ratio (V_{sh}/V_{shl}) of the selection signal S_{sel} . Specifically, C_{gs11}' shown in formula (34) can be represented as shown below.

$$C_{gs11}' = C_{gs011} + C_{ch11} \cdot V_{sh} / 2V_{shl}$$

[0211] Next, a voltage change in the step for retaining the not-selected status of the display pixel PIX (not-selected status retention step) will be described. As shown in Fig. 31A, when the selection step (writing operation) shifts to the not-selected status, the transistor $Tr13$ maintains an ON status based on the voltage V_{gs}' retained between the gate and the source (capacity component C_s'). Then, the contact point $N12$ has a potential lower than that of the power source voltage $V_{cc}(=V_{ccw})$ and the drain-source current I_{ds} flows in the transistor $Tr13$. As shown in Fig. 31B, the current I_{ds} flowing in the transistor $Tr13$ causes the potential at the contact point $N12$ to increase to 0.

[0212] The drain voltage and the source voltage change until there is no different between the drain voltage of the transistor $Tr13$ (the potential of the contact point $N14$) and the source voltage (the potential of the contact point $N12$). A time required for this change is dozen microseconds. The change in the source potential causes the gate potential $V1'$ of the transistor $Tr13$ to change from the formulae (32a), (32b), (33a), and (33b) to a relation shown in the following formula (35).

$$V1' = \{C_s / (C_{gs11} + C_{gd13}' + C_s'')\} \cdot V$$

$$- \{(C_{gs11} + C_{gd13} + C_s) / (C_{gs11} + C_{gd13}' + C_s'')\} \cdot V1 \quad (35)$$

[0213] It is noted that C_s'' shown in formula (35) represents a capacity obtained by adding the above-described C_s' and C_{gs013} to 1/2 of the in-channel gate-source capacity C_{sh13} of the transistor $Tr13$ when $V_{ds}=0$, as shown in the formula (36a). In the formula (35), C_{gd13}' is a sum of the above-described C_{gd13} and 1/2 of the in-channel gate-source capacity C_{ch13} of the transistor $Tr13$ when $V_{ds}=0$. Specifically, C_{gd13}' is represented by the following formula (36b).

$$C_s'' = C_s' + C_{gs013} + C_{ch13}/2 = C_s - C_{ch13}/6 \quad (36a)$$

$$C_{gd13}' = C_{gd13} + C_{ch13}/2 \quad (36b)$$

[0214] In the formula (35), $-V1$ and $V1'$ are not $-V1$ and $V1'$ shown in Fig. 28 and are the potential ($-V1$) of the contact point $N11$ in Fig. 31A and the potential ($V1'$) of the contact point $N11$ in Fig. 31B, respectively. In the not-selected status retention step, the capacity component C_{gd13}' between the contact points $N11$ and $N14$ shown in Fig. 31B is a sum of the gate-drain capacity C_{gs013} other than the in-channel capacity of the transistor $Tr13$ and 1/2 of the channel capacity C_{ch13} of the transistor $Tr13$. Specifically, capacity component C_{gd13}' can be represented as shown below.

$$C_{gd13}' = C_{gd013} + C_{ch13}/2 = C_{gd13} + C_{ch13}/2$$

[0215] Next, the following section will describe a voltage change at each point when the not-selected status retention step shifts to the power source voltage switching step and the power source voltage switching step shifts to the light-emitting step. As shown in Fig. 32A, the drain-source potential difference of the transistor $Tr13$ is 0 in the not-selected status retention step to prevent the drain-source current I_{ds} from flowing. As shown in Fig. 32B, when the not-selected status retention step shifts to the power source voltage switching step, the power source voltage V_{cc} is switched from the low potential (V_{ccw}) to the high potential (V_{cce}). When the power source voltage switching step shifts to the light-

emitting step, the light emission driving current I_{em} flows in the organic EL element OLED via the transistor Tr13 as shown in Fig. 32C.

[0216] First, a case will be described where the not-selected status retention step shifts to the power source voltage switching step. During the shift, the drain-source voltage of the transistor Tr13 shown in Fig. 32A is closer to the potential 0. Thereafter, the power source voltage V_{cc} in the power source voltage switching step is switched from the low potential (V_{ccw}) to the high potential (V_{cce}). Thus, the potential V_{n11} of the gate (contact point N11) of the transistor Tr13 and the potential V_{n12} of the source (contact point N12) increase. The then potential V_{n11} is represented by the formula (37a) and then potential V_{n12} are represented by the formula (37b). It is noted that V_1'' and V'' are the potential V_{n11} of the contact point N11 and the potential V_{n12} of the contact point N12 shown in Fig. 32B, respectively.

$$V_{n11}=V_1''=\{1+C_{ch13}\cdot(3C_s+2C_{pix})/6D\}V'+(C_{gd13}\cdot C_{pix}+C_{gd13}\cdot C_s)\cdot V_{cce}/D \quad (37a)$$

$$V_{n12}=V''=C_{gd13}\cdot C_s\cdot V_{cce}/D+C_{ch13}\cdot(C_{gs11}+C_{gd13}+3C_s)/ \quad (37b)$$

[0217] Furthermore, the light-emitting step switches the power source voltage. Thus, the potential V_1c (the potential V_{n11} of the contact point N11 in the example of Fig. 32C) caused in the gate of the transistor Tr13 (contact point N11) is represented by the following formula (38).

$$V_{n11}=V_1c=V_1''+C_s\cdot(V_{pix}-V'')/(C_{gd13}+C_{gs11}+C_s) \quad (38)$$

[0218] The respective voltages shown in the above-described formulae (34), (35), (37a), (37b), and (38) are all rewritten to voltage signs in the not-selected status switching step. Thus, the gate-source voltage V_{gs} of the driving transistor Tr13 can be represented by the following formula (39).

$$V_{gs}=V_{n11}-V_{n12}=V_1c-V_{oel}=(V_d-\Delta V_{gs})+\{(C_{gs11}+C_{gd13})/(C_s+C_{gs11}+C_{gd13})\} \times \{C_{gd13}\cdot V_{cce}/(C_{gs11}+C_{gd13})-V_{oel}-V\} \quad (39)$$

[0219] In the formula (39), " V " is the same as that shown in formula (32b) for which $V=V_d+(C_{gs11}\cdot C_s/D)\cdot V_{shl}$ is established and " V_d " is a voltage caused between the gate and the source of the transistor Tr13 during the writing operation for which $(V_d+(C_{gs11}\cdot C_s)/D)$ is established as shown in the formula (32b). The voltage shift ΔV_{gs} in the formula (39) is a potential difference between the contact point N11 and the contact point N12 when Fig. 30A is switched to Fig. 30B and is represented by $C_{gs11}\cdot C_{pix}\cdot V_{shl}/D$ as shown in the formula (34).

[0220] Next, the following section will describe, based on the above-described formula (39), an influence by the threshold voltage V_{th} on the gate-source voltage V_{gs} of the transistor Tr13 for light-emission driving. In the formula (39), values of ΔV_{gs} , V , and D are substituted to obtain the following formula (40).

$$V_{gs}=\{C_s/(C_s+C_{gs11}+C_{gd13})\}\cdot V_d + \{(C_{gs11}+C_{gd13})/(C_s+C_{gs11}+C_{gd13})\} \times \{C_{gd13}\cdot V_{cce}/(C_{gs11}+C_{gd13})-V_{oel}-C_{gs11}\cdot V_{shl}/(C_{gs11}+C_{gd13})\} \quad (40)$$

[0221] In the formula (40), the respective capacity components C_{gs11} , C_{gs11}' , and C_{gd13} are normalized by the capacity component C_s to provide the formula (41).

$$V_{gs} = \{V_d - (c_{gs} + c_{gd}) \cdot V_{oel}\} / (1 + c_{gs} + c_{gd}) + \{c_{gd} \cdot V_{cce} - c_{gs}' \cdot V_{shl}\} / (1 + c_{gs} + c_{gd})$$

(41)

[0222] In the formula (41), c_{gs} , c_{gs}' , and c_{gd} are the same as those shown in formula (27). In the formula (41), the first term of the right-hand side depends only on the specified gradation level based on the display data and the threshold voltage V_{th} of the transistor Tr13. In the formula (41), the second term of the right-hand side is a constant added to the gate-source voltage V_{gs} of the transistor Tr13.

[0223] Thus, in order to compensate the threshold voltage V_{th} by specifying a voltage, the source potential during a writing operation (potential of contact point N12)- V_d may be set so that a value ($V_{gs} - V_{th}$) during light emission (a value determining the driving current I_{oel} during light emission) does not depend on the threshold voltage V_{th} . For example, when gate-source voltage $V_{gs} = 0 - (-V_d) = V_d$ is maintained during light emission, ($V_{gs} - V_{th}$) can be prevented from depending on V_{th} by establishing the relation of $V_{gs} = V_d = V_{d0} + V_{th}$. Then, the driving current I_{oel} during light emission is represented only by V_{d0} not depending on V_{th} . When the gate-source voltage during light emission varies from V_{gs} during a writing operation, a relation of $V_d = V_{d0} + eV_{th}$ may be used.

[0224] In the formula (41), the dependence of the organic EL element OLED on the light-emitting voltage V_{oel} in the first term of the right-hand side is determined so as to establish the relations of the following formulae (42a) to (42c). It is noted that $f(x)$, $g(x)$, and $h(x)$ in the formulae (42a) to (42c) are a function of a variable "x" in the parentheses, respectively. Specifically, the gate-source voltage V_{gs} of the transistor Tr13 is determined to be a function of the light-emitting voltage V_{oel} as shown in the formula (42a). The light emission driving current I_{em} is determined so as to be a function of a difference between this voltage V_{gs} and the threshold voltage V_{th} ($V_{gs} - V_{th}$) as shown in the formula (42b). The light-emitting voltage V_{oel} is also determined to be a function of the light emission driving current I_{em} as shown in formula (42c).

$$V_{gs} = f(V_{oel}) \quad (42a)$$

$$I_{em} = g(V_{gs} - V_{th}) \quad (42b)$$

$$V_{oel} = h(I_{em}) \quad (42c)$$

[0225] During the writing operation, a data voltage for giving a voltage based on display data (gradation level voltage) to the source of the driving transistor Tr13 (contact point N12) is V_{d0} . This data voltage V_{d0} is a term that does not depend on the threshold voltage V_{th} as described above. The threshold voltage of the transistor Tr13 at a time T_x is $V_{th}(T_x)$ and the threshold voltage at a time T_y after the time T_x is $V_{th}(T_y)$. A voltage V_{oelx} is applied at the time T_x between the anode and the cathode of the organic EL element OLED during the light-emitting operation and a voltage V_{oely} is applied between the anode and the cathode at the time T_y .

[0226] Then, voltages satisfying a condition of $V_{th}(T_y) > V_{th}(T_x)$ and a difference between the voltages applied to the organic EL element OLED at the time T_y and the time T_x are represented by $\Delta V_{oel} = V_{oely} - V_{oelx}$. In order to compensate the variation ΔV_{th} in the threshold voltage, V_{th} may be compensated to cause the ΔV_{oel} to be close to 0 as much as possible. Thus, the voltage V_d of the first term of the right-hand side in the above-described formula (41) may be set as shown in the following formula (43).

$$V_d = V_{d0} + (1 + c_{gs} + c_{gd}) \cdot \Delta V_{th} \quad (43)$$

[0227] In the formula (43), when assuming that the variation ΔV_{th} is a difference from the threshold voltage $V_{th} = 0V$, $\Delta V_{th} = V_{th}$ can be represented. Since $(c_{gs} + c_{gd})$ is a design value, when the constant e is defined as $e = 1 + c_{gs} + c_{gd}$, the voltage V_d shown in the formula (43) is represented by the following formula (44). Based on this formula (44), the above-described formulae (24) and (25) are introduced.

$$V_d = V_{d0} + (1 + c_{gs} + c_{gd}) \cdot \Delta V_{th} = V_{d0} + e \cdot \Delta V_{th} \quad (44)$$

[0228] The formula (44) and formula (41) can be used to provide the following formula (45) showing a voltage relation not depending on the threshold voltage V_{th} of the transistor Tr13. It is noted that V_{oel0} in the formula (45) is the light-emitting voltage V_{oel} of the organic EL element OLED when the threshold voltage $V_{th}=0V$.

$$V_{gs}-V_{th}=\{V_{d0}-(c_{gs}+c_{gd})\cdot V_{oel0}\}/(1+c_{gs}+c_{gd})+(c_{gd}\cdot V_{cce}-c_{gs}'\cdot V_{shl})/(1+c_{gs}+c_{gd}) \quad (45)$$

[0229] It is noted that, in the black display status as the 0th gradation level, conditions for preventing a voltage equal to or higher than the threshold voltage V_{th} from being applied between the gate and the source of the transistor Tr13 (i.e., voltage conditions for preventing the light emission driving current I_{em} from flowing in the organic EL element OLED) are calculated. The conditions are represented by the formula (46) when the data voltage at the time 0 is $V_{d0}(0)$. Thus, in the data driver 14 shown in Fig. 25, the black gradation level voltage V_{zero} applied to an output end of the inversion calculator 148 via the changing-over switch SW4 can be determined.

$$-V_{d0}(0)=V_{zero}=c_{gd}\cdot V_{cce}-c_{gs}'\cdot V_{shl} \quad (46)$$

[0230] Next, in Embodiment 2, conditions for setting the compensated gradation level voltage $V_{pix}(=-V_{in})$ so as to compensate the gate-source voltage V_{gs} of the driving transistor Tr13 due to parasitic capacitance will be described. By performing the processings of the respective steps shown in Fig. 11, the gate-source voltage V_{gs} of the driving transistor Tr13 varies due to other parasitic capacitances. In order to compensate the variation amount of this voltage V_{gs} , the compensated gradation level voltage V_{pix} in the writing period T_{wrt} (a period during which the compensated gradation level voltage V_{pix} is applied) may be set as shown in the following formula (47). It is noted that V_{ds12} in the formula (47) is a drain-source voltage of the transistor Tr12.

$$V_{pix}=-(V_d+V_{ds12})=-V_{org}-\beta V_{th} \quad (47)$$

[0231] During the writing operation shown in Fig. 34, the writing current I_{wrt} flowing between the drain and the source of the transistor Tr13 can be represented by the following formula (48). It is noted that μ_{FET} in the formula (48) represents a transistor mobility, C_i represents a transistor gate capacity per a unit area, W_{13} represents a channel width of the transistor Tr13, and L_{13} represents a channel length of the transistor Tr13. V_{dse13} is an effective drain-source voltage of the transistor Tr13 during a writing operation and V_{th13} is a threshold voltage of the transistor Tr13. The term "p" represents a unique parameter (fitting parameter) suitable for the characteristic of the thin film transistor.

$$I_{wrt}=\mu_{FET}\cdot C_i\cdot (V_d-V_{th13})\cdot V_{dse13}\cdot (W_{13}/L_{13})=p\cdot \mu_{FET}\cdot C_i\cdot (V_d-V_{th13})^2\cdot (W_{13}/L_{13}) \quad (48)$$

[0232] During a writing operation, the writing current I_{wrt} flowing between the drain and the source of the transistor Tr12 can be represented by the following formula (49). In the formula (49), V_{th12} is a threshold voltage of the transistor Tr12 and a V_{ds12} is a drain-source voltage of the transistor Tr13. W_{12} is a channel width of the transistor Tr12 and L_{12} is a channel length of the transistor Tr12.

$$I_{wrt}=\mu_{FET}\cdot C_i\cdot (V_{sh}+V_d+V_{ds12}-V_{th12})\cdot (W_{12}/L_{12})\cdot V_{dse12} \quad (49)$$

[0233] The drain-source voltage V_{dse12} of the transistor Tr12 can be represented by the following formula (50a) based on the formulae (48) and (49). In the formula (50a), V_{sat12} is an effective drain-source voltage of the transistor Tr12 during a writing operation and is represented by the following formula (50b). It is noted that "q" is a unique parameter

(fitting parameter) suitable for the characteristic of the thin film transistor.

$$V_{ds12} = V_{ds12} / \{1 + (V_{ds12} / V_{sat12})^q\}^{(1/q)} \quad (50a)$$

$$V_{sat12} = p \cdot (V_{sh} + V_d + V_{ds12} - V_{th12}) \quad (50b)$$

[0234] Generally, in an n-channel amorphous silicon transistor, the longer a time during which the transistor is in an ON status (a time during which the gate-source voltage is a positive voltage) is, the larger the shift of the threshold voltage to a higher voltage is. The driving transistor Tr13 is ON during the light-emitting period Tem. This light-emitting period Tem occupies a large part of the cycle period Tcyc. Thus, the threshold voltage of the transistor Tr13 shifts to the positive voltage as time passes and thus the transistor Tr13 has higher resistance.

[0235] On the other hand, the selection transistor Tr12 is ON only during the selection period Tsel. This selection period Tsel occupies a small part of the cycle period Tcyc. Thus, when compared with the driving transistor Tr13, the selection transistor Tr12 has a smaller temporal shift. Thus, when the compensated gradation level voltage Vpix is introduced, the variation in the threshold voltage Vth12 of the transistor Tr12 can be ignored with regards to the variation in the threshold voltage Vth13 of the transistor Tr13.

[0236] As shown in the above-described formulae (48) and (49), the writing current lwrt is determined based on a Thin Film Transistor (TFT) characteristic fitting parameter (e.g., p, q), a parameter determined by a transistor size, a process parameter (e.g., transistor gate thickness, amorphous silicon mobility), and a set value owned by the selection signal (e.g., voltage Vsh). Thus, an equation when lwrt shown in formula (48) is equal to lwrt shown in formula (49) is subjected to an numeric analysis to calculate the drain-source voltage Vds12 of the transistor Tr12. This voltage Vds12 has a relation shown in the formula (47) ($V_{pix} = -V_d - V_{ds12}$) with the compensated gradation level voltage Vpix. Thus, Vds12 can be determined to calculate the compensated gradation level voltage Vpix.

[0237] When the inversion calculator 148 outputs this compensated gradation level voltage Vpix during the writing period Twrt, -Vd is written to the source of the transistor Tr13 (contact point N12). Thus, the transistor Tr13 during the writing period Twrt has a gate-source voltage of Vgs to establish the drain-source voltage $V_{ds0} - (-V_d) = V_{d0} + e \cdot \Delta V_{th}$. By flowing the writing current lwrt as described above, the driving current loled for which the shift of the threshold voltage Vth due to an influence by parasitic capacitance for example is compensated can be flowed in the organic EL element OLED during the writing period Twrt.

[0238] Next, the following section will describe the display apparatus 1 according to Embodiment 2 and an effect by the driving method of the display apparatus 1 with reference to a specific test result. The potential (-Vd) at the source (contact point N12) of the driving transistor Tr13 during a writing operation is set based on the data voltage Vd0 and a multiple of the threshold voltage Vth by a fixed number (multiple of γ) as shown in the formula (24) ($-V_d = -V_{d0} - \gamma V_{th}$). This potential is set based on the voltage Vgs retained between the gate and the source. On the other hand, the compensated gradation level voltage Vpix ($= -V_{in}$) generated by the data driver 14 (inversion calculator 148) is set based on the original gradation level voltage Vorg and a multiple of the threshold voltage Vth by a fixed number (multiple of β) ($-V_{in} = -V_{org} - \beta V_{th}$) as shown in the formula (22).

[0239] The following section will examine conditions required for the relation between the data voltage Vd0 and the original gradation level voltage Vorg to not depend on the constants γ or β and the threshold voltage Vth. As shown in Fig. 34, during the writing operation, the higher input data (specified gradation level) of the original gradation level voltage Vorg is, the wider a difference between the data voltage Vd0 for giving a voltage depending on display data (gradation level voltage) to the source of the driving transistor Tr13 and the original gradation level voltage Vorg ($V_{d0} - V_{org}$) is. For example, in the 0th gradation level (black display status), the data voltage Vd0 and the original gradation level voltage Vorg are both Vzero (=0V). On the other hand, at the 255th gradation level (the highest gradation level), a difference between the data voltage Vd0 and the original gradation level voltage Vorg ($V_{d0} - V_{org}$) is about 1.3V. This is due to a fact that, the higher the applied compensated gradation level voltage Vpix is, the higher the writing current lwrt is and a transistor Tr13 also has a higher source drain voltage.

[0240] It is noted that the example of Fig. 34 shows the power source voltage Vcc (=Vccw) during the writing operation of the ground potential GND (=0V) and the power source voltage Vcc (=Vcce) during the light-emitting operation of 12V. A potential difference (voltage range) Vshl between the high level (Vsh) and the low level (-Vsl) of the selection signal Ssel is 27V. The transistor Tr13 for light emission driving has the channel width W13 of 100 μ m and the transistor Tr11 and transistor Tr12 have the channel widths W11 and W12 of 40 μ m. The display pixel PIX has a size of 129 μ m \times 129 μ m, the pixel has an aperture ratio of 60%, and the capacitor Cs has capacitance of 600fF (=0.6pF).

[0241] The following section will describe a relation between the compensated gradation level voltage to input data

and the threshold voltage during a writing operation. As shown in the formula (22), the compensated gradation level voltage $V_{pix}(=-V_{in})$ depends on the constant β and the threshold voltage V_{th} . When assuming that this constant β is fixed, the higher the threshold voltage V_{th} is, the lower the compensated gradation level voltage V_{pix} by this threshold voltage V_{th} as shown in Fig. 35. This tendency is found in substantially all gradation level zones of the input data (specified gradation level).

[0242] In the example of Fig. 35, when the constant $\beta=1.08$ is set and the threshold voltage V_{th} is changed in an order of 0V, 1V, and 3V, the characteristic line of the compensated gradation level voltage V_{pix} to the respective threshold voltages V_{th} substantially translates in the low voltage direction. At the 0th gradation level (black display status), the compensated gradation level voltage V_{pix} is $V_{zero}(=0V)$ regardless of the value of the threshold voltage V_{th} . It is noted that test conditions of Fig. 35 are the same as those shown in Fig. 34.

[0243] Next, the following section will describe a relation between the light emission driving current I_{em} of the organic EL element OLED and the threshold voltage V_{th} with regards to input data in a light-emitting operation. It is noted that input data has 256 gradation levels among which the lowest gradation level are the 0th gradation level and the highest gradation level are the 255th gradation level. The compensated gradation level voltage V_{pix} shown in the formula (22) is applied from the data driver 14 to the respective display pixels PIX. As a result, the writing voltage $V_{gs}(=0-(-V_d)=V_{d0}+\gamma V_{th})$ shown in formula (24) is applied between the gate and the source of the driving transistor Tr13. When the constant γ is substantially fixed, the light emission driving current I_{em} having a substantially fixed current value flowed in the organic EL element OLED regardless of the value of the threshold voltage V_{th} as shown in Fig. 36A and Fig. 36B. This tendency is found in substantially all gradation level zones of input data (specified gradation level). It is noted that test conditions of Fig. 36A and Fig. 36B are the same as those shown in Fig. 34.

[0244] The example of Fig. 36A shows a test result when the constant $\gamma=1.07$ and the threshold voltage $V_{th}=1.0V$. The example of Fig. 36B shows a test result when the constant $\gamma=1.05$ and the threshold voltage $V_{th}=3.0V$ are set. When Fig. 36A is compared with Fig. 36B, the light emission driving current I_{em} shows substantially the same characteristic line regardless of different values of the threshold voltages V_{th} .

[0245] This test result also showed that a brightness change (difference in brightness) to theoretical value is suppressed to 1.3% or less in substantially all gradation levels (hereinafter this suppression effect is called as " γ effect"). When $\gamma=1.07$ was established as shown in Fig. 36A for example and when the respective specified gradation levels (8bit) were 63, 127, and 255, the respective brightness changes were 0.27%, 0.62%, and 1.29%. When $\gamma=1.05$ was established as shown in Fig. 36B and when the respective specified gradation levels (8bit) were 63, 127, and 255, the respective brightness changes were 0.27%, 0.61%, and 1.27%.

[0246] Next, the following section will describe a relation between light emission driving current to input data and variation in the threshold voltage (shift) in a light-emitting operation. It was found that, with regards to the dependency of " γ effect" on the variation amount of the threshold voltage V_{th} (V_{th} shift width), when the constant γ was assumed as constant, the higher variation width the threshold voltage V_{th} has, the smaller difference in current to the light emission driving current I_{em} in the initial threshold voltage V_{th} .

[0247] As shown in Fig. 37A and Fig. 37B, when $\gamma=1.1$ and V_{th} was changed from 1V to 3V (V_{th} shift width was 2V) and when the respective specified gradation levels (8bit) were 63, 127, and 255, the respective brightness changes were 0.24%, 0.59%, and 1.29%. As shown in Fig. 37A and Fig. 37C, when $\gamma=1.1$ and V_{th} was changed from 1V to 5V (V_{th} shift width was 4V) and when the specified gradation levels (8bit) were 63, 127, and 255, the respective brightness changes were 0.04%, 0.12%, and 0.27%.

[0248] By the above result, it was found that, the higher variation amount (V_{th} shift width) the threshold voltage V_{th} has, the characteristic line is closer to theoretical value. Specifically, it was found that a brightness change (difference in brightness) to theoretical value could be reduced (or suppressed to about 0.3% or less).

[0249] It is noted that, in order to show the advantage of the effect by this embodiment, the above-described a test result having the " γ effect" will be compared with a test result not having the " γ effect". The test result not having the " γ effect" is obtained by driving applying such a voltage V_{th} between the gate and the source of the transistor Tr13 that does not depend on the constant γ in the relation shown in the formula (24) ($V_{gs}=0-(-V_d)=V_{d0}+\gamma V_{th}$). As shown in Figs. 38A and 39B, in the case of the test result not having the " γ effect", a relation between input data and the light emission driving current and the threshold voltage showed a characteristic line according to which, regardless of the constant γ , the higher threshold voltage V_{th} the transistor Tr13 had, the light emission driving current I_{em} was smaller. It is noted that the example of Fig. 38A shows the characteristic line of the light emission driving current I_{em} when the constant $\gamma=1.07$ is set and the threshold voltage $V_{th}=1.0V$ and 3.0V is set. The example of Fig. 38B shows the characteristic line of the light emission driving current I_{em} when the constant $\gamma=1.05$ is set and the threshold voltage $V_{th}=1.0V$ and 3.0V is set.

[0250] It was found that, in substantially all gradation level zones, a brightness change to theoretical value (difference in brightness) was 1.0% or more and a brightness change to theoretical value was 2% or more in an intermediate gradation level (the 127th gradation level in the examples of Figs. 38A and 39B) in particular. When $\gamma=1.07$ and when the respective specified gradation levels (8bit) were 63, 127, and 255, the respective brightness changes were 1.93%, 2.87%, and 4.13%. When $\gamma=1.05$ and when the respective specified gradation levels (8bit) were 63, 127, and 255, the

respective brightness changes were 1.46%, 2.09%, and 2.89%.

[0251] When this brightness change reaches about 2% in the intermediate gradation level, a user recognizes the change as a printed image. Thus, when a voltage V_{gs} not depending on the constant γ (writing voltage; $-V_d = -V_{d0} - V_{th}$) is retained in the capacitor C_s , the displayed picture has a deteriorated quality. On the other hand, according to Embodiment 2, a voltage retained in the capacitor C_s is a writing voltage for which the constant γ is compensated ($=0 - (-V_d) = V_{d0} + \gamma V_{th}$). Thus, as shown in Fig. 36 and Fig. 37, a brightness change to theoretical value (difference in brightness) at the respective gradation levels can be significantly suppressed. Thus, the display apparatus 1 of Embodiment 2 can prevent an image from being printed to display the image with preferred display picture quality.

[0252] Next, the following section will describe a relation between the compensated gradation level voltage V_{pix} and the gate-source voltage V_{gs} of the transistor Tr_{13} . The source of the transistor Tr_{13} (contact point N_{12}) and the data line L_d have therebetween a potential difference due to resistance when the transistor Tr_{12} is ON. Thus, the contact point N_{12} retains a voltage obtained by adding the data voltage V_{d0} to a voltage obtained by multiplying the threshold voltage V_{th} of the transistor Tr_{13} with γ . By the retention of this voltage, such a voltage is retained as the compensated gradation level voltage V_{pix} at the contact point N_{12} that is obtained by adding the original gradation level voltage V_{org} to a voltage β times higher than the threshold voltage V_{th} , as shown in the formula (22).

[0253] The following section will examine, in the relation between the compensated gradation level voltage V_{pix} and the gate-source voltage V_{gs} of the transistor Tr_{13} shown in the formulae (22) and (24), a change γV_{th} of $V_{gs} (=V_d)$ when BV_{th} is OFFSET to $V_{pix} (=V_{in})$.

[0254] As shown in Fig. 39, when the threshold voltage V_{th} changes from 0V to 3V, the constant β determining the compensated gradation level voltage V_{pix} is fixed to the input data (specified gradation level). On the other hand, the constant γ determining the gate-source voltage V_{gs} of the transistor Tr_{13} changes to have a substantially fixed slope with regards to the input data (specified gradation level). In the example of Fig. 39, $\gamma = 1.097$ may be set for $\beta = 1.08$ in the intermediate gradation level (which is in the vicinity of the 128th gradation level when the number of gradation levels are 256) so that the constant γ has an ideal value (which is shown by a chain line in Fig. 39). Since the constant β and the constant γ can be set to relatively close values, $\beta = \gamma$ may be set for a practical use.

[0255] In consideration of the above test results, a constant $\gamma (=B)$ for determining the gate-source voltage V_{gs} of the driving transistor Tr_{13} is desirably 1.05 or more. It was found that the compensated gradation level voltage V_{pix} may be set so that the voltage V_d retained in the source (contact point N_{12}) of the transistor Tr_{13} in at least one gradation level of input data (specified gradation level) is the voltage $(-V_{d0} - \gamma V_{th})$ shown in the formula (24).

[0256] Furthermore, the dimension of the transistor Tr_{13} (a ratio W/L between the channel width W and the channel length L) and the voltage of the selection signal S_{sel} (V_{sh} and $-V_{sl}$) are desirably set so that a change in the light emission driving current I_{em} in accordance with variation in the threshold voltage (V_{th} shift) is within about 2% of the maximum current value in an initial status.

[0257] The compensated gradation level voltage V_{pix} is a value obtained by adding the drain-source voltage of the transistor Tr_{12} to the source potential $(-V_d)$ of the transistor Tr_{13} . The larger absolute value of the difference between the power source voltage V_{ccw} and the compensated gradation level voltage V_{pix} ($V_{ccw} - V_{pix}$) is, the higher value the current flowing between the drain and the source of each of the transistors Tr_{12} and Tr_{13} during the writing operation has. This causes an increased potential difference between the compensated gradation level voltage V_{pix} and the source potential $(-V_d)$ of the transistor Tr_{13} .

[0258] However, when an influence on the voltage drop by the drain-source voltage of the transistor Tr_{12} is reduced, an effect β times higher than the threshold voltage V_{th} directly appears in the " γ effect". Specifically, if the OFFSET voltage γV_{th} that can satisfy the relation of the formula (24) can be set, variation in the value of the light emission driving current I_{em} when the writing operation status shifts to the light-emitting operation status can be compensated. In this case, an influence by the drain-source voltage of the transistor Tr_{12} must be considered.

[0259] As shown in Fig. 34, the transistor Tr_{12} is designed so that the drain-source voltage of the transistor Tr_{12} is about 13V at the maximum gradation level (the maximum drain-source voltage) in the writing operation. In this case, as shown in Fig. 39, a difference between a constant $\gamma (=1.07)$ at the lowest gradation level (the 0th gradation level) and a constant $\gamma (=1.11)$ at the highest gradation level (the 255th gradation level) is sufficiently small. Thus, the difference can be approximated to β shown in the formula (22).

[0260] The voltage V_{d0} of the gate-source voltage V_{gs} of the transistor Tr_{13} of a difference between the power source voltage V_{ccw} and the compensated gradation level voltage V_{pix} ($V_{ccw} - V_{pix}$) is the original gradation level voltage V_{org} . The compensated gradation level voltage V_{pix} is set to a voltage obtained by adding the OFFSET voltage βV_{th} to the original gradation level voltage V_{org} to have a negative polarity. During the writing operation, this compensated gradation level voltage V_{pix} is set to satisfy the formula (22). In this case, the maximum voltage between the drain and the source of the transistor Tr_{12} can be appropriately set to approximate the constant γ to the constant β . As a result, the respective gradation levels can be accurately displayed in a range from the lowest gradation level to the highest gradation level.

[0261] The following section will describe the characteristic of the change of the pixel current to the driving voltage of the organic EL element OLED (having a pixel size of $129\mu m \times 129\mu m$ and an aperture ratio of 60%) used for the test.

As shown in Fig. 40, the pixel current of this organic EL element OLED has a small current value on the order of $10 \times 10^{-3} \mu\text{A}$ to $10 \times 10^{-5} \mu\text{A}$ in a zone in which the driving voltage is a negative voltage. The pixel current also showed the lowest value when the driving voltage is about 0V and sharply increases with an increase of the driving voltage in a zone in which the driving voltage is a positive voltage.

[0262] The following section will describe a relation between the in-channel parasitic capacitance of a transistor applied to the display pixel PIX and the voltage. First, based on a Meyer capacity model generally referred to with regards to the parasitic capacitance of the thin film transistor TFT, a relation between the capacity and the voltage (capacity characteristic) is shown under conditions under which the gate-source voltage V_{gs} is higher than the threshold voltage V_{th} ($V_{gs} > V_{th}$) (i.e., conditions under which a channel is formed between the source and the drain).

[0263] The in-channel parasitic capacitance C_{ch} of the thin film transistor is classified to a gate-source parasitic capacitance C_{gs_ch} and a gate-drain parasitic capacitance C_{gd_ch} . A capacity ratio between the respective parasitic capacitances C_{gs_ch} and C_{gd_ch} and the in-channel parasitic capacitance C_{ch} (C_{gs_ch}/C_{ch} , C_{gd_ch}/C_{ch}) has a predetermined characteristic with regards to a difference between the gate-source voltage V_{gs} and the threshold voltage V_{th} ($V_{gs} - V_{th}$).

[0264] As shown in Fig. 41, when the voltage ratio is 0 (the drain-source voltage $V_{ds} = 0V$), the capacity ratio C_{gs_ch}/C_{ch} is equal to the capacity ratio C_{gd_ch}/C_{ch} and both of the capacity ratios are 1/2. When the voltage ratio increases and the drain-source voltage V_{ds} reaches the saturated zone, the capacity ratio C_{gs_ch}/C_{ch} is about 2/3 and the capacity ratio C_{gd_ch}/C_{ch} is asymptotic to 0.

[0265] As described above, according to Embodiment 2, the display apparatus 1 applies the compensated gradation level voltage V_{pix} having the voltage value shown in the formula (50a) at the writing operation of the display pixel PIX. Thus, the voltage V_{gs} can be retained between the gate and the source of the transistor Tr13. It is noted that this voltage V_{gs} corresponds to display data (gradation level values) and is set to compensate an influence by a voltage change in the pixel driving circuit DC. Thus, the current value of the light emission driving current I_{em} supplied to the organic EL element OLED during a light-emitting operation can be compensated.

[0266] Specifically, the light emission driving current I_{em} having the current value corresponding to the display data is flowed in the organic EL element OLED. Thus, the organic EL element can be caused to emit light with brightness depending on display data. This can suppress the dislocation of the gradation level in the respective display pixels to provide a display apparatus having a superior display quality. It is noted that Embodiment 2 also can appropriately use a method for driving a display apparatus that is substantially the same as that of Embodiment 1.

[0267] Various embodiments and changes may be made thereunto without departing from the scope of the invention. The above-described embodiments are intended to illustrate the present invention, not to limit the scope of the present invention. The scope of the present invention is shown by the attached claims rather than the embodiments.

Claims

1. A display apparatus (1), comprising:

a light-emitting element (OLED) configured to emit light with a gradation level depending on supplied current;
a pixel driving circuit (DC) configured to supply the current to the light-emitting element depending on a voltage applied via a data line (Ld),
wherein the pixel driving circuit (DC) includes:

a driving transistor (Tr13) having a source terminal serially connected to the light-emitting element (OLED) and a drain terminal connected to a power source voltage line (Lv),
a retention transistor (Tr11) having a gate terminal connected to a selection line (Ls), a source terminal connected to the gate terminal of the driving transistor (Tr13) and a drain terminal connected to the drain terminal of the driving transistor (Tr13),
a selection transistor (Tr12) having a gate terminal, a source terminal connected to the data line (Ld) and a drain terminal connected to the source terminal of the driving transistor (Tr13), and
a capacitor (Cs) connected between the gate terminal and the source terminal of the driving transistor (Tr13);

the display apparatus further comprising:

a precharge voltage source configured to apply a predetermined precharge voltage (V_{pre}) to the gate terminal of the driving transistor (Tr13) of the pixel driving circuit (DC) via the data line (Ld),

a voltage reader (145) configured to read, after the application of the precharge voltage (V_{pre}) by the

precharge voltage source has ended and while the selection transistor (Tr12) is turned on, the voltage of the data line (Ld) after a predetermined transient response period, and to generate a first compensation voltage (a.Vref) based on the read voltage (Vref) of the data line (Ld);

an original gradation level voltage generator (142) configured to generate an original gradation level voltage (Vorg) having a voltage value not depending on a threshold voltage of the pixel driving circuit (DC), the original gradation level voltage (Vorg) being for causing the light-emitting element to emit light with a desired brightness corresponding to the gradation level;

a compensated gradation data signal generator (142) configured to generate, based on the original gradation level voltage (Vorg), a compensated gradation level voltage (Vplx) and to apply the compensated gradation level voltage (Vpix) to the pixel driving circuit (DC) via the data line, wherein the compensated gradation data signal generator (142) comprises a voltage calculator (144) configured to obtain for calculation the original gradation level voltage (Vorg) and the first compensation voltage (a.Vref) to generate the compensated gradation level voltage (Vpix) having a voltage value corresponding to the threshold voltage of the driving transistor (Tr13) of the pixel driving circuit (DC); and connection path switching switches (SW1, SW2, SW3) configured to selectively connect the data line (Ld) with the precharge voltage source, the compensated gradation data signal generator (142) and the voltage reader (145) to switch between application of the precharge voltage (Vpre) to the data line (Ld), voltage sensing of the data line (Ld) and application of a corrected data voltage (Vdata) to the data line (Ld);

characterized in that

the gate terminal of the selection transistor (Tr12) is connected to the selection line (Ls);

the voltage reader (145) is configured to generate the first compensation voltage (a.Vref) by multiplying the read voltage (Vref) of the data line (Ld) with a coefficient a;

the predetermined transient response period is shorter than a time during which the voltage of the data line (Ld) converges to a converge voltage value of the pixel driving circuit (DC); and

the voltage calculator (144) is further configured to obtain for calculation a predetermined second compensation voltage (Vofst) to generate the compensated gradation level voltage (Vpix), wherein the second compensation voltage (Vofst) is determined based on an output variation characteristic of the threshold voltage (Vth) of the driving transistor (Tr13), and during the writing operation, the voltage calculator (144) is configured to determine the compensated gradation level voltage (Vpix) according to the equation:

$$\text{compensated gradation level voltage (Vpix)} = \text{first compensation voltage (a.Vref)} - \text{original gradation level voltage (Vorg)} + \text{second compensation voltage (Vofst)}.$$

2. The display apparatus according to claim 1, wherein:

the display apparatus includes a black gradation level voltage source (144) configured to apply, to the pixel driving circuit, a black gradation level voltage for causing the light-emitting element to perform a black display, and a switch (SW1) configured to connect the black gradation level voltage source to the data line at a predetermined timing.

3. The display apparatus according to claim 1, wherein:

the precharge voltage has a voltage value having a higher absolute value than an absolute value of the converge voltage value of the pixel driving circuit.

4. The display apparatus according to claim 1, wherein:

the display apparatus further includes a controller (15) configured to perform, within a predetermined period the steps of:

(i) using the connection path switching switch (SW3) to connect the precharge voltage source to the data line to apply the precharge voltage to the pixel driving circuit;

(ii) using the connection path switching switch (SW2) to connect the voltage reader to the data line to read the voltage of the data line corresponding to the threshold voltage of the pixel driving circuit after the transient response period; and

(iii) using the connection path switching switch (SW1) to connect the compensated gradation data signal gen-

erator to the data line to apply the compensated gradation level voltage to the pixel driving circuit.

5. The display apparatus according to claim 1, wherein:

the display apparatus further includes: a selection driver (12) configured to apply a selection signal to the pixel driving circuit via the selection line to cause the pixel driving circuit to be in a selected state, and a display panel (11) in which a plurality of display pixels are arranged in a matrix manner, each of the plurality of display pixels including a pair of one said light-emitting element and one said pixel driving circuit; and
the plurality of display pixels are arranged in a row direction and a column direction, the data line is connected to the pixel driving circuits of a plurality of the display pixels arranged in the column, and the selection line is connected to the pixel driving circuits of a plurality of the display pixels arranged in the row direction.

6. The display apparatus according to claim 1, wherein:

the compensated gradation data signal generator is further configured to generate the compensated gradation level voltage based on a voltage retained in the pixel driving circuit.

7. A method for driving a display apparatus (1) including:

a pixel driving circuit (DC) comprising:

a driving transistor (Tr13) having a source terminal serially connected to a light-emitting element (OLED) and a drain terminal connected to a power source voltage line (Lv),
a retention transistor (Tr11) having a gate terminal connected to a selection line (Ls), a source terminal connected to the gate terminal of the driving transistor (Tr13) and a drain terminal connected to the drain terminal of the driving transistor (Tr13),
a selection transistor (Tr12) having a gate terminal, a source terminal connected to the data line (Ld) and a drain terminal connected to the source terminal of the driving transistor (Tr13), and
a capacitor (Cs) connected between the gate terminal and the source terminal of the driving transistor (Tr13), wherein
the gate terminal of the selection transistor (Tr12) is connected to the selection line (Ls); and

connection path switching switches (SW1, SW2, SW3) configured to selectively connect the data line (Ld) with a precharge voltage source, a compensated gradation data signal generator (142) and a voltage reader (145) to switch between application of a precharge voltage (Vpre) to the data line (Ld), voltage sensing of the data line (Ld) and application of a compensated gradation level voltage (Vpix) to the data line (Ld), the method comprising:

applying the predetermined precharge voltage (Vpre) to the gate terminal of the driving transistor (Tr13) of the pixel driving circuit (DC) via the data line (Ld);
reading, while the selection transistor (Tr12) is turned on, after the application of the precharge voltage (Vpre) has ended, the voltage of the data line (Ld) after a predetermined transient response period and generating a first compensation voltage (a·Vref) corresponding to a threshold voltage of the drive transistor (Tr13) of the pixel driving circuit (DC) based on the read voltage;
generating an original gradation level voltage (Vorg) having a voltage value not depending on a threshold voltage of the pixel driving circuit (DC), the original gradation level voltage (Vorg) being for causing the light-emitting element to emit light with a desired brightness corresponding to the gradation level;
generating, based on the original gradation level voltage (Vorg) and the first compensation voltage (a·Vref) the compensated gradation level voltage (Vpix), the compensated gradation level voltage (Vpix) having a voltage value corresponding to the threshold voltage of the driving transistor (Tr13) of the pixel driving circuit (DC);
applying the generated compensated gradation level voltage (Vpix) to the pixel driving circuit (DC) via the data line (Ld); and
supplying current from the pixel driving circuit (DC) to the light-emitting element (OLED) depending on the compensated gradation level voltage (Vpix) applied to the pixel driving circuit;
characterized in that
the predetermined transient response period is shorter than a time during which the voltage of the data line (Ld) converges to a converge voltage value of the pixel driving circuit (DC);
the first compensation voltage (a·Vref) corresponding to the threshold voltage of the drive transistor (Tr13)

of the pixel driving circuit (DC) is generated by multiplying the voltage (Vref) read from the data line (Ld) with a coefficient a;

the step of generating the compensated gradation level voltage (Vpix) is further based on a second predetermined compensation voltage (Vofst) determined on the basis of the theoretical value of the threshold voltage of the driving transistor (Tr13) of the pixel driving circuit (DC); and

the compensated gradation level voltage (Vpix) is determined according to the equation:

$$\text{compensated gradation level voltage (Vpix)} = \text{first compensation voltage (a} \cdot \text{Vref)} - \text{original gradation level voltage (Vorg)} + \text{second compensation voltage (Vofst)}.$$

8. The method for driving a display apparatus (1) according to claim 7, wherein the step of generating the compensated gradation level voltage is based on a voltage retained in the pixel driving circuit.

Patentansprüche

1. Anzeigevorrichtung (1), umfassend:

ein lichtemittierendes Element (OLED), das dazu eingerichtet ist, Licht mit einem von einem zugeführten Strom abhängigen Abstufungspegel zu emittieren;

eine Pixelansteuerschaltung (DC), die dazu eingerichtet ist, dem lichtemittierenden Element den Strom abhängig von einer über eine Datenleitung (Ld) angelegten Spannung zuzuführen, wobei die Pixelansteuerschaltung (DC) aufweist:

einen Ansteuertransistor (Tr13) mit einem Source-Anschluss, der in Serie mit dem lichtemittierenden Element (OLED) verbunden ist, und einem Drain-Anschluss, der mit einer Stromquellen-Spannungsleitung (Lv) verbunden ist,

einen Haltetransistor (Tr11) mit einem Gate-Anschluss, der mit einer Auswahlleitung (Ls) verbunden ist, einem Source-Anschluss, der mit dem Gate-Anschluss des Ansteuertransistors (Tr13) verbunden ist, und einem Drain-Anschluss, der mit dem Drain-Anschluss des Ansteuertransistors (Tr13) verbunden ist,

einen Auswahltransistor (Tr12) mit einem Gate-Anschluss, einem Source-Anschluss, der mit der Datenleitung (Ld) verbunden ist, und einem Drain-Anschluss, der mit dem Source-Anschluss des Ansteuertransistors (Tr13) verbunden ist, und

einen Kondensator (Cs), der zwischen dem Gate-Anschluss und dem Source-Anschluss des Ansteuertransistors (Tr13) verbunden ist;

wobei die Anzeigevorrichtung ferner umfasst:

eine Vorlade-Spannungsquelle, die dazu eingerichtet ist, an den Gate-Anschluss des Ansteuertransistors (Tr13) der Pixelansteuerschaltung (DC) über die Datenleitung (Ld) eine vorbestimmte Vorladespannung (Vpre) anzulegen,

einen Spannungsleser (145), der dazu eingerichtet ist, nachdem das Anlegen der Vorladespannung (Vpre) durch die Vorladespannungsquelle geendet hat und während der Auswahltransistor (Tr12) eingeschaltet ist, die Spannung der Datenleitung (Ld) nach einer vorbestimmten transienten Antwortdauer zu lesen und eine erste Kompensationsspannung (a·Vref) basierend auf der gelesenen Spannung (Vref) der Datenleitung (Ld) zu generieren;

einen Ursprüngliche-Abstufungspegel-Spannungsgenerator (142), der dazu eingerichtet ist, eine ursprüngliche Abstufungspegelspannung (Vorg) mit einem Spannungswert zu generieren, der nicht von einer Schwellspannung der Pixelansteuerschaltung (DC) abhängt, wobei die ursprüngliche Abstufungspegelspannung (Vorg) dazu dient, das lichtemittierende Element dazu zu veranlassen, Licht mit einer dem Abstufungspegel entsprechenden gewünschten Helle zu emittieren;

einen Kompensiertes-Abstufungsdatensignal-Generator (142), der dazu eingerichtet ist, basierend auf der ursprünglichen Abstufungspegelspannung (Vorg) eine kompensierte Abstufungspegelspannung (Vpix) zu generieren und die kompensierte Abstufungspegelspannung (Vpix) über die Datenleitung an die Pixelansteuerschaltung (DC) anzulegen, wobei der Kompensiertes-Abstufungsdatensignal-Generator (142) einen Spannungsberechner (144) umfasst, der dazu eingerichtet ist, zur Berechnung die

ursprüngliche Abstufungspegelspannung (Vorg) und die erste Kompensationsspannung ($a \cdot V_{ref}$) zu erlangen, um die kompensierte Abstufungspegelspannung (V_{pix}) mit einem der Schwellspannung des Ansteuertransistors (Tr13) der Pixelansteuerschaltung (DC) entsprechenden Spannungswert zu generieren; und

Verbindungspfad-Umschalterschalter (SW1, SW2, SW3), die dazu eingerichtet sind, selektiv die Datenleitung (Ld) mit der Vorladespannungsquelle, dem Kompensiertes-Abstufungsdatensignal-Generator (142) und dem Spannungsleser (145) zu verbinden, um zwischen Anlegen der Vorladespannung (V_{pre}) an die Datenleitung (Ld), Spannungsmessen an der Datenleitung (Ld) und Anlegen einer korrigierten Datenspannung (V_{data}) an die Datenleitung (Ld) umzuschalten;

dadurch gekennzeichnet, dass

der Gate-Anschluss des Auswahltransistors (Tr12) mit der Auswahlleitung (Ls) verbunden ist; der Spannungsleser (145) dazu eingerichtet ist, die erste Kompensationsspannung ($a \cdot V_{ref}$) durch Multiplizieren der gelesenen Spannung (V_{ref}) der Datenleitung (Ld) mit einem Koeffizienten a zu generieren;

die vorbestimmte transiente Antwortdauer kürzer als eine Zeit ist, während welcher die Spannung der Datenleitung (Ld) bei einem Konvergenzspannungswert der Pixelansteuerschaltung (DC) konvergiert; und

der Spannungsberechner (144) ferner dazu eingerichtet ist, zur Berechnung eine vorbestimmte zweite Kompensationsspannung (V_{ofst}) zu beziehen, um die kompensierte Abstufungspegelspannung (V_{pix}) zu generieren, wobei die zweite Kompensationsspannung (V_{ofst}) basierend auf einer Ausgangsvariationskenngröße der Schwellspannung (V_{th}) des Ansteuertransistors (Tr13) bestimmt ist, und während des Schreibvorgangs der Spannungsberechner (144) dazu eingerichtet ist, die kompensierte Abstufungspegelspannung (V_{pix}) gemäß folgender Gleichung zu bestimmen:

kompensierte Abstufungspegelspannung (V_{pix}) = erste Kompensationsspannung ($a \cdot V_{ref}$) - ursprüngliche Abstufungspegelspannung (Vorg) + zweite Kompensationsspannung (V_{ofst}).

2. Anzeigevorrichtung nach Anspruch 1, wobei:

die Anzeigevorrichtung eine Schwarzabstufungspegel-Spannungsquelle (144) umfasst, welche dazu eingerichtet ist, an die Pixelansteuerschaltung eine Schwarzabstufungspegelspannung anzulegen, welche dazu dient, das lichtemittierende Element dazu zu veranlassen, eine Anzeige von schwarz durchzuführen, und einen Schalter (SW1), welcher dazu eingerichtet ist, die Schwarzabstufungspegel-Spannungsquelle zu einem vorbestimmten Zeitpunkt mit der Datenleitung zu verbinden.

3. Anzeigevorrichtung nach Anspruch 1, wobei:

die Vorladespannung einen Spannungswert aufweist, welcher einen höheren Absolutwert aufweist als ein Absolutwert des Konvergenzspannungswerts der Pixelansteuerschaltung.

4. Anzeigevorrichtung nach Anspruch 1, wobei:

die Anzeigevorrichtung ferner eine Steuereinheit (15) aufweist, die dazu eingerichtet ist, innerhalb einer vorbestimmten Dauer folgende Schritte durchzuführen:

(i) Verwenden des Verbindungspfadumschalterschalters (SW3), um die Vorladespannungsquelle mit der Datenleitung zu verbinden, um die Vorladespannung an die Pixelansteuerschaltung anzulegen;

(ii) Verwenden des Verbindungspfadumschalterschalters (SW2), um den Spannungsleser mit der Datenleitung zu verbinden, um die Spannung der Datenleitung auszulesen, welche der Schwellspannung der Pixelansteuerschaltung nach der transienten Antwortdauer entspricht; und

(iii) Verwenden des Verbindungspfadumschalterschalters (SW1), um den Kompensierte-Abstufungsdaten-Signalgenerator mit der Datenleitung zu verbinden, um die kompensierte Abstufungspegelspannung an die Pixelansteuerschaltung anzulegen.

5. Anzeigevorrichtung nach Anspruch 1, wobei:

die Anzeigevorrichtung ferner umfasst: einen Auswahltreiber (12), der dazu eingerichtet ist, ein Auswahlsignal über die Auswahlleitung an die Pixelansteuerschaltung anzulegen, um die Pixelansteuerschaltung dazu zu veranlassen, in einem ausgewählten Zustand zu sein, und ein Anzeigefeld (11), in welchem mehrere Anzeigepixel nach Art einer Matrix angeordnet sind, wobei ein jeweiliges der mehreren Anzeigepixel ein Paar aus einem der lichtemittierenden Elemente und einer der Pixelansteuerschaltungen aufweist; und die mehreren Anzeigepixel in einer Zeilenrichtung und in einer Spaltenrichtung angeordnet sind, die Datenleitung

mit den Pixelansteuerschaltungen mehrerer der Anzeigepixel verbunden ist, die in der Spalte angeordnet sind, und die Auswahlleitung mit den Pixelansteuerschaltungen mehrerer der Anzeigepixel verbunden ist, die in der Zeilenrichtung angeordnet sind.

5 6. Anzeigevorrichtung nach Anspruch 1, wobei:

der Kompensiertes-Abstufungsdaten-Signalgenerator ferner dazu eingerichtet ist, die kompensierte Abstufungspegelspannung basierend auf einer in der Pixelansteuerschaltung gehaltenen Spannung zu generieren.

10 7. Verfahren zum Ansteuern einer Anzeigevorrichtung (1) mit einer Pixelansteuerschaltung (DC), welche umfasst:

einen Ansteuertransistor (Tr13) mit einem Source-Anschluss, der in Serie mit einem lichtemittierenden Element (OLED) verbunden ist, und einem Drain-Anschluss, der mit einer Stromquellen-Spannungsleitung (Lv) verbunden ist,

15 einen Haltetransistor (Tr11) mit einem Gate-Anschluss, der mit einer Auswahlleitung (Ls) verbunden ist, einem Source-Anschluss, der mit dem Gate-Anschluss des Ansteuertransistors (Tr13) verbunden ist, und einem Drain-Anschluss, der mit dem Drain-Anschluss des Ansteuertransistors (Tr13) verbunden ist,

einen Auswahltransistor (Tr12) mit einem Gate-Anschluss, einem Source-Anschluss, der mit der Datenleitung (Ld) verbunden ist, und einem Drain-Anschluss, der mit dem Source-Anschluss des Ansteuertransistors (Tr13) verbunden ist, und

20 einen Kondensator (Cs), der zwischen dem Gate-Anschluss und dem Source-Anschluss des Ansteuertransistors (Tr13) verbunden ist, wobei der Gate-Anschluss des Auswahltransistors (Tr12) mit der Auswahlleitung (Ls) verbunden ist; und

Verbindungspfad-Umschalterschalter (SW1, SW2, SW3), die dazu eingerichtet sind, selektiv die Datenleitung (Ld) mit der Vorladespannungsquelle, einem Kompensiertes-Abstufungsdatensignal-Generator (142) und einem Spannungsleser (145) zu verbinden, um zwischen Anlegen der Vorladespannung (Vpre) an die Datenleitung (Ld), Spannungsmessen an der Datenleitung (Ld) und Anlegen einer kompensierten Abstufungspegelspannung (Vpix) an die Datenleitung (Ld), wobei das Verfahren umfasst:

30 Anlegen der vorbestimmten Vorladespannung (Vpre) an den Gate-Anschluss des Ansteuertransistors (Tr13) der Pixelansteuerschaltung (DC) über die Datenleitung (Ld);

Auslesen, während der Auswahltransistor (Tr12) eingeschaltet ist, nachdem das Anlegen der Vorladespannung (Vpre) durch die Vorladespannungsquelle geendet hat, der Spannung der Datenleitung (Ld) nach einer vorbestimmten transienten Antwortdauer und Generieren einer ersten Kompensationsspannung ($a \cdot V_{ref}$) welche einer Schwellenspannung des Ansteuertransistors (Tr13) der Pixelansteuerschaltung (DC) entspricht, basierend auf der gelesenen Spannung;

35 Generieren einer ursprünglichen Abstufungspegelspannung (Vorg) mit einem Spannungswert, der nicht von einer Schwellspannung der Pixelansteuerschaltung (DC) abhängt, wobei die ursprüngliche Abstufungspegelspannung (Vorg) dazu dient, das lichtemittierende Element dazu zu veranlassen, Licht mit einer dem Abstufungspegel entsprechenden gewünschten Helle zu emittieren;

40 Generieren, basierend auf der ursprünglichen Abstufungspegelspannung (Vorg) und der ersten Kompensationsspannung ($a \cdot V_{ref}$) der kompensierten Abstufungspegelspannung (Vpix), wobei die kompensierte Abstufungspegelspannung (Vpix) einen Spannungswert aufweist, der der Schwellspannung des Ansteuertransistors (Tr13) der Pixelansteuerschaltung (DC) entspricht;

45 Anlegen der generierten kompensierten Abstufungspegelspannung (Vpix) über die Datenleitung (Ld) an die Pixelansteuerschaltung (DC); und

Zuführen von Strom von der Pixelansteuerschaltung (DC) an das lichtemittierende Element (OLED) abhängig von der an die Pixelansteuerschaltung angelegten kompensierten Abstufungspegelspannung (Vpix);

dadurch gekennzeichnet, dass

50 die vorbestimmte transiente Antwortdauer kürzer als eine Zeit ist, während welcher die Spannung der Datenleitung (Ld) bei einem Konvergenzspannungswert der Pixelansteuerschaltung (DC) konvergiert;

die erste Kompensationsspannung ($a \cdot V_{ref}$), die der Schwellspannung des Ansteuertransistors (Tr13) der Pixelansteuerschaltung (DC) entspricht, durch Multiplizieren der gelesenen Spannung (V_{ref}) der Datenleitung (Ld) mit einem Koeffizienten a generiert wird;

55 der Schritt des Generierens der kompensierten Abstufungspegelspannung (Vpix) ferner auf einer zweiten vorbestimmten Kompensationsspannung (V_{ofst}) basiert, welche auf der Basis des theoretischen Werts der Schwellspannung des Ansteuertransistors (Tr13) bestimmt der Pixelansteuerschaltung (DC) bestimmt ist; und

die kompensierte Abstufungspegelspannung (Vpix) gemäß folgender Gleichung bestimmt wird:

kompen­sierte Abstufungspegelspannung (V_{pix}) = erste Kompen­sa­tionsspannung
 ($a \cdot V_{ref}$) – ursprüngliche Abstufungspegelspannung (V_{org}) + zweite
 Kompen­sa­tionsspannung (V_{ofst}).

8. Verfahren zum Ansteuern einer Anzeigevorrichtung (1) nach Anspruch 7, wobei der Schritt des Generierens der kompen­sierten Abstufungspegelspannung auf einer in der Pixelansteuerschaltung gehaltenen Spannung basiert.

Revendications

1. Appareil d'affichage (1) comprenant :

un élément électroluminescent (OLED) configuré pour émettre de la lumière avec un niveau de gradation en fonction d'un courant fourni ;
 un circuit d'excitation de pixel (DC) configuré pour fournir le courant à l'élément électroluminescent en fonction d'une tension appliquée par le biais d'une ligne de données (Ld),
 dans lequel le circuit d'excitation de pixel (DC) comprend :

un transistor d'excitation (Tr13) ayant une borne source raccordée en série à l'élément électroluminescent (OLED) et une borne drain raccordée à une ligne de tension de source d'énergie (V_s),
 un transistor à capacité de mémorisation (Tr11) ayant une borne de gâchette raccordée à une ligne de sélection (Ls), une borne source raccordée à la borne de gâchette du transistor d'excitation (Tr13) et une borne drain raccordée à la borne drain du transistor d'excitation (Tr13),
 un transistor de sélection (Tr12) ayant une borne de gâchette, une borne source raccordée à la ligne de données (Ld) et une borne drain raccordée à la borne source du transistor d'excitation (Tr13), et
 un condensateur (Cs) raccordé entre la borne de gâchette et la borne source du transistor d'excitation (Tr13) ;

l'appareil d'affichage comprenant en outre :

une source de tension de précharge configurée pour appliquer une tension de précharge prédéterminée (V_{pre}) à la borne de gâchette du transistor d'excitation (Tr13) du circuit d'excitation de pixel (DC) par le biais de la ligne de données (Ld), un lecteur de tension (145) configuré pour lire, après que l'application de la tension de précharge (V_{pre}) par la source de tension de précharge est terminée et pendant que le transistor de sélection (Tr12) est mis sous tension, la tension de la ligne de données (Ld) après une période de réponse transitoire prédéterminée et pour générer une première tension de compensation ($a \cdot V_{ref}$) en se basant sur la tension lue (V_{ref}) de la ligne de données (Ld) ;

un générateur de tension de niveau de gradation d'origine (142) configuré pour générer une tension de niveau de gradation d'origine (V_{org}) ayant une valeur de tension qui ne dépend pas d'une tension de seuil du circuit d'excitation de pixel (DC), la tension de niveau de gradation d'origine (V_{org}) étant destinée à contraindre l'élément électroluminescent d'émettre de la lumière avec une luminosité souhaitée correspondant au niveau de gradation ;

un générateur de signal de données de gradation compensée (142) configuré pour générer, sur la base de la tension de niveau de gradation d'origine (V_{org}), une tension de niveau de gradation compensée (V_{pix}) et pour appliquer la tension de niveau de gradation compensée (V_{pix}) au circuit d'excitation de pixel (DC) par le biais de la ligne de données, dans lequel le générateur de signal de données de gradation compensée (142) comprend un calculateur de tension (144) configuré pour obtenir un calcul de la tension de niveau de gradation d'origine (V_{org}) et de la première tension de compensation ($a \cdot V_{ref}$) pour générer la tension de niveau de gradation compensée (V_{pix}) ayant une valeur de tension correspondant à la tension de seuil du transistor d'excitation (Tr13) du circuit d'excitation de pixel (DC) ; et

des commutateurs de commutation de trajet de raccordement (SW1, SW2, SW3) configurés pour raccorder de façon sélective la ligne de données (Ld) à la source de tension de précharge, au générateur de signal de données de gradation compensée (142) et au lecteur de tension (145) pour commuter entre l'application de la tension de précharge (V_{pre}) à la ligne de données (Ld), une détection de tension de la ligne de données (Ld) et l'application d'une tension de données corrigée (V_{data}) à la ligne de données (Ld) ;

caractérisé en ce que

la borne de gâchette du transistor de sélection (Tr12) est raccordée à la ligne de sélection (Ls) ;

le lecteur de tension (145) est configuré pour générer la première tension de compensation ($a \cdot V_{ref}$) en multipliant la tension lue (V_{ref}) de la ligne de données (L_d) avec un coefficient a ;

la période de réponse transitoire prédéterminée est plus courte qu'un moment pendant lequel la tension de la ligne de données (L_d) converge vers une valeur de tension de convergence du circuit d'excitation de pixel (DC) ;
et

le calculateur de tension (144) est en outre configuré pour obtenir un calcul d'une seconde tension de compensation prédéterminée (V_{fst}) pour générer la tension de niveau de gradation compensée (V_{pix}), dans lequel la seconde tension de compensation (V_{fst}) est déterminée sur la base d'une caractéristique de variation de sortie de la tension de seuil (V_{th}) du transistor d'excitation (Tr_{13}) et, pendant l'opération d'écriture, le calculateur de tension (144) est configuré pour déterminer la tension de niveau de gradation compensée (V_{pix}) selon l'équation :
tension de niveau de gradation compensée (V_{pix}) = première tension de compensation ($a \cdot V_{ref}$) - tension de niveau de gradation d'origine (V_{org}) + seconde tension de compensation (V_{fst}).

2. Appareil d'affichage selon la revendication 1, dans lequel :

l'appareil d'affichage comprend une source de tension de niveau de gradation de noir (144) configurée pour appliquer, au circuit d'excitation de pixel, une tension de niveau de gradation de noir pour contraindre l'élément électroluminescent à effectuer un affichage noir, et un commutateur (SW_1) configuré pour raccorder la source de tension de niveau de gradation de noir à la ligne de données à un moment prédéterminé.

3. Appareil d'affichage selon la revendication 1, dans lequel :

la tension de précharge présente une valeur de tension ayant une valeur absolue supérieure à une valeur absolue de la valeur de tension de convergence du circuit d'excitation de pixel.

4. Appareil d'affichage selon la revendication 1, dans lequel :

l'appareil d'affichage comprend en outre un dispositif de commande (15) configuré pour effectuer, pendant une période prédéterminée, les étapes consistant :

- (i) à utiliser le commutateur de commutation de trajet de raccordement (SW_3) pour raccorder la source de tension de précharge à la ligne de données pour appliquer la tension de précharge au circuit d'excitation de pixel ;
- (ii) à utiliser le commutateur de commutation de trajet de raccordement (SW_2) pour raccorder le lecteur de tension à la ligne de données pour lire la tension de la ligne de données correspondant à la tension de seuil du circuit d'excitation de pixel après la période de réponse transitoire ; et
- (iii) à utiliser le commutateur de commutation de trajet de raccordement (SW_1) pour raccorder le générateur de signal de données de gradation compensée à la ligne de données pour appliquer la tension de niveau de gradation compensée au circuit d'excitation de pixel.

5. Appareil d'affichage selon la revendication 1, dans lequel :

l'appareil d'affichage comprend en outre : un pilote de sélection (12) configuré pour appliquer un signal de sélection au circuit d'excitation de pixel par le biais de la ligne de sélection pour contraindre le circuit d'excitation de pixel à être dans un état sélectionné, et un panneau d'affichage (11) dans lequel une pluralité de pixels d'affichage sont disposés de manière matricielle, chaque pixel d'affichage de la pluralité de pixels d'affichage comprenant une paire d'un dit élément électroluminescent et d'un dit circuit d'excitation de pixel ; et la pluralité de pixels d'affichage sont disposés dans une direction de rangée et dans une direction de colonne, la ligne de données est raccordée aux circuits d'excitation de pixel d'une pluralité de pixels d'affichage disposés dans la colonne et la ligne de sélection est raccordée aux circuits d'excitation de pixel d'une pluralité de pixels d'affichage disposés dans la direction de rangée.

6. Appareil d'affichage selon la revendication 1, dans lequel :

le générateur de signal de données de gradation compensée est en outre configuré pour générer la tension de niveau de gradation compensée en se basant sur une tension conservée dans le circuit d'excitation de pixel.

7. Procédé pour commander un appareil d'affichage (1) comprenant :

un circuit d'excitation de pixel (DC) comprenant :

un transistor d'excitation (Tr_{13}) ayant une borne source raccordée en série à l'élément électroluminescent (OLED) et une borne drain raccordée à une ligne de tension de source d'énergie (L_v),

un transistor à capacité de mémorisation (Tr11) ayant une borne de gâchette raccordée à une ligne de sélection (Ls), une borne source raccordée à la borne de gâchette du transistor d'excitation (Tr13) et une borne drain raccordée à la borne drain du transistor d'excitation (Tr13),
 un transistor de sélection (Tr12) ayant une borne de gâchette, une borne source raccordée à la ligne de données (Ld) et une borne drain raccordée à la borne source du transistor d'excitation (Tr13), et
 un condensateur (Cs) raccordé entre la borne de gâchette et la borne source du transistor d'excitation (Tr13), dans lequel
 la borne de gâchette du transistor de sélection (Tr12) est raccordée à la ligne de sélection (Ls) ; et

des commutateurs de commutation de trajet de raccordement (SW1, SW2, SW3) configurés pour raccorder de façon sélective la ligne de données (Ld) à une source de tension de précharge, à un générateur de signal de données de gradation compensée (142) et à un lecteur de tension (145) pour commuter entre l'application d'une tension de précharge (Vpre) à la ligne de données (Ld), une détection de tension de la ligne de données (Ld) et l'application d'une tension de niveau de gradation compensée (Vpix) à la ligne de données (Ld), le procédé consistant :

à appliquer la tension de précharge prédéterminée (Vpre) à la borne de gâchette du transistor d'excitation (Tr13) du circuit d'excitation de pixel (DC) par le biais de la ligne de données (Ld) ;

à lire, pendant que le transistor de sélection (Tr12) est mis sous tension, après que l'application de la tension de précharge (Vpre) est terminée, la tension de la ligne de données (Ld) après une période de réponse transitoire prédéterminée et à générer une première tension de compensation ($a \cdot V_{ref}$) correspondant à une tension de seuil du transistor d'excitation (Tr13) du circuit d'excitation de pixel (DC) en se basant sur la tension lue ;

à générer une tension de niveau de gradation d'origine (Vorg) ayant une valeur de tension qui ne dépend pas d'une tension de seuil du circuit d'excitation de pixel (DC), la tension de niveau de gradation d'origine (Vorg) étant destinée à contraindre l'élément électroluminescent d'émettre de la lumière avec une luminosité souhaitée correspondant au niveau de gradation ;

à générer, sur la base de la tension de niveau de gradation d'origine (Vorg) et de la première tension de compensation ($a \cdot V_{ref}$), la tension de niveau de gradation compensée (Vpix), la tension de niveau de gradation compensée (Vpix) ayant une valeur de tension correspondant à la tension de seuil du transistor d'excitation (Tr13) du circuit d'excitation de pixel (DC) ;

à appliquer la tension de niveau de gradation compensée (Vpix) générée au circuit d'excitation de pixel (DC) par le biais de la ligne de données (Ld) ; et

à fournir un courant depuis le circuit d'excitation de pixel (DC) à l'élément électroluminescent (OLED) en fonction de la tension de niveau de gradation compensée (Vpix) appliquée au circuit d'excitation de pixel ;
caractérisé en ce que

la période de réponse transitoire prédéterminée est plus courte qu'un moment pendant lequel la tension de la ligne de données (Ld) converge vers une valeur de tension de convergence du circuit d'excitation de pixel (DC) ;

la première tension de compensation ($a \cdot V_{ref}$) correspondant à la tension de seuil du transistor d'excitation (Tr13) du circuit d'excitation de pixel (DC) est générée en multipliant la tension (V_{ref}) lue à partir de la ligne de données (Ld) avec un coefficient a ;

l'étape de génération de la tension de niveau de gradation compensée (Vpix) est en outre basée sur une seconde tension de compensation prédéterminée (V_{fst}) déterminée sur la base de la valeur théorique de la tension de seuil du transistor d'excitation (Tr13) du circuit d'excitation de pixel (DC) ; et
 la tension de niveau de gradation compensée (Vpix) est déterminée selon l'équation :

tension de niveau de gradation compensée (Vpix) = première tension de compensation ($a \cdot V_{ref}$) - tension de niveau de gradation d'origine (Vorg) + seconde tension de compensation (V_{fst}).

8. Procédé pour commander un appareil d'affichage (1) selon la revendication 7, dans lequel l'étape de génération de la tension de niveau de gradation compensée est basée sur une tension conservée dans le circuit d'excitation de pixel.

FIG. 1

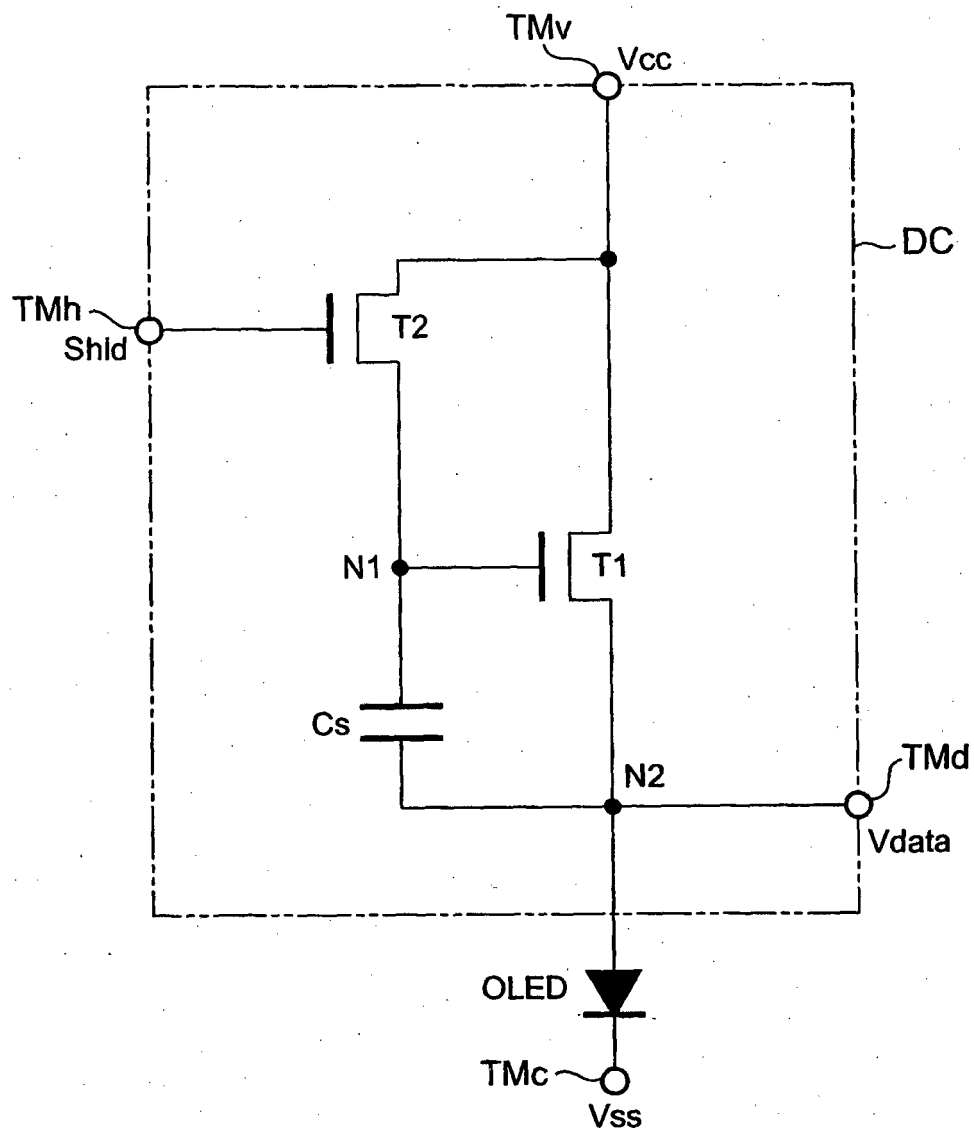


FIG. 2

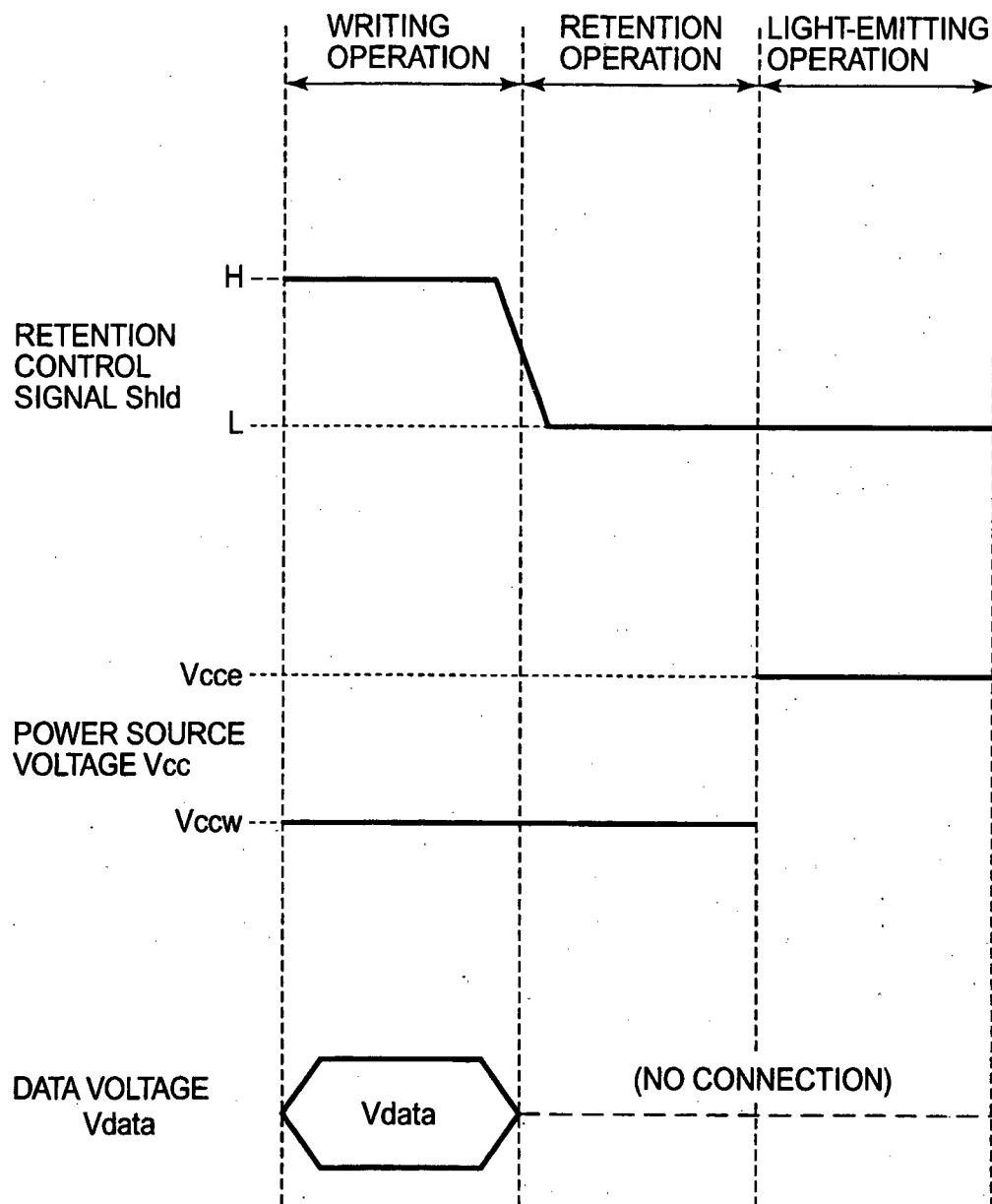


FIG. 3A

DURING WRITING OPERATION

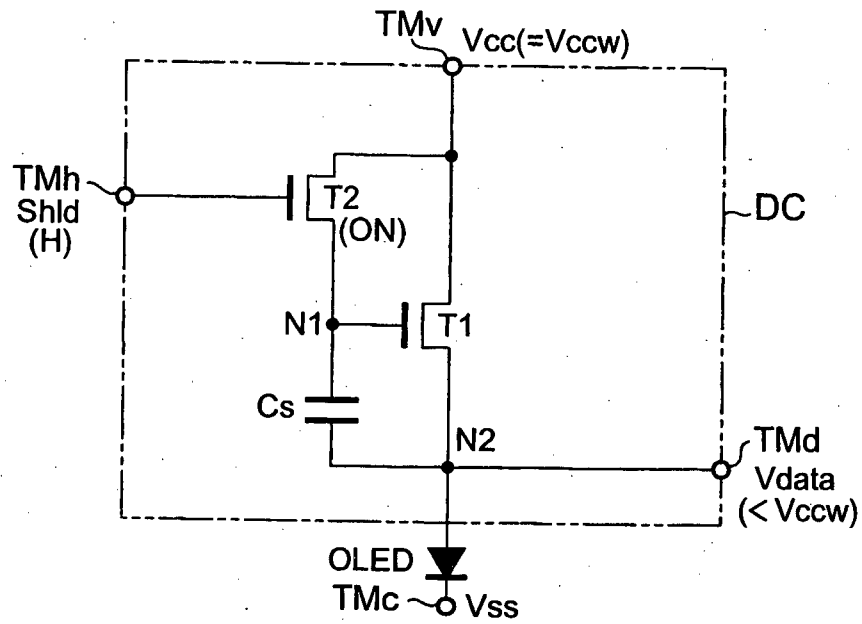


FIG. 3B

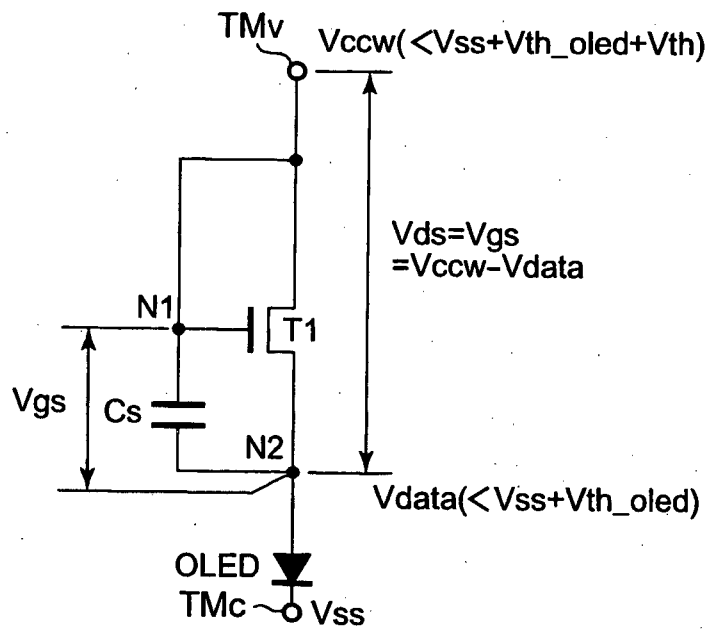


FIG. 4A

DURING WRITING OPERATION

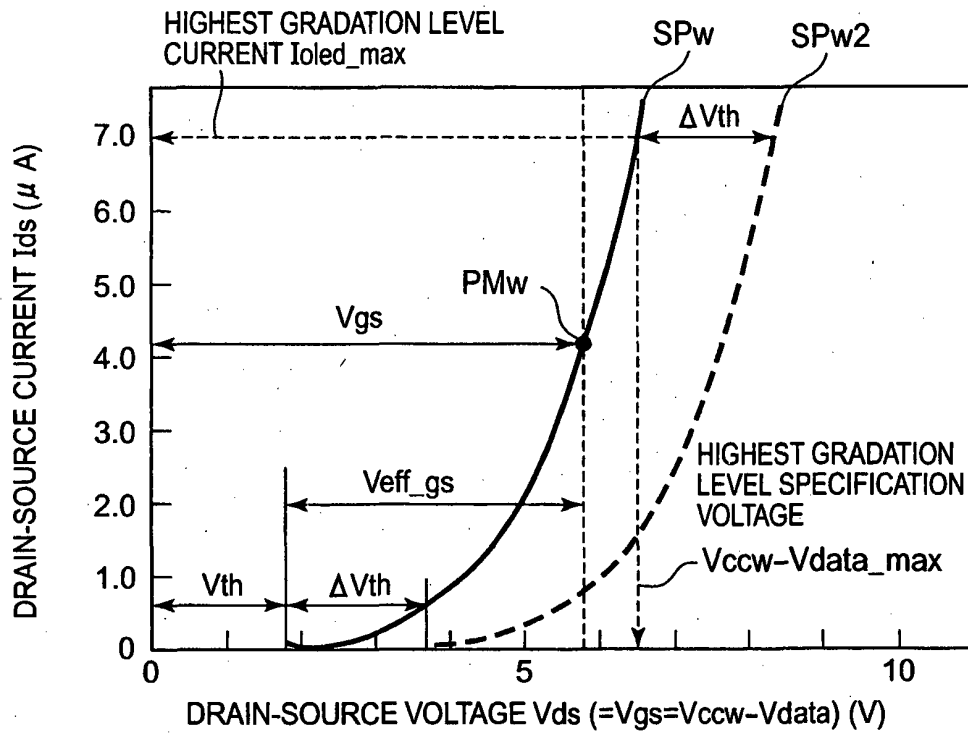


FIG. 4B

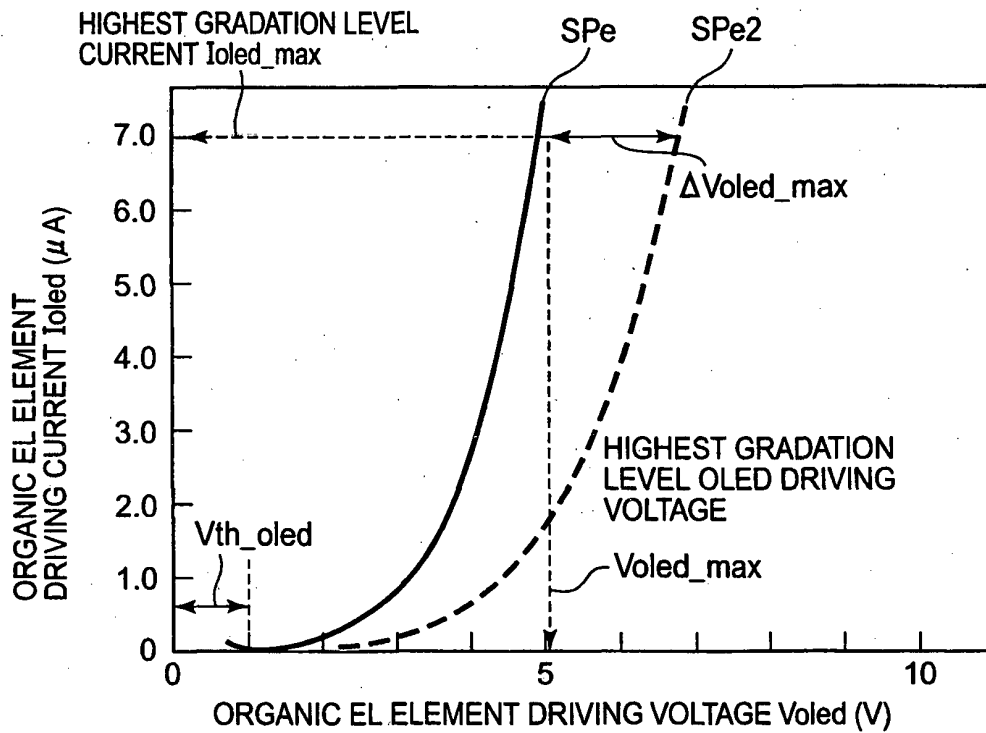


FIG. 5A

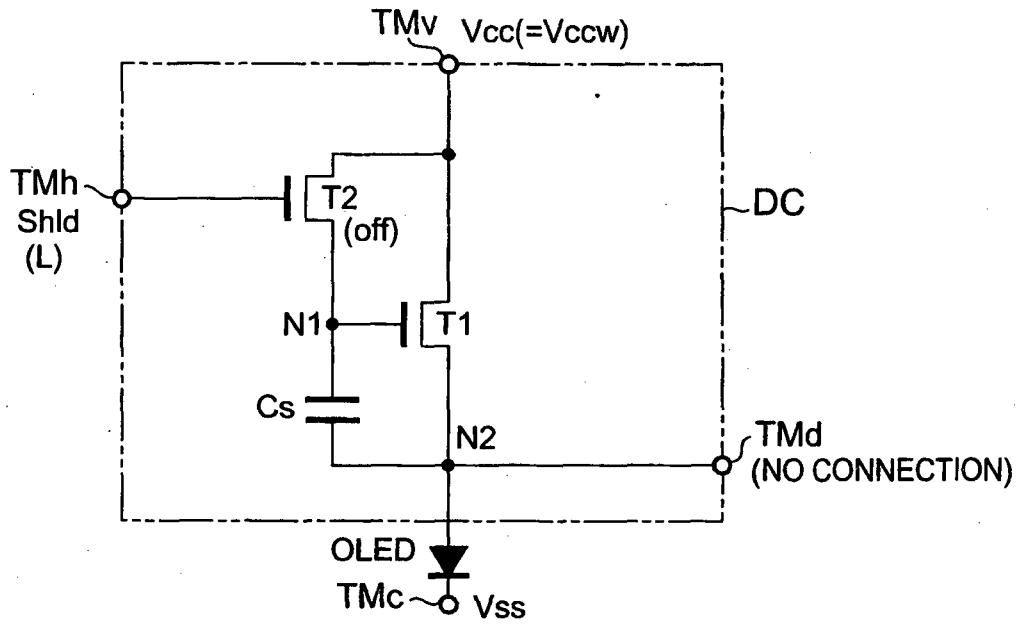
DURING RETENTION OPERATION

FIG. 5B

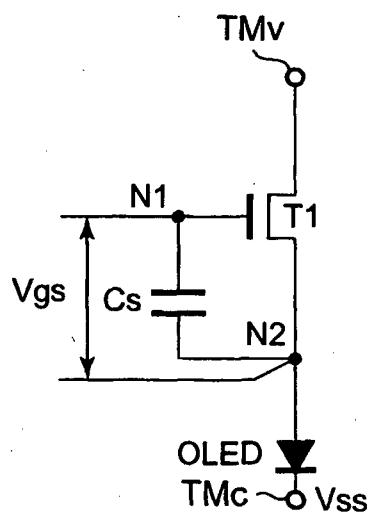


FIG. 6

DURING RETENTION OPERATION

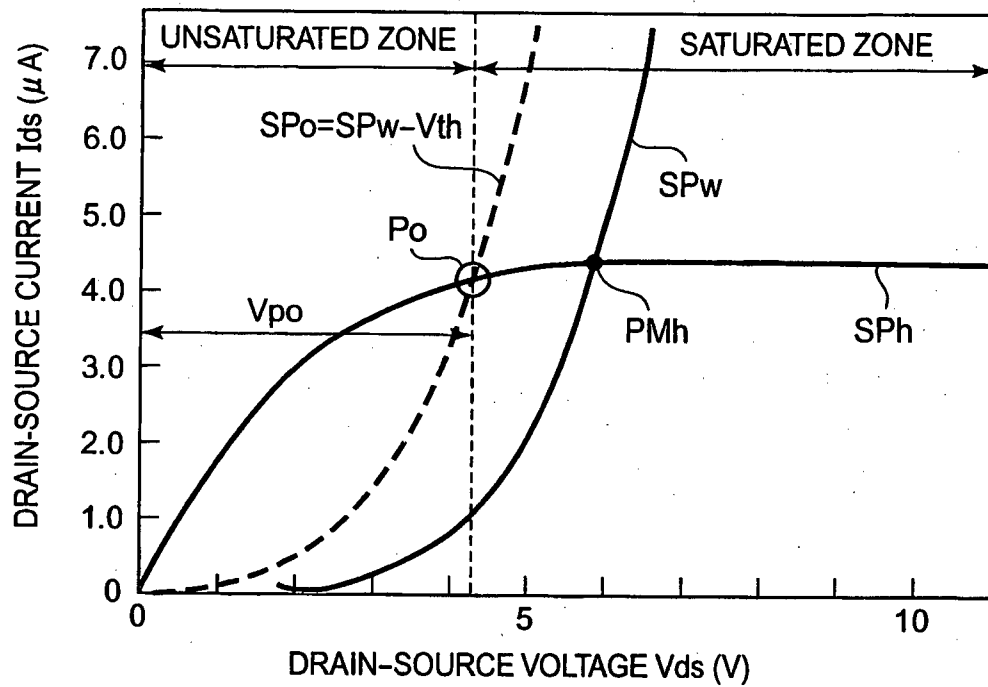


FIG. 7A

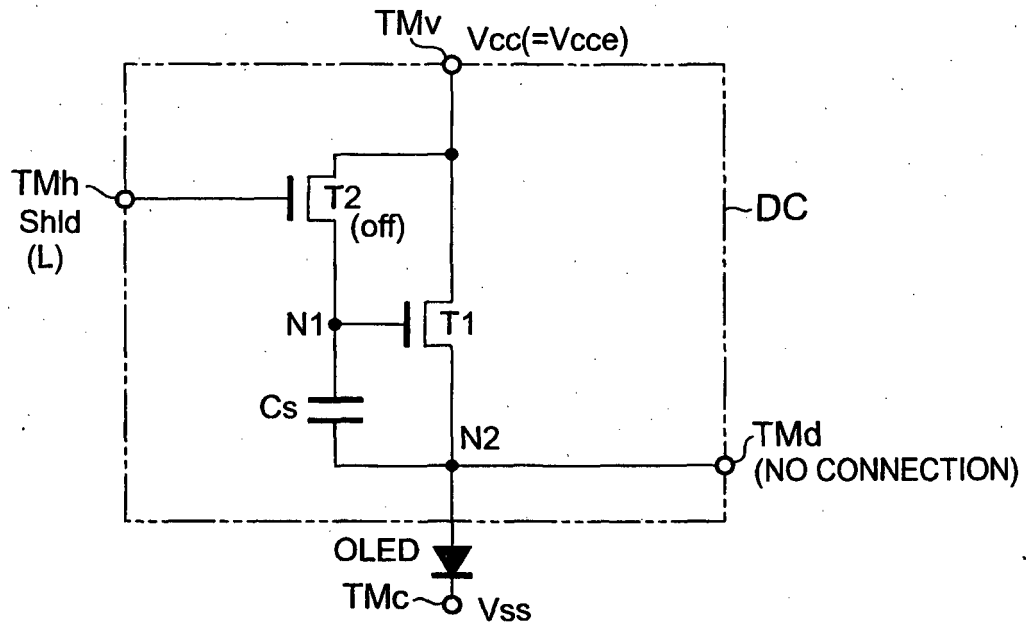
DURING LIGHT-EMITTING OPERATION

FIG. 7B

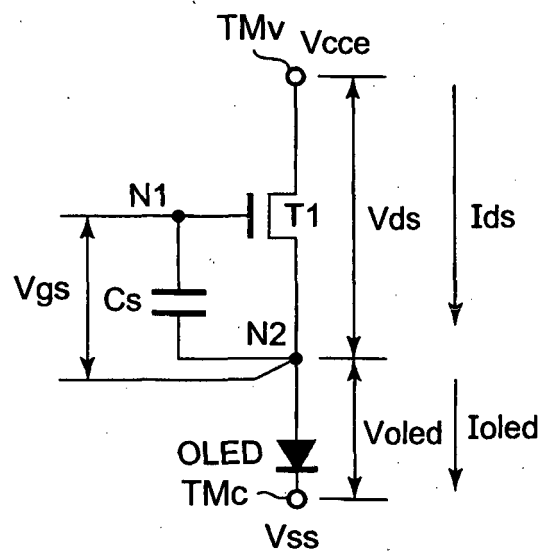


FIG. 8A

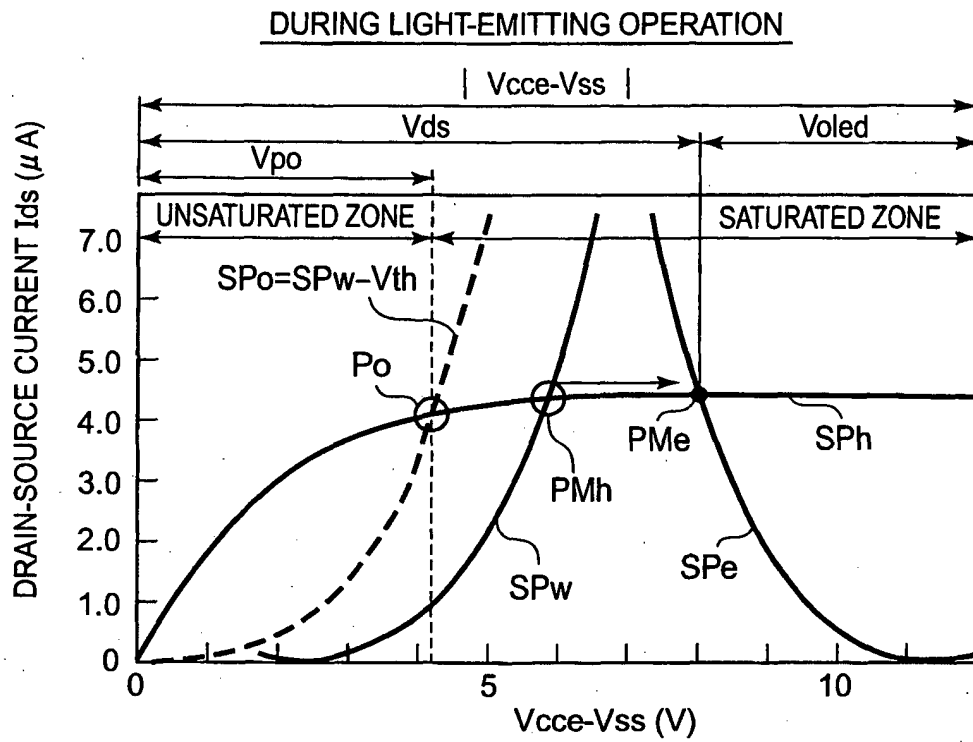


FIG. 8B

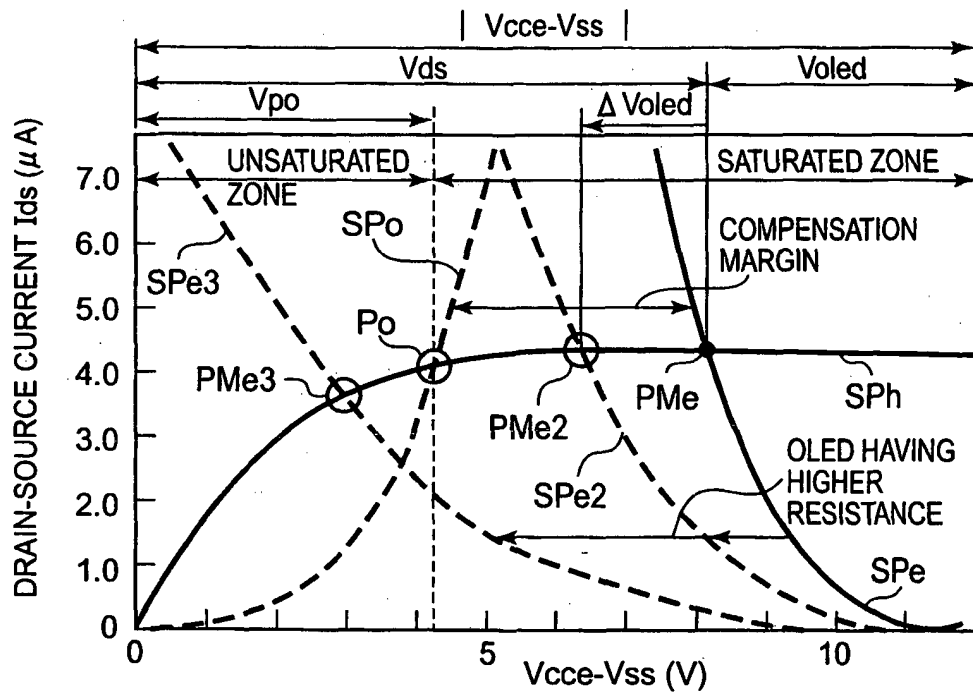


FIG. 9

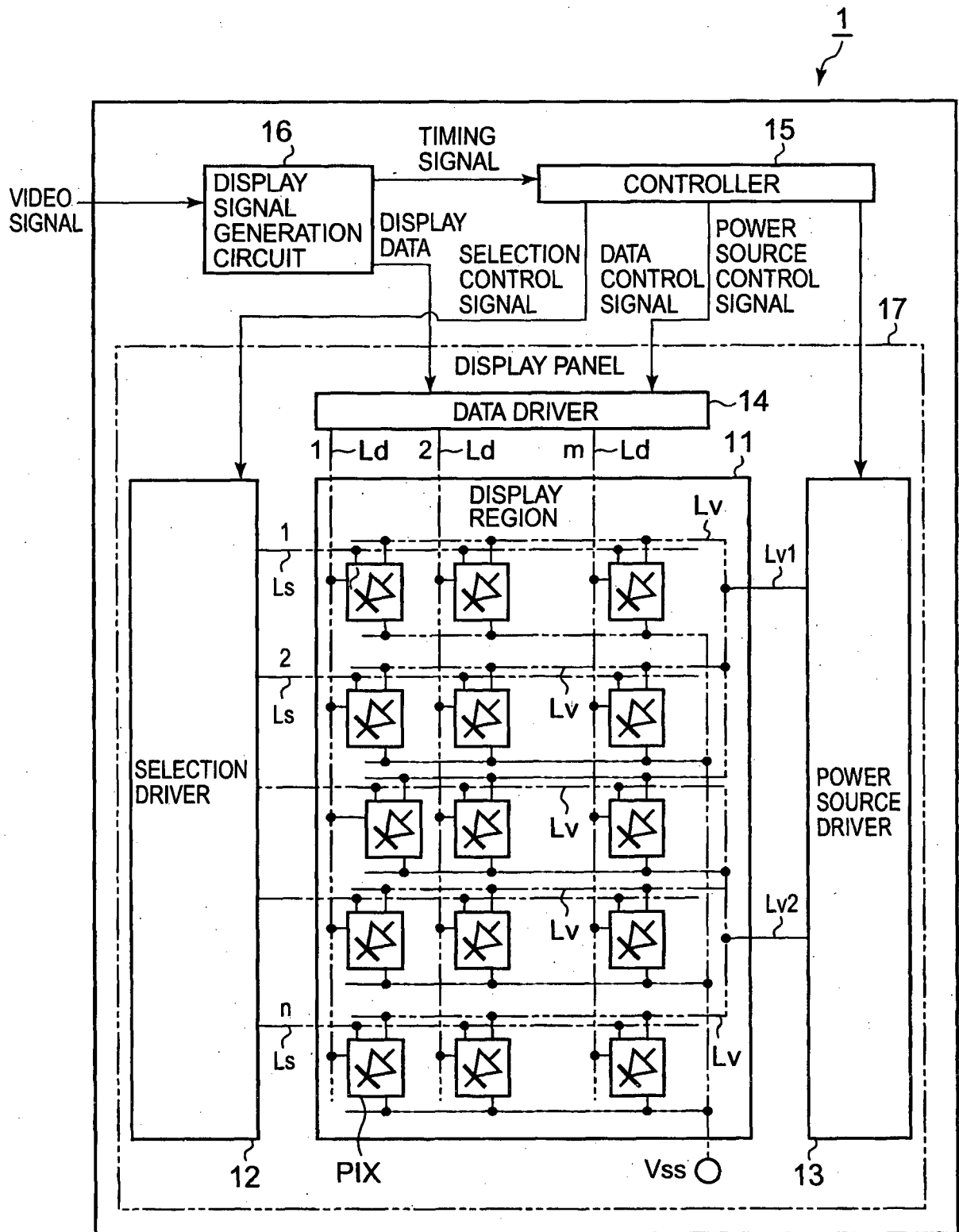


FIG. 10

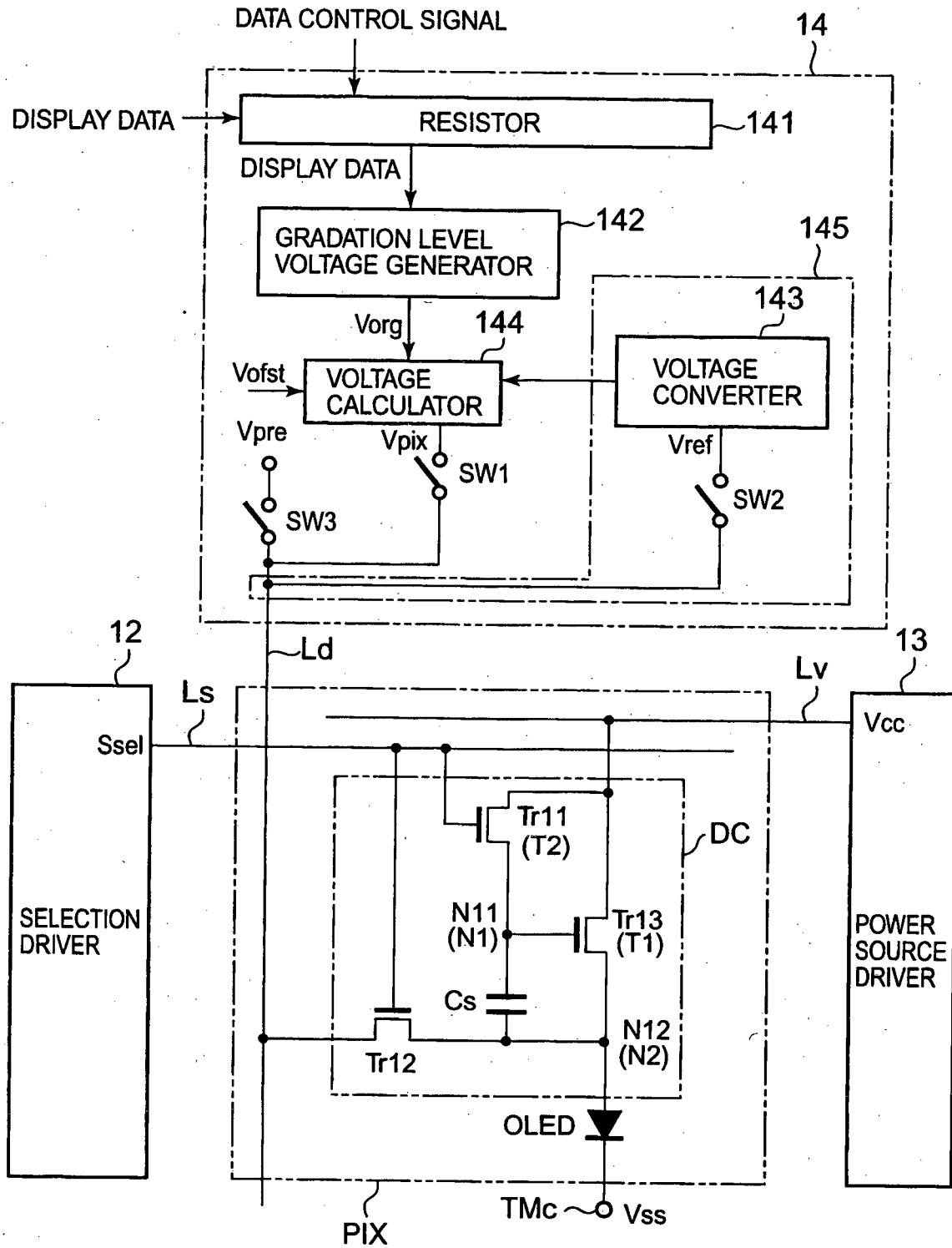


FIG. 11

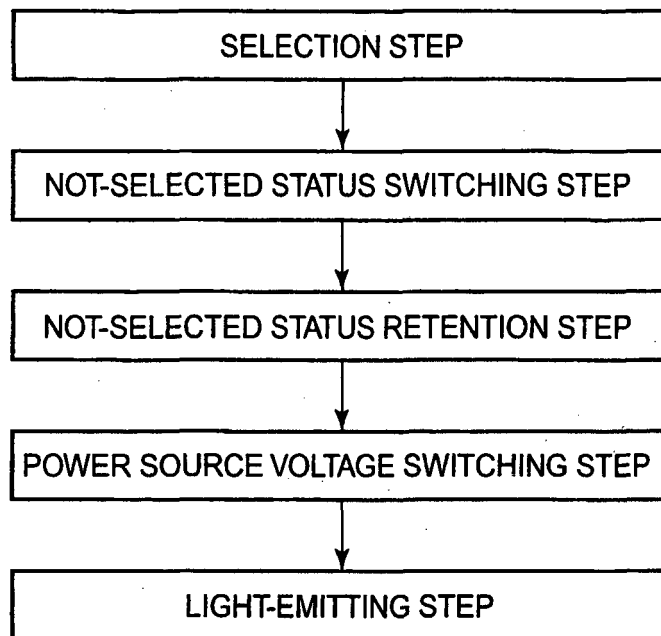


FIG. 12

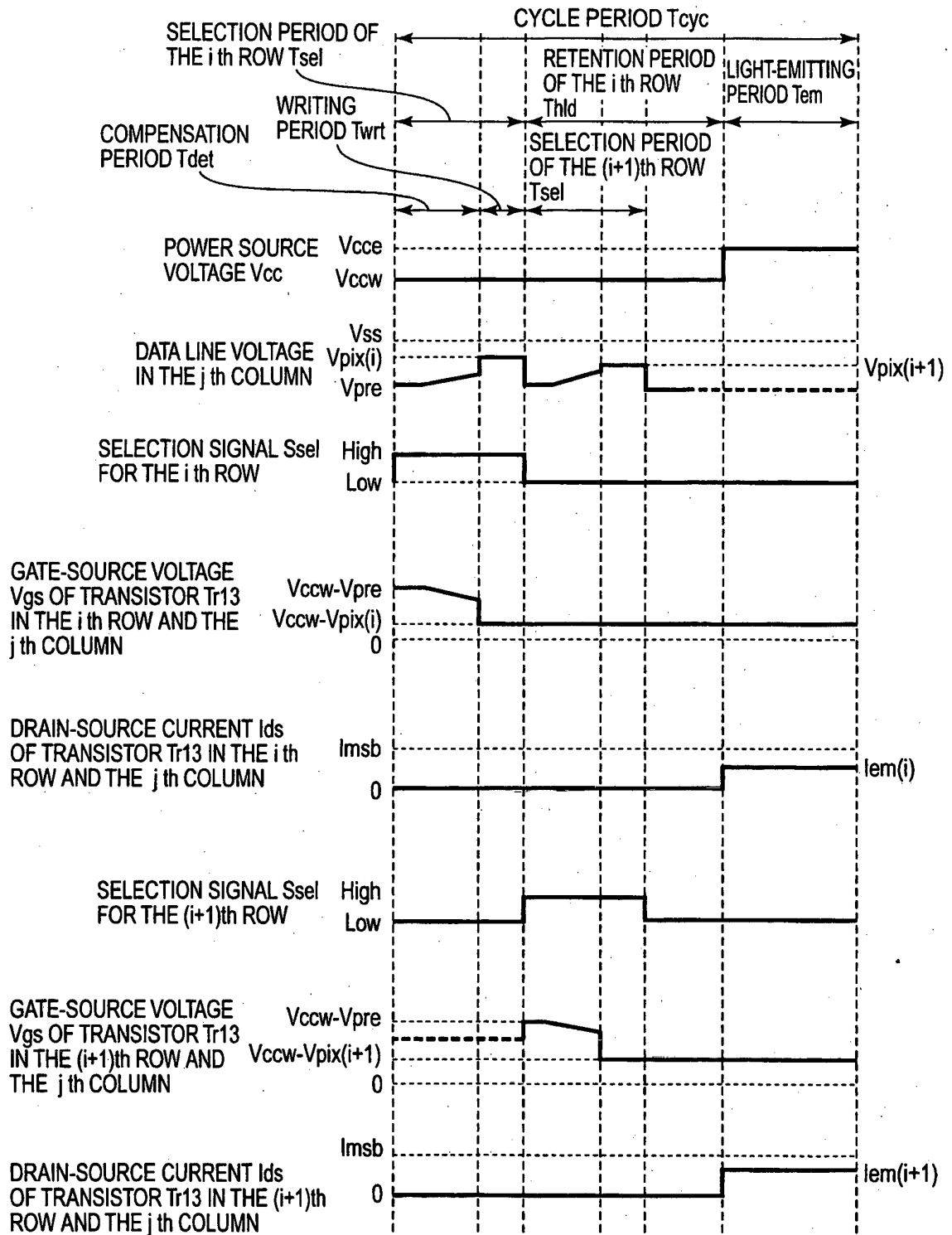


FIG. 13

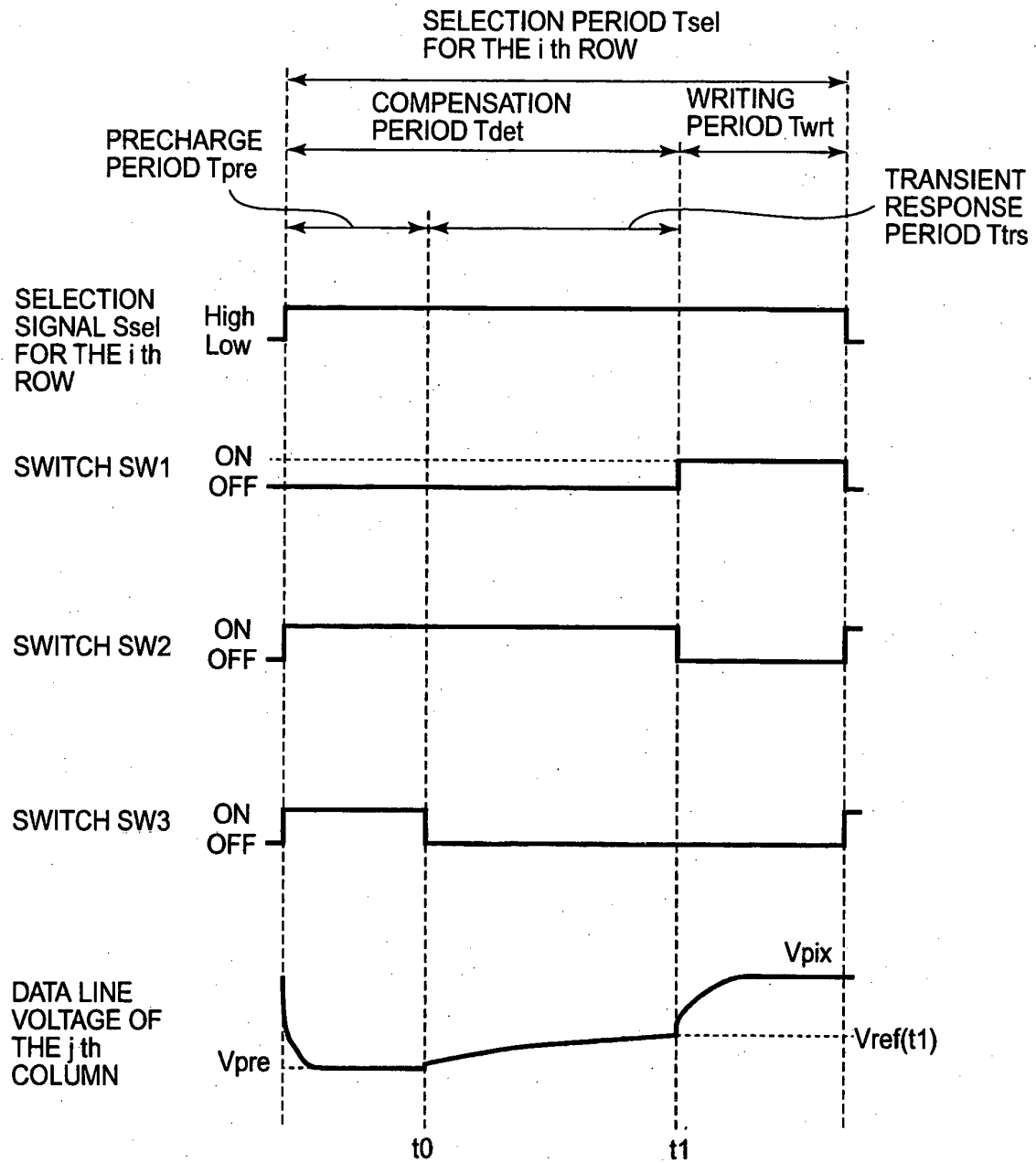


FIG. 14

DURING PRECHARGE OPERATION

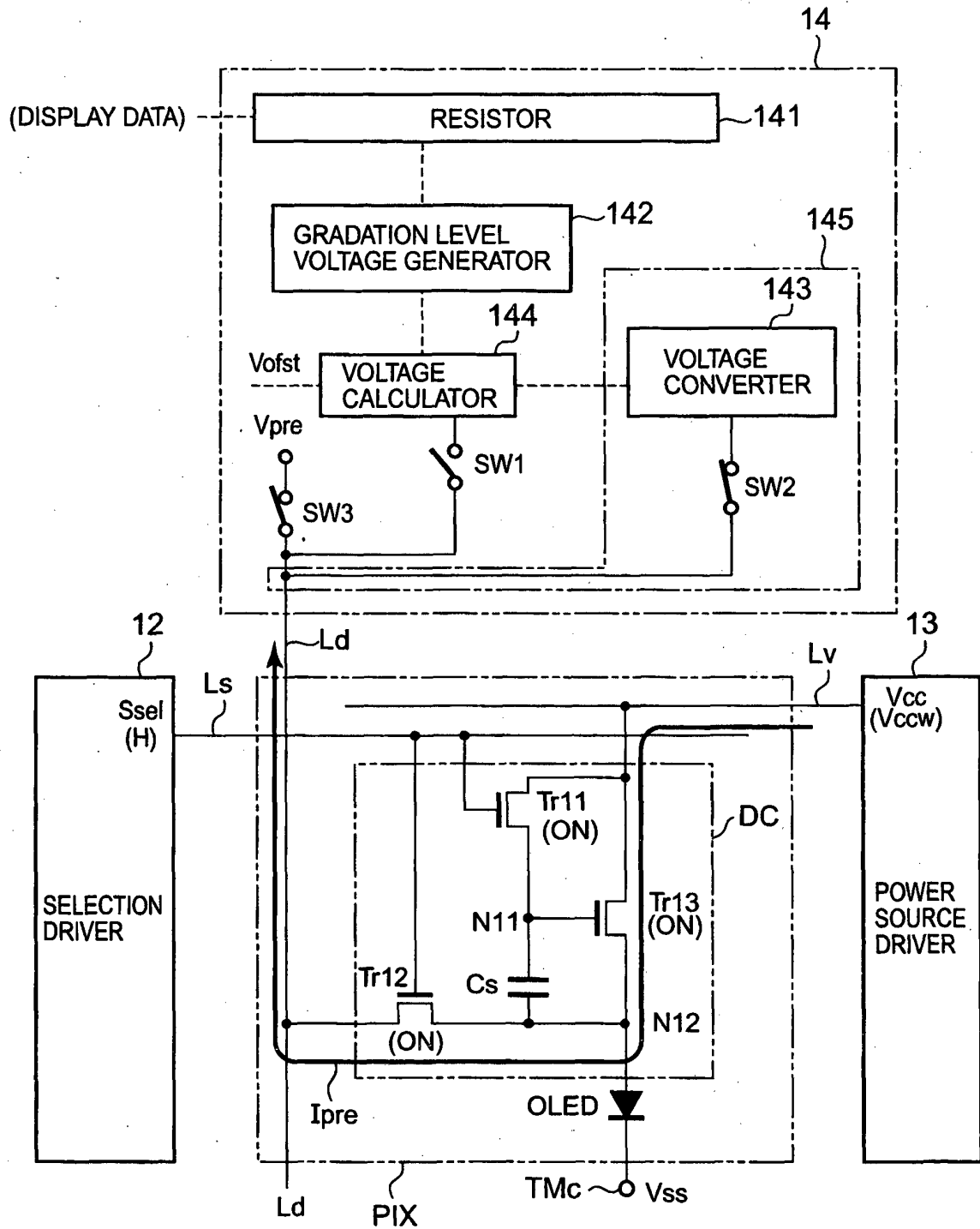


FIG. 15

DURING READING OPERATION OF REFERENCE SIGNAL

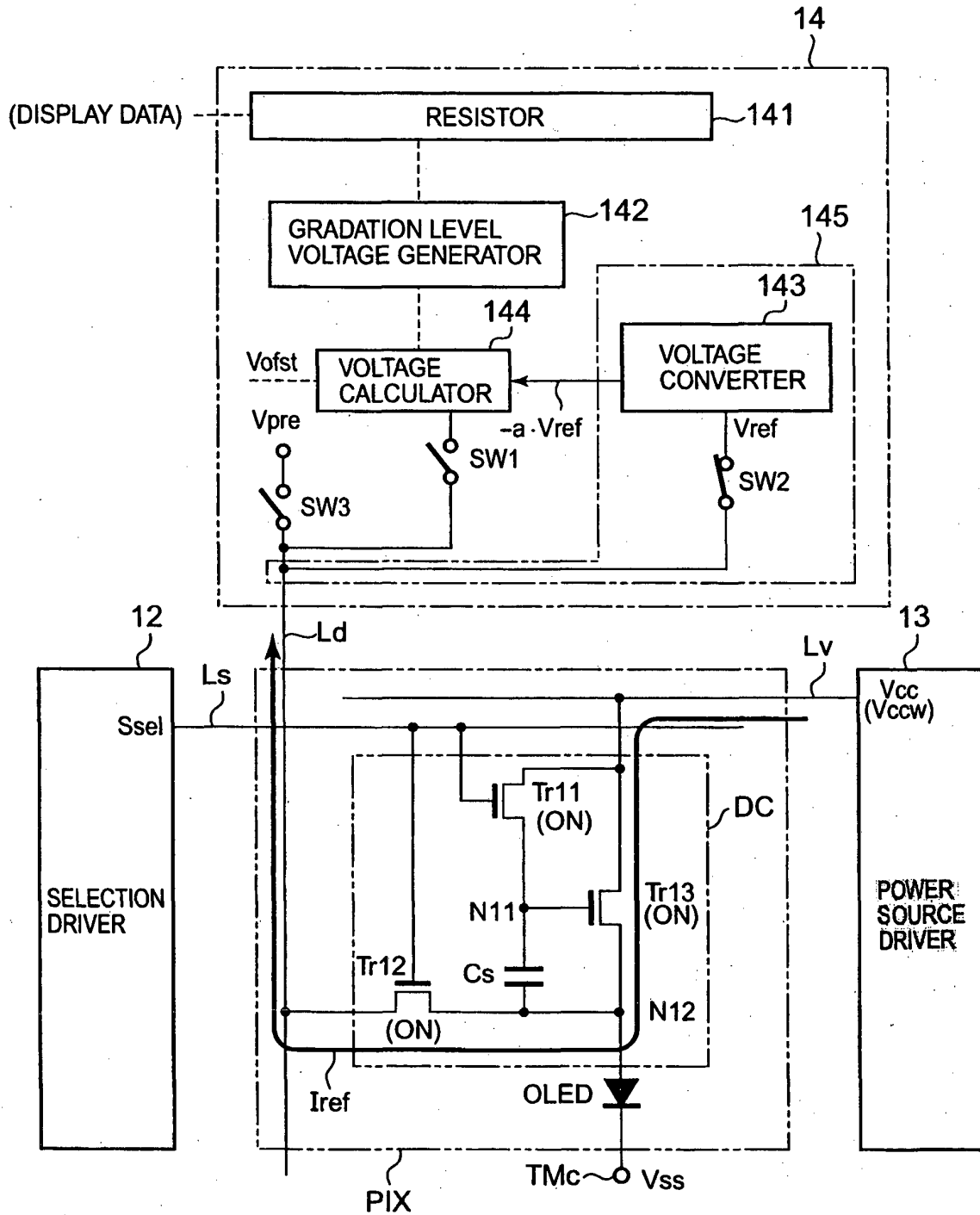


FIG. 16

DURING WRITING OPERATION

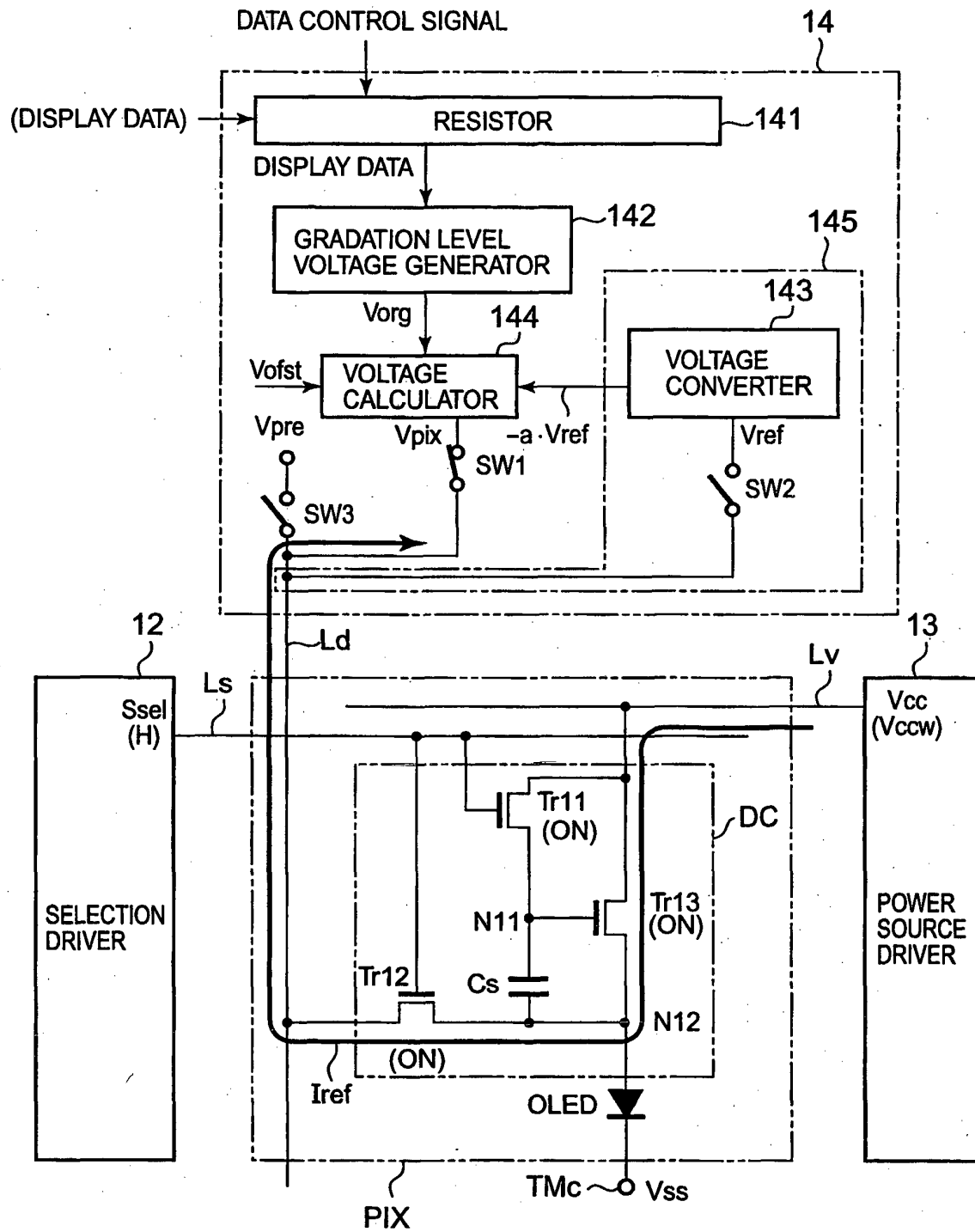


FIG. 17

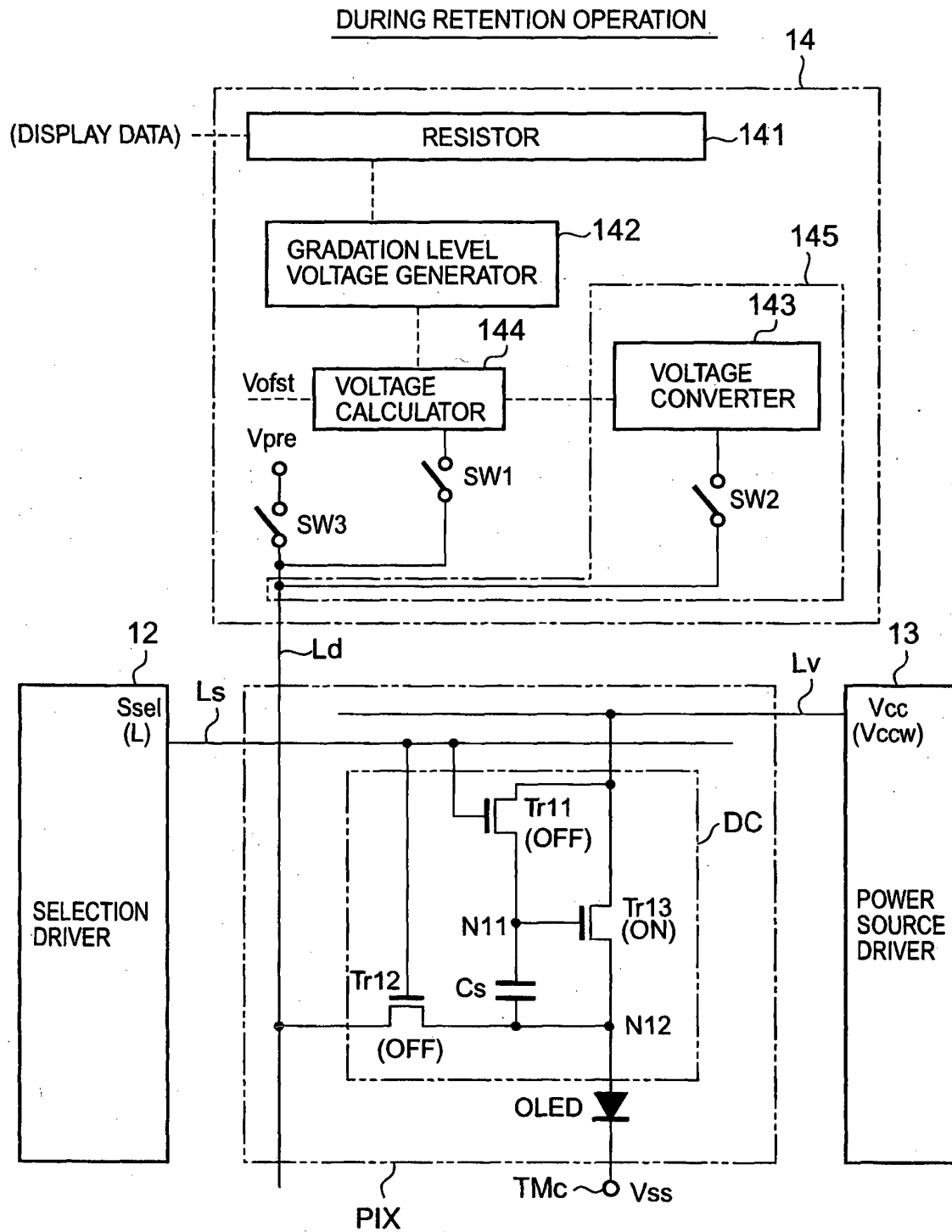


FIG. 18

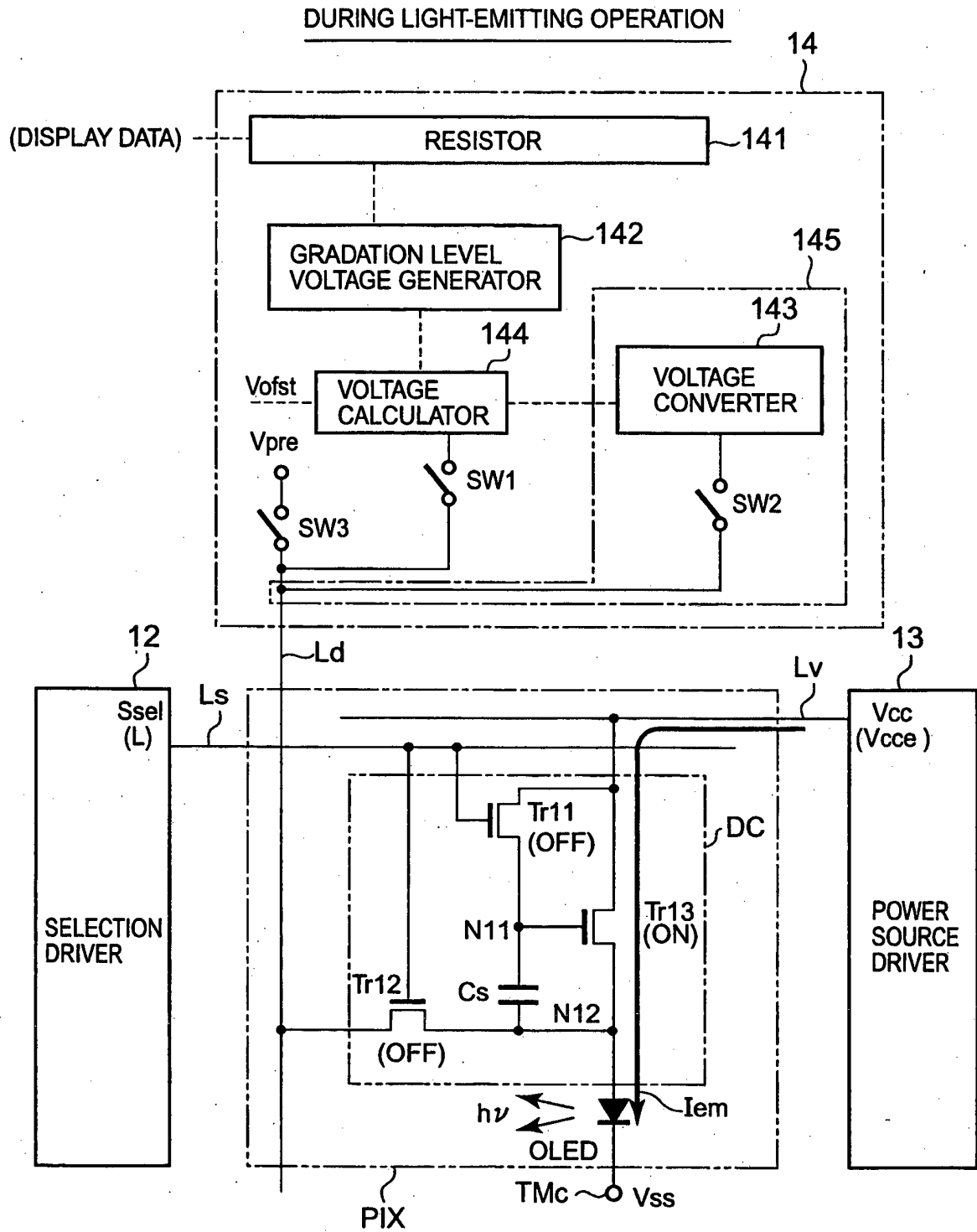


FIG. 19

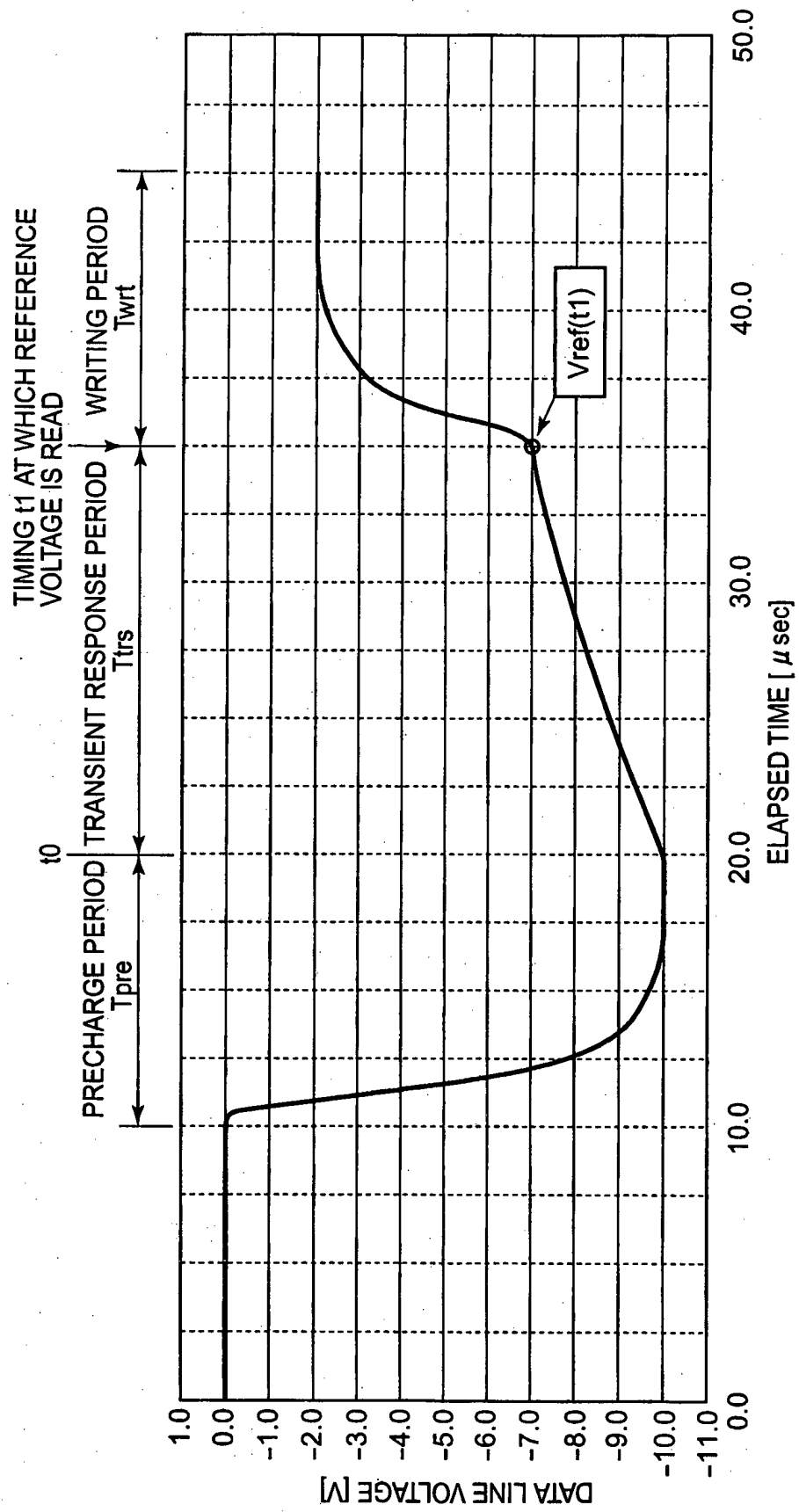


FIG. 20

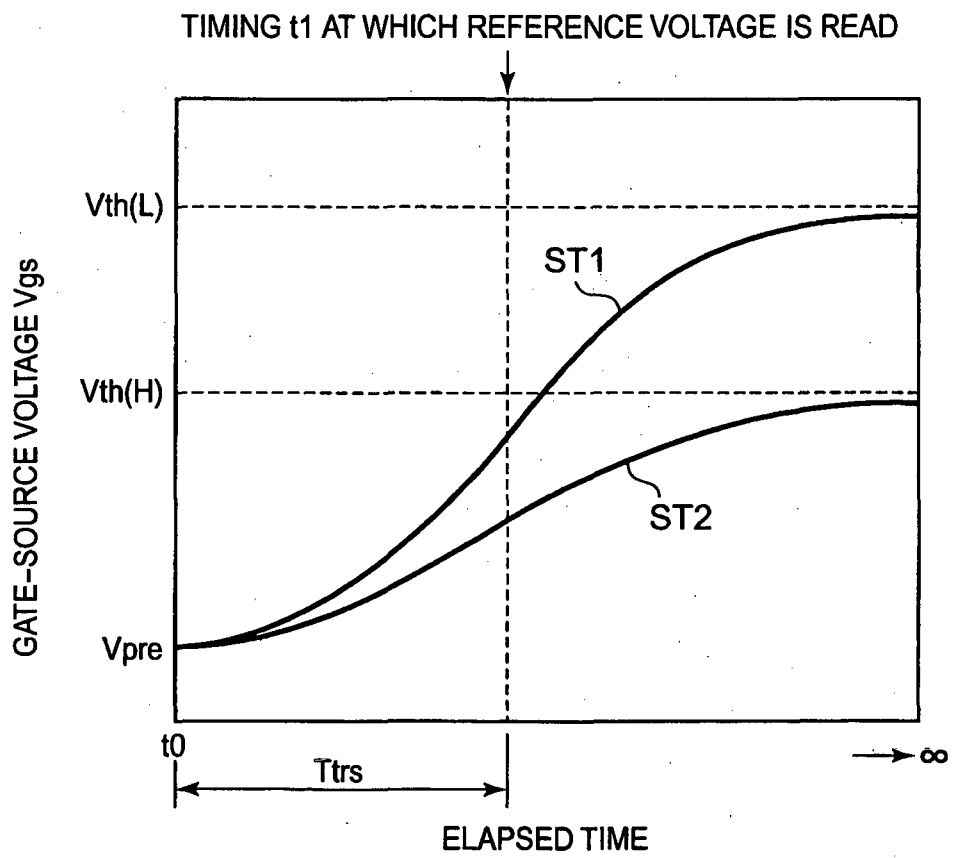


FIG. 21

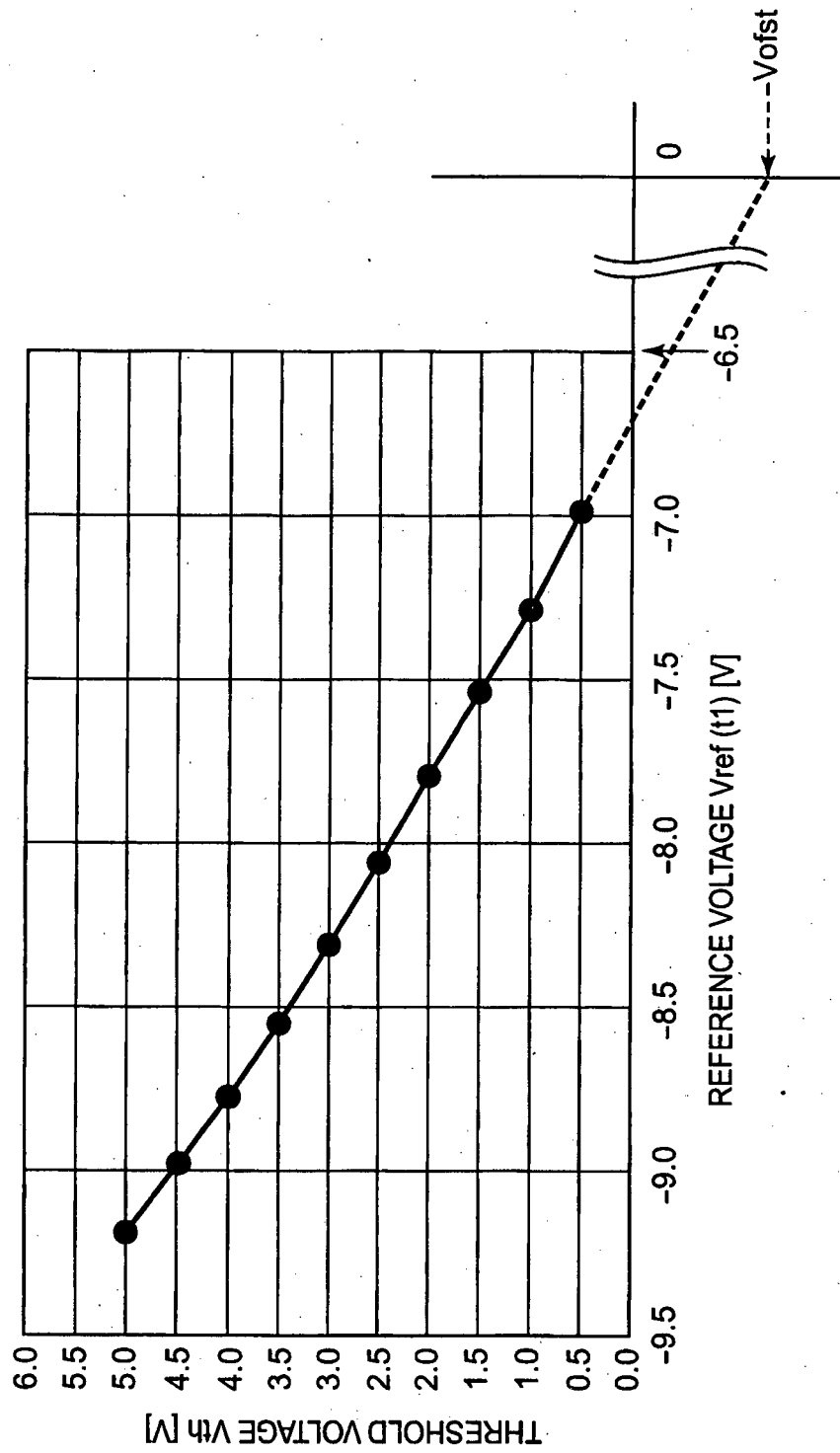


FIG. 22

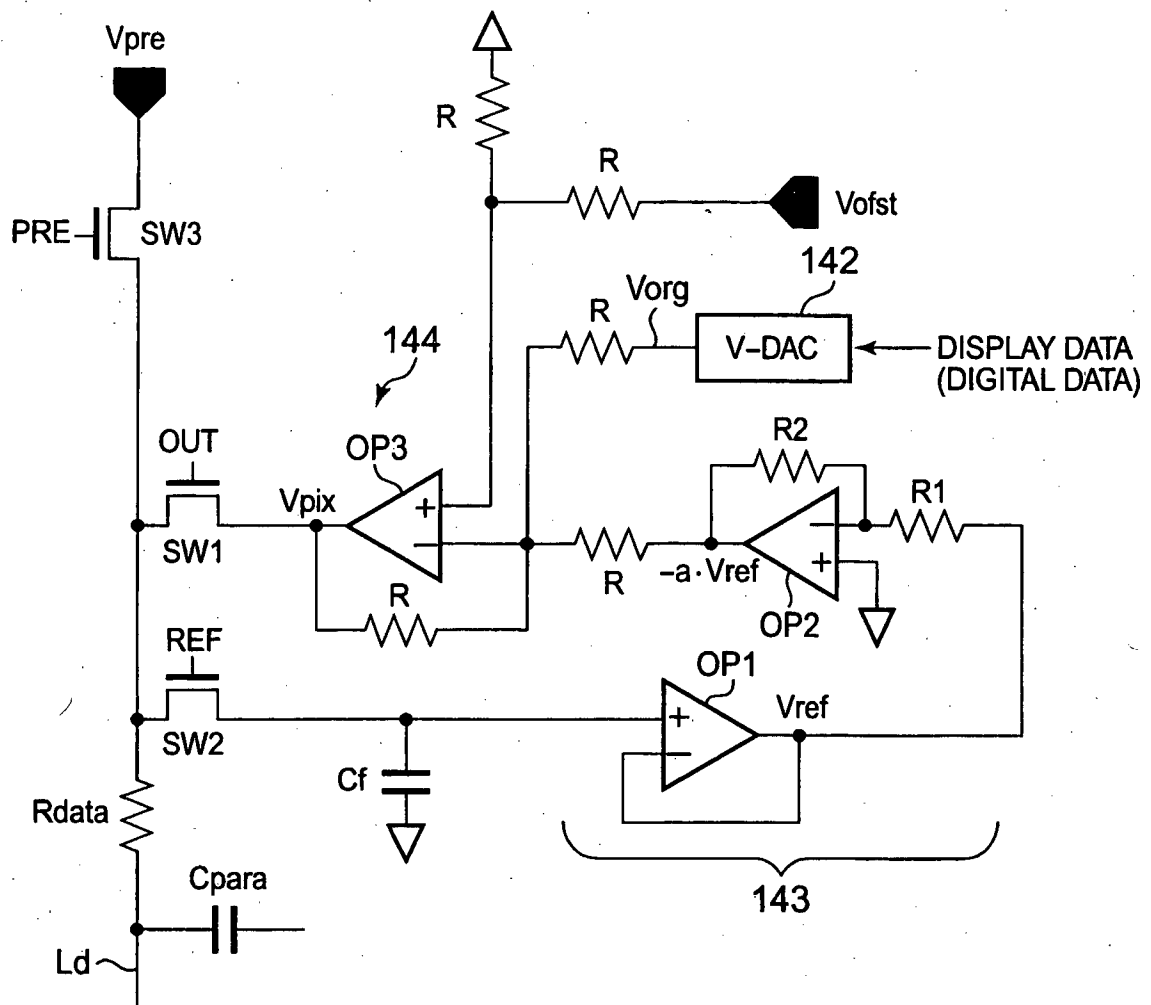


FIG. 23

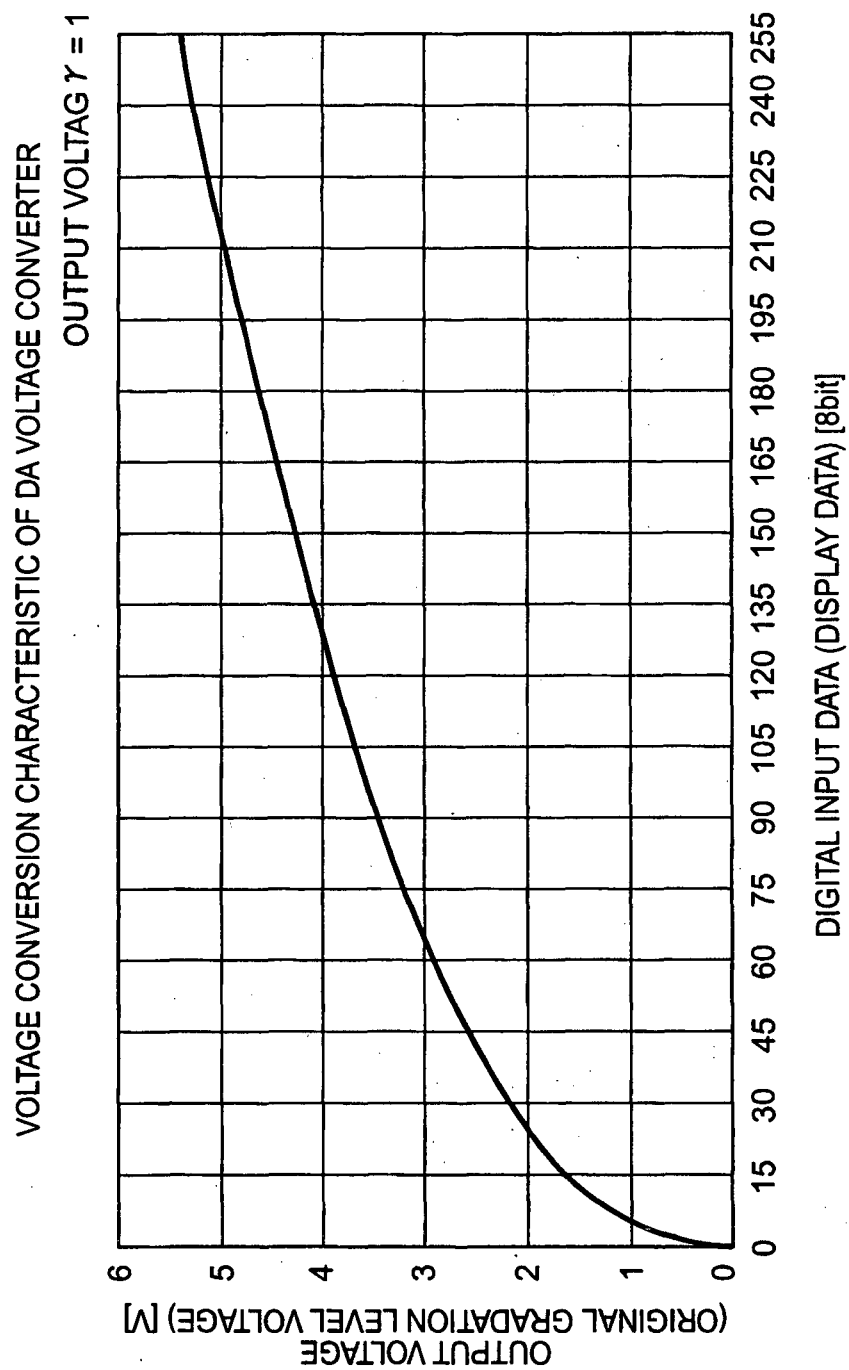
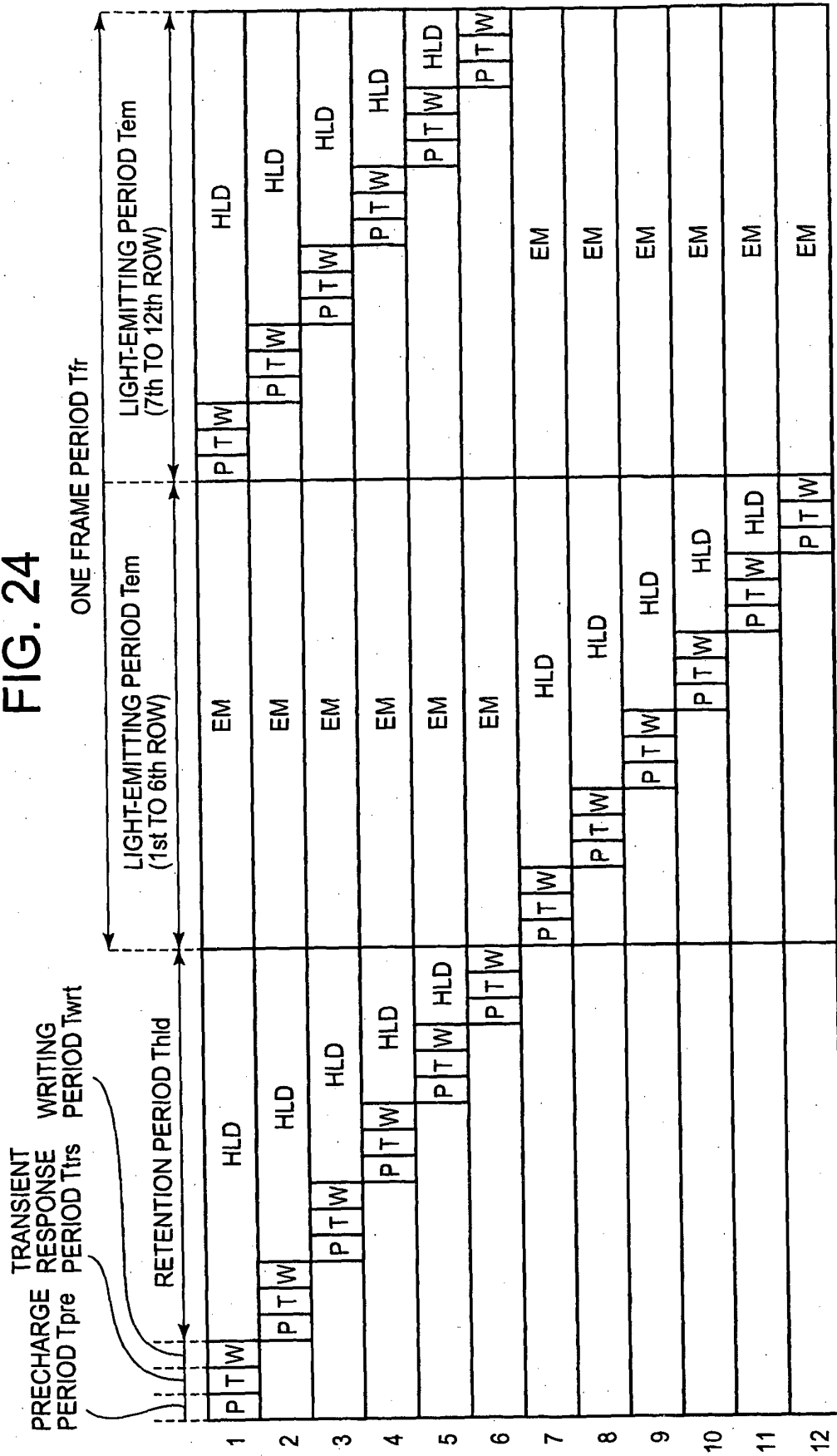


FIG. 24



P PRECHARGE OPERATION, T TRANSIENT RESPONSE, W WRITING OPERATION,
HLD RETENTION OPERATION, EM LIGHT-EMITTING OPERATION

FIG. 25

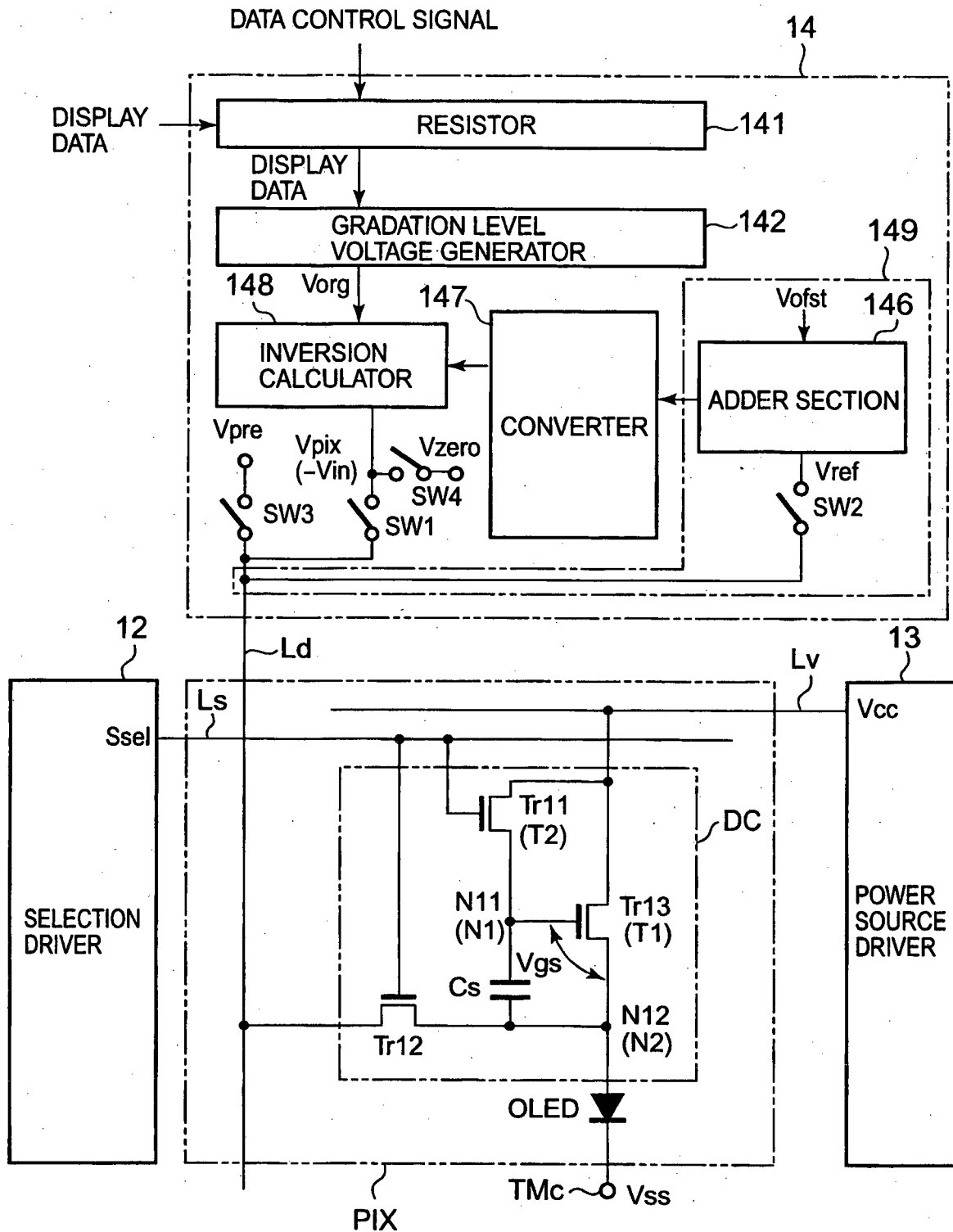


FIG. 26A

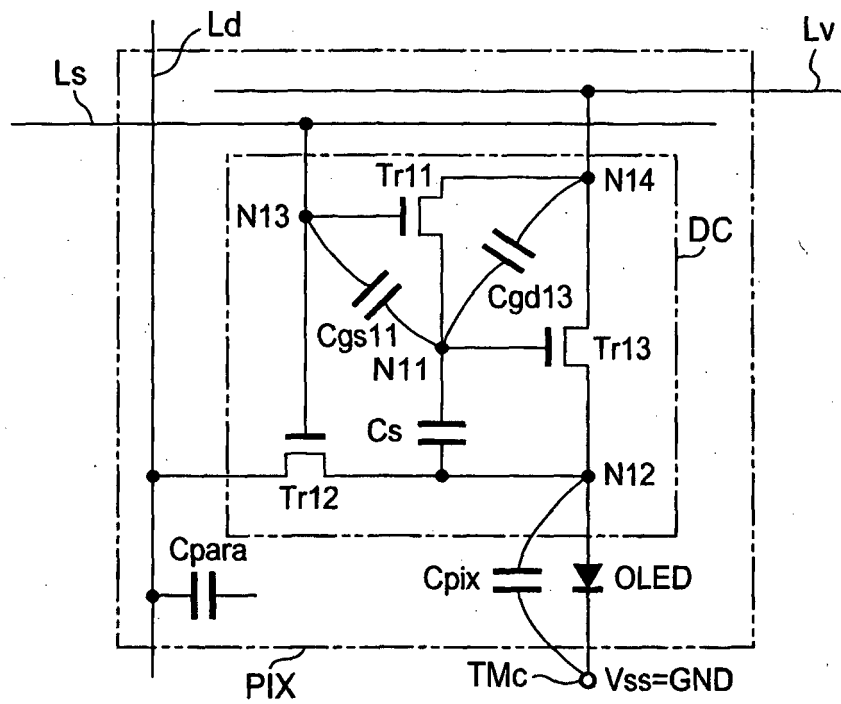


FIG. 26B

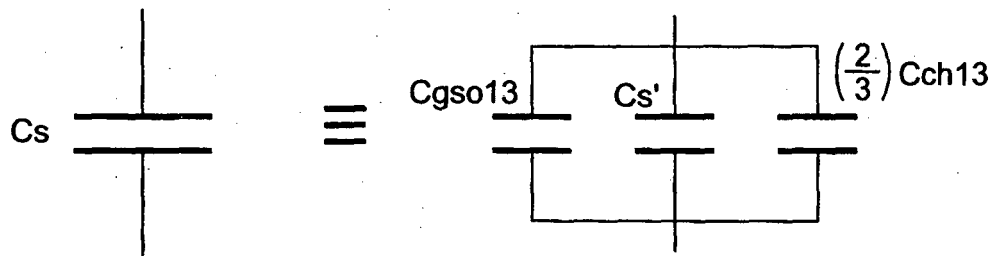


FIG. 27A

EQUIVALENT CIRCUIT DURING
WRITING OPERATION

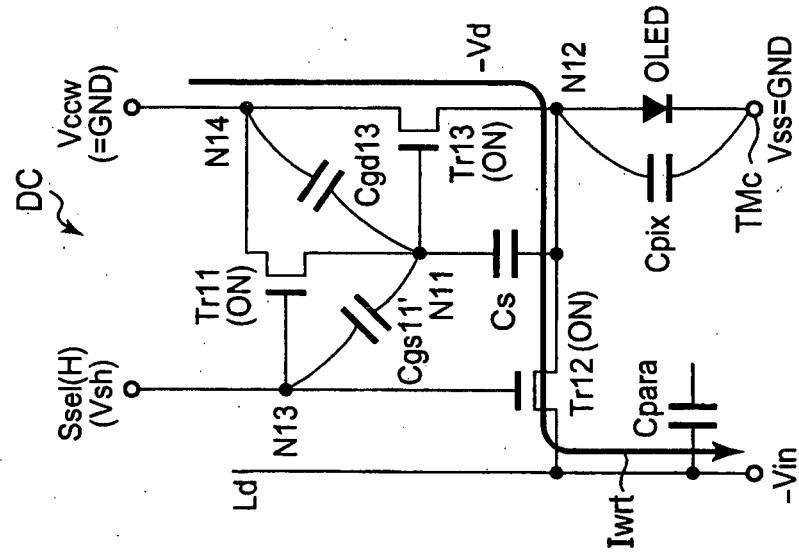


FIG. 27B

EQUIVALENT CIRCUIT DURING
LIGHT-EMITTING OPERATION

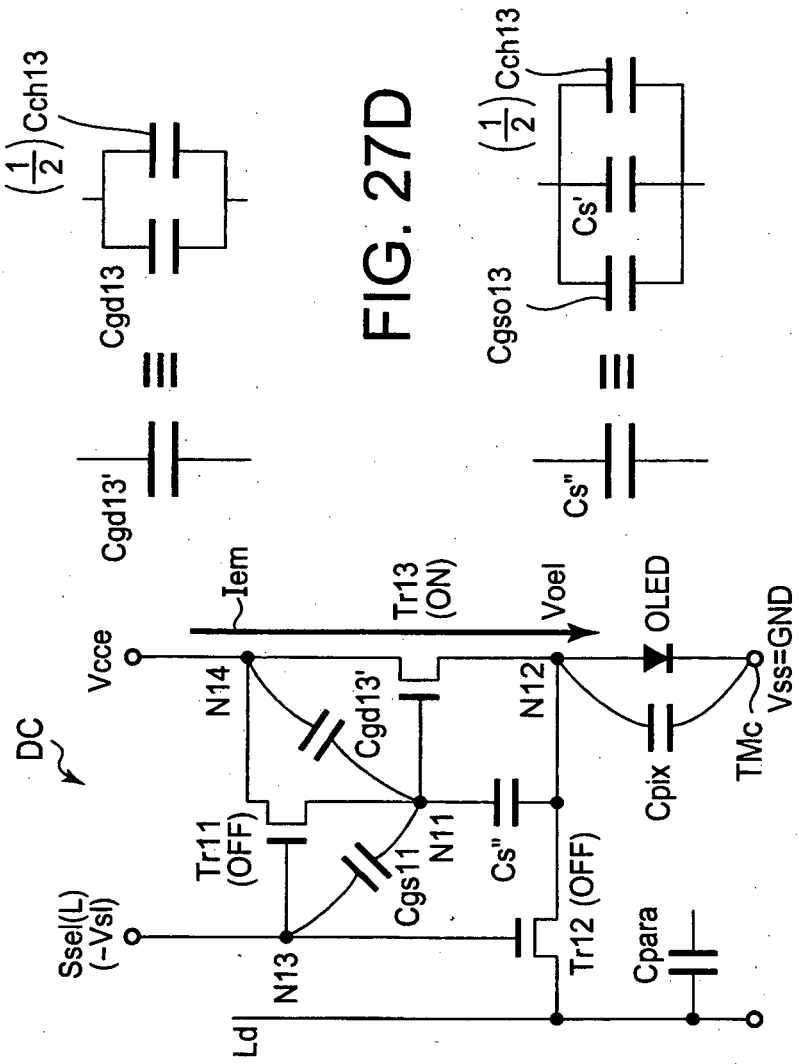


FIG. 27D

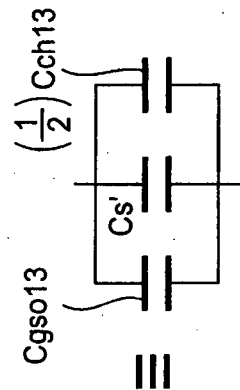


FIG. 28A

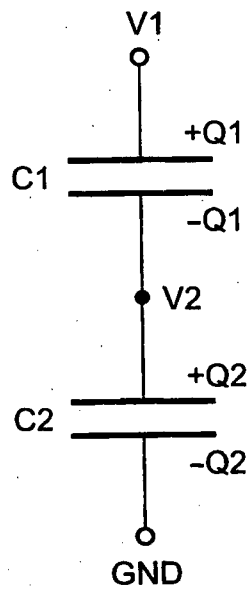


FIG. 28B

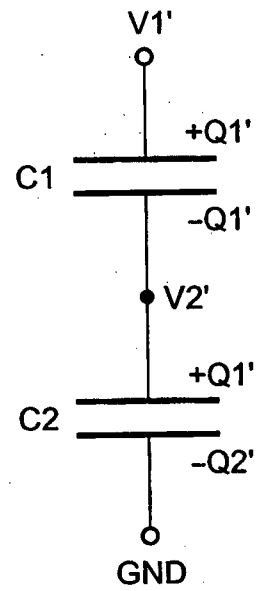


FIG. 29A

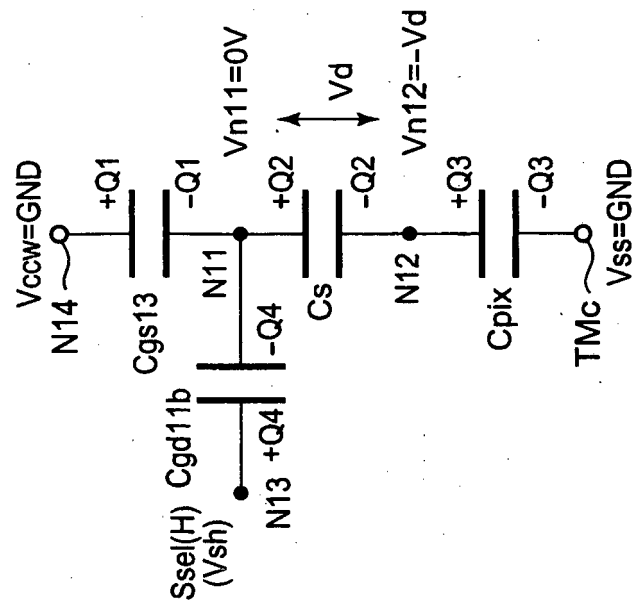


FIG. 29B

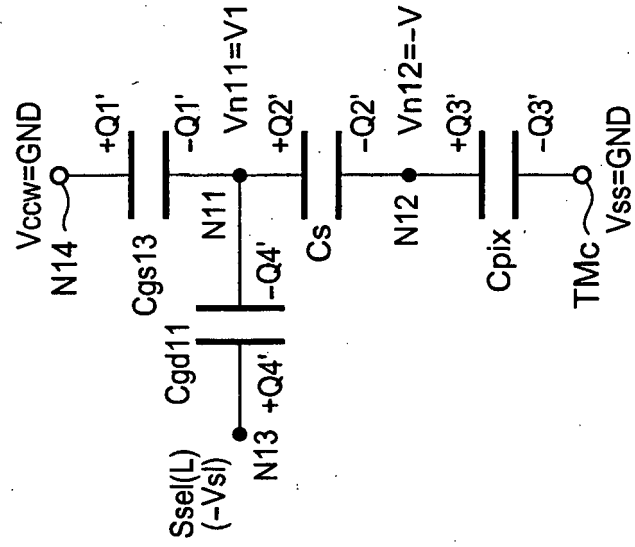


FIG. 33

DURING WRITING OPERATION

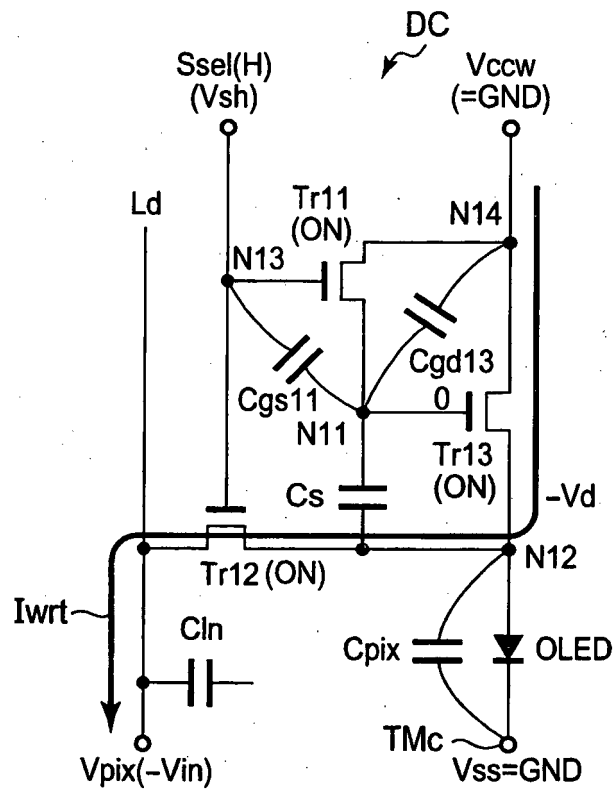


FIG. 34

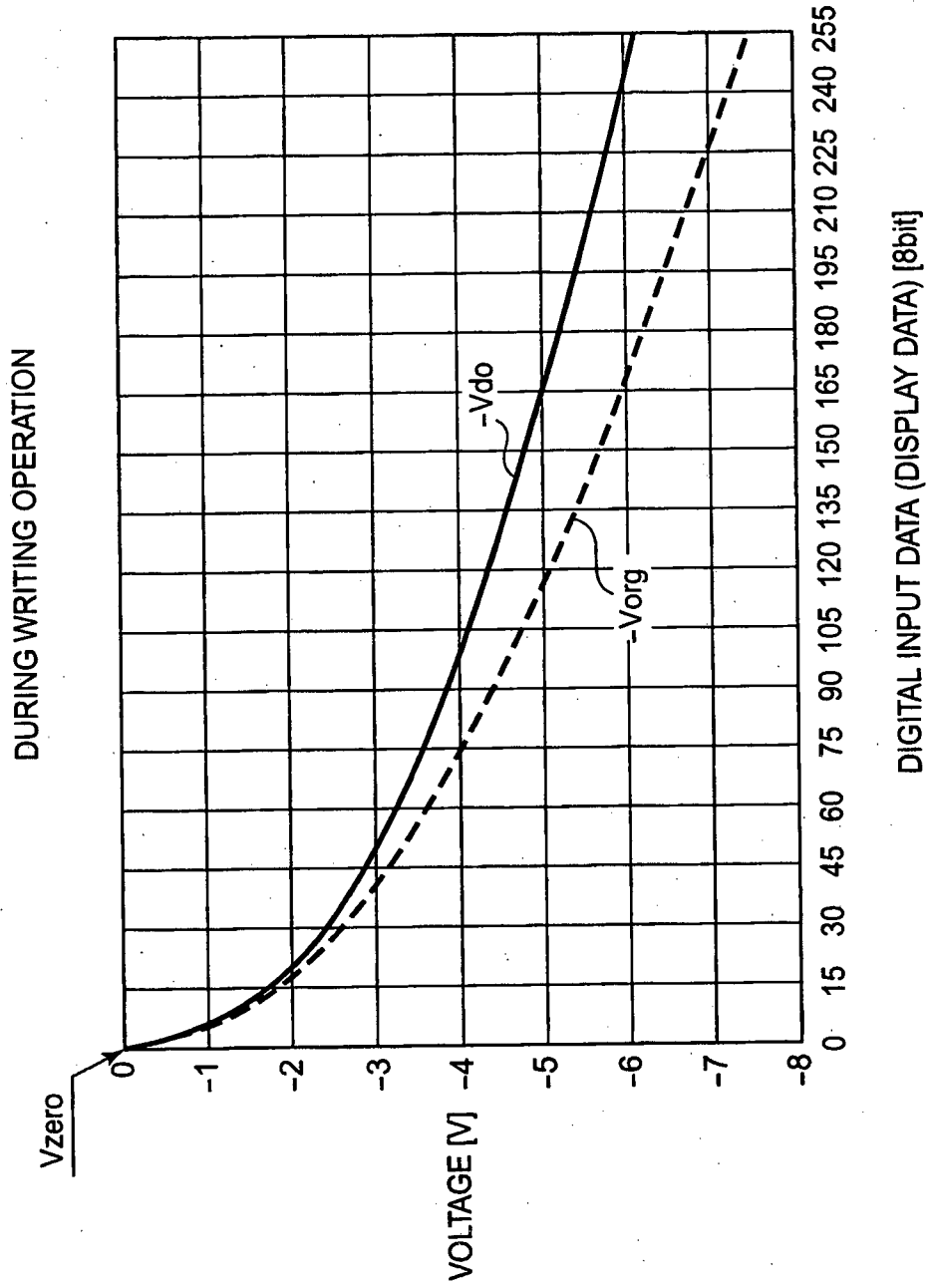


FIG. 35

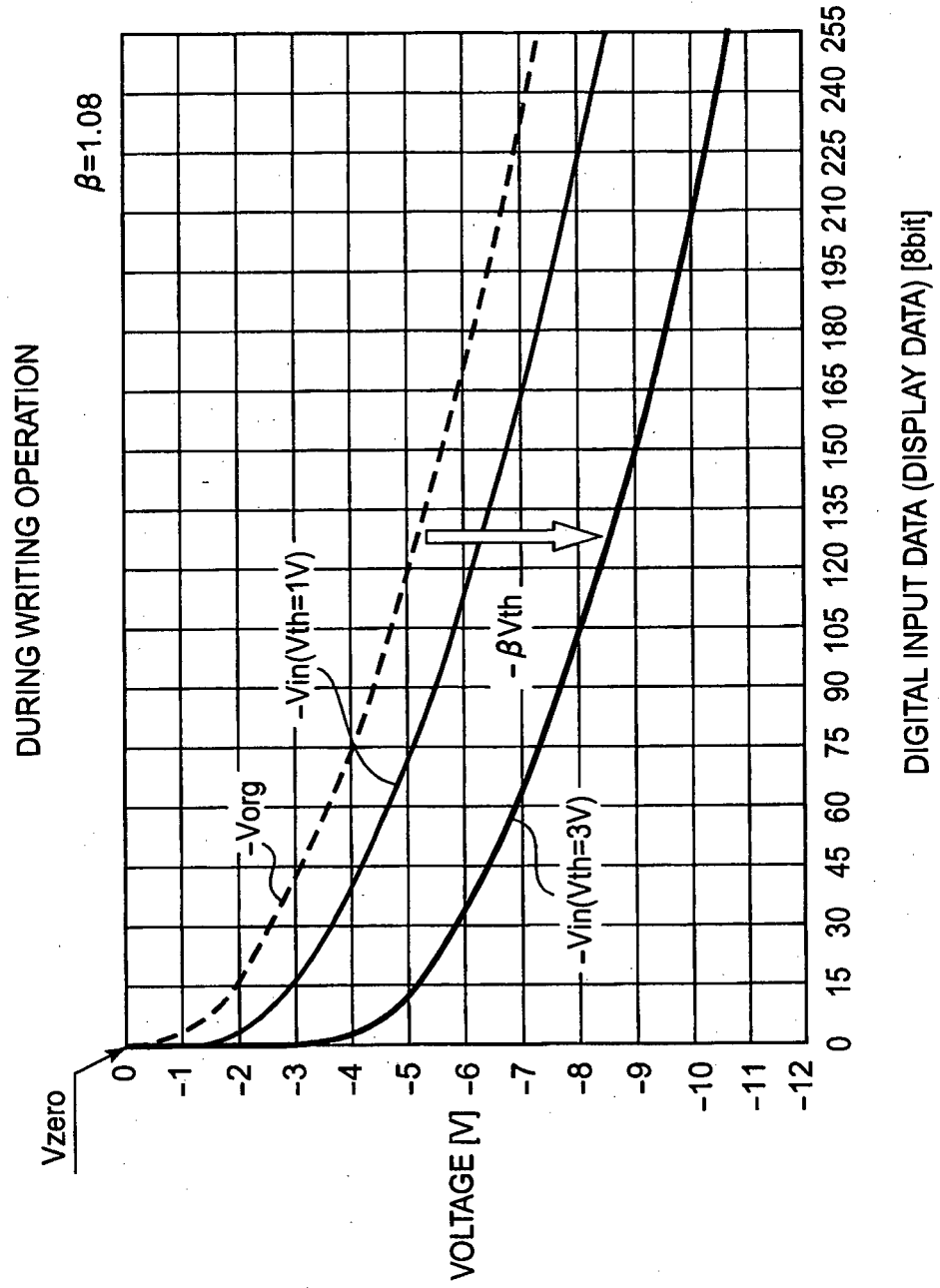


FIG. 36A

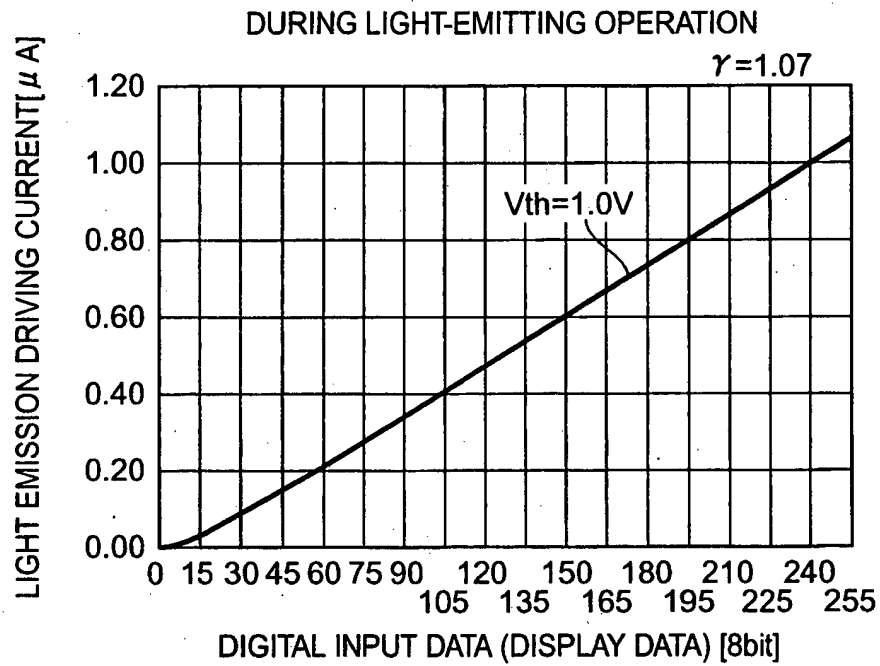


FIG. 36B

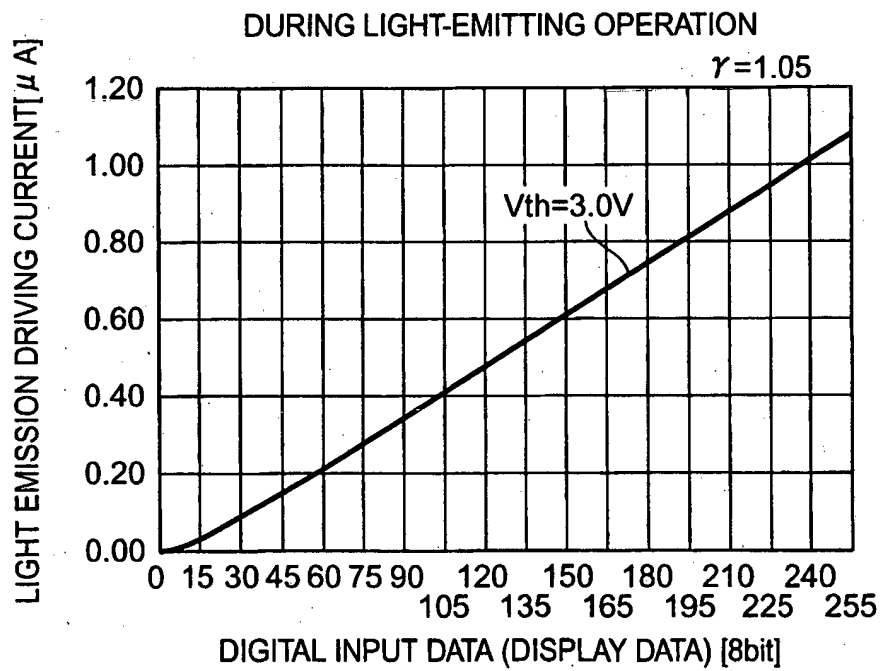


FIG. 37A

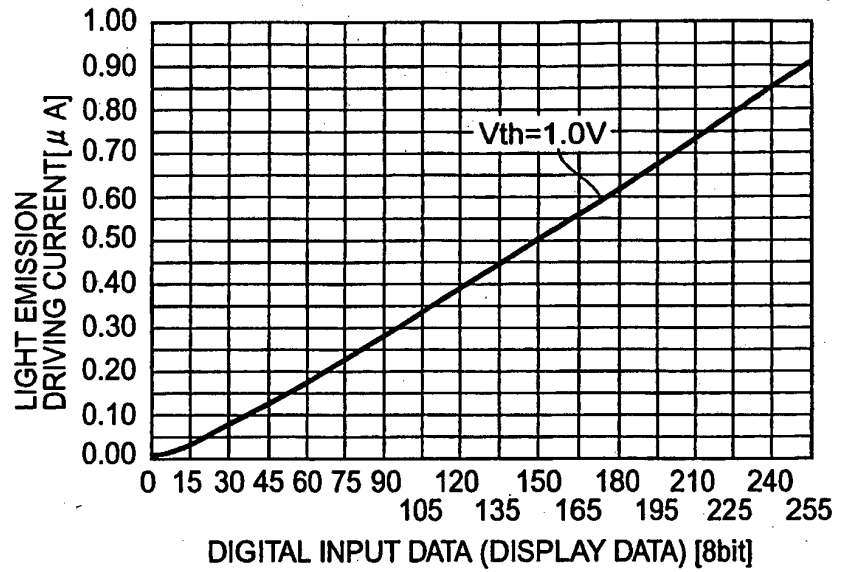


FIG. 37B

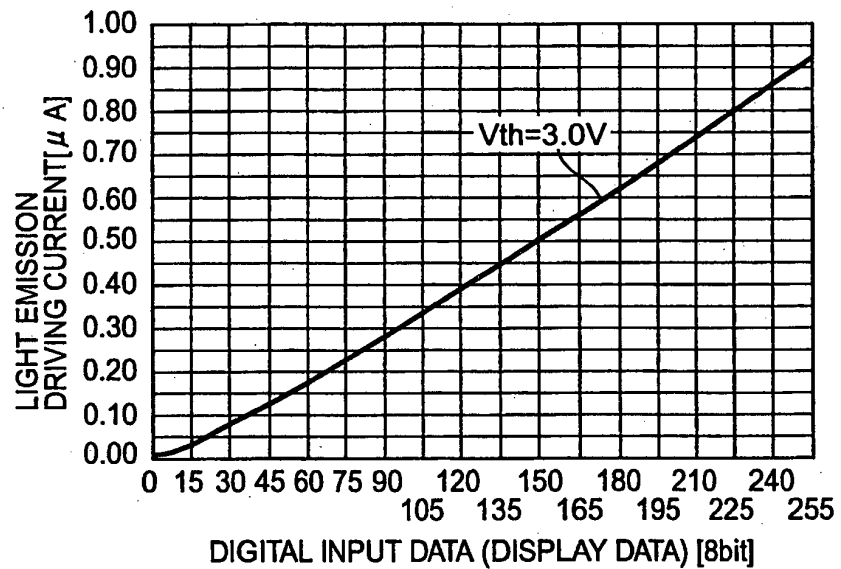


FIG. 37C

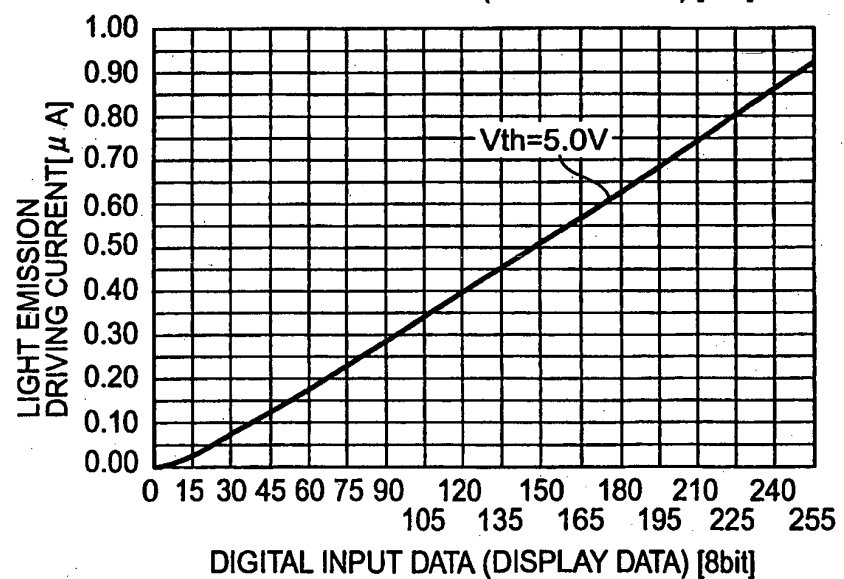


FIG. 38A

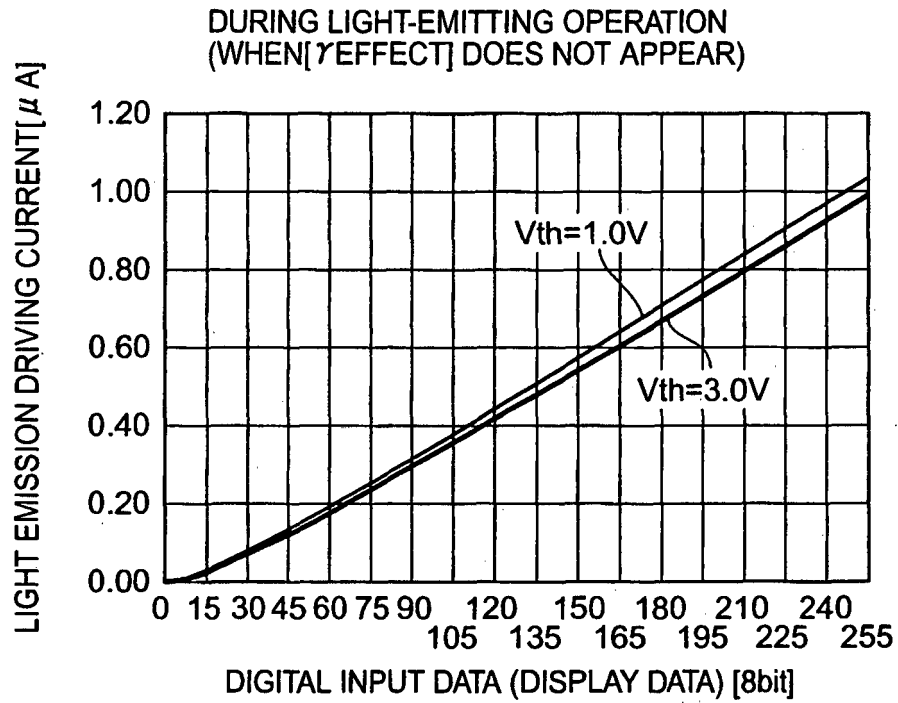


FIG. 38B

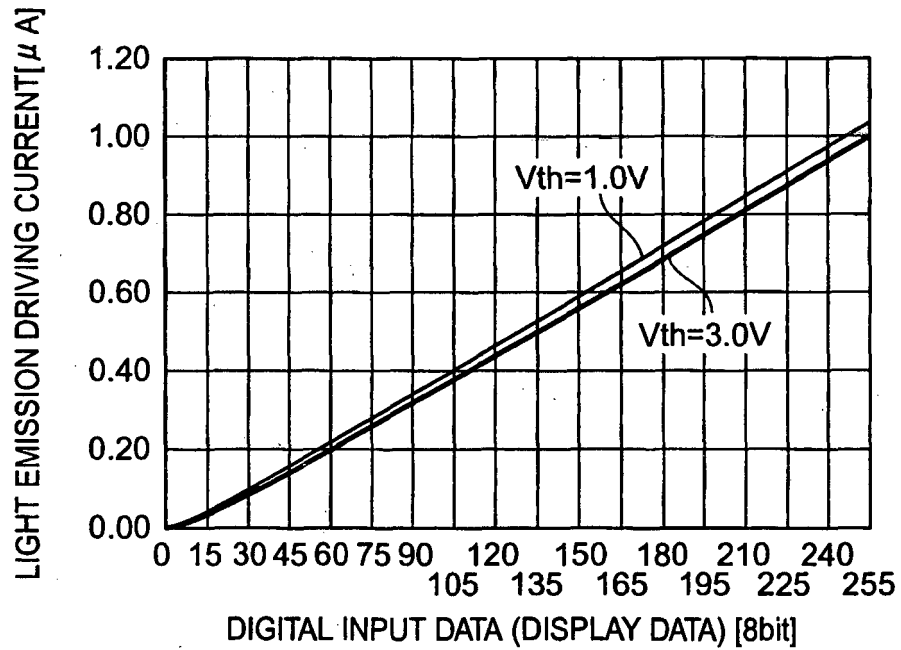


FIG. 39

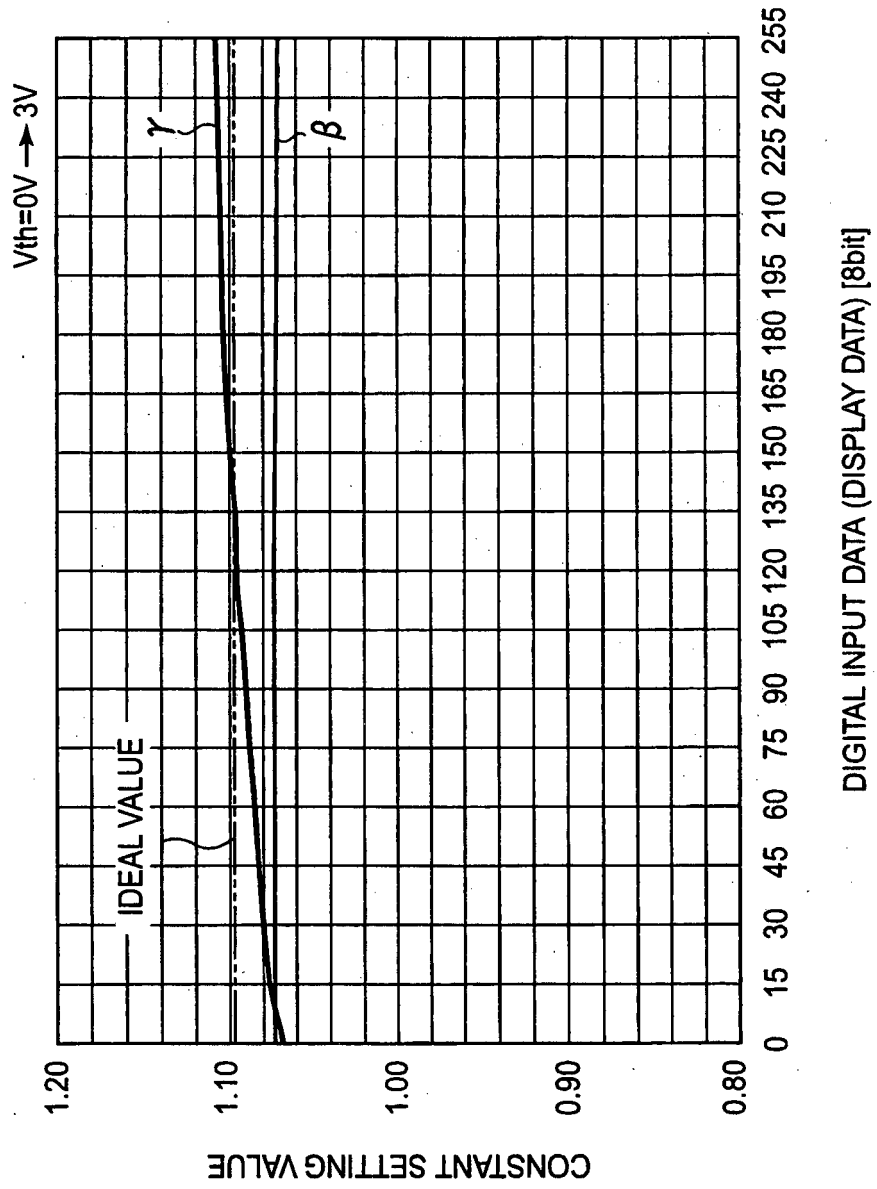


FIG. 40

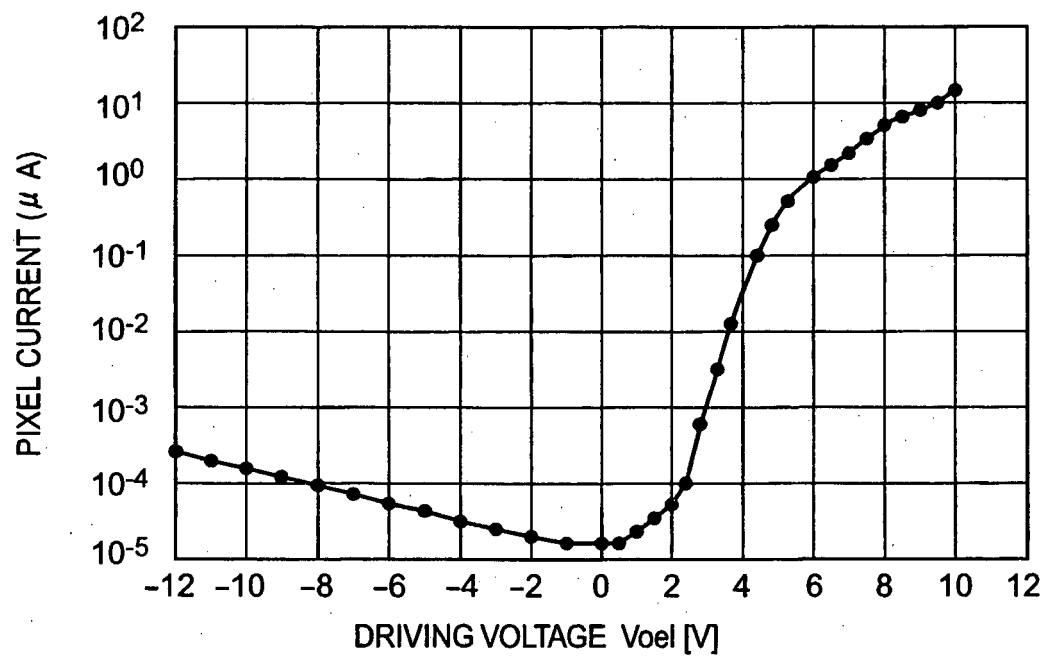
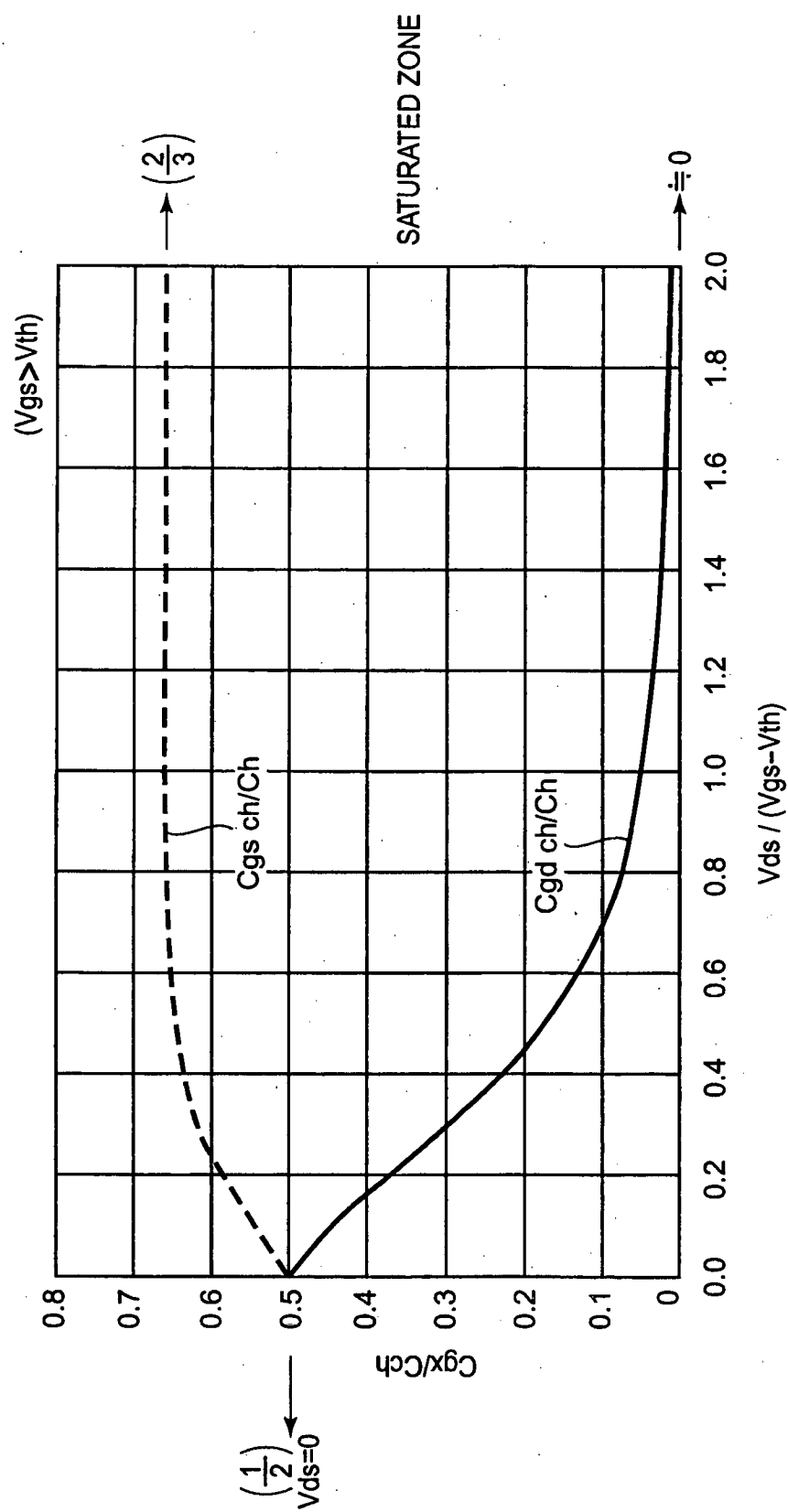


FIG. 41



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- JP H8330600 B [0003] [0004]
- US 20050088103 A [0005]

专利名称(译)	用于驱动显示驱动装置的显示驱动装置和方法，以及用于驱动显示装置的显示装置和方法		
公开(公告)号	EP2067135B1	公开(公告)日	2018-08-01
申请号	EP2007828894	申请日	2007-09-25
[标]申请(专利权)人(译)	卡西欧计算机株式会社		
申请(专利权)人(译)	CASIO COMPUTER CO. , LTD.		
[标]发明人	OGURA JUN		
发明人	OGURA, JUN		
IPC分类号	G09G3/3275 G09G3/3233		
CPC分类号	G09G3/3275 G09G3/3233 G09G2300/0842 G09G2300/0866 G09G2310/0218 G09G2310/0251 G09G2310/027 G09G2320/0233 G09G2320/0261 G09G2320/0295 G09G2320/043		
优先权	2007078963 2007-03-26 JP 2006258717 2006-09-25 JP		
其他公开文献	EP2067135A1		

摘要(译)

根据显示数据，使发光元件（OLED）以优选的亮度和灰度等级发光。在预充电时段期间，数据驱动器经由数据线（Ld）将预充电电压（Vpre）施加到电容器（Cs）。在施加预充电电压之后，电压转换器在瞬态响应时段（Ttrs）之后读取参考电压Vref以产生补偿电压（a·Vref）。电压计算器基于补偿电压（a·Vref）补偿具有根据由灰度级电压发生器产生的显示数据的值的原始灰度级电压Vorg。结果，电压计算器产生补偿灰度级电压Vpix，其对应于用于驱动发光的晶体管Tr13的元件特性的变化量，以将补偿的灰度级电压Vpix施加到数据线Ld。

$$V_{ds} = V_{th} + V_{eff} \quad (1)$$