(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 610 291 A1

(12) EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:
28.12.2005 Bulletin 2005/52

(21) Application number: **03770115.8**

(22) Date of filing: **31.10.2003**

(51) Int Cl.[7]: **G09G 3/30**, G09G 3/28, G09G 3/20, H05B 33/14

(86) International application number:
PCT/JP2003/014042

(87) International publication number:
WO 2004/088623 (14.10.2004 Gazette 2004/42)

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR
Designated Extension States:
AL LT LV MK

(30) Priority: **28.03.2003 JP 2003092534**
30.07.2003 JP 2003204018
27.10.2003 JP 2003366130

(71) Applicant: **SHARP KABUSHIKI KAISHA**
Osaka-shi, Osaka 545-8522 (JP)

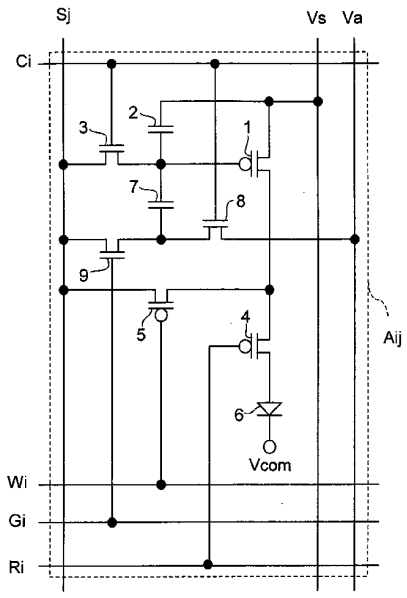
(72) Inventor: **NUMAO, Takaji**
Nara-shi, Nara 630-8115 (JP)

(74) Representative: **Brown, Kenneth Richard et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

(54) DISPLAY DEVICE AND DRIVE METHOD THEREOF

(57) A switching transistor 3 is provided between a gate terminal of a driving TFT 1 and a drain terminal thereof. A first capacitor 2 is provided between the gate terminal of the driving TFT 1 and a source terminal thereof. The current control terminal of the driving TFT 1 is connected to a first terminal of a second capacitor 7. A second terminal of the second capacitor 7 is connected to the drain terminal of the driving TFT 1 via a switching transistor 9, and to a predetermined voltage line Va via a switching transistor 8. This allows restraint of variation of a current flowing, during a non-selection period, through a current driving light emitting element of a display apparatus, the current variation being caused by threshold voltage variation and mobility variation of the driving TFT. A specific example of the display apparatus including such a current driving light emitting element is an organic EL display apparatus.

FIG. 1



EP 1 610 291 A1

Description

TECHNICAL FIELD

[0001] The present invention relates to (i) a display apparatus using a current driving element, such as an organic EL (Electro Luminescence) display and an FED (Field Emission Display); and (ii) a method for driving the display apparatus.

BACKGROUND ART

[0002] What have been actively carried out in recent years are researches and developments for a current driving light-emitting element such as an organic EL display and an FED. Especially, the organic EL display is such a display that can emit light by a low voltage and less power consumption, so that the organic EL display has drawn attention as a display for a mobile device such as a mobile phone or a PDA (Personal Digital Assistants).

[0003] As a structure example of a current driving pixel circuit of such an organic EL display, Fig. 22 illustrates a circuit structure described in "Active Matrix PolyLED Displays" (M. T. Johnson et al., IDW '00, 2000, pp.235-238) and WO 99/65011 (published December 16, 1999).

[0004] In the circuit structure shown in Fig. 22, a driving TFT (Thin Film Transistor) 101 has a source terminal connected to a power source wire Vs, and has a gate terminal connected to the power source wire Vs via a capacitor 104. Moreover, a switching TFT 102 is provided between a drain terminal of the driving TFT 101 and an anode of an organic EL element 103. A cathode of the organic EL element 103 is connected to a common wire Vcom.

[0005] Further, a selection TFT 106 and a switching TFT 105 are provided at a node of the driving TFT 101 and the switching TFT 102. The selection TFT 106 has a source terminal connected to a source wire Sj. The switching TFT 105 has a source terminal connected to the gate terminal of the driving TFT 101.

[0006] In the structure, when a signal indicative of Low is supplied to a scan wire Gi (selection period), the switching TFT 102 becomes OFF, and the selection TFT 106 and the switching TFT element 105 becomes ON. In this case, a current can flow from the power source wire Vs to the source wire Sj via the driving TFT 101 and the selection TFT 106. In cases where the current thus flowing is controlled by a power source of a source driver circuit (not shown) connected to the source wire Sj, a gate voltage of the driving TFT element 101 is set such that a current specified by the source driver circuit flows into the driving TFT 101.

[0007] On the other hand, when the scan wire Gi receives a signal indicative of High (non-selection period), the selection TFT 106 and the switching TFT 105 become OFF, and the switching TFT 102 becomes ON. During this non-selection period, the capacitor 104 retains the gate potential, determined during the selection period, of the driving TFT element 101. With this, during the non-selection period, the driving TFT 101 allows the determined current to flow into the organic EL element 103.

[0008] As an example of a current driving pixel circuit structure similar to the above structure, Fig. 23 illustrates a pixel circuit structure described in "Polysilicon TFT Drivers for Light Emitting Polymer Displays" (Simon W-B. Tam et al., IDW '99, 1999, pp.175-178) and WO 98/48403 (published on October 29, 1998).

[0009] In the circuit structure shown in Fig. 23, a capacitor 111 is provided between a source terminal of a driving TFT 108 and a gate terminal thereof. Between the gate terminal of the driving TFT 108 and a drain terminal thereof, a switching TFT 112 is provided. The drain terminal of the driving TFT 108 is connected to an anode of an organic EL element 109. Further, a switching TFT 107 is provided between the source terminal of the driving TFT 108 and a power source wire Vs. Moreover, a selection TFT 110 is provided between the source terminal of the driving TFT 108 and a source wire Sj.

[0010] The selection TFT 110 has a gate terminal connected to a control wire Wi, and the switching TFT 107 has a gate terminal connected to a control wire Ri, and the switching TFT 112 has a gate terminal connected to a scan wire Gi.

[0011] The following explains an operation of the pixel circuit structure with reference to a timing chart shown in Fig. 24. The timing chart illustrates respective timings of supplying signals to the control wires Wi and Ri, the scan wire Gi, and the source wire Sj.

[0012] In Fig. 24, the selection period corresponds to a period of time from 0 to 3t1. During the selection period, the control wire Ri has a High (GH) potential, so that the switching TFT 107 is OFF. On this occasion, the control wire Wi has a Low (GL) potential, so that the selection TFT 110 is ON. With this, during the selection period, a current flows from the source wire Sj to the organic EL element 109 via the selection TFT 110 and the driving TFT 108.

[0013] During a period of time from 0 to 2t1 within the selection period, the scan wire Gi has a High potential, so that the switching TFT 112 is ON. Accordingly, a current flows from (i) a source driver circuit (not shown) connected to the source wire Sj, to (ii) the organic EL element 109. This determines a gate potential of the driving TFT 108 such that a current specified by the source driver circuit flows into the organic EL element 109. During a period of time from 2t1 to 3t1, the switching TFT 112 is OFF; however, the gate potential of the driving TFT 108 is retained by the capacitor

111. This allows a current to flow from the source wire Sj to the organic EL element 109 during this period, too.

[0014] After the time 3t1 (non-selection period), the switching TFT 110 is OFF, and the switching TFT 107 is ON. With this, during the non-selection period, a determined current is controlled to flow from the power source wire Vs to the organic EL element 109.

[0015] However, the following problem arises in the pixel circuit structure described in "Polysilicon TFT Drivers for Light Emitting Polymer Displays" (IDW '99, pp.175-178). That is, variation in a threshold voltage of the driving TFT 108, and variation in mobility thereof cause variation in the current flowing into the organic EL element 109 during the non-selection period.

[0016] For the purpose of clarifying an adverse effect of such variation of the current, a simulation was carried out under the following five conditions shown in Table 1 below. The simulation found respective values of currents flowing to the organic EL element 109. The simulation result is shown in Fig. 25.

[Table 1]

	Ioled(1)	Ioled(2)	Ioled(3)	Ioled(4)	Ioled(5)
Threshold voltage	Average value	Lower limit value	Upper limit value	Upper limit value	Lower limit value
Mobility	Average value	Lower limit value	Upper limit value	Lower limit value	Upper limit value

[0017] In the simulation shown in Fig. 25, the selection period came every 0.24 ms. During an initial period of time from 0.27 ms to 0.51 ms, a current of 0.1 μA flowed to the source wire Sj. Thereafter, the current was increased by 0.1 μA every 0.24 ms until the current had a value of 0.9 μA. Then, the current was set at 0. After that, the current was increased again by 0.1 μA.

[0018] Specifically, a first selection period corresponds to a period of time from 0.27 ms to 0.30 ms. The current, which had a value of 0.1 μA and which was flowing to the source wire Sj during the selection period, determined the potential of the gate terminal of the driving TFT 108. This determined that the current of 0.1 μA flowed to the organic EL element 109 only during the selection period. Note that the gate potential on this occasion was retained during a following non-selection period continuing from 0.31 ms to 0.51 ms; however, the current flowing to the organic EL element 109 during the non-selection period varied in a range from 0.12 μA to 0.13 μA.

[0019] The variation found by the simulation is illustrated in Fig. 26 whose horizontal axis plots the respective currents (the respective ten currents of 0 to 0.9 μA) which flowed to the source wire Sj, and whose vertical axis plots respective currents which flowed to the organic EL element 109 during the non-selection periods, each of which came after each current supply to the source wire Sj. In Fig. 26, during the non-selection period coming after the supply of the current of 0.9 μA to the source wire Sj, the current that flowed through the organic EL element 109 varied in a range of about 0.95 μA to about 1.12 μA (increases by 5% to 24%).

[0020] Such variation is caused by a difference between (i) a source-drain voltage Vsd of the driving TFT 108 during the selection period (period of time from approximately 270 μs to approximately 300 μs), and (ii) a source-voltage Vsd during the non-selection period (period other than the selection period), as shown in Fig. 27. Note that Fig. 27 illustrates a result of a simulation carried out under the five conditions (see Table 2) of the threshold voltage and the mobility of the driving TFT 108. Note also that voltage values Vsg (1) through Vsg (5) respectively correspond to the conditions Ioled (1) through Ioled (5) (see Table 2), and that voltage values Vsd (1) through Vsg (5) respectively correspond to the conditions Ioled (1) through Ioled (5).

[0021] Namely, in the circuit structure shown in Fig. 23, the switching TFT 112 was ON upon the current writing (period of time from 0 to 2t1 in Fig. 24; period of time from about 270 μs to about 290 μs in Fig. 27) carried out during the selection period, so that each source-drain voltage Vsd coincided with each source-gate voltage Vsg, as shown in Fig. 27.

[0022] The source-gate potential Vsg that the driving TFT 108 had on this occasion was determined according to the threshold voltage of the driving TFT 108 and the mobility thereof. Specifically, comparing (i) a case where the threshold voltage is 1 V with (ii) a case where the threshold voltage is 2V, the source-gate voltages Vsg varies by on the order of 1V. In fact, the above simulation result shows that the source-gate voltage Vsg varied in a range from about 1.4 V to about 3.6 V when the current of 0.1 μA was supplied to the source wire Sj.

[0023] Thereafter, when the switching TFT 112 was turned OFF (at about 290 μs), the source-gate potential of the driving TFT 108 was retained; however, the source-drain voltage Vsd thereof was changed.

[0024] Especially after the pixel circuit was brought into the non-selection period (at about 300 μs), the source-drain voltage Vsd was changed to be approximately 6 V. The voltage Vsd is determined according to "applied-voltage/current property" of the organic EL element 109. The wording "applied-voltage/current property" refers to a property indicating a relation between the applied voltage and the current. In other words, the voltage Vsd is determined according to a

voltage Voled required for the supply of the current of 0.1 μA to the organic EL element 109. In the simulation, the voltage Voled had such a property as to satisfy:

$$Voled = Vs - 6V$$

Further, the applied-voltage/current property of the organic EL element 109 is similar to a property of a diode (the current exponentially increases in response to the applied voltage). For this reason, even when the current flowing through the organic EL element 109 varies by several ten percent, the source-drain voltage of the driving TFT 108 does not vary greatly.

[0025] If the driving TFT 108 were an ideal TFT, the change of the source-drain voltage would never cause the change of the current flowing from the source terminal of the driving TFT 108 to the drain terminal thereof, in cases where the gate-source potential Vsg is constant, and where the source-drain voltage Vsd is larger than the gate-source potential Vsg. However, in an actual TFT, even in cases where a gate-source potential Vsg is constant, a current flowing from a source terminal of the TFT to a drain terminal thereof increases as a source-drain voltage Vsd increases, as shown in Fig. 28. Note that Fig. 28 illustrates a result of a simulation carried out under the five conditions (see Table 2) of the threshold and the mobility of the driving TFT 108. Note also that current values Itft (1) through Itft (5) respectively correspond to the conditions Ioled (1) through Ioled (5) (see Table 2).

[0026] The result shown in Fig. 28 indicates that the variation of the source-drain voltage Vsd upon the current writing causes the variation of the current flowing from the source to the drain during the non-selection period. This changes the current flowing through the organic EL element 109.

[0027] So, an examination was carried out in order to find such current variation between the source terminal of the driving TFT 108 and the drain terminal thereof, with the use of a circuit in which the driving TFT 108 and the organic EL element 109 are provided in series as shown in Fig. 29. The examination is carried out by simulating a current flowing through the organic EL element 109, in the following manner under the aforesaid five conditions of the threshold voltage and the mobility of the driving TFT 108. That is, the simulation is carried out by (i) applying, to the gate terminal of the driving TFT 108, the gate-source potential Vgd, obtained upon the current writing (see Fig. 27), of the driving TFT 108; and (ii) changing a power source voltage Vs - Vcom. A result of the simulation is shown in Fig. 30.

[0028] Fig. 30 shows a case of the gate-source potential Vgd upon the supply of a current of 0.5 μA to the source wire Sj. In this case, the potential of the source wire Sj upon the current writing (See Fig. 27) was changed according to each of the conditions of the threshold voltage of the driving TFT 108 and the mobility thereof. This determined that the current of 0.5 μA was supplied to the organic EL element 109. Therefore, the current flowing through the organic EL element 109 was changed, on condition that the potential of the power wire Vs is constant (16V).

[0029] In this way, the threshold voltage variation of the driving TFT, and the mobility variation thereof cause the variation of the source-drain voltage Vsd upon the current writing, with the result that the current flowing through the organic EL element varies during the non-selection period. Such a phenomenon occurs also in the pixel circuit structure shown in Fig. 22. As such, the conventional circuit structure suffers from such a problem that the threshold voltage variation of the driving TFT and the mobility variation thereof cause the variation of the current flowing through the organic EL element during the non-selection period.

[0030] The present invention is made to solve the problem, and its object is to provide a display apparatus that is able to restrain the variation of the current flowing through the organic EL element during the non-selection period, the variation of the current being caused by the threshold voltage variation of the driving TFT, and the mobility variation thereof.

DISCLOSURE OF INVENTION

[0031] As described above, a first display apparatus of the present invention includes: (1) a first switching transistor, provided between (i) a current control terminal of the driving transistor and (ii) a current output terminal of the driving transistor; (2) a first capacitor, connected to the current control terminal of the driving transistor; and (3) a second capacitor, having a first terminal and a second terminal, the first terminal being connected to the current control terminal of the driving transistor, the second terminal being connected to (i) the current output terminal of the driving transistor via a second switching transistor, and (ii) a predetermined voltage line via a third transistor.

[0032] A pixel circuit structure and a source driver circuit structure each using the above structure allows the following effect. That is, during an output current setting period of the driving transistor of the circuit, the first switching transistor is ON, and a predetermined current is supplied to the driving transistor, with the result that the driving transistor is caused to have a current control terminal potential (potential Vx) accommodating to threshold voltage variation of the driving transistor and mobility variation thereof. The current control terminal potential is retained by the first capacitor.

[0033] Also on this occasion, the first terminal of the first capacitor is electrically connected to the first terminal of

the second capacitor. Therefore, by turning OFF the second switching transistor and turning ON the third switching transistor, the second terminal of the second capacitor is electrically connected to the predetermined voltage line (which has a constant potential Va allowing supply of the predetermined current). Moreover, this causes the second capacitor to retain a potential Va - Vx. These operations are carried out during a first period.

[0034] Next, the second switching transistor is turned ON, and the third switching transistor is turned OFF, with the result that the second terminal of the second capacitor is electrically connected to the current output terminal (a drain terminal or a source terminal of a TFT) of the driving transistor. In cases where the driving transistor has a default current output terminal potential Va, the driving transistor is caused to have the current control terminal potential (a gate potential of a TFT) Vx.

[0035] Thereafter, a desired current is supplied to the driving transistor, thereby changing the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor. This determines the potential of the current control terminal (a gate terminal of a TFT), while the potential of the current input terminal of the driving transistor and the potential of the current output terminal thereof are substantially equal to each other irrespective of the threshold voltage variation and the mobility variation of the driving transistor.

[0036] Further, in a pixel circuit including the driving transistor, a supply of the predetermined current to the current driving light emitting element causes potential drops of the current driving light emitting element in the same manner. With this, while the potential of the current input terminal of the driving transistor is substantially equal to the potential of the current output terminal thereof, the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor can be set such that the driving transistor outputs the predetermined current.

[0037] In the case of disconnecting the connection between the first capacitor and the second capacitor, the current control terminal potential of the driving transistor is retained by the first capacitor. On the other hand, in the case of maintaining the connection therebetween, the current control terminal potential of the driving transistor is retained by the first capacitor and the second capacitor. These operations are carried out during a second period.

[0038] Thereafter, during a non-selection period of the pixel circuit, the current input terminal-current output terminal potential of the driving transistor is changed; however, the changed potential is constant irrespective of the threshold voltage variation and the mobility variation of the driving transistor. This allows restraint of variation of a current flowing from the current input terminal of the driving transistor to the current output terminal thereof. As described above, a second display apparatus of the present invention includes: (1) a first switching transistor, provided between (i) a current control terminal of the driving transistor and (ii) a current input terminal of the driving transistor; (2) a first capacitor, connected to the current control terminal of the driving transistor; and (3) a second capacitor, having a first terminal and a second terminal, the first terminal being connected to the current control terminal of the driving transistor, the second terminal being connected to (i) the current input terminal of the driving transistor via a second switching transistor, and (ii) a predetermined voltage line via a third switching transistor.

[0039] A pixel circuit structure and a source driver circuit structure each using the above structure allows the following effect. That is, during an output current setting period of the driving transistor of the circuit, the first switching transistor is ON, and a predetermined current is supplied to the driving transistor, with the result that the driving transistor is caused to have a current control terminal potential (potential Vx) accommodating to threshold voltage variation of the driving transistor and mobility variation thereof. The current control terminal potential is retained by the first capacitor.

[0040] On this occasion, the first terminal of the first capacitor is electrically connected to the first terminal of the second capacitor. Therefore, by turning OFF the second switching transistor and turning ON the third switching transistor, the second terminal of the second capacitor is electrically connected to the predetermined voltage line (which has a constant potential Va allowing supply of the predetermined current). Moreover, this causes the second capacitor to retain a potential Va - Vx. These operations are carried out during a first period.

[0041] Next, the second switching transistor is turned ON, and the third switching transistor is turned OFF, with the result that the second terminal of the second capacitor is electrically connected to the current input terminal (a drain terminal or a source terminal of a TFT) of the drivingtransistor. In cases where the driving transistor has a default current input terminal potential Va, the driving transistor is caused to have the current control terminal potential (a gate potential of a TFT) Vx.

[0042] Thereafter, a desired current is supplied to the driving transistor, thereby changing the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor. This determines the potential of the current control terminal (a gate terminal of a TFT), while the potential of the current input terminal of the driving transistor and the potential of the current output terminal thereof are substantially equal to each other irrespective of the threshold voltage variation and the mobility variation of the driving transistor.

[0043] Further, in a pixel circuit including the driving transistor, a supply of the predetermined current to the current driving light emitting element causes potential drops of the current driving light emitting element in the same manner. With this, while the potential of the current input terminal of the driving transistor is substantially equal to the potential of the current output terminal thereof, the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor can be set such that the driving transistor outputs the predetermined current.

[0044] In the case of disconnecting the connection between the first capacitor and the second capacitor, the current control terminal potential of the driving transistor is retained by the first capacitor. On the other hand, in the case of maintaining the connection therebetween, the current control terminal potential of the driving transistor is retained by the first capacitor and the second capacitor. These operations are carried out during a second period.

[0045] Thereafter, during a non-selection period of the pixel circuit, the current input terminal-current output terminal potential of the driving transistor is changed; however, the changed potential is constant irrespective of the threshold voltage variation and the mobility variation of the driving transistor. This allows restraint of variation of a current flowing from the current input terminal of the driving transistor to the current output terminal thereof.

[0046] The aforementioned driving circuit structure is applicable to a pixel circuit structure for driving directly the current driving light emitting element, but may be applied to a source driver circuit for setting an output current of a driving transistor provided in a pixel circuit.

[0047] In cases where the driver circuit structure is used as the source driver circuit structure, the display apparatus may be arranged such that the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in each source driver circuit.

[0048] In the case where the driver circuit structure is used as the source driver circuit structure, it is particularly preferable to provide, in a pixel circuit, another transistor for controlling a current that is to be supplied to a current driving light emitting element provided in the pixel circuit. An output current of the transistor in the pixel circuit is controlled by the driving transistor, a component of the source driver circuit.

[0049] On the other hand, in the case where the driver circuit structure is used as the pixel circuit structure, the display apparatus may be arranged such that the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in each pixel circuit.

[0050] In the pixel circuit structure, the components, i.e., the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are all provided in the pixel circuit. With this, a conventional source driver circuit can be used as the source driver circuit for driving the pixel circuit.

[0051] This allows reduction of a stray capacitance between the first capacitor and the second capacitor, and the current writing period of the driving transistor can be accordingly shorter.

[0052] The display apparatus may be arranged such that: one or more of the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in a pixel circuit, and the others are provided in a portion outside the pixel circuit, which portion includes a source driver circuit.

[0053] The structure allows restraint of an increase in the number of capacitors and transistors required for each pixel circuit, as compared with a pixel circuit in which all the components are provided. This is because one or more of the first capacitor, the second capacitor, and the first switching transistor, and the second switching transistor, and the third switching transistor are provided in the source driver circuit or the portion outside the pixel circuit. This makes it possible to obtain desired luminance in each unit area without greater emission of each organic EL element of a display apparatus employing the bottom emission structure (such a structure that light is emitted toward a transparent substrate having TFT elements), as compared with the conventional technique. On this account, the organic EL element can have a longer luminance half-life. In contrast, see a case of a display apparatus employing a top emission structure (such a structure that light is emitted toward a side opposite to a transparent substrate having TFT elements). In this case, the number of elements provided in a pixel never increases, so that each pixel size can be as small as a pixel size in the conventional technique.

[0054] Further, the display apparatus may be arranged such that: the current driving light emitting element, the driving transistor, and the first capacitor are provided in the pixel circuit; and the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in the source driver circuit or the portion outside the pixel circuit, the display apparatus further includes a connecting wire for connecting the current control terminal of the driving transistor to the first terminal of the second capacitor.

[0055] The above structure makes it possible to provide a specific structure of a display apparatus in which one or more of the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in the source driver circuit or the portion outside the pixel circuit.Note that a stray capacitance tends to exist in the connecting wire for connecting the current control terminal of the driving transistor to the first terminal of the second capacitor. Therefore, the first capacitor is caused to have a capacitance equal to a total of the stray capacitance and the capacitance of the capacitor provided in the pixel.

[0056] For this reason, when the second capacitor has a small capacitance, the potential of the second terminal of the second capacitor is required to be increased. However, the great change in the potential of the second terminal of the second capacitor causes great variation of the source-drain potential of the driving transistor, so that this is not preferable. Therefore, the second capacitor is required to have a larger capacitance. This causes the current writing period of the driving transistor to be long.

[0057] In consideration of this, a circuit made up of the second capacitor and the first switching transistor is provided adjacent to the pixel so as to be shared with a plurality of pixel, even though this structure suffers from such a problem

that: acquirement of desired luminance in each unit area requires more emission of the organic EL element due to the decrease of the pixel area.

[0058] For example, one structure made up of the second capacitor and the first switching transistor is provided for every two pixels. This makes it possible to shorten a length of the connecting wire for connecting the current control terminal of the driving transistor to the first terminal of the second capacitor.

[0059] As the result, the stray capacitance of the connecting wire can be restrained, so that the source-drain potential of the driving transistor does not vary greatly even when the second capacitor has a small capacitance. With this, the current writing period of the driving transistor can be shortened.

[0060] Further, the display apparatus may be arranged such that: the current driving light emitting element, the driving transistor, the first switching transistor, the first capacitor, and the second capacitor are provided in the pixel circuit; the second switching transistor and the third switching transistor are provided in the source driver circuit or the portion outside the pixel circuit; and the display apparatus further includes a connecting wire for connecting the second terminal of the second capacitor to (i) the current output terminal of the driving transistor, or (ii) the current input terminal of the driving transistor.

[0061] The above structure makes it possible to provide a specific structure of a display apparatus in which one or more of the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in the source driver circuit or the portion outside the pixel circuit.Further, the display apparatus further includes:

an OFF potential line for supplying an OFF potential; wherein: the connecting wire is connected to the OFF potential line via a fourth switching transistor.

[0062] The above structure makes it possible to supply an OFF potential from the OFF potential line, via the fourth switching transistor and the connecting wire or the source wire, to a current control terminal of a driving transistor of a pixel to be brought into a dark state. The OFF potential surely turns OFF the driving transistor. This allows acquirement of sufficiently low luminance in the pixel in the dark state, thereby improving a contrast in the display apparatus.

[0063] Further, as described above, a first driving method of the present invention includes the steps of: (1) electrically connecting a current control terminal of the driving transistor to a first terminal of a first capacitor; (2) electrically connecting, during a current writing period of the driving transistor, the first terminal of the first capacitor to a first terminal of a second capacitor; (3) during a first period, (i) electrically connecting a second terminal of the second capacitor to a predetermined voltage line, and (ii) electrically connecting the current control terminal of the driving transistor to a current output terminal of the driving transistor, and (iii) causing the first capacitor and the second capacitor to retain a current control terminal potential that the driving transistor has on this occasion; (4) during a second period, (i) correcting the current control terminal potential by disconnecting the current control terminal of the driving transistor from the current output terminal of the driving transistor, and by changing electric connection of the second terminal of the second capacitor from the predetermined voltage line to the current output terminal of the driving transistor, and (ii) causing, during the second period, the first capacitor to retain the current control terminal potential that the driving transistor has on this occasion; and (5) controlling, during a current readout period of the driving transistor, an output current of the driving transistor with the use of the current control terminal potential, retained by the first capacitor, of the driving transistor.

[0064] The driving method allows the following effect. That is, during a first period within the output current setting period of the driving transistor of the pixel circuit and the source driver circuit, a predetermined current is supplied to the driving transistor, with the result that the driving transistor is caused to have a current control terminal potential (potential Vx) accommodating to threshold voltage variation of the driving transistor and mobility variation thereof. The current control terminal potential is retained by the first capacitor and the second capacitor. On this occasion, the first terminal of the first capacitor is electrically connected to the first terminal of the second capacitor. Therefore, the second terminal of the second capacitor is electrically connected to the predetermined voltage line (which has a constant potential Va allowing supply of the predetermined current). This causes the second capacitor to retain a potential Va - Vx.

[0065] Next, the second terminal of the second capacitor is electrically connected to the current output terminal (a drain terminal or a source terminal of a TFT) of the driving transistor. In cases where the driving transistor has a current output terminal potential Va on this occasion, the driving transistor is caused to have the current control terminal potential (a gate potential of a TFT) Vx.

[0066] Thereafter, a desired current is supplied to the driving transistor, thereby changing the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor. This determines the potential of the current control terminal (a gate terminal of a TFT), while the potential of the current input terminal of the driving transistor and the potential of the current output terminal thereof are substantially equal to each other irrespective of the threshold voltage variation and the mobility variation of the driving transistor. Further, a supply of the predetermined current to the current driving light emitting element causes potential drops of the current driving light emitting element in the same manner.

With this, while the potential of the current input terminal of the driving transistor is substantially equal to the potential of the current output terminal thereof, the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor can be set such that the driving transistor outputs the predetermined current.

[0067] In the case of disconnecting the connection between the first capacitor and the second capacitor, the current control terminal potential that the driving transistor has on this occasion is retained by the first capacitor. On the other hand, in the case of maintaining the connection therebetween, the current terminal potential of the driving transistor is retained by the first capacitor and the second capacitor.

[0068] Thereafter, during the current readout period of the driving transistor, the current input terminal-current output terminal potential of the driving transistor is changed; however, the changed potential is constant irrespective of the threshold voltage variation and the mobility variation of the driving transistor. This allows restraint of variation of a current flowing from the current input terminal of the driving transistor to the current output terminal thereof.

[0069] Further, a second driving method of the present invention includes the steps of: (1) electrically connecting a current control terminal of the driving transistor to a first terminal of a first capacitor; (2) electrically connecting, during a current writing period of the driving transistor, the first terminal of the first capacitor to a first terminal of a second capacitor; (3) during a first period, (i) electrically connecting a second terminal of the second capacitor to a predetermined voltage line, and (ii) electrically connecting the current control terminal of the driving transistor to a current input terminal of the driving transistor, and (iii) causing the first capacitor and the second capacitor to retain a current control terminal potential that the driving transistor has on this occasion; (4) during a second period, (i) correcting the current control terminal potential by disconnecting the current control terminal of the driving transistor from the current input terminal of the driving transistor, and by changing electric connection of the second terminal of the second capacitor from the predetermined voltage line to the current input terminal of the driving transistor, and (ii) causing the first capacitor to retain the current control terminal potential that the driving transistor has on this occasion; and (5) controlling, during a current readout period of the driving transistor, an output current of the driving transistor with the use of the current control terminal potential, retained by the first capacitor, of the driving transistor.

[0070] The driving method allows the following effect. That is, during a first period within the output current setting period of the driving transistor of the pixel circuit and the source driver circuit, a predetermined current is supplied to the driving transistor, with the result that the driving transistor is caused to have a current control terminal potential (potential Vx) accommodating to threshold voltage variation of the driving transistor and mobility variation thereof. The current control terminal potential is retained by the first capacitor and the second capacitor. On this occasion, the first terminal of the first capacitor is electrically connected to the first terminal of the second capacitor. Therefore, the second terminal of the second capacitor is electrically connected to the predetermined voltage line (which has a constant potential Va allowing supply of the predetermined current). This causes the second capacitor to retain a potential Va - Vx.

[0071] Next, the second terminal of the second capacitor is electrically connected to the current input terminal (a drain terminal or a source terminal of a TFT) of the driving transistor. In cases where the driving transistor has a current input terminal potential Va on this occasion, the driving transistor is caused to have the current control terminal potential (a gate potential of a TFT) Vx.

[0072] Thereafter, a desired current is supplied to the driving transistor, thereby changing the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor. This determines the potential of the current control terminal (a gate terminal of a TFT), while the potential of the current input terminal of the driving transistor and the potential of the current output terminal thereof are equal to each other irrespective of the threshold voltage variation and the mobility variation of the driving transistor.

[0073] Further, in cases where the driving transistor is provided in the pixel circuit, the supply of the predetermined current to the current driving light emitting element causes potential drops of the current driving light emitting element in the same manner. With this, while the potential of the current input terminal of the driving transistor is substantially equal to the potential of the current output terminal thereof, the potential of the current control terminal (a gate terminal of a TFT) of the driving transistor can be set such that the driving transistor outputs the predetermined current.

[0074] In the case of disconnecting the connection between the first capacitor and the second capacitor, the current control terminal potential of the driving transistor is retained by the first capacitor. On the other hand, in the case of maintaining the connection therebetween, the current terminal potential of the driving transistor is retained by the first capacitor and the second capacitor.

[0075] Thereafter, during the non-selection period of the pixel circuit, the current input terminal-current output terminal potential of the driving transistor is changed; however, the changed potential is constant irrespective of the threshold voltage variation and the mobility variation of the driving transistor. This allows restraint of variation of a current flowing from the current input terminal of the driving transistor to the current output terminal thereof.

[0076] As such, the first and second driving methods of the present invention are beneficial in reducing the difference between (i) the current flowing during the current writing period of the driving transistor constituting the pixel circuit, and (ii) the current flowing during the current readout period of thereof. Moreover, the methods are beneficial in reducing the difference between (i) the current flowing during the current writing period of the driving transistor constituting the

source driver, and (ii) the current flowing during the current readout period of thereof.

[0077] In the latter case, a display by the current driving light emitting element can be uniformly carried out by supplying, to the current driving light emitting element, an output current of each transistor (each transistor, other than the driving transistor, for controlling current supply to the current driving light emitting element of each pixel circuit), which output current is as large as the current flowing through the driving transistor. The transistors and the light emitting element are provided in a matrix manner.

[0078] Further, in the first and second driving methods of the present invention, when the second terminal of the second capacitor has the aforesaid potential Va during the second period, the potential of the current control terminal (gate terminal of the TFT) of the driving transistor is caused to have the aforesaid potential Vx. For this reason, it is preferable that: the second terminal of the second capacitor stay electrically connected to the predetermined voltage line even after the start of the second period, and then the electric connection be disconnected. This shortens time taken for the second terminal of the second capacitor to have the final potential. Accordingly, a larger number of gate wires can be driven, with result that a larger number of pixels can be used for a display.

[0079] Specifically, the second terminal of the second capacitor will have a final potential as large as the potential Va of the predetermined voltage line. Therefore, the time taken for the acquirement of such a final potential can be shortened by causing the second terminal of the second capacitor to have a potential Va in advance.

[0080] This is a preferable driving example of the driving methods of the present invention. See a case where the driving example is applied to the first driving method. That is, the electric connection is disconnected between the current control terminal of the driving transistor and the current output terminal thereof, and then the second terminal of the second capacitor is electrically connected to the current output terminal of the driving transistor while maintaining the electric connection with the predetermined voltage line. The maintained electric connection with the predetermined voltage line causes the second terminal of the second capacitor to have a potential as large as the potential Va of the predetermined voltage line. After this, the second terminal of the second capacitor is electrically disconnected from the predetermined voltage line.

[0081] On the other hand, see a case where the driving example is applied to the second driving method. That is, the electric connection is disconnected between the current control terminal of the driving transistor and the current input terminal thereof, and then the second terminal of the second capacitor is electrically connected to the current input terminal of the driving transistor while maintaining the electric connection with the predetermined voltage line. The maintained electric connection with the predetermined voltage line causes the second terminal of the second capacitor to have a potential as large as the potential Va of the predetermined voltage line. After this, the second terminal of the second capacitor is electrically disconnected from the predetermined voltage line.

[0082] Additional objects, features, and strengths of the present invention will be made clear by the description below. Further, the advantages of the present invention will be evident from the following explanation in reference to the drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0083]

Fig. 1 illustrates one embodiment of the present invention, and is a circuit diagram illustrating a structure of a pixel circuit of a display apparatus according to Embodiment 1.

Fig. 2 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit.

Fig. 3 is a graph illustrating a result of a simulation of respective changes of (i) a source-gate potential and (ii) a source-drain potential of a driving TFT of the pixel circuit.

Fig. 4 is a graph illustrating a result of simulating a current flowing through an organic EL element in the pixel circuit.

Fig. 5 is a graph illustrating a result of simulating a current flowing through an organic EL element in the pixel circuit.

Fig. 6 is a circuit diagram illustrating a structure of the display apparatus according to Embodiment 1, which structure is different from the pixel circuit shown in Fig. 1.

Fig. 7 is a circuit diagram illustrating a structure of a display apparatus according to Embodiment 2.

Fig. 8 is a circuit diagram illustrating respective structures of a pixel circuit and a source driver circuit in the display apparatus according to Embodiment 2.

Fig. 9 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit and the source driver circuit.

Fig. 10 is a graph illustrating a result of simulating a current flowing through an organic EL element in the pixel circuit.

Fig. 11 is a circuit diagram illustrating respective structures of a pixel circuit and a source driver circuit in a display apparatus according to Embodiment 3.

Fig. 12 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit and the source driver circuit.

Fig. 13 is a graph illustrating a result of simulating a current flowing through an organic EL element in the pixel circuit.
Fig. 14 is a circuit diagram illustrating a structure of a source driver circuit in a display apparatus according to Embodiment 4.
Fig. 15 is a wave form chart illustrating respective operation timings of control wires of the source driver circuit.
Fig. 16 is a graph illustrating a result of simulating respective changes in (i) a source-gate potential and (ii) a source-drain potential of a driving TFT in the source driver circuit.
Fig. 17 is a graph illustrating a result of simulating a current flowing from a source terminal of the driving TFT to a drain terminal thereof, in the source driver circuit.
Fig. 18 is a wave form chart illustrating respective operation timings of control wires in a display apparatus in which the source driver circuit shown in Fig. 14 and the pixel circuit shown in Fig. 1 are combined.
Fig. 19 is a graph illustrating a result of simulating respective changes in a source-gate potential and a source-drain potential of a driving TFT of the source driver circuit of the circuit structure obtained by combining the source driver circuit shown in Fig. 14 with the pixel circuit shown in Fig. 1.
Fig. 20 is a graph illustrating a result of simulating a current flowing through an organic EL element of the pixel circuit of the circuit structure obtained by combining the source driver circuit shown in Fig. 14 with the pixel circuit shown in Fig. 1.
Fig. 21 is a circuit diagram illustrating a structure of the display apparatus according to Embodiment 4, which structure is different from the source driver circuit shown in Fig. 14.
Fig. 22 is a circuit diagram illustrating a structure example of a pixel circuit of a conventional display apparatus.
Fig. 23 is another structure example of the pixel circuit of the conventional display apparatus.
Fig. 24 is a wave form chart illustrating respective operation timings of control wires of the conventional pixel circuit.
Fig. 25 is a graph illustrating a result of simulating a current flowing through an organic EL element in the conventional pixel circuit.
Fig. 26 is a graph illustrating a result of simulating a current flowing through an organic EL element in the conventional pixel circuit.
Fig. 27 is a graph illustrating a result of simulating respective changes in a source-gate potential and a source-drain potential of a driving TFT in the conventional pixel circuit.
Fig. 28 is a graph illustrating a relation between (i) a source-drain potential Vsd of the driving TFT, and (ii) a current flowing from a source of the driving TFT to a drain thereof.
Fig. 29 is a circuit diagram illustrating a circuit structure in which a driving TFT is provided in series with an organic EL element.
Fig. 30 is a graph illustrating a result of a simulation for examining variation, during the non-selection period, in a current flowing from (i) a source of the driving TFT of the circuit shown in Fig. 29, to (ii) a drain thereof.
Fig. 31 is a circuit diagram illustrating respective structures of a pixel circuit and a source driver circuit in a display apparatus according to Embodiment 5.
Fig. 32 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit and the source driver circuit.
Fig. 33 is a graph illustrating a result of simulating a current flowing from the source terminal of the driving TFT to the drain terminal of the driving TFT, in the pixel circuit and the source driver circuit.
Fig. 34 is a circuit diagram illustrating (i) a structure of a pixel circuit, and (ii) a structure of a source driver circuit in a display apparatus according to Embodiment 6.
Fig. 35 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit and the source driver circuit.
Fig. 36 is a graph illustrating a result of simulating a current flowing from a source of a driving TFT to a drain thereof in the pixel circuit and the source driver circuit.
Fig. 37 is a circuit diagram illustrating respective structures of another pixel circuit and another source driver circuit in the display apparatus according to Embodiment 6.
Fig. 38 is a circuit diagram illustrating respective structures of a pixel circuit and a source driver circuit in a display apparatus according to Embodiment 7.
Fig. 39 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit and the source driver circuit.
Fig. 40 is a graph illustrating a result of simulating respective changes in the source-gate potential and the source-drain potential of the driving TFT in the pixel circuit shown in Fig. 8 and the source driver circuit shown therein.
Fig. 41 illustrates a circuit diagram illustrating respective structures of a pixel circuit, a source driver circuit, and another circuit in a display apparatus according to Embodiment 8.
Fig. 42 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit and the source driver circuit.
Fig. 43 is a graph illustrating a result of simulating respective changes in (i) a source-drain potential of the driving

TFT and (ii) a current from the source of the driving TFT to the drain thereof, in the pixel circuit (see Fig. 41) and the source driver circuit (see Fig. 41).

Fig. 44 is a circuit diagram illustrating a pixel circuit, a source driver circuit, and another circuit in a display apparatus according to Embodiment 9.

Fig. 45 is a wave form chart illustrating respective operation timings of control wires of the pixel circuit, the source driver circuit, and the aforesaid another circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

[0084] Embodiments of the present invention will be explained with reference to Fig. 1 through Fig. 21, and Fig. 31 through Fig. 45. Note that the present invention is not limited to these.

[0085] Note also that each switching element used in the present invention may be a low temperature polysilicon TFT or a CG (Continuous Grain) silicon TFT; however, Embodiments below uses the CG silicon TFT.

[0086] Here, a structure of such a CG silicon TFT is described in, for example, "4.0-in. TFT-OLED Displays and a Novel Digital Driving Method" (SID' 00 Digest, pp.924-927, Semiconductor Energy Laboratory Co., Ltd). Moreover, a manufacturing process of such a CG silicon TFT is described in, for example, "Continuous Grain Silicon Technology and Its Applications for Active Matrix Display" (AM-LCD 2000, pp.25-28, Semiconductor Energy Laboratory Co., Ltd). That is, the structure and the manufacturing process of the CG silicon TFT are publicly well-know, so that detailed explanation thereof is omitted here.

[0087] Further, a structure of each organic EL element, used in Embodiments and serving as an electric optical element, is described in, for example, "Polymer Light-Emitting Diodes for use in Flat panel Display" (AM-LCD '01, pp. 211-214, Semiconductor Energy Laboratory Co., Ltd). Therefore, the structure is publicly well-known, so that detailed explanation thereof is omitted here.

[Embodiment 1]

[0088] Embodiment 1 will explains a case where a first characteristic structure according to the present invention is applied to a pixel circuit.

[0089] As shown in Fig. 1, in each of pixel circuits Aij of a display apparatus according to Embodiment 1, a driving TFT 1 is provided in series with a organic EL element (current driving light-emitting element) 6 between a power source wire Vs and a common wire Vcom. The driving TFT 1 serves as a driving TFT, and the organic EL element 6 serves as an electric optical element. The driving TFT 1 controls a current that is to be supplied to the organic EL element 6.

[0090] The driving TFT 1 has a gate terminal (current control terminal) connected to a source wire Sj via a switching TFT 3, serving as a first switching transistor. Moreover, the gate terminal (current control terminal) of the driving TFT 1 is connected to one terminal of a first capacitor 2 , and to one terminal of a second capacitor 7. The other terminal of the first capacitor 2 is connected to (i) a source terminal (current input terminal) of the driving TFT 1 and (ii) the power source wire Vs. The other terminal of the second capacitor 7 is connected to a predetermined voltage line Va via a switching TFT 8, which serves as a third switching transistor. Moreover, the other terminal of the second capacitor 7 is connected to the source wire Sj via a switching TFT 9, which serves as a second switching transistor. Note that, the following explanation assumes that a first terminal of the first capacitor 2 refers to its terminal connected to the gate terminal of the driving TFT 1, and a second terminal of the first capacitor 2 refers to the other terminal of the first capacitor 2; and that a first terminal of the second capacitor 7 refers to its terminal connected to the gate terminal of the driving TFT 1, and a second terminal of the second capacitor 7 refers to the other terminal of the second capacitor 7.

[0091] Respective gate terminals of the switching TFT 3 and the switching TFT 8 are connected to a control wire Ci, and a gate terminal of the switching TFT 9 is connected to a control wire Gi.

[0092] A switching TFT 4 is provided between (i) a drain terminal (current output terminal) of the driving TFT 1, and (ii) an anode of the organic EL element 6. The switching TFT 4 has a gate terminal connected to a control wire Ri. A node of the driving TFT 1 and the switching TFT 4 is connected to the source wire Sj via a switching TFT 5. The switching TFT 5 has a gate terminal connected to a control wire Wi.

[0093] Any of the control wires Ci, Gi, and Wi may serve as a second wire (gate wire), and any of the switching TFTs 3, 9, and 5 may serve as a selection TFT. Note that, in the present embodiment, the control wire Gi is also referred to as "gate wire Gi".

[0094] In the circuit structure, the gate terminal of the driving TFT 1 is connected to the drain terminal thereof via The switching TFT 3, the source wire Sj, and the switching TFT 5. Further, the second terminal of the second capacitor 7 is connected to the drain terminal of the driving TFT 1 via the switching TFT 9, the source wire Sj, and the switching TFT 5.

[0095] As such, the means of the present invention encompasses not only a case where the switching TFT 3 serving as the first switching TFT directly connects the current control terminal of the driving TFT to the current output terminal

thereof, but also a case where the switching TFT 3 indirectly connects the current control terminal of the driving TFT to the current output terminal thereof via the source wire Sj and the switching TFT5.

[0096] Likewise, the means of the present invention encompasses not only a case where the switching TFT 9 serving as the second switching TFT directly connects the second terminal of the second capacitor to the current output terminal of the driving TFT, but also a case where the switching TFT 9 indirectly connects the second terminal of the second capacitor to the current output terminal of the driving TFT via the source wire Sj and the switching TFT 5.

[0097] The following explains an operation of the pixel circuit Aij of the display apparatus with reference to Fig. 2. Fig. 2 illustrates respective operation timings of the control wires Ri, Wi, Ci, and Gi, and the source wire Sj.

[0098] In a driving method according to Embodiment 1 (first driving method of the present invention), during a selection period (i.e., a current writing period of the driving transistor) corresponding to a period of time from 0 to 5t1, a potential of the control wire Ri is set at High (GH) such that the switching TFT 4 is OFF, and a potential of the control wire Wi is set at Low (GL) such that the switching TFT 5 is ON.

[0099] During a first period (time t1 to time 2t1), a potential of the control wire Ci is set at High such that the switching TFTs 3 and 8 are ON. This connects the gate terminal (current control terminal) of the driving TFT 1 to the drain terminal (current output terminal) thereof via the switching TFTs 3 and 5. Moreover, this connects the second terminal of the second capacitor 7 to the predetermined voltage line Va via the switching TFT 8. Accordingly, a current is constantly supplied from the power source wire Vs to a source driver circuit (not shown) via the driving TFT 1, the switching TFT 5, the source wire Sj.

[0100] Note that the first period may start from the time 0 as a broken line in Fig. 2 indicates.

[0101] Thereafter (at the time 2t1), the potential of the control wire Ci is set at Low such that the switching TFTs 3 and 8 become OFF. This is done to prevent the switching TFTs 3 and 9 from becoming ON simultaneously. Such an OFF operation actually requires time shorter than t1. At the moment of the turning OFF, the first capacitor 2 and the second capacitor 7 retains the potential, determined during the first period, of the source wire Sj.

[0102] Next, during a second period (time 3t1 to time 4t1), the potential of the control wire Gi is set at High such that the switching TFT 9 is ON. This connects the second terminal of the second capacitor 7 to the drain terminal of the driving TFT 1 via the switching TFTs 9 and 5. Accordingly, a predetermined current is supplied from the power source wire Vs to the source driver circuit (not shown) via the driving TFT 1, the switching TFT 5, and the source wire Sj.

[0103] The source-gate potential of the driving TFT 1 is determined in this way during the second period. Then (at time 4t1), the potential of the control wire Gi is set at Low such that the switching TFT 9 becomes OFF. This causes the first capacitor 2 and the second capacitor 7 to retain the source-gate potential of the driving TFT 1. Note that a period of time from 4t1 to 5t1 after this, i.e., a period of time until the control wire Ri becomes Low and the control wire Wi becomes High is secured such that the selection period is finished after the switching TFT 9 surely becomes OFF. For this reason, this period may be shorter than t1.

[0104] Now, the selection period of the pixel circuit Aij is over, and then a following pixel circuit A(i+1)j is selected. Here, Fig. 3 illustrates a result of simulating respective changes in (i) the source-gate potential Vsg of the driving TFT 1 of the pixel circuit Aij, and (ii) the source-drain potential Vsd thereof. Note that source-drain potentials Vsd (1) through Vsd (5), and source-gate potentials Vsg (1) through Vsg (5) respectively correspond to the following conditions (see Table 2 below) of the threshold voltage of the driving TFT 1, and of the mobility property thereof.

Table 2

	Ioled(1)	Ioled(2)	Ioled(3)	Ioled(4)	Ioled(5)
	Vsg(1)	Vsg(2)	Vsg(3)	Vsg(4)	Vsg(5)
	Vsd(1)	Vsd(2)	Vsd(3)	Vsd(4)	Vsd(5)
Threshold voltage	Average value	Lower limit value	Upper limit value	Upper limit value	Lower limit value
Mobility	Average value	Lower limit value	Upper limit value	Lower limit value	Upper limit value

[0105] In Fig. 3, a period of time from 460 μs to 470 μs corresponds to the aforesaid first period. As shown in Fig. 3, the source-drain potentials Vsd (1) through Vsd (5) coincided with the source-gate potential Vsg (1) through Vsg (5), respectively.

[0106] Further, a period of time from 480 μs to 490 μs in Fig. 3 corresponds to the aforesaid second period. As shown in Fig. 3, the source-drain potentials Vsd had almost the same value during the period, irrespective of the differences in the conditions of the threshold voltage and the mobility of the driving TFT 1.

[0107] The reason of this is as follows. That is, during the foregoing first period, the second terminal of the second capacitor 7 was connected to the predetermined voltage line Va having a constant potential Va, and then the second

terminal was connected to the drain terminal of the driving TFT 1. This caused the first capacitor and the second capacitor to store a charge allowing the driving TFT 1 to have, when the source-drain potential of the TFT 1 was Vs - Va, a source-gate potential equal to the source-gate potential (see Fig. 1 2) that the driving TFT 1 had during the first period.

[0108] This made it possible to cause the driving TFT 1 to have, when the source-drain potential of the driving TFT 1 was the potential Vs - Va, a source-gate potential equal to the source-gate potential that the driving TFT 1 had during the first period, irrespective of the threshold voltage variation and the mobility variation of the driving TFT 1. With the driving TFT 1 thus set, a predetermined current was supplied from the power wire Vs to the source driver circuit (not shown) via the driving TFT 1, the switching TFT 5, and the source wire Sj. A source-gate potential Vsg resulting from the current supply allowed a current to constantly flow through the driving TFT 1, irrespective of the threshold voltage variation and the mobility variation of the driving TFT 1, as long as the source-drain potential of the driving TFT 1 was constant.

[0109] Thereafter, during a non-selection period (i.e., current readout of the driving transistor; time at and after approximately 500 μs), the source-drain potentials of the driving TFT 1 were changed as shown in Fig. 3. Although the current values were different to some extent, the potential drops occurred in substantially the same manner. This is because the organic EL element 6, which is a load of the driving TFT 1, has a diode-like property. With this, the potential of the drain terminal of the driving TFT 1 was substantially constant irrespective of the threshold voltage variation and the mobility variation of the driving TFT 1. Accordingly, the source-drain voltage of the driving TFT 1 became constant. This allowed a restraint of the variation of the current flowing through the organic EL element, irrespective of the threshold voltage and the mobility of the driving TFT 1.

[0110] Note that, it is preferable that the constant potential Va is set at a value (an anode potential, which corresponds to the current, of the organic EL) predictable from an applied-voltage / current property of the organic EL element 6. With this, the source-drain voltage of the driving TFT 1 upon the current writing therein becomes substantially equal to the source-drain voltage upon the current readout therefrom.

[0111] A simulation was carried out to find the current flowing through the organic EL element 6. A result of the simulation is shown in Fig. 4 and Fig. 5.

[0112] In the simulation shown in Fig. 4, the selection period came every 0.32 ms. During an initial period of time from 0.35 ms to 0.67 ms, a current of 0.1 μA was set to flow into the source wire Sj. Thereafter, the current was increased by 0.1 μA every 0.32 ms until the current had a value of 0.9 μA. Then, the current was set at 0. After that, the current was increased again by 0.1 μA.

[0113] The current variation found by the simulation is illustrated in Fig. 5 whose horizontal axis plots the respective currents (the respective ten currents of 0 μA to 0.9 μA) that flowed to the source wire Sj, and whose vertical axis plots respective currents that flowed to the organic EL element 6 during each non-selection period, which came after each current supply to the source wire Sj. In Fig. 5, during the non-selection period coming after the supply of the current of 0.9 μA to the source wire Sj, the current that flowed through the organic EL element varies in a range of about 0.97 μA to about 1.01 μA (increased by 8% to 13%).

[0114] The variation is sufficiently reduced as compared with the result (the current was increased by 5 % to 24 %; in other words, was varied in a range of 19%) of the simulation using the conventional technique shown in Fig. 26. This proves that the means of the present invention is efficient (the current was increased by 8 % to 13%; in other words, was varied in a range of 5%).

[0115] Note that an effective way of further restraining the variation in the pixel circuit structure according to the present invention is to optimize (i) respective absolute capacitances of the first capacitor 2 and the second capacitor 7, (ii) a relative ratio of the absolute capacitances, (iii) the constant potential Va, (iv) a gate width of the driving TFT 1, and the like.

[0116] For example, the variation of the source-drain potential required for the change of the source-gate potential Vsg during the second period can be restrained better as a ratio (C2/C1) of capacitance C2 of the second capacitor 7 to capacitance C1 of the first capacitor 2 is larger. This allows restraint of (i) the variation of the source-drain potential depending on the threshold voltage of the driving TFT 1 and the mobility thereof, and (ii) the variation of the current flowing to the organic EL element 6 during the non-selection period. This is preferable.

[0117] When the respective absolute capacitances of the capacitors are too small, the respective potentials retained by the capacitors are affected by the changes of the potentials of the gate terminals of the switching TFTs 3, 8, and 9, each of which is connected to the capacitors. This causes the variation of the current flowing to the organic EL element 6 during the non-selection period. For this reason, this is not preferable.

[0118] Further, it is preferable that the constant potential Va supplied during the first period be set such that the potential value difference Vs - Va between the predetermined voltage line Va and the power source wire Vs is slightly larger than or substantially equal to the source-drain potential Vsd that is to be expected during the non-selection period. That is, too large a potential difference Vs - Va causes too large a difference between (i) the source-drain potential Vsd during the current writing period, and (ii) the source-drain potential Vsd during the non-selection period.

Accordingly, the current actually flowing to the organic EL element 6 becomes too small as compared with the current supplied from the source wire Sj. This is not preferable.

[0119] Further, a driving TFT 1 having a too large gate width W causes the driving TFT 1 to have a too small source-gate potential, with the result that the change in the gate potential causes the variation of the current flowing into the organic EL element 6 during the non-selection period. This is not preferable. On the other hand, a driving TFT having a too small gate width W requires a too large source-drain potential for the acquirement of the required current. This is not preferable, either.

[0120] The variation of the current flowing to the organic EL is the least (approximately 1%) in the organic EL element used in Embodiment 1 when C1 is 1000 fF, C2 is 500fF, Vs is 16V, Va is 10 V, and W is 12 μm in the pixel circuit Aij shown in Fig. 1. This is suitable.

[0121] Note that the absolute capacitance C1 of the first capacitor 2, the absolute capacitance C2 of the second capacitor 7, the relative ratio of the absolute capacitances, the constant potential Va, and the gate width W of the driving TFT 1 are dependent on (i) the property of the organic EL element to be driven, (ii) a required luminescence, and (iii) the property of the driving TFT 1 to be used. For this reason, such a simulation is required to be carried out several times again upon actually designing a panel.

[0122] Note also that, in the pixel circuit structure shown in Fig. 1, the switching TFT 3 is connected to the source wire Sj so as to connect the gate terminal of the driving TFT 1 to the drain terminal thereof; however, the switching TFT 3 may be directly connected to the drain terminal of the driving TFT 1. This is also true of the switching TFT 9 for connecting the second terminal of the second capacitor 7 to the drain terminal of the driving TFT 1. That is, the switching TFTs 3 and 9 may be directly connected to the drain terminal of the driving TFT 1.

[0123] Further, the organic EL element may be so provided as to be associated with the source terminal of the driving TFT. In such a structure, a driving TFT 1' is an n-type TFT, and has a source terminal connected to a cathode of an organic EL element 6', as shown in Fig. 6. Moreover, in the structure shown in Fig. 6, switching TFTs 4' and 5' are n-type TFTs unlike those in the pixel circuit structure shown in Fig. 1.

[0124] Further, the switching TFTs 3 and 9 are connected to a drain terminal of the driving TFT 1'.

[0125] The other wires and operations in the pixel circuit structure shown in Fig. 6 are the same as those in the structure shown in Fig. 1. Therefore, structures equivalent to those shown in Fig. 1 are given the same reference symbols, and explanation thereof is omitted here.

[Embodiment 2]

[0126] Embodiment 2 will explain a first example in which the first characteristic structure according to the present invention is applied to a pixel circuit and a source driver circuit.

[0127] A display apparatus according to Embodiment 2 is so arranged that components of the characteristic structure of the present invention are provided separately in the pixel circuit and the source driver circuit. See Fig. 7. In the structure of the display apparatus, pixel circuits Aij are provided in regions in which source wires Sj (j is an integer falling within a range from 1 to m) intersect with gate wires Gi (i is an integer falling within a range from 1 to n), respectively. The source wires Sj are connected to a source driver circuit 50, and the gate wires Gi are connected to a gate driver circuit 51. Each of the source wires Sj serves as the first wire, and each of the gate wires Gi serves as the second wire.

[0128] Fig. 8 illustrates respective structures of each pixel circuit Aij and a source driver output terminal circuit Dj, serving as an output stage of the source driver circuit 50. Each of the pixel circuit Aij and the source driver output terminal circuit Dj includes the characteristic structure of the present invention.

[0129] As shown in Fig. 8, in the display apparatus according to Embodiment 2, the pixel circuit Aij is provided in the region in which the source wire Sj and the gate wire Gi intersect with each other. Provided in the pixel circuit Aij are: (i) a driving TFT 11, which serves as an active element; (ii) an organic EL element 16, which serves as an electric optical element; and (iii) , a first capacitor 12. The driving TFT 11 and the organic EL element 16 are provided in series between a power source wire Vs and a common wire Vcom.

[0130] The driving TFT 11 has a gate terminal (current control terminal) connected to one terminal (hereinafter, referred to as "first terminal") of the first capacitor 12. The other terminal (hereinafter, referred to as "second terminal") of the first capacitor 12 is connected to a source terminal (current input terminal) of the driving TFT 11, and to the power source wire Vs.

[0131] Further, in the pixel circuit structure, a signal line Tj, serving as a third wire, is provided in parallel with the source wire Sj. The signal line Tj is connected to the gate terminal of the driving TFT 11 via a switching TFT 15.

[0132] Further, a switching TFT 13 is provided between a drain terminal (current output terminal) of the driving TFT 11 and an anode of the organic EL element 16. A node of the driving TFT 11 and the switching TFT 13 is connected to the source wire Sj via a switching TFT 14.

[0133] The components of the pixel circuit Aij, i.e., the switching TFTs 15, 14, and 13 have gate terminals connected

to control wires Gi, Wi, and Ri, respectively.

[0134] In the source driver circuit 50, one output terminal circuit Dj is provided for a plurality of pixel circuits A1j through Anj. As shown in Fig. 8, in the output terminal circuit Dj, one terminal (hereinafter, referred to as "first terminal") of a second capacitor 25 is connected to the signal wire Tj. A switching TFT 22, which serves as the first switching transistor, is provided between the signal line Tj and the source wire Sj. Further, a switching transistor TFT 23, serving as the third switching transistor, is provided between (i) the other terminal (hereinafter, referred to as "second terminal") of the second capacitor 25, and (ii) a predetermined voltage line Va. Moreover, the switching TFT 24, serving as the second switching transistor, is provided between the second terminal of the second capacitor 25 and the source wire Sj. Further, a switching TFT 21, serving as a fourth transistor, is provided between the signal wire Tj and an OFF potential wire Voff.

[0135] In the output terminal circuit Dj, the switching TFT 21 has a gate terminal connected to a control wire Ej, and each of the switching TFTs 22 and 23 has a gate terminal connected to a control wire Cj, and the switching TFT 24 has a gate terminal connected to a control wire Bj.

[0136] The following explains respective operations of the pixel circuit Aij and the output terminal circuit Dj in the display apparatus with reference to Fig. 9. Fig. 9 illustrates respective operation timings of the control wires Ri, Wi, Gi, Cj, Ej, and Bj, and the source wire Sj.

[0137] In a driving method (first driving method of the present invention) according to Embodiment 2, the selection period of the pixel circuit Aij corresponds to a period of time from 0 to 5t1. During the period, a potential of the control wire Ri is set at High (GH) such that the switching TFT 13 is OFF, and a potential of the control wire Wi is set at Low (GL) such that the switching TFT 14 is ON.

[0138] In the pixel circuit Aij, during the first period (time t1 to 2t1), a potential of the control wire Gi is set at High such that the switching TFT 15 is ON. This electrically connects the gate terminal of the driving TFT 11 to the signal line Tj. With this, the gate terminal of the driving TFT 11 is connected to the first capacitor 12 and the second capacitor 25.

[0139] Meanwhile, during the period, in the output terminal circuit Dj, a potential of the control wire Cj is set at High such that the switching TFTs 22 and 23 are ON. This electrically connects the gate terminal of the driving TFT 11 to the drain terminal thereof via the switching TFTs 15, 22, and 14. This also connects the second terminal of the second capacitor 25 to the predetermined voltage line Va via the switching TFT 23. With this, a current flows constantly from the power source wire Vs to a current output terminal Ij via the driving TFT 11, the switching TFT 14, and the source wire Sj.

[0140] Thereafter, the potential of the control wire Cj is set at Low such that the switching TFTs 22 and 23 become OFF. This causes the first capacitor 12 and the second capacitor 25 to retain the potential that the source wire Sj has on this occasion.

[0141] The first capacitor 12 and the second capacitor 25 thus retaining the potential on this occasion causes the driving TFT 11 to have a gate potential allowing a current to flow constantly as above (as the aforesaid current supply, during the first period, from the source terminal of the driving TFT 11 to the drain terminal thereof) while the second terminal of the second capacitor 25 has a potential Va, irrespective of the threshold voltage of the driving TFT 11 and the mobility thereof.

[0142] Next, during the second period (time 3t1 to time 4t1), the potential of the control wire Bj is set at High such that the switching TFT 24 is ON. This connects the second terminal of the second capacitor 25 to the drain terminal of the driving TFT 11 via the switching TFTs 24 and 14. With this, a desired current flows from the power source wire Vs to the current output terminal Ij via the driving TFT 11, the switching TFT 14, and the source wire Sj.

[0143] With this, a current is set to flow through the driving TFT 11 as above even during the second period, irrespective of the threshold voltage and the mobility of the driving TFT 11, as long as the source-drain potential of the driving TFT 11 is the potential Vs - Va. In other words, the supply of the desired current to the driving TFT 11 can determine the gate-source potential of the driving TFT 11 on condition that the source-drain potential of the driving TFT 11 is substantially constant.

[0144] At the time 4t1 after this, the potential of the control wire Gi is set at Low such that the switching TFT 15 becomes OFF. This causes the first capacitor 12 to retain the source-gate potential that the driving TFT- 11 has during the second period.

[0145] At the time 5t1 after this, the following operations are carried out. That is, the potential of the control wire Bj is set at Low such that the switching TFT 24 becomes OFF. This disconnects the electric connection between the second capacitor 25 and the source wire Sj. The potential of the control wire Wi is set at High such that the switching TFT 14 becomes OFF. This disconnects the electric connection between the drain terminal of the driving TFT 11 and the source wire Sj. Moreover, the potential of the control wire Ri is set at Low such that the switching TFT 13 becomes ON. With this, a current is supplied from the driving TFT 11 to the organic EL element 16.

[0146] Now, the selection period of the pixel circuit Aij is over, and then a following pixel circuit A(i+1)j is selected.

[0147] A simulation was carried out to find values of a current flowing through the organic EL element 16, with the use of the pixel circuit structure (see Fig. 8) and the output terminal circuit structure (see Fig. 8) of the source driver

circuit. A result of the simulation is shown in Fig. 10.

[0148] In the simulation shown in Fig. 10, the selection period came every 0.55 ms. During an initial period of time 0.06 ms to 0.61 ms, a current of 0.1 μA was set to flow into the source wire Sj. Thereafter, the current was increased by 0.1 μA every 0.55 ms until the current had a value of 0.9 μA. Then, the current was set at 0. After that, the current was increased again by 0.1 μA.

[0149] Here; a comparison is made between (i) Embodiment 2 (see Fig. 10) employing such a structure that some components of the characteristic structure of the present invention are provided in the source driver circuit, and (ii) Embodiment 1 (see Fig. 4) employing such a structure that all the components are provided in the pixel circuit. The comparison clarifies that: as is the case with the structure of Embodiment 1, the structure of Embodiment 2 also makes it possible to reduce the adverse effect of the threshold voltage variation and the mobility variation of the driving TFT 11, and therefore makes it possible to restrain the variation of the current flowing to the organic EL element 16 during the non-selection period.

[0150] Further, in the structure according to Embodiment 2, the switching TFTs and the capacitor are not provided in the pixel circuit, but are provided in the source driver circuit as shown in Fig. 8, unlike the pixel circuit of Embodiment 1 (see Fig. 1). This makes it possible to provide a large area for organic EL elements in each pixel of a display apparatus employing a bottom emission structure (such a structure that light is emitted toward a transparent substrate having TFT elements).

[0151] This makes it possible to obtain desired luminance in each unit area with less emission of each organic EL element, so that the organic EL element can have a longer luminance half-life.

[0152] In contrast, see a case of a display apparatus employing a top emission structure (such a structure that light is emitted toward a side opposite to a transparent substrate having TFT elements). In this case, the number of elements provided in a pixel never increases, so that each pixel size can be as small as a pixel size in the conventional technique.

[0153] Further, when supplying no current to the organic EL element 16 during the non-selection period, the following operation may be carried out. That is, the potential of the control wire Ej is set at High such that the switching TFT 21 is ON, as shown in Fig. 9 (a period of time 6t1 to 10t1). With this, an OFF potential Voff is supplied to the signal line Tj. Note that, during the period, the respective potentials of the control wire Cj and the control wire Bj are Low.

[0154] With this, the signal line Tj has the OFF potential during the period (6t1 to 10t1), so that substantially no current flows through the organic EL element 16 during a period of time from 5.01 ms to 5.56 ms (see Fig. 10).

[0155] A comparison between this simulation result and the simulation result of the conventional technique (see Fig. 25) clarifies that: the use of the switching TFT 21 of the circuit structure shown in Fig. 8 makes it possible that substantially no current flows through the organic EL element 16. This allows an improvement in contrast of the display apparatus, so that this is preferable.

[Embodiment 3]

[0156] Embodiment 3 will explain a second example in which the first characteristic structure according to the present invention is applied to a pixel circuit and a source driver circuit.

[0157] A display apparatus according to Embodiment 3 is arranged such that the components of the characteristic structure of the present invention are provided separately in the pixel circuit and the source driver circuit. Therefore, the display apparatus has a structure shown in Fig. 7, as is the case with Embodiment 2. For this reason, explanation thereof is omitted here.

[0158] Fig. 11 illustrates respective structures of (i) each pixel circuit Aij and (ii) a source driver output terminal circuit Dj, serving as an output stage of the source driver circuit 50. Each of the pixel circuit Aij and the source driver output terminal circuit Dj includes the components of the characteristic structure of the present invention.

[0159] As shown in Fig. 11, in the pixel circuit Aij of the display apparatus according to Embodiment 3, a single gate wire Gi replaces the three control wires Gi, Wi, and Ri in the pixel circuit structure (see Fig. 8) of Embodiment 2, and an n-type switching TFT 14' replaces the p-type switching TFT 14. In other words, the switching TFTs 13, 15, and 14' in the pixel circuit Aij shown in Fig. 11 are driven by the gate wire Gi.

[0160] Moreover, the power source wire Vs in Fig. 8 is provided in parallel with the source wire Sj, whereas a power source wire Vs in Fig. 11 is provided in parallel with the gate wire Gi. However, the other components of the circuits shown in Fig. 11 are provided in the same manner as those of the circuits shown in Fig. 8 are provided. For this reason, detailed explanation thereof is omitted here.

[0161] The following explains respective operations of the pixel circuit Aij and the output terminal circuit Dj in the display apparatus with reference to Fig. 12. Fig. 12 illustrates respective operation timings of the control wires Gi, Cj, Ej, Bj, and the source wire Sj.

[0162] In a driving method according to Embodiment 3, during a period of time t1 to 5t1 within the selection period of the pixel circuit Aij, the potential of the gate wire Gi is set at High (GH) such that the switching TFT 13 is OFF and that the switching TFTs 14' and 15 are ON.

[0163] During the period, the gate terminal of the driving TFT 11 is connected to the signal line Tj, with the result that the gate terminal of the driving TFT 11 is connected to the first capacitor 12 and the second capacitor 25.

[0164] Meanwhile, during the first period (t1 to 2t1), in the output terminal circuit Dj, the potential of the control wire Cj is set at High such that the switching TFTs 22 and 23 are ON. This connects the gate terminal of the driving TFT 11 to the drain terminal thereof via the switching TFTs 15, 22, and 14'. This also connects the second terminal of the second capacitor 25 to the predetermined voltage line Va.

[0165] With this, a current is constantly supplied from the power source wire Vs to the current output terminal Ij via the driving TFT 11, the switching TFT 14', and the source wire Sj. At the time 2t1, the potential of the control wire Cj is set at Low such that the switching TFTs 22 and 23 becomes OFF. This causes the first capacitor 12 and the second capacitor 25 to retain the potential that the source wire Sj has on this occasion.

[0166] The first capacitor 12 and the second capacitor 25 thus retaining the potential causes the driving TFT 11 to have such a gate potential that compensates the threshold voltage and the mobility of the driving TFT 11, and that allows constant current supply as above (as the aforesaid current supply, during the first period, from the source terminal of the driving TFT 11 to the drain terminal thereof) when the second terminal of the second capacitor 25 has a potential Va.

[0167] Next, during the second period (time 3t1 to time 4t1), the potential of the control wire Bj is set at High such that the switching TFT 24 is ON. This connects the second terminal of the second capacitor 25 to the drain terminal of the driving TFT 11 via the switching TFTs 24 and 14'.

[0168] With this, a predetermined current is supplied from the power source wire Vs to the current output terminal Ij via the driving TFT 11, the switching TFT 14', and the source wire Sj. This makes it possible to determine the gate-source potential of the driving TFT 11 such that a current flows through the driving TFT 11 during the second period irrespective of the threshold voltage and the mobility of the driving TFT 11, while the source-drain potential of the driving TFT 11 is substantially constant.

[0169] At the time 4t1 after this, the potential of the control wire Bj is set at Low such that the switching TFT 24 becomes OFF. This causes the second capacitor 25 to retain the source-gate potential that the driving TFT 11 had during the second period.

[0170] At time 5t1 after this, the potential of the gate wire Gi is set at Low such that the switching TFT 15 becomes OFF. This disconnects the electric connection between the first capacitor 12 and the signal wire Tj, and causes the first capacitor 12 to retain the potential that the signal wire Tj has on this occasion. Also at the time 5t1, the switching TFT 14' is turned OFF so as to disconnect the electric connection between the drain terminal of the driving TFT 11 and the source wire Sj, and the switching TFT 13 is turned ON so as to cause a current to flow from the driving TFT 11 to the organic EL element 16.

[0171] Now, the selection period of the pixel circuit Aij is over, and a following pixel circuit A (i + 1) j is selected.

[0172] A simulation was carried out so as to find values of a current flowing through the organic EL element 16, with the use of the pixel circuit structure (see Fig. 11) and the output terminal circuit structure (see Fig. 11) of the source driver circuit. A result of the simulation is shown in Fig. 13.

[0173] In the simulation shown in Fig. 13, the selection period came every 0.55 ms. During an initial period of time 0.06 ms to 0.61 ms, a current of 0.1 μA was set to flow to the source wire Sj. Thereafter, the current was increased by 0.1 μA every 0.55 ms until the current had a value of 0.9 μA. Then, the current was set at 0. After that, the current was increased again by 0.1 μA.

[0174] Here, a comparison is made between (i) the simulation result according to Embodiment 3, and (ii) the simulation result (see Fig. 25) of the conventional technique. The comparison clarifies that: although Embodiment 3 employs such a structure that the number of the control wires in the pixel circuit Aij is reduced, the structure of Embodiment 3 also makes it possible to reduce the adverse effect of the threshold voltage variation and the mobility variation of the driving TFT 11, and therefore makes it possible to restrain the variation of the current flowing to the organic EL element 16 during the non-selection period.

[0175] Further, the pixel circuit structure (see Fig. 11) according to Embodiment 3 adopts the single control wire Gi unlike the pixel circuit structure (see Fig. 8) described in Embodiment 2. This makes it possible to provide a larger area for organic EL elements in each pixel of a display apparatus employing a bottom emission structure (such a structure that light is emitted toward a transparent substrate having TFT elements). Accordingly, each organic EL element can have a longer luminance half-life, so that this is preferable.

[Embodiment 4]

[0176] Embodiment 4 will explain an example in which a second characteristic structure according to the present invention is applied to a source driver circuit.

[0177] Fig. 14 illustrates a structure of a current output circuit Fj, which serves as an output stage of the source driver circuit of a display apparatus according to Embodiment 3. An output terminal Ij in the current output circuit Fj is, for

example, connected to the source wire Sj shown in Fig. 1, or connected to the current output terminal Ij shown in Fig. 8 and Fig. 11.

[0178] The current output circuit Fj is arranged such that a gate terminal (current control terminal) of a driving TFT 31, serving as an active element, is connected to one terminal (hereinafter, referred to as "first terminal") of a first capacitor 32, and to one terminal (hereinafter, referred to as "first terminal") of a second capacitor 33. Further, the other terminal (hereinafter, referred to as "second terminal") of the first capacitor 32, and a drain terminal (current output terminal) of the driving TFT 31 are connected to a common electrode Vcom.

[0179] Between the gate terminal of the driving TFT 31 and a source terminal (current input terminal) of the TFT, a switching TFTs 34 and 35 are provided in series.

[0180] Further, a switching TFT 36 is provided between the other terminal (hereinafter, referred to as "second terminal") of the second capacitor 33, and a predetermined voltage line Vb. Switching TFTs 37 and 35 are provided in series between the second terminal of the second capacitor 33 and the source terminal of the driving TFT 31.

[0181] Further, a switching TFT 38 is provided between the output terminal Ij of the current output circuit Fj and the source terminal of the driving TFT 31.

[0182] Each of the switching TFTs 34 and 36 has a gate terminal connected to a control wire DCj. The switching TFTs 37, 35, and 38 have gate terminals connected to control wires DPj, DWj, and DRj, respectively.

[0183] The following explains an operation of the current output circuit Fj in the source driver circuit of the display apparatus with reference to Fig. 15. Fig. 15 illustrates respective operation timings of the control wires DRj, DWj, DCj, DPj, and a common current wire Icom.

[0184] In a driving method according to Embodiment 4, during the current setting period corresponding to a period of time from t1 to 5t1, a potential of the control wire DRj is set at Low such that the switching TFT 38 is OFF, and a potential of the control wire DWj is set at High such that the switching TFT 35 is ON.

[0185] During the first period (t1 to 2t1), a potential of the control wire DCj is set at High such that the switching TFTs 34 and 36 are ON. This electrically connects the gate terminal of the driving TFT 31 to the source terminal thereof via the switching TFTs 34 and 35. Further, this also connects the second terminal of the second capacitor 33 to the predetermined voltage line Vb via the switching TFT 36. With this, a current is constantly supplied from the common current wire Icom to the common electrode Vcom via the switching TFT 35 and the driving TFT 31.

[0186] At the time 2t1, the potential of the control wire DCj is set at Low such that the switching TFTs 34 and 36 become OFF. This causes the first capacitor 32 and the second capacitor 33 to retain the potential that the common current wire Icom had during the first period.

[0187] The first capacitor 32 and the second capacitor 33 thus retaining the potential causes the driving TFT 31 to have such a gate potential that compensates the threshold voltage and the mobility of the driving TFT 31, and that allows constant current supply as above (as the aforesaid current supply, during the first period, from the source terminal of the driving TFT 31 to the drain terminal thereof) when the second terminal of the second capacitor 33 has a potential Vb.

[0188] Next, during the second period (time 3t1 to 4t1), the potential of the control wire DPj is set at High such that the switching TFT 37 is ON. This connects the second terminal of the second capacitor 33 to the source terminal of the driving TFT 31 via the switching TFTs 37 and 35. With this, a desired current is supplied from the common wire Icom to the common electrode Vcom via the switching TFT 35 and the driving TFT 31.

[0189] This determines the gate-drain potential of the driving TFT 31 such that a desired current flows into the driving TFT 31 irrespective of the threshold voltage and mobility of the driving TFT 31, while the source-drain potential of the driving TFT 31 is substantially constant.

[0190] At the time 4t1, the potential of the control wire DPj is set at Low such that the switching TFT 37 becomes OFF. This causes the first capacitor 32 and the second capacitor 33 to retain the gate-drain potential that the driving TFT 31 had during the second period.

[0191] At time 5t1 after this, the potential of the control wire DWj is set at Low such that the switching TFT 35 becomes OFF. This disconnects the electric connection between the common current wire Icom and the source terminal of the driving TFT 31. Moreover, the potential of the control wire DRj is set at High such that the switching TFT 38 becomes ON. This causes a desired current to flow from the current output terminal Ij to the driving TFT 31.

[0192] Now, the selection period of the current output circuit Fj is over, and a next current output circuit Fj+ 1 is selected.

[0193] A simulation was carried out to find (i) the source-drain voltage Vsd of the driving TFT 31, and (ii) the gate-drain voltage Vgd thereof, by changing the threshold voltage and the mobility of the driving TFT 31 during the selection period of the current output circuit Fj in accordance with conditions described in Table 3 below. A result of the simulation is shown in Fig. 16.

Table 3

	Ioled(1)	Ioled(2)	Ioled(3)	Ioled(4)	Ioled(5)
	Vgd(1)	Vgd(2)	Vgd(3)	Vgd(4)	Vgd(5)
	Vsd(1)	Vsd(2)	Vsd(3)	Vsd(4)	Vsd(5)
Threshold voltage	Average value	Upper limit value	Lower limit value	Upper limit value	Lower limit value
Mobility	Average value	Upper limit	Lower limit	Lower limit	Upper limit
	value	value	value	value	value

[0194] In Fig. 16, a period of time from 0.61 ms to 0.62 ms corresponds to the aforesaid first period. As shown in Fig. 16, source-drain potentials Vsd (1) through Vsd (5) coincided with source-gate potentials Vsg (1) through Vsg (5), respectively.

[0195] Moreover, a period of time from 0.63 ms to 0.64 ms in Fig. 16 corresponds to the aforesaid second period. As shown in Fig. 16, the source-drain potentials Vsd of the driving TFT 31 were substantially the same during the period, irrespective of the threshold voltage of the driving TFT and the mobility thereof.

[0196] In other words, the desired current flowed from the common current wire Icom to the common electrode Vcom via the switching TFT 35 and the driving TFT 31 during the second period, so that each gate-drain potential Vgd could be set, irrespective of the threshold voltage variation and the mobility variation of the driving TFT, on condition that the source-drain potential of the driving TFT 31 is constant.

[0197] This makes it possible to realize the current output circuit that allows substantially constant current supply, irrespective of the threshold voltage of the driving TFT 31 and the mobility thereof, while the source-drain potential is constant.

[0198] Thereafter, a readout period of the current output circuit Fj started. During the readout period, the substantially constant current output of the driving TFT 31 allows each source-drain potential Vsd of the driving TFT 31 to be substantially constant. Note that, in the simulation, a resistor was provided between the current output terminal Ij and the power source wire Vs, instead of the organic EL element.

[0199] A simulation was carried out to find variation of the current supplied from the driving TFT 31 on this occasion, in accordance with the aforesaid five conditions (see Table 3) pertaining to the threshold voltage and the mobility of the driving TFT 31. A result of the simulation is shown in Fig. 17.

[0200] In the simulation shown in Fig. 17, the selection period came every 0.55 ms. During an initial period of time from 0.06 ms to 0.65 ms, a current of 0.1 μA was set to flow to the source wire Sj. Thereafter, the current was increased by 0.1 μA every 0.55 ms until the current had a value of 0.9 μA. Then, the current was set at 0. After that, the current was increased again by 0.1 μA.

[0201] The simulation result shown in Fig. 17 clarifies that the use of the source driver circuit according to Embodiment 4 provides an effect of restraining the variation of the current flowing through the driving TFT 31, the current variation being caused by the threshold voltage variation and the mobility variation of the driving TFT 31. (Specifically, the current variation at a time of 3.6 ms in Fig. 17 falls within a range from 1.05 μA to 1.15 μA, i.e., falls within a variation range of 9%.)

[0202] Especially, until the output current was 0.8 μA, substantially identical current values were obtained irrespective of the threshold voltage variation and the mobility variation in the driving TFT 31.

[0203] Incidentally, in cases where the characteristic structure of the present invention is used as the source driver circuit, it is preferable that the characteristic structure is also used in a pixel circuit. An example of this is explained as follows.

[0204] That is, the current output terminal Ij of the source driver circuit shown in Fig. 14 is connected to the pixel circuit described in Embodiment 1. An effect of this was examined by carrying out a simulation.

[0205] Firstly, signals were supplied to the control terminals shown in Fig. 14 and Fig. 1 at timings shown in Fig. 18, respectively.

[0206] Fig. 19 illustrates a result of the simulation for examining, by way of the driving timings, the source-drain potential Vsd and the source-gate potential Vsg of the driving TFT 31 shown in Fig. 14.

[0207] In Fig. 19, a period of time from 0.61 ms to 0.65 ms corresponds to the current setting period of the driving TFT 31 of the source driver circuit shown in Fig. 14. On the other hand, a period of time from 0.70 ms to 0.75 ms corresponds to the selection period of the pixel circuit shown in Fig. 1.

[0208] Moreover, a period of time from 0.61 ms to 0.62 ms corresponds to the first period of the driving TFT 31 of the source driver circuit. During the period, the source-drain potentials Vsd of the driving TFT 31 respectively coincided with the gate-drain potentials Vgd thereof, irrespective of the threshold voltage and the mobility in the driving TFT 31.

[0209] Next, a period of time from 0.63 ms to 0.64 ms corresponds to the second period of the driving TFT 31 of the source driver circuit. During the period, the source-drain potentials Vsd of the driving TFT 31 respectively coincided with the source-drain potentials Vsd, irrespective of the threshold voltage of the driving TT 31 and the mobility thereof.

[0210] Next, a period of time from 0.71 ms to 0.72 ms corresponds to the first period of the pixel circuit. During the period, the source-drain potentials Vsd of the driving TFT 31 of the source driver circuit vary according to the threshold voltage variation and the mobility variation of the driving TFT 1 of the pixel circuit. This causes variation of an output current of the driving TFT 31 of the source driver circuit.

[0211] A period of time from 0.73 ms to 0.74 ms corresponds to the second period of the pixel circuit. On the contrary to the first period, during the second period, the source-drain potentials Vsd respectively coincided with the source-drain potentials Vsd, irrespective of the threshold voltage and the mobility of the driving TFT 31 of the pixel circuit. This allows restraint of the variation of a current flowing through the organic EL element 6 provided in the pixel circuit.

[0212] Note that, in this case, it is preferable that the source potential of the source driver circuit upon the current readout corresponds to the potential Vb of the predetermined voltage line. In order to obtain such a source potential, the potential Va of the predetermined voltage line in the pixel circuit, and the potential Vb of the predetermined voltage line may be caused to be equal.

[0213] As such, the characteristic structure of the present invention can be used as the current output circuit of the source driver circuit, and be used in the pixel circuit. The use of the characteristic structure in any of the circuit structures allows a desired current to flow to the driving TFT irrespective of the threshold voltage of the driving TFT and the mobility thereof.

[0214] Further, in cases where a current is supplied from the source driver circuit as shown in Fig. 23, it is preferable that, in the pixel circuit used together with the source driver circuit, a TFT 31' and TFTs 34' through 38' be p-type transistors.

[0215] Note that, in the circuit shown Fig. 21, a source terminal of the driving TFT 31' is connected to the power wire Vs, so that this structure is an example to which the first structure of the present invention is applied. The first structure refers to such a structure that the driving TFT 31' outputs a current.

[Embodiment 5]

[0216] Embodiment 5 will explain a third example in which the first characteristic structure according to the present invention is applied to a pixel circuit and a source driver circuit.

[0217] A display apparatus according to Embodiment 5 also has such a structure that the components of the characteristic structure of the present invention are separately provided in the pixel circuit and in the source driver circuit. Therefore, the display apparatus have the structure shown in Fig. 7, as is the case with Embodiment 2. For this reason, explanation thereof is omitted here.

[0218] Fig. 31 illustrates respective structures of a pixel circuit Aij and a source driver output terminal circuit Dj serving as an output stage of the source driver circuit 50. Each of the pixel circuit Aij and the source driver output terminal circuit Dj includes the components of characteristic structure of the present invention.

[0219] As shown in Fig. 31, in the display apparatus according to Embodiment 5, the pixel circuit Aij is provided in a region in which a source wire Sj and a gate wire Gi intersect with each other. In the pixel circuit Aij, there are provided (i) a driving TFT 41, serving as an active element; (ii) an organic EL element 48, serving as an electric optical element; (iii) a switching TFT 42, serving as a first switching transistor; (iv) a first capacitor 44; and (v) a second capacitor 45. The driving TFT 41 and the organic EL element 48 are provided in series between a power wire Vs and a common wire Vcom.

[0220] Further, the driving TFT 41 has a gate terminal (current control terminal) connected to one terminal (hereinafter, referred to as "first terminal") of the first capacitor 44, and to one terminal (hereinafter, referred to as "first terminal") of the second capacitor 45. The other terminal (hereinafter, referred to as "second terminal") of the first capacitor 44 is connected to a source terminal (current input terminal) of the driving TFT 41, and to the power source wire Vs.

[0221] Further, the switching TFT 42, which serves as the first switching transistor, is provided between the gate terminal (current control terminal) of the driving TFT 41, and the source wire Sj.

[0222] Further, provided in parallel with the source wire Sj is a signal line (connection wire) Tj, which serves as a third wire. The signal line Tj is connected to the other terminal (hereinafter, referred to as "second terminal") of the second capacitor 45 via the switching TFT 43.

[0223] Further, a switching TFT 46 is provided between (i) a drain terminal (current output terminal) of the driving TFT 41, and (ii) an anode of the organic EL element 48. A node of the driving TFT 41 and the switching TFT 46 is connected to the source wire Sj via the switching TFT 47.

[0224] The switching TFTs 42 and 43, each of which is a component of the pixel circuit Aij, have gate terminals connected to the control wires Ci and Gi, respectively. Moreover, each of the switching TFTs 46 and 47 has a gate terminal connected to the control wire Wi.

[0225] In the source driver circuit 50, one output terminal circuit Dj is provided for a plurality of pixel circuits A1j through Anj. As shown in Fig. 31, in the output terminal circuit Dj, a switching TFT 51 serving as the second transistor is provided between the signal line Tj and the source wire Sj. Further, a switching TFT 49, serving as the third switching transistor, is provide between the signal line Tj and a predetermined voltage line Va.

[0226] In the output terminal circuit Dj, the switching TFT 49 has a gate terminal connected to a control wire Cc. Further, the switching TFT 51 has a gate terminal connected to a control wire Bc.

[0227] The following explains respective operations of the pixel circuit Aij and the output terminal circuit Dj in the display apparatus with reference to Fig. 32. Fig. 32 illustrates respective operation timings of the control wires Wi, Gi, Ci, Cc, Bc, and the source wire Sj.

[0228] In a driving method according to Embodiment 5, a period of time from t1 to 6t1 corresponds to a selection period of the pixel circuit Aij. During the period, a potential of the control wire Wi is set at High (GH) such that the switching TFT 46 is OFF and that switching TFT 47 is ON. Further, during a period of time from t1 to 5t1, a potential of the control wire Gi is set at High (GH) such that the switching TFT 43 is ON.

[0229] During a first period (time t1 to time 2t1) within the selection period of the pixel circuit Aij, a potential of the control wire Ci is set at High such that the switching TFT 42 is ON. This electrically connects the gate terminal of the driving TFT 41 to the source wire Sj. With this, the gate terminal of the driving TFT 41 is electrically connected to the drain terminal thereof via the switching TFTs 42 and 47. Accordingly, a current constantly flows from the power source wire Vs to the current output terminal Ij via the driving TFT 41, the switching TFT 47, and the source wire Sj.

[0230] Further, during a period of time t1 to 3t1, the potential of the control wire Cc of the output terminal circuit Dj is set at High such that the switching TFT 49 is ON. This connects the second terminal of the second capacitor 45 to the predetermined voltage line Va via the switching TFT 43, the signal line Tj, and the switching TFT 49.

[0231] Thereafter, the potential of the control wire Ci is set at Low such that the switching TFT 42 becomes OFF. This causes the first capacitor 44 and the second capacitor 45 to retain the potential that the source wire Sj has on this occasion.

[0232] The charge thus retained by the first capacitor 44 and the second capacitor 45 on this occasion causes the driving TFT 41 to have such a gate terminal potential that allows constant current supply as above (as the current supply, during the first period, from the source terminal of the driving TFT 41 to the drain terminal thereof), irrespective of the threshold voltage of the driving TFT 41 and the mobility thereof, while the second terminal of the second capacitor 45 has a potential Va. Thereafter, the control wire Cc is set at Low such that the switching TFT 49 becomes OFF.

[0233] Next, during a second period (time 4t1 to time 5t1), the potential of the control wire Bc is set at High such that the switching TFT 51 is ON. This connects the second terminal of the second capacitor 45 to the drain terminal of the driving TFT 41 via the switching TFTs 43, 51, and 47. With this, a desired current is supplied from the power source wire Vs to the current output terminal Ij via the driving TFT 41, the switching TFT 47, and the source wire Sj.

[0234] This allows a current to flow through the driving TFT 41 as above (as the current supply from the source terminal of the driving TFT 41 to the drain terminal thereof, during the first period) even during the second period, irrespective of the threshold voltage and the mobility of the driving TFT 41, while the source-drain potential of the driving TFT 41 is the potential Vs - Va. In other words, the supply of the desired current to the driving TFT 41 determines the gate-source potential of the driving TFT 41 on condition that the source-drain potential of the driving TFT 41 is substantially constant.

[0235] At the time 5t1 after this, the potential of the control wire Gi is set at Low such that the switching TFT 43 becomes OFF. With this, the source-gate potential of the driving TFT 41 during the second period is retained by the first capacitor 44 and the second capacitor 45.

[0236] At the time 6t1 after this, the potential of the control wire Bc is set at Low such that the switching TFT 51 becomes OFF. This disconnects the electric connection between the signal line Tj and the source wire Sj. Further, the potential of the control wire Wi is set at Low such that the switching TFT 47 becomes OFF, and that the switching TFT 46 becomes ON. With this, a current flows from the driving TFT 41 to the organic EL element 48.

[0237] Now, the selection period of the pixel circuit Aij is over, and a next pixel circuit A (i + 1)j is selected.

[0238] A simulation was carried out to find a current flowing through the organic EL element 48, with the use of the pixel circuit structure (see Fig. 31) and the output terminal circuit structure (see Fig. 31) of the source driver circuit. A result of the simulation is shown in Fig. 33.

[0239] In the simulation of Fig. 33, the selection period came every 0.27 ms. During an initial period of time from 0.30 ms to 0.57 ms, a current of 0.9 μA was set to flow to the source wire Sj. Thereafter, the current was decreased by 0.1 μA every 0.27 ms until the current had a value of 0 μA. Then, the current was set at 0.9 μA again.

[0240] Here, a comparison is made between (i) the simulation result (especially, a result corresponding to a period of time from 0.30 ms to 1.9 ms) according to Embodiment 5 in which the second switching transistor and the third switching transistor are provided in the source driver output terminal circuit Dj, and (ii) the simulation result (see Fig. 25) of the conventional technique. The comparison clarifies that the structure of Embodiment 5 also makes it possible to reduce the adverse effect of the threshold voltage variation of the driving TFT 41 and the mobility variation thereof,

and accordingly makes it possible to restrain the variation of the current flowing to the organic EL element 48 during the non-selection period.

[Embodiment 6]

[0241] Embodiment 6 will explain a case where the second characteristic structure according to the present invention is applied to a pixel circuit.

[0242] As shown in Fig. 34, in each pixel circuit Aij of a display apparatus according to Embodiment 6, a driving TFT 63 and an organic EL element 69 are provided in series between the power source wire Vs and a common wire Vcom. The driving TFT 63 serves as a driving transistor, and the organic EL element 69 serves as an electric optical element.

[0243] The driving TFT 63 has a gate terminal (current control terminal) connected to a source wire Sj via a switching TFT 64, which serves as the first switching transistor. Moreover, the gate terminal of the driving TFT 63 is connected to one terminal (hereinafter, referred to as "first terminal") of a first capacitor 68, and to one terminal (hereinafter, referred to as "first terminal") of a second capacitor 67. The other terminal (hereinafter, referred to as "second terminal") of the first capacitor 68 is connected to a drain terminal (current output terminal) of the driving TFT 63, and to an anode of the organic EL element 69. Moreover, the other terminal (hereinafter, referred to as "second terminal") of the second capacitor 67 is connected to a power source wire (predetermined voltage line) Vs via a switching TFT 65, and to the source wire Sj via a switching TFT 66. The switching TFT 65 serves as the third switching transistor, and the switching TFT 66 serves as the second switching transistor.

[0244] Respective gate terminals of the switching TFTs 64 and 65 are connected to a control wire Ci, and a gate terminal of the switching TFT 66 is connected to a control wire Gi.

[0245] A switching TFT 61 is provided between a source terminal (current input terminal) of the driving TFT 63, and the power source wire Vs. The switching TFT 61 has a gate terminal connected to a control wire Ri. A node of the driving TFT 63 and the switching TFT 61 is connected to the source wire Sj via a switching TFT 62. The switching TFT 62 has a gate terminal connected to the control wire Wi.

[0246] Note that any of the control wires Ci, Gi, and Wi may serve as a second wire (gate wire). Note also that any of the switching TFTs 62, 64, and 66 may serve as a selection TFT.

[0247] In the circuit structure, the gate terminal of the driving TFT 63 is connected to the source terminal of the driving TFT 63 via the switching TFT 64, the source wire Sj, and the switching TFT 62. Further, the second terminal of the second capacitor 67 is connected to the source terminal of the driving TFT 63 via the switching TFT 66, the source wire Sj, and the switching TFT 62.

[0248] The following explains an operation of the pixel circuit Aij of the display apparatus with reference to Fig. 35. Fig. 35 illustrates respective operation timings of the control wires Ri, Wi, Ci, Gi, and the source wire Sj.

[0249] In a driving method according to Embodiment 6, the selection period corresponds to a period of time from 0 to 6t1. During the period, a potential of the control wire Ri is set at High (GH) such that the switching TFT 61 is OFF. Moreover, during a period of time from t1 to 5t1, a potential of the control wire Wi is set at Low (GL) such that the switching TFT 62 is ON.

[0250] During the first period (time t1 to 2t1), a potential of the control wire Ci is set at Low such that the switching TFTs 64 and 65 are ON. This connects the gate terminal of the driving TFT 63 to the source terminal thereof via the switching TFTs 64 and 62. This also connects the second terminal of the second capacitor 67 to the power source line (predetermined voltage line) Vs via the switching TFT 65. With this, a current flows constantly from a source driver circuit (not shown) to the organic EL element 69 via the source wire Sj, the switching TFT 62, and the driving TFT 63.

[0251] Thereafter (at the time 2t1), the potential of the control wire Ci is set at High such that the switching TFTs 64 and 65 become OFF. This causes the first capacitor 68 and the second capacitor 67 to retain the potential, determined during the first period, of the source wire Sj.

[0252] Next, during the second period (time 3t1 to 4t1), a potential of the control wire Gi is set at Low such that the switching TFT 66 is ON. This connects the second terminal of the second capacitor 67 to the source terminal of the driving TFT 63 via the switching TFTs 66 and 62. With this, a predetermined current flows from the source driver circuit (not shown) to the organic EL element 69 via the source wire Sj, the switching TFT 62, the driving TFT 63.

[0253] Thereafter (at the time 4t1), the potential of the control wire Gi is set at High such that the switching TFT 66 becomes OFF. This causes the first capacitor 68 and the second capacitor 67 to retain the drain-gate potential, determined during the second period, of the driving TFT 63.

[0254] Thereafter, the potential of the control wire Wi is set at High such that the switching TFT 62 becomes OFF, and the potential of the control wire Ri is set at Low such that the switching TFT 61 becomes ON.

[0255] Now, the selection period of the pixel circuit Aij is over, and a next pixel circuit A(i + 1)j is selected.

[0256] Note that, in the source driver output terminal circuit Dj shown in Fig. 34, a switching TFT 70, serving as a fourth transistor, is provided between an OFF potential line Voff and the source wire Sj.

[0257] The switching TFT 70 has a gate terminal connected to a control wire Ej. In the case of supplying no current

to the selected organic EL element 69, the control wire Ej is set at High during the second period (9t1 to 11t1) such that the switching TFT 70 is ON, as shown in Fig. 35. This allows an open connection between the source wire Sj and the current output circuit of the source driver. With this, an OFF potential is supplied from the OFF potential line Voff to the source wire.

[0258] The OFF potential is a potential equal to or lower than a potential of the common electrode Vcom. Therefore, when the OFF potential supplied via the switching TFT 62 becomes the source potential of the driving TFT 63, or when the OFF potential causes the switching TFT 62 to be OFF, the gate potential of the driving TFT 63 is discharged from the source terminal thereof. This decreases the gate potential of the driving TFT 63 to a potential lower than the potential that driving TFT 63 had during the first period, with the result that the driving TFT 63 becomes OFF.

[0259] A simulation was carried out to find a current flowing through the organic EL element 69, with the use of the pixel circuit structure (see Fig. 34) and the output terminal circuit structure (see Fig. 34) of the source driver circuit. A result of the simulation is shown in Fig. 36.

[0260] In the simulation of Fig. 36, the selection period came every 1.08 ms. During an initial period of time from 2.30 ms to 3.38 ms, a current of 1.1 μA was set to flow to the source wire Sj. Thereafter, the current decreased by 0.12 μA every 1.08 ms until no current (a current of 0 μA) flowed. Then, the current of 1.1 μA was set to flow again.

[0261] Here, a comparison is made between (i) the simulation result according to Embodiment 6 employing a structure that controls the current control terminal of the driving transistor and the current input terminal thereof, and (ii) the simulation result (see Fig. 25) of the conventional technique. The comparison clarifies that the structure of Embodiment 6 also makes it possible to reduce the adverse effect of the threshold voltage variation and the mobility variation of the driving TFT 63, and accordingly makes it possible to restrain the variation of the current flowing to the organic EL element 69 during the non-selection period.

[0262] Note that there is provided, in the pixel circuit structure shown in Fig. 1, the power source wire Va for supplying the predetermined potential Va to the second terminal of the second capacitor 7. However, in the pixel circuit to which the second characteristic structure according to the present invention is applied, the predetermined potential wire and the power source wire Vs can be shared with each other. For this reason, no power source wire Va may be provided as shown in Fig. 34.

[0263] Further, there may be provided, in the source driver circuit, a part of the components of the means of the present invention, i.e., one or more of the driving TFT, the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor, as shown in Fig. 37.

[0264] Specifically, in a pixel circuit structure Aij shown in Fig. 37, a first capacitor 98 is provided between a gate of a driving TFT 94 and a drain thereof, a first switching TFT 95 is provided between a gate terminal of the driving TFT 94 and the source wire Sj, and a second capacitor 97 and a switching TFT 93 are provided in series between a gate terminal of the driving TFT 94 and a signal line Tj. An organic EL element 96 is provided between a drain terminal of the driving TFT 94 and a common electrode Vcom. Moreover, a switching TFT 91 is provided between a source terminal of the driving TFT 94 and a power source wire Vs. Further, a switching TFT 92 is provided between the source terminal of the driving TFT 94 and a source wire Sj.

[0265] Moreover, in a source driver output terminal circuit Dj, a switching TFT 100, serving as the second switching transistor, is provided between the signal line Tj and the source wire Sj. Provided between the signal Tj and the predetermined voltage line Vb is a switching TFT 99, which serves as the third switching transistor.

[0266] As is the case with the pixel circuit shown in Fig. 31, the timings shown in Fig. 32 also respectively correspond to timings of the driving operation using the pixel circuit Aij and the source driver output terminal circuit Dj. For this reason, explanation thereof is omitted here.

[Embodiment 7]

[0267] Embodiment 7 explains another example in which the second characteristic structure according to the present invention is applied to a pixel circuit and a source driver circuit.

[0268] A display apparatus according to Embodiment 7 also has such a structure in which the components of the characteristic structure of the present invention are separately provided in the pixel circuit and the source driver circuit. Therefore, the display apparatus has a structure shown in Fig. 7 as is the case with Embodiment 2, so that explanation thereof is omitted here.

[0269] Fig. 38 illustrates respective structures of the pixel circuit Aij and the source driver output terminal circuit Dj, which serves as an output stage of the source driver circuit 50. Each of the pixel circuit Aij and the source driver output terminal circuit Dj includes the components of the characteristic structure of the present invention.

[0270] As shown in Fig. 38, in the display apparatus according to Embodiment 7, each pixel circuit Aij is provided in a region in which a source wire Sj and a gate wire Gi intersect with each other. Provided in the pixel circuit Aij are a driving TFT 74, an organic EL element 76, and a first capacitor 75. The driving TFT 74 serves as an active element, and the organic EL element 76 serves as an electric optical element, and the driving TFT 74 and the organic EL element

76 are provided in series between a power source wire Vs and a common wire Vcom.

[0271] The driving TFT 74 has a gate terminal (current control terminal) connected to one terminal (hereinafter, referred to as "first terminal") of the first capacitor 75. The other terminal (hereinafter, referred to as "second terminal") of the first capacitor 75 is connected to a drain terminal (current output terminal) of the driving TFT 74, and to an anode of the organic EL element 76.

[0272] Further, in the pixel circuit structure, a signal line Tj, serving as the third wire, is provided in parallel with the source wire Sj, and is connected to the gate terminal of the driving TFT 74 via the switching TFT 73.

[0273] Further, a switching TFT 71 is provided between a source terminal (current input terminal) of the driving TFT 74, and the power wire Vs. A node of the driving TFT 74 and the switching TFT 71 is connected to the source wire Sj via a switching TFT 72.

[0274] These components of the pixel circuit Aij, i.e., the switching TFTs 73, 72, 71 have gate terminals connected to control wires Gi, Wi, and Ri, respectively.

[0275] In the source driver circuit 50, each output terminal circuit Dj is provided for a plurality of pixel circuits A1j through Anj. In the output terminal circuit Dj, the signal line Tj is connected to one terminal (hereinafter, referred to as "first terminal") of a second capacitor 80 as shown in Fig. 38. Moreover, provided between the signal line Tj and the source wire Sj is a switching TFT 77, which serves as the first switching transistor. Further, a switching TFT 78, serving as the third switching transistor, is provided between (i) the other terminal (hereinafter, referred to as "second terminal") of the second capacitor 80, and (ii) a predetermined voltage line Va. Provided between the second terminal of the second capacitor 80 and the source wire Sj is a switching TFT 79, which serves as the second switching transistor. Further, a switching TFT 81, serving as the fourth switching transistor, is provided between the signal line Tj and an OFF potential line Voff.

[0276] In the output terminal circuit Dj, the switching TFT 81 has a gate terminal connected to a control wire Ej, and the switching TFTs 77 and 78 each have gate terminals connected to a control wire Cc, and the switching TFT 79 has a gate terminal connected to a control wire Bc.

[0277] The following explains respective operations of the pixel circuit Aij and the output terminal circuit Dj in the display apparatus with reference to Fig. 39. Fig. 39 illustrates respective operation timings of the control wires Ri, Wi, Gi, Cc, Bc, Ej, and the source wire Sj.

[0278] In a driving method according to Embodiment 7, the selection period of the pixel circuit Aij corresponds to a period of time from 0 to 6t1. During the period, a potential of the control wire Ri is set at High (GH) such that the switching TFT 71 is OFF. Further, during a period of time from t1 to 5t1, a potential of the control wire Wi is set at Low (GL) such that the switching TFT 72 is ON. This connects the source terminal of the driving TFT 74 to the source wire Sj.

[0279] Further, in the pixel circuit Aij, during a period of time from t1 to 4t1, a potential of the control wire Gi is set at Low such that the switching TFT 73 is ON. This electrically connects the gate terminal of the driving TFT 74 to the signal line Tj. With this, the gate terminal of the driving TFT 74 is connected to the first capacitor 75 and the second capacitor 80.

[0280] Meanwhile, in the output terminal circuit Dj, during a first period (time t1 to time 2t1), a potential of the control wire Cc is set at High such that the switching TFTs 77 and 78 are ON. This electrically connects the gate terminal of the driving TFT 74 to the source terminal thereof via the switching TFTs 73, 77, and 72. This also connects the second terminal of the second capacitor 80 to the predetermined voltage line Va via the switching TFT 78. With this, a current constantly flows from the source driver circuit (not shown) to the organic EL element 76 via the source wire Sj, the switching TFT 72, and the driving TFT 74.

[0281] Thereafter, the potential of the control wire Cc is set at Low such that the switching TFTs 77 and 78 become OFF. This causes the first capacitor 75 and the second capacitor 80 to retain the potential that the signal wire Tj has on this occasion.

[0282] The charge thus stored by the first capacitor 75 and the second capacitor 80 on this occasion causes the driving TFT 74 to have a gate potential allowing constant current supply as above (as the aforesaid current supply, during the first period, from the source terminal of the driving TFT 74 to the drain terminal thereof), while the second terminal of the second capacitor 80 has a potential Va, irrespective of the threshold voltage of the driving TFT 74 and the mobility thereof.

[0283] Next, during a second period (time 3t1 to time 4t1), the potential of the control wire Bc is set at High such that the switching TFT 79 becomes ON. This connects the second terminal of the second capacitor 80 to the source terminal of the driving TFT 74 via the switching TFTs 79 and 72. With this, a desired current flows from the source driver circuit (not shown) to the organic EL element 76 via the source wire Sj, the switching TFT 72, and the driving TFT 74.

[0284] This allows a current to flow through the driving TFT 74 as above (as the current supply, during the first period, from the source of the driving TFT 74 to the drain thereof) even during the second period irrespective of the threshold voltage and the mobility of the driving TFT 74, while the source-drain potential of the driving TFT 74 is the potential Va - Vx (Vx indicates an anode potential that the organic EL element 76 has during the second period). In other words, the supply of the desired current to the driving TFT 74 can determine the gate-source potential of the driving TFT on

condition that the source-drain potential of the driving TFT 74 is substantially constant.

[0285] At the time 4t1 after this, the potential of the control wire Gi is set at High such that the switching TFT 73 becomes OFF. This causes the first capacitor 75 to retain the drain-gate potential that the driving TFT 74 had during the second period.

[0286] At the time 5t1 after this, the potential of the control wire Bc is set at Low such that the switching TFT 79 becomes OFF. This disconnects the electric connection between the second capacitor 80 and the source wire Sj. Moreover, the potential of the control wire Wi is set at High such that the switching TFT 72 becomes OFF. This disconnects the electric connection between the source terminal of the driving TFT 74 and the source wire Sj. Further, at the time 6t1, the potential of the control wire Ri is set at Low such that the switching TFT 71 becomes ON. With this, a current flows from the driving TFT 74 to the organic EL element 76.

[0287] Now, the selection period of the pixel circuit Aij is over, and then a following pixel circuit A(i+1)j is selected.

[0288] Further, during a period of time from 9t1 to 11t1 in Fig. 39, the potential of the control wire Ej is set at High such that the switching TFT 81 becomes ON. This causes an OFF potential Voff to be supplied to the signal line Tj, with the result that the signal line Tj is caused to have the OFF potential. This allows substantially no current to flow into the organic EL element 76 during the non-selection period. Note that, during the period, the potential of the control wire Cc is Low, and the potential of the control wire Bc is High.

[0289] A simulation was carried out to find a current flowing through the organic EL element 76, with the use of the pixel circuit structure and the output terminal circuit structure of the source driver circuit. A result of the simulation was similar to the result of Embodiment 6.

[Embodiment 8]

[0290] Embodiment 8 will explain a characteristic operation of a driving method according to the present invention. The driving method of Embodiment 8 solves a problem that arises in Embodiment 2 in which the components of the characteristic structure of the present invention are provided separately in the pixel circuit and the source driver circuit. Firstly, this problem is explained.

[0291] In an actual display apparatus, stray capacitances exist in the source wire Sj and the signal wire Tj, which are provided across the pixel circuit Aij (see Fig. 8) and the source driver output terminal circuit Dj (see Fig. 8). Supposing that each stray capacitance is 5 pF, a simulation was carried out to examine respective changes of (i) a current Ip flowing through the driving TFT 11 of the pixel circuit Aij shown in Fig. 8, and (ii) the source-drain potential Vsd of the driving TFT 11. A result of the simulation is shown in Fig. 40.

[0292] In Fig. 40, a period of time from 0.992 ms to 1.080 ms corresponds to the selection period. During the period, the control wire Ri was set at High such that the switching TFT 13 was OFF, and the control wire Wi was set at Low such that the switching TFT 14 was ON. Moreover, a period of time from 0.992 ms to 1.024 ms corresponds to the first period in the driving method of the present invention. During the period, the gate wire Gi was set at High such that the switching TFT 15 was ON, and the control wire Cj was set at High such that the switching TFTs 22 and 23 were ON.

[0293] This short-circuited the gate terminal of the driving TFT 11 and the drain terminal thereof, with the result that the gate terminal of the driving TFT 11 was connected to the capacitors 12 and 25, and that the second terminal of the capacitor 25 was connected to the predetermined voltage line Va. It took 20 μs until the gate-source potential Vsd of the driving TFT 11 became stable. Thereafter, the control wire Cj was set at Low such that the switching TFTs 22 and 23 became OFF. Now, the first period was finished.

[0294] Further, a period of time from 1.034 ms to 1.074 ms corresponds to the second period in the driving method of the present invention. During the period, the control wire Bj was set at High such that the switching TFT 24 was ON.

[0295] During the period, the potential of the second terminal of the second capacitor 25 approached to Va, so that the driving TFT 11 has a source-drain potential of substantially Vs - Va. On condition that the source-drain potential was substantially constant, the source-gate potential of the driving TFT 11 was determined. This allowed the current to constantly flow through the driving TFT 11, irrespective of the threshold voltage of the driving TFT 11 and the mobility property thereof. It took 30 μs until the current Ip stably flowed from the source to the drain. Thereafter, the gate wire Gi was set at Low such that the switching TFT 15 became OFF. Now, the selection period was over.

[0296] During the non-selection period coming after this (see a part corresponding to time at and after 1.096 ms), the source-drain potential Vsd of the driving TFT 11 was constant, and the current Ip constantly flowed from the source of the driving TFT 11 to the drain thereof.

[0297] Note that source-drain potentials Vsd (1) through Vsd(5), and source-drain currents Ip (1) through Ip(5) in Fig. 40 are results obtained by changing the threshold voltage of the driving TFT 11 and the mobility thereof in accordance with the conditions shown in Table 2.

[0298] As such, the use of the present driving method makes it possible to constantly supply a current to the organic EL element 16, irrespective of the threshold voltage variation and the mobility variation of the driving TFT 11. This allows acquirement of a uniform display.

[0299] However, for such acquirement, the selection period is required to be longer than the selection period of the conventional pixel circuit structure (see Fig. 22). Specifically, a period as long as the first period shown in Fig. 40 is sufficient for the selection period of the pixel circuit structure shown in Fig. 22, whereas the driving method of the present invention requires the first and second periods shown in Fig. 40 for the selection period. For shortening the selection period in the driving method of the present invention, the second period is required to be shorter.

[0300] Fig. 41 illustrates a circuit structure for realizing such a driving method. The circuit structure shown in Fig. 41 has a structure in which the components of the first characteristic structure are separately provided in the pixel circuit Aij and the source driver output terminal circuit Dj, as is the case with the circuit structure shown in Fig. 8. In Fig. 41, capacitors, TFTs, and the like, each of which has the equivalent functions as each of those shown in Fig. 8, will be given the same reference symbols, and detailed explanation thereof will be omitted here.

[0301] Note that, in the circuit structure shown in Fig. 41, the stray capacitance of the source wire Sj is represented by a capacitor 17, and the stray capacitance of the signal wire Tj is represented by a capacitor 18. Note also that the signal line Tj is connected to a protection circuit made up of TFTs 19 and 20.

[0302] In the protection circuit, the n-type TFT 19 is provided between the signal line Tj and the power wire Vs, and the p-type TFT 20 is provided between the signal line Tj and the common wire Vcom. Further, a potential DL is supplied to a gate terminal of the TFT 19, and a potential DH is supplied to a gate terminal of the TFT 20.

[0303] With this, when the signal line Tj has a potential lower than DL (precisely, a potential obtained by subtracting a threshold potential of the TFT 19 from the potential DL), a current flows from the power source wire Vs to the signal line Tj. This protects the potential from further decreasing. On the contrary, when the signal line Tj has a potential higher than DH (precisely, a potential obtained by adding the potential DH to a threshold potential of the TFT 20), a current flows from the signal line Tj to the common wire Vcom. This protects the potential from further increasing.

[0304] Further, in the circuit structure shown in Fig. 41, the gate terminal of the switching TFT 22, which serves as the first switching element, is not wired to the gate terminal of the switching TFT 23, which serves as the third switching element. Instead, the gate terminal of the switching TFT 22 is wired (connected) to the control wire Cc, and the gate terminal of the switching TFT 23 is wired (connected) to the control wire Fc. Further, the signal wire Bj in Fig. 8 is replaced with the signal line Bc. This allows the signal wire Bj to be a common wire independent from the source wire Sj.

[0305] The following explains respective operations of the pixel circuit Aij (see Fig. 41) and the output terminal circuit Dj (see Fig. 41) with reference to Fig. 42. Fig. 42 illustrates respective operation timings of the control wires Gi, Wi, Cc, Bc, Fc, Ej, and the source wire Sj.

[0306] That is, during the selection period of the pixel circuit Aij, i.e., during a period of time from t1 to 8t1, the potential of the control wire Wi is set at High (GH) such that the switching TFT 13 is OFF, and that the switching TFT 14 is ON.

[0307] In the pixel circuit Aij, during the first period (time t1 to 4t1), the potential of the control wire Gi is set at High such that the switching TFT 15 is ON. This electrically connects the gate terminal of the driving TFT 11 to the signal line Tj. With this, the gate of the driving TFT 11 is connected to the first capacitor 12 and the second capacitor 25.

[0308] Meanwhile, during the period, in the output terminal circuit Dj, the potential of the control wire Cc is set at High such that the switching TFT 22 is ON, and the potential of the control wire Fc is set at High such that the switching TFT 23 is ON. This electrically connects the gate terminal of the driving TFT 11 to the drain terminal thereof via the switching TFTs 15, 22, 14. This also connects the second terminal of the second capacitor 25 to the predetermined voltage line Va via the switching TFT 23. With this, a current constantly flows from the power source wire Vs to the current output terminal Ij via the driving TFT 11, the switching TFT 14, and the source wire Sj.

[0309] At the time 4t1 after this, the potential of the control wire Cc is set at Low such that the switching TFT 22 becomes OFF. This causes the first capacitor 12 and the second capacitor 25 to retain the potential that the source wire Sj has on this occasion.

[0310] The first capacitor 12 and the second capacitor 25 thus retaining the potential on this occasion causes the driving TFT 11 to have a gate potential allowing constant current supply as above (as the aforesaid current supply, during the first period, from the source terminal of the driving TFT 11 to the drain terminal thereof) while the second terminal of the second capacitor 25 has a potential Va; irrespective of the threshold voltage and the mobility of the driving TFT 11.

[0311] Next, during a second period (time 5t1 to time 7t1), the potential of the control wire Bc is set at High such that the switching TFT 24 is ON. This connects the second terminal of the second capacitor 25 to the drain terminal of the driving TFT 11 via the switching TFTs 24 and 14. With this, a desired current flows from the power source wire Vs to the current output terminal Ij via the driving TFT 11, the switching TFT 14, and the source wire Sj.

[0312] However, in the present driving method shown in Fig. 42, the control wire Fc is High during a period of time from t1 to 6t1. That is, the switching TFT 23 is still ON even after the start of the second period. This allows a voltage to be supplied from the predetermined voltage line Va to the second terminal of the second capacitor 25 during a first part, continuing from 5t1 to 6t1, of the second period continuing from time 5t1 to time 7t1, unlike the driving method shown in Fig. 9. The current causes the source wire Sj to have the potential Va. (The driving TFT 11 is so set as to allow a current to constantly flow therethrough, so that the current thus constantly supplied flows between the power

source wire Vs and the predetermined voltage line Va.)

[0313] As such, in the driving method shown in Fig. 42, the potential of the source wire Sj is set at Va in advance, and then the control wire Fc is set at Low such that the switching TFT 23 becomes OFF. During the rest of the second period, i.e., during the period of time from 6t1 to 7t1, the potential of the source wire Sj is changed in conformity with the threshold voltage and the mobility property of the driving TFT 11. With this, on condition that the source-drain potential of the driving TFT 11 is substantially constant, the gate-source potential of the driving TFT can be determined.

[0314] At the time 7t1 after this, the potential of the control wire Gi is set at Low such that the switching TFT 15 becomes OFF. This causes the first capacitor 12 to retain the source-gate potential that the driving TFT 11 has during the second period.

[0315] At time 8t1 after this, the potential of the control wire Bc is set at Low such that the switching TFT 24 becomes OFF. This disconnects the electric connection between the second capacitor 25 and the source wire Sj. Moreover, the potential of the control wire Wi is set at Low such that the switching TFT 14 becomes OFF, and that the switching TFT 13 becomes ON. This causes a current to flow from the driving TFT 11 to the organic EL element 16.

[0316] As such, in the driving method of Fig. 42, a voltage is supplied from the predetermined voltage line Va to the second terminal of the second capacitor 25 even during the first part, continuing from time 5t1 to 6t1, of the second period continuing from 5t1 to 7t1, unlike the driving method of Fig. 9. This allows the source-drain potential Vsd of the driving TFT 11 to be substantially constant from the beginning of the second period, and accordingly allows the current Ip, flowing between the source terminal and the drain terminal of the driving TFT 11, to be substantially constant from the beginning of the second period, as shown in a simulation result of Fig. 43.

[0317] Thereafter, the source-gate potential Vsg of the driving TFT 11 is changed so as to compensate the threshold voltage and the mobility property of the driving TFT 11 (the source-drain potential Vsd of the driving TFT 11 is also changed in response to the change of the source-gate potential Vsg). The potential thus changed is retained by the first capacitor 12, by setting the gate wire Gi at Low. This allows a current to be uniformly supplied to the organic EL element 16 during the non-selection period, irrespective of the threshold voltage variation and the mobility variation of the driving TFT 11.

[0318] In the simulation shown in Fig. 43, the second period corresponds to a period of time from 0.618 to 0.634, i. e., continues for 16 μs. Therefore, for 8 μs corresponding to the first part of the second period, the predetermined potential wire Va and the second terminal of the second capacitor 25 are short-circuited. In consideration of this, the driving method shown in Fig. 42 can shorten the second period as compared with the driving method shown in Fig. 9.

[0319] Further, in the driving method of the present invention, the first period is not required to continue until the gate-source potential Vsd of the driving TFT 11 becomes stable.

[0320] The reason for this is as follows. That is, expected variation upon the completion of the first period is substantially no different from the variation in the conventional pixel circuit structure shown in Fig. 22. Moreover, expected variation while the source wire Sj has the potential Va after the start of the second period is also substantially no different from the variation in the conventional pixel circuit structure shown in Fig. 22. However, during the rest of the second period, i.e., while changing the potential of the source wire Sj from Va, the variation is reduced as compared with the variation of the conventional pixel circuit structure shown in Fig. 22.

[0321] As such, even though the gate-source potential Vsd of the driving TFT 11 is varied to some extent upon the completion of the first period, the variation is compensated during the second period. This allows a current to be uniformly supplied to the organic EL element 16 during the non-selection period irrespective of the threshold voltage variation and the mobility variation of the driving TFT 11.

[0322] As such, the preferable driving example of the driving method of the present invention makes it possible to shorten the length of the second period, with the result that the required selection period is shorter. On this account, a larger number of the gate wires Gi can be driven, and a larger number of the pixels can be accordingly used for a display. As such, the preferable driving example is apparently beneficial.

[Embodiment 9]

[0323] There is another means for solving the aforesaid problem that the circuit structure shown in Fig. 8 causes the selection period to be longer. Specifically, it is effective that the second capacitor is provided close to a pixel circuit provided together with a source driver circuit. Note that the first characteristic structure according to the present invention is applied to each of the pixel circuit and the source driver circuit.

[0324] A specific example of such a circuit structure is a circuit structure (see Fig. 44) made up of a pixel circuit, a source driver output terminal circuit Dj, and another circuit Bij. In Fig. 44, capacitors and TFTs carrying out the equivalent operations as those shown in Fig. 8 are given the same reference symbols, and explanation thereof will be omitted here.

[0325] In the circuit structure shown in Fig. 44, the aforesaid another circuit Bij, made up of a second capacitor 27 and a switching TFT 26, is provided for every two pixel circuits Aij and A(i+1)j. Further, in each of the pixel circuit Aij and A(i+1)j, a switching TFT 25 is provided between a gate terminal of a driving TFT 11 and a first terminal of the

second capacitor 27.

[0326] This shortens a length of a wire connecting the gate terminal of the driving TFT 11 to the second capacitor 27. Accordingly, a stray capacitance of the wire is restrained, so that even a second capacitor 27 having a small capacitance works sufficiently. Specifically, the second capacitor 25 shown in Fig. 41 has a capacitance of approximately 2 pF, whereas the second capacitor 27 shown in Fig. 44 has a capacitance of approximately 1 pF as is the case with the first capacitor 12.

[0327] The following explains an operation of the pixel circuit shown in Fig. 44, with reference to Fig. 45. Fig. 45 illustrates respective operation timings of control wires Gi, Wi, Pi, Gi+1, Wi+1, Fc, Bc, and a source wire Sj.

[0328] That is, the selection period of the pixel circuit Aij corresponds to a period of time from t1 to 8t1 in the timings shown in Fig. 45. During the period, a potential of the control wire Wi is set at High (GH) such that a switching TFT 13 is OFF, and that a switching TFT 14 is ON.

[0329] During a first period (time t1 to 4t1), a potential of the control wire Gi is set at High such that the switching TFT 25 is ON, and a potential of the control wire Fc is set at High such that the switching TFT 28 in the source driver output terminal circuit Dj is ON, and a potential of the control wire Pi is set at High such that the switching TFT 26 is ON.

[0330] This electrically connects the gate terminal of the driving TFT 11 to the drain terminal thereof via the switching TFTs 25, 26, 14. This also connects the second terminal of the second capacitor 27 to a predetermined voltage line Va via a signal line Tj and a switching TFT 28. With this, a current is constantly supplied from a power source wire Vs to a current output terminal Ij via the driving TFT 11, the switching TFT 14, and the source wire Sj.

[0331] Thereafter (at the time 4t1), the potential of the control wire Pi is set at Low such that the switching TFT 26 becomes OFF. This causes the first capacitor 12 and the second capacitor 27 to retain the potential, determined during the first period, of the source wire Sj.

[0332] During the second period (time 5t1 to time 7t1), the potential of the control wire Bc is set at High such that a switching TFT 29 in the source driver output terminal circuit Dj is ON. Moreover, the control wire Fc is maintained to be High during the first part (time 5t1 to time 6t1) of the second period such that the source wire Sj has a predetermined potential Va.

[0333] During the rest (time 6t1 to 7t1) of the second period, the potential of the gate wire Gi is set at Low such that the switching TFT 27 is OFF, after the current Ip flowing between the source of the driving TFT 11 and the drain thereof becomes stable. Then, the potential of the control wire Bc is set at Low such that the switching TFT 29 becomes OFF. Then, the selection period of the pixel A(i + 1)j starts.

[0334] That is, the selection period of the pixel circuit A(i + 1) j corresponds to a period of time from 9t1 to 16t1 in the timings shown in Fig. 44. During the period, a potential of the control wire Wi+1 is set at High (GH) such that a switching TFT 13 is OFF, and that a switching TFT 14 is ON.

[0335] During a first period (time 9t1 to 12t1), a potential of the control wire Gi+1 is set at High such that the switching TFT 25 is ON, and the potential of the control wire Fc is set at High such that the switching TFT 28 is ON, and the potential of the control wire Pi is set at High such that the switching TFT 26 is ON.

[0336] This electrically connects the gate terminal of the driving TFT 11 to the drain terminal thereof via the switching TFTs 25, 26, and 14. This also connects the second terminal of the second capacitor 27 to the predetermined voltage line Va via the signal line Tj and the switching TFT 28. On this occasion, a current constantly flows from the power source wire Vs to the current output terminal Ij via the driving TFT 11, the switching TFT 14, and the source wire Sj.

[0337] Thereafter (at the time 12t1), the potential of the control wire Pi is set at Low such that the switching TFT 26 becomes OFF. This causes the first capacitor 12 and the second capacitor 27 to retain the potential, determined during the first period, of the source wire Sj.

[0338] During a second period (time 13t1 to time 15t1), the potential of the control wire Bc is set at High such that the switching TFT 29 is ON. Moreover, the control wire Fc is maintained to be High during a first part (time 13t1 to time 14t1) of the second period such that the source wire Sj has a predetermined potential Va.

[0339] During the rest (time 14t1 to 15t1) of the second period, the potential of the gate wire Gi is set at Low after the current Ip stably flows between the source of the driving TFT 11 and the drain thereof. With this, the switching TFT 27 is OFF.

[0340] By providing the aforesaid another circuit Bij for every two pixels Aij and A(i + 1) in this way, the means of the present invention can be attained.

[0341] Further, each shorter wire between the gate terminal of each driving TFT 11 and the second capacitor 27 restrains the stray capacitance of the wire, so that even a second capacitor 27 having a small capacitance allows the effect of the means of the present invention. (The effect indicates that a current is constantly supplied from the driving TFT 11 to the organic EL 16, irrespective of the threshold voltage variation and the mobility property variation of the driving TFT 11.)

[0342] Moreover, as compared with the circuit structure shown in Fig. 1, the circuit structure allows reduction of the respective number of the second capacitor 27 and the switching TFT 26, each of which is required for every two pixels Aij and A(i + 1)j. With this, an open area ratio can be increased.

[0343] Embodiments described above assume that each organic EL used therein is a polymer molecule organic EL. While a manufacture of an organic EL element made of a low molecular organic EL requires vapor deposition, a manufacture of an organic EL element made of a polymer molecule organic EL employs an ink jet process. In the latter case, a hydrophilic hole is formed, for each driving TFT, in a hydrophobic bank. However, the hole is not necessarily required to be formed per pixel, but may be shared by a plurality of RGB color pixels. Especially, it is preferable to form a stripe-shaped hole having droplet recipients on both ends, because a size of each droplet recipient can be determined irrespective of RGB pixel pitches.

INDUSTRIAL APPLICABILITY

[0344] The present invention is applicable to a display apparatus using a current driving element, such as an organic EL (Electro Luminescence) display and an FED (Field Emission Display). The present invention allows restraint of variation of a current flowing through the current driving element during the non-selection period, thereby improving display quality.

Claims

1. A display apparatus including a current driving light emitting element and a driving transistor, the display apparatus comprising:

   a first switching transistor, provided between (i) a current control terminal of the driving transistor and (ii) a current output terminal of the driving transistor;
   a first capacitor, connected to the current control terminal of the driving transistor; and
   a second capacitor, having a first terminal and a second terminal, the first terminal being connected to the current control terminal of the driving transistor, the second terminal being connected to (i) the current output terminal of the driving transistor via a second switching transistor, and (ii) a predetermined voltage line via a third switching transistor.

2. A display apparatus including a current driving light emitting element and a driving transistor, the display apparatus comprising:

   a first switching transistor, provided between (i) a current control terminal of the driving transistor and (ii) a current input terminal of the driving transistor;
   a first capacitor, connected to the current control terminal of the driving transistor; and
   a second capacitor, having a first terminal and a second terminal, the first terminal being connected to the current control terminal of the driving transistor, the second terminal being connected to (i) the current input terminal of the driving transistor via a second switching transistor, and (ii) a predetermined voltage line via a third switching transistor.

3. The display apparatus as set forth in claim 1 or 2, wherein:

   the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in each pixel circuit or each source driver circuit.

4. The display apparatus as set forth in claim 3, wherein:

   each of the source driver circuits includes the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor; and
   each of the pixel circuits includes a transistor for controlling a current that is to be supplied to the current driving light emitting element.

5. The display apparatus as set forth in claim 1 or 2, wherein:

   one or more of the first capacitor, the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in a pixel circuit, and the others are provided in a portion outside the pixel circuit, which portion includes a source driver circuit.

6. The display apparatus as set forth in claim 5,
wherein:

the current driving light emitting element, the driving transistor, and the first capacitor are provided in the pixel circuit; and
the second capacitor, the first switching transistor, the second switching transistor, and the third switching transistor are provided in the portion outside the pixel circuit, which portion includes the source driver circuit,
the display apparatus, further comprising:

a connecting wire for connecting the current control terminal of the driving transistor to the first terminal of the second capacitor.

7. The display apparatus as set forth in claim 6, wherein:

the current driving light emitting element, the driving transistor, and the first capacitor are provided in the pixel circuit;
the second capacitor, the first switching transistor are provided outside the pixel circuit; and
the second switching transistor and the third switching transistor are provided in the source driver,
the display apparatus, further comprising:

a connecting wire for connecting the second terminal of the second capacitor to the second switching transistor and the third switching transistor.

8. The display apparatus as set forth in claim 5,
wherein:

the current driving light emitting element, the driving transistor, the first switching transistor, the first capacitor, and the second capacitor are provided in the pixel circuit;
the second switching transistor and the third switching transistor are provided in the portion outside the pixel circuit, which portion includes the source driver circuit,
the display apparatus, further comprising:

a connecting wire for connecting the second terminal of the second capacitor to (i) the current output terminal of the driving transistor, or (ii) the current input terminal of the driving transistor.

9. The display apparatus as set forth in claim 6 or 8, further comprising:

an OFF potential line for supplying an OFF potential;

wherein:

the connecting wire is connected to the OFF potential line via a fourth switching transistor.

10. A method for driving a display apparatus including a current driving light emitting element and a driving transistor, the method comprising the steps of:

electrically connecting a current control terminal of the driving transistor to a first terminal of a first capacitor;
electrically connecting, during a current writing period of the driving transistor, the first terminal of the first capacitor to a first terminal of a second capacitor;
during a first period, (i) electrically connecting a second terminal of the second capacitor to a predetermined voltage line, and (ii) electrically connecting the current control terminal of the driving transistor to a current output terminal of the driving transistor, and (iii) causing the first capacitor and the second capacitor to retain a current control terminal potential that the driving transistor has on this occasion;
during a second period, (i) correcting the current control terminal potential by disconnecting the current control terminal of the driving transistor from the current output terminal of the driving transistor, and by changing electric connection of the second terminal of the second capacitor from the predetermined voltage line to the current output terminal of the driving transistor, and (ii) causing, during the second period, the first capacitor to retain the current control terminal potential that the driving transistor has on this occasion; and

controlling, during a current readout period of the driving transistor, an output current of the driving transistor with the use of the current control terminal potential, retained by the first capacitor, of the driving transistor.

11. A method for driving a display apparatus including a current driving light emitting element and a driving transistor, the method comprising the steps of:

electrically connecting a current control terminal of the driving transistor to a first terminal of a first capacitor;
electrically connecting, during a current writing period of the driving transistor, the first terminal of the first capacitor to a first terminal of a second capacitor;
during a first period, (i) electrically connecting a second terminal of the second capacitor to a predetermined voltage line, and (ii) electrically connecting the current control terminal of the driving transistor to a current input terminal of the driving transistor, and (iii) causing the first capacitor and the second capacitor to retain a current control terminal potential that the driving transistor has on this occasion;
during a second period, (i) correcting the current control terminal potential by disconnecting the current control terminal of the driving transistor from the current input terminal of the driving transistor, and by changing electric connection of the second terminal of the second capacitor from the predetermined voltage line to the current input terminal of the driving transistor, and (ii) causing the first capacitor to retain the current control terminal potential that the driving transistor has on this occasion; and
controlling, during a current readout period of the driving transistor, an input current of the driving transistor with the use of the current control terminal potential, retained by the first capacitor, of the driving transistor.

12. The driving method as set forth in claim 10 or 11, wherein:

during the second period, the electric connecting of the second terminal of the second capacitor to the current output terminal of the driving transistor is carried out before disconnecting the predetermined voltage line from the second terminal of the second capacitor.

FIG. 1

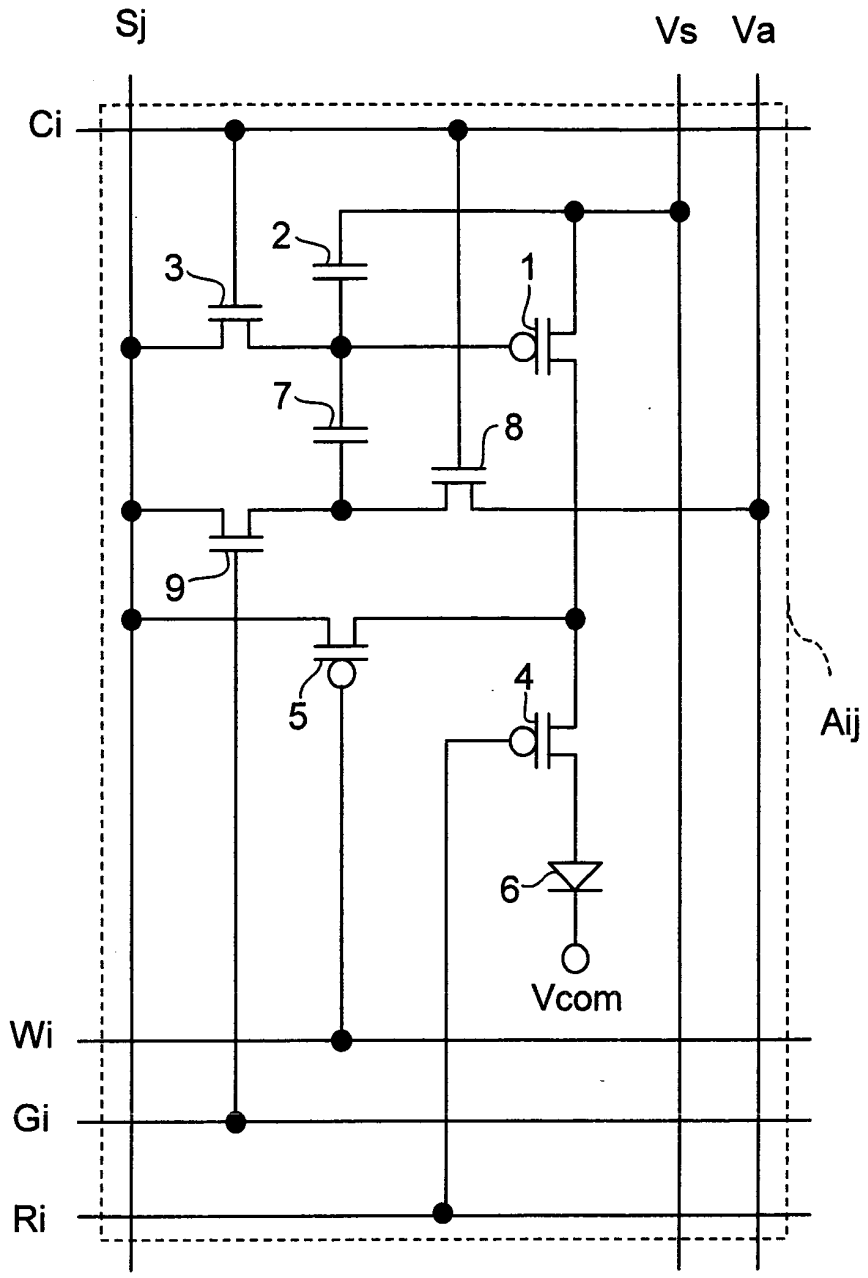


FIG. 2

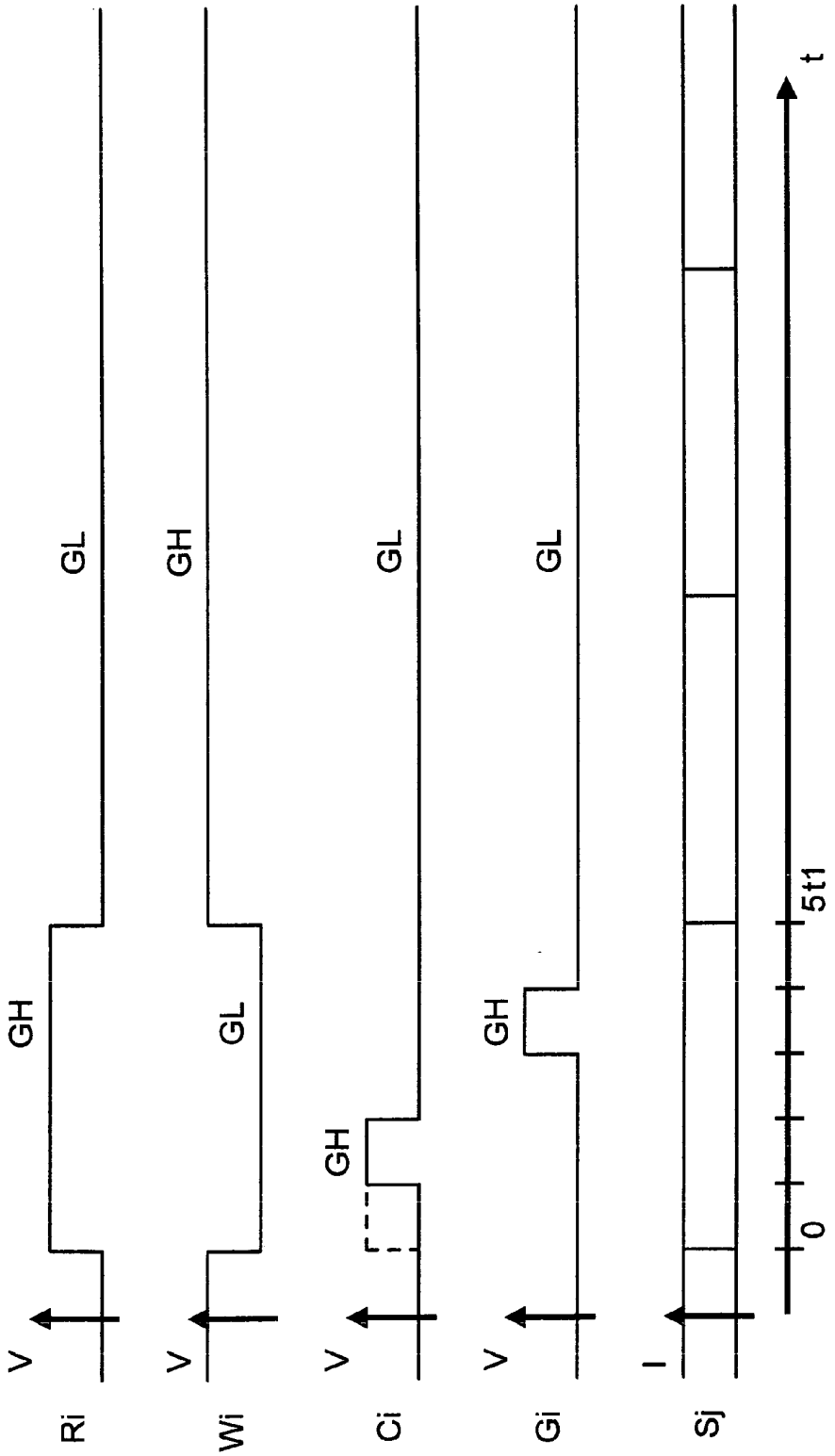


FIG. 3

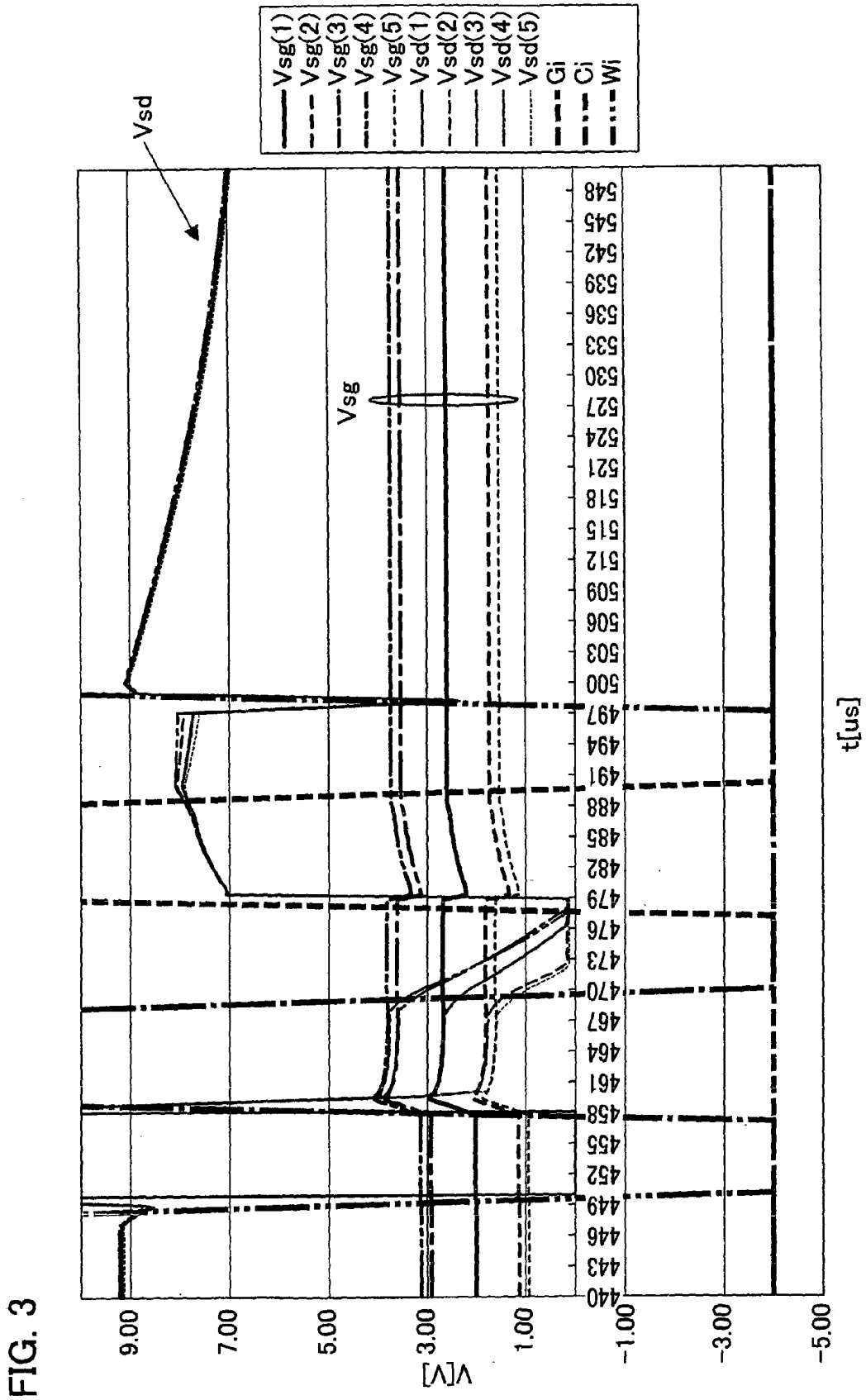

Vsg(1)
Vsg(2)
Vsg(3)
Vsg(4)
Vsg(5)
Vsd(1)
Vsd(2)
Vsd(3)
Vsd(4)
Vsd(5)
Gi
Ci
Wi
Vsd
Vsg
9.00
7.00
5.00
3.00
1.00
-1.00
-3.00
-5.00
V[V]
440
443
446
449
452
455
458
461
464
467
470
473
476
479
482
485
488
491
494
497
500
503
506
509
512
515
518
521
524
527
530
533
536
539
542
545
548
t[us]

FIG. 4

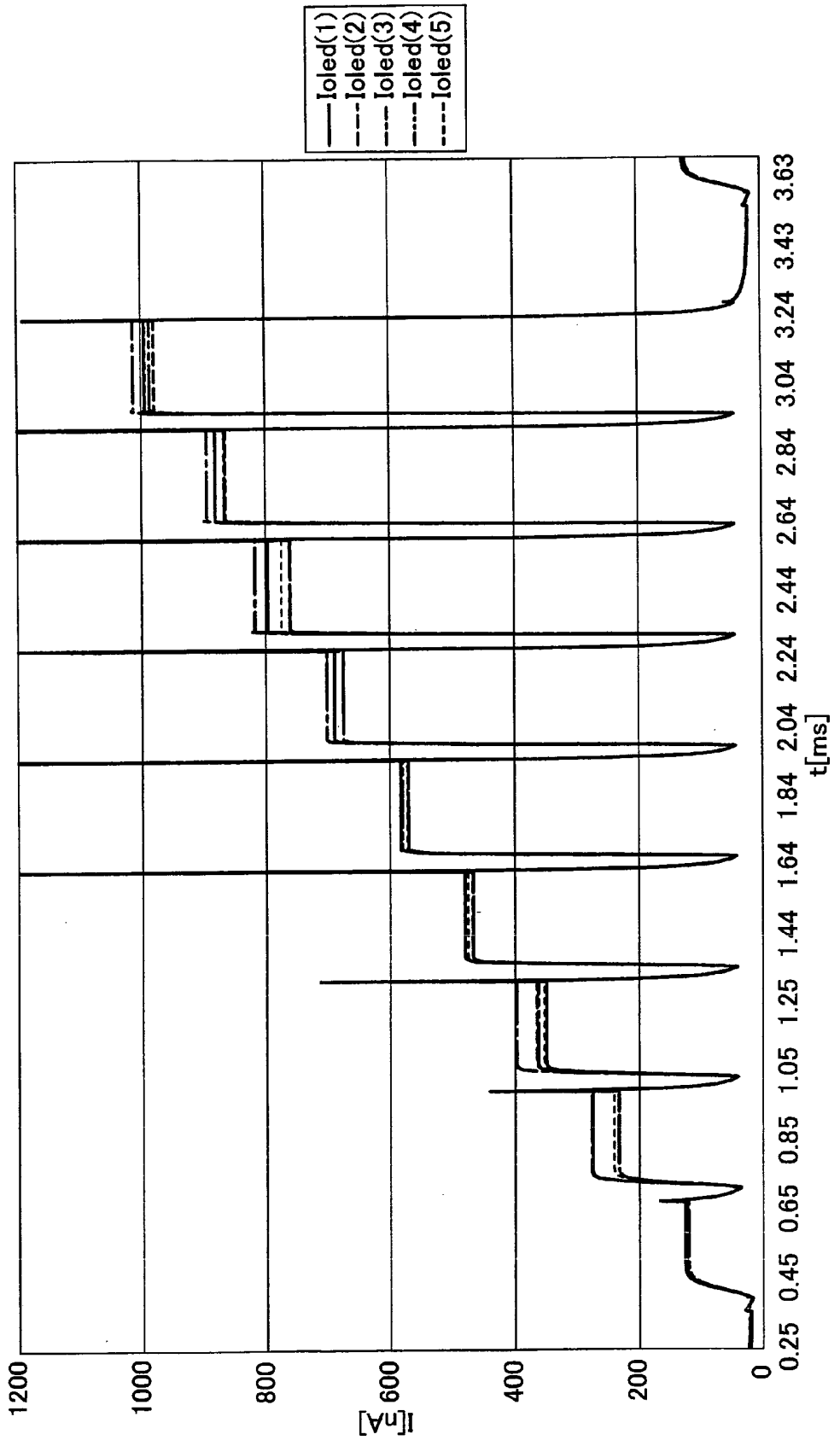

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[nA]
1200
1000
800
600
400
200
0
0.25
0.45
0.65
0.85
1.05
1.25
1.44
1.64
1.84
2.04
2.24
2.44
2.64
2.84
3.04
3.24
3.43
3.63
t[ms]

FIG. 5

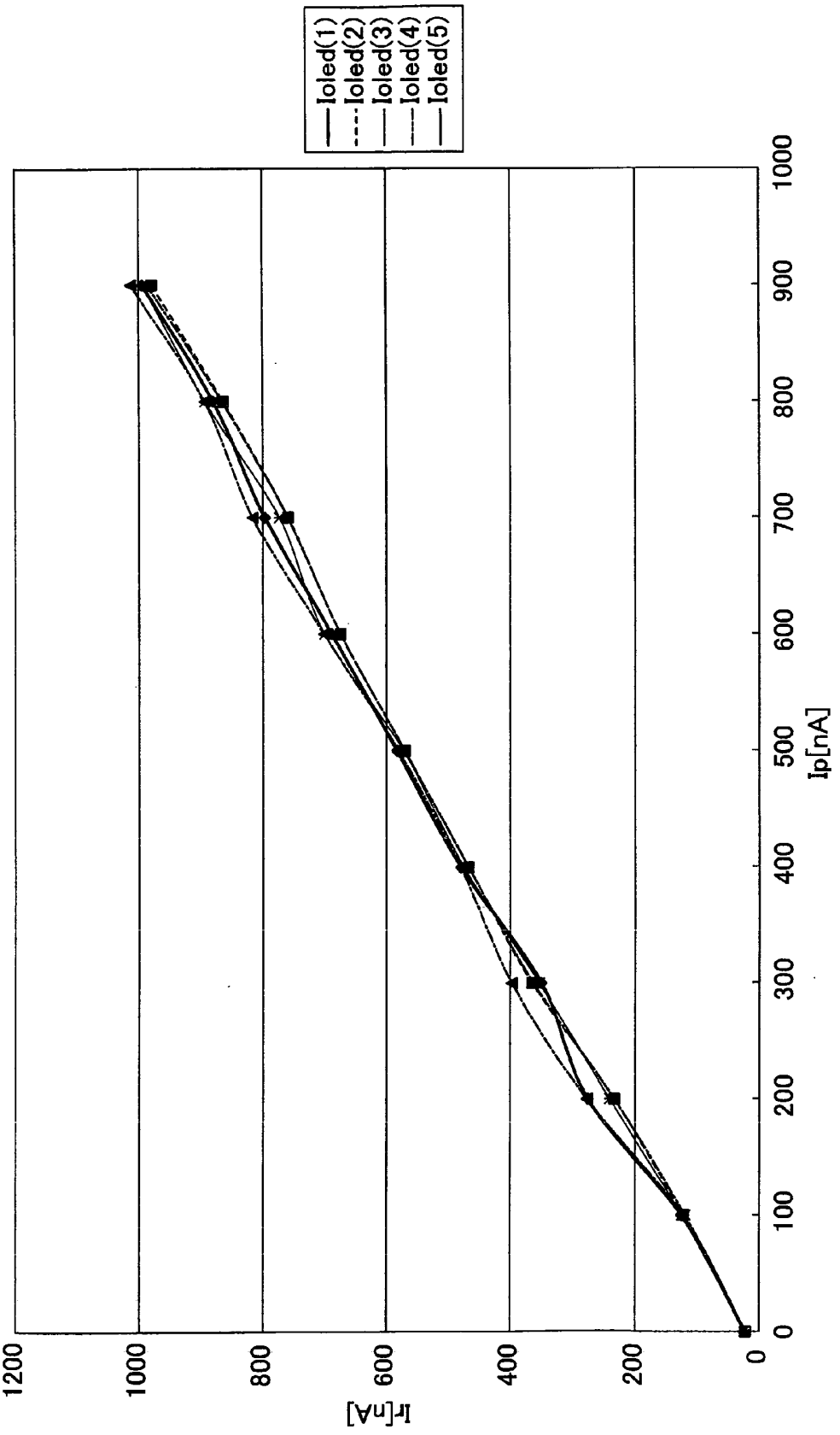

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
Ir[nA]
Ip[nA]
0
200
400
600
800
1000
1200
0
100
200
300
400
500
600
700
800
900
1000

FIG. 6

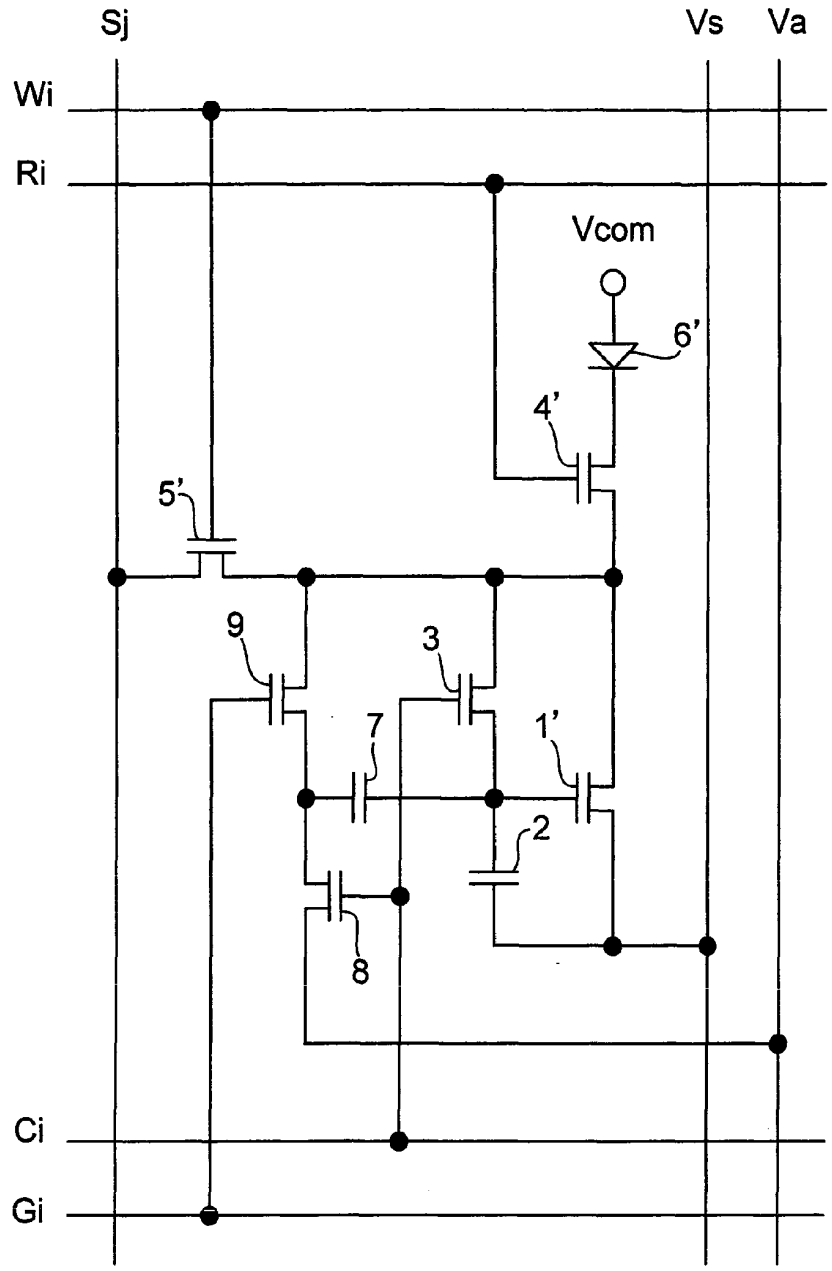


FIG. 7

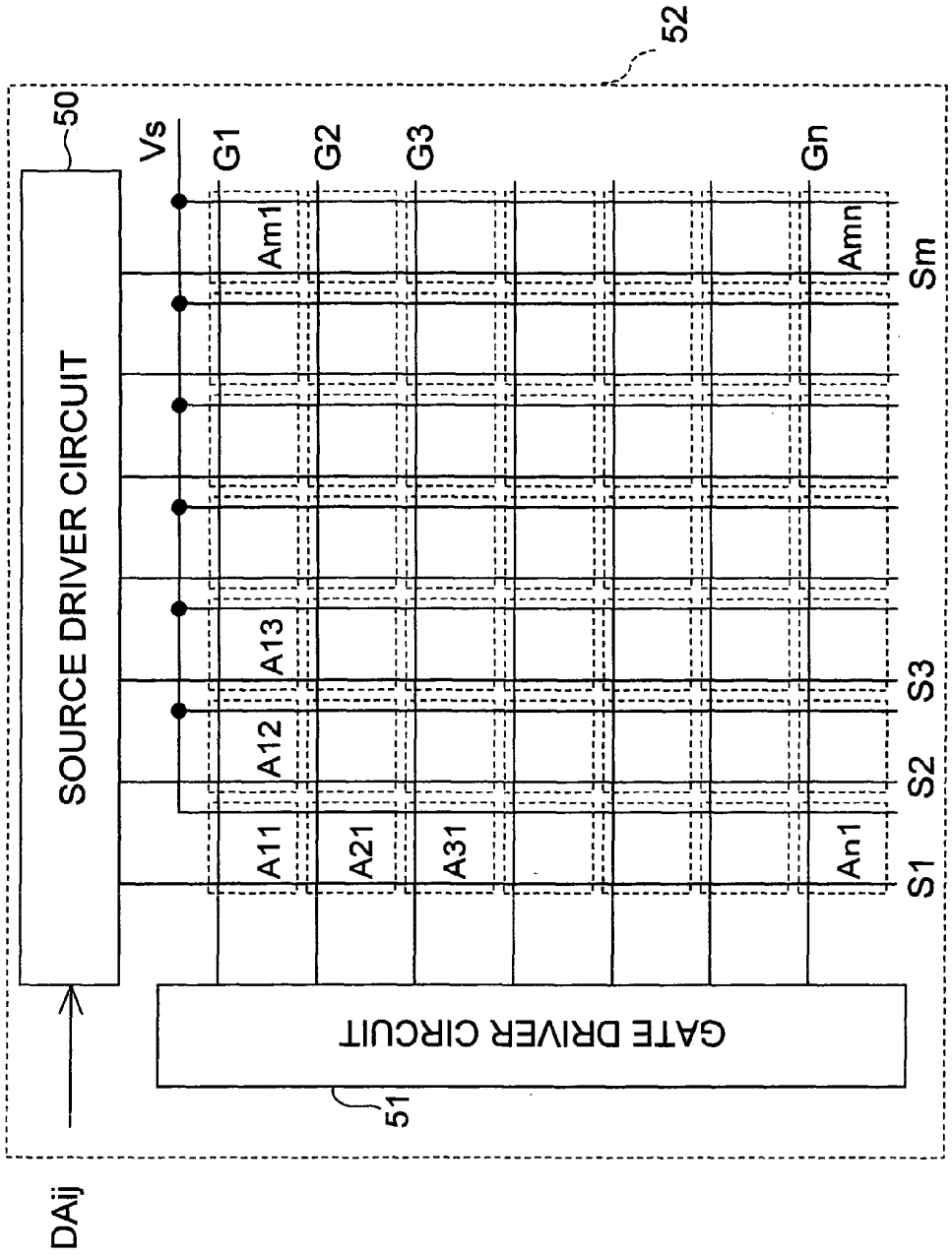
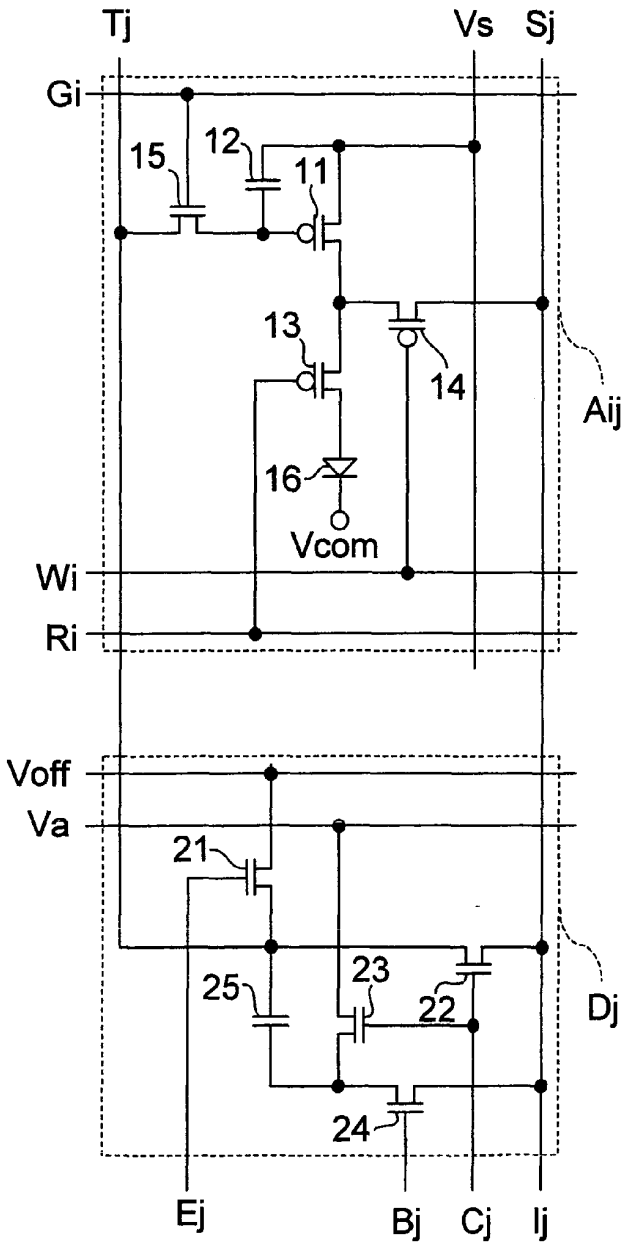

52
50
Vs
G1
G2
G3
Gn
SOURCE DRIVER CIRCUIT
Am1
Amn
Sm
A13
S3
A12
S2
A11
A21
A31
An1
S1
GATE DRIVER CIRCUIT
51
DAij

FIG. 8


Tj
Vs
Sj
Gi
15
12
11
13
14
Aij
16
Vcom
Wi
Ri
Voff
Va
21
25
23
22
Dj
24
Ej
Bj
Cj
Ij

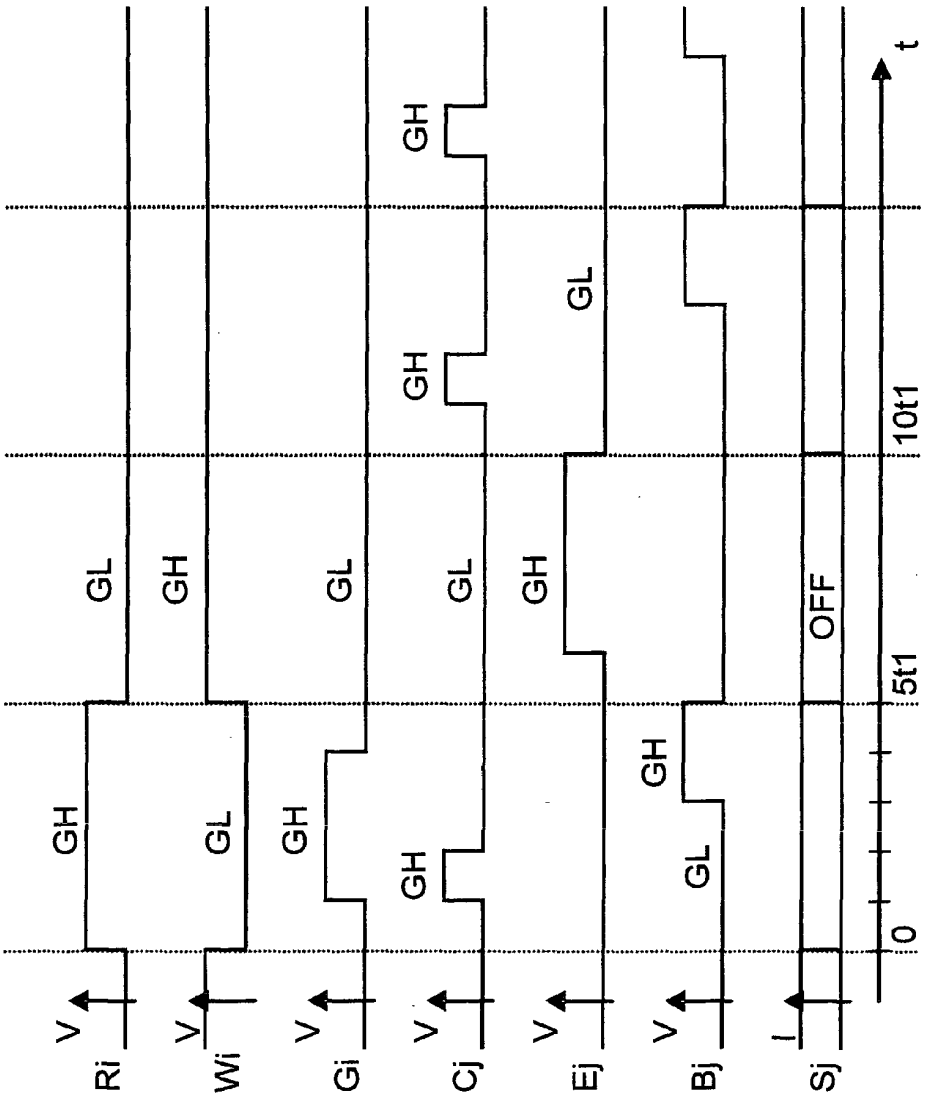

V
Ri
GH
GL
V
Wi
GH
GL
V
Gi
GH
GL
V
Cj
GH
GH
GL
V
Ej
GH
GL
V
Bj
GH
GL
I
Sj
OFF
0
5t1
10t1
t

FIG. 9

FIG. 10

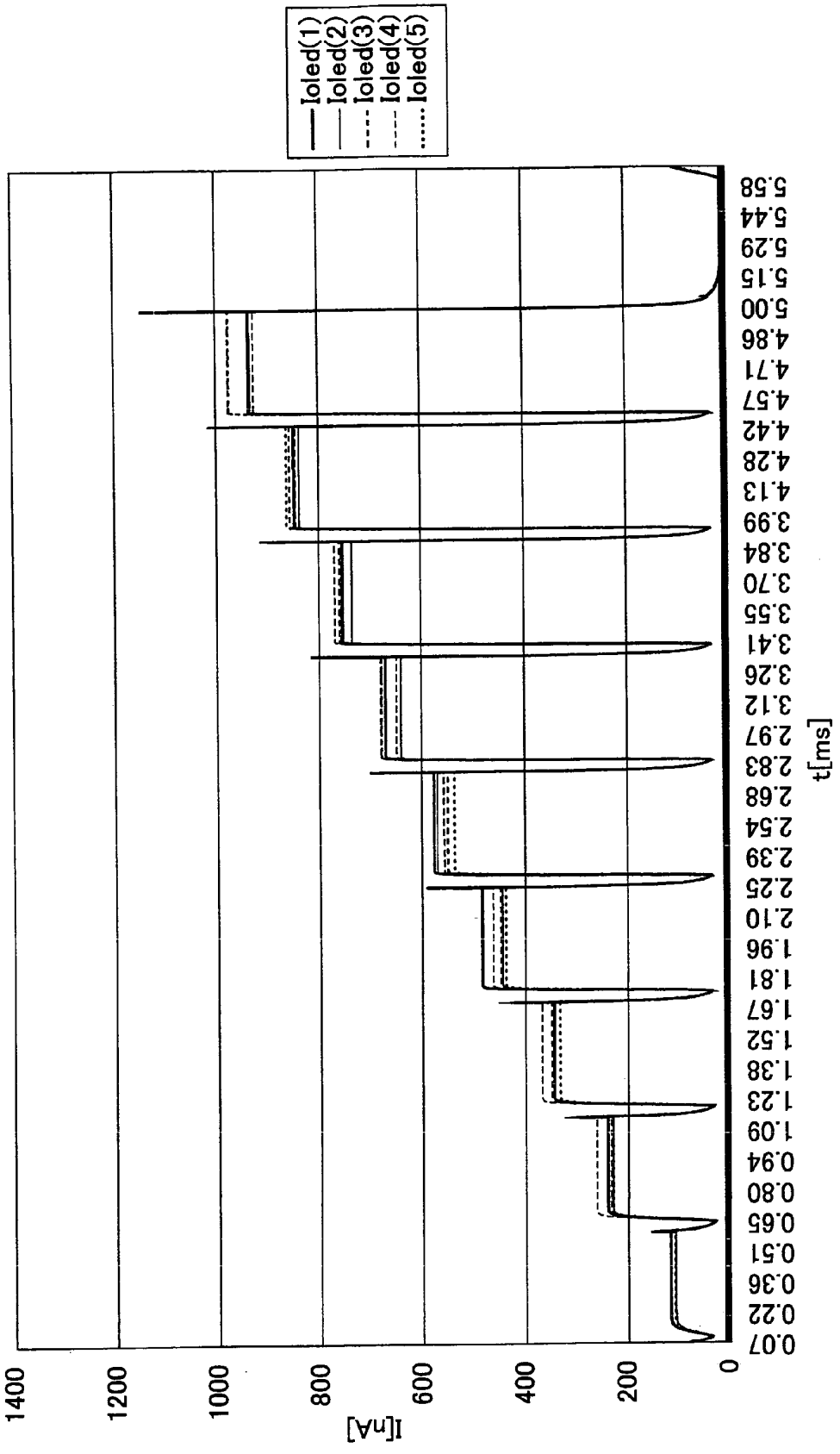

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[nA]
1400
1200
1000
800
600
400
200
0
t[ms]
0.07
0.22
0.36
0.51
0.65
0.80
0.94
1.09
1.23
1.38
1.52
1.67
1.81
1.96
2.10
2.25
2.39
2.54
2.68
2.83
2.97
3.12
3.26
3.41
3.55
3.70
3.84
3.99
4.13
4.28
4.42
4.57
4.71
4.86
5.00
5.15
5.29
5.44
5.58

FIG. 11

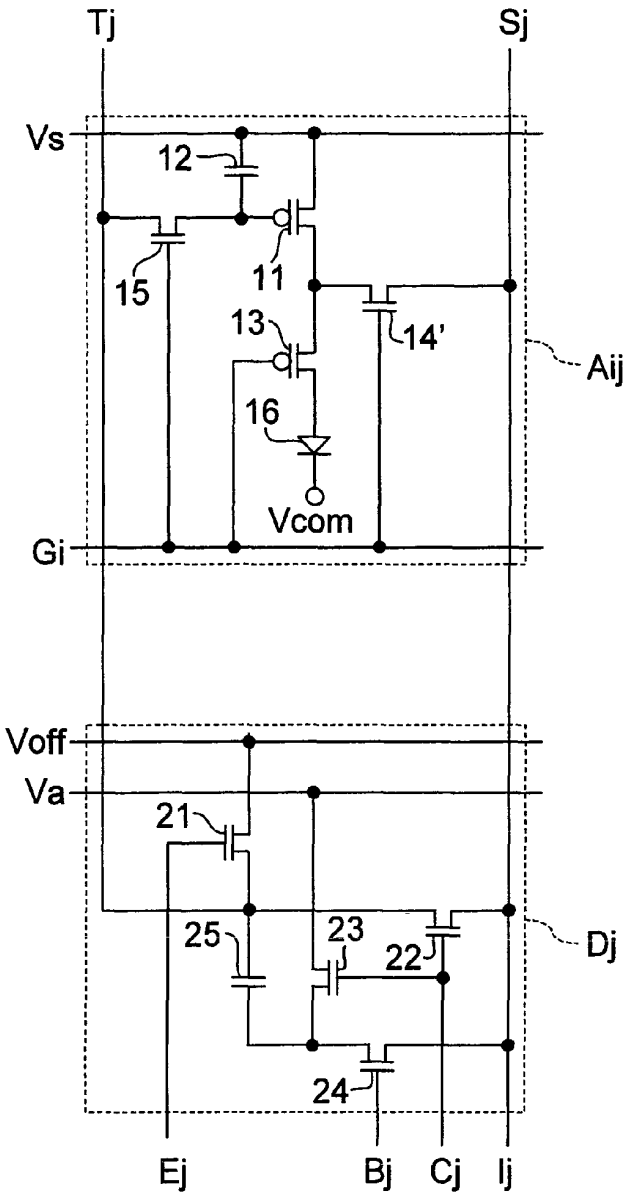

Tj
Sj
Vs
12
15
11
13
14'
Aij
16
Vcom
Gi
Voff
Va
21
25
23
22
Dj
24
Ej
Bj
Cj
Ij

FIG. 12

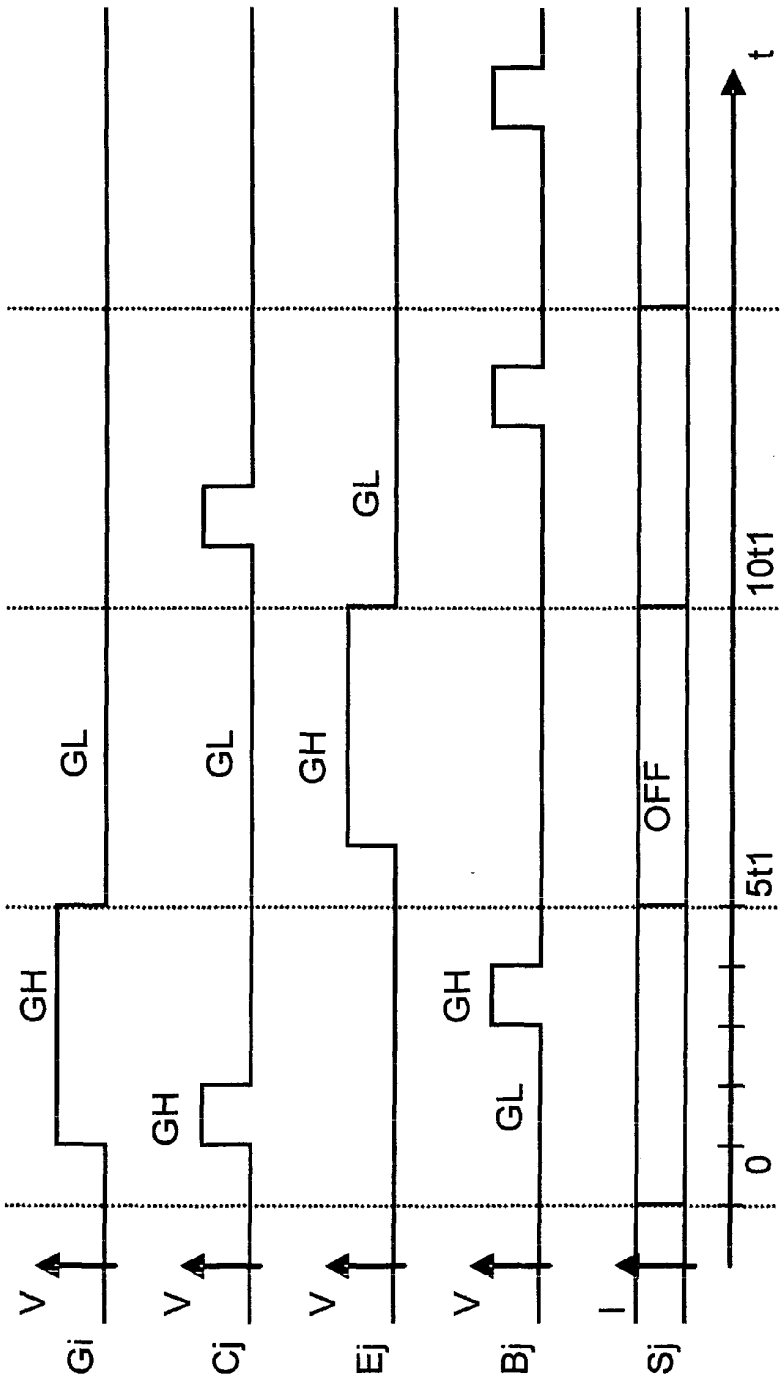


FIG. 13

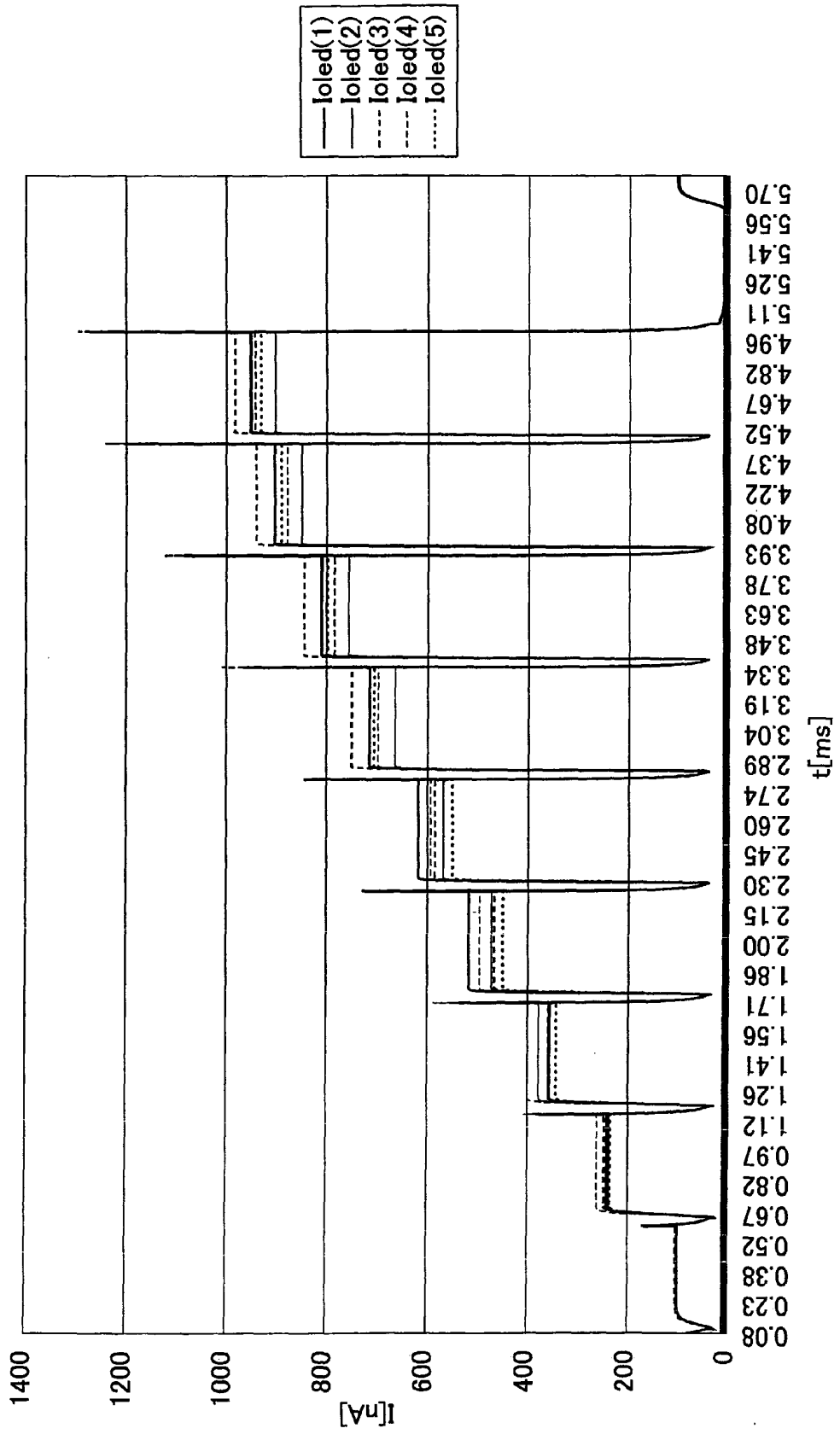

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[nA]
0
200
400
600
800
1000
1200
1400
t[ms]
0.08
0.23
0.38
0.52
0.67
0.82
0.97
1.12
1.26
1.41
1.56
1.71
1.86
2.00
2.15
2.30
2.45
2.60
2.74
2.89
3.04
3.19
3.34
3.48
3.63
3.78
3.93
4.08
4.22
4.37
4.52
4.67
4.82
4.96
5.11
5.26
5.41
5.56
5.70

FIG. 14

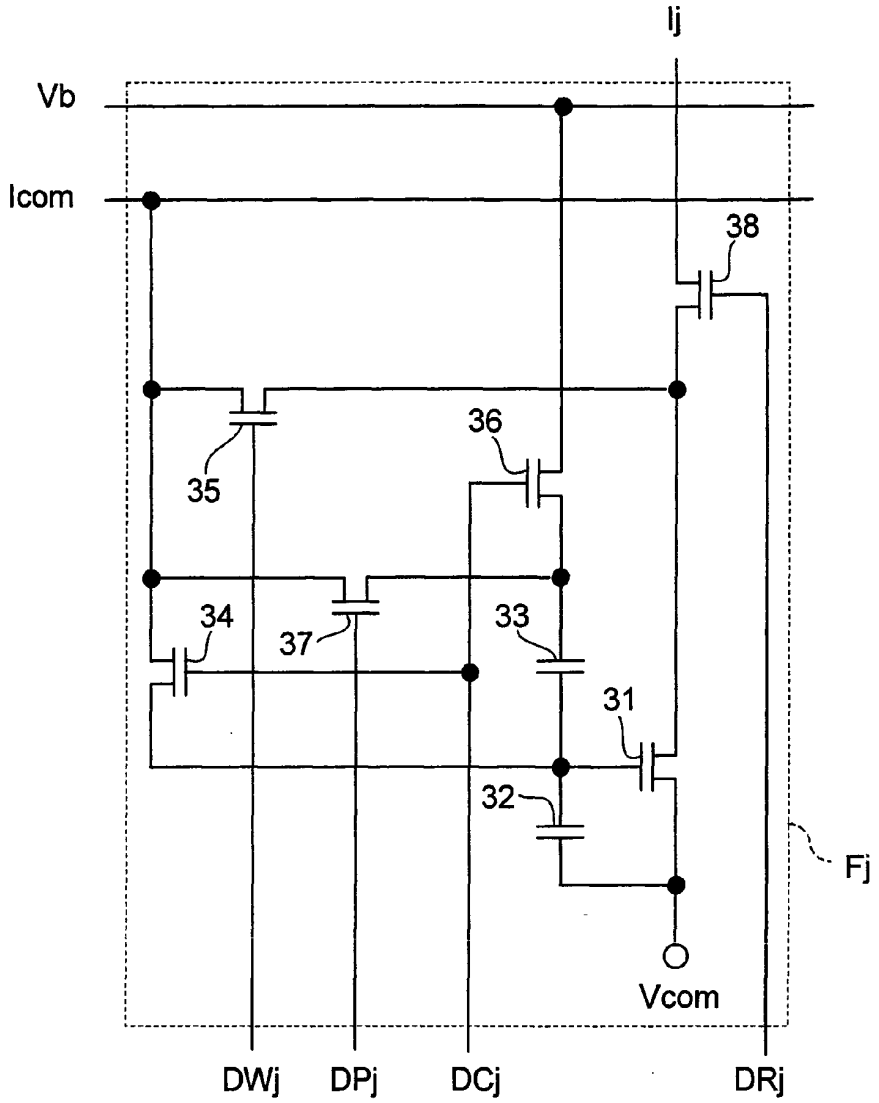


FIG. 15

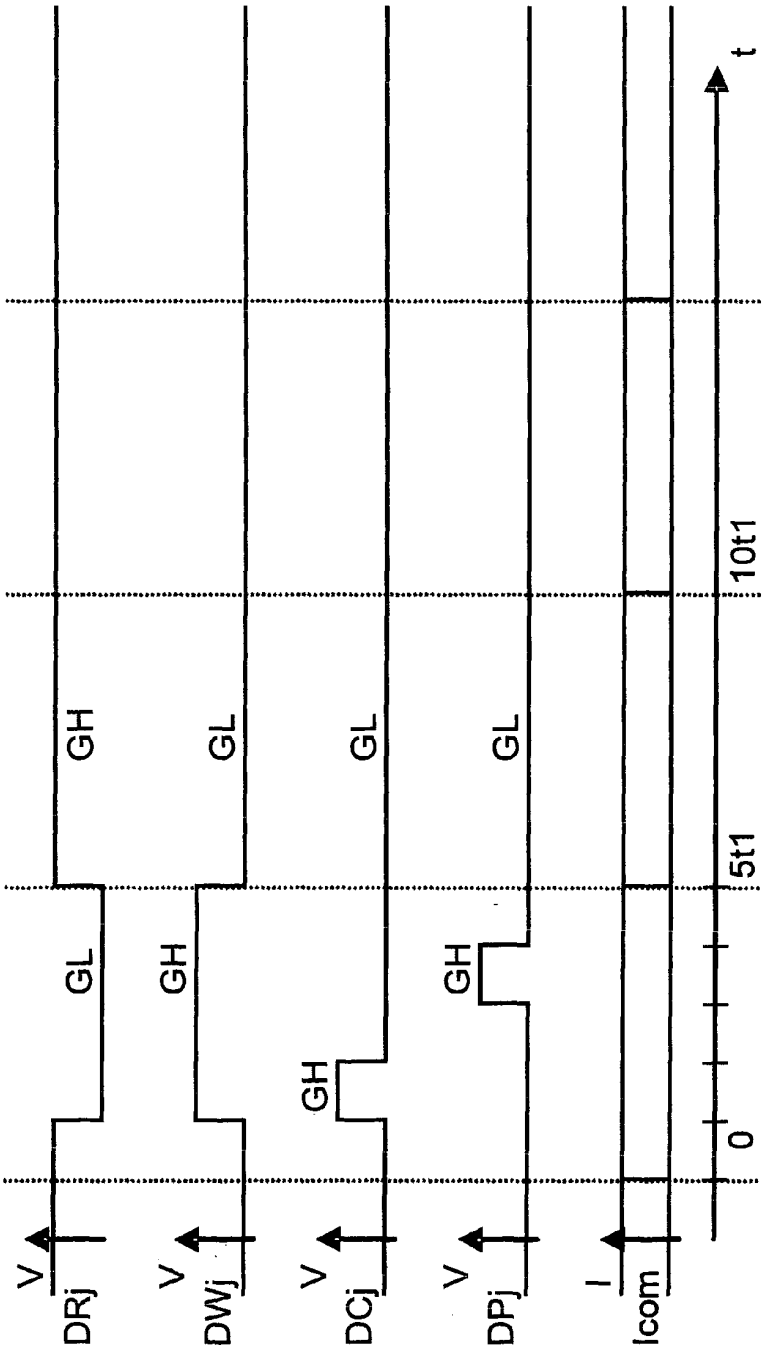


FIG. 16

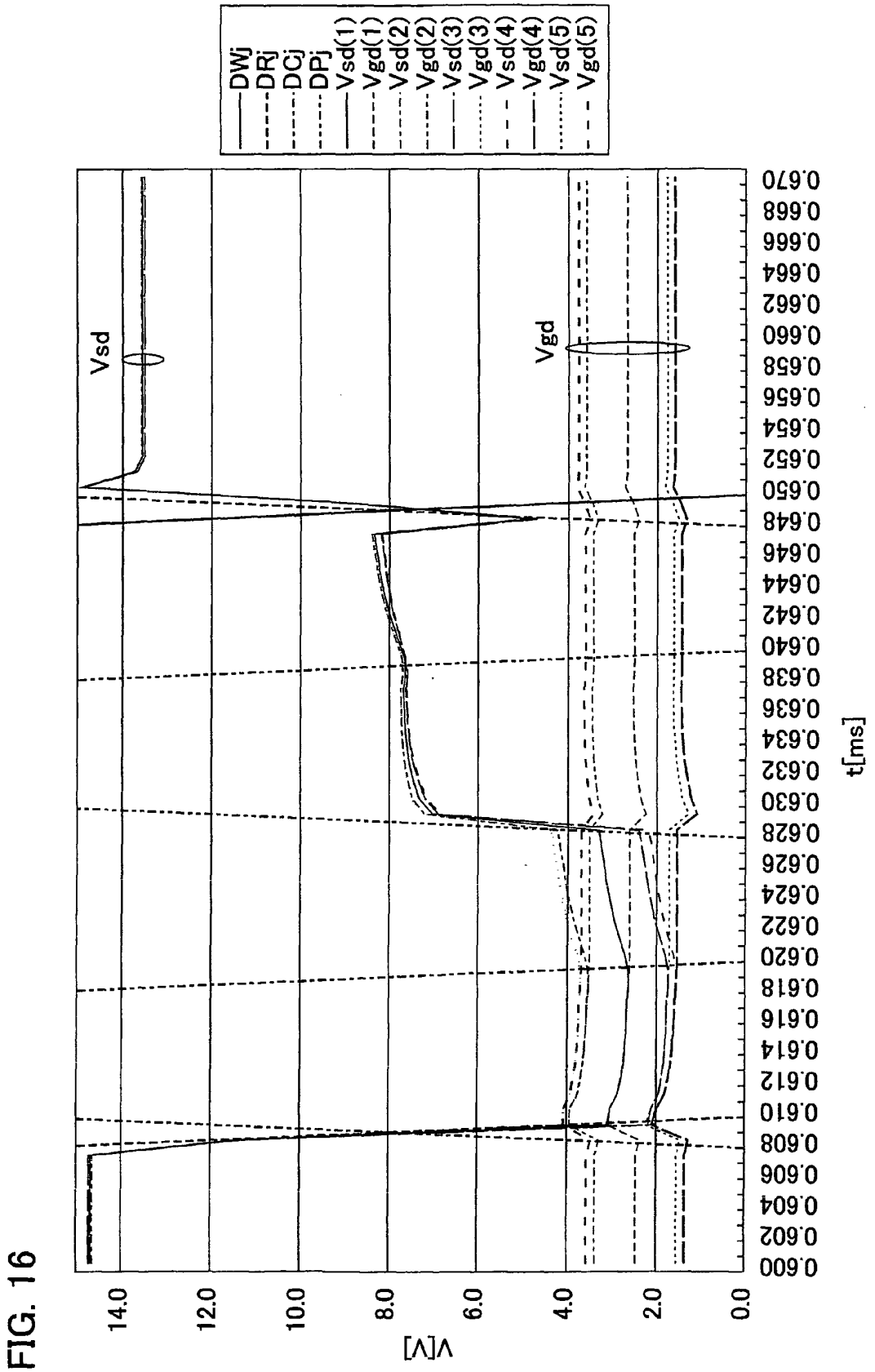

DWj
DRj
DCj
DPj
Vsd(1)
Vgd(1)
Vsd(2)
Vgd(2)
Vsd(3)
Vgd(3)
Vsd(4)
Vgd(4)
Vsd(5)
Vgd(5)
Vsd
Vgd
V[V]
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
t[ms]
0.600
0.602
0.604
0.606
0.608
0.610
0.612
0.614
0.616
0.618
0.620
0.622
0.624
0.626
0.628
0.630
0.632
0.634
0.636
0.638
0.640
0.642
0.644
0.646
0.648
0.650
0.652
0.654
0.656
0.658
0.660
0.662
0.664
0.666
0.668
0.670

FIG. 17

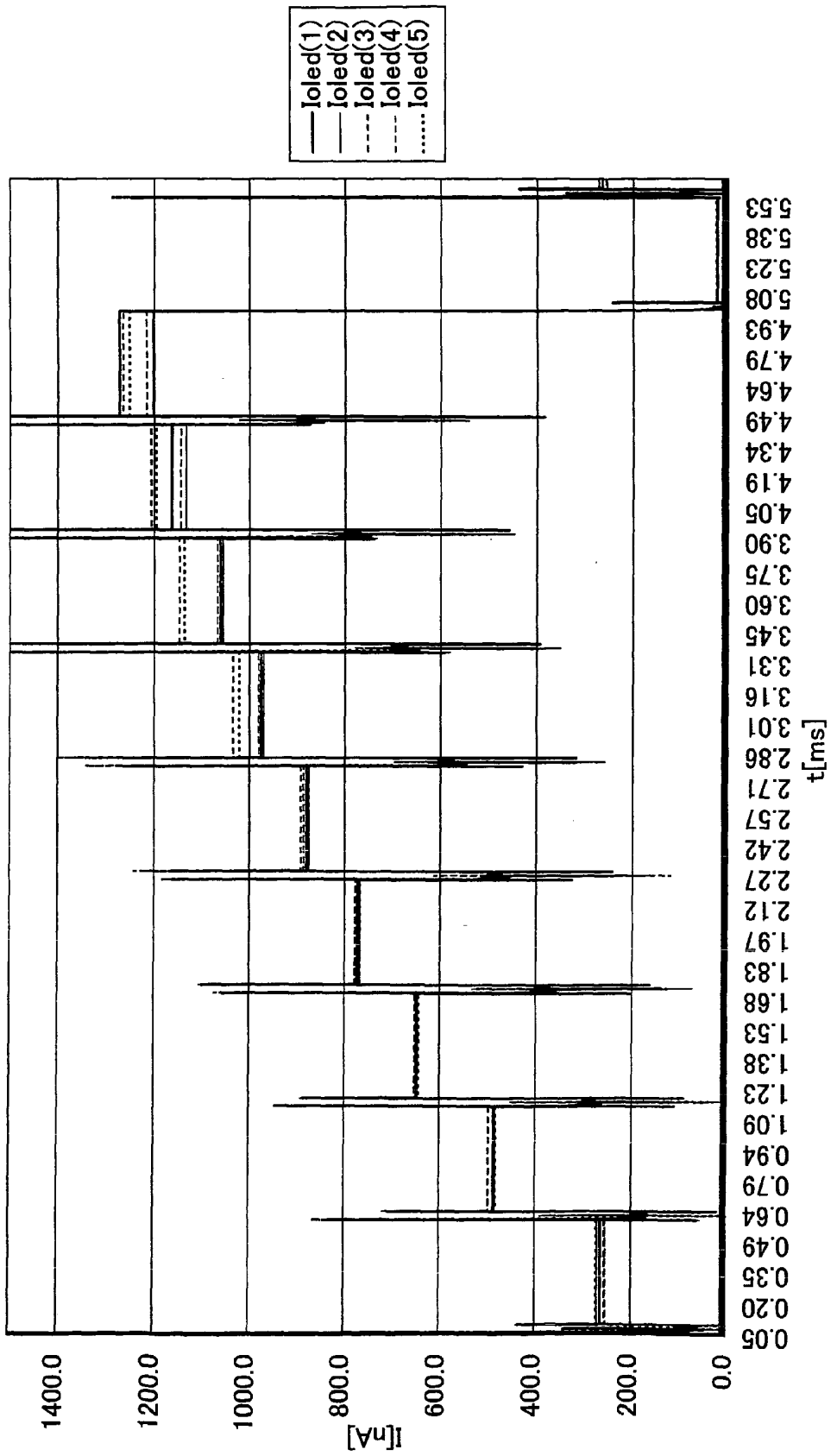

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[nA]
1400.0
1200.0
1000.0
800.0
600.0
400.0
200.0
0.0
t[ms]
0.05
0.20
0.35
0.49
0.64
0.79
0.94
1.09
1.23
1.38
1.53
1.68
1.83
1.97
2.12
2.27
2.42
2.57
2.71
2.86
3.01
3.16
3.31
3.45
3.60
3.75
3.90
4.05
4.19
4.34
4.49
4.64
4.79
4.93
5.08
5.23
5.38
5.53

FIG. 18

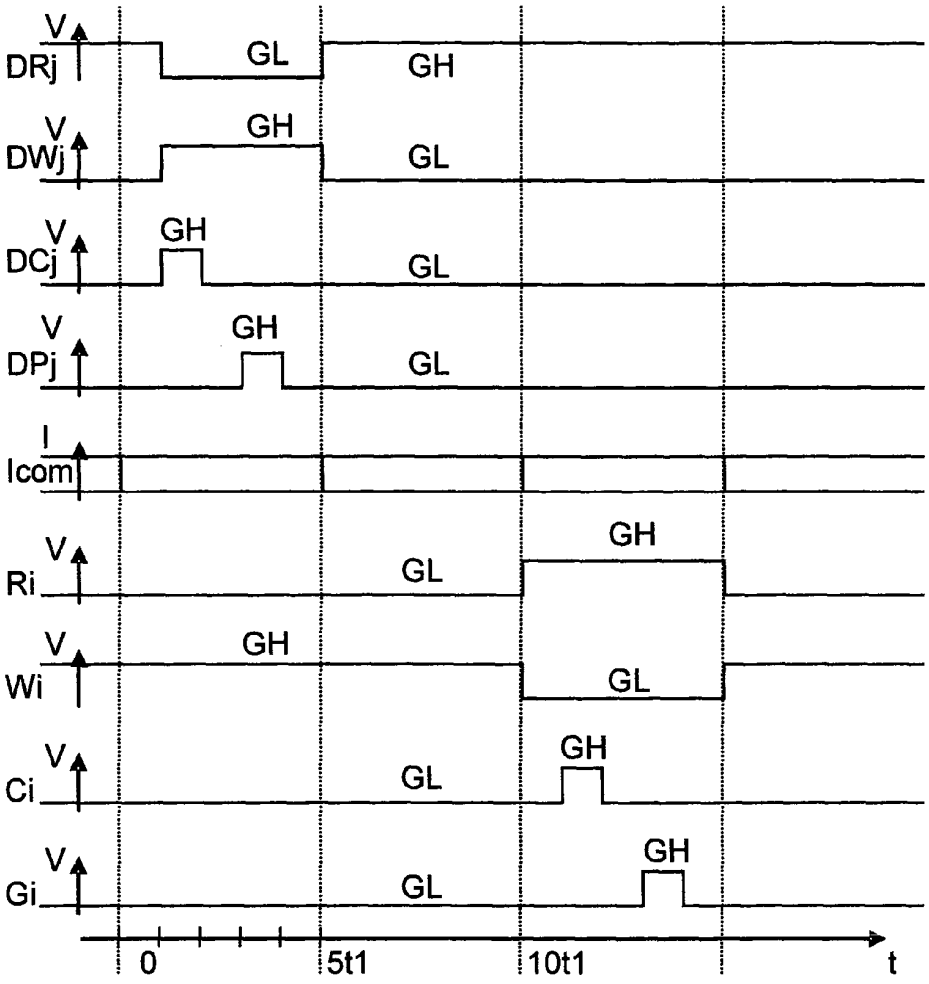

V
DRj
GL
GH
V
DWj
GH
GL
V
DCj
GH
GL
V
DPj
GH
GL
I
Icom
V
Ri
GL
GH
V
Wi
GH
GL
V
Ci
GL
GH
V
Gi
GL
GH
0
5t1
10t1
t

FIG. 19

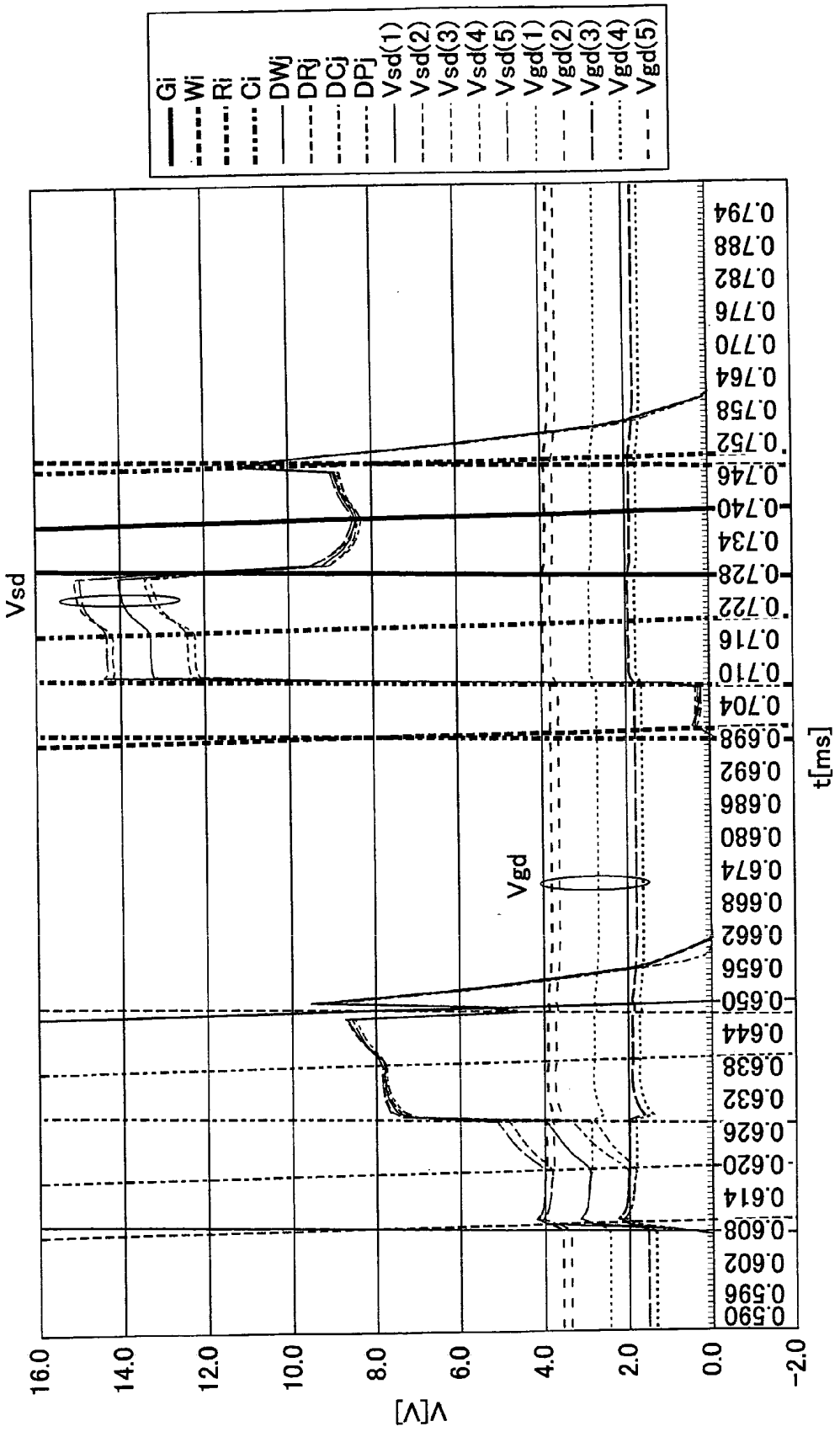

Gi
Wi
Ri
Ci
DWj
DRj
DCj
DPj
Vsd(1)
Vsd(2)
Vsd(3)
Vsd(4)
Vsd(5)
Vgd(1)
Vgd(2)
Vgd(3)
Vgd(4)
Vgd(5)
Vsd
Vgd
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
V[V]
0.590
0.596
0.602
0.608
0.614
0.620
0.626
0.632
0.638
0.644
0.650
0.656
0.662
0.668
0.674
0.680
0.686
0.692
0.698
0.704
0.710
0.716
0.722
0.728
0.734
0.740
0.746
0.752
0.758
0.764
0.770
0.776
0.782
0.788
0.794
t[ms]

FIG. 20

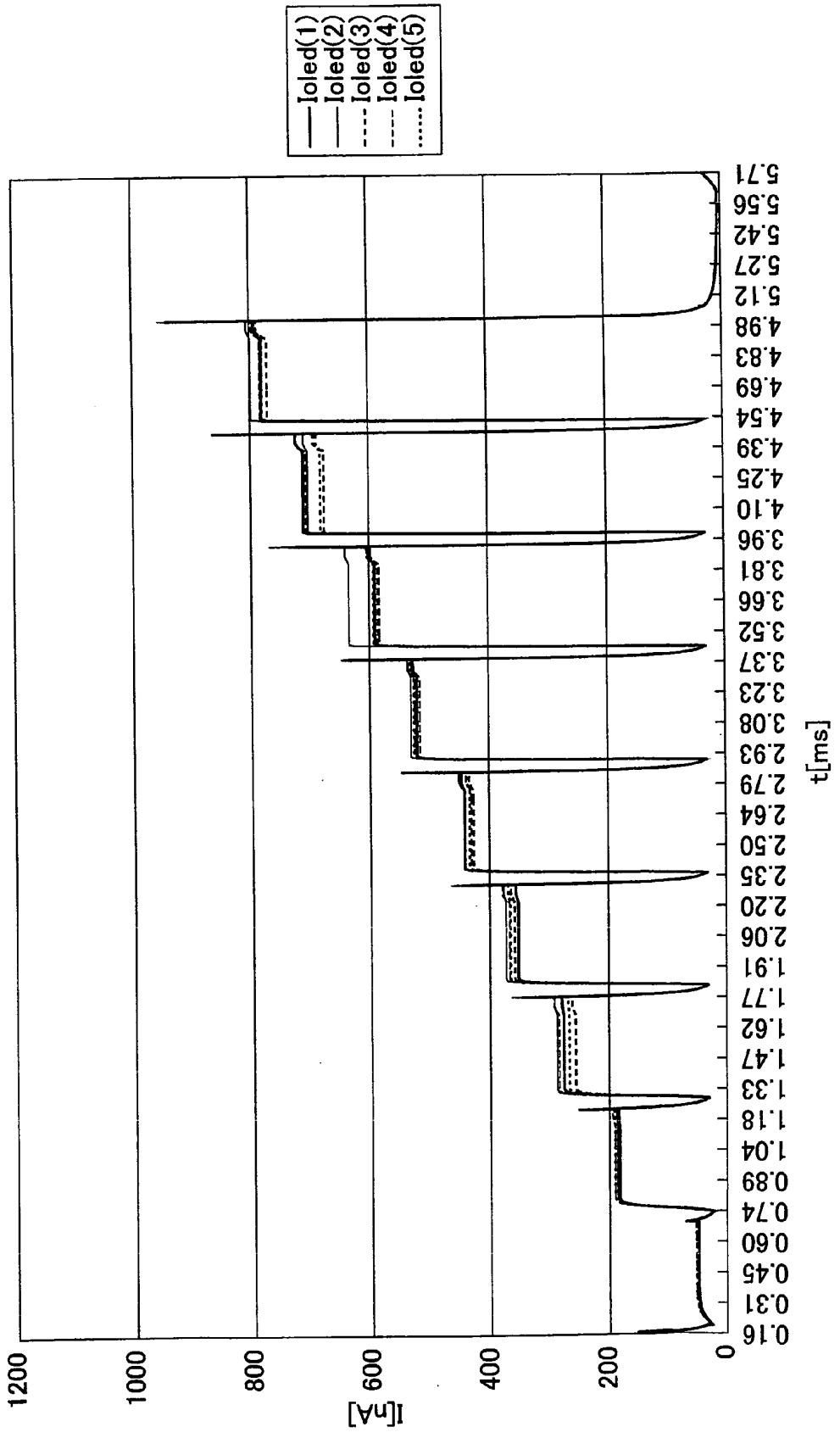

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[nA]
1200
1000
800
600
400
200
0
t[ms]
0.16
0.31
0.45
0.60
0.74
0.89
1.04
1.18
1.33
1.47
1.62
1.77
1.91
2.06
2.20
2.35
2.50
2.64
2.79
2.93
3.08
3.23
3.37
3.52
3.66
3.81
3.96
4.10
4.25
4.39
4.54
4.69
4.83
4.98
5.12
5.27
5.42
5.56
5.71

FIG. 21

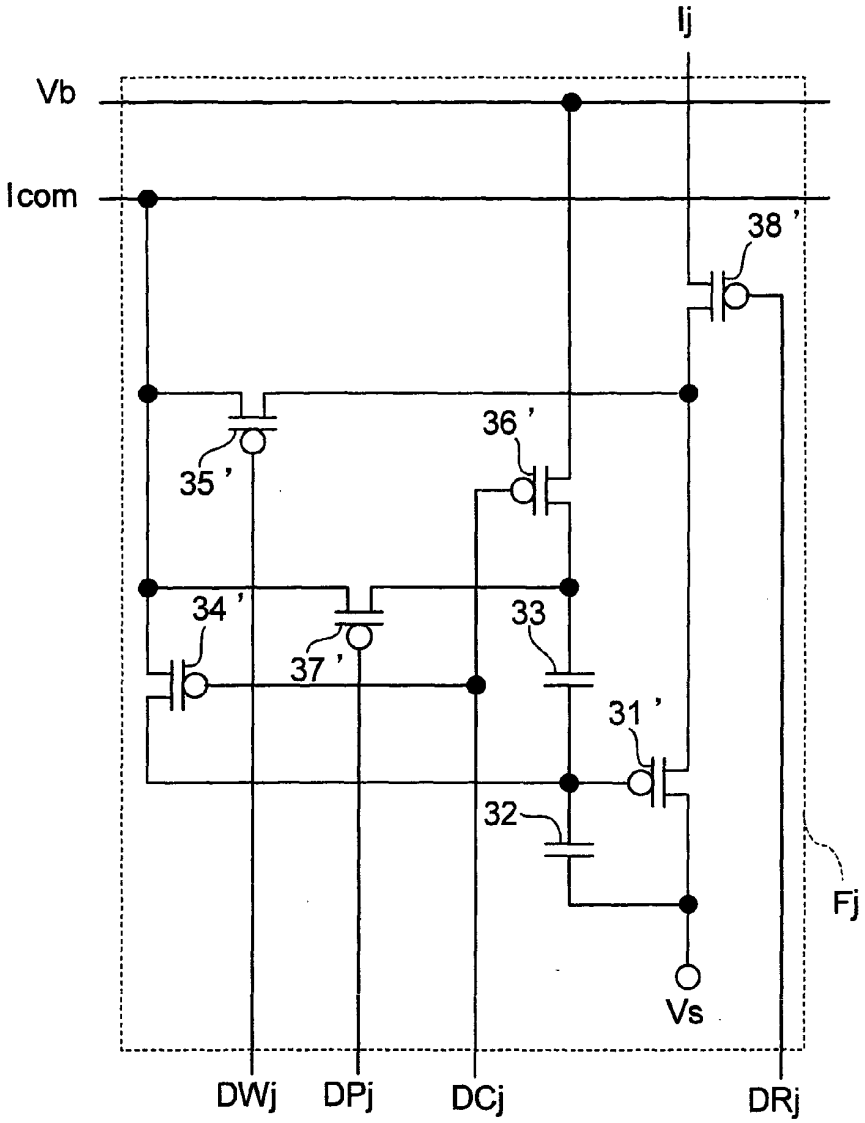


FIG. 22

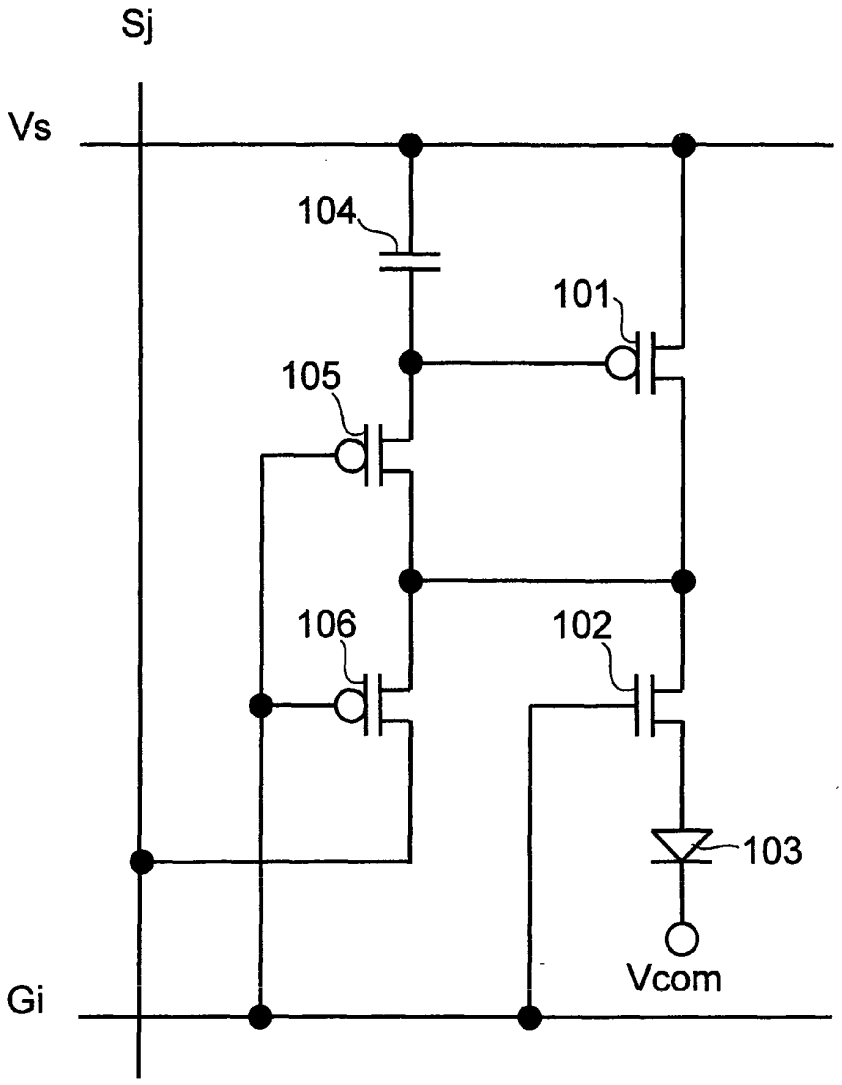
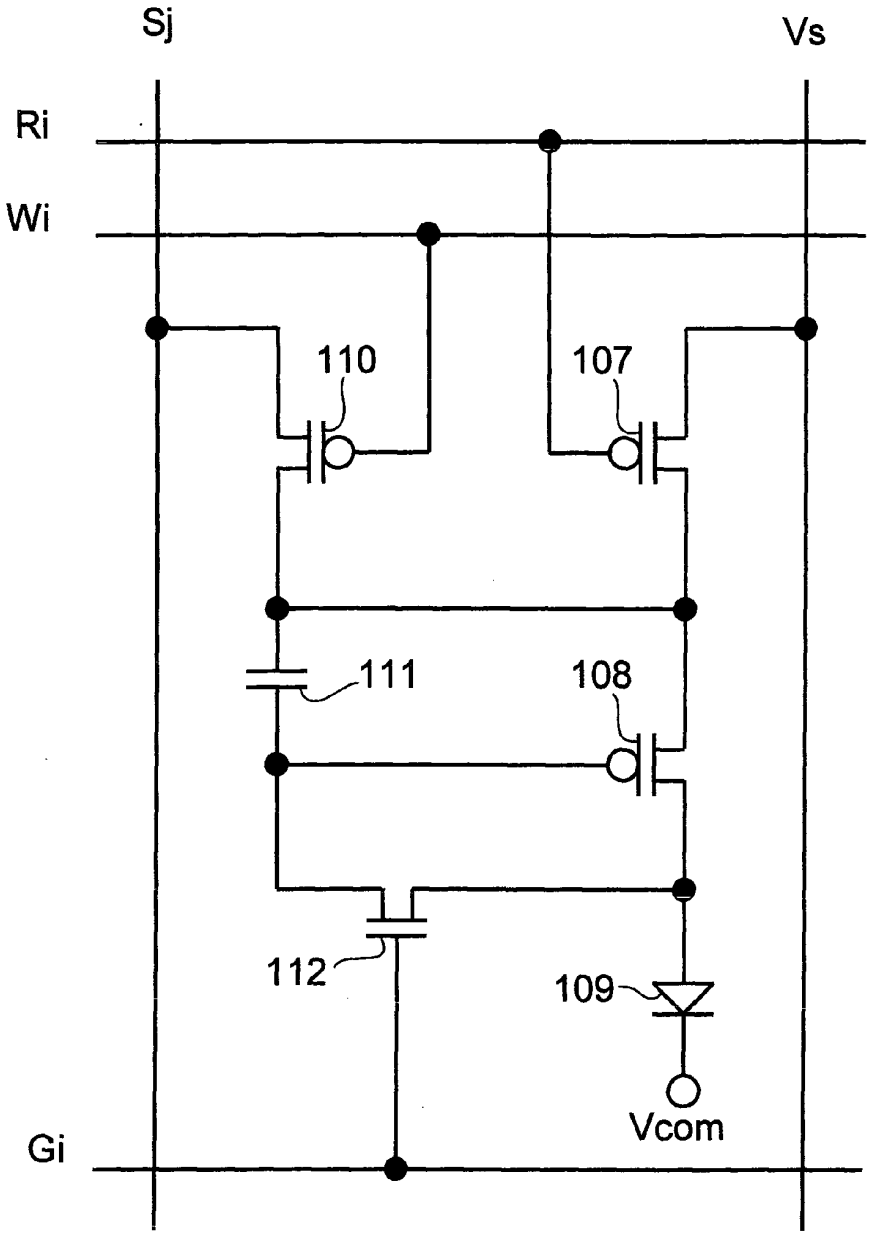


FIG. 23



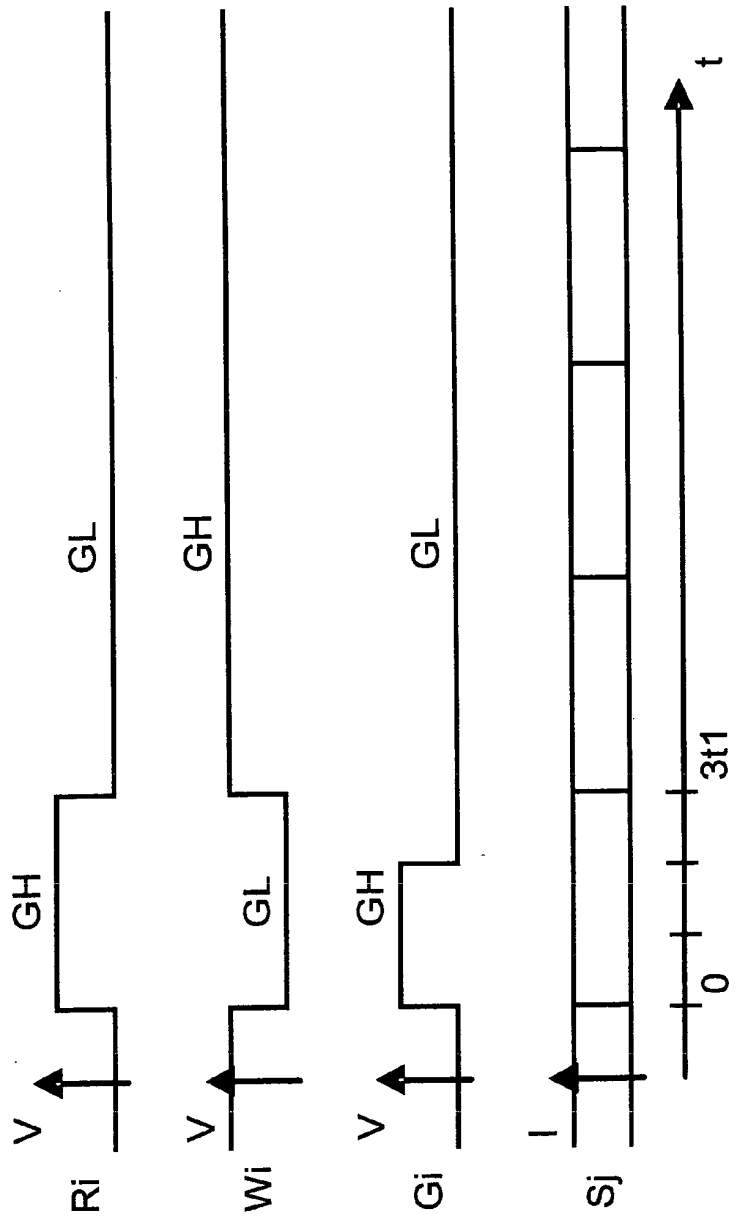


FIG. 24

FIG. 25

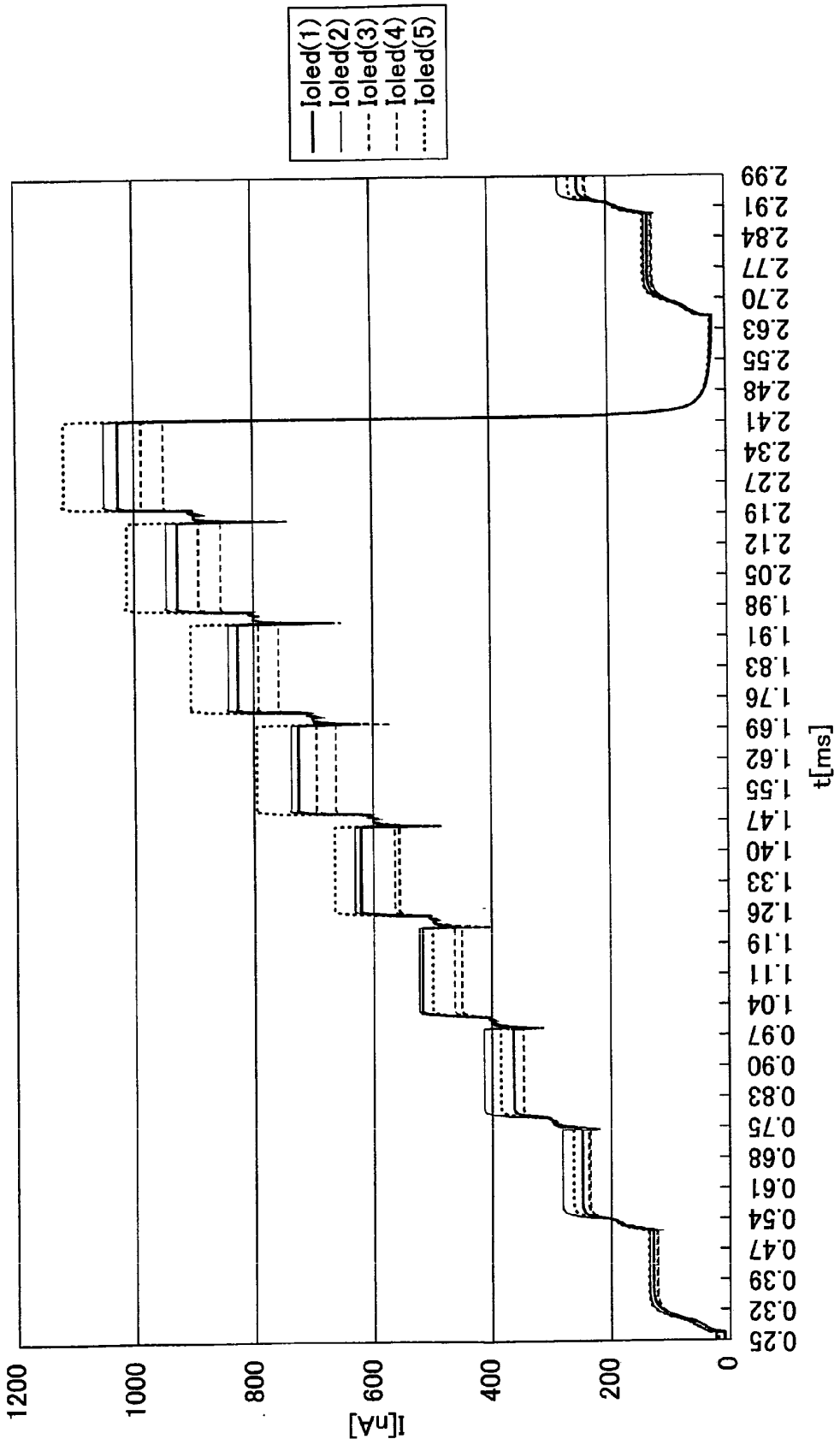

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[nA]
1200
1000
800
600
400
200
0
t[ms]
0.25
0.32
0.39
0.47
0.54
0.61
0.68
0.75
0.83
0.90
0.97
1.04
1.11
1.19
1.26
1.33
1.40
1.47
1.55
1.62
1.69
1.76
1.83
1.91
1.98
2.05
2.12
2.19
2.27
2.34
2.41
2.48
2.55
2.63
2.70
2.77
2.84
2.91
2.99

FIG. 26

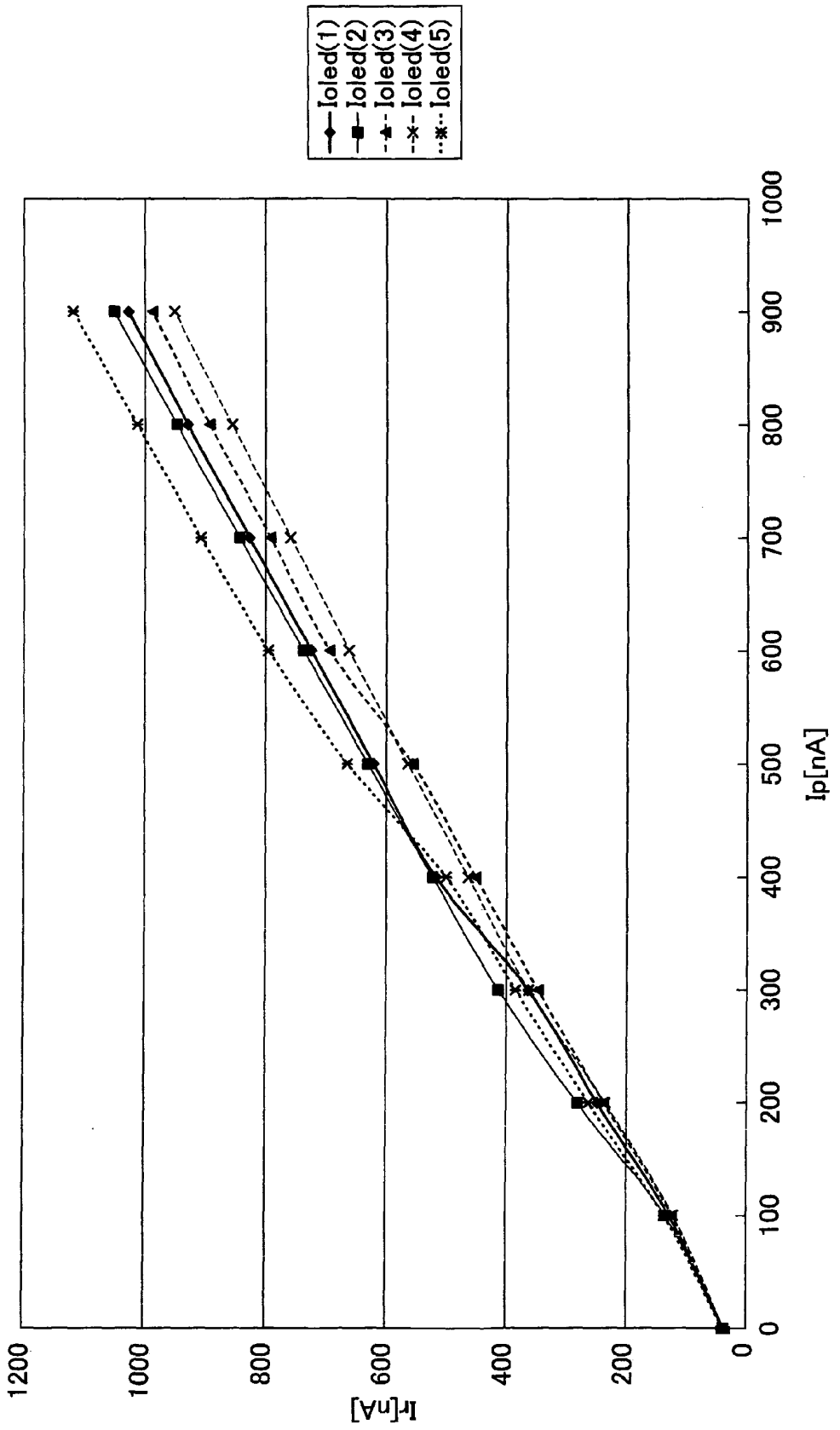

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
Ir[nA]
Ip[nA]
0
200
400
600
800
1000
1200
0
100
200
300
400
500
600
700
800
900
1000

FIG. 27

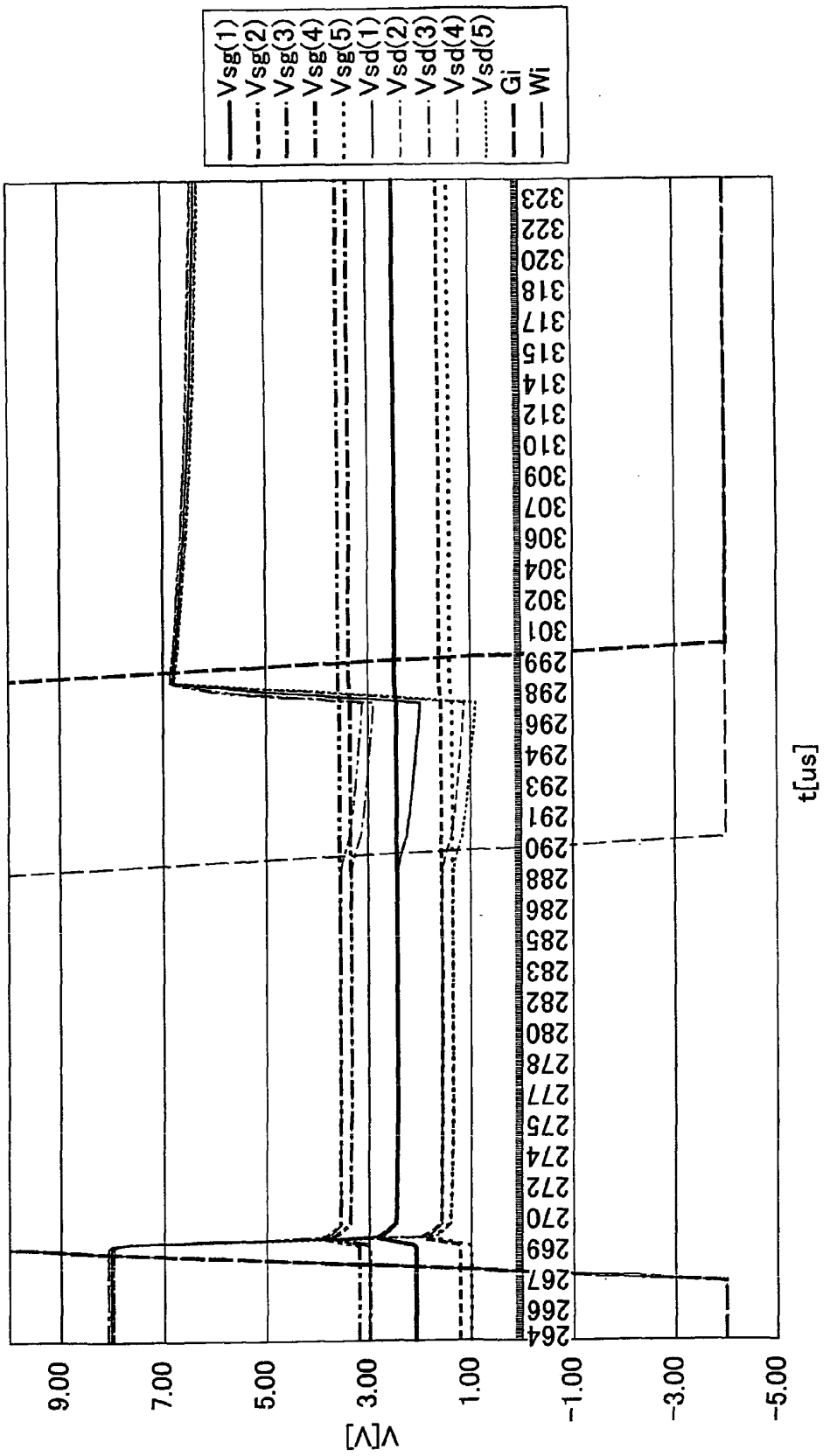

Vsg(1)
Vsg(2)
Vsg(3)
Vsg(4)
Vsg(5)
Vsd(1)
Vsd(2)
Vsd(3)
Vsd(4)
Vsd(5)
Gi
Wi
9.00
7.00
5.00
3.00
1.00
-1.00
-3.00
-5.00
V[V]
264
266
267
269
270
272
274
275
277
278
280
282
283
285
286
288
290
291
293
294
296
298
299
301
302
304
306
307
309
310
312
314
315
317
318
320
322
323
t[us]

FIG. 28

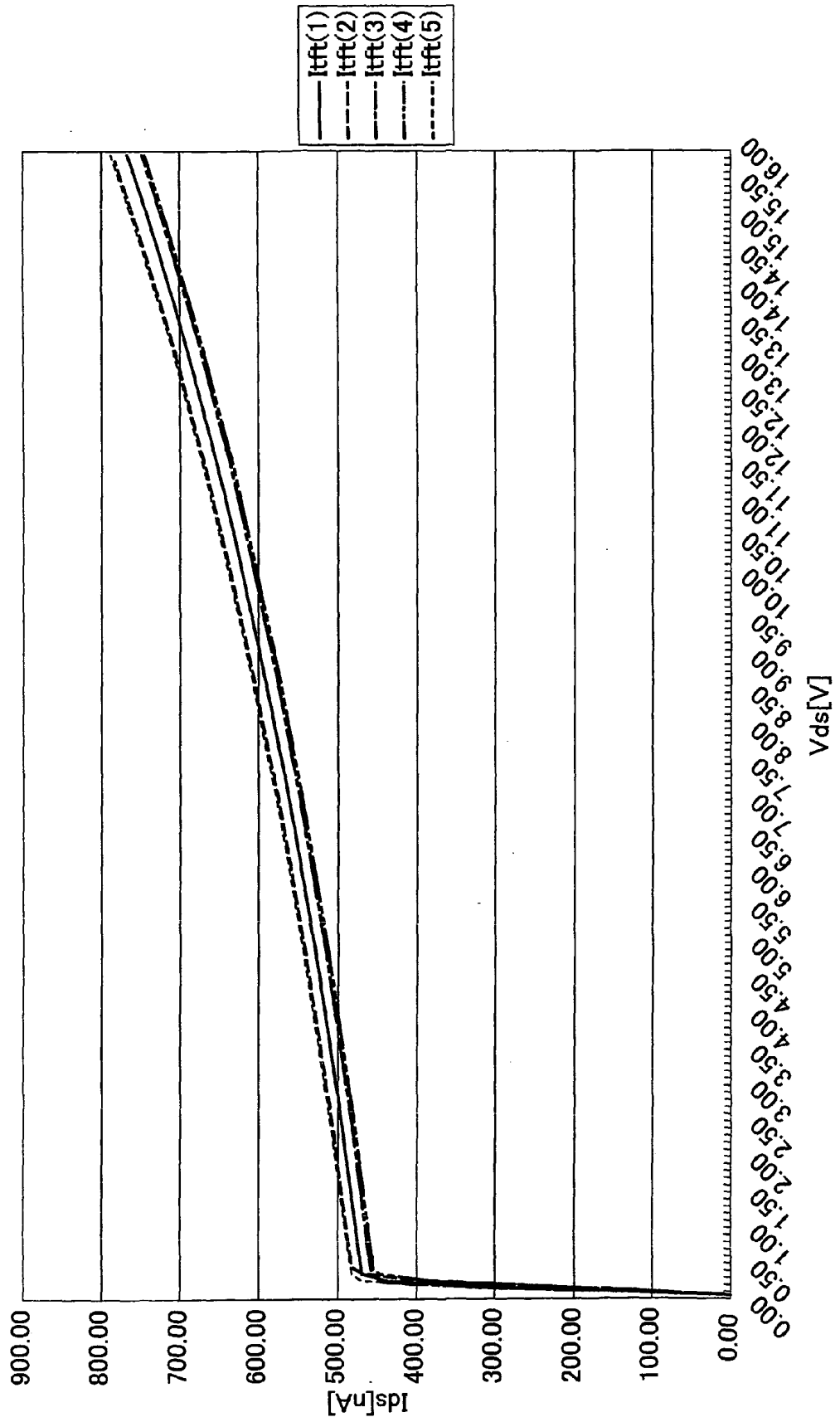

Itft(1)
Itft(2)
Itft(3)
Itft(4)
Itft(5)
Ids[nA]
900.00
800.00
700.00
600.00
500.00
400.00
300.00
200.00
100.00
0.00
Vds[V]
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50
8.00
8.50
9.00
9.50
10.00
10.50
11.00
11.50
12.00
12.50
13.00
13.50
14.00
14.50
15.00
15.50
16.00

FIG. 29

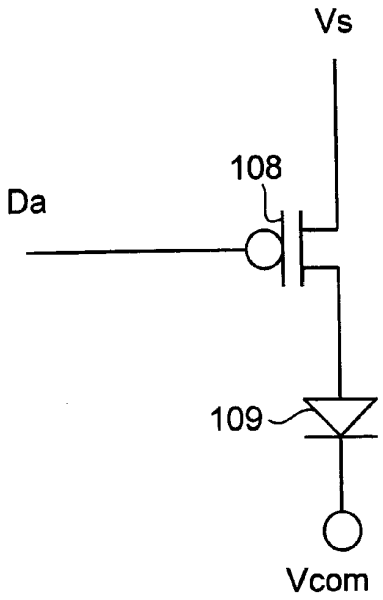


FIG. 30

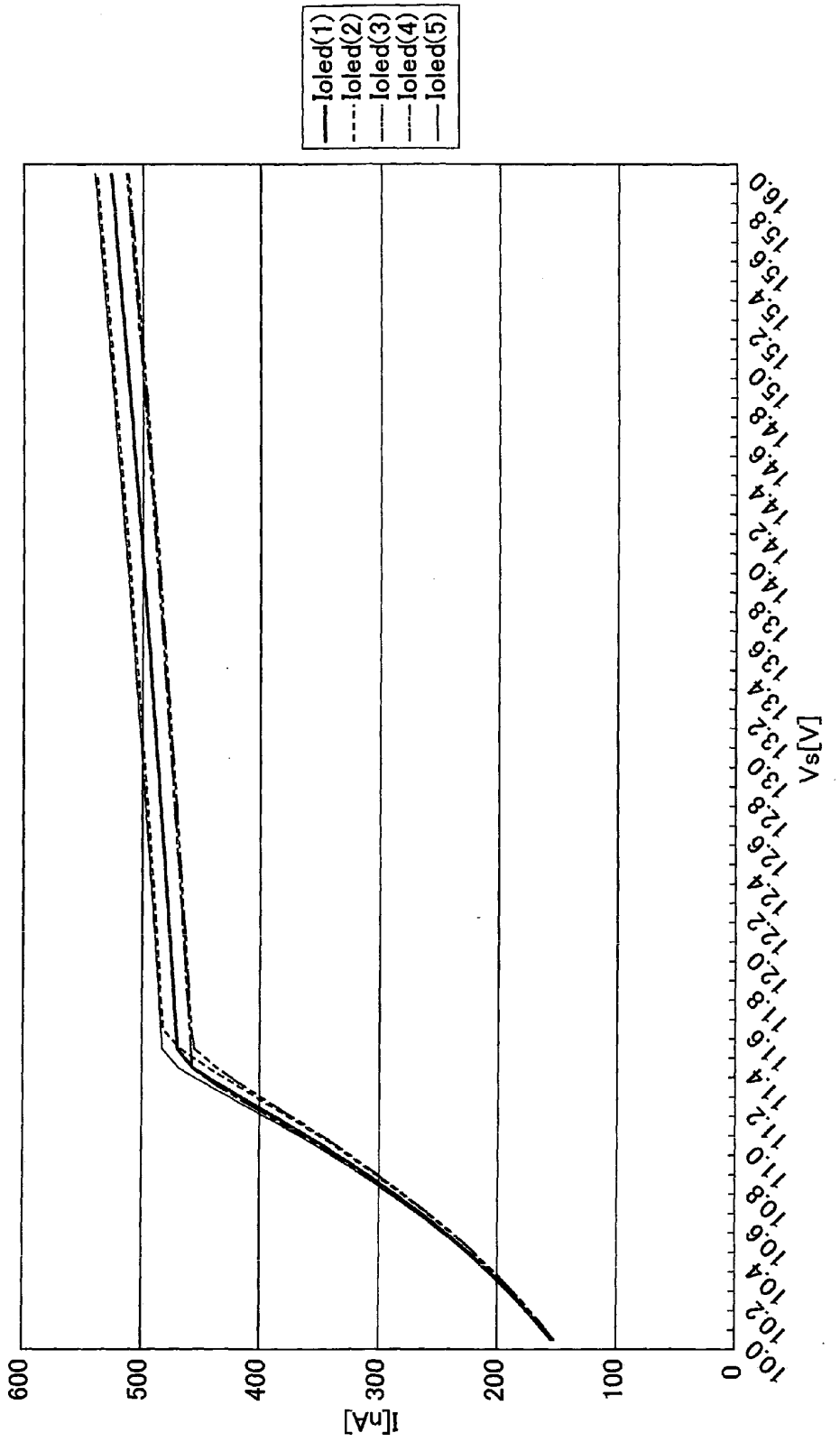

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[nA]
600
500
400
300
200
100
0
Vs[V]
10.0
10.2
10.4
10.6
10.8
11.0
11.2
11.4
11.6
11.8
12.0
12.2
12.4
12.6
12.8
13.0
13.2
13.4
13.6
13.8
14.0
14.2
14.4
14.6
14.8
15.0
15.2
15.4
15.6
15.8
16.0

FIG. 31

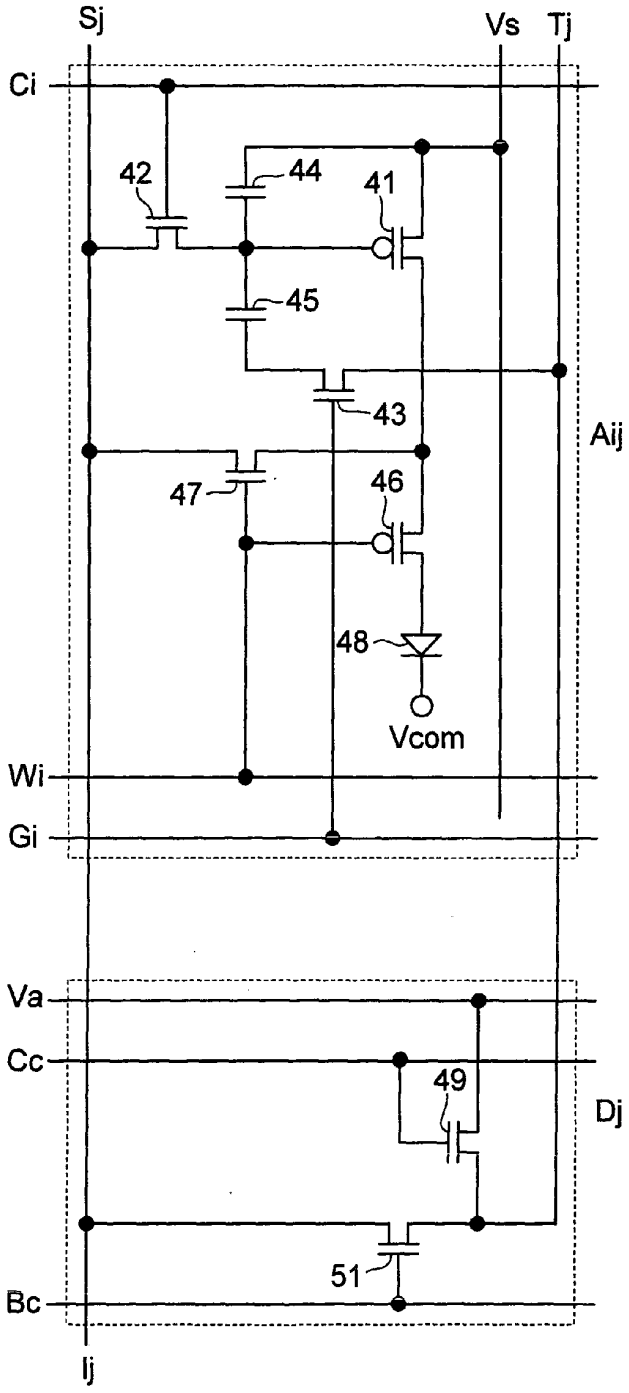


FIG. 32

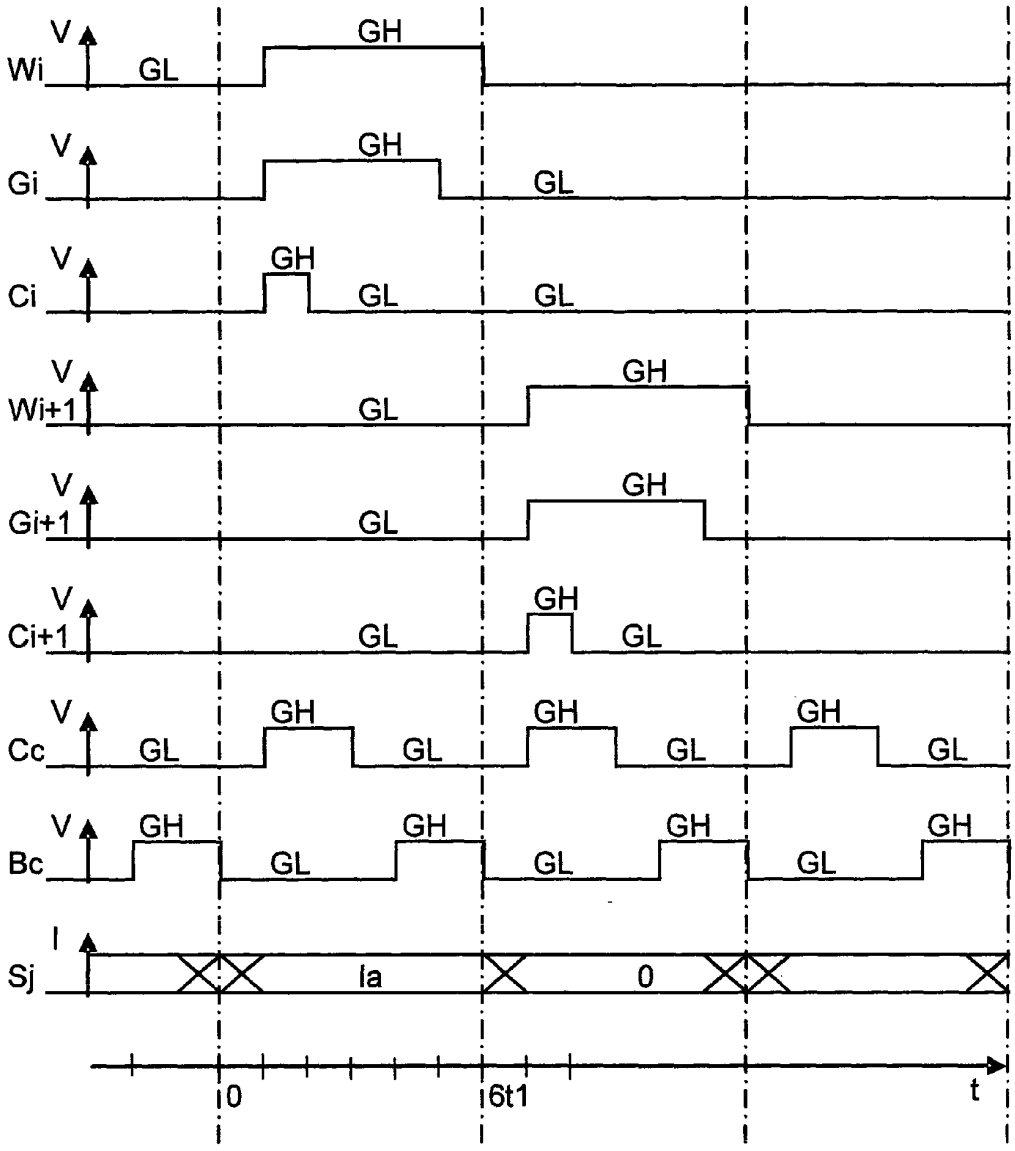

V
Wi
GL
GH
V
Gi
GH
GL
V
Ci
GH
GL
GL
V
Wi+1
GL
GH
V
Gi+1
GL
GH
V
Ci+1
GL
GH
GL
V
Cc
GL
GH
GL
GH
GL
GH
GL
V
Bc
GH
GL
GH
GL
GH
GL
GH
GL
I
Sj
Ia
0
0
6t1
t

FIG. 33

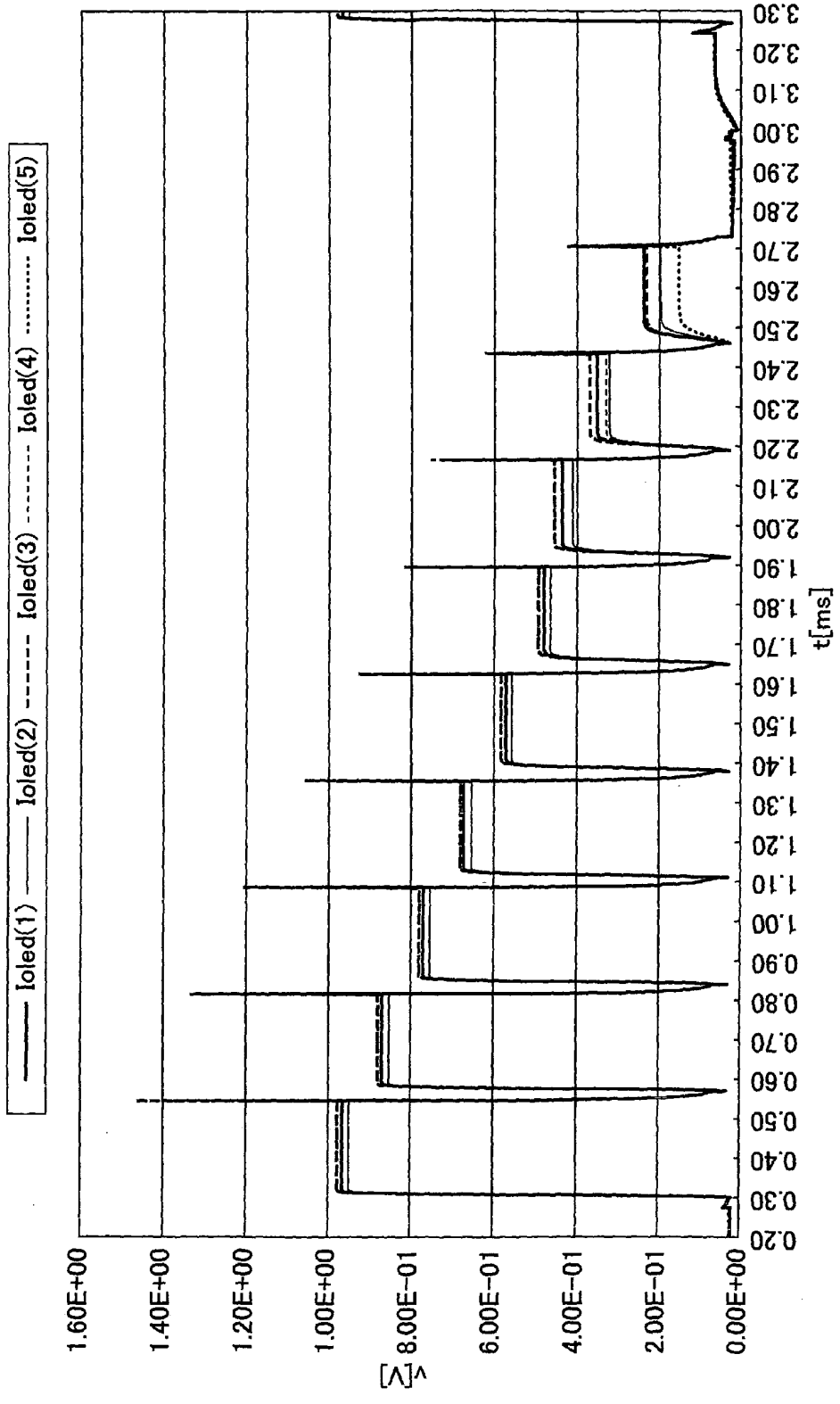

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
1.60E+00
1.40E+00
1.20E+00
1.00E+00
8.00E-01
6.00E-01
4.00E-01
2.00E-01
0.00E+00
v[V]
0.20
0.30
0.40
0.50
0.60
0.70
0.80
0.90
1.00
1.10
1.20
1.30
1.40
1.50
1.60
1.70
1.80
1.90
2.00
2.10
2.20
2.30
2.40
2.50
2.60
2.70
2.80
2.90
3.00
3.10
3.20
3.30
t[ms]

FIG. 34

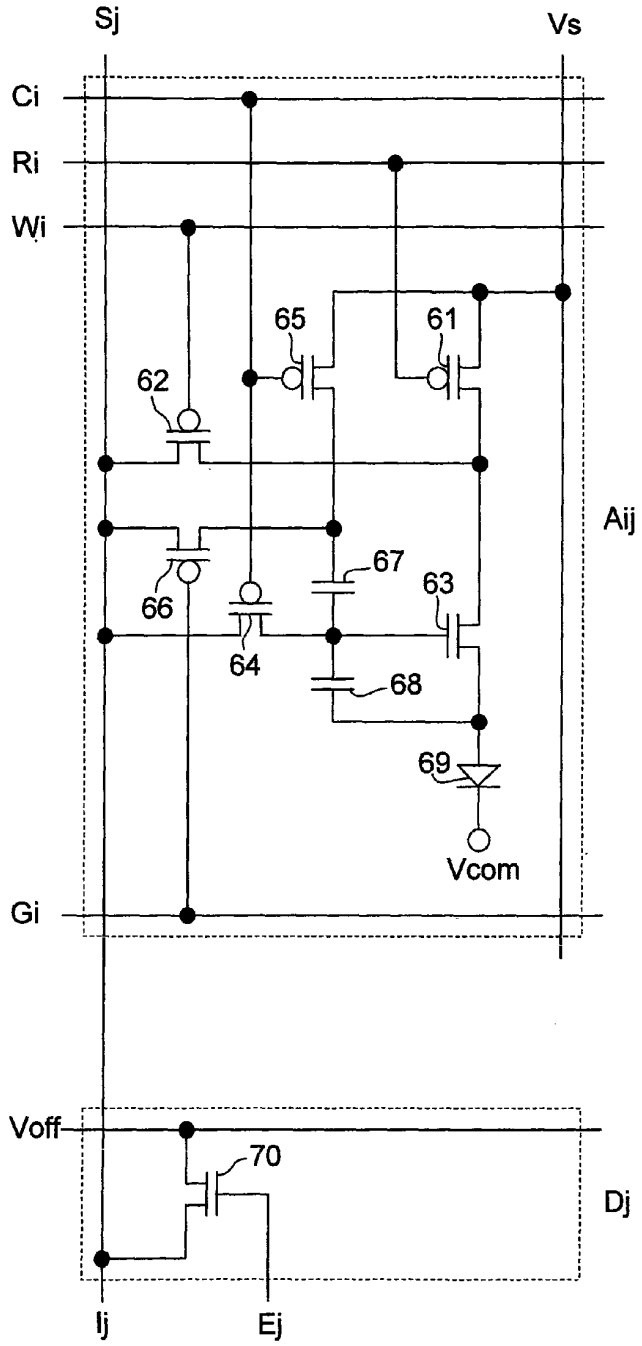


FIG. 35

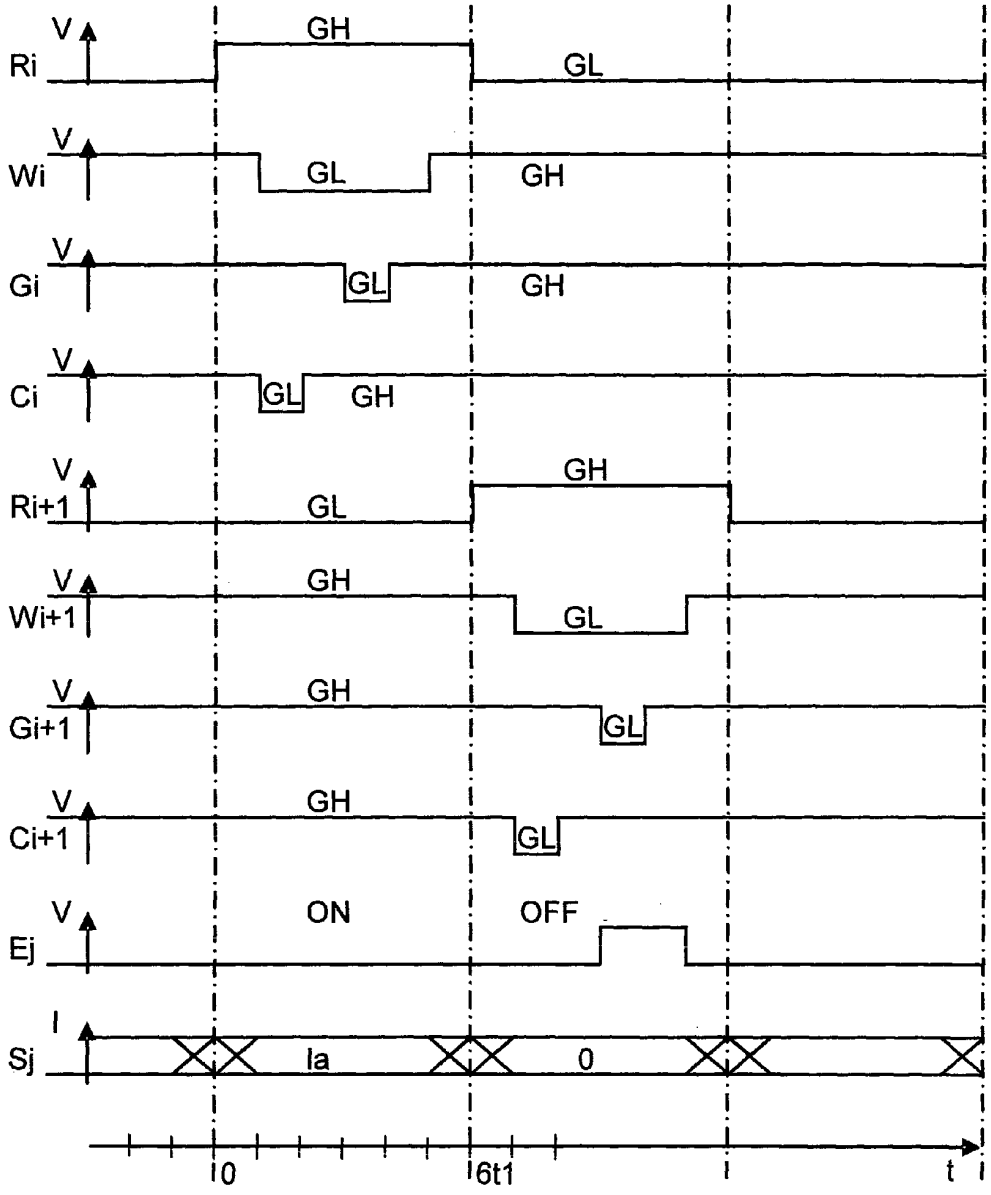

V
Ri
GH
GL
V
Wi
GL
GH
V
Gi
GL
GH
V
Ci
GL
GH
V
Ri+1
GH
GL
V
Wi+1
GH
GL
V
Gi+1
GH
GL
V
Ci+1
GH
GL
V
Ej
ON
OFF
I
Sj
Ia
0
0
6t1
t

FIG. 36

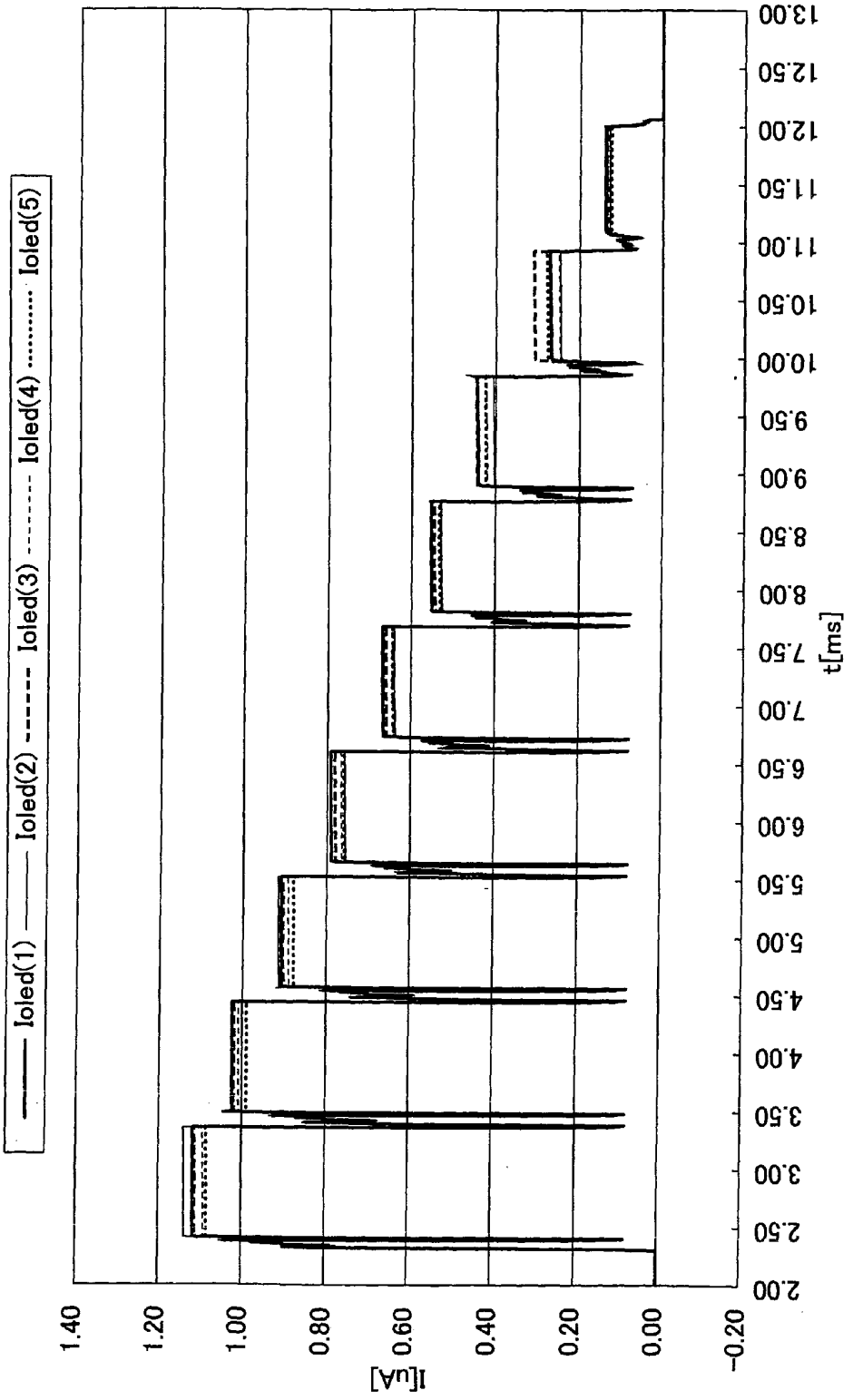

Ioled(1)
Ioled(2)
Ioled(3)
Ioled(4)
Ioled(5)
I[uA]
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
-0.20
t[ms]
2.00
2.50
3.00
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50
8.00
8.50
9.00
9.50
10.00
10.50
11.00
11.50
12.00
12.50
13.00

FIG. 37

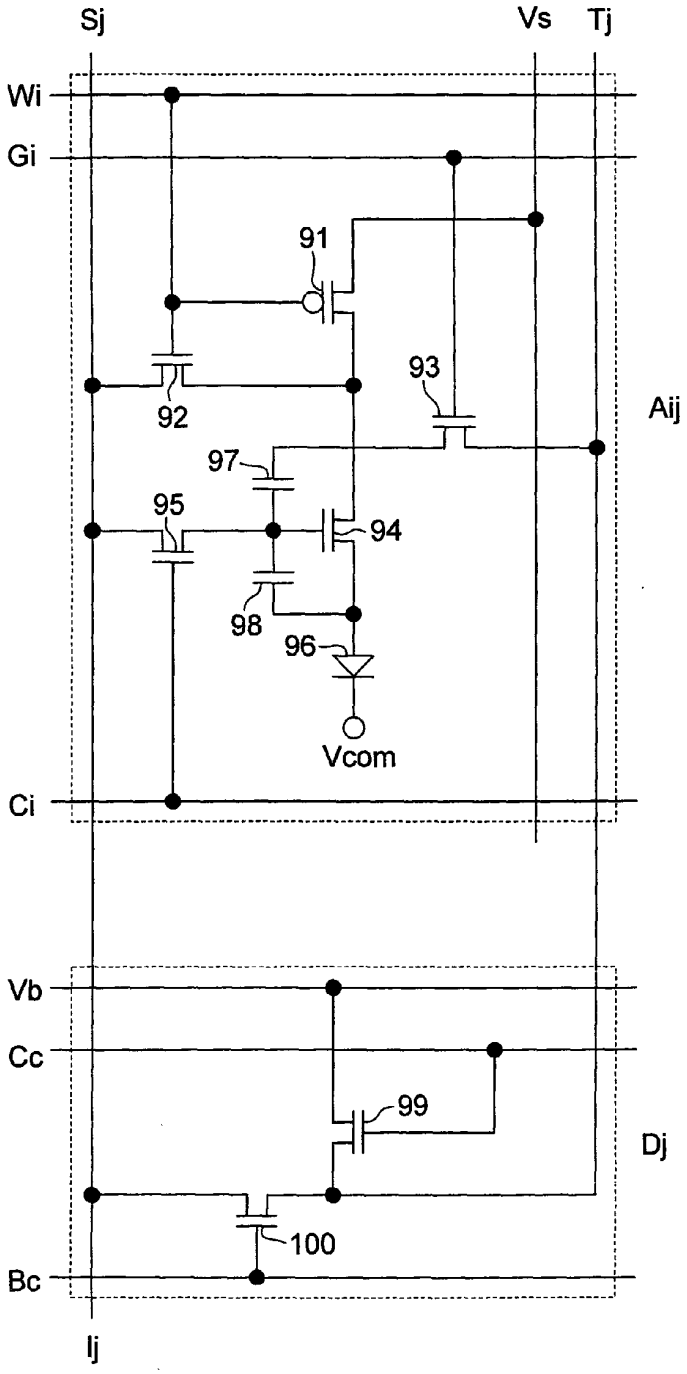

Sj
Vs
Tj
Wi
Gi
91
92
93
Aij
97
95
94
98
96
Vcom
Ci
Vb
Cc
99
Dj
100
Bc
Ij

FIG. 38

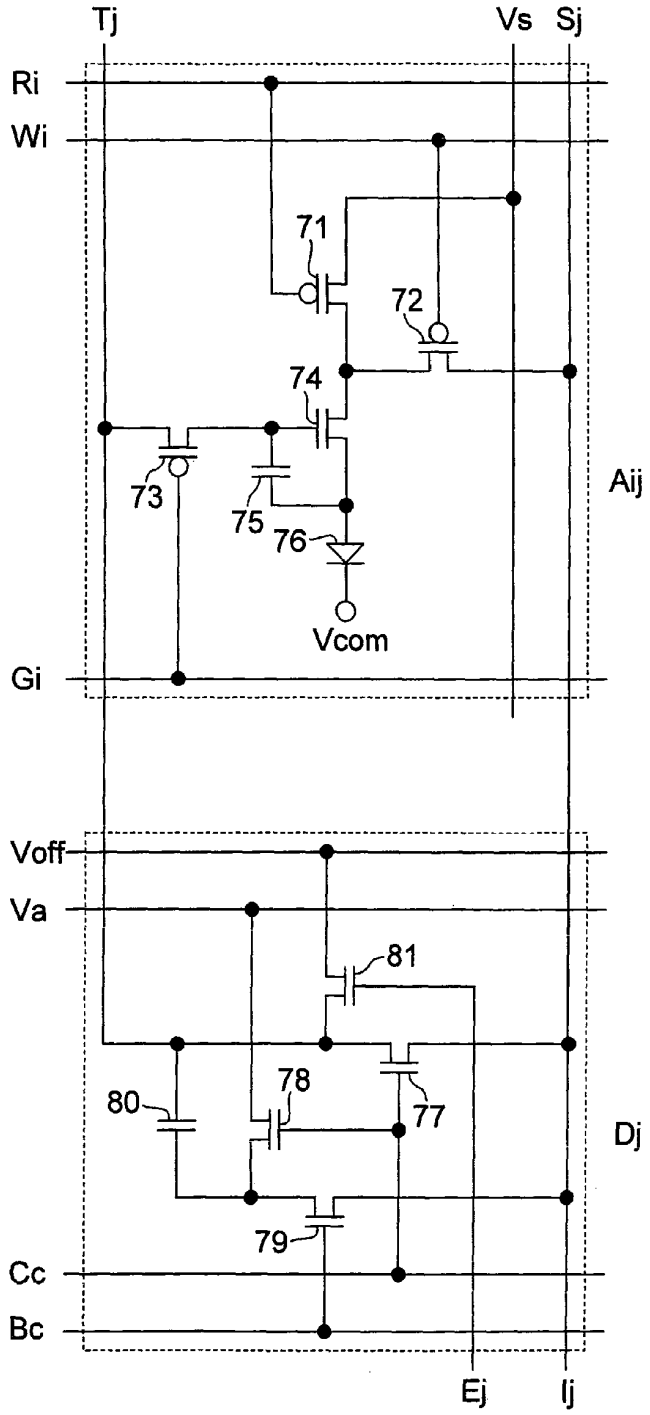

Tj
Vs
Sj
Ri
Wi
71
72
74
73
75
76
Vcom
Aij
Gi
Voff
Va
81
80
78
77
Dj
79
Cc
Bc
Ej
Ij

FIG. 39

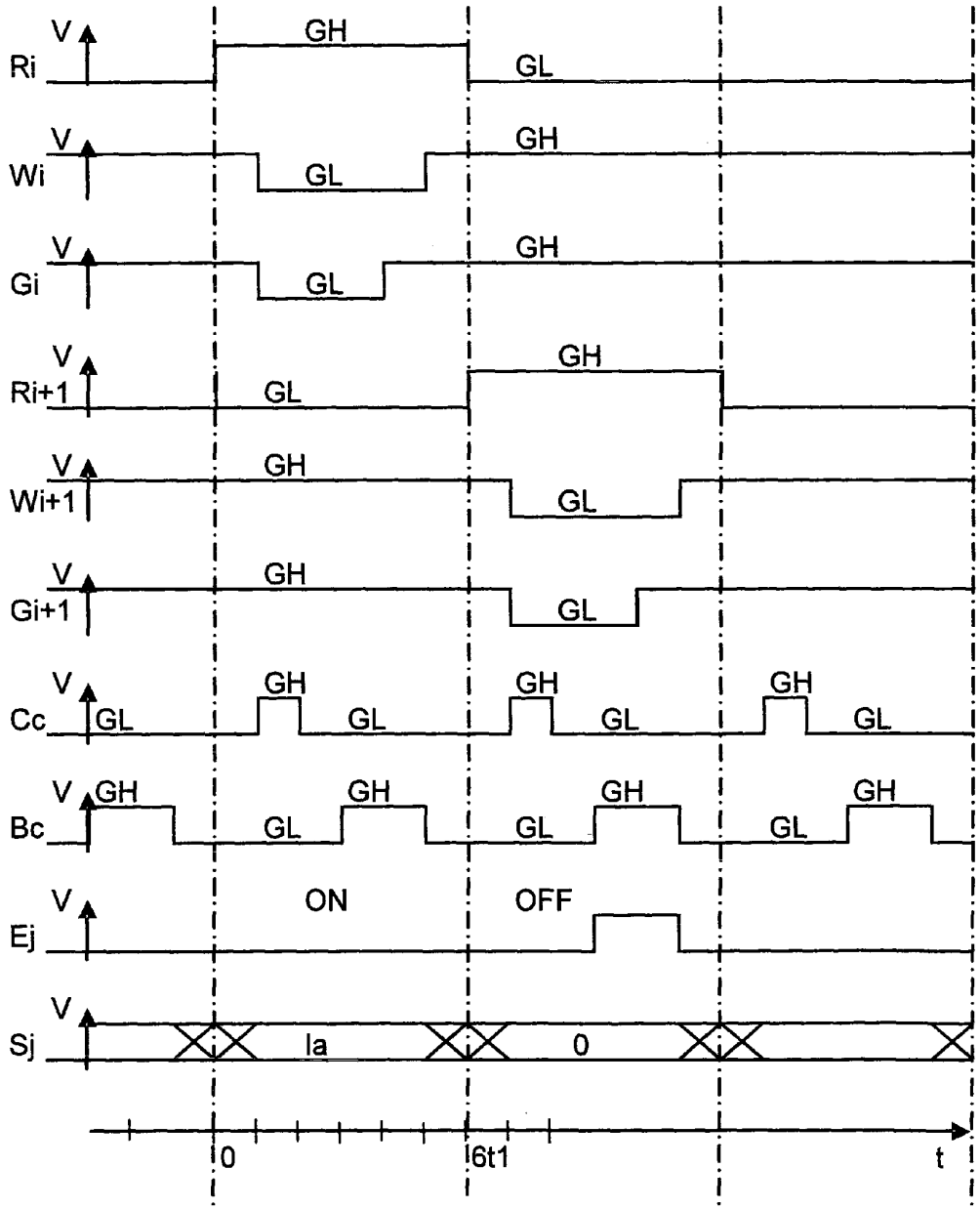

V
Ri
GH
GL
V
Wi
GH
GL
V
Gi
GH
GL
V
Ri+1
GH
GL
V
Wi+1
GH
GL
V
Gi+1
GH
GL
V
Cc
GH
GL
GH
GL
GH
GL
V
Bc
GH
GH
GL
GH
GL
GH
GL
V
Ej
ON
OFF
V
Sj
Ia
0
0
6t1
t

FIG. 40

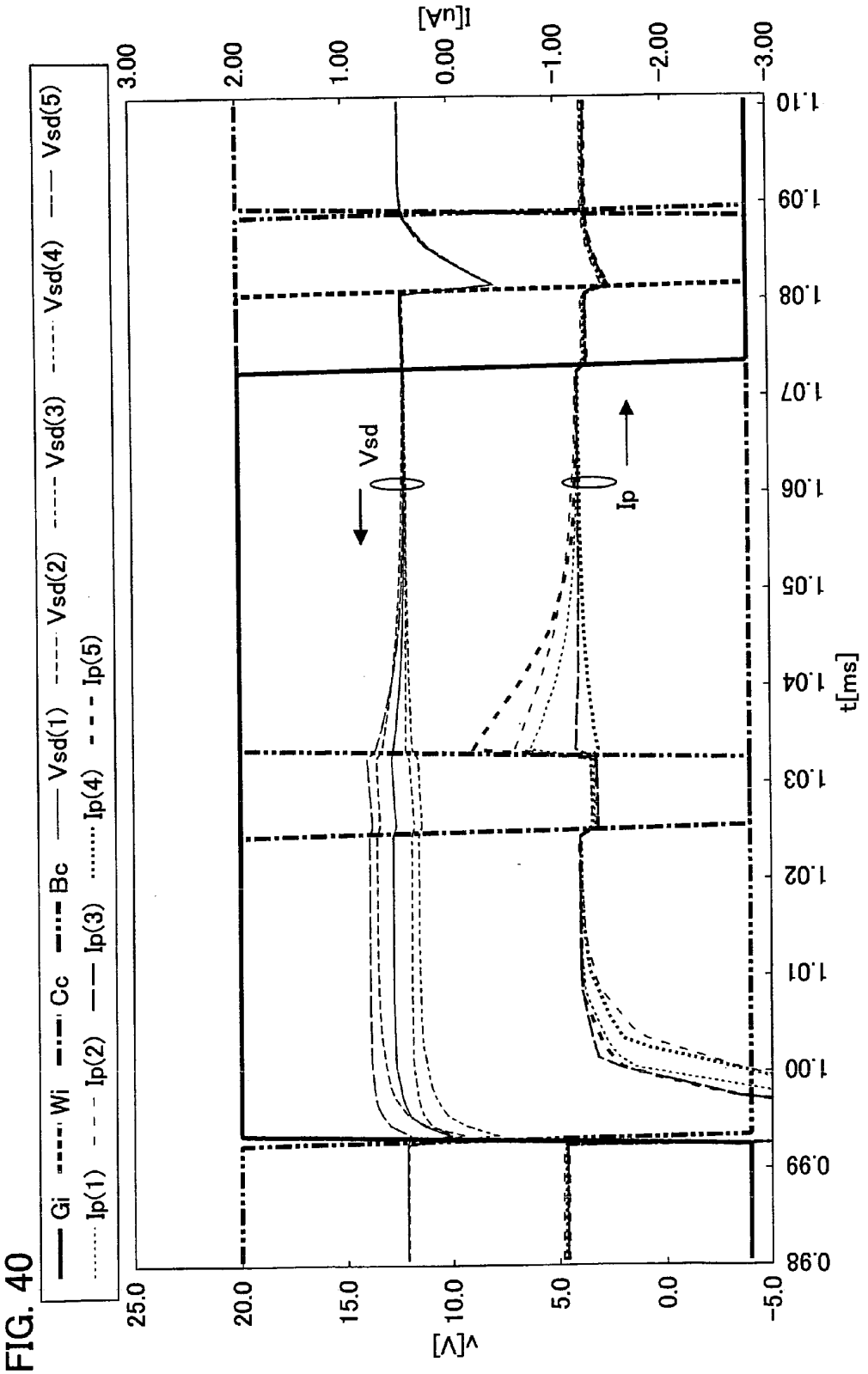

Gi
Wi
Cc
Bc
Vsd(1)
Vsd(2)
Vsd(3)
Vsd(4)
Vsd(5)
Ip(1)
Ip(2)
Ip(3)
Ip(4)
Ip(5)
Vsd
Ip
v[V]
i[uA]
t[ms]
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
3.00
2.00
1.00
0.00
-1.00
-2.00
-3.00
0.98
0.99
1.00
1.01
1.02
1.03
1.04
1.05
1.06
1.07
1.08
1.09
1.10

FIG. 41

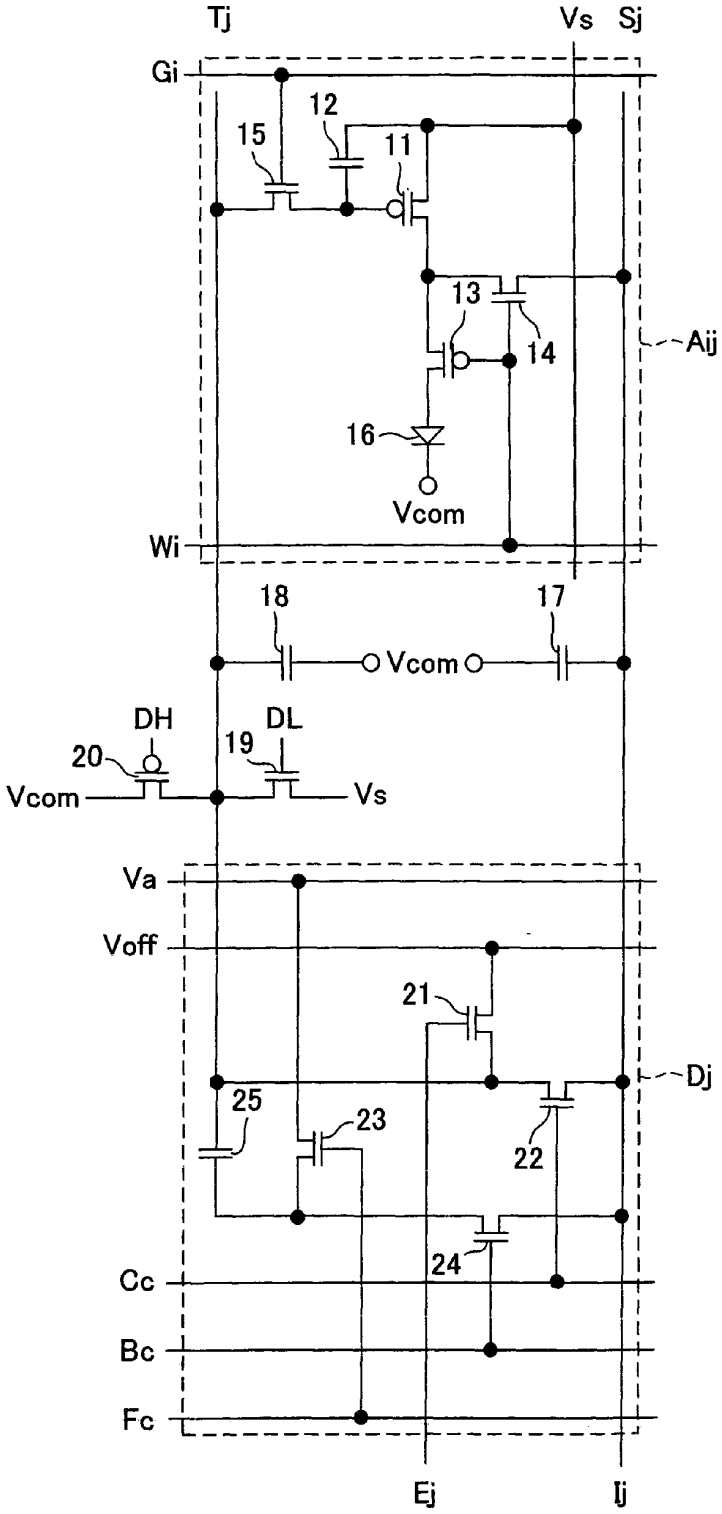

Tj
Vs
Sj
Gi
12
15
11
13
14
Aij
16
Vcom
Wi
18
17
Vcom
DH
DL
20
19
Vcom
Vs
Va
Voff
21
Dj
25
23
22
24
Cc
Bc
Fc
Ej
Ij

FIG. 42

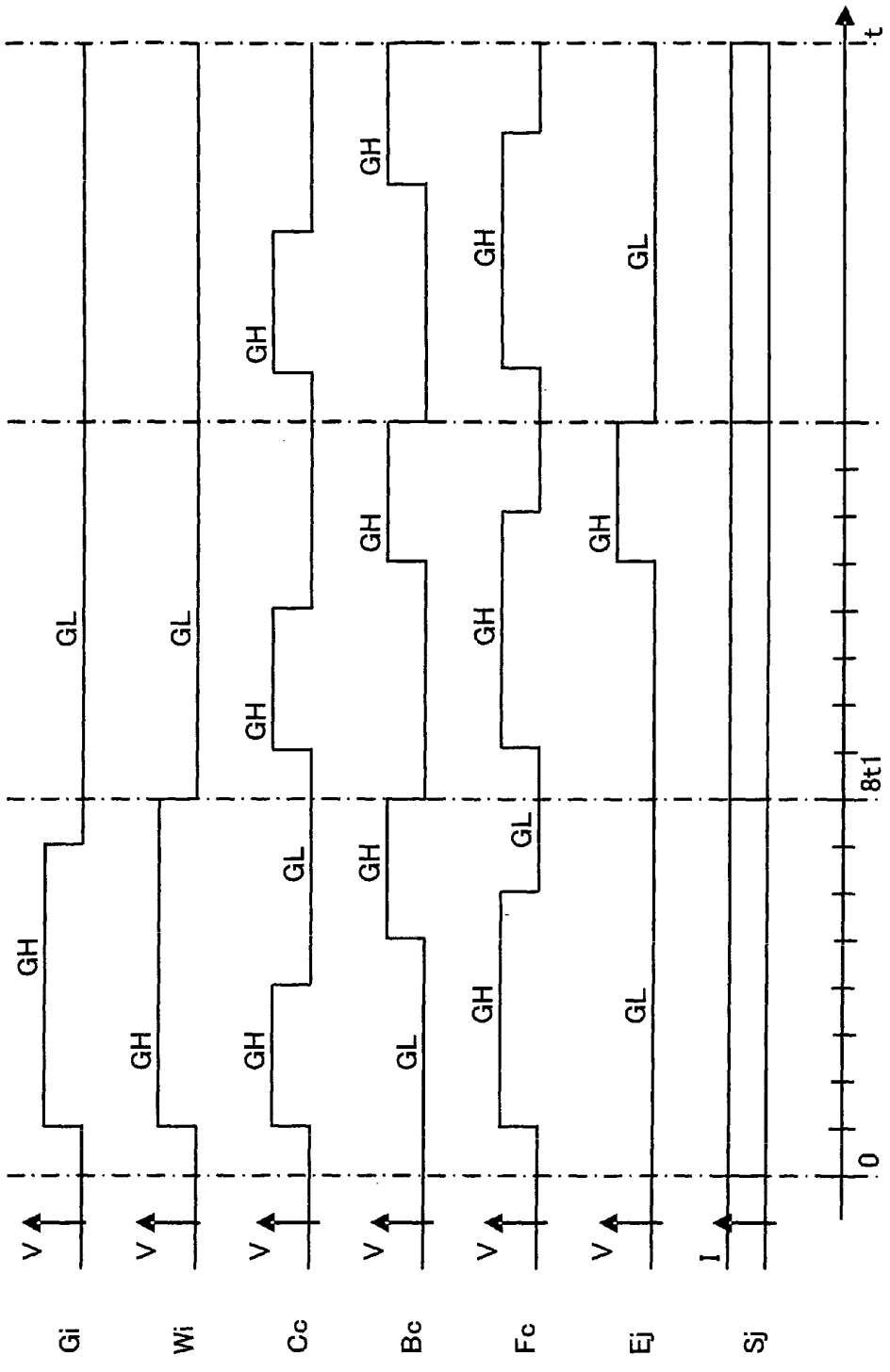


FIG. 43

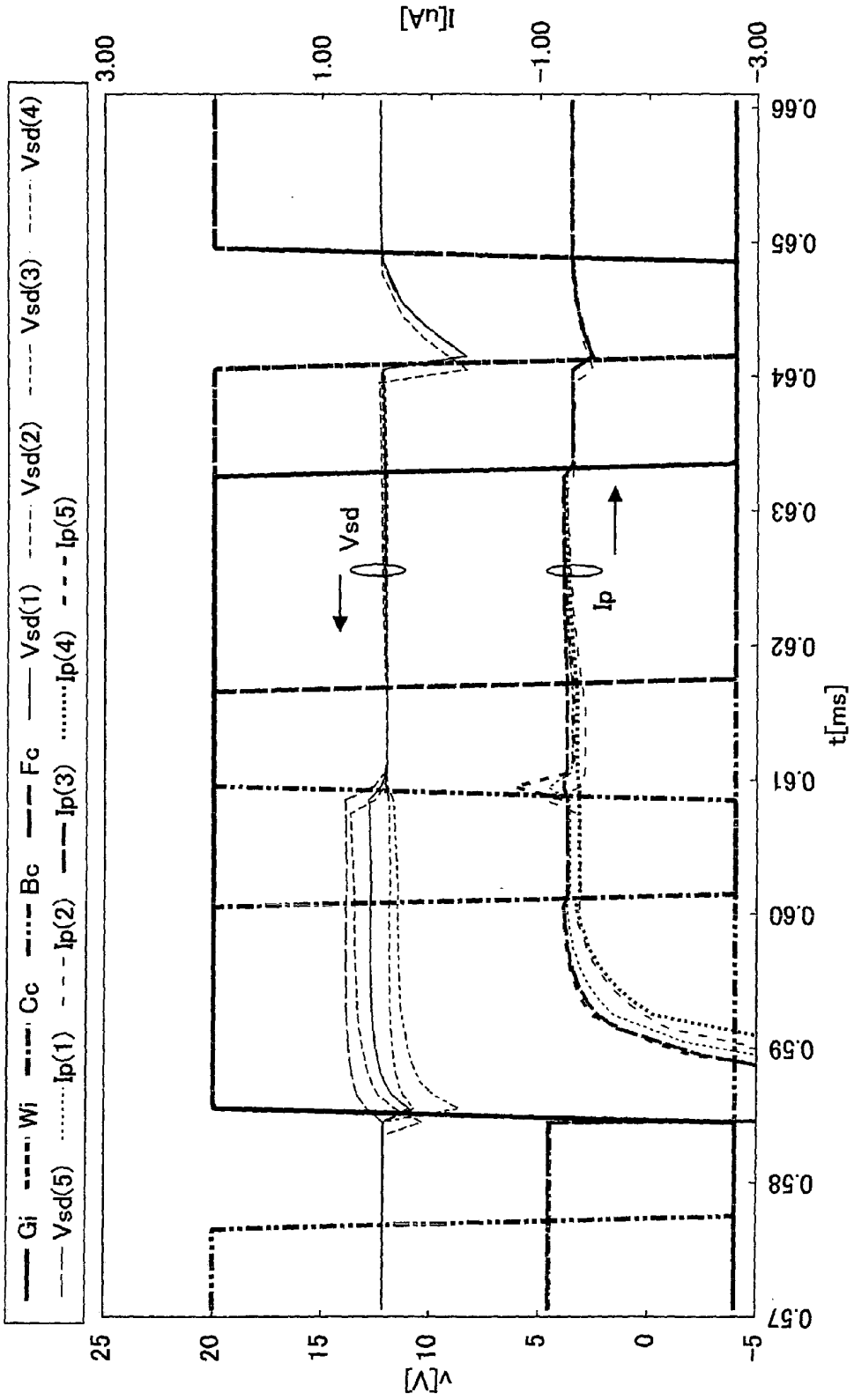

Gi
Wi
Cc
Bc
Fc
Vsd(1)
Vsd(2)
Vsd(3)
Vsd(4)
Vsd(5)
Ip(1)
Ip(2)
Ip(3)
Ip(4)
Ip(5)
Vsd
Ip
v[V]
I[uA]
t[ms]
25
20
15
10
5
0
-5
3.00
1.00
-1.00
-3.00
0.57
0.58
0.59
0.60
0.61
0.62
0.63
0.64
0.65
0.66

FIG. 44

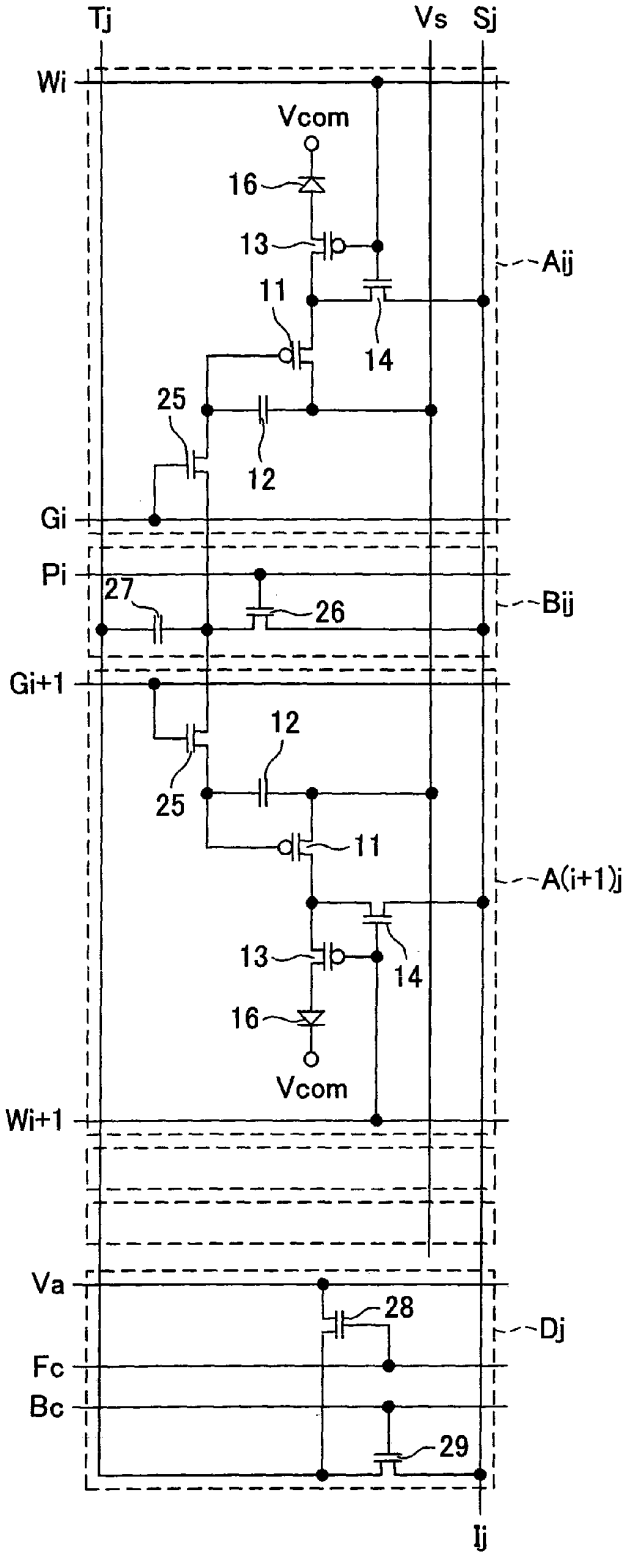
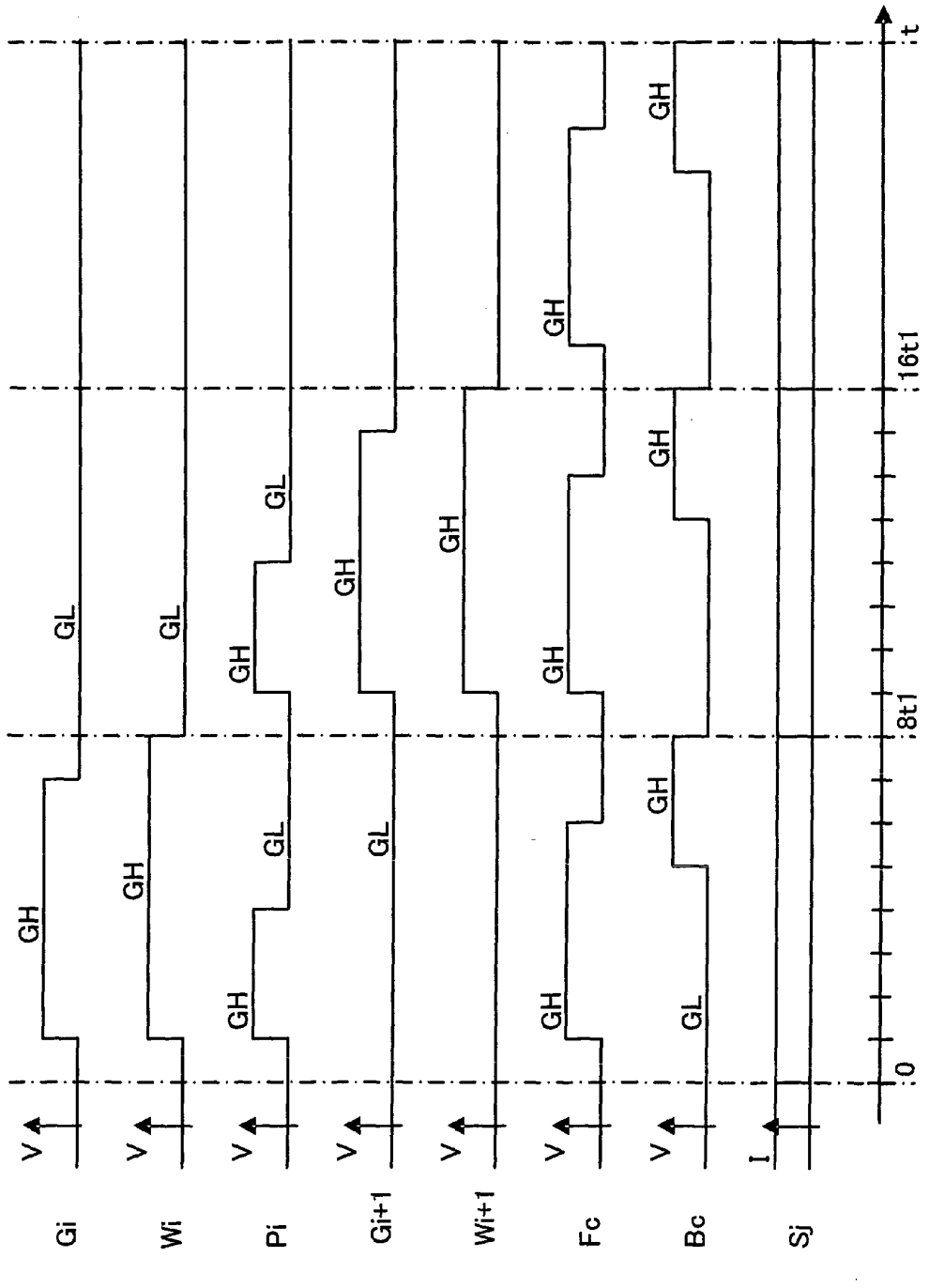

Tj
Vs
Sj
Wi
Vcom
16
13
11
14
Aij
25
12
Gi
Pi
27
26
Bij
Gi+1
12
25
11
A(i+1)j
13
14
16
Vcom
Wi+1
Va
28
Dj
Fc
Bc
29
Ij

FIG. 45



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/14042

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G09G3/30, G09G3/28, G09G3/20, H05B33/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G09G3/30, G09G3/28, G09G3/20, H05B33/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-2004
Kokai Jitsuyo Shinan Koho 1971-2004 Jitsuyo Shinan Toroku Koho 1996-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2002-351401 A (Mitsubishi Electric Corp.), 06 December, 2002 (06.12.02), Par. No. [0015]; Fig. 1 Par. Nos. [0015] to [0017]; Figs. 1 to 2 & KR 2003001530 A & WO 2002/075712 A1	1-5,9 10-12
Y	JP 2003-76327 A (NEC Corp.), 14 March, 2003 (14.03.03), Par. Nos. [0023] to [0036]; Figs. 1 to 2 & KR 2003021149 A & EP 1291839 A2 & US 2003/043131 A1	1-9
Y	WO 1998/048403 A1 (Sarnoff Corp.), 29 October, 1998 (29.10.98), Figs. 3 to 4 & EP 978114 A1 & US 6229506 B1 & JP 2002-514320 A	1-5

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 February, 2004 (02.02.04)	17 February, 2004 (17.02.04)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/14042

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 10-319908 A (Sarnoff Corp.), 04 December, 1998 (04.12.98), Par. Nos. [0037] to [0052]; Figs. 4 to 7 & KR 98081367 A & US 5952789 A	6-9
Y	JP 2003-58108 A (Sony Corp.), 28 February, 2003 (28.02.03), Par. Nos. [0042] to [0051]; Figs. 6 to 8 (Family: none)	6-9

Form PCT/ISA/210 (continuation of second sheet) (July 1998)

专利名称(译)	显示装置及其驱动方法		
公开(公告)号	EP1610291A4	公开(公告)日	2009-04-29
申请号	EP2003770115	申请日	2003-10-31
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	NUMAO TAKAJI		
发明人	NUMAO, TAKAJI		
IPC分类号	H01L51/50 G09G3/20 G09G3/30 G09G3/32 G09G3/28 H05B33/14		
CPC分类号	G09G3/325 G09G3/3275 G09G2300/0417 G09G2300/0819 G09G2300/0842 G09G2300/0852 G09G2300/0861 G09G2310/0262 G09G2320/0223 G09G2320/029 G09G2320/043		
优先权	2003366130 2003-10-27 JP 2003204018 2003-07-30 JP 2003092534 2003-03-28 JP		
其他公开文献	EP1610291A1		
外部链接	Espacenet		

摘要(译)

开关晶体管3设置在驱动TFT 1的栅极端子和其漏极端子之间。 在驱动TFT 1的栅极端子和其源极端子之间设置有第一电容器2。 驱动TFT 1的电流控制端子连接至第二电容器7的第一端子。第二电容器7的第二端子经由开关晶体管9连接至驱动TFT 1的漏极端子，并连接至预定晶体管。电压线Va经由开关晶体管8。这允许抑制在非选择时段期间流经显示装置的电流驱动发光元件的电流的变化，该电流变化是由阈值电压变化和迁移率变化引起的。 驱动TFT的 包括这样的电流驱动发光元件的显示装置的具体示例是有机EL显示装置。

FIG. 1