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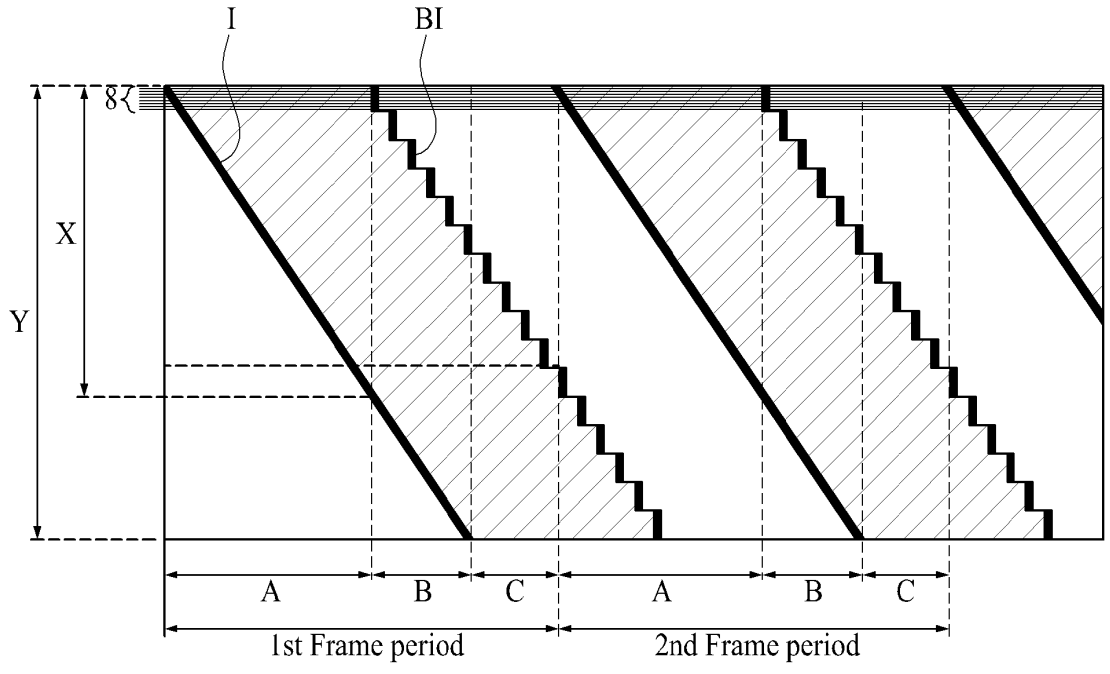
(54) ORGANIC LIGHT EMITTING DISPLAY APPARATUS

(57) Disclosed is an organic light emitting display apparatus. The organic light emitting display apparatus outputs black gate pulses for a black image (BI) and sensing gate pulses for sensing in a vertical blank period (C) and differently sets timings, at which the sensing gate pulses are output after the black gate pulses are output, for each gate line.

FIG. 6



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Description

BACKGROUND

Field of the Invention

[0001] The present disclosure relates to an organic light emitting display apparatus based on a black image mode which displays an image and then displays a black image during one frame period, for improving a motion picture response time (MPRT).

Discussion of the Related Art

[0002] In addition to liquid crystal display (LCD) apparatuses, organic light emitting display apparatuses have a problem where an image is not clearly seen due to the delay of a motion picture response time (MPRT).

[0003] In order to solve such a problem, a black image mode which displays an image and then displays a black image during one frame period is used.

[0004] In a related art organic light emitting display apparatus, a characteristic deviation of a threshold voltage (Vth) or mobility of a driving transistor occurs in each pixel due to causes such as a process deviation and degradation. For this reason, the amounts of currents for respectively driving organic light emitting diodes differ, and due to this, a luminance deviation occurs between pixels.

[0005] In order to overcome such drawbacks, various kinds of compensation methods are used.

[0006] In order to apply the compensation methods, sensing image data voltages have to be output to an organic light emitting display panel in a vertical blank period, where image data voltages are not output, of one frame period

[0007] Moreover, in an organic light emitting display apparatus using the black image mode, black image data voltages have to be output to the organic light emitting display panel in the vertical blank period.

[0008] However, in the related art organic light emitting display apparatus, all of the sensing image data voltages for compensating for mobility and the black image data voltages for applying the black image mode may not be output to the organic light emitting display panel in the vertical blank period.

SUMMARY

[0009] Accordingly, the present disclosure is directed to providing an organic light emitting display apparatus that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0010] An aspect of the present disclosure is directed to providing an organic light emitting display apparatus which outputs black gate pulses for a black image and sensing gate pulses for sensing in a vertical blank period and differently sets timings, at which the sensing gate pulses are output after the black gate pulses are output, for each gate line.

[0011] Additional advantages and features of the disclosure will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the disclosure. The objectives and other advantages of the disclosure may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0012] To achieve these and other advantages and in accordance with the purpose of the disclosure, as embodied and broadly described herein, there is provided an organic light emitting display apparatus defined in claim 1. Further embodiments are defined in the dependent claims. Various embodiments provide an organic light emitting display apparatus including an organic light emitting display panel including a plurality of pixels each including an organic light emitting diode and a driving transistor for driving the organic light emitting diode, a gate driver outputting image gate pulses, which control outputs of image data voltages used to display an image, to gate lines included in the organic light emitting display panel in a first period of a first frame period, outputting the image gate pulses and black gate pulses for controlling outputs of black image data voltages used to display a black image in a second period arriving after the first period, and outputting a sensing gate pulse to one gate line connected to driving transistors, of which characteristic variation is to be sensed, in a third period until a first period of a second frame starts after the second period of the first frame period, a data driver outputting data voltages to data lines included in the organic light emitting display panel, and a controller controlling the gate driver and the data driver, wherein the gate driver includes a first driver generating the image gate pulses, the black gate pulses, and the sensing gate pulse by using first to eighth gate clocks transferred from the controller in the first frame period, a second driver generating the image gate pulses, the black gate pulses, and the sensing gate pulse by using ninth to sixteenth gate clocks transferred from the controller in the first frame period, and a third driver controlling the first driver and the second driver to output the sensing gate pulse in a third period of the first frame period.

[0013] According to various embodiments of the present disclosure, there is provided an organic light emitting display apparatus including an organic light emitting display panel including a plurality of pixels each including an organic light emitting diode and a driving transistor for driving the organic light emitting diode, a gate driver outputting image gate pulses, which control outputs of image data voltages used to display an image, to gate lines included in the organic light emitting display panel in a first period of a first frame period, outputting the image gate pulses and black gate pulses for controlling outputs of black image data voltages used to display

a black image in a second period arriving after the first period, and outputting a sensing gate pulse to one gate line connected to driving transistors, of which characteristic variation is to be sensed, in a third period until a first period of a second frame starts after the second period of the first frame period, a data driver outputting data voltages to data lines included in the organic light emitting display panel, and a controller controlling the gate driver and the data driver, wherein a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse is output in the third period of the first frame period differs from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse is output in a third period of the second frame period.

[0014] According to various embodiments, there is provided an organic light emitting display apparatus comprising: an organic light emitting display panel including a plurality of pixels each including an organic light emitting diode and a driving transistor for driving the organic light emitting diode; a gate driver outputting image gate pulses, which control outputs of image data voltages used to display an image, to gate lines included in the organic light emitting display panel in a first period of a first frame period, outputting the image gate pulses and black gate pulses for controlling outputs of black image data voltages used to display a black image in a second period arriving after the first period, and outputting a sensing gate pulse to one gate line connected to driving transistors, of which characteristic variation is to be sensed, in a third period until a first period of a second frame starts after the second period of the first frame period; a data driver outputting data voltages to data lines included in the organic light emitting display panel; and a controller controlling the gate driver and the data driver, wherein the gate driver comprises: a first driver generating the image gate pulses, the black gate pulses, and the sensing gate pulse by using first to eighth gate clocks transferred from the controller in the first frame period; a second driver generating the image gate pulses, the black gate pulses, and the sensing gate pulse by using ninth to sixteenth gate clocks transferred from the controller in the first frame period; and a third driver controlling the first driver and the second driver to output the sensing gate pulse in a third period of the first frame period.

[0015] According to various embodiments, the data driver outputs the image data voltages in the first period, outputs the image data voltages or the black image data voltages in the second period, and outputs sensing image data voltages for displaying a sensing image or the black image data voltages in the third period.

[0016] According to various embodiments, the black gate pulses are output in a period from the second period of the first frame period to a partial period of the first period of the second frame period.

[0017] According to various embodiments, the third driver selects a sensing gate line, to which the sensing gate pulse is to be output, from among the gate lines according to a line selection signal transferred from the controller and controls the first driver or the second driver according to a reset signal transferred from the controller so that the first driver or the second driver outputs the sensing gate pulse to the sensing gate line.

[0018] According to various embodiments, the controller outputs the line selection signal to the third driver at a timing at which a gate clock, corresponding to an image gate pulse output to the sensing gate line in the first period or the second period of the first frame period, of the gate clocks is output to the first driver or the second driver.

[0019] According to various embodiments, when the sensing gate pulse is output from the first driver, the controller selects, as a sensing-enabled period, one period of a first sleeping period and transfers the reset signal, indicating the start of the sensing-enabled period, to the third driver, wherein the first sleeping period is a period between a period where the second driver outputs black gate pulses after the first driver is driven for outputting the black gate pulses and a period where the first driver is again driven for outputting the black gate pulses, in the third period.

[0020] According to various embodiments, when the sensing gate pulse is output from the second driver, the controller selects, as a sensing-enabled period, one period of a second sleeping period and transfers the reset signal, indicating the start of the sensing-enabled period, to the third driver, wherein the second sleeping period is a period between a period where the first driver outputs black gate pulses after the second driver is driven for outputting the black gate pulses and a period where the second driver is again driven for outputting the black gate pulses, in the third period.

[0021] According to various embodiments, a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse is output in the third period of the first frame period differs from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse is output in a third period of the second frame period.

[0022] According to various embodiments, the first driver or the second driver simultaneously outputs the black gate pulses to eight gate lines.

[0023] According to various embodiments, the first driver generates the image gate pulses by using first to eighth gate clocks, and the second driver generates the image gate pulses by using ninth to sixteenth gate clocks.

[0024] According to various embodiments, an interval between a fourth image gate pulse and a fifth image gate pulse each output from the first driver is greater than an interval between other image gate pulses output from the first driver, and an interval between a twelfth gate clock and a thirteenth gate clock each output from the second driver is greater than an interval between other gate clocks output from the second driver.

[0025] According to various embodiments, the first driver outputs the black gate pulse in a period between a period where the fourth gate clock is output and a period

where the fifth gate clock is output, and the second driver outputs the black gate pulse in a period between a period where the twelfth gate clock is output and a period where the thirteenth gate clock is output.

[0026] According to various embodiments, there is provided an organic light emitting display apparatus comprising: an organic light emitting display panel including a plurality of pixels each including an organic light emitting diode and a driving transistor for driving the organic light emitting diode; a gate driver outputting image gate pulses, which control outputs of image data voltages used to display an image, to gate lines included in the organic light emitting display panel in a first period of a first frame period, outputting the image gate pulses and black gate pulses for controlling outputs of black image data voltages used to display a black image in a second period arriving after the first period, and outputting a sensing gate pulse to one gate line connected to driving transistors, of which characteristic variation is to be sensed, in a third period until a first period of a second frame starts after the second period of the first frame period; a data driver outputting data voltages to data lines included in the organic light emitting display panel; and a controller controlling the gate driver and the data driver, wherein a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse is output in the third period of the first frame period differs from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse is output in a third period of the second frame period.

[0027] According to various embodiments, the black gate pulses are output in a period from the second period of the first frame period to a partial period of the first period of the second frame period.

[0028] According to various embodiments, the gate driver comprises: a first driver generating the image gate pulses, the black gate pulses, and the sensing gate pulse by using first to eighth gate clocks transferred from the controller in the first frame period; a second driver generating the image gate pulses, the black gate pulses, and the sensing gate pulse by using ninth to sixteenth gate clocks transferred from the controller in the first frame period; and a third driver controlling the first driver and the second driver to output the sensing gate pulse in a third period of the first frame period.

[0029] According to various embodiments, the first driver and the second driver alternately output sixteen image gate pulses.

[0030] According to various embodiments, the first driver and the second driver repeatedly perform the same function at a period corresponding to thirty-two image gate pulses.

[0031] According to various embodiments, when the first driver and the second driver alternately output sixteen image gate pulses, the first driver and the second driver repeatedly perform the same function at a period corresponding to thirty-two image gate pulses, and number of the gate lines is 2,160, a period where the gate pulses are output is expressed as 32n+16 (where n is a natural number equal to or less than 67), and when n is 67, all of 2,160 gate pulses are output.

[0032] According to various embodiments, the first driver outputs sixteen image gate pulses by using the first to eighth gate clocks, after the first driver outputs the sixteen image gate pulses, the second driver outputs sixteen image gate pulses by using the ninth to sixteenth gate clocks, after the second driver outputs the sixteen image gate pulses, the first driver outputs sixteen other image gate pulses by using the first to eighth gate clocks, and after the first driver outputs the sixteen other image gate pulses, the second driver outputs sixteen other image gate pulses by using the ninth to sixteenth gate clocks.

[0033] According to various embodiments, the first driver or the second driver simultaneously output the black gate pulses to eight gate lines.

[0034] According to various embodiments of the present disclosure, there is provided an organic light emitting display apparatus comprising: an organic light emitting display panel including a plurality of pixels each including an organic light emitting diode and a driving transistor for driving the organic light emitting diode; a gate driver configured to output image gate pulses, which control outputs of image data voltages used to display an image, to gate lines included in the organic light emitting display panel in a first period of a first frame period, to output the image gate pulses and black gate pulses for controlling outputs of black image data voltages used to display a black image in a second period subsequent to the first period, and to output a sensing gate pulse to one gate line connected to driving transistors, of which characteristic variation is to be sensed, in a third period subsequent to the second period until a first period of a second frame starts; a data driver configured to output data voltages to data lines included in the organic light emitting display panel; and a controller configured to control the gate driver and the data driver.

[0035] According to various embodiments, the gate driver comprises: a first driver configured to generate the image gate pulses, the black gate pulses, and the sensing gate pulse by using a first predetermined number of gate clocks transferred from the controller in the first frame period, optionally by using first to eighth gate clocks transferred from the controller in the first frame period; a second driver configured to generate the image gate pulses, the black gate pulses, and the sensing gate pulse by using a second predetermined number of gate clocks transferred from the controller in the first frame period, optionally by using ninth to sixteenth gate clocks transferred from the controller in the first frame period; and a third driver configured to control the first driver and the second driver to output the sensing gate pulse in a third period of the first frame period.

[0036] According to various embodiments, the third driver is configured to select a sensing gate line, to which the sensing gate pulse is to be output, from among the

gate lines according to a line selection signal transferred from the controller and to control the first driver or the second driver according to a reset signal transferred from the controller so that the first driver or the second driver outputs the sensing gate pulse to the sensing gate line.

[0037] According to various embodiments, the controller is configured to output the line selection signal to the third driver at a timing at which a gate clock, corresponding to an image gate pulse output to the sensing gate line in the first period or the second period of the first frame period, of the gate clocks is output to the first driver or the second driver.

[0038] According to various embodiments, the controller is configured to select, as a sensing-enabled period, when the sensing gate pulse is output from the first driver, one period of a first sleeping period and to transfer the reset signal, indicating the start of the sensing-enabled period, to the third driver, wherein the first sleeping period is a period between a period where the second driver outputs black gate pulses after the first driver is driven for outputting the black gate pulses and a period where the first driver is again driven for outputting the black gate pulses, in the third period.

[0039] According to various embodiments, the controller is configured to select, as a sensing-enabled period, when the sensing gate pulse is output from the second driver, one period of a second sleeping period and to transfer the reset signal, indicating the start of the sensing-enabled period, to the third driver, wherein the second sleeping period is a period between a period where the first driver outputs black gate pulses after the second driver is driven for outputting the black gate pulses and a period where the second driver is again driven for outputting the black gate pulses, in the third period.

[0040] According to various embodiments, the first driver and/or the second driver are/is configured to simultaneously output the black gate pulses to eight gate lines.

[0041] According to various embodiments, the first driver is configured to generate the image gate pulses by using first to eighth gate clocks, and the second driver is configured to generate the image gate pulses by using ninth to sixteenth gate clocks.

[0042] According to various embodiments, an interval between a fourth image gate pulse and a fifth image gate pulse each output from the first driver is greater than an interval between other image gate pulses output from the first driver, and an interval between a twelfth image gate pulse and a thirteenth image gate pulse each output from the second driver is greater than an interval between other image gate pulses output from the second driver.

[0043] According to various embodiments, the first driver is configured to output the black gate pulse in a period between a period where the fourth gate clock is output and a period where the fifth gate clock is output, and the second driver is configured to output the black gate pulse in a period between a period where the twelfth gate clock is output and a period where the thirteenth gate clock is output.

[0044] According to various embodiments, the first driver and the second driver are configured to alternately output sixteen image gate pulses.

[0045] According to various embodiments, the first driver and the second driver are configured to repeatedly perform the same function at a period corresponding to thirty-two image gate pulses.

[0046] According to various embodiments, when the first driver and the second driver are configured to alternately output sixteen image gate pulses, the first driver and the second driver are configured to repeatedly perform the same function at a period corresponding to thirty-two image gate pulses, and the number of the gate lines is 2,160, wherein a period where the gate pulses are output is expressed as 32n+16, where n is a natural number equal to or less than 67, and when n is 67, all of 2,160 gate pulses are output.

[0047] According to various embodiments, the first driver is configured to output sixteen image gate pulses by using the first to eighth gate clocks, the second driver is configured to output sixteen image gate pulses by using the ninth to sixteenth gate clocks, after the first driver outputs the sixteen image gate pulses, the first driver is configured to output sixteen other image gate pulses by using the first to eighth gate clocks, after the second driver outputs the sixteen image gate pulses, and the second driver is configured to output sixteen other image gate pulses by using the ninth to sixteenth gate clocks, after the first driver outputs the sixteen other image gate pulses.

[0048] According to various embodiments, the data driver is configured to output the image data voltages in the first period, to output the image data voltages or the black image data voltages in the second period, and to output sensing image data voltages for displaying a sensing image or the black image data voltages in the third period.

[0049] According to various embodiments, the black gate pulses are output in a period from the second period of the first frame period to a partial period of the first period of the second frame period.

[0050] According to various embodiments, a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse is output in the third period of the first frame period differs from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse is output in a third period of the second frame period.

[0051] It is to be understood that both the foregoing general description and the following detailed description of the present disclosure are exemplary and explanatory and are intended to provide further explanation of the disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0052] The accompanying drawings, which are includ-

ed to provide a further understanding of the disclosure and are incorporated in and constitute a part of this application, illustrate embodiments of the disclosure and together with the description serve to explain the principle of the disclosure. In the drawings:

FIG. 1 is an exemplary diagram illustrating a configuration of an organic light emitting display apparatus according to the present disclosure;

FIG. 2 is an exemplary diagram illustrating a configuration of one pixel of an organic light emitting display apparatus according to the present disclosure;

FIG. 3 is an exemplary diagram illustrating a configuration of a controller applied to an organic light emitting display apparatus according to the present disclosure;

FIG. 4 is an exemplary diagram illustrating a configuration of a data driver applied to an organic light emitting display apparatus according to the present disclosure;

FIG. 5 is an exemplary diagram illustrating a configuration of a gate pulse output unit of a gate driver applied to an organic light emitting display apparatus according to the present disclosure;

FIG. 6 is an exemplary diagram illustrating a driving period of an organic light emitting display apparatus according to the present disclosure;

FIG. 7 is an exemplary diagram showing waveforms of clocks applied to an organic light emitting display apparatus according to the present disclosure;

FIG. 8 is an exemplary diagram showing gate pulses output from a gate driver in a second period of an organic light emitting display apparatus according to the present disclosure;

FIG. 9 is an exemplary diagram showing gate pulses output from a gate driver in a third period of an organic light emitting display apparatus according to the present disclosure; and

FIG. 10 is an exemplary diagram showing a third period of an organic light emitting display apparatus according to the present disclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0053] Reference will now be made in detail to the exemplary embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0054] Advantages and features of the present disclosure, and implementation methods thereof will be clarified through following embodiments described with reference to the accompanying drawings. The present disclosure may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present disclosure to those skilled in the art. Furthermore, the present disclosure is only defined by scopes of claims.

[0055] In the specification, in adding reference numerals for elements in each drawing, it should be noted that like reference numerals already used to denote like elements in other drawings are used for elements wherever possible.

[0056] A shape, a size, a ratio, an angle, and a number disclosed in the drawings for describing embodiments of the present disclosure are merely an example, and thus, the present disclosure is not limited to the illustrated details. Like reference numerals refer to like elements throughout. In the following description, when the detailed description of the relevant known function or configuration is determined to unnecessarily obscure the important point of the present disclosure, the detailed description will be omitted. In a case where 'comprise', 'have', and 'include' described in the present specification are used, another part may be added unless 'only~' is used. The terms of a singular form may include plural forms unless referred to the contrary.

[0057] In construing an element, the element is construed as including an error range although there is no explicit description.

[0058] In describing a position relationship, for example, when a position relation between two parts is described as 'on~', 'over~', 'under~', and 'next~', one or more other parts may be disposed between the two parts unless 'just' or 'direct' is used.

[0059] In describing a time relationship, for example, when the temporal order is described as 'after~', 'subsequent~', 'next~', and 'before~', a case which is not continuous may be included unless 'just' or 'direct' is used.

[0060] The term "at least one" should be understood as including any and all combinations of one or more of the associated listed items. For example, the meaning of "at least one of a first item, a second item, and a third item" denotes the combination of all items proposed from two or more of the first item, the second item, and the third item as well as the first item, the second item, or the third item.

[0061] It will be understood that, although the terms "first", "second", etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure.

[0062] Features of various embodiments of the present disclosure may be partially or overall coupled to or combined with each other, and may be variously inter-operated with each other and driven technically as those skilled in the art can sufficiently understand. The embodiments of the present disclosure may be carried out independently from each other, or may be carried out together in co-dependent relationship.

[0063] Hereinafter, embodiments of the present disclosure will be described in detail with reference to the accompanying drawings.

[0064] FIG. 1 is an exemplary diagram illustrating a configuration of an organic light emitting display apparatus according to the present disclosure. FIG. 2 is an exemplary diagram illustrating a configuration of one pixel of an organic light emitting display apparatus according to the present disclosure. FIG. 3 is an exemplary diagram illustrating a configuration of a controller applied to an organic light emitting display apparatus according to the present disclosure. FIG. 4 is an exemplary diagram illustrating a configuration of a data driver applied to an organic light emitting display apparatus according to the present disclosure.

[0065] The organic light emitting display apparatus according to the present disclosure, as illustrated in FIGS. 1 and 2, may include an organic light emitting display panel 100, a data driver, a gate driver 200, and a controller 400. The data driver may include at least one data driver integrated circuit (IC) 300.

[0066] In description below, a vertical blank period may denote a period between one frame and another frame. A frame may denote one image. Therefore, the vertical blank period may denote a period between periods where two different images are output.

[0067] One frame period may denote a period where one image is displayed and may include one vertical blank period. That is, one frame period may include a period where one image is displayed and the vertical blank period where no image is displayed. Herein, when the order of frame periods is needed, the terms "a first frame period" and "a second frame period" may be used, and when the order of frame periods is not needed, the term "one frame period" may be used.

[0068] Herein, a first one frame period may be defined as a first frame period, and a second one frame period may be defined as a second frame period. That is, the first frame period and the second frame period may be periods which are successively executed.

[0069] Moreover, herein, a mode which displays an image and then displays a black image during one frame period may be referred to as a black image mode. The black image mode may be used to solve a problem where an image is not clearly seen due to the delay of a motion picture response time (MPRT). In the black image mode, for example, only an image desired by a user may be displayed during a fore 1/2 period of one frame period, and during the other 1/2 period, a black image and an image may all be displayed.

[0070] Hereinafter, the elements may be sequentially described.

[0071] First, the organic light emitting display panel 100 may include a plurality of pixels which each include an organic light emitting diode OLED and a driving transistor for driving the organic light emitting diode OLED.

[0072] That is, as illustrated in FIG. 2, in the organic light emitting display panel 100, each of the plurality of pixels 110 may include the organic light emitting diode OLED and a pixel driving circuit PDC.

[0073] Moreover, in the organic light emitting display panel 100, a pixel area where each pixel 110 is provided may be defined, and a plurality of signal lines for providing a driving signal to the pixel driving circuit PDC may be provided.

[0074] The signal lines may include a gate line GL, a sensing pulse line SPL, a data line DL, a sensing line SL, a first driving power line PLA, and a second driving power line PLB.

[0075] A plurality of gate lines GL may be arranged in parallel at certain intervals in a first direction (for example, a widthwise direction) of the organic light emitting display panel 100.

[0076] A plurality of sensing pulse lines SPL may be arranged at certain intervals in parallel with the gate lines GL.

[0077] The data line DL may be provided in a second direction (for example, a lengthwise direction) of the organic light emitting display panel 100 to intersect the gate line GL and the sensing pulse line SPL, and the data line DL, the gate line GL, and the sensing pulse line SPL may be arranged in parallel at certain intervals. However, an arrangement structure of the data line DL and the gate line GL may be variously modified.

[0078] The sensing line SL may be spaced apart from the data line DL by a certain interval, and the sensing lines SL and the data lines DL may be arranged in parallel at certain intervals. However, the present disclosure is not limited thereto. For example, at least three pixels 110 may configure one unit pixel. In this case, one sensing line SL may be provided in the unit pixel. Therefore, when d (where d is an integer equal to or more than two) number of data lines DL1 to DLd in a horizontal line of the organic light emitting display panel 100, the number "k" of the sensing lines SL may be d/4. To provide an additional description, the data lines DL may be provided in the second direction (the lengthwise direction) of the organic light emitting display panel 100, the sensing lines SL may be provided in parallel with the data lines DL, and each of the sensing lines SL may be connected to at least three pixels 110 configuring each of unit pixels provided in one horizontal line.

[0079] The first driving power line PLA may be provided apart from the data line DL and the sensing line SL by a certain interval in parallel therewith. The first driving power line PLA may be connected to a power supply 500 and may transfer a first driving power EVDD, supplied from the power supply 500, to the pixel 110.

[0080] The second driving power line PBL may transfer a second driving power EVSS, supplied from the power supply 500, to the pixel 110.

[0081] The pixel driving circuit PDC may include a driving transistor Tdr which controls a current flowing in the organic light emitting diode OLED and a switching transistor Tswl connected between the data line DL, the driving transistor Tdr, and the gate line GL. Also, the pixel

driving circuit PDC included in each of the pixels 110 may include a capacitor Cst, connected between a first node n1 and a second node n2, and a sensing transistor Tsw2 for external compensation.

[0082] The switching transistor Tswl may be turned on by a gate pulse GP and may transfer a data voltage Vdata, supplied through the data line DL, to a gate of the driving transistor Tdr.

[0083] The sensing transistor Tsw2 may be turned on by a sensing pulse SP and may transfer a sensing voltage, supplied through the sensing line SL, to the second node n2 which is a source electrode of the driving transistor Tdr.

[0084] As the switching transistor Tswl is turned on, the capacitor Cst may be charged with a voltage supplied to the first node n1, and then, the driving transistor Tdr may be turned on with a charged voltage.

[0085] The driving transistor Tdr may be turned on with a voltage of the capacitor Cst and may control the amount of data current Ioled flowing from the first driving power line PLA to the organic light emitting diode OLED.

[0086] The organic light emitting diode OLED may emit light with the data current Ioled supplied from the driving transistor Tdr, and for example, may emit the light having luminance corresponding to the data current Ioled.

[0087] Hereinabove, a structure of the pixel 110 including the sensing line SL for performing the external compensation has been described with reference to FIG. 2, but in addition to the structure illustrated in FIG. 2, the pixel 110 may be provided in various structures including the sensing line SL.

[0088] For example, the external compensation may denote an operation of calculating a variation amount of a threshold voltage or mobility of the driving transistor Tdr provided in the pixel 110 and varying levels of data voltages supplied to the unit pixel on the basis of the variation amount. Therefore, in order to calculate the variation amount of the threshold voltage or mobility of the driving transistor Tdr, a structure of the pixel 110 may be changed to various structures. In this case, the sensing line SL should be provided.

[0089] Moreover, in order to perform the external compensation, a method of calculating the variation amount of the threshold voltage or mobility of the driving transistor Tdr by using the pixel 110 may be variously changed based on the structure of the pixel 110.

[0090] In this case, sensing for the external compensation may be performed on one gate line in one vertical blank period.

[0091] To provide an additional description, the present disclosure relates to an organic light emitting display apparatus which, when threshold voltages or mobility of driving transistors Tdr included in the organic light emitting display panel 100 are sensed, displays a black image along with the sensing during a vertical blank period, for the external compensation. Accordingly, the present disclosure does not directly relate to an external compensation method.

[0092] Therefore, a structure of each pixel for the external compensation may be implemented as various pixel structures proposed for the external compensation, and a method of performing the external compensation may be implemented as various external compensation methods.

[0093] That is, a detailed structure of each pixel for performing the external compensation and a detailed method for the external compensation are irrelevant to the scope of the present disclosure. Therefore, an example of a pixel for the external compensation has been simply described above with reference to FIG. 2, and an external compensation method will be simply described below.

[0094] Moreover, as described above, the present disclosure may use the black image mode. The structure of the pixel 110 with the black image mode applied thereto may be variously changed based on the black image mode, in addition to the structure illustrated in FIG. 2.

[0095] That is, FIG. 2 illustrates the structure of the pixel 110 for performing the external compensation and the black image mode, and thus, the structure of the pixel 110 may be changed to various structures, in addition to the structure illustrated in FIG. 2.

[0096] Hereinafter, an organic light emitting display apparatus based on the external compensation will be described as an example of the present disclosure.

[0097] Second, the gate driver 200 may sequentially supply the gate pulse GP to a plurality of gate lines GL1 to GLg by using gate control signals GCS transferred from the controller 400.

[0098] Here, the gate pulse GP may denote a signal for turning on the switching transistor Tsw1 connected to the gate lines GL1 to GLg. A signal for turning off the switching transistor Tswl may be referred to as a gate-off signal. A generic name for the gate pulse GP and the gate-off signal may be a gate signal.

[0099] The gate driver 200 may be provided independently from the organic light emitting display panel 100 and may be connected to the organic light emitting display panel 100 through a tape carrier package (TCP), a chip-on film (COF), or a flexible printed circuit board (FPCB), but is not limited thereto, and/or may be directly equipped in the organic light emitting display panel 100 by using a gate-in panel (GIP) type.

[0100] The gate driver 200 may output image gate pulses, which control outputs of image data voltages for displaying an image, to the gate lines included in the organic light emitting display panel in a first period of a first frame period.

[0101] The gate driver 200 may output the image gate pulses and black gate pulses for controlling outputs of black image data voltages for displaying a black image in a second period arriving after (subsequent to) the first period.

[0102] The gate driver 200 may output a sensing gate pulse to one gate line connected to driving transistors, of which characteristic variation is to be sensed, in a third

period after the second period of the first frame period until a first period of a second frame starts.

[0103] The image gate pulses, the black gate pulses, and the sensing gate pulses may be the gate pulses for turning on the switching transistor Tswl.

[0104] The black gate pulses may be output in a period from the second period of the first frame period to the first period of the second frame period.

[0105] The third period may correspond to the vertical blank period. A generic name for the first period and the second period may be a display period.

[0106] To this end, as illustrated in FIG. 1, the gate driver 200 may include a first driver 221 which generates the image gate pulses, the black gate pulses, and the sensing gate pulse by using first to eighth gate clocks transferred from the controller 400 in the first frame period, a second driver 222 which generates the image gate pulses, the black gate pulses, and the sensing gate pulse by using ninth to sixteenth gate clocks transferred from the controller 400 in the first frame period, and a third driver 210 which controls the first driver 221 and the second driver 222 to output the sensing gate pulse in the third period of the first frame period. In an exemplary embodiment the image gate pulses, the black gate pulses, and the sensing gate pulses may be identical.

[0107] The gate pulses may be output from the first driver 221 and the second driver 222. Therefore, the first driver 221 and the second driver 222 may be included in a gate pulse output unit 220.

[0108] A detailed configuration and function of the gate driver 200 will be described below in detail with reference to FIG. 5.

[0109] Third, the controller 400 may control the gate driver 200 and the data driver IC 300.

[0110] The controller 400, as illustrated in FIG. 3, may generate a gate control signal GCS for controlling driving of the gate driver 200 and a data control signal DCS for controlling driving of the data driver IC 300 by using a timing synchronization signal TSS output from an external system.

[0111] Moreover, in a sensing mode where sensing for the external compensation is performed, the controller 400 may transfer pieces of sensing image data, which are to be supplied to pixels connected to a gate line on which the external compensation is performed, to the data driver IC 300. Sensing for the external compensation may be performed at various timings. For example, sensing for the external compensation relevant to mobility variations of the driving transistors Tdr may be performed in the vertical blank period.

[0112] The controller 400 may calculate external compensation values on the basis of pieces of sensing data Sdata which are provided from the data driver after the sensing is performed in the vertical blank period and may store the external compensation values in a storage unit 450. The storage unit 450 may be included in the controller 400, or may be independently implemented outside the controller 400.

[0113] In a display period where an image is displayed, the controller 400 may compensate for pieces of input video data Ri, Gi, and Bi transferred from the external system by using the external compensation values to generate pieces of external compensation image data, or may not perform the external compensation on the input video data and may realign the pieces of input video data to generate and output pieces of normal image data. The data driver IC 300 may convert the pieces of external compensation image data or the pieces of normal image data into the data voltages Vdata and may supply the data voltages Vdata to the data lines DL1 to DLd.

[0114] In order to perform the above-described function, as illustrated in FIG. 3, the controller 400 may include a data aligner which realigns the pieces of input video data Ri, Gi, and Bi transferred from the external system by using the timing synchronization signal TSS transferred from the external system and supplies pieces of realigned image data to the data driver IC 300, a control signal generator 420 which generates the gate control signal GCS and the data control signal DCS by using the timing synchronization signal TSS, a calculator 410 which calculates an external compensation value for compensating for a characteristic variation of the driving transistor Tdr provided in each of the pixels 110 by using the pieces of sensing data Sdata transferred from the data driver IC 300, the storage unit 450 which stores the external compensation value, and an output unit 440 which outputs, to the data driver IC 300 or the gate driver 200, pieces of image data Data generated by the data aligner 430 and the gate control signal GCS and the data control signal DCS each generated by the control signal generator 200. The storage unit 450 may include the controller 400, and as illustrated in FIG. 3, may be implemented independently from the controller 400. The data aligner 430 may convert the pieces of input video data into the pieces of image data by using the external compensation value.

[0115] Particularly, the calculator 410 may set a gate line on which sensing is to be performed in one vertical blank period and may set a timing (hereinafter referred to as a sensing timing) at which the sensing is performed.

[0116] In this case, a timing at which the sensing is performed may be set differently for each gate line. However, all of the sensing timings may not differ in all of the gate lines. For example, at least two different sensing timings may be applied to the present disclosure.

[0117] The calculator 410 may control the control signal generator 420 so as to set a gate line on which the sensing is to be performed and may control the control signal generator 420 so as to set the sensing timing.

[0118] The control signal generator 420 may generate a line selection signal for setting a gate line on which the sensing is to be performed and may transfer the generated line selection signal to the gate driver 200, based on control by the calculator 410. Also, the control signal generator 420 may generate a reset signal for setting the sensing timing and may transfer the generated reset sig-

nal to the gate driver 200, based on control by the calculator 410.

[0119] The line selection signal and the reset signal may be included in the gate control signal GCS.

[0120] The control signal generator 420 may generate gate clocks used to generate the gate pulses and may transfer the generated gate clocks to the gate driver 200. The gate clocks may be included in the gate control signal GCS.

[0121] Fourth, the data driver may include at least one data driver IC 300. In FIG. 1, an organic light emitting display apparatus where two or more data driver ICs 300 are provided is illustrated as an example of the present disclosure.

[0122] The data driver IC 300 may be included in a COF 600 attached on the organic light emitting display panel 100. The COF 600 may be connected to a main board 700 including the controller 400. However, the data driver IC 300 may be directly equipped in the organic light emitting display panel 100.

[0123] Each of the data driver ICs 300 may be connected to corresponding data lines and sensing lines and may operate in a display mode, a black mode, and a sensing mode according to a control signal transferred from the controller 400.

[0124] The display mode may be a mode which displays an image and may be performed in the first period and the second period.

[0125] The black mode may be a mode which displays a black image and may be performed in the second period and the third period. Particularly, the black mode may be performed in a period from the second period of the first frame period to a portion of the first period of the second frame period, i.e. the black mode may be performed during a period including second and third periods of a frame period, and a part of a first period of a subsequent frame period.

[0126] The sensing mode may be a mode which senses mobility of the driving transistors and may be performed in the third period (i.e., the vertical blank period).

[0127] At least one data driver IC 300, as illustrated in FIG. 4, may include a data power supply unit 310 and a sensing unit 320. The data power supply unit 310 may be connected to the data lines DL, and the sensing unit 320 may be connected to the sensing lines SL.

[0128] The data power supply unit 310 may output the image data voltages to the data lines DL included in the organic light emitting display panel 100 in the first period, output the image data voltages or the black image data voltages in the second period, and output sensing image data voltages for outputting a sensing image or the black image data voltages in the third period.

[0129] For example, in the display mode (i.e., the first period and the second period), the data power supply unit 310 may convert the pieces of image data Data, supplied from the controller 400 by units of horizontal lines, into image data voltages and may supply the image data voltages to the data lines DL so as to display an image.

[0130] In the black mode (i.e., the second period, the third period, and a partial period of the first period arriving after (subsequent to) the third period), the data power supply unit 310 may convert the pieces of black image data, transferred from the controller 400, into black image data voltages and may supply the black image data voltages to the data lines connected to the data driver IC 300 so as to display a black image.

[0131] In the sensing mode (i.e., the third period), the data power supply unit 310 may convert the pieces of sensing image data, transferred from the controller 400, into sensing image data voltages and may supply the sensing image data voltages to the data lines connected to the data driver IC 300 so as to sense a variation amount of mobility of each of the driving transistors Tdr.

[0132] In the display mode, the sensing unit 320 may supply a voltage, needed for driving of the pixel driving circuit PDC, to the pixels 110 through the sensing lines SL.

[0133] In the black mode, the sensing unit 320 may supply a voltage, needed for driving of the pixel driving circuit PDC, to the pixels 110 through the sensing lines SL.

[0134] In the sensing mode, the sensing unit 320 may supply sensing voltages to sensing lines connected to the sensing unit 320, and then, may receive signals corresponding to the sensing voltages. The sensing unit 320 may convert the signals, representing variations of the mobility of the driving transistors Tdr included in the pixels 110 provided in one horizontal line, into the pieces of sensing data Sdata which are digital data. The sensing unit 320 may provide the pieces of sensing data Sdata to the controller 400. In this case, the controller 400 may calculate an external compensation value by using the pieces of sensing data Sdata.

[0135] FIG. 5 is an exemplary diagram illustrating a configuration of a gate pulse output unit of a gate driver applied to an organic light emitting display apparatus according to the present disclosure. FIG. 6 is an exemplary diagram illustrating a driving period of an organic light emitting display apparatus according to the present disclosure. FIG. 7 is an exemplary diagram showing waveforms of clocks applied to an organic light emitting display apparatus according to the present disclosure. FIG. 8 is an exemplary diagram showing gate pulses output from a gate driver in a second period of an organic light emitting display apparatus according to the present disclosure. FIG. 9 is an exemplary diagram showing gate pulses output from a gate driver in a third period of an organic light emitting display apparatus according to the present disclosure.

[0136] First, a configuration of the gate driver 200 will be described below.

[0137] As described above, the gate driver 200 may include the gate pulse output unit 220, including the first driver 221 and the second driver 222, and the third driver 210.

[0138] The gate pulse output unit 220 may be connect-

ed to the gate lines GL1 to GLg and may output the gate pulse GP to the gate lines GL1 to GLg.

[0139] The first driver 221 configuring the gate pulse output unit 220 may generate the image gate pulses, the black gate pulses, and the sensing gate pulse by using the first to eighth gate clocks CLK1 to CLK8 transferred from the controller 400 in the first frame period.

[0140] The second driver 222 configuring the gate pulse output unit 220 may generate the image gate pulses, the black gate pulses, and the sensing gate pulse by using the ninth to sixteenth gate clocks CLK9 to CLK16 transferred from the controller 400 in the first frame period.

[0141] The third driver 210 may control the first driver 221 and the second driver 222 to output the sensing gate pulse in the third period of the first frame period.

[0142] That is, the third driver 210 may select a sensing gate line, to which the sensing gate pulse is to be output, from among the gate lines according to the line selection signal LSP transferred from the controller 400.

[0143] Moreover, the third driver 210 may control the first driver 221 or the second driver 222 according to a reset signal RESET transferred from the controller 400 in order for the first driver 221 or the second driver 222 to output the sensing gate pulse to the sensing gate line.

[0144] The line selection signal LSP, as illustrated in FIGS. 6 and 7, may be transferred from the controller 400 to the gate driver 200 along with one of the gate clocks which are used in a display period DP including a first period A and a second period B.

[0145] The reset signal RESET, as illustrated in FIGS. 6 and 7, may be transferred from the controller 400 to the gate driver 200 in a sensing period SP corresponding to a third period C.

[0146] Hereinafter, a basic operation of outputting, by the organic light emitting display apparatus according to the present disclosure, gate pulses GP will be described with reference to FIG. 5. Particularly, the below-described gate pulses GP may be gate pulses used to display an image.

[0147] For example, as shown in FIG. 5, a gate pulse GP generated from a first gate clock CLK1 by a first stage ST1 may be output to a first gate line GL1, a gate pulse GP generated from a second gate clock CLK2 by a second stage ST2 may be output to a second gate line GL2, gate pulses GP generated from third to sixth gate clocks CLK3 to CLK6 by third to sixth stages ST3 to ST6 may be respectively output to third to sixth gate line GL3 to GL6, a gate pulse GP generated from a seventh gate clock CLK7 by a seventh stage ST7 may be output to a seventh gate line GL7, and a gate pulse GP generated from an eighth gate clock CLK8 by an eighth stage ST8 may be output to an eighth gate line GL8.

[0148] A gate pulse GP generated from the first gate clock CLK1 by a ninth stage ST9 may be output to a ninth gate line GL9, a gate pulse GP generated from the second gate clock CLK2 by a tenth stage ST10 may be output to a tenth gate line GL10, gate pulses GP generated from the third to sixth gate clocks CLK3 to CLK6 by eleventh to fourteenth stages ST11 to ST14 may be respectively output to eleventh to fourteenth gate line GL11 to GL14, a gate pulse GP generated from the seventh gate clock CLK7 by a fifteenth stage ST15 may be output to a fifteenth gate line GL15, and a gate pulse GP generated from the eighth gate clock CLK8 by a sixteenth stage ST16 may be output to a sixteenth gate line GL16.

[0149] A gate pulse GP generated from a ninth gate clock CLK9 by a seventeenth stage ST17 may be output to a seventeenth gate line GL17, a gate pulse GP generated from a tenth gate clock CLK10 by an eighteenth stage ST18 may be output to an eighteenth gate line GL18, gate pulses GP generated from eleventh to fourteenth gate clocks CLK11 to CLK14 by nineteenth to twenty-second stages ST19 to ST22 may be respectively output to nineteenth to twenty-second gate line GL19 to GL22, a gate pulse GP generated from a fifteenth gate clock CLK15 by a twenty-third stage ST23 may be output to a twenty-third gate line GL23, and a gate pulse GP generated from a sixteenth gate clock CLK16 by a twenty-fourth stage ST24 may be output to a twenty-fourth gate line GL24.

[0150] A gate pulse GP generated from the ninth gate clock CLK9 by a twenty-fifth stage ST25 may be output to a twenty-fifth gate line GL25, a gate pulse GP generated from the tenth gate clock CLK10 by a twenty-sixth stage ST26 may be output to a twenty-sixth gate line GL26, gate pulses GP generated from the eleventh to fourteenth gate clocks CLK11 to CLK14 by twenty-seventh to thirtieth stages ST27 to ST30 may be respectively output to twenty-seventh to thirtieth gate line GL27 to GL30, a gate pulse GP generated from the fifteenth gate clock CLK15 by a thirty-first stage ST31 may be output to a thirty-first gate line GL31, and a gate pulse GP generated from the sixteenth gate clock CLK16 by a thirty-second stage ST32 may be output to a thirty-second gate line GL32.

[0151] Each of the stages may generate the image gate pulse, the black gate pulse, and the sensing gate pulse by using the gate control signal.

[0152] That is, as shown in FIG. 5, the gate pulses GP output to the first to sixteenth gate lines GL1 to GL16 may be generated from the first to eighth gate clocks CLK1 to CLK8 by the first driver 221, and the gate pulses GP output to the seventeenth to thirty-second gate lines GL17 to GL32 may be generated from the ninth to sixteenth gate clocks CLK9 to CLK16 by the second driver 222.

[0153] Therefore, a driver for outputting the gate pulses may be changed by units of sixteen gate pulses. Hereinafter, such a feature may be expressed as 16 periods.

[0154] Moreover, the same functions may be repeated at a period corresponding to 32 gate pulses. Hereinafter, such a feature may be expressed as 32 periods.

[0155] Therefore, for example, when the number of gate lines is 2,160, a period where 2,160 gate pulses are output may be expressed as 32n+16(Y). Here, n may be

a natural number equal to or less than 67. For example, when the number of gate lines is 2,160, 32 periods may be repeated 67 times, and when 16 periods are performed once, the gate pulses may be output to all of the 2,160 gate lines.

[0156] That is, the display period including the first period A and the second period B of one frame period may be expressed as 32n+16(Y), and in the display period A and B, the image gate pulses for displaying an image I may be output to the gate lines on the basis of the above-described method.

[0157] In this case, after the gate pulses are output from the first driver 221, the first driver 221 may not output the gate pulses during 16 periods, and when the 16 periods elapse, the first driver 221 may again output the gate pulses.

[0158] Moreover, after the gate pulses are output from the second driver 222, the second driver 222 may not output the gate pulses during 16 periods, and when the 16 periods elapse, the second driver 222 may again output the gate pulses.

[0159] The one frame period (i.e., a period corresponding to a sum of the first period A, the second period B, and the third period C) may be set to 32m periods. Here, m may be a natural number more than n.

[0160] However, the above-described periods (i.e., 16 periods, 32 periods, 32n+16 periods, and 32m periods) are merely an example for describing the present disclosure, and the present disclosure is not limited thereto. That is, the periods may be variously changed.

[0161] Hereinafter, a method of outputting, by the organic light emitting display apparatus according to the present disclosure, image gate pulses IGP and black gate pulses BGP in the second period B will be described with reference to FIGS. 5 to 8.

[0162] As described above, the first driver 221 and the second driver 222 may repeatedly output the image gate pulses at every 16 periods.

[0163] In this case, as shown in FIG. 8, an interval between a fourth image gate pulse and a fifth image gate pulse of first to eighth image gate pulses IGP output from the first driver 221 may be set to be greater than an interval between other image gate pulses. To this end, as shown in FIG. 7, an interval between a fourth gate clock CLK4 and a fifth gate clock CLK5 of first to eighth gate clocks CLK1 to CLK8 used by the first driver 221 may be set to be greater than an interval between other gate clocks.

[0164] Moreover, as shown in FIG. 8, an interval between a twentieth image gate pulse and a twenty-first image gate pulse of seventeenth to twenty-fourth image gate pulses IGP output from the second driver 222 may be set to be greater than an interval between other image gate pulses. To this end, as shown in FIG. 7, an interval between a twelfth gate clock CLK12 and a thirteenth gate clock CLK13 of ninth to sixteenth gate clocks CLK9 to CLK16 used by the first driver 221 may be set to be greater than an interval between other gate clocks.

[0165] In the present disclosure, the black gate pulse BGP for displaying the black image may be output during a period corresponding to the interval between the fourth image gate pulse and the fifth image gate pulse. The black gate pulse BGP may be generated by a combination of the gate clocks, or may be generated by other gate clocks.

[0166] In this case, the black gate pulse BGP may be simultaneously output to eight gate lines. Therefore, switching transistors respectively connected to the eight gate lines may be simultaneously turned on, and thus, black image data voltages may be simultaneously supplied to data lines respectively connected to the switching transistors.

[0167] Therefore, as shown in FIG. 6, pixels corresponding to the eight gate lines may simultaneously display a black image BI.

[0168] The second driver 222 may simultaneously output the black gate pulses BGP to the eight gate lines. Therefore, pixels corresponding to the eight gate lines connected to the second driver 222 may simultaneously display a black image.

[0169] In this case, as shown in FIG. 8, the black gate pulse BGP may be output to the gate lines in a first sleeping period 1SLP where the first driver 221 does not output the image gate pulses IGP and a second sleeping period 2SLP where the second driver 222 does not output the image gate pulses IGP.

[0170] For example, FIG. 8 shows the second period B of the display period. In the second period B, image data voltages and black image data voltages may be output to the organic light emitting display panel 100, and to this end, as shown in FIG. 8, the image gate pulses IGP and the black gate pulses BGP may be output to the gate lines. The second period B, as shown in FIG. 6, may start from a time when 32k+16(X) periods elapse. Here, k may be a natural number less than n.

[0171] In the second period B, for example, as shown in FIG. 8, the first driver 221 may sequentially output the image gate pulses IGP to the gate lines during first 16 periods, the second driver 222 may sequentially output the image gate pulses IGP to the gate lines during second 16 periods, the first driver 221 may sequentially output the image gate pulses IGP to the gate lines during third 16 periods, and the second driver 222 may sequentially output the image gate pulses IGP to the gate lines during fourth 16 periods.

[0172] In this case, a period until the first driver 221 outputs the image gate pulses IGP again after outputting the image gate pulses IGP may be referred to as a first sleeping period 1SLP, and a period until the second driver 222 outputs the image gate pulses IGP again after outputting the image gate pulses IGP may be referred to as a second sleeping period 2SLP.

[0173] In the present disclosure, the black gate pulses BGP may be output in the first sleeping period 1SLP and the second sleeping period 2SLP of the second period B. That is, the black gate pulses BGP may be output in

the first sleeping period 1SLP and the second sleeping period 2SLP of the second period B.

[0174] To provide an additional description, in the first period A of the display period DP, only the image gate pulse IGP shown in FIG. 8 may be output to the gate lines, and thus, the image I may be displayed by the organic light emitting display panel 100.

[0175] In the second period B of the display period DP, as shown in FIG. 8, after the image gate pulses IGP are output from the first driver 221, the black gate pulses may be output from the first driver 221 in the first sleeping period 1SLP, and after the image gate pulses IGP are output from the second driver 222, the black gate pulses may be output from the second driver 222 in the second sleeping period 2SLP, whereby the organic light emitting display panel 100 may display black images BI in a type illustrated in FIG. 6.

[0176] Finally, a method of outputting, by the organic light emitting display apparatus according to the present disclosure, black gate pulses BGP and sensing gate pulses in the third period C will be described with reference to FIGS. 5 to 9.

[0177] As described above, the black gate pulses BGP may be output in the first sleeping period 1SLP and the second sleeping period 2SLP of the second period B, and the image gate pulses IGP may be output in periods other than the first sleeping period 1SLP and the second sleeping period 2SLP of the second period B.

[0178] In this case, the sensing gate pulses may be output in the first sleeping period 1SLP and the second sleeping period 2SLP of the third period C, and the black gate pulses BGP may be output in periods other than the first sleeping period 1SLP and the second sleeping period 2SLP of the third period C.

[0179] In the third period C, for example, as shown in FIG. 9, the first driver 221 may sequentially output the black gate pulses BGP to the gate lines during first 16 periods, the second driver 222 may sequentially output the black gate pulses BGP to the gate lines during second 16 periods, the first driver 221 may sequentially output the black gate pulses BGP to the gate lines during third 16 periods, and the second driver 222 may sequentially output the black gate pulses BGP to the gate lines during fourth 16 periods.

[0180] In this case, a period until the first driver 221 outputs the black gate pulses BGP again after outputting the black gate pulses BGP may be referred to as a first sleeping period 1SLP, and a period until the second driver 222 outputs the black gate pulses BGP again after outputting the black gate pulses BGP may be referred to as a second sleeping period 2SLP.

[0181] In the present disclosure, the sensing gate pulses may be output in the first sleeping period 1SLP and the second sleeping period 2SLP of the third period C.

[0182] To provide an additional description, in the present disclosure, the first driver 221 and the second driver 222 may be driven at 16 periods, and thus, there may be periods (i.e., the first sleeping period 1SLP and the second sleeping period 2SLP) where the first driver 221 is not driven.

[0183] In this case, only the image gate pulses IGP may be output in the first period A, and thus, specific signals may not be output in the first sleeping period 1SLP and the second sleeping period 2SLP.

[0184] In the second period B, the black gate pulses BGP as well as the image gate pulses IGP may be output. Therefore, in the present disclosure, the black gate pulses BGP may be output in the first sleeping period 1SLP and the second sleeping period 2SLP of the second period B, and in the other periods, the image gate pulses IGP may be output.

[0185] In the third period C, the image gate pulses IGP may not be output, and the black gate pulses BGP and the sensing gate pulses may be output. Therefore, in the present disclosure, the sensing gate pulses may be output in the first sleeping period 1SLP and the second sleeping period 2SLP of the third period C, and in the other periods, the black gate pulses BGP may be output.

[0186] Here, all periods of the first sleeping period 1SLP and all periods of the second sleeping period 2SLP may not be used as a period (i.e., a sensing-enabled period) where the sensing gate pulses are output.

[0187] That is, a period capable of being used as the sensing-enabled period in the first sleeping period 1SLP and the second sleeping period 2SLP is not limited, and a timing of the sensing-enabled period may be set differently for each gate line.

[0188] For example, a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse BGP is output in the third period C of the first frame period may differ from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse BGP is output in the third period C of the second frame period. This will be described below in detail with reference to FIG. 10.

[0189] The structure and configuration of the gate driver 200 described above with reference to FIGS. 5 to 9 have been described above as an example of the present disclosure, and thus, the present disclosure is not limited thereto. That is, the structure and configuration of the gate driver 200 may be changed to various types for performing the above-described function.

[0190] FIG. 10 is an exemplary diagram showing a third period of an organic light emitting display apparatus according to the present disclosure, and particularly, is an exemplary diagram showing different sensing-enabled periods in a sleeping period. Hereinafter, a driving method of the organic light emitting display apparatus according to the present disclosure will be described with reference to FIGS. 1 to 10. In the following description, description which is the same as or similar to the above description is omitted or will be simply given.

[0191] First, in the first period A of the first frame period, the gate driver 200 may output image gate pulses, which control outputs of image data voltages for displaying the image I, to the gate lines included in the organic light

emitting display panel 100.

[0192] In this case, the first driver 221 may generate image gate pulses IGP by using the first to eighth gate clocks transferred from the controller 400 and may output the generated image gate pulses IGP to sixteen gate lines.

[0193] The second driver 222 may generate image gate pulses IGP by using the ninth to sixteenth gate clocks transferred from the controller 400 and may output the generated image gate pulses IGP to sixteen other gate lines.

[0194] The third driver 210 may select a sensing gate line, to which the sensing gate pulse is to be output in the third period C, from among the gate lines according to the line selection signal LSP transferred from the controller 400.

[0195] The controller 400 may convert pieces of input video data into pieces of image data and may transfer the pieces of image data to the data driver IC 300.

[0196] Particularly, the controller 400 may output the line selection signal LSP to the third driver 210 at a timing at which a gate clock corresponding to an image gate pulse output to the sensing gate line in the first period A of the first frame period among the gate clocks CLK1 to CLK16 is output to the first driver 221 or the second driver 222.

[0197] The third driver 210 may store the line selection signal LSP received in the first period A. The line selection signal LSP may include information about a sensing gate line on which sensing is performed in the third period C.

[0198] The data driver IC 300 may convert the pieces of image data, transferred from the controller 400, into the image data voltages.

[0199] The data driver IC 300 may output the image data voltages to the data lines in a period where the image gate pulse IGP is supplied to the gate line.

[0200] Therefore, as shown in FIG. 6, the image I may be displayed by the organic light emitting display panel 100 in the period A.

[0201] Subsequently, in the second period B of the first frame period, the gate driver 200 may output, to the gate lines included in the organic light emitting display panel 100, image gate pulses IGP for controlling outputs of image data voltages used to output an image I and black gate pulses BGP for controlling outputs of black image data voltages used to output a black image I.

[0202] That is, the gate driver 200 may output the image gate pulses IGP and the black gate pulses BGP to the gate lines by using a method described above with reference to FIG. 8.

[0203] A function of outputting, by the controller 400, the line selection signal LSP to the third driver 210 may be performed in the second period B as well as the first period A.

[0204] For example, when an image gate pulse output to a sensing gate line on which sensing is to be performed in the third period C is output to the sensing gate line in the second period B, the controller 400 may output the line selection signal LSP to the third driver 210 at a timing at which a gate clock corresponding to an image gate pulse among the gate clocks CLK1 to CLK16 is output to the first driver 221 or the second driver 222 in the second period B.

[0205] The third driver 210 may store the line selection signal LSP received in the second period B. The line selection signal LSP may include information about a sensing gate line on which sensing is performed in the third period C.

[0206] In the first frame period, the line selection signal LSP may be transferred to the third driver 210 only once.

[0207] That is, since sensing is performed on one sensing gate line in the third period C, the line selection signal LSP may be transferred to the third driver 210 in the first frame period only once.

[0208] In the second period B, the controller 400 may generate pieces of image data corresponding to the image I and pieces of black image data corresponding to the black image BI and may transfer the generated image data and black image data to the data driver IC 300.

[0209] The pieces of black image data may be stored in the storage unit 450, and then, may be transferred to the data driver IC 300.

[0210] The data driver IC 300 may convert the pieces of image data into image data voltages and may convert the pieces of black image data into black image data voltages.

[0211] The data driver IC 300 may output the image data voltages to the data lines in a period where the image gate pulse IGP is supplied to the gate line and may output the black image data voltages to the data lines in a period where the black gate pulse BGP is supplied to the gate line.

[0212] Therefore, in the second period B, as shown in FIG. 6, the image I and the black image BI may be displayed by the organic light emitting display panel 100.

[0213] Finally, in the third period C after the second period B of the first frame period until the first period A of the second frame starts, the gate driver 200 may output the black gate pulses BGP, which control outputs of the black image data voltages used to display the black image BI, to the gate lines included in the organic light emitting display panel 100.

[0214] Moreover, in the first sleeping period 1SLP or the second sleeping period 2SLP, the gate driver 200 may output a sensing gate pulse to one gate line (i.e., a sensing gate line) connected to driving transistors on which characteristic variation is to be sensed (i.e., sensing is to be performed).

[0215] The third driver 210 may control the first driver 221 or the second driver 222 in the third period C in order for the sensing gate pulse to be output.

[0216] Particularly, the third driver 310 may control the first driver 221 or the second driver 222 according to a reset signal RESET transferred from the controller 400 so that the first driver 221 or the second driver 222 outputs the sensing gate pulse to the sensing gate line.

[0217] When the sensing gate pulse is output from the first driver 221, the controller 400 may select, as a sensing-enabled period SPP, one period of a first sleeping period 1SLP until the second driver 222 outputs black gate pulses after the first driver 221 is driven for outputting the black gate pulses and the first driver 221 is again driven for outputting the black gate pulses, in the third period C, and may transfer the reset signal RESET, indicating the start of the sensing-enabled period SPP, to the third driver 210.

[0218] The third driver 210 may control the first driver 221 or the second driver 222 according to the reset signal RESET transferred from the controller 400. That is, the third driver 210 may store information about a sensing gate line on which the sensing is to be performed, based on the line selection signal LSP transferred in the first period A or the second period B. In the third period C, when the reset signal RESET is received, the third driver 210 may transfer the reset signal RESET to one, connected to the sensing gate line, of the first driver 221 and the second driver 222.

[0219] The reset signal RESET may be supplied to a stage which outputs a sensing gate pulse to the sensing gate line. The stage which has received the reset signal RESET may output the sensing gate pulse to the sensing gate line at a start timing of the sensing-enabled period SPP.

[0220] When the sensing gate pulse is output from the second driver 222, the controller 400 may select, as a sensing-enabled period SPP, one period of a second sleeping period 2SLP until the first driver 221 outputs black gate pulses after the second driver 222 is driven for outputting the black gate pulses and the second driver 222 is again driven for outputting the black gate pulses, in the third period C, and may transfer the reset signal RESET, indicating the start of the sensing-enabled period SPP, to the third driver 210.

[0221] The third driver 210 may control the first driver 221 or the second driver 222 according to the reset signal RESET transferred from the controller 400. That is, the third driver 210 may store information about a sensing gate line on which the sensing is to be performed, based on the line selection signal LSP transferred in the first period A or the second period B. In the third period C, when the reset signal RESET is received, the third driver 210 may transfer the reset signal RESET to one, connected to the sensing gate line, of the first driver 221 and the second driver 222.

[0222] The reset signal RESET may be supplied to a stage which outputs a sensing gate pulse to the sensing gate line. The stage which has received the reset signal RESET may output the sensing gate pulse to the sensing gate line at a start timing of the sensing-enabled period SPP.

[0223] In the third period C, the controller 400 may generate pieces of black image data corresponding to the black image BI and pieces of sensing image data corresponding to the sensing image and may transfer the generated black image data and sensing image data to the data driver IC 300.

[0224] The data driver IC 300 may convert the pieces of black image data into black image data voltages and may convert the pieces of sensing image data into sensing image data voltages.

[0225] The data driver IC 300 may output the black image data voltages to the data lines in a period where the black gate pulse BGP is supplied to the gate line and may output the sensing image data voltages to the data lines in a period where the sensing gate pulse is supplied to the gate line.

[0226] Therefore, in the third period C, the organic light emitting display panel 100 may display the black image BI and the sensing image. In this case, variation amounts of mobility of driving transistors Tdr included in pixels connected to the sensing gate lines may be sensed based on the sensing image data voltages. External compensation values may be calculated based on the variation amounts of mobility and may be used in a second frame or frames subsequent thereto.

[0227] As described above, a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse BGP is output in the third period C of the first frame period may differ from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse BGP is output in the third period C of the second frame period.

[0228] For example, in FIG. 10, with respect to line E-E', a left portion represents the second period B, and a right portion represents the third period C.

[0229] Moreover, in FIG. 10, the ordinate axis denotes the gate clocks or the gate lines. Also, in FIG. 10, with respect to line D-D', a left portion represents black gate pulses which are output according to initial driving of the first driver 221 and the second driver 222, and a right portion represents black gate pulses which are output according to second driving of the first driver 221 and the second driver 222.

[0230] For example, as illustrated in the left ordinate axis and a left portion with respect to line D-D' in FIG. 10, black gate pulses may be output to first to sixteenth gate lines according to first to eighth gate clocks CLK1 to CLK8 used in the first driver 221, and black gate pulses may be output to seventeenth to thirty-second gate lines according to ninth to sixteenth gate clocks CLK9 to CLK16 used in the second driver 222.

[0231] After the black gate pulses are output to the sixteenth gate line, as illustrated in a right portion with respect to line D-D', black gate pulses may be output to thirty-third to forty-eighth gate lines according to the first to eighth gate clocks CLK1 to CLK8 used in the first driver 221, and black gate pulses may be output to forty-ninth to sixty-fourth gate lines according to the ninth to sixteenth gate clocks CLK9 to CLK16 used in the second driver 222.

[0232] Moreover, in FIG. 10, the abscissa axis represents time. In FIG. 10, one tetragon is represented by a

number, and the number may denote time or may denote a gate line. For convenience of description, in FIG. 10, the number is illustrated along with H. Here, H may denote time. In other words, the time is given in units of H.

[0233] As described above, the first driver 221 or the second driver 222 may simultaneously output the black gate pulses BGP to eight gate lines. Therefore, in FIG. 10, eight black gate pulses simultaneously output to eight gate lines are represented as a group.

[0234] For example, black gate pulses output at 5H of the abscissa axis in FIG. 10 are illustrated as a first black gate pulse group 1BGPG, black gate pulses output at 15H are illustrated as a second black gate pulse group 2BGPG, black gate pulses output at 25H are illustrated as a third black gate pulse group 3BGPG, and black gate pulses output at 35H are illustrated as a fourth black gate pulse group 4BGPG.

[0235] Moreover, in FIG. 10, each of regions illustrated by V represents a region which is driven for outputting a black gate pulse to a gate line connected to each of stages of the first driver 221 or the second driver 222, and each of regions illustrated by W represents a region which is driven for generating signals needed for a previous stage or a next stage with respect to each of stages of the first driver 221 or the second driver 222.

[0236] That is, in FIG. 10, a region illustrated by V and W represents a period where the first driver 221 and the second driver 222 are driven, and a region which is not illustrated by V and W represents a period where the first driver 221 and the second driver 222 are not driven.

[0237] As described above, a first sleeping period 1SLP may denote a period until the second driver 222 outputs black gate pulses after the first driver 221 is driven for outputting the black gate pulses BGP and the first driver 221 is again driven for outputting the black gate pulses, in the third period C.

[0238] A second sleeping period 2SLP may denote a period until the first driver 221 outputs black gate pulses after the second driver 222 is driven for outputting the black gate pulses BGP and the second driver 222 is again driven for outputting the black gate pulses, in the third period C.

[0239] In this case, as shown in FIG. 10, there may be regions illustrated by W in the first sleeping period 1SLP and the second sleeping period 2SLP.

[0240] As described above, the region illustrated by W may denote a region where the first driver 221 and the second driver 222 are driven for outputting black gate pulses BGP.

[0241] A sensing gate pulse may not be output while the first driver 221 and the second driver 222 are being driven for outputting the black gate pulses.

[0242] Therefore, in the present disclosure, the controller 400 may select, as a sensing-enabled period SPP, one period from among the first sleeping period 1SLP and the second sleeping period 2SLP and may transfer the reset signal RESET, indicating the start of the sensing-enabled period SPP, to the third driver 210. Also, the third driver 210 may control the first driver 221 or the second driver 222 according to the reset signal RESET, and the first driver 221 or the second driver 222 may output the sensing gate pulse to the gate line at a timing corresponding to the reset signal RESET.

[0243] For example, in FIG. 10, a sensing gate pulse may be output to first and second gate lines at a timing 20H, a sensing gate pulse may be output to third and fourth gate lines at a timing 21H, a sensing gate pulse may be output to fifth and sixth gate lines at a timing 22H, and a sensing gate pulse may be output to seventh and eighth gate lines at a timing 25H.

[0244] In this case, it may be seen that a timing, at which the sensing gate pulse is output after a black gate pulse is output from a corresponding gate line, is set differently for each gate line.

[0245] That is, a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse is output in the third period C of one frame period may differ from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse is output in the third period C of one other frame period.

[0246] To provide an additional description, only one sensing gate pulse may be output in the third period C of one frame period, and a time, at which the sensing gate pulse is output after the black gate pulse is output in the third period C of one other frame period, may be set differently for each gate line.

[0247] However, the timing may not be set differently in all gate lines, and the above-described patterns may be repeated at certain periods.

[0248] In the present disclosure, the controller 400 may store pieces of information about timings shown in FIG. 10.

[0249] Therefore, the controller 400 may set a timing at which the sensing-enabled period SPP starts, based on the pieces of information about the timings and a sensing gate line on which sensing is to be performed, and may output the reset signal RESET to the third driver 210 according to the timing.

[0250] According to the present disclosure, a timing at which black image data voltages for outputting a black image are supplied to a panel and a timing at which sensing image data voltages for outputting a sensing image are supplied to the panel may be differently set, and thus, a function of outputting the black image and a function of sensing a driving transistor may all be performed in the vertical blank period.

[0251] The above-described feature, structure, and effect of the present disclosure are included in at least one embodiment of the present disclosure, but are not limited to only one embodiment. Furthermore, the feature, structure, and effect described in at least one embodiment of the present disclosure may be implemented through combination or modification of other embodiments by those skilled in the art. Therefore, content associated with the combination and modification should be construed as being within the scope of the present disclosure.

[0252] It will be apparent to those skilled in the art that various modifications and variations can be made in the present disclosure without departing from the scope of the disclosure. Thus, it is intended that the present disclosure covers the modifications and variations of this disclosure provided they come within the scope of the appended claims.

Claims

1. An organic light emitting display apparatus comprising:

an organic light emitting display panel (100) including a plurality of pixels (110) each including an organic light emitting diode (OLED) and a driving transistor (Tdr) for driving the organic light emitting diode (OLED);
a gate driver (200) configured to output image gate pulses (IGP), which control outputs of image data voltages used to display an image, to gate lines (GL1, ..., GLg) included in the organic light emitting display panel (100) in a first period (A) of a first frame period, to output the image gate pulses (IGP) and black gate pulses (BGP) for controlling outputs of black image data voltages used to display a black image in a second period (B) subsequent to the first period (A), and to output a sensing gate pulse to one gate line (GL1, ..., GLg) connected to driving transistors (Tdr), of which characteristic variation is to be sensed, in a third period (C) subsequent to the second period (B) until a first period (A) of a second frame starts;
a data driver (300) configured to output data voltages to data lines (DL1, ..., DLd) included in the organic light emitting display panel (100); and
a controller (400) configured to control the gate driver (200) and the data driver (300).

2. The organic light emitting display apparatus of claim 1,
wherein the gate driver (200) comprises:

a first driver (221) configured to generate the image gate pulses (IGP), the black gate pulses (BGP), and the sensing gate pulse by using a first predetermined number of gate clocks (CLK1, ..., CLK8) transferred from the controller (400) in the first frame period, optionally by using first to eighth gate clocks (CLK1, ..., CLK8) transferred from the controller (400) in the first frame period;
a second driver (222) configured to generate the image gate pulses (IGP), the black gate pulses (BGP), and the sensing gate pulse by using a second predetermined number of gate clocks (CLK9, ..., CLK16) transferred from the controller (400) in the first frame period, optionally by using ninth to sixteenth gate clocks (CLK9, ..., CLK16) transferred from the controller (400) in the first frame period; and
a third driver (210) configured to control the first driver (221) and the second driver (222) to output the sensing gate pulse in a third period (C) of the first frame period.

3. The organic light emitting display apparatus of claim 2, wherein the third driver (210) is configured to select a sensing gate line, to which the sensing gate pulse is to be output, from among the gate lines (GL1, ..., GLg) according to a line selection signal (LSP) transferred from the controller (400) and to control the first driver (221) or the second driver (222) according to a reset signal (RESET) transferred from the controller (400) so that the first driver (221) or the second driver (222) outputs the sensing gate pulse to the sensing gate line.

4. The organic light emitting display apparatus of claim 3, wherein the controller (400) is configured to output the line selection signal (LSP) to the third driver (210) at a timing at which a gate clock, corresponding to an image gate pulse (IGP) output to the sensing gate line in the first period (A) or the second period (B) of the first frame period, of the gate clocks is output to the first driver (221) or the second driver (222).

5. The organic light emitting display apparatus of claim 3 or 4, wherein the controller (400) is configured to select, as a sensing-enabled period (SSP), when the sensing gate pulse is output from the first driver (221), one period of a first sleeping period (1SLP) and to transfer the reset signal (RESET), indicating the start of the sensing-enabled period (SSP), to the third driver (210), and
wherein the first sleeping period (1SLP) is a period between a period where the second driver (221) outputs black gate pulses (BGP) after the first driver (221) is driven for outputting the black gate pulses (BGP) and a period where the first driver (221) is again driven for outputting the black gate pulses (BGP), in the third period (C).

6. The organic light emitting display apparatus of any one of claims 3 to 5, wherein the controller (400) is configured to select, as a sensing-enabled period (SSP), when the sensing gate pulse is output from the second driver (222), one period of a second sleeping period (2SLP) and to transfer the reset signal (RESET), indicating the start of the sensing-enabled period (SSP), to the third driver (210), and
wherein the second sleeping period (2SLP) is a period between a period where the first driver (221) outputs black gate pulses (BGP) after the second

driver (222) is driven for outputting the black gate pulses (BGP) and a period where the second driver (222) is again driven for outputting the black gate pulses (BGP), in the third period (C).

7. The organic light emitting display apparatus of any one of claims 2 to 6, wherein the first driver (221) and/or the second driver (222) are/is configured to simultaneously output the black gate pulses (BGP) to eight gate lines (GL1, ..., GLg).

8. The organic light emitting display apparatus of any one of claims 2 to 7, wherein
the first driver (221) is configured to generate the image gate pulses (IGP) by using first to eighth gate clocks (CLK1, ..., CLK8), and
the second driver (222) is configured to generate the image gate pulses (IGP) by using ninth to sixteenth gate clocks (CLK9, ..., CLK16).

9. The organic light emitting display apparatus of claim 8, wherein
an interval between a fourth image gate pulse (IGP) and a fifth image gate pulse (IGP) each output from the first driver (221) is greater than an interval between other image gate pulses (IGP) output from the first driver (221), and
an interval between a twelfth image gate pulse (IGP) and a thirteenth image gate pulse (IGP) each output from the second driver (222) is greater than an interval between other image gate pulses (IGP) output from the second driver (222).

10. The organic light emitting display apparatus of claim 8 or 9, wherein
the first driver (221) is configured to output the black gate pulse (BGP) in a period between a period where the fourth gate clock (CLK4) is output and a period where the fifth gate clock (CLK5) is output, and
the second driver (222) is configured to output the black gate pulse (BGP) in a period between a period where the twelfth gate clock (CLK12) is output and a period where the thirteenth gate clock (CLK13) is output.

11. The organic light emitting display apparatus of any one of claims 2 to 10, wherein the first driver (221) and the second driver (222) are configured to alternately output sixteen image gate pulses (IGP).

12. The organic light emitting display apparatus of any one of claims 2 to 11, wherein the first driver (221) and the second driver (222) are configured to repeatedly perform the same function at a period corresponding to thirty-two image gate pulses (IGP).

13. The organic light emitting display apparatus of any one of claims 2 to 12, wherein
when the first driver (221) and the second driver (222) are configured to alternately output sixteen image gate pulses (IGP), the first driver (221) and the second driver (222) are configured to repeatedly perform the same function at a period corresponding to thirty-two image gate pulses (IGP), and the number of the gate lines (GL1, ..., GLg) is 2,160,
a period where the gate pulses (GP) are output is expressed as 32n+16, where n is a natural number equal to or less than 67, and when n is 67, all of 2,160 gate pulses (GP) are output.

14. The organic light emitting display apparatus of claim 13, wherein
the first driver (221) is configured to output sixteen image gate pulses (IGP) by using the first to eighth gate clocks (CLK1, ..., CLK8),
the second driver (222) is configured to output sixteen image gate pulses (IGP) by using the ninth to sixteenth gate clocks (CLK9, ..., CLK16), after the first driver (221) outputs the sixteen image gate pulses (IGP),
the first driver (221) is configured to output sixteen other image gate pulses (IGP) by using the first to eighth gate clocks (CLK1, ..., CLK8), after the second driver (222) outputs the sixteen image gate pulses (IGP), and
the second driver (222) is configured to output sixteen other image gate pulses (IGP) by using the ninth to sixteenth gate clocks (CLK9, ..., CLK 16), after the first driver (221) outputs the sixteen other image gate pulses (IGP).

15. The organic light emitting display apparatus of any one of claims 1 to 14, wherein the data driver (300) is configured to output the image data voltages in the first period (A), to output the image data voltages or the black image data voltages in the second period (B), and to output sensing image data voltages for displaying a sensing image or the black image data voltages in the third period (C).

16. The organic light emitting display apparatus of any one of claims 1 to 15, wherein the black gate pulses (BGP) are output in a period from the second period (B) of the first frame period to a partial period of the first period (A) of the second frame period.

17. The organic light emitting display apparatus of any one of claims 1 to 16, wherein a period until the sensing gate pulse is output to a sensing gate line after the black gate pulse (BGP) is output in the third period (C) of the first frame period differs from a period until the sensing gate pulse is output to another sensing gate line after the black gate pulse (BGP) is output in a third period (C) of the second frame period.

FIG. 1

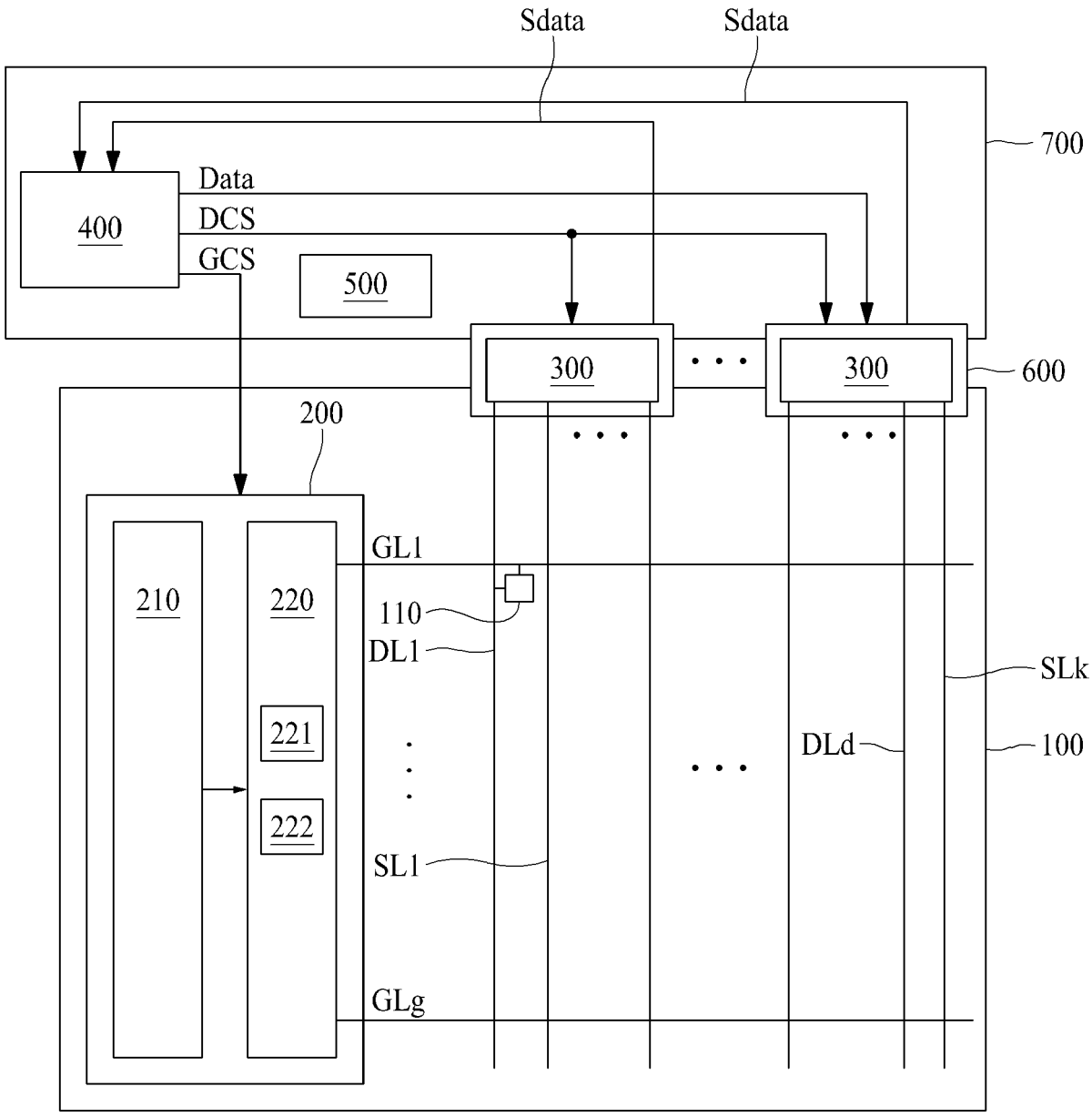

Sdata
Sdata
700
400
Data
DCS
GCS
500
300
300
600
200
210
220
221
222
GL1
110
DL1
SL1
GLg
SLk
DLd
100

FIG. 2

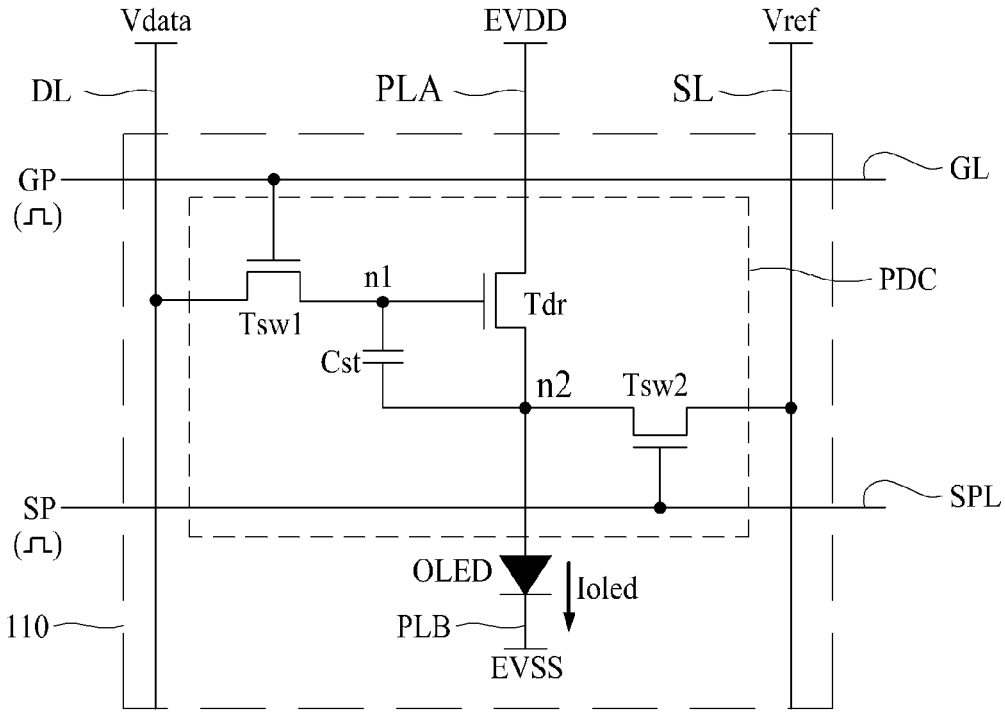

Vdata
EVDD
Vref
DL
PLA
SL
GP
GL
n1
PDC
Tsw1
Tdr
Cst
n2
Tsw2
SP
SPL
OLED
Ioled
110
PLB
EVSS

FIG. 3

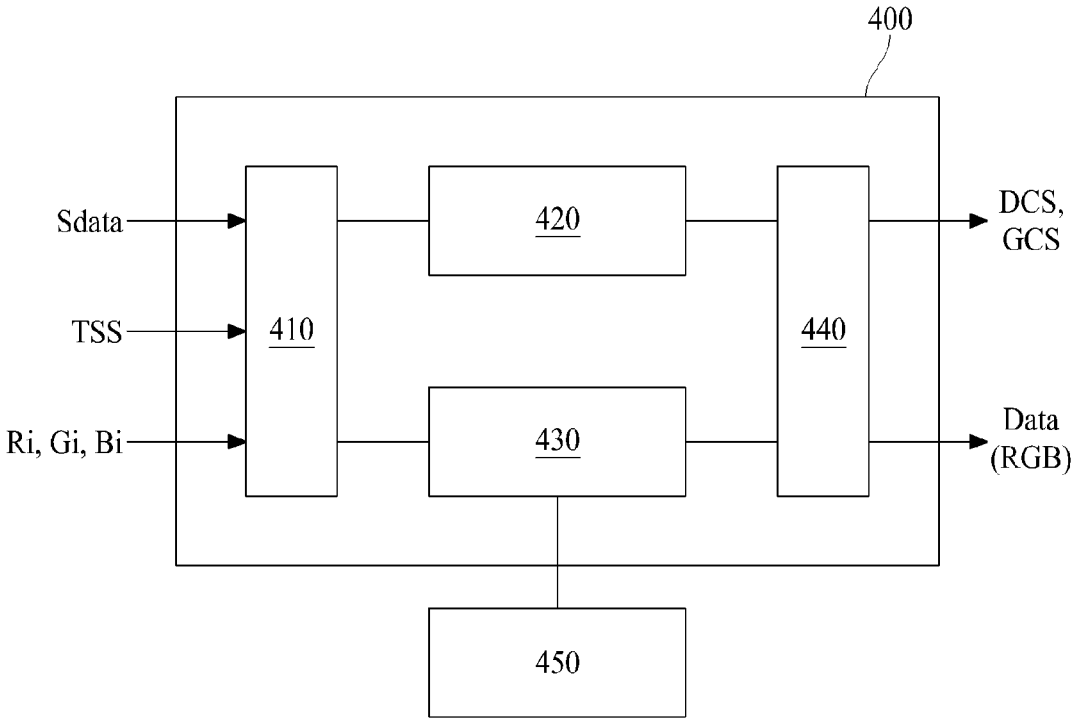

400
Sdata
TSS
Ri, Gi, Bi
410
420
430
440
DCS,
GCS
Data
(RGB)
450

FIG. 4

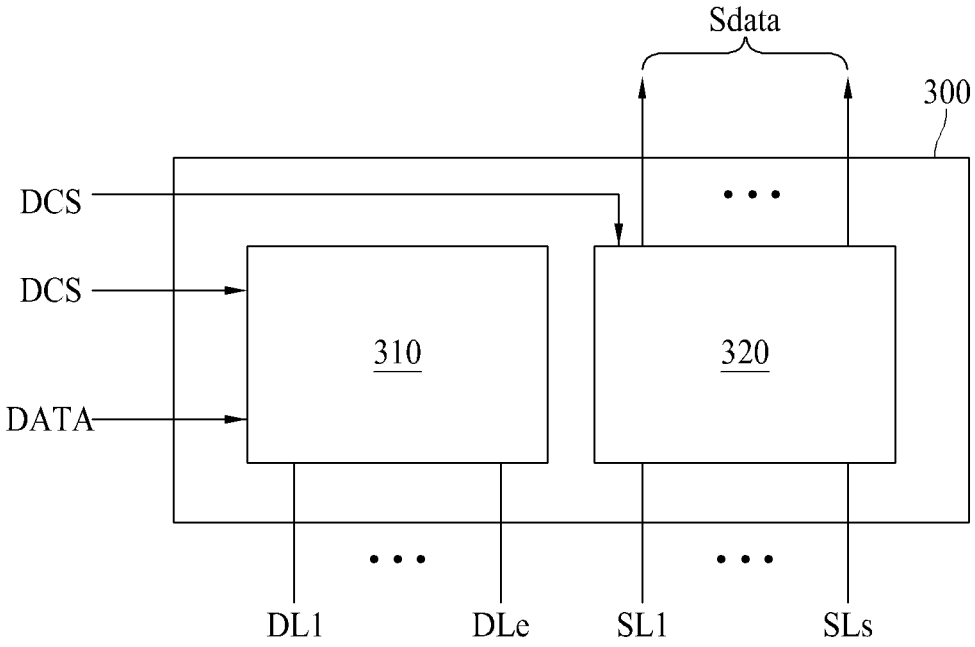


FIG. 5

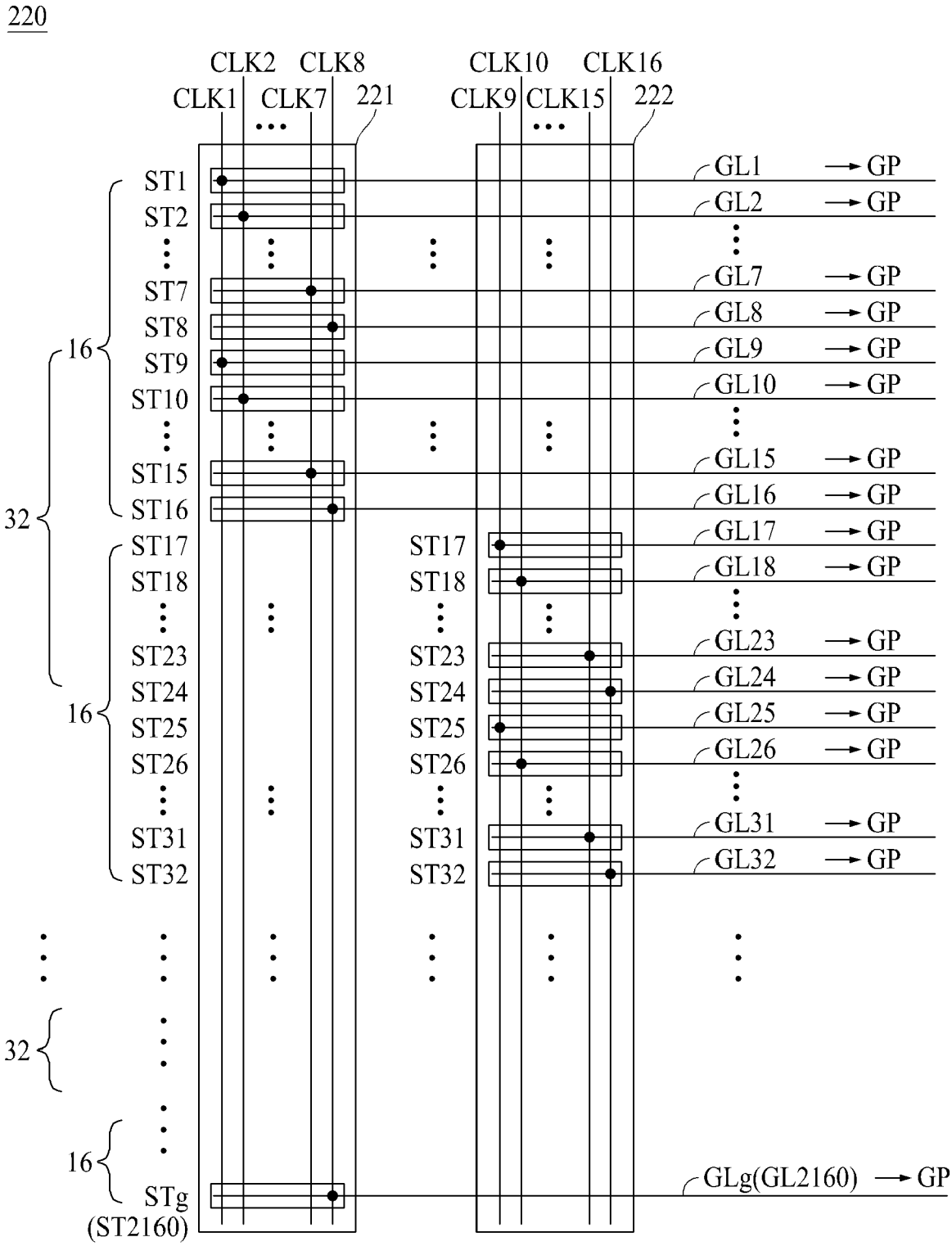

220
CLK2
CLK8
CLK1
CLK7
221
CLK10
CLK16
CLK9
CLK15
222
ST1
ST2
ST7
ST8
ST9
ST10
ST15
ST16
ST17
ST18
ST23
ST24
ST25
ST26
ST31
ST32
STg
(ST2160)
16
32
16
32
16
GL1
GL2
GL7
GL8
GL9
GL10
GL15
GL16
GL17
GL18
GL23
GL24
GL25
GL26
GL31
GL32
GLg(GL2160)
GP

FIG. 6

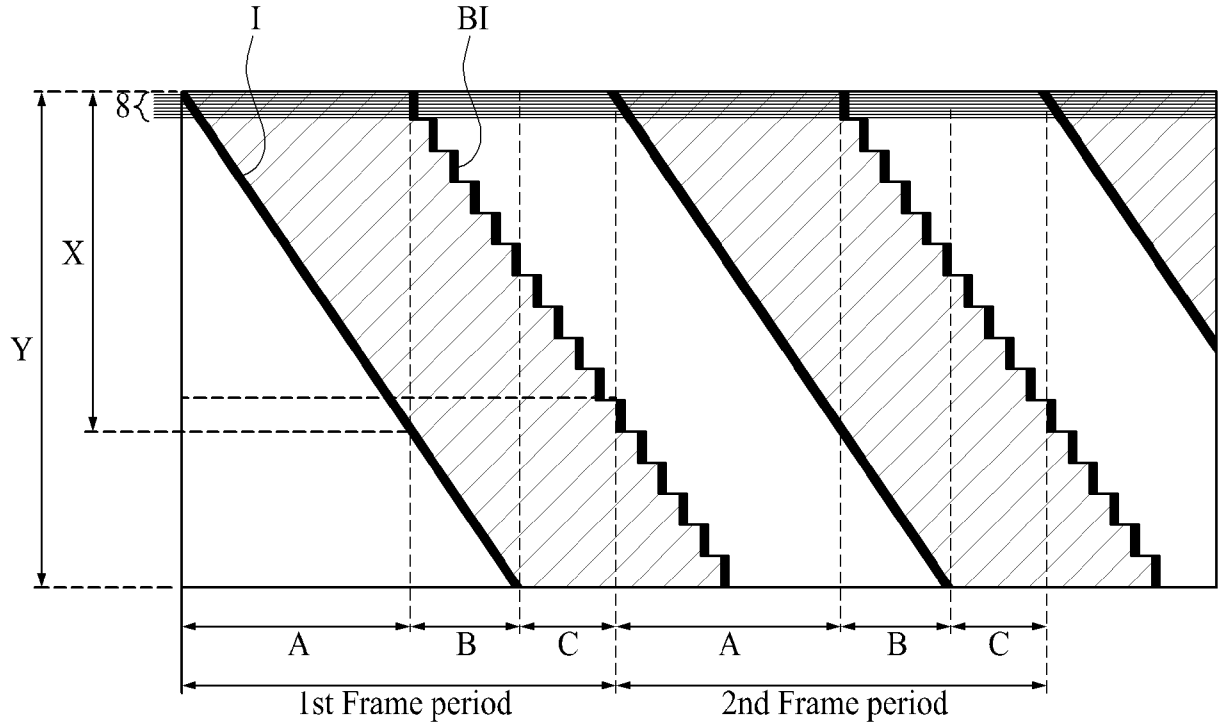

I
BI
87
X
Y
A
B
C
A
B
C
1st Frame period
2nd Frame period

FIG. 7

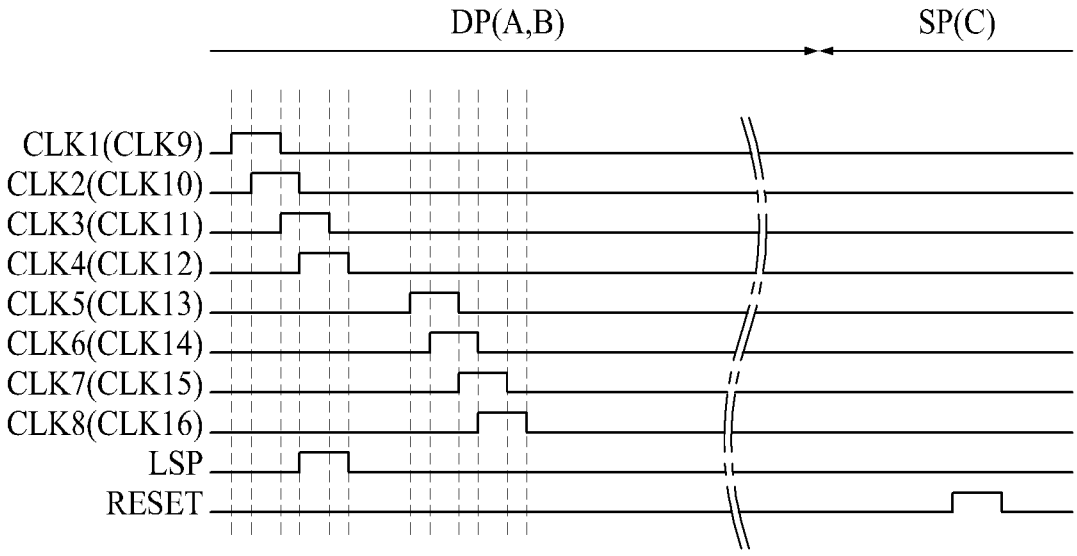

DP(A,B)
SP(C)
CLK1(CLK9)
CLK2(CLK10)
CLK3(CLK11)
CLK4(CLK12)
CLK5(CLK13)
CLK6(CLK14)
CLK7(CLK15)
CLK8(CLK16)
LSP
RESET

FIG. 8

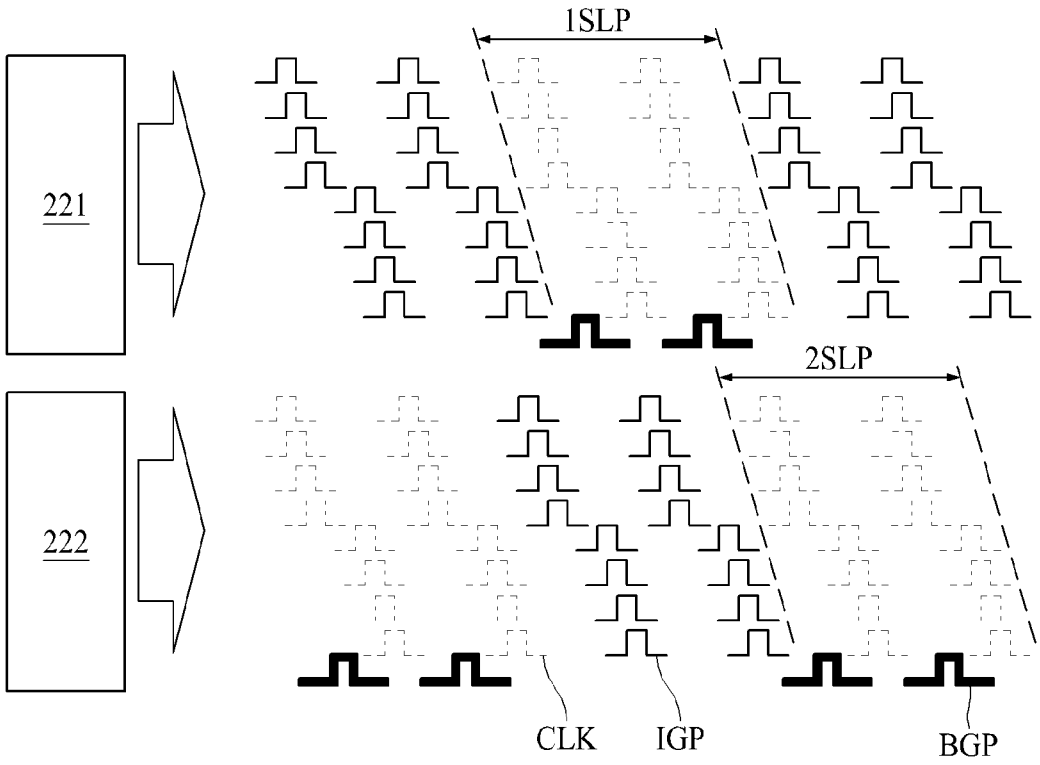


FIG. 9

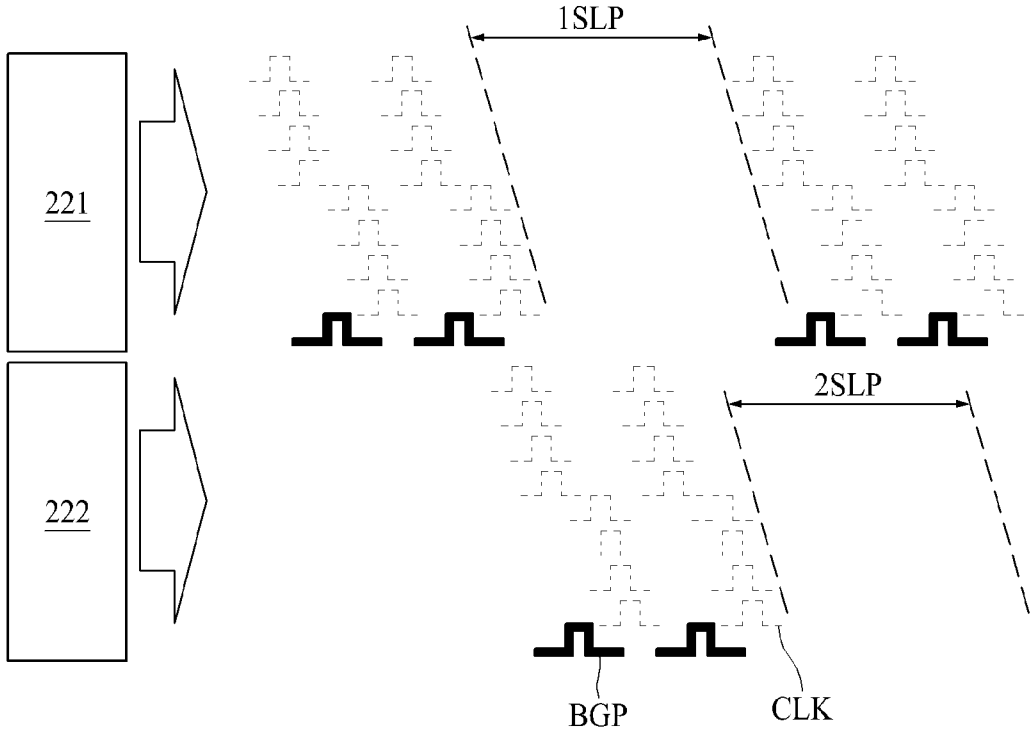
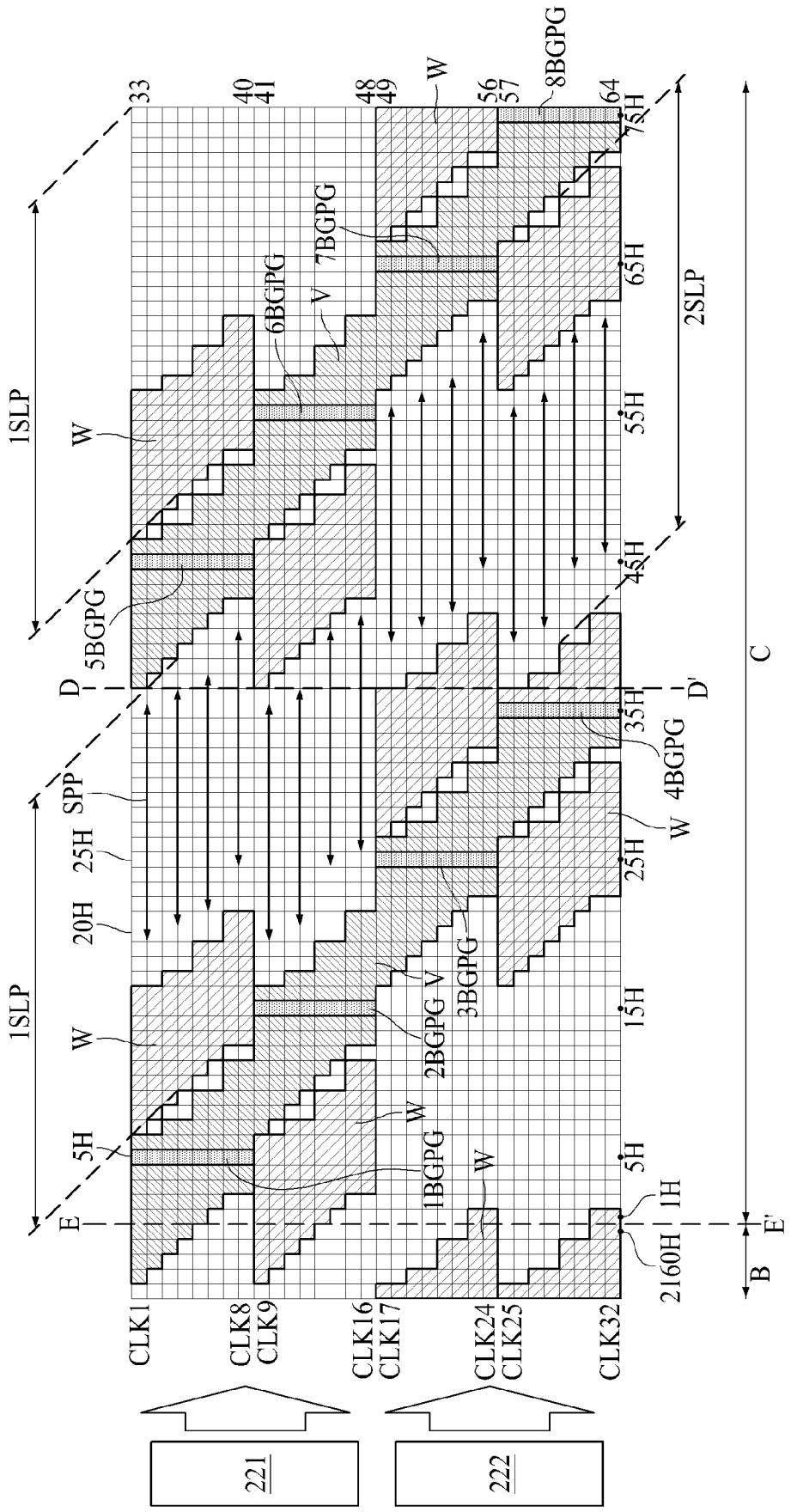


FIG. 10


33
40
41
48
49
56
57
64
W
8BGPG
7BGPG
6BGPG
V
1SLP
W
5BGPG
65H
55H
45H
2SLP
D
D'
C
SPP
25H
20H
1SLP
W
5H
E
E'
35H
4BGPG
W
25H
2BGPG
V
3BGPG
15H
W
1BGPG
W
5H
1H
2160H
B
CLK1
CLK8
CLK9
CLK16
CLK17
CLK24
CLK25
CLK32
221
222

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 19 19 2455

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2017/345376 A1 (TANI RYOSUKE [KR] ET AL) 30 November 2017 (2017-11-30) * paragraph [0043] - paragraph [0059] * * paragraph [0064] - paragraph [0080] * -----	1,15-17	INV. G09G3/3233 G09G3/3266 G09G3/3291
X	US 2018/137825 A1 (AN CHANGHO [KR] ET AL) 17 May 2018 (2018-05-17) * paragraph [0045] - paragraph [0066] * * paragraph [0099] - paragraph [0122] * * paragraph [0134] - paragraph [0147] * -----	1,2 3-14	
			TECHNICAL FIELDS SEARCHED (IPC)
			G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	31 October 2019	Njibamum, David

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 19 19 2455

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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31-10-2019

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	有机发光显示装置		
公开(公告)号	EP3624104A1	公开(公告)日	2020-03-18
申请号	EP2019192455	申请日	2019-08-20
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE GEUNWOO PARK YONGKYU LEE MUNJUN		
发明人	LEE, GEUNWOO PARK, YONGKYU LEE, MUNJUN		
IPC分类号	G09G3/3233 G09G3/3266 G09G3/3291		
CPC分类号	G09G3/3208 G09G3/3291 G09G3/3233 G09G3/3266 G09G2300/0804 G09G2310/0218 G09G2310/0245 G09G2310/0251 G09G2310/08 G09G2320/0252 G09G2320/0261 G09G2320/029 G09G3/3258 G09G2310/0205 G09G2310/0286 G09G2310/061 G09G2320/0238 G09G2320/0257 G09G2330/028		
优先权	1020180109111 2018-09-12 KR		
外部链接	Espacenet		

摘要(译)

公开了一种有机发光显示装置。 有机发光显示设备在垂直消隐时段（C）中输出用于黑色图像的黑选通脉冲（BI）和用于感测的感测选通脉冲，并且不同地设置定时，在该定时下，在黑选通脉冲被输出之后输出感测选通脉冲。 输出，用于每条栅极线。

FIG. 6