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(54) Driving apparatus, oled panel and method for driving oled panel

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Description

TECHNICAL FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to a driving apparatus, an OLED(Organic Light-Emitting Diode) panel, and a method for driving OLED panel.

BACKGROUND

[0002] A display adopting OLED (Organic Light-Emitting Diode) is a newly developing flat panel display device. Due to the advantages of the display adopting OLED, such as simple preparation process, low cost, fast response speed, easy to achieve color display and a large display screen, low power consumption, easy to match a integrated circuit driver, high luminance, wide range of operating temperature, thin and light structure, easy to achieve flexible display, and the like, so the display adopting OLED has a wide range of applications.

[0003] According to the driving manners, OLED can be divided into two different types: Passive Matrix Organic Light Emission Display (PMOLED) and Active Matrix Organic Light Emission Display (AMOLED). The Passive Matrix Organic Light Emission Display has a simple preparation process and a low cost, but has the disadvantages of crosstalk, high power consumption, and short life-span, etc., and thus does not meet the requirements of display with high resolution and large size. On the contrary, Active Matrix Organic Light Emission Display allows a pixel unit to emit light during the period of a frame by incorporating Thin Film Transistors (TFT) in the panel, and thus has the advantages of low driving current being required, low power consumption and long life-span and is capable of satisfying the requirements of display with high resolution, multiple grey levels and large size.

[0004] However, TFT has a threshold voltage, and the drift of the threshold voltage will cause non-uniformity of the luminance of OLED. Various pixel compensation circuits are proposed to solve the above problem, and can be divided, according to driving signals, into two different types: Voltage Programmed Pixel Circuit (VPPC) and Current Programmed Pixel Circuit (CPPC). CPPC is capable of compensating the effects of threshold voltage of TFT, carrier mobility and temperature. Meanwhile, the luminance of OLED can be controlled more accurately by adopting CCPC, since OLED is a current-driving device, the luminance of which is proportion to the current flowing through OLED.

The configuration of a current driving pixel unit of current mirror type in the prior art is shown in Fig.1, and the timing sequence for controlling the pixel unit shown in Fig. 1 is illustrated in Fig.2. In Figure 1, A2 and A4 are controlled to be tuned on alternatively, and OLED is driven by A1. Such a configuration is capable of compensating the variation of the output current caused by such factors as the parameters of devices in a pixel current array and the temperature. Nevertheless, the main defect of the pixel circuit shown in Fig.1 lies in the parasitic capacitances generated by the switching transistors A2 and A3 and the overlap capacitances between signal lines, wherein the overlap capacitances causes the Current Programmed Pixel Circuit to take a long time to achieve a stable current in the condition of low grey level and low current, which in turn severely constrains the application of the pixel unit of current driving type in a display of large dimension and high resolution.

[0005] US2005/280613A1 discloses a display device which displays image information based on display data and in Fig. 4 an example of a voltage current conversion-current supply circuit applicable to a data driver applicable to the display device. US2005/270205A1 relates to a DA converter, a data line driving circuit, an electro-optical device, a driving method thereof, and an electronic apparatus and sicloses in Figs. 8-9 a data line driving circuit used in an electro-optical device, wherein the data line driving circuit comrpises a V/I converting circuit and a voltage current selector for applying an analog voltage signal to a data line. US2005/168416A1 relates to a drive circuit for a display apparatus includes a gradation voltage generation circuit and a D/A conversion circuit. The gradation voltage generation circuit generates a plurality of different first gradation voltages and a plurality of different second gradation voltages. The D/A conversion circuit drives a light emitting element of a pixel through a data line with a gradation voltage based on one of the first gradation voltages as a first specific gradation voltage in a precharge period and drives the light emitting element of the pixel through the data line with a gradation current based on one of the second gradation voltages as a second specific gradation voltage. The D/A conversion circuit includes a voltage driver to drive the light emitting element, and a current driver to drive the light emitting element. US2009/040212A1 discloses a driver, which includes a digital-to-analog converter receiving a pixel value and outputting one of gamma voltages corresponding to the pixel value, and an output stage providing a driving voltage and a driving current corresponding to the gamma voltage outputted from the digital-to-analog converter, in which the driving voltage is provided during a first part of the programming period and the driving current is provided during a second part of the programming period.

SUMMARY

[0006] In view of the above, the present disclosure provides a driving apparatus, an OLED panel and a method for driving the OLED panel, for providing fast and stable data current and thus achieving the driving of pixel circuit of current driving type and compensation for the threshold voltage of TFT.

[0007] In an embodiment of the present disclosure, there is provided a driving apparatus including a switching module for selecting a voltage signal according to a received clock signal; a conversion module for converting the voltage signal into a current signal; and an output module for outputting the voltage signal or the converted current signal to drive a pixel circuit array, wherein an output terminal of the switching module is connected to an input terminal of the conversion module and an input terminal of the output module, and an output terminal of the conversion module is connected to an input terminal of the output module.

[0008] In an embodiment of the present disclosure, there is provided an OLED panel including substrate and a pixel circuit array formed on the substrate, as well as the driving apparatus.

[0009] In an embodiment of the present disclosure, there is provided a method for driving an OLED panel including the steps of: inputting a first level signal from a clock signal generating module to a switching module; transmitting a received data voltage signal from an output module to a pixel circuit array; inputting a second level signal from the clock signal generating module to the switching module; converting by a conversion module the received data voltage signal into a data current signal; transmitting the data current signal from the output module to the pixel circuit array to drive OLED.

[0010] In an embodiment of the present disclosure, there is provided a driving apparatus including a switching module for selecting a voltage signal according to a received clock signal; a conversion module for converting the voltage signal into a current signal; and an output module for outputting the voltage signal or the converted current signal to drive a pixel circuit array, wherein the switching module is connected to the conversion module and the output module, and the conversion module is connected to the switching module and the output module. The driving apparatus according to the embodiment of the present disclosure selects the voltage signal by the switching module, and thus can firstly output the voltage signal, quickly charge/discharge parasitic capacitance on a data line by the voltage signal, and then output a current signal. So, the effect of the parasitic capacitance on the current signal is reduced and the output current can achieve a stable state quickly, which thus is helpful for the stable driving of the pixel circuit array. Meanwhile, the circuit of driving current type can effectively compensate the effects of such factors as threshold voltage of TFT, carrier mobility, temperature, and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The present disclosure will become more fully understood from the detailed description given hereinafter and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present disclosure and wherein:

FIG.1 is a schematic diagram showing a driving pixel unit apparatus in the prior art;
FIG.2 is a timing sequence diagram of the driving pixel unit apparatus shown in Fig.1;
FIG.3 is a main block diagram of a driving apparatus according to an embodiment of the present disclosure;
FIG.4 is a detail block diagram of the driving apparatus according to the embodiment of the present disclosure;
FIG.5A is a specific configuration diagram of the driving apparatus according to the embodiment of the present disclosure;
FIG.5B is a detail block diagram of the conversion module and a connection diagram of the conversion module and other modules in the embodiment of the present disclosure;
FIG.6A is a detail configuration diagram of the driving apparatus with a conversion module being implemented in another manner in an embodiment of the present disclosure;
FIG.6B is a schematic diagram of the operational amplifier in the embodiment of the present disclosure;
FIG.6C is a detail block diagram of the conversion module and a connection diagram of the conversion module and other modules in another embodiment of the present disclosure;
FIG.7 is a main flowchart of a method for driving OLED panel according to an embodiment of the present disclosure; and
FIG.8 is detail flowchart of the method for driving OLED panel according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0012] In summary, a driving apparatus according to an embodiment of the present disclosure includes a switching module for selecting a voltage signal according to a received clock signal; a conversion module for converting the voltage signal into a current signal; and an output module for outputting the voltage signal or the converted current signal to drive a pixel circuit array, wherein the switching module is connected to the conversion module and the output module, and the conversion module is connected to the switching module and the output module. The driving apparatus according to the embodiment of the present disclosure can firstly output the voltage signal by selecting the voltage signal with the switching module, and quickly charge/discharge parasitic capacitance across data lines by the voltage signal, then output a current signal so as to reduce the effect of the parasitic capacitance on the current signal, so that the current signal can reach a stable state quickly, decreasing the non-uniformity of the output current and facilitating the stable driving of the pixel circuit array. Meanwhile, Current Programmed Pixel Circuit can effectively compensate the effects of such factors as threshold voltage of TFT, carrier mobility, temperature, and the like.

[0013] OLED panel according to an embodiment of the present disclosure includes a substrate, a pixel circuit array formed on the substrate, and a driving apparatus. An input terminal of the pixel circuit array is connected to an output terminal of the driving apparatus. That is, a data line of the pixel circuit array is connected to the output terminal of the driving apparatus.

[0014] Referring to Fig.3, the driving apparatus according to an embodiment of the present disclosure includes a switching module 301, a conversion module 302 and an output module 303. A first output terminal of the switching module 301 is connected to an input terminal of the conversion module 302, a second output terminal of the switching module 301 is connected to an input terminal of the output module 303, and an output terminal of the conversion module 302 is connected to an input terminal of the output module 303. All of the transistors used in the embodiment of the present disclosure may be TFT (Thin Film Field Effect Transistor).

[0015] Referring to Fig.4, the driving apparatus can further include a voltage generating module 304 and a clock signal generating module 305. An output terminal of the clock signal generating module 305 is connected to a first input terminal of the switching module 301, and an output terminal of the voltage generating module 304 is connected to a second input terminal of the switching module 301.

[0016] Referring to Fig.5A, a specific configuration diagram of the driving apparatus according to the embodiment of the present disclosure is shown. The switching module 301 in the embodiment of the present disclosure may be a switching circuit. The switching module 301 is used to select and output a voltage signal according to a received clock signal. The switching module 301 can include a first switching transistor (hereinafter, referred to as T1) and a second switching transistor (hereinafter, referred to as T2). A gate of T1 is connected to a gate of T2, and is connected to the clock signal generating module 305; a source of T1 is connected to a drain of T2, and is connected to the voltage generating module 304; a drain of T1 is connected to the conversion module 302, and a source of T2 is connected to the output module 303, that is, to a data line of the pixel circuit array via the output module 303. The switching module 301 has two input terminals and two output terminals, wherein a first input terminal is the terminal at which the gate of T1 and the gate of T2 are connected, a second input terminal is the terminal at which the source of T1 and the drain of T2 are connected, a first output terminal is the terminal connected with the drain of T1, and a second output terminal is the terminal connected with the source of T2. T1 and T2 in the embodiment of the present disclosure are TFTs with opposite polarity, for example, T1 is a P type TFT and T2 is a N type TFT so that T1 and T2 are complementary, and only one control signal is required for controlling T1 and T2 to be on or off. Alternatively, T1 and T2 may also be TFTs with the same polarity, for example, both T1 and T2 are P type TFTs or N type TFTs, and two control signals are required at this time to control T1 and T2 respectively. Or, T1 and T2 may be triodes instead of TFTs, nevertheless the field effect transistor is a voltage-controlled device and the triode is a current-controlled device, and thus the switching module 301 adopting the field effect transistor has a better effect than that adopting the triode. Or, the switching module 301 may also adopts other circuits having a switching and selecting function. When T1 is a P type TFT and T2 is a N type TFT, the clock signal generating module 305 first outputs a high level signal, and thus T1 turns off and T2 turns on, so that a data voltage signal generated by the voltage generating module 304 arrives at a data line via T2 and the output module 303. The data voltage signal can charge the parasitic capacitance on the data line quickly. After that, the signal generated by the clock signal generating module 305 changes from the high level to a low level, and thus T1 turns on and T2 turns off, so the data voltage signal generated by the voltage generating module 304 does not flow directly into the output module 303, but enters into the conversion module 302 via T1.

[0017] The conversion module 302 is used to convert a received voltage signal into a current signal and output the same. The conversion module 302 includes a first transistor M1, a second transistor M2, a third transistor M3, a fourth transistor M4, a fifth transistor M5, a sixth transistor M6, a seventh transistor M7, a eighth transistor M8, a ninth transistor M9 and a tenth transistor M10. A gate of M1 is connected to the drain of T1 in the switching module 301; a drain of M1 is connected to a drain and a gate of M3 and a gate of M4; a source of M1 is connected to a source of M6, a gate and a drain of M9, and a source of M10, and is grounded; a gate and a drain of M2 is connected to a gate of M5, a drain of M4 and a gate of M10; a source of M2 is connected to a source of M9, a source of M5 and a gate of M6; a source of M3 is connected to a source of M4, a source of M7 and a source of M8 and to a first power supply VDD with a certain potential, and VDD may be an output terminal of a power supply line for supplying power in the embodiment of the present disclosure; a drain of M5 is connected to a drain and a gate of M7, and a gate of M8; a drain of M6 is connected to a drain of M8; a drain of M10 is connected to the source of T2 in the switching module 301, and both are connected to the output module 303 together, that is, both are connected to the data line of the pixel circuit array together via the output module 303. In the embodiment of the present disclosure, M1, M2, M5, M6 and M10 are all N type TFTs, and M3, M4, M7, M8 and M9 are all P type TFTs. The polarities of M1~M10 can be changed, but M1, M2, M5, M6 and M10 should be of the same polarity, and M3, M4, M7, M8 and M9 should be of the same polarity. Under such a circumstance, connections among the respective elements in the circuit can be changed respectively according to the polarities of TFTs, and those skilled in the art can easily make the corresponding variations according to the prior art and the concept of the present invention, so no more descriptions and diagrams are detailed here.

[0018] M1, M2, M3 and M4 constitute a cascode mirror current source configuration for implementing the conversion from a data voltage signal to a data current signal. The configuration may also be substituted by other configuration units having the function of voltage conversion.

[0019] Referring to Fig.5B, a detailed block diagram of the conversion module 302 in the embodiment of the present disclosure is shown. The conversion module 302 includes a data voltage input unit 30211., a threshold voltage compensating unit 30221, and a data current output unit 30231. An input terminal of the data voltage input unit 30211 is connected to the first output terminal of the switching module 301, an output terminal of the data voltage input unit 30211 is connected to an input terminal of the threshold voltage compensating unit 30221, an output terminal of the threshold voltage compensating unit 30221 is connected to an input terminal of the data current output unit 30231, and an output terminal of the data current output unit 30231 is connected to the input terminal of the output module 303.

[0020] M1, M2, M3, M4 and M9 constitute the data voltage input unit 30211 for converting the received data voltage signal into the data current signal. The data voltage input unit 30211 may also be substituted by other configurations having the function of converting a data voltage into a data current. M5, M6, M7 and M8 constitute the threshold voltage compensating unit 30221, which implements the compensation for threshold voltage of TFT by designing TFT with different width/length ratio of channel. That is, the threshold voltage compensating unit 30221 is used to compensate the threshold voltage of the transistor. Such a configuration may also be substituted by other configuration units having the function of compensating the threshold voltage of TFT. M10 constitutes the data current output unit 30231 for outputting the converted data current signal, and is connected to the pixel circuit array via the output module 303 for inputting the data current signal to the pixel circuit array. The data voltage input unit 30211 can be also referred as a first data voltage input unit.

[0021] When T1 turns on and T2 turns off in the switching module 301, the data voltage signal V_{Data} enters into the conversion module 302 through the gate of M1. The gate and drain of M3 are connected together, and thus M3 operates always in the saturation region after it turns on. At the same time, the source voltage of M3 is the same as that of M4, and the gate voltage of M3 is the same as that of M4. It can be seen from Fig.5A that the current of M1 is the same as that of M3, and the current of M2 is the same as that of M4. The following equations can be obtained according to the formulae for calculating the current of TFT in the saturation region.

$$I_{M1} = I_{M3} = 1/2(W/L)_{M1} C_{OX} \mu_n (V_{Data} - V_{Th})^2 \quad (1)$$

$$I_{M2} = I_{M4} = 1/2(W/L)_{M2} C_{OX} \mu_n (V_{Out} - V_A - V_{Th})^2 \quad (2)$$

$$I_{M1} * I_{M2} = I_{M3} * I_{M4} \quad (3)$$

wherein W represents the length of channel of TFT, L represents the width of channel of TFT, Cox represents the capacitance of the insulating layer of TFT, μ_n represents the carrier mobility, and V_{Th} represents the threshold voltage of TFT. V_A represents the source voltage of M5 in Fig.5A, and V_{out} represents the drain voltage of M2 in Fig.5A.

[0022] TFT can be designed as $(W/L)_{M2}*(W/L)_{M4} = 4(W/L)_{M1}*(W/L)_{M3}$ so as to obtain:

$$V_{Out}=1/2V_{Data}+V_A+1/2V_{Th} \quad (4)$$

[0023] Meanwhile, the length/width ration of channel of M5 and that of M6 can be designed to be the same, that is, $(W/L)_{M5}=(W/L)_{M6}$, and M7 and M8 are in a cascode connection, so the current flowing through M7 is the same as that flowing through M8, that is, $I_{M7} = I_{M8}$, and we can obtain:

$$I_{M7} = I_{M5} = 1/2(W/L)_{M5} C_{OX} \mu_n (V_{OUT} - V_A - V_{Th})^2 \quad (5)$$

$$I_{M8} = I_{M6} = 1/2(W/L)_{M6} C_{OX} \mu_n (V_A - V_{Th})^2 \qquad (6)$$

$$V_{Out} = 2V_A \qquad (7)$$

[0024] Then we can obtain:

$$V_{out} = V_{Data} + V_{Th} \qquad (8)$$

[0025] Then, the data current output from M10 can be:

$$I_{Data} = 1/2(W/L)_{M10} C_{OX} \mu_n (V_{Out} - V_{Th})^2 = 1/2(W/L)_{M10} C_{OX} \mu_n V_{Data}{}^2 \qquad (9)$$

[0026] It can be seen that the data current output from M10 is independent of the threshold voltage of TFT in the driving apparatus, that is to say, the drift of the threshold voltage of TFT will not affect the output current of the driving apparatus, and thus the compensation for the threshold voltage of TFT can be achieved.

[0027] With the conversion module 302, the conversion from the data voltage signal to the data current signal can be implemented, and thus the pixel circuit array of current driving type can be driven by a chip for providing voltage driving. As a result, the technical problem of the pixel circuit array of current driving type lacking corresponding source driving Integrated Circuit Chips can be solved, while maintaining the advantages of high stability and high accuracy of the pixel circuit array of current driving type. At the same time, the conversion module 302 is capable of compensating the threshold voltage of TFT, and thus a stable output of the data current is achieved.

[0028] Under the control of the clock signal generating module 305, the pixel circuit array is driven by a constant data voltage signal in a first stage and by a constant data current signal in a second stage. As compared with the conventional driving manner, the effects of the driving manner according to the embodiment of the present disclosure and the conventional driving manner are the same in the stage of OLED emitting light; however in the stage of driving, the driving apparatus proposed in the embodiment of the present disclosure can make the driving current achieve a stable state quickly and thus has a better effect on the driving for the pixel circuit array.

[0029] The output module 303 is used to output the voltage signal or the converted current signal to drive the pixel circuit array. More specifically, the output module 303 may be a lead wire which is connected to the input terminal of the data line. The output terminal of the data line is connected to the pixel circuit array.

[0030] The voltage generating module 304 is used to generate the data voltage signal.

[0031] The clock signal generating module 305 is used to generate a clock signal. More specifically, the clock signal generating module 305 can generate a changing clock signal. For example, the clock signal generating module 305 in the embodiment of the present disclosure first generates a first level signal, that is, a high level signal in the embodiment of the present disclosure, and then generates a second level signal, that is, a low level signal in the embodiment of the present disclosure. The signal generated by clock signal generating module 305 can change correspondingly according to the polarity of TFT in the driving apparatus.

[0032] Referring to Fig.6A, a specific configuration diagram of the driving apparatus with a conversion module 302 being implemented in another manner according to an embodiment of the present disclosure is shown.

[0033] The conversion module 302 is used to convert a received voltage signal into a current signal. The conversion module 302 includes a first amplifier A1, a second amplifier A2, a first resistor R1, a second resistor R2, a third resistor R3, a fourth resistor R4, and a fifth resistor R5. A terminal of R3 is connected to the drain of T1 in the switching module 301; another terminal of R3 is connected to a terminal of R5 and to a first input terminal of A1 (terminal D in Fig.6A); a terminal of R1 is grounded, and another terminal of R1 is connected to a terminal of R2 and to a second input terminal of A1 (that is, terminal C in Fig.6A); another terminal of R2 is connected to a terminal of R4 and to an output terminal of A1 (that is, terminal A in Fig.6A); another terminal of R4 is connected to a first input terminal of A2 (that is, terminal Vout in Fig.6A); another terminal of R5 is connected to an output terminal of A2 (that is, terminal B in Fig.6A); a second input terminal of A2 (that is, terminal E in Fig.6A) is connected to the output terminal of A2; and the terminal Vout is connected to the output module 303. A1 and A2 are cascode operational amplifiers, the schematic diagram of which is shown in Fig.6B. The cascode operational amplifier includes four TFTs (M11, M12, M13 and M14), which is similar to a differential circuit and can suppress zero drift. In the embodiment of the present disclosure, R1, R2, R3, R4 and R5 have the same resistance.

[0034] Referring to Fig.6C, a detail block diagram of another conversion module 302 according to an embodiment of the present disclosure is shown. The conversion module 302 includes a data voltage input unit 30212 and a negative feedback unit 30222. A1, R1, R2, R3 and R4 constitute the data voltage input unit 30212 for converting the received data voltage signal into the data current signal. The data voltage input unit 30212 can also be substituted by other configuration units having the function of voltage converting. A2 and R5 constitute the negative feedback unit 30222 for compensating the threshold voltage of transistor. With the negative feedback circuit, the constancy of gain can be effectively increased, the non-linear distortion can be effectively reduced, the noise in the feedback loop can be effectively suppressed, and the frequency band can be effectively extended. The negative feedback unit 30222 can also be substituted by other configuration units having the effect of feedback. An input terminal of the data voltage input unit 30212 is connected to the first output terminal of the switching module 301, an output terminal of the data voltage input unit 30212 is connected to an input terminal of the negative feedback unit 30222 and the input terminal of the output module 303, and an output terminal of the negative feedback unit 30222 is connected to an input terminal of the data voltage input unit 30212. The data voltage input unit 30212 cal also be referred to as a second data voltage input unit.

[0035] When T1 turns on and T2 turns off in the switching module 301, the data voltage signal enters the conversion module 302 via R3. The data voltage signal V_{Data} generated by the voltage generating module 304 is applied to the first input terminal of A1 via R3. According to the principle of the operational amplifier, the voltage at the terminal C and the voltage at the terminal D in Fig.6A satisfy the following equation:

$$V_C=V_D \qquad (10)$$

[0036] For the same reasons,

$$V_E=V_B=V_{OUT} \qquad (11)$$

[0037] According to the Law of Current Conservation,

$$(V_{DATA}-V_D)/R_3=(V_D-V_B)/R_5 \qquad (12)$$

$$(V_A-V_{OUT})/R_4=(V_C-V_A)/R_2=(0-V_C)/R_1 \qquad (13)$$

[0038] Since R1=R2=R3=R4=R5=R, so we can obtain:

$$V_A=2V_C=2V_D \qquad (14)$$

$$V_{DATA}+V_{OUT}=2V_D \qquad (15)$$

[0039] Then, we can obtain:

$$I_{Data}=(V_A-V_{OUT})/R=V_{DATA}/R \qquad (16)$$

[0040] Consequently, the conversion from the data voltage signal to the data current signal can be implemented. Also it can be seen from the equation (16) that the output data current signal is independent of the threshold voltage of TFT, and thus the compensation for the threshold voltage of TFT can be achieved.

[0041] A method for driving a pixel circuit array will be described below by means of a specific flow.

[0042] Referring to Fig.7, the main flow of the method for driving OLED panel according to the embodiment of the present disclosure is as follows:

At step 701, the clock signal generating module 305 inputs a first level signal to the switching module 301. The first level signal is a high level signal in the embodiment of the present disclosure.

At step 702, the output module 303 transmits a received data voltage signal to a pixel circuit array. In combination with Fig.6, T1 turns off and T2 turns on in the switching module 301, so the switching module 301 transmits the received data voltage signal to the output module 303, and the output module 303 then transmits the received data voltage signal to the pixel circuit array.

At step 703, the clock signal generating module 305 inputs a second level signal to the switching module 301. The second level signal is a low level signal in the embodiment of the present disclosure.

At step 704, the conversion module 302 converts the received data voltage signal into a data current signal. Combining Fig.6, T2 turns off and T1 turns on in the switching module 301, so the switching module 301 transmits the received data voltage signal to the conversion module 302, and the conversion module 302 then converts the received data voltage signal into the data current signal.

At step 705, the output module 303 transmits the data current signal to the pixel circuit array for driving OLED. After the conversion module 302 converts the received data voltage signal into the data current signal, the conversion module 302 transmits the data current signal obtained to the output module 303, and then the output module 303 transmits the data current signal to the pixel circuit array for driving OLED.

[0043] Referring Fig.8, the detailed flow of the method for driving OLED panel according to the embodiment of the present disclosure is as follows:

At step 801, the clock signal generating module 305 inputs a high level signal to the switching module 301. The embodiment of the present disclosure will be described in detail in conjunction with Fig.6.

At step 802, T2 in the switching module 301 transmits a received data voltage signal to the output module 303, at this time, T1 in the switching module 301 turns off.

At step 803, the output module 303 transmits the received data voltage signal to the pixel circuit array.

At step 804, the input signal from the clock signal generating module 305 changes from a high level to a low level.

At step 805, T1 in the switching module 301 transmits the received data voltage signal to the conversion module 302, at this time, T2 in the switching module 301 turns off.

At step 806, the conversion module 302 converts the received data voltage signal into a data current signal.

At step 807, the conversion module 302 transmits the data current signal obtained by the conversion to the output module 303.

At step 808, the output module 303 transmits the data current signal to the pixel circuit array.

[0044] The driving apparatus according to the embodiment of the present disclosure includes a switching module 301 for selecting a voltage signal according to a received clock signal; a conversion module 302 for converting the voltage signal into a current signal; and an output module 303 for outputting the voltage signal or the converted current signal to drive a pixel circuit array, wherein the switching module 301 is connected to the conversion module 302 and the output module 303, and the conversion module 302 is connected to the switching module 301 and the output module 303. The driving apparatus according to the embodiment of the present disclosure selects the voltage signal by the switching module 301, and thus can firstly output the voltage signal, quickly charge/discharge parasitic capacitance across data lines by the voltage signal; and then output a current signal. Consequently, the effect of the parasitic capacitance on the current signal is reduced, so that the output current can achieve a stable state quickly, which thus is helpful for the stable driving of the pixel circuit array. Meanwhile, the pixel circuit of current driving type can effectively compensate the effects of such factors as threshold voltage of TFT, carrier mobility, temperature, and the like, and thus the stability of the circuit can be increased.

[0045] The benefits of the embodiments of the present disclosure lie in that, by controlling the switching module 301, a data voltage signal can firstly be output to quickly charge/discharge the parasitic capacitance on a data line, so that the electrical potential on the data line can be adjusted to close to a predetermined value in a short time while reducing the effect of the parasitic capacitance on the current signal. After that, the data voltage signal enters into the conversion module 302 under the control of the switching module 301 and is then converted to a data current signal corresponding to the data voltage signal, so as to directly drive a pixel circuit array by the data current signal, which expedites the driving process of the pixel circuit array of current driving type. As a result, the embodiment of the present disclosure may have the advantages of high accuracy and good stability. The data voltage signal in the embodiment of the present disclosure can be supplied directly by the existing data voltage generating IC (Integrated Circuit) for TFT-LCD (Thin Film Transistor-Liquid Crystal Display), so that the problem of the existing pixel circuit array of current driving type lacking a dedicated driving IC can be solved.

[0046] The above descriptions are only for illustrating the preferred embodiments of the present disclosure, and in no way limit the scope of the present disclosure. The embodiments of the disclosure being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the disclosure, and all such modifications as would be obvious to those skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A driving apparatus including:

a switching module (301) for selecting and outputting a data voltage signal according to a received clock signal;
a conversion module (302) for converting the data voltage signal into a data current signal and outputting the data current signal;
an output module (303) for outputting the data voltage signal or the converted data current signal to drive a pixel circuit array;
wherein a first output terminal of the switching module (301) is connected to an input terminal of the conversion module (302), a second output terminal of the switching module (301) is connected to an input terminal of the output module (303), and an output terminal of the conversion module (302) is connected to an input terminal of the output module (303);
wherein the conversion module (302) includes a first data voltage input unit (30211) for converting the data voltage signal into the data current signal, a threshold voltage compensating unit (30221) for compensating the threshold voltage of transistor, and a first data current output unit (30231) for outputting the data current signal converted,
wherein an input terminal of the first data voltage input unit (30211) is connected to the first output terminal of the switching module (301), an output terminal of the first data voltage input unit (30211) is connected to an input terminal of the threshold voltage compensating unit (30221), an output terminal of the threshold voltage compensating unit (30221) is connected to an input terminal of the first data current output unit (30231), and an output terminal of the first data current output unit (30231) is connected to the input terminal of the output module (303);
the first data voltage input unit (30211) includes a first transistor (M1), a second transistor (M2), a third transistor (M3), a fourth transistor (M4), and a ninth transistor (M9); the threshold voltage compensating unit (30221) includes a fifth transistor (M5), a sixth transistor (M6), a seventh transistor (M7), and an eighth transistor (M8); and the first data current output unit (30231) includes a tenth transistor (M10);
wherein a gate of the first transistor (M1) is connected to the first output terminal of the switching module (301); a drain of the first transistor (M1) is connected to a drain and a gate of the third transistor (M3) and a gate of the fourth transistor (M4); a source of the first transistor (M1) is connected to a source of the sixth transistor (M6), a gate and a drain of the ninth transistor (M9), and a source of the tenth transistor (M10), and is grounded; a gate and a drain of the second transistor (M2) are connected to a gate of the fifth transistor (M5), a drain of the fourth transistor (M4) and a gate of the tenth transistor (M10); a source of the second transistor (M2) is connected to a source of the ninth transistor (M9), a source of the fifth transistor (M5) and a gate of the sixth transistor (M6); a source of the third transistor (M3) is connected to a source of the fourth transistor (M4), a source of the seventh transistor (M7) and a source of the eighth transistor (M8) and a first power supply terminal (VDD); a drain of the fifth transistor (M5) is connected to a drain and a gate of the seventh transistor (M7), and a gate of the eighth transistor (M8); a drain of the sixth transistor (M6) is connected to a drain of the eighth transistor (M8); and a drain of the tenth transistor (M10) is connected to the second output terminal of the switching module (301) and the input terminal of the output module(303).

2. The driving apparatus of claim 1, further including a clock signal generating module (305) and a voltage generating module (304),
wherein the clock signal generating module (305) has an output terminal connected to a first input terminal of the switching module (301) and is used for generating the clock signal; and
the voltage generating module (304) has an output terminal connected to a second input terminal of the switching module (301) and is used for generating the data voltage signal.

3. The driving apparatus of claim 2, wherein the switching module (301) includes a first switching transistor (T1) and a second switching transistor (T2),
wherein a gate of the first switching transistor (T1) is connected to a gate of the second switching transistor (T2) and the output terminal of the clock signal generating module (305);
a source of the first switching transistor (T1) is connected to a drain of the second switching transistor (T2) and the output terminal of the voltage generating module (304);
a drain of the first switching transistor (T1) is connected to the gate of the first transistor (M1); and
a source of the second switching transistor (T2) is connected to the drain of the tenth transistor (M10) and the input terminal of the output module (303).

4. The driving apparatus of claim 3, wherein the first switching transistor (T1) and the second switching transistor (T2) are of opposite polarities.

5. The driving apparatus of any of claims 1-4, wherein the first transistor (M1), the second transistor (M2), the fifth transistor (M5), the sixth transistor (M6) and the tenth transistor (M10) are of the same polarity, and the third transistor (M3), the fourth transistor (M4), the seventh transistor (M7), the eighth transistor (M8) and the ninth transistor (M9) are of the same polarity.

6. The driving apparatus of any of claims 1-5, wherein the output module (303) is a lead wire, the output terminal of which is connected to the input terminal of the data line in the pixel circuit array.

7. The driving apparatus of any of claims 3-6, wherein the first switching transistor (T1) and the second switching transistor (T2) are Thin Film Field Effect Transistors, and the first transistor (M1), the second transistor (M2), the third transistor (M3), the fourth transistor (M4), the fifth transistor (M5), the sixth transistor (M6), the seventh transistor (M7), the eighth transistor (M8), the ninth transistor (M9) and the tenth transistor (M10) are Thin Film Transistors.

8. An OLED panel including a substrate, a pixel circuit array formed on the substrate, and the driving apparatus of any one of claims 1-7.

9. A method for driving the OLED panel as recited in claim 8, including the steps of:

inputting a first level signal from a clock signal generating module (305) to a switching module (301);
transmitting a received data voltage signal from an output module (303) to a pixel circuit array;
inputting a second level signal from the clock signal generating module (305) to the switching module (301);
converting by a conversion module (302) the received data voltage signal into a data current signal; and
transmitting the data current signal from the output module (303) to the pixel circuit array to drive OLED.

10. The method of claim 9, wherein
after inputting the first level signal from the clock signal generating module (305), the method further includes the step of transmitting the received data voltage signal by the switching module (301) to the output module (303); and
after inputting the second level signal from the clock signal generating module (305) to the switching module (301), the method further includes the step of transmitting the received data voltage signal by the switching module (301) to the conversion module (302).

11. The method of claim 10, wherein the first level signal is a high level signal, and the second level signal is a low level signal.

Patentansprüche

1. Steuervorrichtung, beinhaltend:

ein Schaltmodul (301) zur Auswahl und zur Ausgabe eines Datenspannungssignals gemäß einem empfangenen Taktsignal;
ein Umwandlungsmodul (302) zur Umwandlung des Datenspannungssignals in ein Datenstromsignal und zur Ausgabe des Datenstromsignals;
ein Ausgabemodul (303) zur Ausgabe des Datenspannungssignals oder des umgewandelten Datenstromsignals, um ein Pixelschaltungs-Array anzusteuern;
wobei ein erster Ausgabeanschluss des Schaltmoduls (301) mit einem Eingabeanschluss des Umwandlungsmoduls (302) verbunden ist, wobei ein zweiter Ausgabeanschluss des Schaltmoduls (301) mit einem Eingabeanschluss des Ausgabemoduls (303) verbunden ist und wobei ein Ausgabeanschluss des Umwandlungsmoduls (302) mit einem Eingabeanschluss des Ausgabemoduls (303) verbunden ist;
wobei das Umwandlungsmodul (302) eine erste Datenspannungseingabeeinheit (30211) zur Umwandlung des Datenspannungssignals in das Datenstromsignal, eine Schwellenwertspannungskompensationseinheit (30221) zur Kompensation der Schwellenwertspannung des Transistors und eine erste Datenstromausgabeeinheit (30231) zur Ausgabe des umgewandelten Datenstromsignals beinhaltet,
wobei ein Eingabeanschluss der ersten Datenspannungseingabeeinheit (30211) mit dem ersten Ausgabeanschluss des Schaltmoduls (301) verbunden ist, wobei ein Ausgabeanschluss der ersten Datenspannungsein-

gabeeinheit (30211) mit einem Eingabeanschluss der Schwellenwertspannungskompensationseinheit (30221) verbunden ist, wobei ein Ausgabeanschluss der Schwellenwertspannungskompensationseinheit (30221) mit einem Eingabeanschluss der ersten Datenstromausgabeeinheit (0231) verbunden ist und wobei ein Ausgabeanschluss der ersten Datenstromausgabeeinheit (30231) mit dem Eingabeanschluss des Ausgabemoduls (303) verbunden ist;
wobei die erste Datenspannungseingabeeinheit (30211) einen ersten Transistor (M1), einen zweiten Transistor (M2), einen dritten Transistor (M3), einen vierten Transistor (M4) und einen neunten Transistor (M9) beinhaltet;
wobei die Schwellenwertspannungskompensationseinheit (30221) einen fünften Transistor (M5), einen sechsten Transistor (M6), einen siebten Transistor (M7) und einen achten Transistor (M8) beinhaltet; und wobei die erste Datenstromausgabeeinheit (30231) einen zehnten Transistor (M10) beinhaltet;
wobei ein Gate des ersten Transistors (M1) mit dem ersten Ausgabeanschluss des Schaltmoduls (301) verbunden ist; wobei ein Drain des ersten Transistors (M1) mit einem Drain und einem Gate des dritten Transistors (M3) und einem Gate des vierten Transistors (M4) verbunden ist;
wobei eine Source des ersten Transistors (M1) verbunden ist mit einer Source des sechsten Transistors (M6), einem Gate und einem Drain des neunten Transistors (M9) und einer Source des zehnten Transistors (M10) und geerdet ist; wobei ein Gate und ein Drain des zweiten Transistors (M2) verbunden ist mit einem Gate des fünften Transistors (M5), einem Drain des vierten Transistors (M4) und einem Gate des zehnten Transistors (M10); wobei eine Source des zweiten Transistors (M2) verbunden ist mit einer Source des neunten Transistors (M9), einer Source des fünften Transistors (M5) und einem Gate des sechsten Transistors (M6); wobei eine Source des dritten Transistors (M3) verbunden ist mit einer Source des vierten Transistors (M4), einer Source des siebten Transistors (M7) und einer Source des achten Transistors (M8) und einem ersten Energiezufuhranschluss (VDD); wobei ein Drain des fünften Transistors (M5) verbunden ist mit einem Drain und einem Gate des siebten Transistors (M7) und einem Gate des achten Transistors (M8);
wobei ein Drain des sechsten Transistors (M6) verbunden ist mit einem Drain des achten Transistors (M8); und wobei ein Drain des zehnten Transistors (M10) verbunden ist mit dem zweiten Ausgabeanschluss des Schaltmoduls (301) und dem Eingabeanschluss des Ausgabemoduls (303).

2. Steuervorrichtung gemäß Anspruch 1, außerdem beinhaltend ein Taktsignalerzeugungsmodul (305) und ein Spannungserzeugungsmodul (304), wobei das Taktsignalerzeugungsmodul (305) einen Ausgabeanschluss aufweist, der an einen ersten Eingabeanschluss des Schaltmoduls (301) angeschlossen ist und verwendet wird zur Erzeugung des Taktsignals; und
wobei das Spannungserzeugungsmodul (304) einen Ausgabeanschluss aufweist, der an einen zweiten Eingabeanschluss des Schaltmoduls (301) angeschlossen ist und verwendet wird zur Erzeugung des Datenspannungssignals.

3. Steuervorrichtung gemäß Anspruch 2, wobei das Schaltmodul (301) einen ersten Schalttransistor (T1) und einen zweiten Schalttransistor (T2) beinhaltet,
wobei ein Gate des ersten Schalttransistors (T1) verbunden ist mit einem Gate des zweiten Schalttransistors (T2) und dem Ausgabeanschluss des Taktsignalerzeugungsmoduls (305);
wobei eine Source des ersten Schalttransistors (T1) verbunden ist mit einem Drain des zweiten Schalttransistors (T2) und dem Ausgabeanschluss des Spannungserzeugungsmoduls (304);
wobei ein Drain des ersten Schalttransistors (T1) verbunden ist mit dem Gate des ersten Transistors (M1); und wobei eine Source des zweiten Schalttransistors (T2) verbunden ist mit dem Drain des zehnten Transistors (M10) und dem Eingabeanschluss des Ausgabemoduls (303).

4. Steuervorrichtung gemäß Anspruch 3, wobei der erste Schalttransistor (T1) und der zweite Schalttransistor (T2) von unterschiedlichen Polaritäten sind.

5. Steuervorrichtung gemäß einem der Ansprüche 1-4, wobei der erste Transistor (M1), der zweite Transistor (M2), der fünfte Transistor (M5), der sechste Transistor (M6) und der zehnte Transistor (M10) von gleicher Polarität sind und wobei der dritte Transistor (M3), der vierte Transistor (M4), der siebte Transistor (M7), der achte Transistor (M8) und der neunte Transistor (M9) von der gleichen Polarität sind.

6. Steuervorrichtung gemäß einem der Ansprüche 1-5, wobei das Ausgabemodul (303) ein Zuleitungsdraht ist, wobei der Ausgabeanschluss desselben verbunden ist mit dem Eingabeanschluss der Datenleitung in dem Pixelschaltungs-Array.

7. Steuervorrichtung gemäß einem der Ansprüche 3-6, wobei der erste Schalttransistor (T1) und der zweite Schalt-

transistor (T2) Dünnfilm-Feld-Effekt-Transistoren sind, und wobei der erste Transistor (M1), der zweite Transistor (M2), der dritte Transistor (M3), der vierte Transistor (M4), der fünfte Transistor (M5), der sechste Transistor (M6), der siebte Transistor (M7), der achte Transistor (M8), der neunte Transistor (M9) und der zehnte Transistor (M10) Dünnfilm-Transistoren sind.

8. OLED-Tafel, aufweisend ein Substrat, ein Pixelschaltungs-Array, das auf dem Substrat gebildet ist, und eine Steuervorrichtung gemäß einem der Ansprüche 1-7.

9. Verfahren zur Ansteuerung einer OLED-Tafel gemäß Anspruch 8, beinhaltend die Schritte:

Eingeben eines ersten Levelsignals von einem Taktsignalerzeugungsmodul (305) an ein Schaltmodul (301);
Übertragen eines empfangenen Datenspannungssignals von einem Ausgabemodul (303) an ein Pixelschaltungs-Array;
Eingabe eines zweiten Levelsignals von dem Taktsignalerzeugungsmodul (305) an das Schaltmodul (301);
Umwandeln des empfangenen Datenspannungssignals mittels eines Umwandlungsmoduls (302) des empfangenen Datenspannungssignals in ein Datenstromsignal; und
Übertragen des Datenstromsignals von dem Ausgabemodul (303) an das Pixelschaltungs-Array, um das OLED anzusteuern.

10. Verfahren gemäß Anspruch 9, wobei
nach dem Eingeben des ersten Levelsignals von dem Taktsignalerzeugungsmodul (305) das Verfahren außerdem den Schritt umfasst des Übertragens des empfangenen Datenspannungssignals mittels des Schaltmoduls (301) an das Ausgabemodul (303); und
nach dem Eingeben des zweiten Levelsignals von dem Taktsignalerzeugungsmodul (305) an das Schaltmodul (301) das Verfahren außerdem den Schritt beinhaltet des Übertragens des empfangenen Datenspannungssignals mittels des Schaltmoduls (301) an das Umwandlungsmodul (302).

11. Verfahren gemäß Anspruch 10, wobei das erste Levelsignal ein Hochspannungssignal ist und das zweite Levelsignal ein Niederspannungssignal ist.

Revendications

1. Un appareil de pilotage, incluant :

un module de commutation (301) pour sélectionner et fournir en sortie un signal de tension de données selon un signal d'horloge reçu ;
un module de conversion (302) pour convertir le signal de tension de donnée en un signal de courant de données et fournir en sortie le signal de courant de données ;
un module de sortie (303) pour fournir en sortie le signal de tension de données ou le signal de courant de données converti pour piloter une matrice de circuits de pixel ;
dans lequel une première borne de sortie du module de commutation (301) est connectée à une borne d'entrée du module de conversion (302), une deuxième borne de sortie du module de commutation (301) est connectée à une borne d'entrée du module de sortie (303), et une borne de sortie du module de conversion (302) est connectée à une borne d'entrée du module de sortie (303) ;
dans lequel le module de conversion (302) inclut une première unité d'entrée de tension de données (30211) pour convertir le signal de tension de données en un signal de courant de données, une unité de compensation de tension de seuil (30221) pour compenser la tension de seuil de transistor, et une première unité de sortie de courant de données (30231) pour fournir en sortie le signal de courant de données converti,
dans lequel une borne d'entrée de la première unité d'entrée de tension de données (30211) est connectée à la première borne de sortie du module de commutation (301), une borne de sortie de la première unité d'entrée de tension de données (30211) est connectée à une borne d'entrée de l'unité de compensation de tension de seuil (30221), une borne de sortie de l'unité de compensation de tension de seuil (30221) est connectée à une borne d'entrée de la première unité de sortie de courant de données (30231), et une borne de sortie de la première unité de sortie de courant de données (30231) est connectée à une borne d'entrée du module de sortie (303) ;
la première unité d'entrée de tension de données (30211) inclut un premier transistor (M1), un deuxième transistor (M2), un troisième transistor (M3), un quatrième transistor (M4) et un neuvième transistor (M9) ; l'unité

de compensation de tension de seuil (30221) inclut un cinquième transistor (M5), un sixième transistor (M6), un septième transistor (M7) et un huitième transistor (M8) ; et la première unité de sortie de courant de données (30231) inclut un dixième transistor (M10) ;
dans lequel une grille du premier transistor (M1) est connecté à la première borne de sortie du module de commutation (301) ; un drain du premier transistor (M1) est connecté à un drain et une grille du troisième transistor (M3) et une grille du quatrième transistor (M4) ; une source du premier transistor (M1) est connectée à une source du sixième transistor (M6), une grille et un drain du neuvième transistor (M9) et une source du dixième transistor (M10) et est reliée à la terre ; une grille et un drain du deuxième transistor (M2) sont connectés à une grille du cinquième transistor (M5), un drain du quatrième transistor (M4) et une grille du dixième transistor (M10) ; une source du deuxième transistor (M2) est connectée à une source du neuvième transistor (M9), une source du cinquième transistor (M5) et une grille du sixième transistor (M6) ; une source du troisième transistor (M3) est connectée à une source du quatrième transistor (M4), une source du septième transistor (M7) et une source du huitième transistor (M8) et une première borne d'alimentation (VDD) ; un drain du cinquième transistor (M5) est connecté à un drain et une grille du septième transistor (M7) et une grille du huitième transistor (M8) ; un drain du sixième transistor (M6) est connecté à un drain du huitième transistor (M8) ; et un drain du dixième transistor (M10) est connecté à la deuxième borne de sortie du module de commutation (301) et la borne d'entrée du module de sortie (303).

2. L'appareil de pilotage de la revendication 1, incluant en outre un module de génération de signal d'horloge (305) et un module de génération de tension (304),

dans lequel le module de génération de signal d'horloge (305) a une borne de sortie connectée à une première borne d'entrée du module de commutation (301) et est utilisé pour générer le signal d'horloge ; et
le module de génération de tension (304) a une borne de sortie connectée à une deuxième borne d'entrée du module de commutation (301) et est utilisé pour générer le signal de tension de données.

3. L'appareil de pilotage de la revendication 2, dans lequel le module de commutation (301) inclut un premier transistor de commutation (T1) et un deuxième transistor de commutation (T2),

dans lequel une grille du premier transistor de commutation (T1) est connecté à une grille du deuxième transistor de commutation (T2) et la borne de sortie du module de génération de signal d'horloge (305) ;
une source du premier transistor de commutation (T1) est connectée à un drain du deuxième transistor de commutation (T2) et la borne de sortie du module de génération de tension (304) ;
un drain du premier transistor de commutation (T1) est connecté à la grille du premier transistor (M1) ; et
une source du deuxième transistor de commutation (T2) est connectée au drain du dixième transistor (M10) et la borne d'entrée du module de sortie (303).

4. L'appareil de pilotage de la revendication 3, dans lequel le premier transistor de commutation (T1) et le deuxième transistor de commutation (T2) ont des polarités opposées.

5. L'appareil de pilotage de l'une quelconque des revendications 1 à 4, dans lequel le premier transistor (M1), le deuxième transistor (M2), le cinquième transistor (M5), le sixième transistor (M6) et le dixième transistor (M10) ont la même polarité, et le troisième transistor (M3), le quatrième transistor (M4), le septième transistor (M7), le huitième transistor (M8) et le neuvième transistor (M9) ont la même polarité.

6. L'appareil de pilotage de l'une quelconque des revendications 1 à 5, dans lequel le module de sortie (303) est un fil conducteur et la borne de sortie ce celui-ci est connectée à la borne d'entrée de la ligne de données dans la matrice de circuits de pixel.

7. L'appareil de pilotage de l'une quelconque des revendications 3 à 6, dans lequel le premier transistor de commutation (T1) et le deuxième transistor de commutation (T2) sont des transistors à effet de champs à couches minces, et le premier transistor (M1), le deuxième transistor (M2), le troisième transistor (M3), le quatrième transistor (M4), le cinquième transistor (M5), le sixième transistor (M6), le septième transistor (M7), le huitième transistor (M8), le neuvième transistor (M9) et le dixième transistor (M10) sont des transistors en couches minces.

8. Un panneau OLED incluant un substrat, une matrice de circuits de pixel formée sur le substrat et l'appareil de pilotage de l'une quelconque des revendications 1 à 7.

9. Un procédé pour piloter un panneau OLED tel que défini dans la revendication 8, incluant les étapes de :

fournir en entrée un premier signal de niveau à partir d'un module de génération de signal d'horloge (305) à un module de commutation (301) ;
transmettre un signal de tension de données reçu d'un module de sortie (303) à une matrice de circuits de pixel ;
fournir un deuxième signal de niveau à partir du module de génération de signal d'horloge (305) au module de commutation (301) ;
convertir avec un module de conversion (302) le signal de tension de données reçu en un signal de courant de données ; et
transmettre le signal de courant de données du module de sortie (303) à la matrice de circuits de pixel pour piloter des OLED.

10. Le procédé selon la revendication 9, dans lequel :

après avoir fourni en entrée le premier signal de niveau à partir du module de génération de signal d'horloge (305), le procédé inclut en outre l'étape de transmission du signal de tension de données reçu par le module de commutation (301) au module de sortie (303) ;

et

après avoir fourni en entrée le deuxième signal de niveau à partir du module de génération de signal d'horloge (305) au module de commutation (301), le procédé inclut en outre l'étape de transmettre le signal de tension de données reçu par le module de commutation (301) au module de conversion (302).

11. Le procédé selon la revendication 10, dans lequel le premier signal de niveau est un signal de niveau haut et le deuxième signal de niveau est un signal de niveau bas.

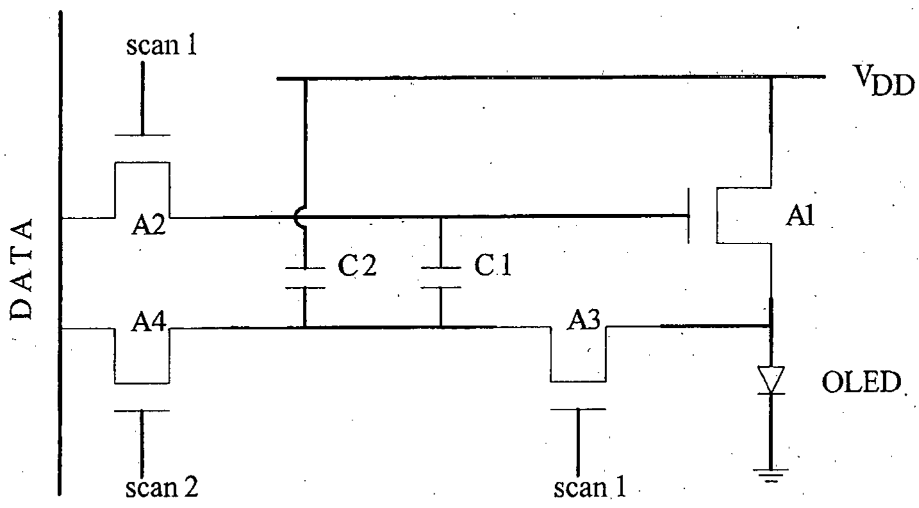
scan 1
VDD
A2
A1
DATA
C2
C1
A4
A3
OLED
scan 2
scan 1

Fig.1

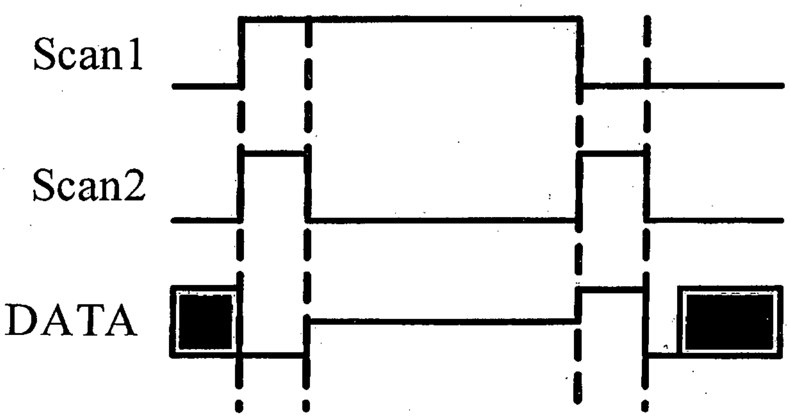
Scan1
Scan2
DATA

Fig.2

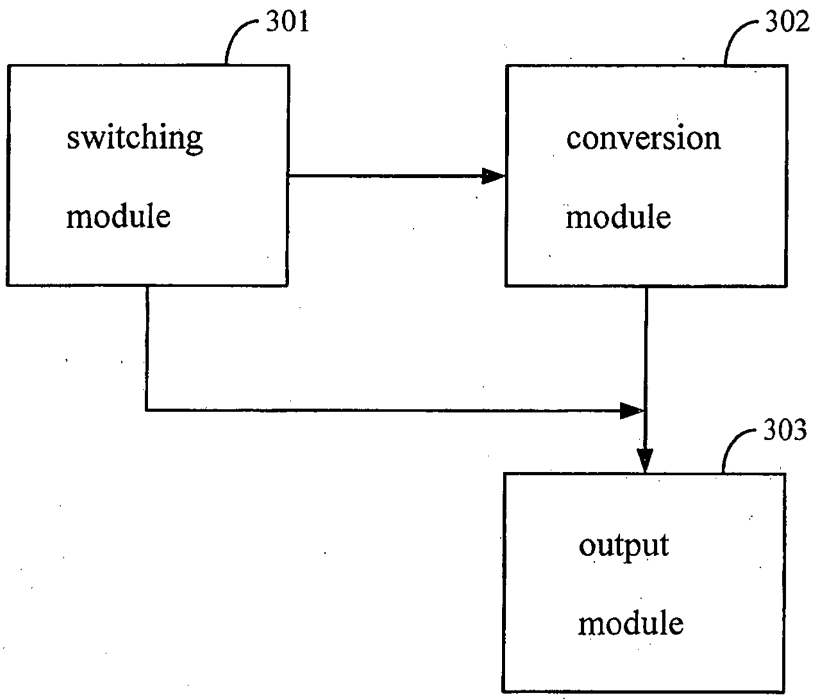
301
302
switching
module
conversion
module
303
output
module

Fig.3

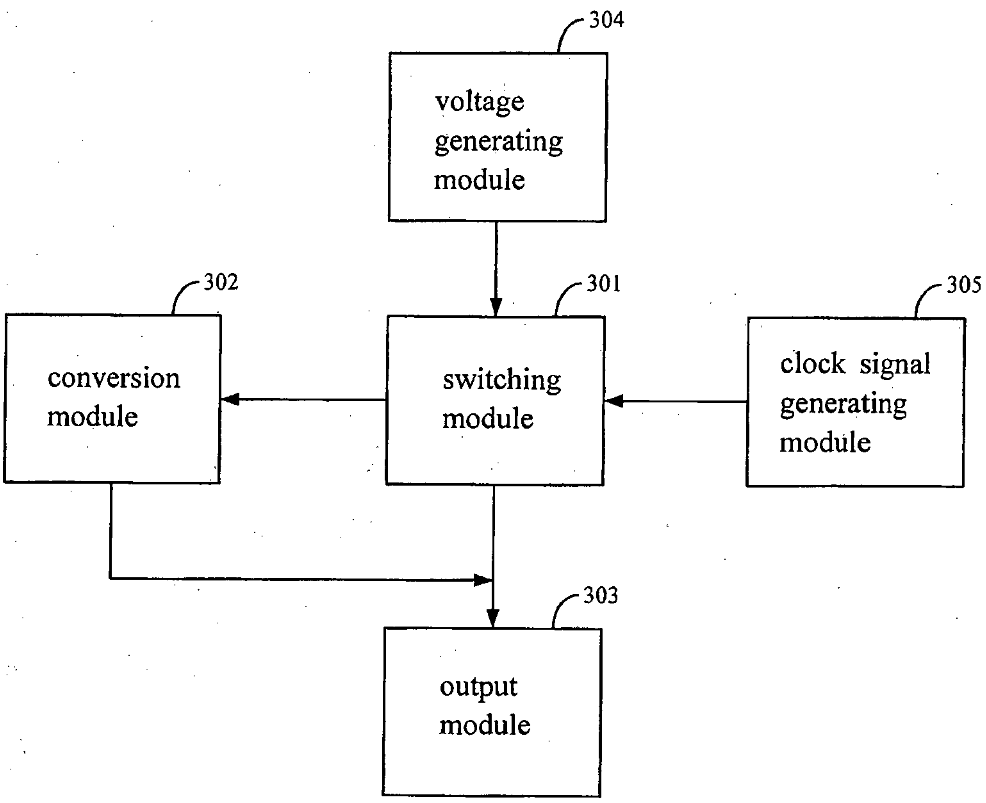
304
voltage
generating
module
302
301
305
conversion
module
switching
module
clock signal
generating
module
303
output
module

Fig.4

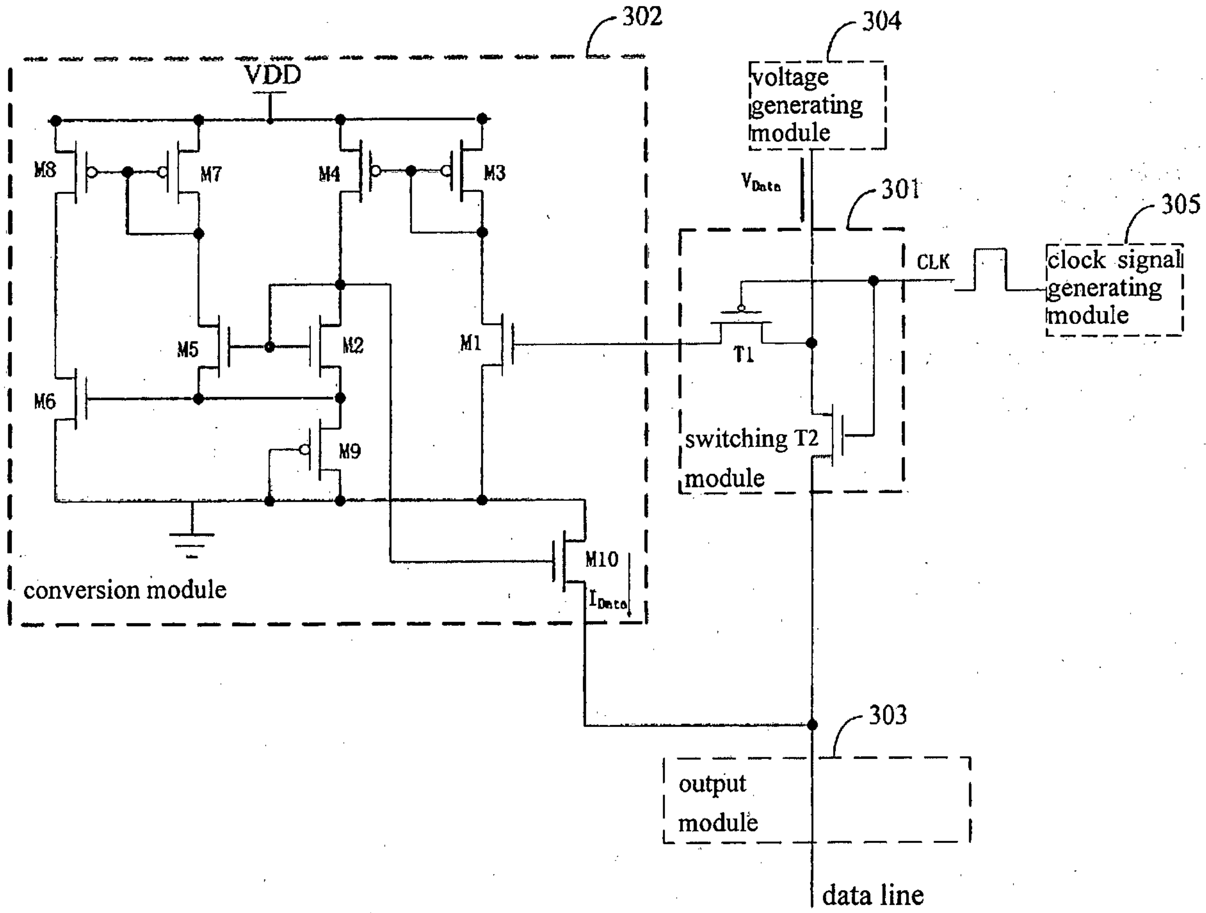
302
304
305
301
303
VDD
M8
M7
M4
M3
M5
M2
M1
M6
M9
M10
I_{Data}
conversion module
voltage generating module
V_{Data}
CLK
clock signal generating module
T1
switching T2
module
output module
data line

Fig.5A

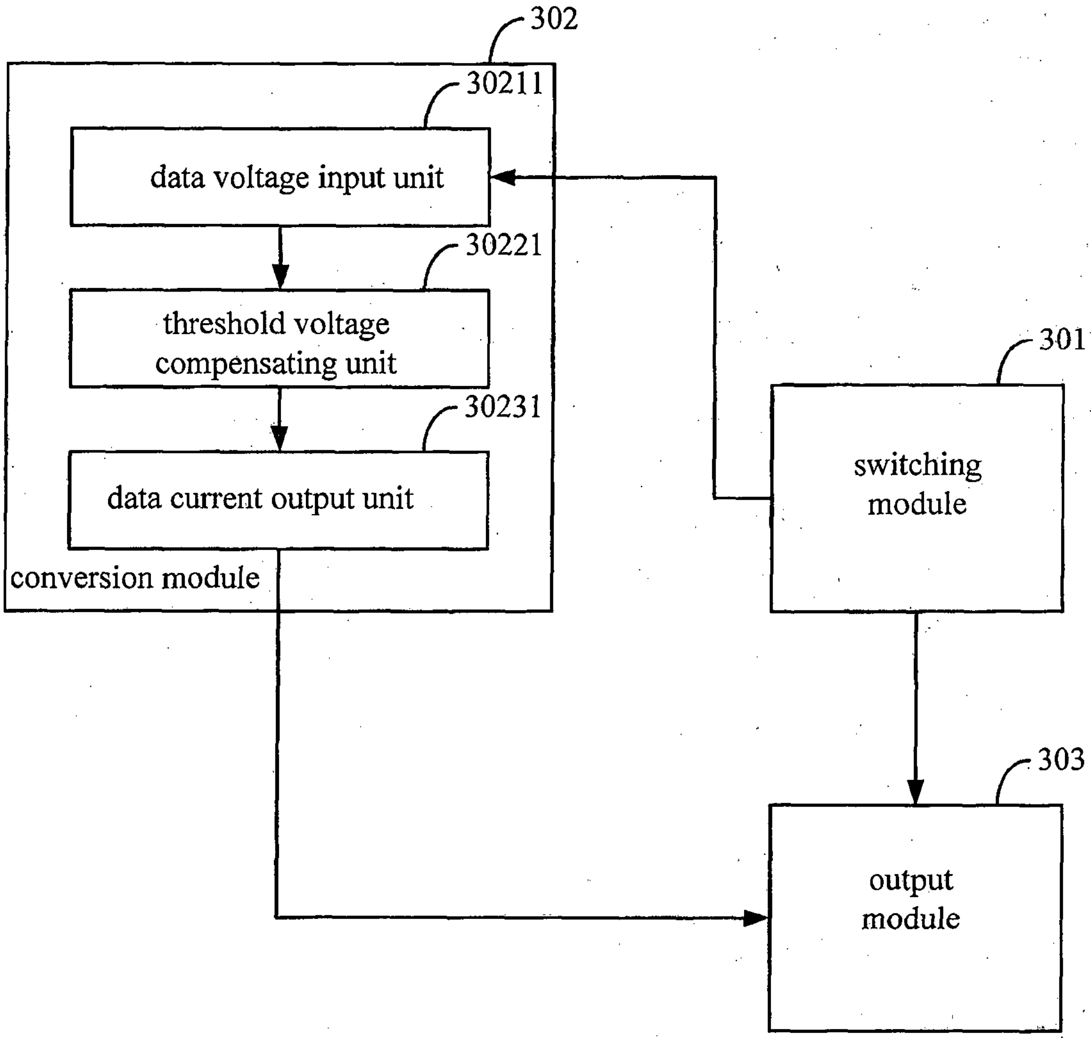
302
30211
data voltage input unit
30221
threshold voltage
compensating unit
30231
data current output unit
conversion module
301
switching
module
303
output
module

Fig.5B

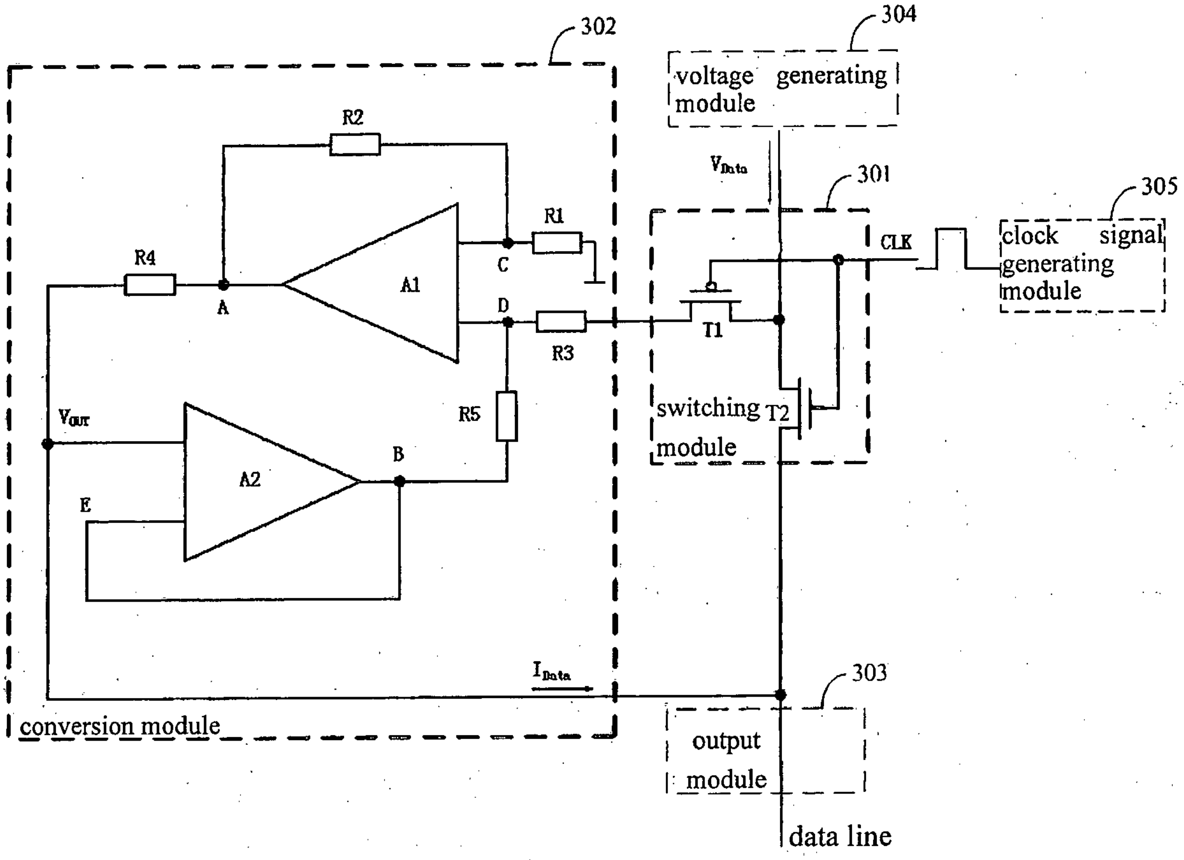
302
304
voltage generating module
V_{Data}
301
305
R2
R1
C
CLK
clock signal generating module
R4
A1
A
D
T1
R3
V_{OUT}
R5
switching module
T2
A2
B
E
I_{Data}
303
conversion module
output module
data line

Fig.6A

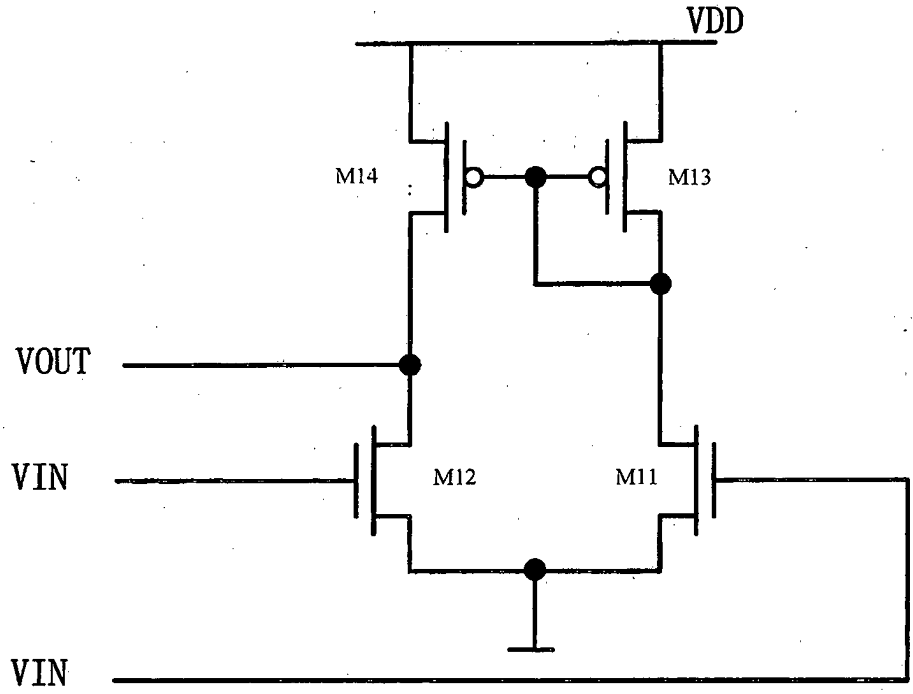
VDD
M14
M13
VOUT
VIN
M12
M11
VIN

Fig.6B

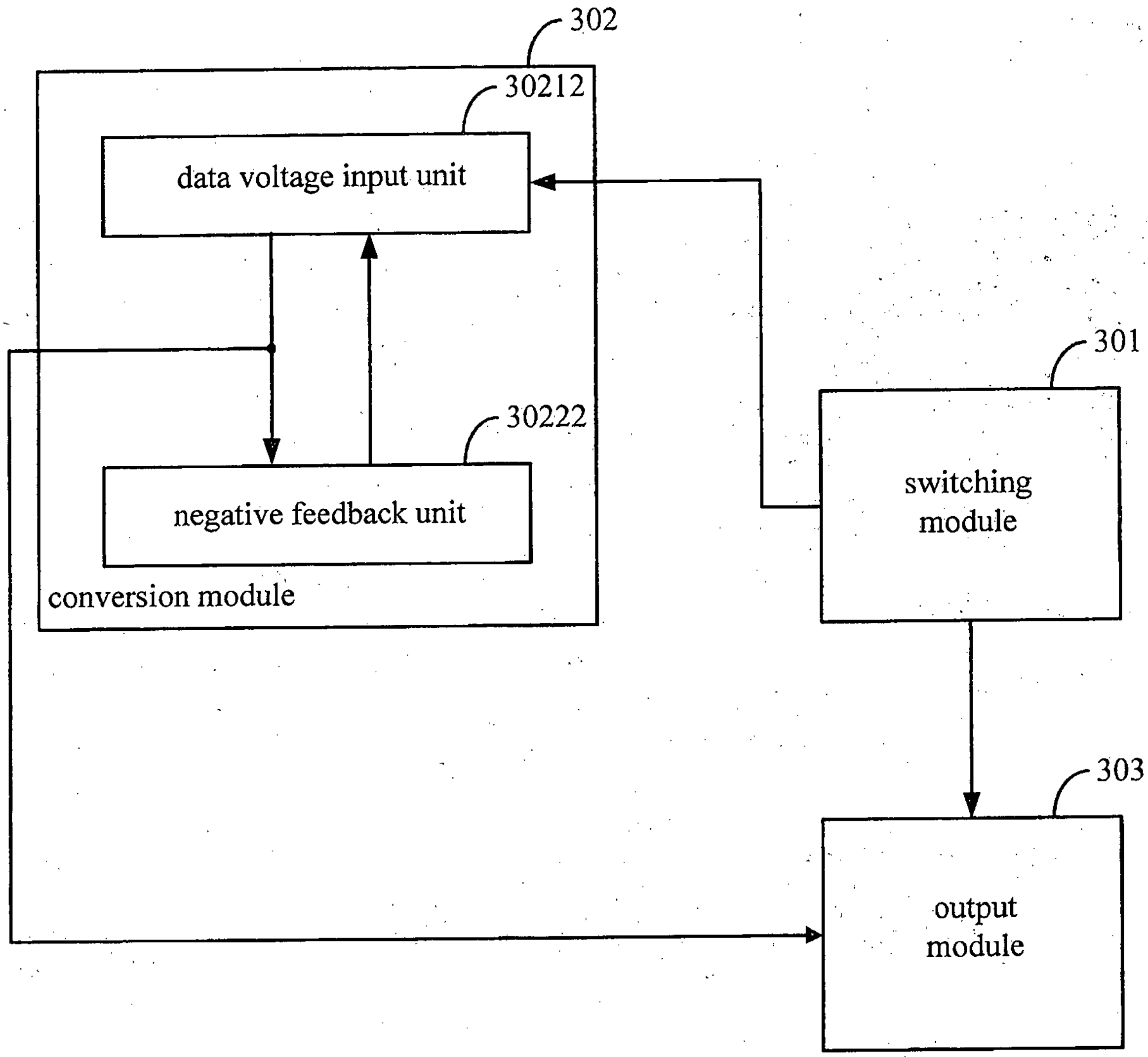
302
30212
data voltage input unit
30222
negative feedback unit
conversion module
301
switching module
303
output module

Fig.6C

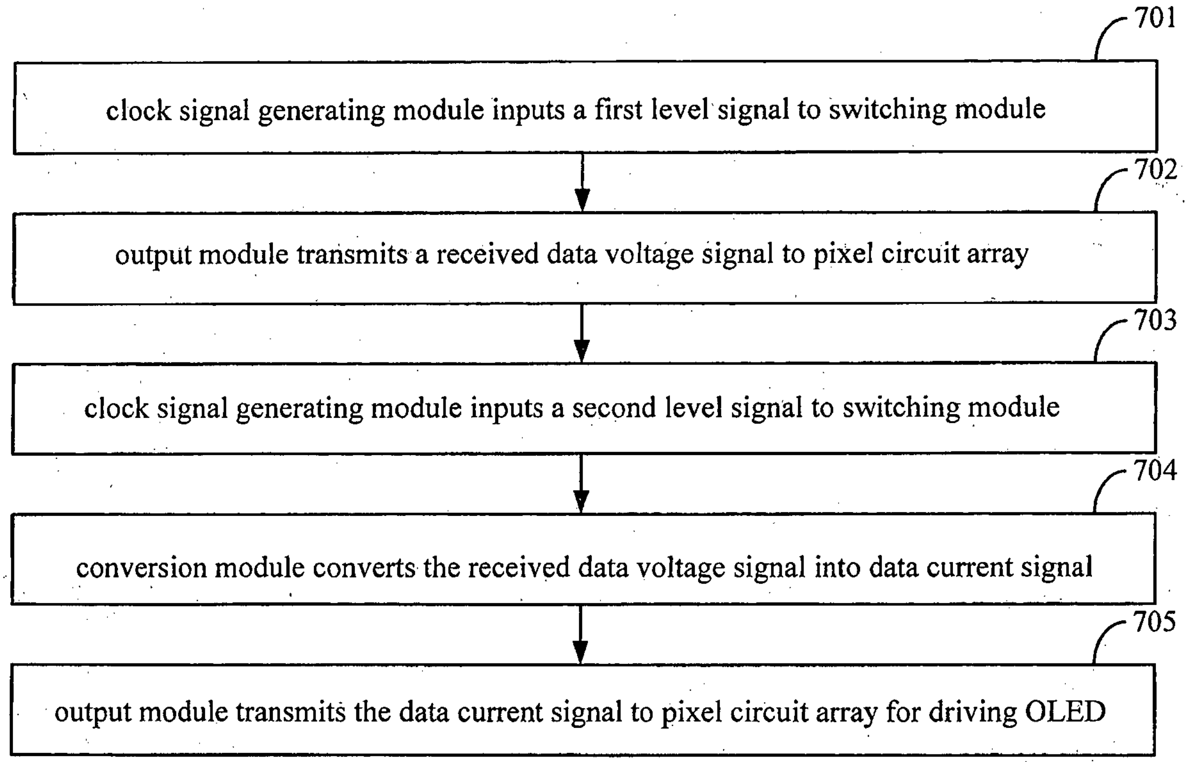
701
clock signal generating module inputs a first level signal to switching module
702
output module transmits a received data voltage signal to pixel circuit array
703
clock signal generating module inputs a second level signal to switching module
704
conversion module converts the received data voltage signal into data current signal
705
output module transmits the data current signal to pixel circuit array for driving OLED

Fig.7

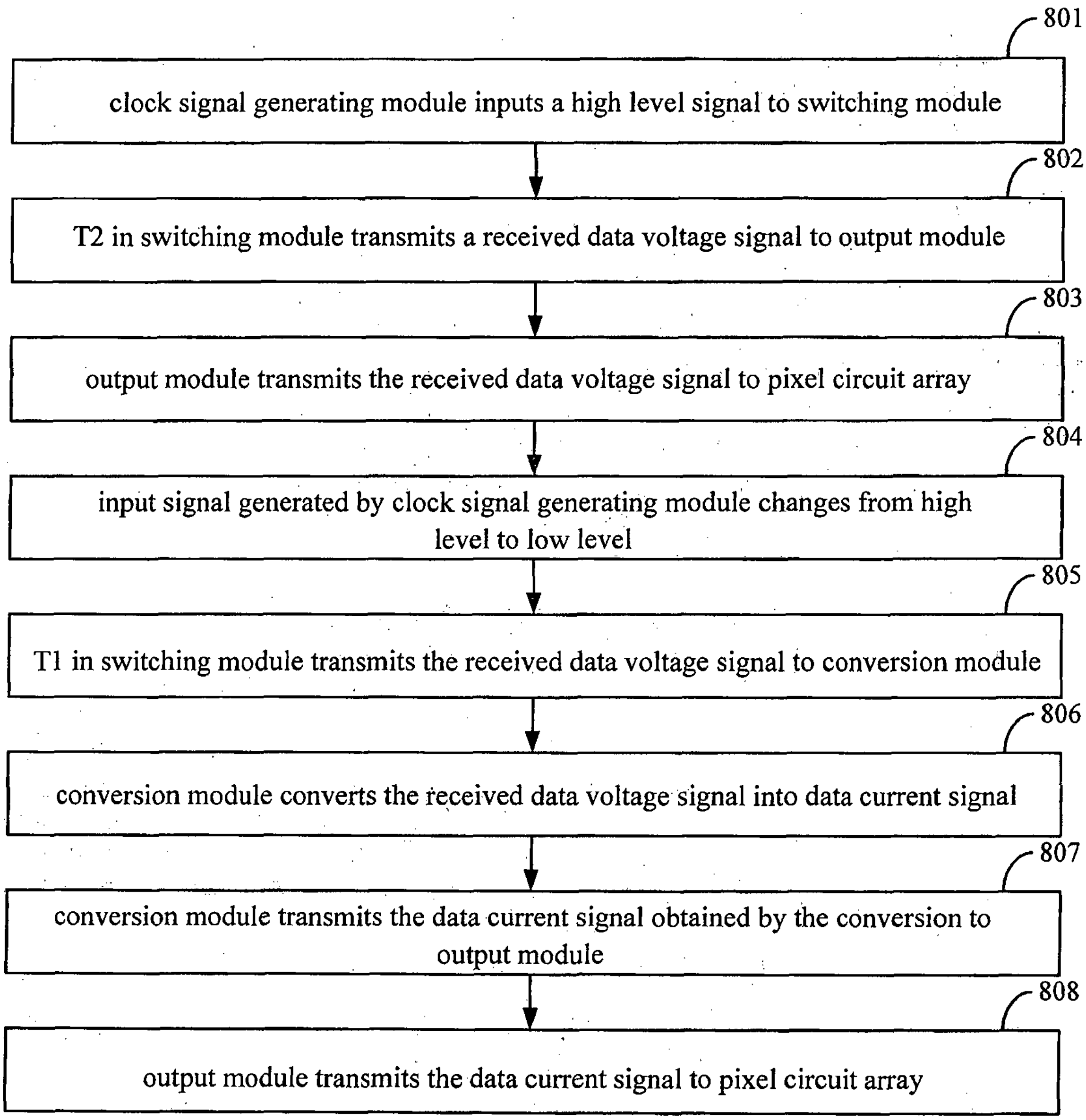
801
clock signal generating module inputs a high level signal to switching module
802
T2 in switching module transmits a received data voltage signal to output module
803
output module transmits the received data voltage signal to pixel circuit array
804
input signal generated by clock signal generating module changes from high level to low level
805
T1 in switching module transmits the received data voltage signal to conversion module
806
conversion module converts the received data voltage signal into data current signal
807
conversion module transmits the data current signal obtained by the conversion to output module
808
output module transmits the data current signal to pixel circuit array

Fig.8

REFERENCES CITED IN THE DESCRIPTION

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- US 2005168416 A1 **[0005]**
- US 2009040212 A1 **[0005]**

专利名称(译)	驱动装置，oled面板和用于驱动oled面板的方法		
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当前申请(专利权)人(译)	京东方科技集团股份有限公司.		
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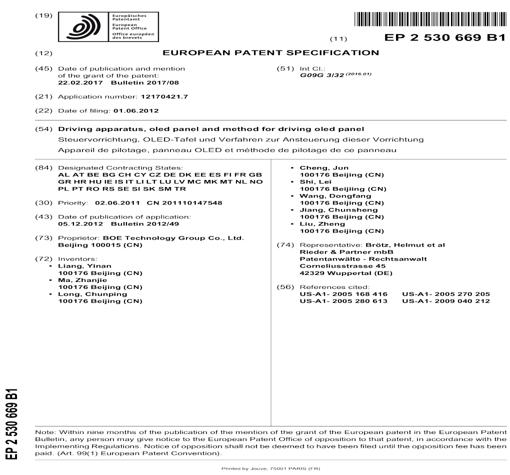
摘要(译)

本公开涉及驱动装置，OLED（有机发光二极管）面板和用于驱动OLED面板的方法。驱动装置可以集成在像素电路的基板上，并且能够提供快速且稳定的电流驱动。驱动装置包括切换模块，用于根据接收的时钟信号选择电压信号;转换模块，用于将电压信号转换为电流信号;输出模块，用于输出电压信号或转换后的电流信号以驱动像素电路阵列，其中，开关模块连接到转换模块和输出模块，转换模块连接到开关模块和输出模块。



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(54) Driving apparatus, oled panel and method for driving oled panel
Steuervorrichtung, OLED-Tafel und Verfahren zur Ansteuerung dieser Vorrichtung
Appareil de pilotage, panneau OLED et méthode de pilotage de ce panneau

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