(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 843 312 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention
of the grant of the patent:
06.05.2015 Bulletin 2015/19

(51) Int Cl.:
G09G 3/20 $^{(2006.01)}$ ***G09G 3/32*** $^{(2006.01)}$

(21) Application number: **07103920.0**

(22) Date of filing: **12.03.2007**

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(54) Data driver and organic light emitting display using the same

Datentreiber und organische lichtemittierende Anzeige damit

Lecteur de données et afficheur organique électroluminescent l'utilisant

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(84) Designated Contracting States:
DE FR GB

(30) Priority: **06.04.2006 KR 20060031637**

(43) Date of publication of application:
10.10.2007 Bulletin 2007/41

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- **MATSUEDA Y ET AL: "35.1: 2.5-in. AMOLED with Integrated 6-Bit Gamma Compensated Digital Data Driver" 2004 SID INTERNATIONAL SYMPOSIUM. SEATTLE, WA, MAY 25 - 27, 2004, SID INTERNATIONAL SYMPOSIUM, SAN JOSE, CA : SID, US, 25 May 2004 (2004-05-25), pages 1116-1119, XP007011917**

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Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a data driver and an organic light emitting display using the same. More particularly, the present invention relates to a data driver which is formed of PMOS transistors, and an organic light emitting display using the same.

2. Description of the Related Art

[0002] Various flat panel displays having reduced weight and volume as compared to cathode ray tubes (CRTs) have been developed. These flat panel displays include, e.g., a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), an organic light emitting display, etc.

[0003] The organic light emitting display may display an image using an organic light emitting diode (OLED) that generates light by recombining an electron and a hole. The organic light emitting display may offer certain advantages, since it may exhibit low power consumption and may provide a rapid response time.

[0004] The organic light emitting display may include pixels arranged in a matrix, a data driver configured to drive data lines connected to the pixels, and a scan driver configured to drive scan lines connected to the pixels.

[0005] During operation, the data driver may supply data signals corresponding to data within every horizontal period, so as to display a predetermined image in the pixels. The scan driver may select pixels to which the data signals are supplied by sequentially supplying a scan signal within every horizontal period.

[0006] EP 1 300 826 A2 discloses a HD display device with a data driver including a digital/analog converter. External to the display panel a controller IC is provided. The width of the data bus between the controller IC and the data driver is adapted to reduce the operating frequency of the data driver.

[0007] Matsueda Y et al: "35.1: 2.5-in. AMOLED with integrated 6-Bit Gamma Compensated Digital Data Driver" 2004 SID INTERNATIONAL SYMPOSIUM. SEATTLE, WA, MAY 25 - 27, 2004, SID INTERNATIONAL SYMPOSIUM, SAN JOSE, CA: SID, US, 25 May 2004 (2004-05-25), pages 1116-1119, discloses an AMOLED with an integrated data driver, wherein the data driver consists of CMOS circuitry.

[0008] US 2004/119666 A1 discloses a driving circuit for a flat panel display.

[0009] WO 2004/086347 A2 discloses a display device comprising a drive circuit with a data driver. The data driver has a plurality of current holding circuits for the plurality of display pixels.

[0010] As a panel of the organic light emitting display increases in size, it may be desirable to mount the data driver in the panel, in order to reduce the size, weight and manufacturing expense associated with the display. It may be difficult, however, to mount a conventional data driver in the panel because the conventional data driver may include PMOS transistors and NMOS transistors. Therefore, it may be desirable to have a data driver that is implemented with only PMOS transistors, so that the data driver may be mountable in the panel.

SUMMARY OF THE INVENTION

[0011] The present invention is therefore directed to a data driver, and an organic light emitting display using the same, that substantially overcome one or more of the problems due to the limitations and disadvantages of the related art.

[0012] It is therefore a feature of an exemplary embodiment of the present invention to provide a data driver which is formed of PMOS transistors and which is mountable in a panel, and an organic light emitting display using the same.

[0013] At least one of the above and other features and advantages of the present invention are realized by providing a data driver including a shift register unit configured to receive a first clock signal, a second clock signal, and a start pulse, and to generate a sampling pulse, a sampling latch unit configured to receive and output bits and reversed bits of digital data, in correspondence with the sampling pulse, a holding latch unit configured to receive the bits and reversed bits output by the sampling latch unit, and to output the bits and reversed bits, in correspondence with a first enable signal and a second enable signal, and a digital-to-analog converter configured to receive the bits and reversed bits output by the holding latch unit and to generate an analog signal corresponding to values of the received bits and reversed bits. The shift register unit includes at least one shift register, the sampling latch unit includes at least one sampling latch, and the holding latch unit includes at least one holding latch, and the shift register, the sampling latch, and the holding latch are substantially the same. The shift register, the sampling latch, and the holding latch each include a first transistor having a gate electrode connected to a second input terminal, a second electrode connected to a first node, and a first electrode connected to an external input terminal, a second transistor having a gate electrode connected to the first node, a first electrode connected to a first input terminal, and a second electrode connected to an output terminal, a third transistor having a gate electrode connected to the second input terminal, a first electrode connected to a second node, and a second electrode connected to a fourth power supply, a fourth transistor having a gate electrode connected to the first node, a first electrode connected to the second input terminal, and a second electrode connected to the second node, a fifth transistor having a gate electrode connected to the second node, a first electrode connected to a third power supply, and a second electrode connected to the output terminal, and a capacitor connected between the gate electrode and the second electrode of the second transistor. The first through fifth transistors are PMOS transistors.

[0014] The shift register unit may include one shift register per channel. The sampling latch unit may include a predetermined number of sampling latches per channel, the predetermined number being twice a number of bits of input digital data. The holding latch unit may include the predetermined number of holding latches per channel.

[0015] The digital-to-analog converter may include a plurality of transistors configured to receive the bits and reversed bits output by the holding latch unit, and the transistors receiving the bits and reversed bits may be PMOS transistors.

[0016] A charging signal may be input at a high level to the sampling latch unit when the bits and reversed bits are input to the sampling latch unit. The first clock signal and the second clock signal may have a phase difference of about 180 degrees. The first clock signal and the second clock signal may both be at a high level during a predetermined period.

[0017] The third power supply may provide a higher voltage than that provided by the fourth power supply. The shift register unit may include even and odd-numbered shift registers, the first clock signal may be supplied to the first input terminals of the odd-numbered shift registers, and the second clock signal may be supplied to the second input terminals of the odd-numbered shift registers. The second clock signal may be supplied to the first input terminals of the even-numbered shift registers, and the first clock signal may be supplied to the second input terminals of the even-numbered shift registers.

[0018] In the shift register, when a low level signal is supplied to the second input terminal, the capacitor may be charged with a voltage that corresponds to the voltage supplied from the external input terminal, and when a high level signal is supplied to the second input terminal, a voltage may be supplied to the output terminal that corresponds to the voltage charged in the capacitor. In the sampling latch, the sampling pulse may be supplied to the second input terminal, and a charging signal may be supplied to the first input terminal. The sampling latch may receive each bit or reversed bit when the sampling pulse is at a low level and the charging signal is at a high level, and the sampling latch may output each bit or reversed bit when the sampling pulse is at a high level and the charging signal is at a low level. In the holding latch, the first enable signal may be provided to the second input terminal, and the second enable signal may be provided to the first input terminal.

[0019] The first enable signal and the second enable signal may have a phase difference of about 180 degrees. The holding latch may receive a signal from the sampling latch when the first enable signal is at a low level, and the received signal may be output by the holding latch when the first enable signal is at a high level. The first enable signal may be maintained at a high level during output by the sampling latch, and the first enable signal may change to a low level after output by the sampling latch.

[0020] The data driver may further include a conversion unit configured to receive the first clock signal, the second clock signal and the sampling pulse, and to sequentially generate a conversion signal, wherein the conversion signal may be supplied to the sampling latch unit. The conversion unit may have one conversion circuit per channel. The conversion circuit may include an input unit and an output unit, the input unit may be configured to receive the sampling pulse at an input terminal thereof and to control a signal that is supplied to the output unit, and the output unit may be configured to control whether or not the conversion signal is output, in correspondence with the signal controlled by the input unit and the sampling pulse input to the input terminal.

[0021] The output unit may include an eleventh transistor having a first electrode connected to a third power supply and having a second electrode connected to an output terminal, a twelfth transistor having a first electrode connected to the output terminal and having a second electrode connected to a fourth power supply, the fourth power supply providing a lower voltage than that provided by the third power supply, a thirteenth transistor having a gate electrode connected to a gate electrode of the eleventh transistor and having a first electrode connected to the second electrode of the eleventh transistor, a fourteenth transistor having a first electrode connected to a second electrode of the thirteenth transistor, having a second electrode connected to the fourth power supply, and having a gate electrode connected to the input unit, a fifteenth transistor having a first electrode connected to a third input terminal, having a second electrode connected to the gate electrode of the eleventh transistor, and having a gate electrode connected to a first input terminal, a twelfth capacitor connected between the gate electrode and the first electrode of the eleventh transistor, and an eleventh capacitor connected between a gate electrode of the twelfth transistor and the first electrode of the twelfth transistor. The data driver may further include a fourteenth capacitor connected between the output terminal and the fourth power supply.

[0022] The input unit may include a sixteenth transistor having a first electrode connected to the gate electrode of the fourteenth transistor and having a second electrode connected to the first input terminal, a seventeenth transistor having a first electrode connected to a gate electrode of the sixteenth transistor, and having a gate electrode and a second electrode both connected to a second input terminal, an eighteenth transistor having a gate electrode connected to the third input terminal, having a first electrode connected to the third power supply, and having a second electrode connected to the gate electrode of the sixteenth transistor, and a thirteenth capacitor connected between the gate electrode of the sixteenth transistor and the first electrode of the sixteenth transistor. The eleventh through eighteenth transistors may be PMOS transistors. The conversion unit may include even numbered and odd-numbered conversion circuits, and the odd-numbered conversion circuits may receive the first clock signal at the first input terminal, and may receive the second clock signal at the second input terminal. The even-numbered conversion circuits may receive the second clock signal at the first input terminal, and may receive the first clock signal at the second input terminal. The conversion circuit may output a signal level opposite to a signal input to the third input terminal if a low level signal is input to the first input terminal, and the conversion circuit may maintain an output of a previous period if a high level signal is input to the first input terminal.

[0023] At least one of the above and other features and advantages of the present invention may also be realized by providing an organic light emitting display, including a scan driver configured to sequentially supply a scan signal to scan lines, a data driver configured to supply a data signal to data lines, and a pixel unit including a plurality of pixels connected to the scan lines and the data lines, wherein the data driver includes a shift register unit configured to receive a first clock signal, a second clock signal, and a start pulse, and to sequentially generate a sampling pulse, a sampling latch unit configured to receive and output bits and reversed bits of digital data, in correspondence with the sampling pulse, a holding latch unit configured to receive the bits and reversed bits output by the sampling latch unit, and to output the bits and reversed bits, in correspondence with a first enable signal and a second enable signal, and a digital-to-analog converter configured to receive the bits and reversed bits output by the holding latch unit and to generate an analog signal corresponding to values of the received bits and reversed bits.

[0024] The data driver may further include a conversion unit configured to receive the first clock signal, the second clock signal and the sampling pulse, and to sequentially generate a conversion signal, and the conversion signal may be supplied to the sampling latch unit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

FIG. 1 illustrates a block diagram of an organic light emitting display according to an exemplary embodiment of the present invention;
FIG. 2 illustrates a circuit diagram of an exemplary embodiment of a pixel of FIG. 1;
FIG. 3 illustrates a basic block diagram of a first exemplary embodiment of a data driver of FIG. 1;
FIG. 4 illustrates a detailed block diagram of a first exemplary embodiment of a data driver of FIG. 3;
FIG. 5 illustrates a timing diagram for driving the data driver of FIG. 4;
FIG. 6 illustrates a circuit diagram of an exemplary shift register provided in a shift register unit of FIG. 4;
FIG. 7 illustrates a circuit diagram of an exemplary sampling latch provided in a sampling latch unit of FIG. 4;
FIG. 8 illustrates a circuit diagram of an exemplary holding latch provided in a holding latch unit of FIG. 4;
FIG. 9 illustrates a circuit diagram of an exemplary digital-to-analog converter (DAC) unit of FIG. 4;
FIG. 10 illustrates a basic block diagram of a second exemplary embodiment of a data driver of FIG. 1;
FIG. 11 illustrates a detailed block diagram of a second exemplary embodiment of a data driver of FIG. 10;
FIG. 12 illustrates a timing diagram for driving a data driver of FIG. 11;
FIG. 13 illustrates a circuit diagram of an exemplary conversion circuit of FIG. 11; and
FIG. 14 illustrates a timing diagram for driving a conversion circuit of FIG. 13.

DETAILED DESCRIPTION OF THE INVENTION

[0026] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are illustrated. The present invention may, however, be embodied in different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

[0027] FIG. 1 illustrates a block diagram of an organic light emitting display according to an exemplary embodiment of the present invention. Referring to FIG. 1, the organic light emitting display may include a pixel unit 30 including a plurality of pixels 40 connected to scan lines (S1...Sn) and data lines (D1...Dm), a scan driver 10 configured to drive the scan lines (S1...Sn), a data driver 20 configured to drive the data lines (D1...Dm), and a timing controller 50 configured to control the scan driver 10 and the data driver 20.

[0028] The timing controller 50 may generate a data driver control signal (DCS) and a scan driver control signal (SCS) in correspondence to synchronization signals supplied from an external source. The data driver control signal (DCS) and the scan driver control signal (SCS) generated by the timing controller 50 may be supplied to the data driver 20 and the scan driver 10, respectively. The timing controller 50 may receive data from an external source and supply the (DATA) to the data driver 20.

[0029] The data driver 20 may receive the data driver control signal (DCS) from the timing controller 50. The data driver 20 may generate data signals and supply the generated data signals to the data lines (D1 to Dm), so as to synchronize with a scan signal.

[0030] The pixel unit 30 may receive a first power supply (ELVDD) and a second power supply (ELVSS) from an external source, and supply them to each of the pixels 40. Each of the pixels 40 receiving the first power supply (ELVDD) and the second power supply (ELVSS) may generate light corresponding to the data signal by controlling a current flowing from the first power supply (ELVDD) to the second power supply (ELVSS) via an electroluminescent device.

[0031] The scan driver 10 may receive the scan driver control signal (SCS) from the timing controller 50. The scan driver 10 may generate a scan signal and sequentially supply the generated scan signal to the scan lines (S 1 to Sn).

[0032] FIG. 2 illustrates a circuit diagram of an exemplary embodiment of a pixel of FIG. 1. For the sake of discussion, a pixel 40 connected to an nth scan line (Sn) and an mth data line (Dm) will be described, as illustrated in FIG. 2. Referring to FIG. 2, the pixel 40 may include an OLED and a pixel circuit 42 connected to the data line (Dm) and the scan line (Sn), so as to control whether or not the OLED may emit light.

[0033] An anode electrode of the OLED may be connected to the pixel circuit 42, and a cathode electrode of the OLED may be connected to the second power supply (ELVSS). The OLED may emit light in correspondence to a current supplied from the pixel circuit 42. That is, the pixel circuit 42 receiving the data signal supplied to the data line (Dm) may control whether or not the OLED emits light when the scan signal is supplied to the scan line (Sn).

[0034] The pixel circuit 42 may include a first transistor (M1) connected to a second transistor (M2), the data line (Dm), and the scan line (Sn). The pixel circuit 42 may also have the second transistor (M2) connected between the first power supply (ELVDD) and the OLED, and a storage capacitor (C) connected between a gate electrode and a first electrode of the second transistor (M2).

[0035] A gate electrode of the first transistor (M1) may be connected to the scan line (Sn), and a first electrode of the first transistor (M1) may be connected to the data line (Dm). A second electrode of the first transistor (M1) may be connected to one terminal of the storage capacitor (C). The first transistor (M1) may supply the data signal to the storage capacitor (C), since the first transistor (M1) may be turned on when the scan signal is supplied to the scan line (Sn). It is to be understood that the first electrode of the first transistor (M1) may be a source electrode or a drain electrode. For example, if the first electrode of the first transistor (M1) is the source electrode, the second electrode of the first transistor (M1) may be the drain electrode, and vice versa.

[0036] The gate electrode of the second transistor (M2) may be connected to one terminal of the storage capacitor (C), and the first electrode of the second transistor (M2) may be connected to the other terminal of the storage capacitor (C) and the first power supply (ELVDD). The second electrode of the second transistor (M2) may be connected to the OLED.

[0037] In this exemplary arrangement, the second transistor (M2) may control whether or not the OLED emits light according to the voltage stored in the storage capacitor (C). That is, the second transistor (M2) may allow the OLED to emit light when a predetermined voltage corresponding to the data signal is stored in the storage capacitor (C), and a current corresponding to the predetermined voltage may be supplied to the OLED.

[0038] FIG. 3 illustrates a basic block diagram of a first exemplary embodiment of a data driver of FIG. 1. The data driver 20 will be described assuming that it includes "m" channels. Referring to FIG. 3, the data driver 20 may include a shift register unit 100, a sampling latch unit 300, a holding latch unit 400, and a digital-analog converter (DAC) unit 500.

[0039] The shift register unit 100 may receive a start pulse (SP), a first clock signal (CLK1), and a second clock signal (CLK2), to sequentially generate a sampling pulse (SAP). The shift register unit 100 may include "m" shift registers.

[0040] The sampling latch unit 300 may receive the sampling pulse (SAP) and a charging signal (CH). The sampling latch unit 300 may also receive each bit and reversed bit of the input digital data, and may store the bit and the reversed bit of the input digital data. Accordingly, the sampling latch unit 300 may include twice as many sampling latches as the number of bits of the digital data input into every channel. For example, if a 6-bit digital data is input, then the sampling latch unit 300 may include 12 (=6x2) sampling latches in every channel. Each sampling latch may store the bit (DATA) or the reversed bit (/DATA) of the input digital data.

[0041] The holding latch unit 400 may receive a first enable signal (EN1) and a second enable signal (EN2). The holding latch unit 400 may simultaneously receive each bit and reversed bit output from the sampling latch unit 300. The holding latch unit 400 may output each bit and reversed bit to the DAC unit 500. Accordingly, similar to the sampling latch unit 300, the holding latch unit 400 also may have twice as many holding latches as the number of bits of the digital data input into every channel. For example, if a 6-bit digital data is input, then the holding latch unit 400 may include 12 (=6x2) holding latches in every channel.

[0042] The DAC unit 500 may generate an analog signal corresponding to each bit value of the digital data output from the holding latch unit 400. For example, the DAC unit 500 may select one of a plurality of gray scale voltages to correspond to the bit value of the digital data supplied from the holding latch unit 400 and generate an analog data signal. The DAC unit 500 may supply analog data signals to the data lines (D1 to Dm), respectively. The DAC unit 500 may include "m" number of DACs.

[0043] FIG. 4 illustrates a detailed block diagram of a first exemplary embodiment of a data driver of FIG. 3, and FIG. 5 illustrates a timing diagram for driving the data driver of FIG. 4. FIG. 4 will be described assuming that the data driver includes "m" number of channels and 6-bit digital data is input. However, it is to be understood that this is merely an exemplary implementation, and the present invention is not limited thereto. Also, FIG. 5 illustrates a timing diagram in which a most significant bit and a reversed most significant bit of the digital data may be input into every channel.

[0044] Referring to FIG. 4, the shift register unit 100 may include one shift register (SR1...SRm) per channel. The sampling latch unit 300 may include 12 sampling latches per channel, e.g., sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12). The holding latch unit 400 may include 12 holding latches per channel, e.g., holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12). For clarity, FIG. 4 primarily illustrates the shift registers, the sampling latches, and the holding latches for the first channel only.

[0045] Odd-numbered shift registers (SR1, SR3, ..., SRm-1) of the shift registers (SR1...SRm) may receive the first clock signal (CLK1) through respective first input terminals (clk) and may receive the second clock signal (CLK2) through respective second input terminals (/clk). Even-numbered shift registers (SR2, SR4, ..., SRm) may receive the second clock signal (CLK2) through respective first input terminals (clk) and may receive the first clock signal (CLK1) through respective second input terminals (/clk). The first clock signal (CLK1) and the second clock signal (CLK2) may have a phase difference, e.g., about 180°. The first clock signal (CLK1) and the second clock signal (CLK2) may both be at a high level at the same time during a predetermined period, as illustrated in FIG. 5.

[0046] The first shift register (SR1) may receive the first clock signal (CLK1), the second clock signal (CLK2), and the start pulse (SP) to generate a first sampling pulse (SAP1). A second shift register (SR2) may receive a first clock signal (CLK1), a second clock signal (CLK2) and a first sampling pulse (SAP1) to generate a second sampling pulse (SAP2). That is, the shift registers (SR1...SRm) may receive the start pulse (SP) or the sampling pulse (SAP) of a previous stage, so as to sequentially generate a sampling pulse (SAP), as illustrated in FIG. 5.

[0047] The sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) may receive the charging signal (CH) through respective first input terminals (clk) and the sampling pulse (SAP) through respective second input terminals (/clk). The sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) may also receive each bit or reversed bit of the digital data and may store each bit or reversed bit of the digital data. For example, the sampling latches (SAL1_1...SAL1_12) corresponding to the first channel may receive the charging signal (CH) through the respective first input terminals (clk) and may receive the first sampling pulse (SAP1) through the respective second input terminals (/clk). The sampling latches (SAL1_1...SAL1_12) may also receive each bit or reversed bit of the digital data corresponding to the first channel, and store the bit and the reversed bit of the digital data.

[0048] In an implementation, a first sampling latch (SAL1_1) provided in the first channel may receive a most significant bit, e.g., D[5] (a1 in FIG. 5) of the digital data, and may store the most significant bit D[5] of the digital data when the first sampling pulse (SAP1) and the charging signal (CH) are supplied to the first sampling latch. A second sampling latch (SAL1_2) may receive a reversed most significant bit, e.g., /D[5] (/a1 in FIG. 5) of the digital data, and may store the reversed most significant bit /D[5] when the first sampling pulse (SAP1) and the charging signal (CH) are supplied to the second sampling latch (SAL1_2).

[0049] The remaining sampling latches (SAL1_3...SAL1_12) provided in the first channel may receive each bit or reversed bit (D[4], /D[4], D[3], /D[3], D[2], /D[2], D[1], /D[1], D[0], /D[0]) of the digital data, and may store the bit or the reversed bit of the digital data when the first sampling pulse (SAP1) and the charging signal (CH) are supplied to the remaining sampling latches (SAL1_3...SAL1_12), in the same manner as described above. As illustrated in FIG. 5, the charging signal (CH) may be at a high level during the period when the digital data is input to the sampling latches (SAL1_1...SAL1_12).

[0050] The holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) may receive the second enable signal (EN2) through respective first input terminals (clk) and may receive the first enable signal (EN1) through respective second input terminals (/clk). The holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) receiving the first enable signal (EN1) and the second enable signal (EN2) may simultaneously receive each of the bits of the digital data stored in the sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12). The holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) may output each of the bits of the received digital data to the DAC unit 500.

[0051] In an implementation, the holding latches (HOL1_1...HOL1_12) corresponding to the first channel may receive the second enable signal (EN2) through the respective first input terminals (clk) and may receive the first enable signal (EN1) through the respective second input terminals (/clk), and may simultaneously receive each bit or reversed bit of the digital data stored in the sampling latches (SAL1_1...SAL1_12) corresponding to the first channel. The holding latches (HOL1_1...HOL1_12) may output the bit or the reversed bit of the digital data to the DAC of the first channel.

[0052] For example, the first holding latch (HOL1_1) provided in the first channel may receive the bit D[5] stored in the first sampling latch (SAL1_1), and the second holding latch (HOL1_2) may receive the reversed bit /D[5] stored in the second sampling latch (SAL1_2). Similarly, the holding latches (HOL1_3...HOL1_12) provided in the first channel may simultaneously receive each bit or reversed bit (D[4], /D[4], D[3], /D[3], D[2], /D[2], D[1], /D[1], D[0], /D[0]) of the digital data stored in the sampling latches (SAL1_3...SAL1_12), and may output the bit or the reversed bit to the DAC of the first channel, in the same manner as described above.

[0053] The bit and the reversed bit respectively output from the holding latches (HOL1_1...HOL1_12) may be input to each of the corresponding terminals of the DAC provided in every channel. The DACs may select one of a plurality of gray scale voltages to correspond to the bit value of the digital data supplied from the holding latches. The DACs may respectively generate an analog data signal corresponding to the selected gray scale voltage, so as to respectively supply the analog signal to the data lines (D1...Dm).

[0054] FIG. 6 illustrates a circuit diagram of an exemplary shift register provided in a shift register unit of FIG. 4. Referring to FIG. 6, the shift register (SR) may receive the start pulse (SP) or the sampling pulse (SAP) of a previous stage. The shift register (SR) may include a first transistor (M1) having a gate electrode connected to a second input terminal (/clk), a second transistor (M2) connected between the first transistor (M1) and an output terminal (out), a third transistor (M3) and a fourth transistor (M4) connected respectively between a fourth power supply VSS and the second input terminal (/clk), a fifth transistor (M5) connected between a third power supply (VDD) and the output terminal (out), and a capacitor (C1) connected between a gate electrode and a second electrode of the second transistor (M2). The first through fifth transistors (M1...M5) may each be a PMOS transistor. The third power supply (VDD) may have a higher voltage compared to the voltage of the fourth power supply (VSS).

[0055] A first electrode of the first transistor (M1) may receive the start pulse (SP) or the sampling pulse (SAP) of a previous stage. The first electrode may be connected to an external input terminal. The gate electrode of the first transistor (M1) may be connected to the second input terminal (/clk), and the second electrode of the first transistor (M1) may be connected to a first node (N1). The first transistor (M1) may be turned on or turned off in correspondence to a first clock signal (CLK1) or a second clock signal (CLK2) supplied to the second input terminal (/clk).

[0056] A gate electrode of the second transistor (M2) may be connected to the first node (N1), and a first electrode of the second transistor (M2) may be connected to the first input terminal (clk). The second electrode of the second transistor (M2) may be connected to the output terminal (out). The second transistor (M2) may be turned on or turned off in correspondence to a voltage of the first node (N1).

[0057] A first electrode of the third transistor (M3) may be connected to a second node (N2), and a second electrode of the third transistor (M3) may be connected to the fourth power supply (VSS). A gate electrode of the third transistor (M3) may be connected to the second input terminal (/clk). The third transistor (M3) may be turned on or turned off in correspondence to the first clock signal (CLK1) or the second clock signal (CLK2) supplied to the second input terminal (/clk).

[0058] A first electrode of the fourth transistor (M4) may be connected to the second input terminal (/clk), and a second electrode of the fourth transistor (M4) may be connected to the second node (N2). A gate electrode of the fourth transistor (M4) may be connected to the first node (N1). The fourth transistor (M4) may be turned on or turned off in correspondence to a voltage of the first node (N1).

[0059] A first electrode of the fifth transistor (M5) may be connected to the third power supply (VDD), and a second electrode of the fifth transistor (M5) may be connected to the output terminal (out). A gate electrode of the fifth transistor (M5) may be connected to the second node (N2). The fifth transistor (M5) may be turned on or turned off in correspondence to a voltage of the second node (N2).

[0060] The capacitor (C1) may be connected between the gate electrode and the second electrode of the second transistor (M2). A voltage charged in the capacitor (C1) may correspond to the start pulse (SP) or the sampling pulse

[0061] (SAP) of the previous stage supplied to the first node (N1) when the first transistor (M1) may be turned on.

[0062] An exemplary operation of a shift register (SR) will now be described, taking the first shift register (SR1) as a particular example. For the sake of discussion, it will be assumed that the fourth power supply (VSS) may be a low level voltage, and the third power supply (VDD) may be a high level voltage of the clock signals (CLK1, CLK2). The fourth power supply (VSS) may have a lower voltage compared to the voltage of the third power supply (VDD). For example, the fourth power supply (VSS) may be a ground voltage.

[0063] The first transistor (M1) and the third transistor (M3) may be turned on when the first clock signal (CLK1) at a high level is input, the second clock signal (CLK2) at a low level is input, and a start pulse (SP) at a low level is be input, as illustrated in FIG. 5. If the first transistor (M1) is turned on, then the start pulse (SP) at a low level may be supplied to the first node (N1). The second transistor (M2) and the fourth transistor (M4) may be turned on.

[0064] If the fourth transistor (M4) is turned on, then a low level of the second clock signal (CLK2) may be supplied to the second node (N2). If the third transistor (M3) is turned on, then the fourth power supply (VSS) may be supplied to the second node (N2). The fifth transistor (M5) may be turned on to supply the voltage of the third power supply (VDD) to the output terminal (out). If the second transistor (M2) is turned on, then the first clock signal (CLK1) at a high level may be supplied to the output terminal (out).

[0065] At this time, a voltage corresponding to a difference between the first node (N1) and the output terminal (out) may be charged in the capacitor (C1). That is, the voltage corresponding to the difference between the low voltage of the start pulse (SP) and the third power supply (VDD) may be charged in the capacitor (C1).

[0066] Subsequently, the first clock signal (CLK1) may be at a low level, the second clock signal (CLK2) may be a high level, and the start pulse (SP) may be at a high level. The first transistor (M1) and the third transistor (M3) receiving the second clock signal (CLK2) at a high level may be turned off. The first node (N1) may be set to a low level in correspondence to the voltage charged in the capacitor (C1). The second transistor (M2) may be turned on, and a voltage of the output terminal (out) may decrease to a low level voltage of the first clock signal (CLK1). That is, a first sampling pulse (SAP1) may be generated, as illustrated in FIG. 5.

[0067] If the voltage of the first node (N1) is at a low level, the fourth transistor (M4) may be turned on. If the fourth transistor (M4) is turned on, then the second clock signal (CLK2) at a high level may be supplied to the second node (N2). Accordingly, the fifth transistor (M5) may be turned off.

[0068] Subsequently, the first clock signal (CLK1) may be at a high level, the second clock signal (CLK2) may be at a low level, and the start pulse (SP) may be at a high level. The first transistor (M1) and the third transistor (M3) receiving the second clock signal (CLK2) at a low level may be turned on. If the third transistor (M3) is turned on, then a voltage of the fourth power supply (VSS) may be supplied to the second node (N2). The fifth transistor (M5) may be turned on, and the voltage of the third power supply (VDD) may be supplied to the output terminal (out).

[0069] If the first transistor (M1) is turned on, then a high level voltage may be supplied to the first node (N1). The high level voltage may not be charged in the capacitor (C1). Accordingly, the second transistor (M2) and the fourth transistor (M4) may be turned on, although the phases of the next clock signals (CLK1, CLK2) are reversed. The shift register (SR) may output at a high level.

[0070] That is, the shift register (SR) may store a low level voltage in the capacitor (C1) during a half cycle of the clock signals (CLK1, CLK2) and output a low level voltage, i.e., the sampling pulse (SAP), during the other half cycle of the clock signals (CLK1, CLK2) when a low level voltage may be input to an external input terminal.

[0071] The second shift register (SR2) may charge a voltage corresponding to a first sampling pulse (SAP1) in the capacitor (C1) when the first clock signal (CLK1) at a low level, the second clock signal (CLK2) at a high level, and the first sampling pulse (SAP1) may be input. The second shift register (SR2) may output a second sampling pulse (SAP2) when the first clock signal (CLK1) may be at a high level, and the second clock signal (CLK2) may be at a low level. The shift registers (SR1...SRm) may sequentially output sampling pulses (SAP1 to SAPm) by repeating this operation, as described above.

[0072] As illustrated in FIG. 5, when the first and the second clock signals (CLK1, CLK2) are both at a high level, the previous output may be maintained if, during the previous procedure, the first clock signal (CLK1) was at a low level and the second clock signal (CLK2) was at a high level. Also, since many of the high levels of the first and second clock signals (CLK1, CLK2) may overlap, i.e., be high at the same time, a gap may be generated between output pulses of the adjacent shift registers (SR) because the output is at a high level if the first clock signal (CLK1) is at a high level and the second clock signal (CLK2) is at a low level.

[0073] FIG. 7 illustrates a circuit diagram of an exemplary sampling latch provided in a sampling latch unit of FIG. 4. The first sampling latches (SAL1_1, SAL2_1, ..., SALm_1) of the sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12). The first sampling latches (SAL1_1, SAL2_1, ... , SALm_1) may receive a most significant bit, e.g., the bit D[5]. Referring to FIG. 7, each of the sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12), as illustrated in FIG. 4, may be implemented with the same circuit as the shift register (SR), as illustrated in FIG. 6. However, the sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) may receive the charging signal (CH) through the respective first input terminals (clk), and may receive the sampling pulse (SAP) through the respective second input terminal (/clk).

[0074] An exemplary operation of the first sampling latch (SAL1_1) in the first channel will now be described in connection with the timing diagram illustrated in FIG. 5. The first sampling latch (SAL1_1) may receive a most significant bit, e.g., the bit D[5] (a1 of FIG. 5), when the first sampling pulse (SAP1) is at a low level and the charging signal (CH) is at a high level. The bit D[5] input to the first sampling latch (SAL1_1) may be stored in the capacitor (C1). The fifth transistor (M5) may be turned on, since the first sampling pulse (SAP1) may be at a low level. Accordingly, a high level voltage may be output from the output terminal (out).

[0075] Subsequently, if the first sampling pulse (SAP1) is at a high level, and the charging signal (CH) is at a high level, then a voltage corresponding to the D[5] may be output through the output terminal (out). For example, a low level voltage may be output through the output terminal (out) if the bit D[5] (a1) is a low level voltage, and a high level voltage may be output through the output terminal (out) if the bit D[5] (a1) is a high level voltage.

[0076] In the same manner as described above, the first sampling latch (SAL2_1) provided in the second channel may also receive a most significant bit, e.g., the bit D[5] (a2 of FIG. 5) of the digital data when the second sampling pulse (SAP2) is at a low level and the charging signal (CH) is at a high level. The bit D[5] of the digital data may be stored in the capacitor (C1). Subsequently, the second sampling pulse (SAP2) may be at a high level, the charging signal (CH) may be at a low level, and a voltage corresponding to the bit D[5] may be output through the output terminal (out).

[0077] The second sampling latch (SAL2_2) may receive the reversed bit /D[5] (/a1, /a2,..., /an in FIG. 5), and may store the reversed bit /D[5] in the capacitor (C1) when each of the sampling pulses (SAP1, SAP2, ..., SAPm) are at a low level and the charging signal (CH) is at a high level. Thus, the second sampling latch (SAL2_2) may operate in the same manner as the first sampling latches (SAL1_1, SAL2_1, ..., SALm_1) provided in each of the channels. The voltage corresponding to the reversed bit /D[5] may be output from the output terminal (out) if the sampling pulses (SAP1, SAP2, ..., SAPm) are at a high level and the charging signal (CH) is at a low level.

[0078] The sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) may receive a bit or a reversed bit of the digital data when a sampling pulse (SAP) and a charging signal (CH) are supplied to the sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12). The sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) may output a voltage corresponding to the received bit through the output terminal (out).

[0079] FIG. 8 illustrates a circuit diagram of an exemplary holding latch provided in a holding latch unit of FIG. 4. Referring to FIG. 8, each of the holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12), as illustrated in FIG. 4, may be implemented with the same circuit as the shift register (SR), as illustrated in FIG. 6. However, the holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) may receive the second enable signal (EN2) through the respective first input terminals (clk), and may receive the first enable signal (EN1) through the respective second input terminals (/clk).

[0080] An exemplary operation will now be described in connection with the timing diagram illustrated in FIG. 5. When the sampling latches (SAL1...SALm) output the digital data, the first enable signal (EN1) may be at a low level and the second enable signal (EN2) may be at a high level, as illustrated in FIG. 5. Subsequently, each of the holding latches may receive a data bit output from each of the sampling latches (SAL1 to SALm). The data bits input to the holding latches may be stored in the capacitor (C1) included in each of the holding latches.

[0081] Then, if the first enable signal (EN1) may be at a high level, and the second enable signal (EN2) may be at a low level, each of the holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) may output a voltage (high or low) corresponding to the data bit stored in each of the holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) to the DAC unit 500.

[0082] For example, the first holding latch (HOL1_1) provided in the first channel may receive the bit D[5] (a1 of FIG. 5) output from the first sampling latch (SAL1_1), and then store the bit D[5] in the capacitor (C1) when the first enable signal (EN1) is at a low level and the second enable signal (EN2) is at a high level. Subsequently, if the first enable signal (EN1) is at a high level, and the second enable signal (EN2) is at a low level, then the first holding latch (HOL1_1) may output a voltage (high or low) corresponding to the stored D[5] (a1) to the DAC of the first channel.

[0083] In the same manner as described above, the first holding latch (HOL2_1) provided in the second channel may also receive the bit D[5] output from the first sampling latch (SAL2_1) and may store the bit D[5] in the capacitor (C1) when the first enable signal (EN1) is at a low level and the second enable signal (EN2) is at a high level. The first holding latch (HOL1_1) may output a voltage (high or low) corresponding to the stored bit D[5] to the DAC of the first channel when the first enable signal (EN1) is at a high level and the second enable signal (EN2) is at a low level.

[0084] The second holding latch (HOL2_2) may output a voltage corresponding to the reversed bit /D[5] to the DAC of the second channel during the above-mentioned operation, since it may operate in the same manner as the first holding latches (HOL1_1, HOL2_1,...,HOLm_1) provided in each of the channels.

[0085] FIG. 9 illustrates a circuit diagram of an exemplary digital-to-analog converter (DAC) unit of FIG. 4. For the sake of discussion, an exemplary DAC will be described assuming that it receives 6-bit digital data. Referring to FIG. 9, the DAC may be implemented using only PMOS transistors. The DAC may receive each bit and reversed bit of the 6-bit digital data output through the holding latch. The DAC may select one of a plurality of gray scale voltages to correspond to the bit and the reversed bit of the 6-bit digital data, and may generate an analog data signal corresponding to one of a plurality of gray scale voltages to supply the analog data signal to a data line, e.g., data line D1.

[0086] For example, if the input digital data is [000000], then V0 of the gray scale voltages may be selected and output. If the input digital data is [000001], then V1 of the gray scale voltages may be selected and output. If the input digital data is [111111], then V63 of the gray scale voltages may be selected and output. Therefore, a total of 64 gray scale voltages may be displayed if the 6-bit digital data is input. That is, a gray scale voltage corresponding to a specific digital data may be supplied to a data line corresponding to the specific digital data if the gray scale voltage corresponding to the specific digital data is selected.

[0087] FIG. 5 is described with reference to the above-mentioned operation of the shift registers (S/R), the sampling latches (SAL), the holding latches (HOL) and the DACs, as follows. It is assumed, however, that a most significant bit and a reversed most significant bit are input into every channel.

[0088] The odd-numbered shift registers (SR1, SR3, ...) may charge a voltage corresponding to the start pulse (SP) or the sampling pulse (SAP) of a previous stage when the second clock signal (CLK2) is at a low level, and may output a low level voltage to correspond to the start pulse (SP) or the sampling pulse (SAP) of the previous stage charged when the second clock signal (CLK2) is at a high level. The even-numbered shift registers (SR2, SR4, ...) may charge a voltage corresponding to the sampling pulse (sap) of the previous stage, when the first clock signal (CLK1) may be at a low level, and may output a low level voltage to correspond to the sampling pulse (sap) charged, when the first clock signal (CLK1) may be at a high level. Accordingly, the shift registers (SR1...SRm) may sequentially generate sampling pulses (SAP1 to SAPm), as illustrated in FIG. 5.

[0089] As illustrated in FIG. 5, when the first and second clock signals (CLK1, CLK2) are both at a high level the previous output may be maintained if, during the previous procedure, the first clock signal (CLK1) was at a low level and the second clock signal (CLK2) was at a high level. Also, since many of the high levels of the first and second clock signals (CLK1, CLK2) overlap, i.e., CLK1 and CLK2 are high at the same time, a gap may be generated between output pulses of the adjacent shift registers (SR) because the output is at a high level if the first clock signal (CLK1) is at a high level and the second clock signal (CLK2) is at a low level, as discussed previously.

[0090] Each of the first and second sampling latches (SAL1_1, SAL1_2, ..., SALm_1, SALm_2) provided in every channel may receive a most significant bit (D[5]) or a reversed most significant bit (/D[5]) and store the most significant bit (D[5]) or the reversed most significant bit (/D[5]) when the charging signal (CH) is at a high level and a sampling pulse (any one of SAP1 to SAPm) is supplied to the first and second sampling latches (SAL1_1, SAL1_2, ..., SALm_1, SALm_2). Subsequently, the first and the second sampling latches (SAL1_1, SAL1_2, ..., SALm_1, SALm_2) may simultaneously output a voltage corresponding to the stored data bit when the sampling pulse (any one of SAP1 to SAPm) is at a high level and the charging signal (CH) is at a low level.

[0091] That is, the first and the second sampling latches (SAL1_1, SAL1_2, ..., SALm_1, SALm_2) may receive the bit D[5] and the reversed bit /D[5] and store the bit D[5] and the reversed bit /D[5] in the capacitor (C1) when each of the sampling pulse (SAP1, SAP2, ..., SAPm) is at a low level and the charging signal (CH) is at a high level. Subsequently, the voltage corresponding to the bit D[5] and the reversed bit /D[5] may be simultaneously output through the output terminal (out) when each of the sampling pulses (SAP1, SAP2, ..., SAPm) are at a high level and the charging signal (CH) is at a low level.

[0092] Each of the first and the second holding latches (HOL1_1, HOL1_2, ..., HOLm_1, HOLm_2) may receive a data bit output from the first and the second sampling latches (SAL1_1, SAL1_2, ..., SALm_1, SALm_2) when the first enable signal (EN1) is at a low level and the second enable signal (EN2) is at a high level. Also, each of the first and the second holding latches (HOL1_1, HOL1_2, ..., HOLm_1, HOLm_2) may output a high level voltage or a low level voltage to the DACs, to correspond to the digital data stored in the first and second holding latches (HOL1_1, HOL1_2, ..., HOLm_1, HOLm_2), when the first enable signal (EN1) is at a high level and the second enable signal (EN2) is at a low level.

[0093] The bit and the reversed bit respectively output from the holding latches may be input to each of the corresponding terminals of the DACs provided in every channel. The DACs may select one of a plurality of gray scale voltages to correspond to a bit value of the data supplied from the holding latches. The DACs may respectively generate an analog data signal corresponding to the selected gray scale voltage, so as to respectively supply the analog data signal to the data lines (D 1 to Dm).

[0094] The data driver 20 may be implemented using only PMOS transistors, as described above. The data driver 20 may be mounted in a panel and therefore the manufacturing cost of a display incorporating the same may be reduced.

[0095] FIG. 10 illustrates a basic block diagram of a second exemplary embodiment of a data driver of FIG. 1. The data driver will be described assuming that it includes "m" channels. Referring to FIG. 10, the data driver 20’ may include a shift register unit 100, a conversion unit 200, a sampling latch unit 300, a holding latch unit 400, and a DAC unit 500. The conversion unit 200 is an additional element as compared to the data driver 20 illustrated in FIG. 3. The conversion unit 200 may output a conversion signal (CV). The charging signal (CH) may not be used.

[0096] The shift register unit 100 may receive the start pulse (SP), the first clock signal (CLK1), and the second clock signal (CLK2) to sequentially generate the sampling pulse (SAP). The shift register unit 100 may include "m" shift registers.

[0097] The conversion unit 200 may receive the first clock signal (CLK1), the second clock signal (CLK2), and the sampling pulse (SAP) to sequentially generate a conversion signal (CV). The conversion unit 200 may include "m" conversion circuits.

[0098] The sampling latch unit 300 may receive the sampling pulse (SAP) and the conversion signal (CV). The sampling latch unit 300 may also receive each bit and reversed bit of the input digital data, and then may store the bit and the reversed bit. Accordingly, the sampling latch unit 300 may include twice as many sampling latches as the number of bits of the input digital data. For example, if 6-bit digital data is input, then the sampling latch unit 300 may include 12 (=6x2) sampling latches in every channel. Each sampling latch may store the bit (DATA) or the reversed bit (/DATA).

[0099] The holding latch unit 400 may receive the first enable signal (EN1) and the second enable signal (EN2). The holding latch unit 400 may simultaneously receive each bit and reversed bit output from the sampling latch unit 300. The holding latch unit 400 may output each bit and reversed bit to the DAC unit 500. Accordingly, similar to the sampling latch unit 300, the holding latch unit 400 also may include twice as many holding latches as the number of bits of the digital data input into every channel. For example, if 6-bit digital data is input, then the holding latch unit 400 may include 12 (=6x2) holding latches in every channel.

[0100] The DAC unit 500 may generate an analog signal corresponding to each bit value of the digital data output from the holding latch unit 400. That is, the DAC unit 500 may select one of a plurality of gray scale voltages to correspond to the bit value of the digital data supplied from the holding latch unit 400 and generates an analog data signal. The DAC unit 500 may supply analog data signals to the data lines (D1 to Dm), respectively. The DAC unit 500 may include "m" number of DACs.

[0101] FIG. 11 illustrates a detailed block diagram of a second exemplary embodiment of a data driver of FIG. 10, and FIG. 12 illustrates a timing diagram for driving a data driver of FIG. 11. FIG. 10 will be described assuming that the data driver has "m" number of channels and 6-bit digital data is input. However, it is to be understood that the present invention is not limited thereto. FIG. 12 illustrates a timing diagram in which a most significant bit and a reversed most significant bit of the digital data may be input into every channel.

[0102] As previously discussed above, the conversion unit 200 may be included between the shift register unit and the sampling latch unit, and may output the conversion signal (CV). Thus, the charging signal (CH) may not be used. Accordingly, the second exemplary embodiment may differ from the first embodiment previously described in connection with FIGS. 4 and 5. A specific operation may be the same as the first embodiment, as described above.

[0103] Referring to FIG. 11, the shift register unit 100 and the conversion unit 200 may include one of shift registers (SR1...SRm) and one of conversion circuits (CC1...CCm) per channel, respectively. The sampling latch unit 300 may include 12 sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) per channel and the holding latch unit 400 may include 12 holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) per channel. For clarity, a configuration of the first channel is primarily illustrated in FIG. 11.

[0104] Odd-numbered shift registers (SR1, SR3, ...) of the shift registers (SR1...SRm) may receive the first clock signal (CLK1) through respective first input terminals (clk) and may receive the second clock signal (CLK2) through respective second input terminals (/clk). Even-numbered shift registers (SR2, ..., SRm) of the shift registers (SR1...SRm) may receive the second clock signal (CLK2) through respective first input terminals (clk) and may receive the first clock signal (CLK1) through respective second input terminals (/clk). The first clock signal (CLK1) and the second clock signal (CLK2) may have a phase difference, e.g., about 180°. The first clock signal (CLK1) and the second clock signal (CLK2) may both be at a high level at the same time during a predetermined period, as illustrated in FIG. 12.

[0105] The first shift register (SR1) of the shift registers (SR1...SRm) may receive the first clock signal (CLK1), the second clock signal (CLK2), and the start pulse (SP) to generate the first sampling pulse (SAP1). The second shift register (SR2) may receive the first clock signal (CLK1), the second clock signal (CLK2), and the first sampling pulse (SAP1) to generate the second sampling pulse (SAP2). That is, the shift registers (SR1...SRm) may receive the start pulse (SP) or the sampling pulse (SAP) of a previous stage so as to sequentially generate the sampling pulse (SAP), as illustrated in FIG. 12.

[0106] The odd-numbered conversion circuits (CC1, CC3, ...) of the conversion circuits (CC1...CCm) may receive the first clock signal (CLK1) through the respective first input terminals (clk) and may receive the second clock signal (CLK2) through the respective second input terminals (/clk). The even-numbered conversion circuits (CC2, CC4, ...) may receive the second clock signal (CLK2) through the respective first input terminals (clk) and may receive the first clock signal (CLK1) through the respective second input terminals (/clk).

[0107] The conversion circuits (CC1...CCm) may receive the sampling pulse (SAP), the first clock signal (CLK1), and the second clock signal (CLK2) to generate the conversion signal (CV). For example, a first conversion circuit (CC1) may receive the first sampling pulse (SAP1), the first clock signal (CLK1), and the second clock signal (CLK2) to generate the first conversion signal (CV1). The second conversion circuit (CC2) may receive the second sampling pulse (SAP2), the first clock signal (CLK1), and the second clock signal (CLK2) to generate the second conversion signal (CV2). As illustrated in FIG. 12, the first conversion signal (CV1) and the second conversion signal (CV2) may overlap during a predetermined period.

[0108] The sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) may receive the conversion signal (CV) through the respective first input terminals (clk) and may receive the sampling pulse (SAP) through the respective second input terminals (/clk). The sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12) may also receive a bit or a reversed bit of the digital data and store the bit or the reversed bit of the digital data.

[0109] For example, the sampling latches (SAL1_1...SAL1_12) corresponding to the first channel may receive the first conversion signal (CV1) through the respective first input terminals (clk) and may receive the first sampling pulse (SAP1) through the respective second input terminals (/clk). The sampling latches (SAL1_1...SAL1_12) may receive the bit or the reversed bit of the digital data corresponding to the first channel and store the bit or the reversed bit of the digital data.

[0110] In an implementation, the first sampling latch (SAL1_1) provided in the first channel may receive a most significant bit of the digital data, e.g., bit D[5] (a1 in FIG. 12), and may store the bit D[5] of the digital data when the first sampling pulse (SAP1) and the first conversion signal (CV1) are supplied to the first sampling latch. The second sampling latch (SAL1_2) may receive a reversed most significant bit, e.g., bit /D[5] (/a1 in FIG. 12) of the digital data, and may store the reversed most significant bit /D[5] when the first sampling pulse (SAP1) and the first conversion signal (CV1) are supplied to the second sampling latch (SAL1_2).

[0111] The remaining sampling latches (SAL1_3...SAL1_12) provided in the first channel also may receive a bit or a reversed bit of the digital data, e.g., bits D[4], /D[4], D[3], /D[3], D[2], /D[2], D[1], /D[1], D[0], /D[0], and may store the bit or the reversed bit when the first sampling pulse (SAP1) and the first conversion signal (CV1) are supplied to the remaining sampling latches (SAL1_3...SAL1_12), in the same manner as described above.

[0112] The holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) may receive the second enable signal (EN2) through the respective first input terminals (clk) and may receive the first enable signal (EN1) through the respective second input terminals (/clk). The holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) receiving the first enable signal (EN1) and the second enable signal (EN2) may simultaneously receive each of the bits of the digital data (DATA) stored in the sampling latches (SAL1_1...SAL1_12, ..., SALm_1...SALm_12). The holding latches (HOL1_1...HOL1_12, ..., HOLm_1...HOLm_12) may output each of the bits of the received digital data to the DAC unit 500.

[0113] In an implementation, the holding latches (HOL1_1...HOL1_12) corresponding to the first channel may receive the second enable signal (EN2) through the respective first input terminals (clk) and may receive the first enable signal (EN1) through the respective second input terminals (/clk), and may simultaneously receive each bit or reversed bit of the digital data stored in the sampling latch (SAL1_1...SAL1_12) corresponding to the first channel. The holding latches (HOL1_1...HOL1_12) may output the bit or the reversed bit of the digital data to the DAC of the first channel.

[0114] For example, the first holding latch (HOL1_1) provided in the first channel may receive the bit D[5] stored in the first sampling latch (SAL1_1) and the second holding latch (HOL1_2) may receive the reversed bit /D[5] stored in the second sampling latch (SAL1_2). Similarly, the holding latches (HOL1_3...HOL1_12) provided in the first channel may simultaneously receive each bit or reversed bit D[4], /D[4], D[3], /D[3], D[2], /D[2], D[1], /D[1], D[0], /D[0] stored in the sampling latches (SAL1_3...SAL1_12) and may output the bit or the reversed bit to the DAC of the first channel, in the same manner as described above.

[0115] The bit and the reversed bit of the digital data respectively output from the holding latches may be input to each of the corresponding terminals of the DAC provided in every channel. The DACs may select one of a plurality of gray scale voltages to correspond to the bit value of the digital data supplied from the holding latches. The DACs may respectively generate an analog data signal corresponding to the selected gray scale voltage, so as to respectively supply the analog signal to the data lines (D1...Dm).

[0116] FIG. 13 illustrates a circuit diagram of an exemplary conversion circuit of FIG. 11. Referring to FIG. 13, each of the conversion circuits (CC1...CCm) may include an input unit 202 and an output unit 204. Transistors (M11 through M18) included in the input and output units 202 and 204 may be PMOS-type transistors, i.e., each transistor may be PMOS.

[0117] The output unit 204 may control whether or not a conversion signal (CV) may be output that corresponds to a high level or a low level voltage input from the input unit 202, a state of clock signals (CLK1 or CLK2) input through the first input terminal (clk), and a sampling pulse (SAP) input through the third input terminal (in).

[0118] The output unit 204 may include an eleventh transistor (M11) connected between a third power supply (VDD) and an output terminal (out), a twelfth transistor (M12) and a fourteenth capacitor (C14) connected between the output terminal (out) and the fourth power supply (VSS), a thirteenth transistor (M13) and an eleventh capacitor (C11) connected between a gate electrode and a first electrode of the twelfth transistor (M12), a fourteenth transistor (M14) connected to a gate electrode of the twelfth transistor (M12) and an output terminal of the input unit 202, a fifteenth transistor (M15) connected between a third input terminal (in) and the eleventh transistor (M11), and a twelfth capacitor (C12) connected between a gate electrode and a first electrode of the eleventh transistor (M11).

[0119] The gate electrode of the eleventh transistor (M11) may be connected to a second electrode of the fifteenth transistor (M15) and one terminal of the twelfth capacitor (C12), and the first electrode of the eleventh transistor (M1) may be connected to the third power supply (VDD). The second electrode of the eleventh transistor (M11) may be connected to the output terminal (out). The eleventh transistor (M11) may be turned on or turned off in accordance with a voltage input from the third input terminal (in), or a voltage stored in the twelfth capacitor (C12) when the fifteenth transistor (M15) is turned on.

[0120] The twelfth capacitor (C12) may be connected between the first electrode and the gate electrode of the eleventh transistor (M11). A voltage corresponding to a turned-on or turned-off state of the eleventh transistor (M 11) may be charged in the twelfth capacitor (C12). For example, if the eleventh transistor (M11) is turned on, then a voltage capable of turning on the eleventh transistor (M11) may be charged in the twelfth capacitor (C12), and if the eleventh transistor (M11) is turned off, then a voltage capable of turning off the eleventh transistor (M11) may be charged in the twelfth capacitor (C12)

[0121] The gate electrode of the twelfth transistor (M12) may be connected to a first electrode of the fourteenth transistor (M14), one terminal of the eleventh capacitor (C11), and a second electrode of the thirteenth transistor (M13). The first electrode of the twelfth transistor (M12) may be connected to the output terminal (out), and the second electrode of the twelfth transistor (M12) may be connected to the fourth power supply (VSS). The twelfth transistor (M12) may be turned on or turned off in accordance with a voltage supplied to the gate electrode of the twelfth transistor (M12).

[0122] The eleventh capacitor (C11) may be connected between the first electrode and the gate electrode of the twelfth transistor (M12). A voltage corresponding to a turned-on or turned-off state of the twelfth transistor (M12) may be charged in the eleventh capacitor (C11). For example, if the twelfth transistor (M12) is turned on, then a voltage capable of turning on the twelfth transistor (M12) may be charged in the eleventh capacitor (C11), and if the twelfth transistor (M12) is turned off, then a voltage capable of turning off the twelfth transistor (M12) may be charged in the eleventh capacitor (C11).

[0123] The gate electrode of the thirteenth transistor (M13) may be connected to the gate electrode of the eleventh transistor (M11), and the first electrode of the thirteenth transistor (M13) may be connected to the second electrode of the eleventh transistor (M11). The second electrode of the thirteenth transistor (M13) may be connected to the gate electrode of the twelfth transistor (M12). The thirteenth transistor (M13) may control a voltage supplied to the gate electrode of the twelfth transistor (M12) while being turned on or turned off together with the eleventh transistor (M11).

[0124] The gate electrode of the fourteenth transistor (M14) may be connected to the output terminal of the input unit 202, and the first electrode of the fourteenth transistor (M 14) may be connected to the gate electrode of the twelfth transistor (M12). The second electrode of the fourteenth transistor (M14) may be connected to the fourth power supply (VSS). The fourteenth transistor (M14) may control a voltage supplied to the gate electrode of the twelfth transistor (M12) while being turned on or turned off in accordance to the voltage supplied from the output terminal of the input unit 202.

[0125] The gate electrode of the fifteenth transistor (M15) may be connected to the first input terminal (clk), and the first electrode of the fifteenth transistor (M15) may be connected to the third input terminal (in). The second electrode of the fifteenth transistor (M 15) may be connected to the gate electrode of the eleventh transistor (M11). The fifteenth transistor (M15) may supply a voltage of the third input terminal (in) to the gate electrode of the eleventh transistor (M 11) while being turned on or turned off in accordance with the first clock signal (CLK1) or the second clock signal (CLK2) input through the first input terminal (clk).

[0126] The fourteenth capacitor (C14) may be connected between the output terminal (out) and the fourth power supply (VSS). The fourteenth capacitor (C14) may be employed for stabilizing the voltage of the output terminal (out).

[0127] The input unit 202 may supply a high level or a low level voltage to the output unit 204 that corresponds to a voltage of the first input terminal (clk), a second input terminal (/clk) and the third input terminal (in).

[0128] The input unit 202 may include an eighteenth transistor (M18) connected to the third power supply (VDD) and the third input terminal (in), a sixteenth transistor (M16) connected between the eighteenth transistor (M18) and the output unit 204, and a seventeenth transistor (M17) connected between the eighteenth transistor (M18) and the second input terminal (/clk).

[0129] The first electrode of the sixteenth transistor (M16) may be connected to an input terminal of the output unit 204, and the second electrode of the sixteenth transistor (M16) may be connected to the first input terminal (clk). The gate electrode of the sixteenth transistor (M16) may be connected to a second electrode of the eighteenth transistor (M18) and a first electrode of the seventeenth transistor (M17). The sixteenth transistor (M16) may be turned on or turned off in accordance with the voltage supplied from the third input terminal (in), the second input terminal (/clk), or the thirteenth capacitor (C13).

[0130] The thirteenth capacitor (C13) may be connected between the first electrode and the gate electrode of the sixteenth transistor (M16). A voltage corresponding to a turned-on or turned-off state of the sixteenth transistor (M16) may be charged in such a thirteenth capacitor (C13). For example, if the sixteenth transistor (M16) is turned on, then a voltage capable of turning on the sixteenth transistor (M16) may be charged in the thirteenth capacitor (C13), and if the sixteenth transistor (M16) is turned off, then a voltage capable of turning off the sixteenth transistor (M16) may be charged in the thirteenth capacitor (C13)

[0131] The gate electrode and the second electrode of the seventeenth transistor (M17) may be connected to the second input terminal (/clk), and the first electrode of the seventeenth transistor (M17) may be connected to a second electrode of the eighteenth transistor (M18). The seventeenth transistor (M17) may be connected in a diode form, and then turned on or turned off in accordance with the first clock signal (CLK1) or the second clock signal (CLK2) supplied to the second input terminal (/clk).

[0132] The gate electrode of the eighteenth transistor (M18) may be connected to the third input terminal (in), and the first electrode of the eighteenth transistor (M18) may be connected to the third power supply (VDD). The second electrode of the eighteenth transistor (M 18) may be connected to the gate electrode of the sixteenth transistor (M16). The eighteenth transistor (M18) may be turned on or turned off in accordance with the voltage supplied to the third input terminal (in).

[0133] FIG. 14 illustrates a timing diagram for driving a conversion circuit of FIG. 13. In the following description, it will be assumed that the first clock signal (CLK1) may be supplied to the first input terminal (clk), and the second clock signal (CLK2) may be supplied to the second input terminal (/clk), as illustrated in FIG. 14. Referring to FIGS. 13 and 14, during the first period T(1), a low level voltage may be input through the first input terminal (clk), a high level voltage may be input through the second input terminal (/clk), and a high level voltage may be input through the third input terminal (in).

[0134] If the high level voltage is input through the third input terminal (in) and the second input terminal (/clk), then the seventeenth transistor (M17) and the eighteenth transistor (M18) may be turned off. At this time, the sixteenth transistor (M16) may be turned on by the voltage previously stored in the thirteenth transistor (C13). The low level voltage input through the first input terminal (clk) may be output through the output terminal of the input unit 202 via the sixteenth transistor (M16).

[0135] If the low level voltage is output through the output terminal of the input unit 202, then the fourteenth transistor (M14) may be turned on. Also, the fifteenth transistor (M15) may be turned on in accordance with the low level voltage supplied to the first input terminal (clk). If the fifteenth transistor (M15) is turned on, then the high level voltage supplied to the third input terminal (in) may be supplied to the gate electrodes of the eleventh transistor (M11) and the thirteenth transistor (M13). In this case, the eleventh transistor (M11) and the thirteenth transistor (M13) may be turned off, and a voltage corresponding to a turned-off state may be charged in the twelfth capacitor (C12).

[0136] If the fourteenth transistor (M14) is turned on, then the voltage of the fourth power supply (VSS) may be supplied to the gate electrode of the twelfth transistor (M12). If the voltage of the fourth power supply (VSS) is supplied to the gate electrode of the twelfth transistor (M12), then the twelfth transistor (M12) may be turned on, and a voltage corresponding to a turned-on state may be charged in the eleventh capacitor (C11). Furthermore, if the twelfth transistor (M12) is turned on, then a low level voltage may be output through the output terminal (out) during the first period (T1).

[0137] During the second period (T2), a high level voltage may be input to the first input terminal (clk), a low level voltage may be input to the second input terminal (/clk), and a low level voltage may be input to the third input terminal (in).

[0138] If the low level voltage is input to the second input terminal (/clk), then a seventeenth transistor (M17) may be turned on. If the low level voltage is input to the third input terminal (in), then the eighteenth transistor (M18) may be turned on. In this case, the sixteenth transistor (M16) may be turned on, and the high level voltage input to the first input terminal (clk) may be output through the output terminal of the input unit 202. At this time, a voltage corresponding to a turned-on state of the sixteenth transistor (M16) may be charged in the thirteenth capacitor (C 13).

[0139] If a high level voltage is output through the output terminal of the input unit 202, then a fourteenth transistor (M 14) may be turned off. The fifteenth transistor (M15) may be turned off in accordance with the high level voltage supplied to the first input terminal (clk).

[0140] If the fifteenth transistor (M15) is turned off, then the eleventh transistor (M11) and the thirteenth transistor (M13) may be turned off in accordance with the turned-off voltage stored in the twelfth capacitor (C12). Furthermore, if the fourteenth transistor (M14) is turned off, then the twelfth transistor (M12) may be turned on in accordance with the turned-on voltage stored in the eleventh capacitor (C11), and a low level voltage may be output through the output terminal (out). That is, the previous output state of the first period (T1) may be maintained during the second period (T2).

[0141] During the third period (T3), a low level voltage may be input to the first input terminal (clk), a high level voltage may be input to the second input terminal (/clk), and a low level voltage may be input to the third input terminal (in).

[0142] If a high level of a voltage is input to the second input terminal (/clk), then the seventeenth transistor (M17) may be turned off. If a low level voltage is input to the third input terminal (in), then the eighteenth transistor (M18) may be turned on. The gate voltage of the sixteenth transistor (M16) may be increased to a voltage of the third power supply (VDD). If the gate voltage of the sixteenth transistor (M16) is increased to the voltage of the third power supply (VDD), then a voltage of a first electrode of the sixteenth transistor (M16) may not be reduced below the voltage of the third power supply (VDD), and therefore the fourteenth transistor (M 14) may be turned off.

[0143] The fifteenth transistor (M15) may be turned on in accordance with the low level voltage supplied to the first input terminal (clk). If the fifteenth transistor (M15) is turned on, then the low level voltage input to the third input terminal (in) may be supplied to the gates of the eleventh transistor (M11) and the thirteenth transistor (M13). Accordingly, the eleventh transistor (M11) and the thirteenth transistor (M13) may be turned on. In this case, a voltage corresponding to a turned-on state of the eleventh transistor (M11) may be charged in the twelfth capacitor (C12).

[0144] If the eleventh transistor (M11) is turned on, then a voltage of the third power supply (VDD) may be supplied to the output terminal (out). That is, a high level voltage may be output to the output terminal (out). If the thirteenth transistor (M13) is turned on, then the third power supply (VDD) may be supplied to the gate electrode of the twelfth transistor (M12), and therefore the twelfth transistor (M12) may be turned off. In this case, a voltage corresponding to a turned-off state may be stored in the eleventh capacitor (C11).

[0145] During the fourth period (T4), a high level voltage may be input to the first input terminal (clk), a low level voltage may be input to the second input terminal (/clk), and a high level voltage may be input to the third input terminal (in).

[0146] If the low level voltage is input to the second input terminal (/clk), then a seventeenth transistor (M17) may be turned on. If the high level voltage is input to the third input terminal (in), then the eighteenth transistor (M18) may be turned off. The low level voltage input to the second input terminal (/clk) may be supplied to the sixteenth transistor (M16), and therefore the sixteenth transistor (M16) may be turned on. If the sixteenth transistor (M16) is turned on, then the high level voltage supplied to the first input terminal (clk) may be supplied to the fourteenth transistor (M14), and therefore the fourteenth transistor (M 14) may be turned off.

[0147] The fifteenth transistor (M15) may be turned off in accordance with the high level voltage supplied to the first input terminal (clk). If the fifteenth transistor (M15) is turned off, then the eleventh transistor (M11) and the thirteenth transistor (M13) may be turned on by the voltage stored in the twelfth capacitor (C12). If the fourteenth transistor (M14) is turned off, then the twelfth transistor (M12) is turned off in accordance with the voltage stored in the eleventh capacitor (C11). That is, the same high level voltage output during the third period (T3) may be output during the fourth period (T4).

[0148] As discussed above, the conversion circuit (CC) may output a voltage level opposite to a voltage supplied to the third input terminal (in) if a low level voltage is input to the first input terminal (clk), and may maintain its output of the previous period if a high level voltage is input to the first input terminal (clk).

[0149] As described above, a data driver and an organic light emitting display using the same according to embodiments of the present invention may enable the data driver to be mounted in a panel. In particular, the shift registers, the sampling latches, the holding latches and the DAC included in the data driver may be implemented with only PMOS transistors. Accordingly, the data driver may be mounted in the panel and may be manufactured at a reduced cost.

[0150] Exemplary embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A data driver (20) for an organic light emitting display receiving digital data (DATA) and supplying a data signal to data lines (D1... Dm), comprising:

a shift register unit (100) configured to receive a first clock signal (CLK1), a second clock signal (CLK2), and a start pulse (SP), and configured to generate a sampling pulse (SAP1, SAP2, SAP3, SAPm);
a sampling latch unit (300) configured to receive and output bits and reversed bits of digital data (DATA), in correspondence with the sampling pulse (SAP1, SAP2, SAP3, SAPm);
a holding latch unit (400) configured to receive the bits and reversed bits output by the sampling latch unit (300), and configured to output the bits and reversed bits, in correspondence with a first enable signal (EN1) and a second enable signal (EN2); and
a digital-to-analog converter (500) configured to receive the bits and reversed bits output by the holding latch unit (400) and configured to generate an analog signal corresponding to values of the received bits and reversed bits
wherein the shift register unit (100) includes at least one shift register, the sampling latch unit includes (300) at least one sampling latch, and the holding latch unit (400) includes at least one holding latch, and the shift register, the sampling latch, and the holding latch each include:

a first transistor (M1) having a gate electrode connected to a second input terminal (Iclk) for an inverted clock signal, a second electrode connected to a first node (N_1), and a first electrode connected to an external input terminal (SP, DATA) for the digital signal;
a second transistor (M2) having a gate electrode connected to the first node (N1), a first electrode connected to a first input terminal (Clk) for a clock signal, and a second electrode connected to an output terminal (OUT);
a third transistor (M3) having a gate electrode connected to the second input terminal (Clk), a first electrode connected to a second node (N2), and a second electrode connected to a fourth power supply (VDD);
a fourth transistor (M4) having a gate electrode connected to the first node (N1), a first electrode connected to the second input terminal (Clk), and a second electrode connected to the second node (N2);
a fifth transistor having a gate electrode connected to the second node (N2), a first electrode connected to a third power supply (VDD), and a second electrode connected to the output terminal (OUT); and
a capacitor (C1) connected between the gate electrode and the second electrode of the second transistor,
wherein the first through fifth transistors are all PMOS transistors.

2. The data driver as claimed in claim 1, wherein the shift register unit (100) includes one shift register per data line (D1...Dm).

3. The data driver according to one of the preceding claims, wherein the sampling latch unit (300) includes a predetermined number of sampling latches per date line (D1 ... Dm), the predetermined number being twice a number of bits of input digital data.

4. The data driver according to one of the preceding claims, wherein the holding latch unit (400) includes the predetermined number of holding latches per data line (D1 ... Dm).

5. The data driver according to one of the preceding claims, wherein the digital-to-analog converter (500) includes a plurality of transistors configured to receive the bits and reversed bits output by the holding latch unit (400), and
the transistors being adapted to receive the bits and reversed bits are PMOS transistors.

6. The data driver according to one of the preceding claims, wherein a latch signal is input at a high level to the sampling latch unit (300) when the bits and reversed bits are input to the sampling latch unit (300).

7. The data driver according to one of the preceding claims, wherein the first clock signal (CLK1) and the second clock signal (CLK2) have a phase difference of 180 degrees.

8. The data driver as claimed in claim 7, wherein the first clock signal (CLK1) and the second clock signal (CLK2) are both at a high level during a predetermined period.

9. The data driver as claimed in claim 1, wherein the third power supply (VDD) is adapted to provide a higher voltage than that provided by the fourth power supply (VSS).

10. The data driver according to one of the claims 1 and 9, wherein the shift register unit (100) includes even and odd-numbered shift registers,
the first clock signal (CLK1) is supplied to the first input terminals of the odd-numbered shift registers, and
the second clock signal (CLK2) is supplied to the second input terminals of the odd-numbered shift registers.

11. The data driver as claimed in claim 10, wherein the second clock signal (CLK2) is supplied to the first input terminals of the even-numbered shift registers, and
the first clock signal (CLK1) is supplied to the second input terminals of the even-numbered shift registers.

12. The data driver according to one of the claims 1 and 9, wherein, in the shift register (100):

when a low level signal is supplied to the second input terminal, the capacitor (C1) is charged with a voltage that corresponds to the voltage supplied from the external input terminal, and
when a high level signal is supplied to the second input terminal, a voltage is supplied to the output terminal that corresponds to the voltage charged in the capacitor (C1).

13. The data driver according to one of the claims 1 and 9, wherein, in the sampling latch (300):

the sampling pulse is supplied to the second input terminal, and
a latch signal is supplied to the first input terminal.

14. The data driver as claimed in claim 13, wherein the sampling latch (300) receives each bit or reversed bit when the sampling pulse is at a low level and the latch signal is at a high level, and
the sampling latch (300) outputs each bit or reversed bit when the sampling pulse is at a high level and the latch signal is at a low level.

15. The data driver according to one of the claims 1 and 9, wherein, in the holding latch (400):

the first enable signal (EN1) is provided to the second input terminal, and
the second enable signal (EN2) is provided to the first input terminal.

16. The data driver as claimed in claim 15, wherein the first enable signal (EN1) and the second enable signal (EN2) have a phase difference of 180 degrees.

17. The data driver as claimed in claim 15, wherein the holding latch (400) receives a signal from the sampling latch (300) when the first enable signal (EN1) is at a low level, and
the received signal is output by the holding latch (400) when the first enable signal (EN1) is at a high level.

18. The data driver as claimed in claim 15, wherein the first enable signal (EN1) is maintained at a high level during output by the sampling latch (300), and
the first enable signal (EN1) changes to a low level after output by the sampling latch (300).

19. The data driver according to one of the preceding

claims, further comprising a conversion unit (200) configured to receive the first clock signal (CLK1), the second clock signal (CLK2) and the sampling pulse, and to sequentially generate a conversion signal,
wherein the conversion signal is supplied to the sampling latch unit (300);
wherein the conversion unit (200) has one conversion circuit per data line (D1... Dm);
wherein the conversion circuit includes an input unit and an output unit,
the input unit is configured to receive the sampling pulse at an input terminal thereof and to control a signal that is supplied to the output unit; and
the output unit is configured to control whether or not the conversion signal is output, in correspondence with the signal controlled by the input unit and the sampling pulse input to the input terminal;
wherein the output unit includes:

an eleventh transistor having a first electrode connected to a third power supply (VDD) and having a second electrode connected to an output terminal;
a twelfth transistor having a first electrode connected to the output terminal and having a second electrode connected to a fourth power supply (VSS), the fourth power supply (VSS) providing a lower voltage than that provided by the third power supply (VDD);
a thirteenth transistor having a gate electrode connected to a gate electrode of the eleventh transistor and having a first electrode connected to the second electrode of the eleventh transistor;
a fourteenth transistor having a first electrode connected to a second electrode of the thirteenth transistor, having a second electrode connected to the fourth power supply, and having a gate electrode connected to the input unit;
a fifteenth transistor having a first electrode connected to a third input terminal, having a second electrode connected to the gate electrode of the eleventh transistor, and having a gate electrode connected to a first input terminal;
a twelfth capacitor connected between the gate electrode and the first electrode of the eleventh transistor; and
an eleventh capacitor connected between a gate electrode of the twelfth transistor and the first electrode of the twelfth transistor;
wherein the data driver (20) further comprises a fourteenth capacitor connected between the output terminal and the fourth power supply; and
wherein the input unit includes:

a sixteenth transistor having a first electrode connected to the gate electrode of the fourteenth transistor and having a second electrode connected to the first input terminal;
a seventeenth transistor having a first electrode connected to a gate electrode of the sixteenth transistor, and having a gate electrode and a second electrode both connected to a second input terminal;
an eighteenth transistor having a gate electrode connected to the third input terminal, having a first electrode connected to the third power supply, and having a second electrode connected to the gate electrode of the sixteenth transistor; and
a thirteenth capacitor connected between the gate electrode of the sixteenth transistor and the first electrode of the sixteenth transistor, wherein the eleventh through eighteenth transistors are PMOS transistors.

20. The data driver as claimed in claim 19, wherein the conversion unit (200) includes even numbered and odd-numbered conversion circuits, and
the odd-numbered conversion circuits receive the first clock signal (CLK1) at the first input terminal, and receive the second clock signal (CLK2) at the second input terminal.

21. The data driver as claimed in claim 20, wherein the even-numbered conversion circuits receive the second clock signal (CLK2) at the first input terminal, and receive the first clock signal (CLK1) at the second input terminal.

22. The data driver as claimed in claim 19, wherein the conversion circuit (200) outputs a signal level opposite to a signal input to the third input terminal if a low level signal is input to the first input terminal, and the conversion circuit (200) maintains an output of a previous period if a high level signal is input to the first input terminal.

23. An organic light emitting display, comprising:

a scan driver (10) configured to sequentially supply a scan signal to scan lines;
a data driver (20) according to one of the claims 1-22 configured to supply a data signal to data lines; and
a pixel unit including a plurality of organic light emitting pixels connected to the scan lines and the data lines.

Patentansprüche

1. Datentreiber (20) für eine organische lichtemittierende Anzeige, der digitale Daten (DATA) erhält und ein Datensignal an Datenleitungen (D1...Dm) anlegt, aufweisend:

eine Schieberegistereinheit (100), die konfiguriert ist, um ein erstes Taktsignal (CLK1), ein zweites Taktsignal (CLK2) und einen Startimpuls (SP) zu erhalten, und konfiguriert ist, um einen Abtastimpuls (SAP1, SAP2, SAP3, SAPm) zu erzeugen;
eine Abtastspeichereinheit (300), die konfiguriert ist, um Bits und umgekehrte Bits der digitalen Daten (DATA) entsprechend dem Abtastimpuls (SAP1, SAP2, SAP3, SAPm) zu erhalten und auszugeben;
eine Haltespeichereinheit (300), die konfiguriert ist, um die Bits und die umgekehrten Bits, die von der Abtastspeichereinheit (300) ausgegeben werden, zu erhalten, und konfiguriert ist, um die Bits und die umgekehrten Bits entsprechend einem ersten Freigabesignal (EN1) und einem zweiten Freigabesignal (EN2) auszugeben; und
einen Digital-Analog-Wandler (500), der konfiguriert ist, um die Bits und die umgekehrten Bits, die von der Haltespeichereinheit (400) ausgegeben werden, zu erhalten, und konfiguriert ist, um ein analoges Signal entsprechend Werten der erhaltenen Bits und umgekehrten Bits zu erzeugen,
wobei die Schieberegistereinheit (100) zumindest ein Schieberegister aufweist, die Abtastspeichereinheit (300) zumindest einen Abtastspeicher aufweist und die Haltespeichereinheit (400) zumindest einen Haltespeicher aufweist, und wobei das Schieberegister, der Abtastspeicher und der Haltespeicher jeweils aufweisen:

einen ersten Transistor (M1), der eine Gate-Elektrode, die mit einem zweiten Eingangsanschluss (/clk) für ein umgekehrtes Taktsignal verbunden ist, eine zweite Elektrode, die mit einem ersten Knoten (N1) verbunden ist, und eine erste Elektrode, die mit einem externen Eingangsanschluss (SP, DATA) für das digitale Signal verbunden ist, aufweist;
einen zweiten Transistor (M2), der eine Gate-Elektrode, die mit dem ersten Knoten (N1) verbunden ist, eine erste Elektrode, die mit einem ersten Eingangsanschluss (clk) für ein Taktsignal verbunden ist, und eine zweite Elektrode, die mit einem Ausgangsanschluss (out) verbunden ist, aufweist;
einen dritten Transistor (M3), der eine Gate-Elektrode, die mit dem zweiten Eingangsanschluss (/clk) verbunden ist, eine erste Elektrode, die mit einem zweiten Knoten (N2) verbunden ist, und eine zweite Elektrode, die mit einer vierten Energieversorgung (VDD) verbunden ist, aufweist;
einen vierten Transistor (M4), der eine Gate-Elektrode, die mit dem ersten Knoten (N1) verbunden ist, eine erste Elektrode, die mit dem zweiten Eingangsanschluss (clk) verbunden ist, und eine zweite Elektrode, die mit dem zweiten Knoten (N2) verbunden ist, aufweist;
einen fünften Transistor, der eine Gate-Elektrode, die mit dem zweiten Knoten (N2) verbunden ist, eine erste Elektrode, die mit einer dritten Energieversorgung (VDD) verbunden ist, und eine zweite Elektrode, die mit dem Ausgangsanschluss (out) verbunden ist, aufweist; und
einen Kondensator (C1), der zwischen die Gate-Elektrode und die zweite Elektrode des zweiten Transistors geschaltet ist,
wobei der erste bis fünfte Transistor jeweils PMOS-Transistoren sind.

2. Datentreiber nach Anspruch 1, wobei die Schieberegistereinheit (100) ein Schieberegister je Datenleitung (D1...Dm) aufweist.

3. Datentreiber nach einem der vorhergehenden Ansprüche, wobei die Abtastspeichereinheit (300) eine vorbestimmte Anzahl von Abtastspeichern je Datenleitung (D1...Dm) aufweist, wobei die vorbestimmte Anzahl zweimal eine Anzahl von Bits der eingegebenen digitalen Daten ist.

4. Datentreiber nach einem der vorhergehenden Ansprüche, wobei die Haltespeichereinheit (400) die vorbestimmte Anzahl von Haltespeichem je Datenleitung (D1...Dm) aufweist.

5. Datentreiber nach einem der vorhergehenden Ansprüche, wobei der Digital-Analog-Umsetzer (500) eine Vielzahl von Transistoren aufweist, die konfiguriert sind, um die Bits und die umgekehrten Bits, die von der Haltespeichereinheit (400) ausgegeben werden, zu erhalten, und
die Transistoren, die angepasst sind, um die Bits und die umgekehrten Bits zu erhalten, PMOS-Transistoren sind.

6. Datentreiber nach einem der vorhergehenden Ansprüche, wobei ein Speichersignal auf einem hohen Pegel in die Abtastspeichereinheit (300) eingegeben wird, wenn die Bits und die umgekehrten Bits in die Abtastspeichereinheit (300) eingegeben werden.

7. Datentreiber nach einem der vorhergehenden Ansprüche, wobei das erste Taktsignal (CLK1) und das zweite Taktsignal (CLK2) eine Phasendifferenz von 180 Grad aufweisen.

8. Datentreiber nach Anspruch 7, wobei das erste Taktsignal (CLK1) und das zweite Taktsignal (CLK2) während einer vorbestimmten Periode beide auf einem hohen Pegel sind.

9. Datentreiber nach Anspruch 1, wobei die dritte Energieversorgung (VDD) angepasst ist, um eine höhere Spannung als die von der vierten Energieversorgung (VSS) bereitgestellte Spannung bereitzustellen.

10. Datentreiber nach einem der Ansprüche 1 und 9, wobei die Schieberegistereinheit (100) geradzahlige und ungeradzahlige Schieberegister aufweist,
das erste Taktsignal (CLK1) den ersten Eingangsanschlüssen der ungeradzahligen Schieberegister zugeführt wird, und
das zweite Taktsignal (CLK2) den zweiten Eingangsanschlüssen der ungeradzahligen Schieberegister zugeführt wird.

11. Datentreiber nach Anspruch 10, wobei das zweite Taktsignal (CLK2) den ersten Eingangsanschlüssen der geradzahligen Schieberegister zugeführt wird, und
das erste Taktsignal (CLK1) den zweiten Eingangsanschlüssen der geradzahligen Schieberegister zugeführt wird.

12. Datentreiber nach einem der Ansprüche 1 und 9, wobei im Schieberegister (100):

> wenn ein Niedrigpegelsignal dem zweiten Eingangsanschluss zugeführt wird, der Kondensator (C1) mit einer Spannung, die der vom externen Eingangsanschluss gelieferten Spannung entspricht, geladen wird, und,
> wenn ein Hochpegelsignal dem zweiten Eingangsanschluss zugeführt wird, der Ausgangsanschluss mit einer Spannung, die der im Kondensator (C1) geladenen Spannung entspricht, versorgt wird.

13. Datentreiber nach einem der Ansprüche 1 und 9, wobei im Abtastspeicher (300):

> der Abtastimpuls dem zweiten Eingangsanschluss zugeführt wird, und
> ein Speichersignal dem ersten Eingangsanschluss zugeführt wird.

14. Datentreiber nach Anspruch 13, wobei der Abtastspeicher (300) jedes Bit oder umgekehrte Bit erhält, wenn der Abtastimpuls auf einem niedrigen Pegel ist und das Abtastsignal auf einem hohen Pegel ist, und
der Abtastspeicher (300) jedes Bit oder umgekehrte Bit ausgibt, wenn der Abtastimpuls auf einem hohen Pegel ist und das Speichersignal auf einem niedrigen Pegel ist.

15. Datentreiber nach einem der Ansprüche 1 und 9, wobei im Haltespeicher (400):

> das erste Freigabesignal (EN1) zum ersten Eingangsanschluss geliefert wird, und
> das zweite Freigabesignal (EN2) zum ersten Eingangsanschluss geliefert wird.

16. Datentreiber nach Anspruch 15, wobei das erste Freigabesignal (EN) und das zweite Freigabesignal (EN2) eine Phasendifferenz von 180 Grad aufweisen.

17. Datentreiber nach Anspruch 15, wobei der Haltespeicher (400) ein Signal vom Abtastspeicher (300) erhält, wenn das erste Freigabesignal (EN1) auf einem niedrigen Pegel ist, und
das erhaltene Signal vom Haltespeicher (400) ausgegeben wird, wenn das erste Freigabesignal (EN1) auf einem hohen Pegel ist.

18. Datentreiber nach Anspruch 15, wobei das erste Freigabesignal (EN1) während der Ausgabe durch den Abtastspeicher (300) auf einem hohen Pegel aufrechterhalten wird, und
das erste Freigabesignal (EN1) sich nach der Ausgabe durch den Abtastspeicher (300) auf einen niedrigen Pegel ändert.

19. Datentreiber nach einem der vorhergehenden Ansprüche, weiterhin aufweisend eine Umwandlungseinheit (200), die konfiguriert ist, um das erste Taktsignal (CLK1), das zweite Taktsignal (CLK2) und den Abtastimpuls zu erhalten und um sequenziell ein Umwandlungssignal zu erzeugen,
wobei das Umwandlungssignal an die Abtastspeichereinheit (300) angelegt wird;
wobei die Umwandlungseinheit (200) eine Umwandlungsschaltung je Datenleitung (D1...Dm) aufweist;
wobei die Umwandlungsschaltung eine Eingabeeinheit und eine Ausgabeeinheit aufweist,
die Eingabeeinheit konfiguriert ist, um den Abtastimpuls bei einem Eingangsanschluss davon zu erhalten und ein Signal, das der Ausgabeeinheit zugeführt wird, zu steuern; und
die Ausgabeeinheit konfiguriert ist, um zu steuern, ob das Umwandlungssignal entsprechend dem von der Eingabeeinheit gesteuerten Signal und dem in den Eingangsanschluss eingegebenen Abtastimpuls ausgegeben wird;
wobei die Ausgabeeinheit aufweist:

> einen elften Transistor, der eine erste Elektrode, die mit einer dritten Energieversorgung (VDD) verbunden ist, aufweist, und eine zweite Elektrode, die mit einem Ausgangsanschluss ver-

bunden ist, aufweist;
einen zwölften Transistor, der eine erste Elektrode, die mit dem Ausgangsanschluss verbunden ist, aufweist, und eine zweite Elektrode, die mit einer vierten Energieversorgung (VSS) verbunden ist, aufweist, wobei die vierte Energieversorgung (VSS) eine niedrigere Spannung als die von der dritten Energieversorgung (VDD) bereitgestellte Spannung bereitstellt;
einen dreizehnten Transistor, der eine Gate-Elektrode, die mit einer Gate-Elektrode des elften Transistors verbunden ist, aufweist und eine erste Elektrode, die mit der zweiten Elektrode des elften Transistors verbunden ist, aufweist;
einen vierzehnten Transistor, der eine erste Elektrode, die mit einer zweiten Elektrode des dreizehnten Transistors verbunden ist, aufweist, eine zweite Elektrode, die mit der vierten Energieversorgung verbunden ist, aufweist und eine Gate-Elektrode, die mit der Eingabeeinheit verbunden ist, aufweist;
einen fünfzehnten Transistor, der eine erste Elektrode, die mit einem dritten Eingangsanschluss verbunden ist, aufweist, eine zweite Elektrode, die mit der Gate-Elektrode des elften Transistors verbunden ist, aufweist und eine Gate-Elektrode, die mit einem ersten Eingangsanschluss verbunden ist, aufweist;
einen zwölften Kondensator, der zwischen die Gate-Elektrode und die erste Elektrode des elften Transistors geschaltet ist; und
einen elften Kondensator, der zwischen eine Gate-Elektrode des zwölften Transistors und die erste Elektrode des zwölften Transistors geschaltet ist;
wobei der Datentreiber (20) weiterhin einen vierzehnten Kondensator, der zwischen den Ausgangsanschluss und die vierte Energieversorgung geschaltet ist, aufweist; und
wobei die Eingabeeinheit aufweist:

> einen sechzehnten Transistor, der eine erste Elektrode, die mit der Gate-Elektrode des vierzehnten Transistors verbunden ist, aufweist und eine zweite Elektrode, die mit dem ersten Eingangsanschluss verbunden ist, aufweist;
> einen siebzehnten Transistor, der eine erste Elektrode, die mit einer Gate-Elektrode des sechzehnten Transistors verbunden ist, aufweist und eine Gate-Elektrode und eine zweite Elektrode, die beide mit einem zweiten Eingangsanschluss verbunden sind, aufweist;
> einen achtzehnten Transistor, der eine Gate-Elektrode, die mit dem dritten Eingangsanschluss verbunden ist, aufweist, eine erste Elektrode, die mit der dritten Energieversorgung verbunden ist, aufweist und eine zweite Elektrode, die mit der Gate-Elektrode des sechzehnten Transistors verbunden ist, aufweist; und
> einen dreizehnten Kondensator, der zwischen die Gate-Elektrode des sechzehnten Transistors und die erste Elektrode des sechzehnten Transistors geschaltet ist, wobei der elfte bis achtzehnte Transistor PMOS-Transistoren sind.

20. Datentreiber nach Anspruch 19, wobei die Umwandlungseinheit (200) geradzahlige und ungeradzahlige Umwandlungsschaltungen aufweist, und
die ungeradzahligen Umwandlungsschaltungen das erste Taktsignal (CLK1) am ersten Eingangsanschluss erhalten und das zweite Taktsignal (CLK2) am zweiten Eingangsanschluss erhalten.

21. Datentreiber nach Anspruch 20, wobei die geradzahligen Umwandlungsschaltungen das zweite Taktsignal (CLK2) am ersten Eingangsanschluss erhalten und das erste Taktsignal (CLK1) am zweiten Eingangsanschluss erhalten.

22. Datentreiber nach Anspruch 19, wobei die Umwandlungsschaltung (200) einen Signalpegel ausgibt, der einem Signal, das in den dritten Eingangsanschluss eingegeben wird, entgegengesetzt ist, wenn ein Niedrigpegelsignal in den ersten Eingangsanschluss eingegeben wird, und
die Umwandlungsschaltung (200) eine Ausgabe einer vorhergehenden Periode aufrechterhält, wenn ein Hochpegelsignal in den ersten Eingangsanschluss eingegeben wird.

23. Organische lichtemittierende Anzeige, aufweisend:

> einen Ansteuerungstreiber (10), der konfiguriert ist, um ein Ansteuersignal sequenziell an Ansteuerleitungen anzulegen;
> einen Datentreiber (20) nach einem der Ansprüche 1-22, der konfiguriert ist, um ein Datensignal an Datenleitungen anzulegen; und
> eine Pixeleinheit, die eine Vielzahl organischer lichtemittierender Pixel, die mit den Ansteuerleitungen und den Datenleitungen verbunden sind, aufweist.

Revendications

1. Circuit d'attaque de données (20) destiné à un affichage électroluminescent organique recevant des données numériques (DATA) et fournissant un signal de données à des lignes de données (D1...Dm), comprenant :

une unité à registres à décalage (100) configurée pour recevoir un premier signal d'horloge (CLK1), un deuxième signal d'horloge (CLK2), et une impulsion de départ (SP), et configurée pour générer une impulsion d'échantillonnage (SAP1, SAP2, SAP3, SAPm) ;
une unité à registres à verrouillage d'échantillonnage (300) configurée pour recevoir et fournir en sortie des bits et des bits inversés de données numériques (DATA), en correspondance avec l'impulsion d'échantillonnage (SAP1, SAP2, SAP3, SAPm) ;
une unité à registres à verrouillage de maintien (400) configurée pour recevoir les bits et les bits inversés fournis en sortie par l'unité à registres à verrouillage d'échantillonnage (300), et configurée pour délivrer en sortie les bits et les bits inversés, en correspondance avec un premier signal de validation (EN1) et un deuxième signal de validation (EN2) ; et
un convertisseur numérique-analogique (500) configuré pour recevoir les bits et les bits inversés fournis en sortie par l'unité à registres à verrouillage de maintien (400) et configuré pour générer un signal analogique correspondant à des valeurs des bits et des bits inversés reçus,
dans lequel l'unité à registres à décalage (100) comprend au moins un registre à décalage, l'unité à registres à verrouillage d'échantillonnage comprend (300) au moins un registre à verrouillage d'échantillonnage, et l'unité à registres à verrouillage de maintien (400) comprend au moins un registre à verrouillage de maintien, et le registre à décalage, le registre à verrouillage d'échantillonnage, et le registre à verrouillage de maintien comprennent chacun .
un premier transistor (M1) ayant une électrode/clk de grille connectée à une deuxième borne d'entrée (clk) pour un signal d'horloge inversé, une deuxième électrode connectée à un premier noeud (N1), et une première électrode connectée à une borne d'entrée externe (SP, DATA) pour le signal numérique ;
un deuxième transistor (M2) ayant une électrode de grille connectée au premier noeud (N1), une première électrode connectée à une première borne d'entrée (clk) pour un signal d'horloge, et une deuxième électrode connectée à une borne de sortie (out) ;
un troisième transistor (M3) ayant une électrode/clk de grille connectée à la deuxième borne d'entrée (CLK), une première électrode connectée à un deuxième noeud (N2), et une deuxième électrode connectée à une quatrième alimentation électrique (VDD) ;
un quatrième transistor (M4) ayant une électrode/clk de grille connectée au premier noeud (N1), une première électrode connectée à la deuxième borne d'entrée (clk), et une deuxième électrode connectée au deuxième noeud (N2) ;
un cinquième transistor ayant une électrode de grille connectée au deuxième noeud (N2), une première électrode connectée à une troisième alimentation électrique (VDD), et une deuxième électrode connectée à la borne de sortie (out) ; et
un condensateur (C1) connecté entre l'électrode de grille et la deuxième électrode du deuxième transistor,
dans lequel les premier à cinquième transistors sont tous des transistors PMOS.

2. Circuit d'attaque de données selon la revendication 1, dans lequel l'unité à registres à décalage (100) comprend un registre à décalage par ligne de données (D1...Dm).

3. Circuit d'attaque de données selon l'une quelconque des revendications précédentes, dans lequel l'unité à registres à verrouillage d'échantillonnage (300) comprend un nombre prédéterminé de registres à verrouillage d'échantillonnage par ligne de données (D1...Dm), le nombre prédéterminé étant deux fois supérieur à un nombre de bits de données numériques d'entrée.

4. Circuit d'attaque de données selon l'une des revendications précédentes, dans lequel l'unité à registres à verrouillage de maintien (400) comprend le nombre prédéterminé de registres à verrouillage de maintien par ligne de données (D1...Dm).

5. Circuit d'attaque de données selon l'une quelconque des revendications précédentes, dans lequel le convertisseur numérique-analogique (500) comprend une pluralité de transistors configurés pour recevoir les bits et les bits inversés fournis en sortie par l'unité à registres à verrouillage de maintien (400), et
les transistors aptes à recevoir les bits et les bits inversés sont des transistors PMOS.

6. Circuit d'attaque de données selon l'une des revendications précédentes, dans lequel un signal de verrouillage est fourni en entrée à un niveau haut à l'unité à registres à verrouillage d'échantillonnage (300) lorsque les bits et les bits inversés sont fournis en entrée à l'unité à registres à verrouillage d'échantillonnage (300).

7. Circuit d'attaque de données selon l'une quelconque des revendications précédentes, dans lequel le premier signal d'horloge (CLK1) et le deuxième signal d'horloge (CLK2) présentent une différence de phase de 180 degrés.

8. Circuit d'attaque de données selon la revendication

7, dans lequel le premier signal d'horloge (CLK1) et le deuxième signal d'horloge (CLK2) sont tous deux à un niveau haut pendant une période prédéterminée.

9. Circuit d'attaque de données selon la revendication 1, dans lequel la troisième alimentation électrique (VDD) est apte à fournir une tension plus élevée que celle fournie par la quatrième alimentation électrique (VSS).

10. Circuit d'attaque de données selon l'une des revendications 1 et 9, dans lequel l'unité à registres à décalage (100) comprend des registres à décalage de numéros pair et impair,
le premier signal d'horloge (CLK1) est fourni aux premières bornes d'entrée des registres à décalage de numéro impair, et
le deuxième signal d'horloge (CLK2) est fourni aux deuxièmes bornes d'entrée des registres à décalage de numéro impair.

11. Circuit d'attaque de données selon la revendication 10, dans lequel le deuxième signal d'horloge (CLK2) est fourni aux premières bornes d'entrée des registres à décalage de numéro pair, et le premier signal d'horloge (CLK1) est fourni aux deuxième bornes d'entrée des registres à décalage de numéro pair.

12. Circuit d'attaque de données selon l'une des revendications 1 et 9, dans lequel, dans le registre à décalage (100) :

> lorsqu'un signal au niveau bas est fourni à la deuxième borne d'entrée, le condensateur (C1) est chargé avec une tension qui correspond à la tension fournie par la borne d'entrée externe, et
> lorsqu'un signal au niveau haut est fourni à la deuxième borne d'entrée, une tension est fournie à la borne de sortie qui correspond à la tension chargée dans le condensateur (C1).

13. Circuit d'attaque de données selon l'une des revendications 1 et 9, dans lequel, dans le registre à verrouillage d'échantillonnage (300) :

> l'impulsion d'échantillonnage est fournie à la deuxième borne d'entrée, et un signal de verrouillage est fourni à la première borne d'entrée.

14. Circuit d'attaque de données selon la revendication 13, dans lequel le registre à verrouillage d'échantillonnage (300) reçoit chaque bit ou bit inversé lorsque l'impulsion d'échantillonnage est à un niveau bas et le signal de verrouillage est à un niveau haut, et
le registre à verrouillage d'échantillonnage (300) fournit en sortie chaque bit ou bit inversé lorsque l'impulsion d'échantillonnage est à un niveau haut et le signal de verrouillage est à un niveau bas.

15. Circuit d'attaque de données selon l'une des revendications 1 et 9, dans lequel, dans le registre à verrouillage de maintien (400) :

> le premier signal de validation (EN1) est fourni à la deuxième borne d'entrée, et
> le deuxième signal de validation (EN2) est fourni à la première borne d'entrée.

16. Circuit d'attaque de données selon la revendication 15, dans lequel le premier signal de validation (EN1) et le deuxième signal de validation (EN2) présentent une différence de phase de 180 degrés.

17. Circuit d'attaque de données selon la revendication 15, dans lequel le registre à verrouillage de maintien (400) reçoit un signal du registre à verrouillage d'échantillonnage (300) lorsque le premier signal de validation (EN1) est à un niveau bas, et
le signal reçu est fourni en sortie par le registre à verrouillage de maintien (400) lorsque le premier signal de validation (EN1) est à un niveau haut.

18. Circuit d'attaque de données selon la revendication 15, dans lequel le premier signal de validation (EN1) est maintenu à un niveau haut pendant sa fourniture en sortie par le registre à verrouillage d'échantillonnage (300), et
le premier signal de validation (EN1) passe à un niveau bas après sa fourniture en sortie par le registre à verrouillage d'échantillonnage (300).

19. Circuit d'attaque de données selon l'une des revendications précédentes, comprenant en outre une unité de conversion (200) configurée pour recevoir le premier signal d'horloge (CLK1), le deuxième signal d'horloge (CLK2) et l'impulsion d'échantillonnage, et pour générer séquentiellement un signal de conversion,
dans lequel le signal de conversion est fourni à l'unité à registres à verrouillage d'échantillonnage (300) ;
dans lequel l'unité de conversion (200) comporte un circuit de conversion par ligne de données (D1...Dm) ;
dans lequel le circuit de conversion comprend une unité d'entrée et une unité de sortie, l'unité d'entrée est configurée pour recevoir l'impulsion d'échantillonnage sur une borne d'entrée de celle-ci et pour commander un signal qui est fourni à l'unité de sortie ; et
l'unité de sortie est configurée pour contrôler si oui ou non le signal de conversion est fourni en sortie, en correspondance avec le signal contrôlé par l'unité d'entrée et l'impulsion d'échantillonnage fournie en

entrée à la borne d'entrée ;
dans lequel l'unité de sortie comprend .
un onzième transistor ayant une première électrode connectée à une troisième alimentation électrique (VDD) et ayant une deuxième électrode connectée à une borne de sortie ;
un douzième transistor ayant une première électrode connectée à la borne de sortie et ayant une deuxième électrode connectée à une quatrième alimentation électrique (VSS), la quatrième alimentation électrique (VSS) fournissant une tension plus basse que celle fournie par la troisième alimentation électrique (VDD) ;
un treizième transistor ayant une électrode de grille connectée à une électrode de grille du onzième transistor et ayant une première électrode connectée à la deuxième électrode du onzième transistor ;
un quatorzième transistor ayant une première électrode connectée à une deuxième électrode du treizième transistor, ayant une deuxième électrode connectée à la quatrième alimentation électrique, et ayant une électrode de grille connectée à l'unité d'entrée ;
un quinzième transistor ayant une première électrode connectée à une troisième borne d'entrée, ayant une deuxième électrode connectée à l'électrode de grille du onzième transistor, et ayant une électrode de grille connectée à une première borne d'entrée ;
un douzième condensateur connecté entre l'électrode de grille et la première électrode du onzième transistor ; et
un onzième condensateur connecté entre une électrode de grille du douzième transistor et la première électrode de grille du douzième transistor ;
dans lequel le circuit d'attaque de données (20) comprend en outre un condensateur connecté entre la quatorzième borne de sortie et la quatrième alimentation électrique ; et
dans lequel l'unité d'entrée comprend :

> un seizième transistor ayant une première électrode connectée à l'électrode de grille du quatorzième transistor et ayant une deuxième électrode connectée à la première borne d'entrée ;
> un dix-septième transistor ayant une première électrode connectée à une électrode de grille du seizième transistor, et ayant une électrode de grille et une deuxième électrode toutes deux connectées à une deuxième borne d'entrée ;
> un dix-huitième transistor ayant une électrode de grille connectée à la troisième borne d'entrée, ayant une première électrode connectée à la troisième alimentation électrique, et ayant une deuxième électrode connectée à l'électrode de grille du seizième transistor ; et
> un treizième condensateur connecté entre l'électrode de grille du seizième transistor et la première électrode du seizième transistor, dans lequel les onzième à dix-huitième transistors sont des transistors PMOS.

20. Circuit d'attaque de données selon la revendication 19, dans lequel l'unité de conversion (200) comprend des circuits de conversion de numéro pair et de numéro impair, et
les circuits de conversion de numéro impair reçoivent le premier signal d'horloge (CLK1) sur la première borne d'entrée, et reçoivent le deuxième signal d'horloge (CLK2) sur la deuxième borne d'entrée.

21. Circuit d'attaque de données selon la revendication 20, dans lequel les circuits de conversion de numéro pair reçoivent le deuxième signal d'horloge (CLK2) sur la première borne d'entrée, et reçoivent le premier signal d'horloge (CLK1) sur la deuxième borne d'entrée.

22. Circuit d'attaque de données selon la revendication 19, dans lequel le circuit de conversion (200) fournit en sortie un niveau de signal opposé à un signal fourni en entrée à la troisième borne d'entrée si un signal au niveau bas est fourni en entrée à la première borne d'entrée, et
le circuit de conversion (200) maintient une sortie d'une période précédente si un signal au niveau haut est fourni en entrée à la première borne d'entrée.

23. Affichage électroluminescent organique, comprenant :

> un circuit d'attaque de balayage (10) configuré pour fournir séquentiellement un signal de balayage à des lignes de balayage ;
> un circuit d'attaque de données (20) selon l'une des revendications 1 à 22, configuré pour fournir un signal de données à des lignes de données ; et
> une unité de pixels comprenant une pluralité de pixels électroluminescents organiques connectés aux lignes de balayage et aux lignes de données.

FIG. 1

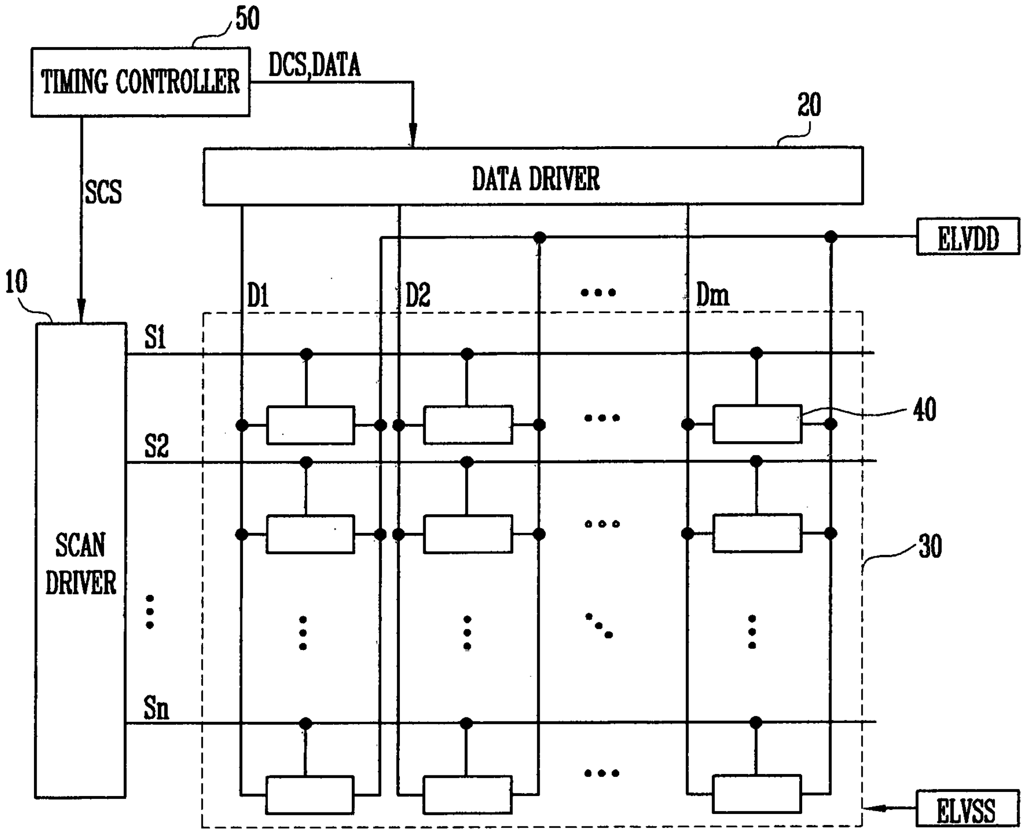

50
TIMING CONTROLLER
DCS,DATA
20
DATA DRIVER
SCS
ELVDD
10
D1
D2
Dm
S1
40
S2
SCAN DRIVER
30
Sn
ELVSS

FIG. 2

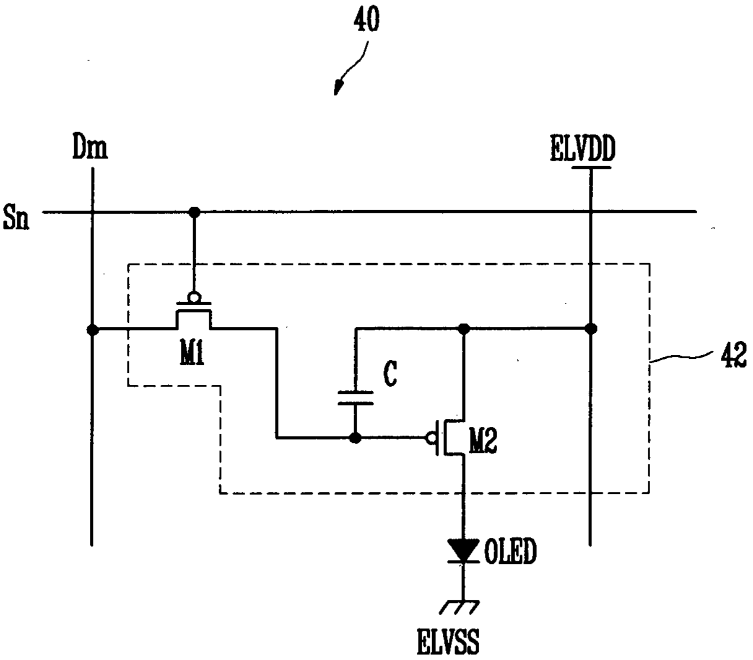

40
Dm
ELVDD
Sn
M1
C
42
M2
OLED
ELVSS

FIG. 3

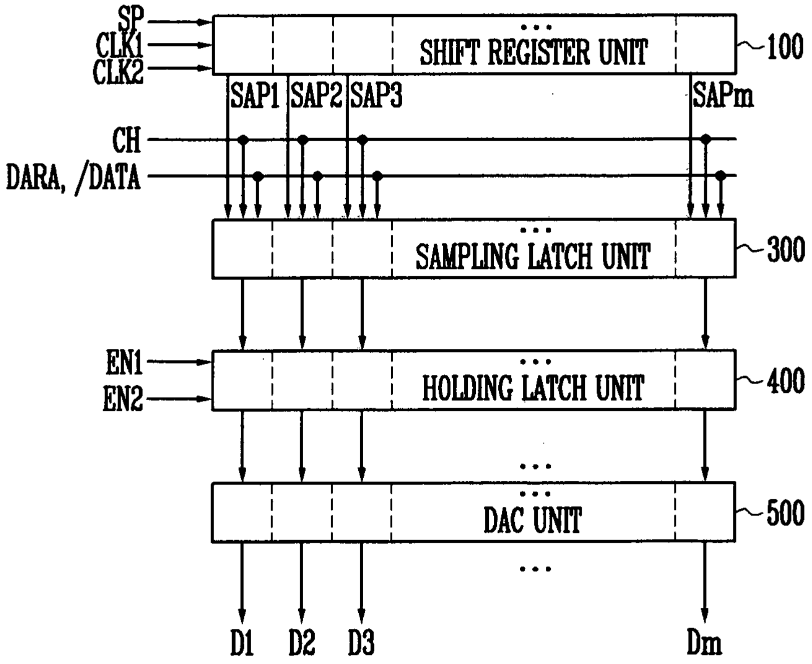

SP
CLK1
CLK2
SHIFT REGISTER UNIT
100
SAP1
SAP2
SAP3
SAPm
CH
DARA, /DATA
SAMPLING LATCH UNIT
300
EN1
EN2
HOLDING LATCH UNIT
400
DAC UNIT
500
D1
D2
D3
Dm

FIG. 4

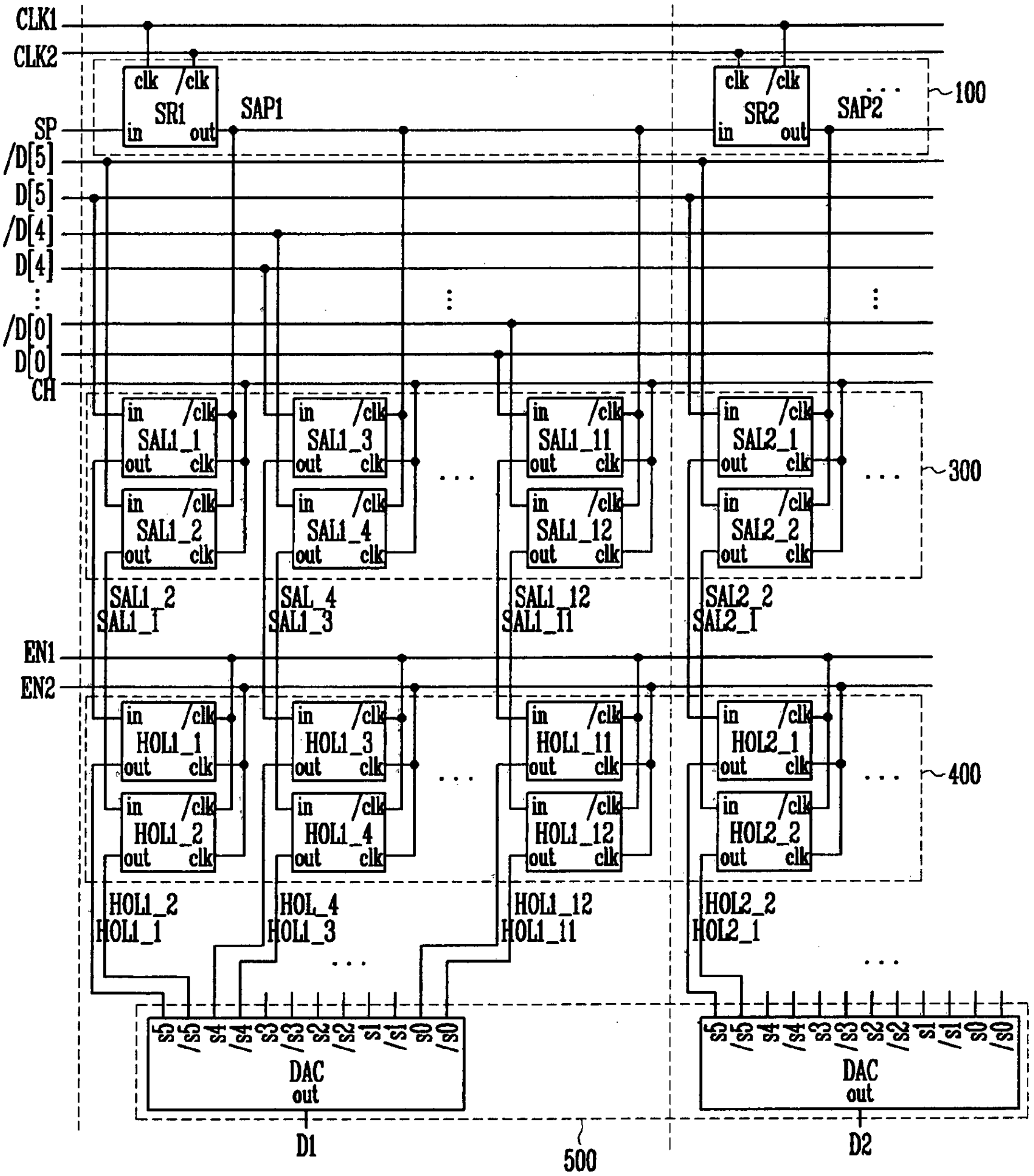

CLK1
CLK2
SP
/D[5]
D[5]
/D[4]
D[4]
/D[0]
D[0]
CH
EN1
EN2
clk /clk
SR1
in out
SAP1
SR2
SAP2
100
SAL1_1
SAL1_2
SAL1_3
SAL1_4
SAL1_11
SAL1_12
SAL2_1
SAL2_2
300
SAL1_2
SAL1_1
SAL_4
SAL1_3
SAL1_12
SAL1_11
SAL2_2
SAL2_1
HOL1_1
HOL1_2
HOL1_3
HOL1_4
HOL1_11
HOL1_12
HOL2_1
HOL2_2
400
HOL1_2
HOL1_1
HOL_4
HOL1_3
HOL1_12
HOL1_11
HOL2_2
HOL2_1
s5 /s5 s4 /s4 s3 /s3 s2 /s2 s1 /s1 s0 /s0
DAC
out
D1
500
D2

FIG. 5

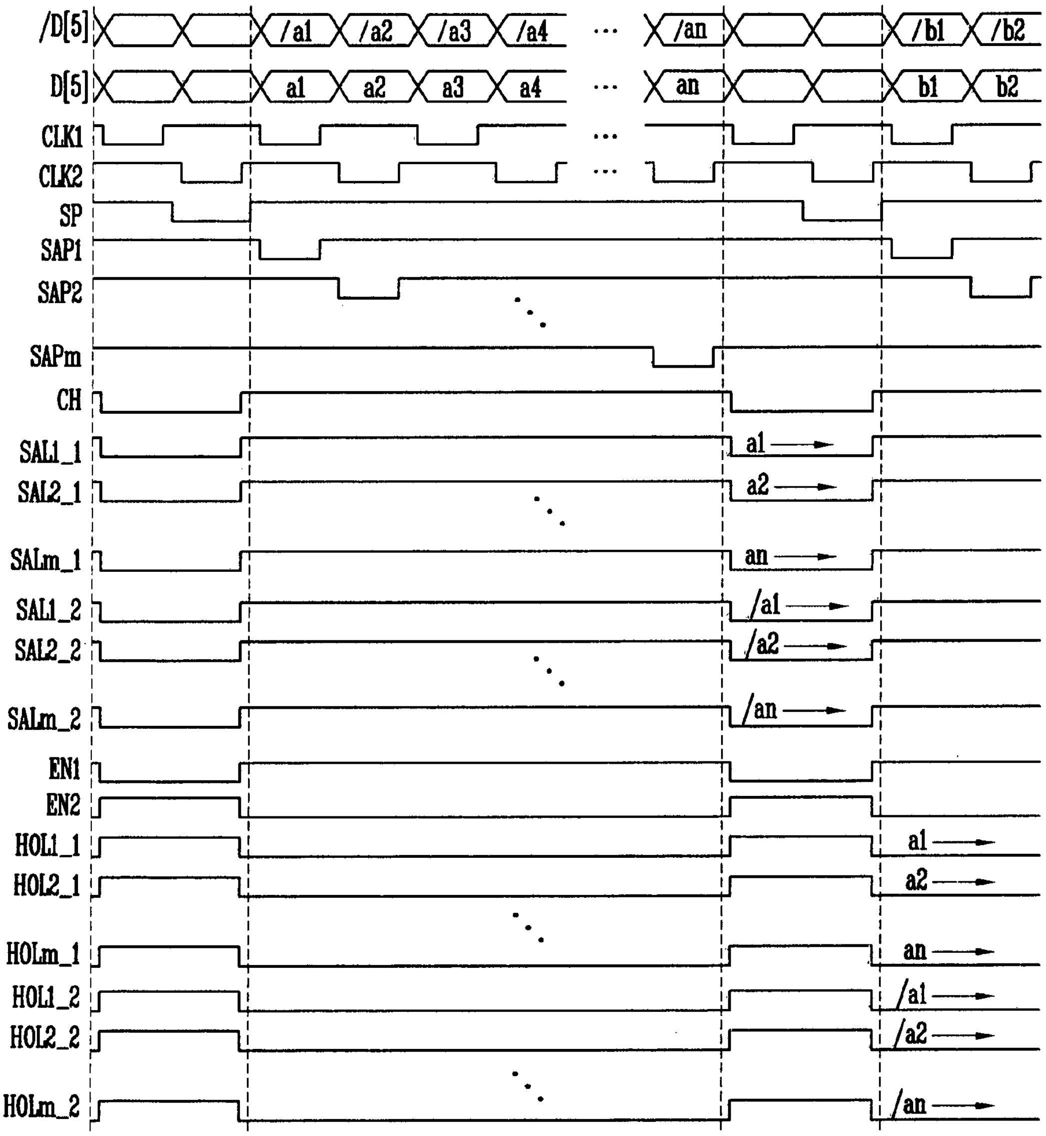

/D[5]
/a1
/a2
/a3
/a4
/an
/b1
/b2
D[5]
a1
a2
a3
a4
an
b1
b2
CLK1
CLK2
SP
SAP1
SAP2
SAPm
CH
SAL1_1
a1
SAL2_1
a2
SALm_1
an
SAL1_2
/a1
SAL2_2
/a2
SALm_2
/an
EN1
EN2
HOL1_1
a1
HOL2_1
a2
HOLm_1
an
HOL1_2
/a1
HOL2_2
/a2
HOLm_2
/an

FIG. 6

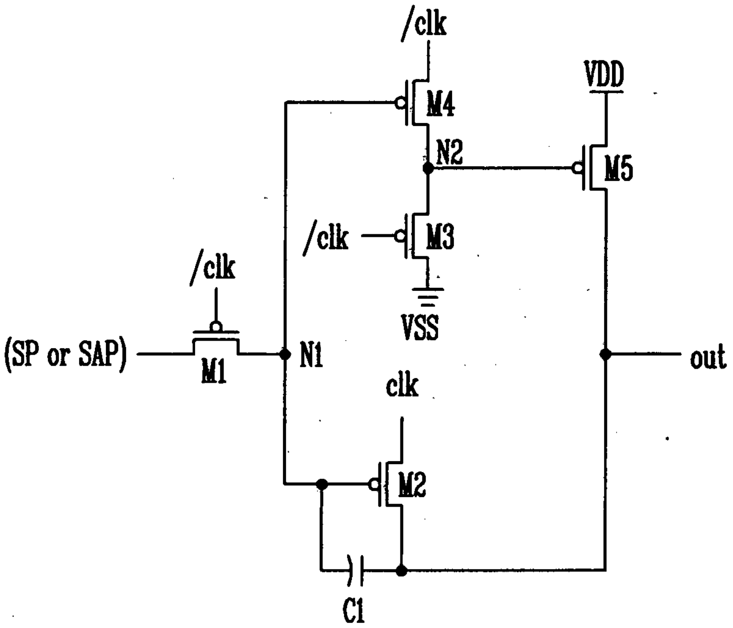

/clk
VDD
M4
N2
M5
/clk
M3
/clk
VSS
(SP or SAP)
M1
N1
out
clk
M2
C1

FIG. 7

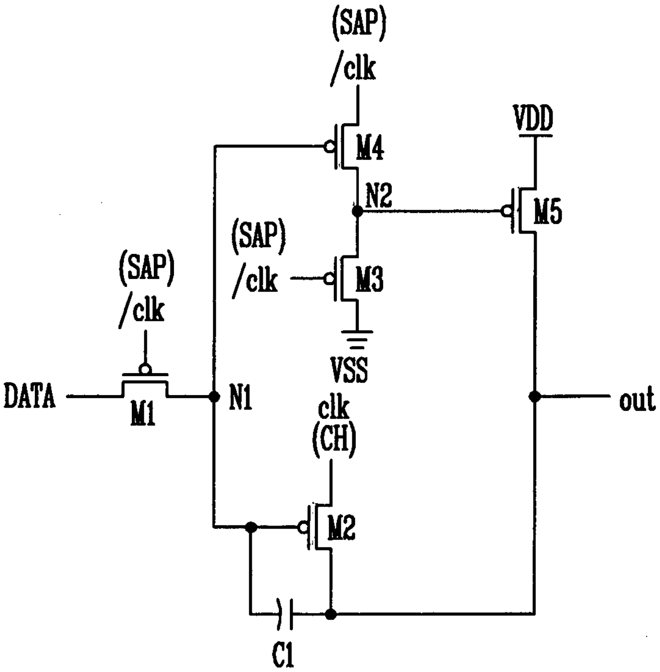

(SAP)
/clk
VDD
M4
N2
M5
(SAP)
/clk
M3
(SAP)
/clk
VSS
DATA
M1
N1
out
clk
(CH)
M2
C1

FIG. 8

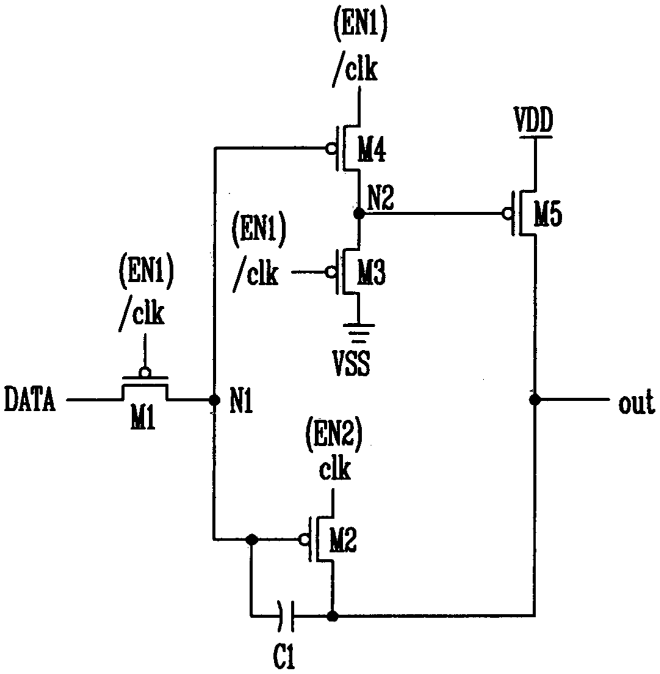

(EN1)
/clk
M4
VDD
N2
M5
(EN1)
/clk
M3
(EN1)
/clk
VSS
DATA
M1
N1
out
(EN2)
clk
M2
C1

FIG. 9

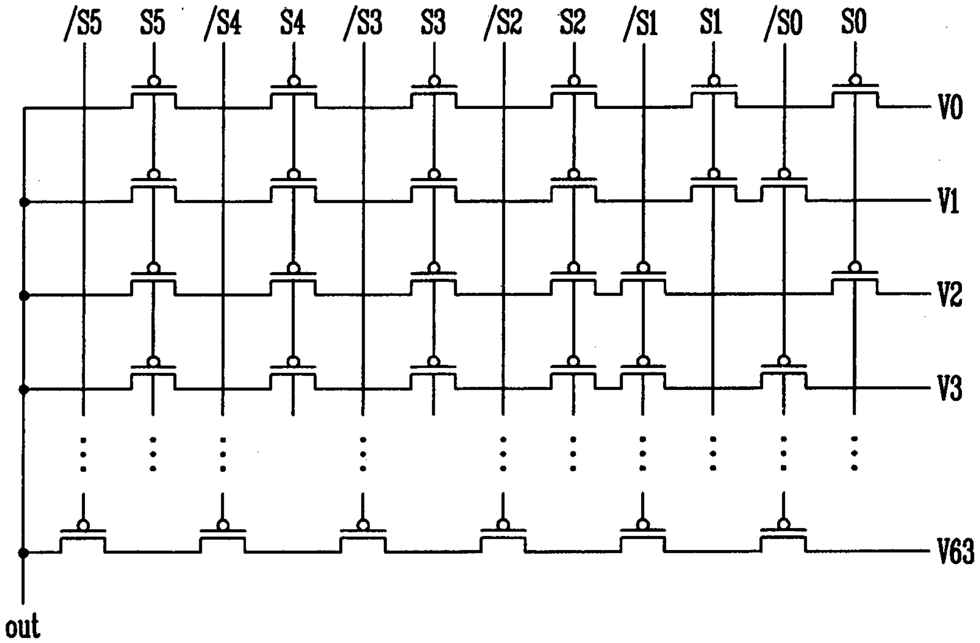

/S5
S5
/S4
S4
/S3
S3
/S2
S2
/S1
S1
/S0
S0
V0
V1
V2
V3
V63
out

FIG. 10

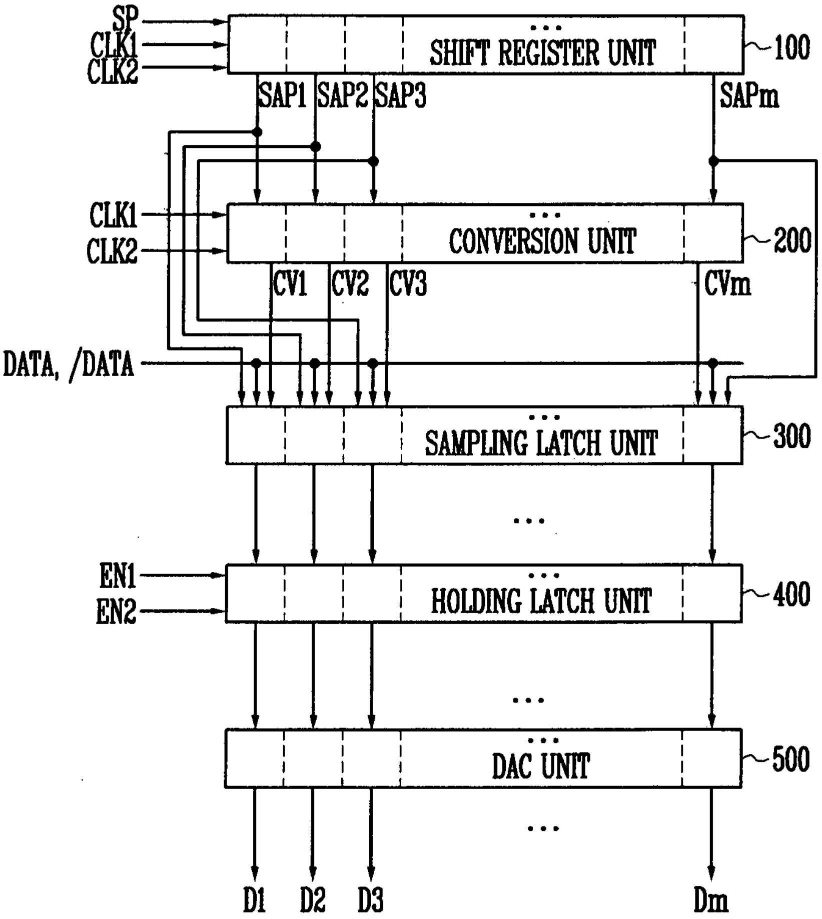

SP
CLK1
CLK2
SHIFT REGISTER UNIT
100
SAP1
SAP2
SAP3
SAPm
CLK1
CLK2
CONVERSION UNIT
200
CV1
CV2
CV3
CVm
DATA, /DATA
SAMPLING LATCH UNIT
300
EN1
EN2
HOLDING LATCH UNIT
400
DAC UNIT
500
D1
D2
D3
Dm

FIG. 11

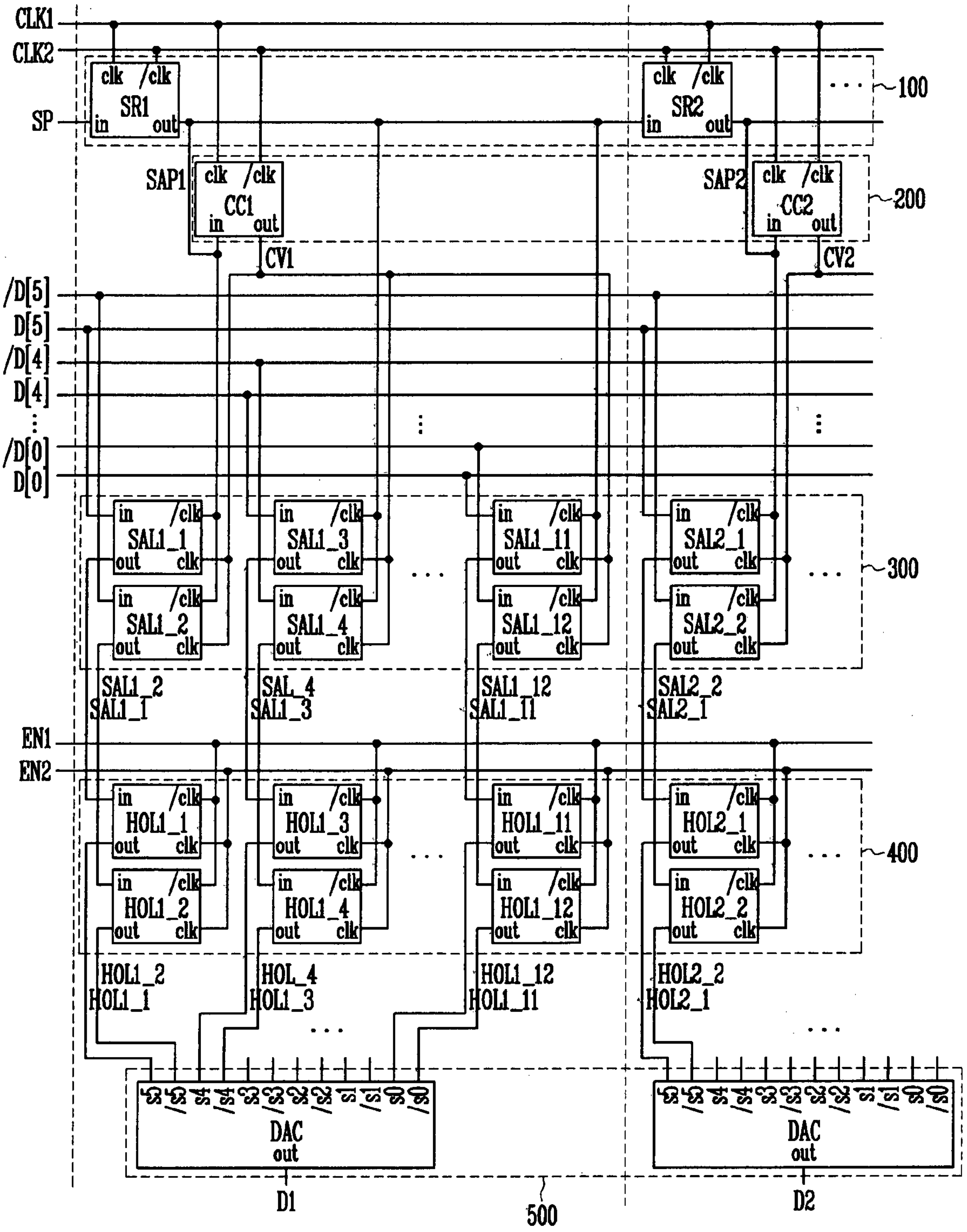

CLK1
CLK2
SP
clk
/clk
SR1
in
out
SR2
100
SAP1
CC1
SAP2
CC2
200
CV1
CV2
/D[5]
D[5]
/D[4]
D[4]
/D[0]
D[0]
SAL1_1
SAL1_2
SAL1_3
SAL1_4
SAL1_11
SAL1_12
SAL2_1
SAL2_2
300
SAL1_2
SAL1_1
SAL_4
SAL1_3
SAL1_12
SAL1_11
SAL2_2
SAL2_1
EN1
EN2
HOL1_1
HOL1_2
HOL1_3
HOL1_4
HOL1_11
HOL1_12
HOL2_1
HOL2_2
400
HOL1_2
HOL1_1
HOL_4
HOL1_3
HOL1_12
HOL1_11
HOL2_2
HOL2_1
S5
/S5
S4
/S4
S3
/S3
S2
/S2
S1
/S1
S0
/S0
DAC
out
D1
500
D2

FIG. 12

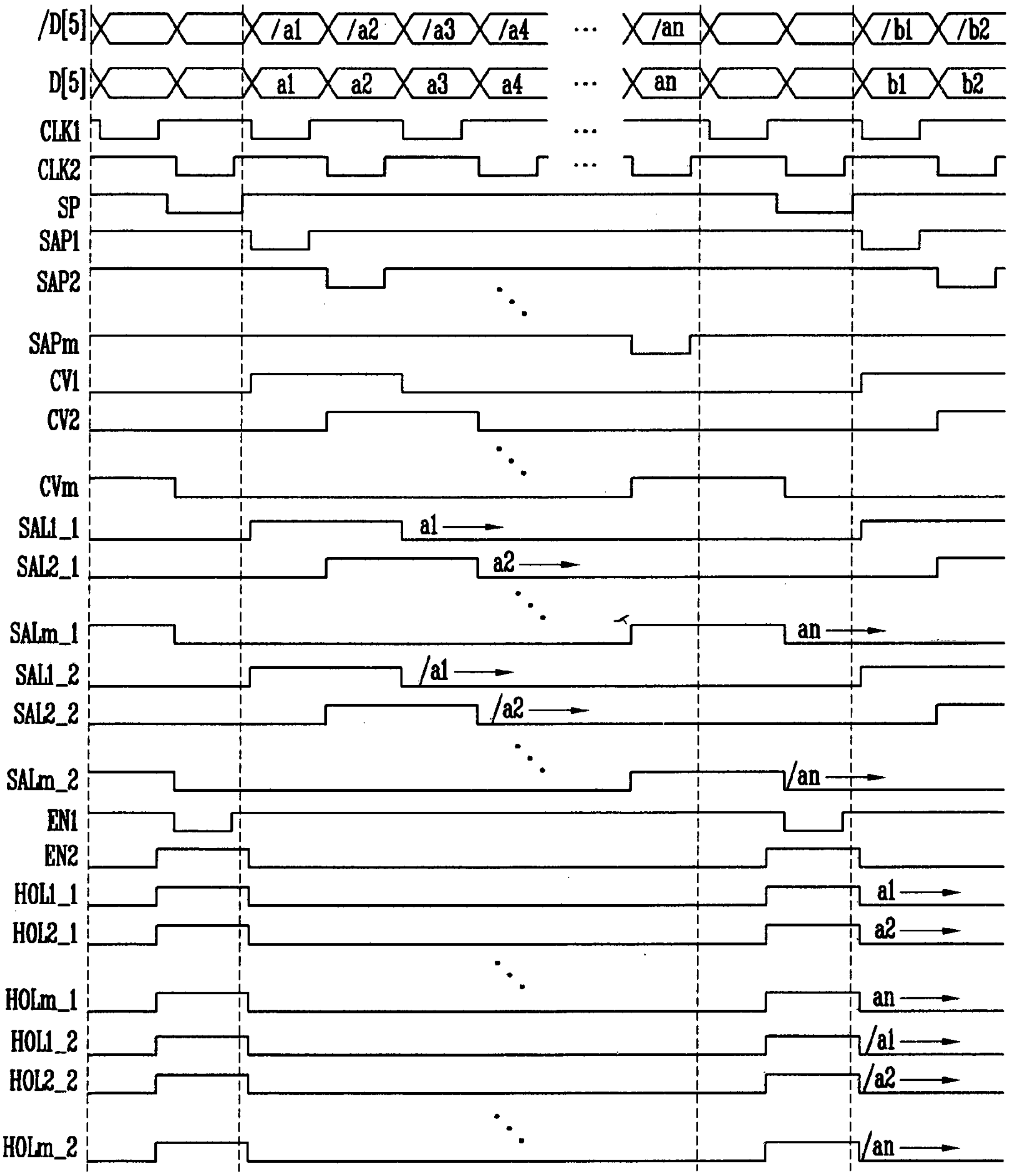

/D[5]
/a1
/a2
/a3
/a4
/an
/b1
/b2
D[5]
a1
a2
a3
a4
an
b1
b2
CLK1
CLK2
SP
SAP1
SAP2
SAPm
CV1
CV2
CVm
SAL1_1
a1
SAL2_1
a2
SALm_1
an
SAL1_2
/a1
SAL2_2
/a2
SALm_2
/an
EN1
EN2
HOL1_1
a1
HOL2_1
a2
HOLm_1
an
HOL1_2
/a1
HOL2_2
/a2
HOLm_2
/an

FIG. 13

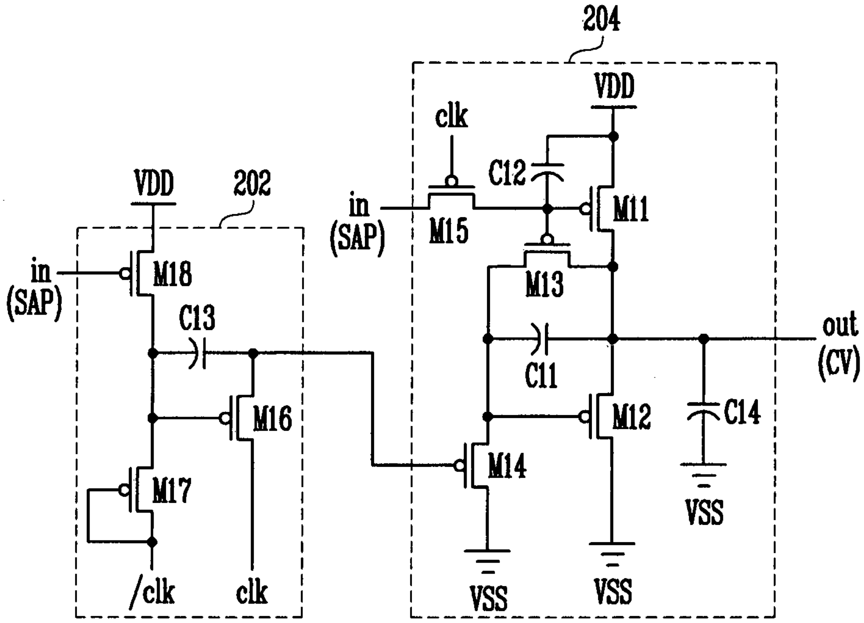
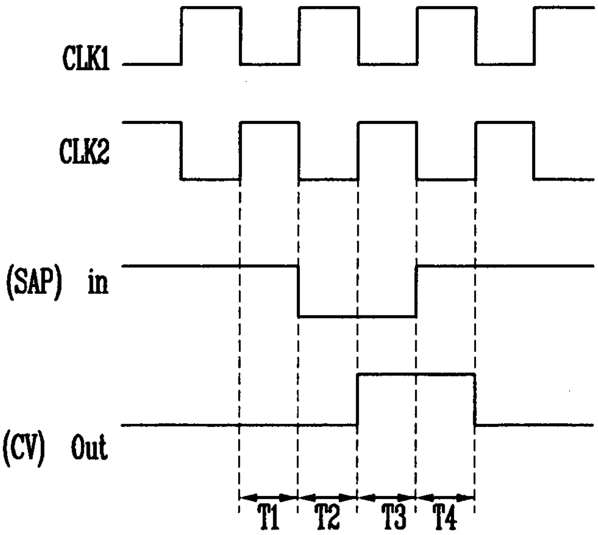

204
VDD
clk
C12
M11
in
(SAP)
M15
M13
202
VDD
in
(SAP)
M18
C13
out
(CV)
C11
M16
M12
C14
M14
M17
VSS
VSS
VSS
/clk
clk

FIG. 14


CLK1
CLK2
(SAP) in
(CV) Out
T1
T2
T3
T4

REFERENCES CITED IN THE DESCRIPTION

Patent documents cited in the description

- EP 1300826 A2 **[0006]**
- US 2004119666 A1 **[0008]**
- WO 2004086347 A2 **[0009]**

Non-patent literature cited in the description

- **MATSUEDA Y et al.** 35.1: 2.5-in. AMOLED with integrated 6-Bit Gamma Compensated Digital Data Driver. *2004 SID INTERNATIONAL SYMPOSIUM,* 25 May 2004, 1116-1119 **[0007]**

专利名称(译)	数据驱动器和使用其的有机发光显示器		
公开(公告)号	EP1843312B1	公开(公告)日	2015-05-06
申请号	EP2007103920	申请日	2007-03-12
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	SHIN DONG YONG LEGAL & IP TEAM		
发明人	SHIN, DONG YONG LEGAL & IP TEAM		
IPC分类号	G09G3/20 G09G3/32		
CPC分类号	G09G3/20 G09G3/3275 G09G2300/0408 G09G2310/027 G09G2310/08		
优先权	1020060031637 2006-04-06 KR		
其他公开文献	EP1843312A1		
外部链接	Espacenet		

摘要(译)

一种数据驱动器，包括：移位寄存器单元，被配置为接收第一时钟信号，第二时钟信号和起始脉冲;以及产生采样脉冲;采样锁存单元，被配置为接收和输出位和反转的数字数据位，与采样脉冲相对应的保持锁存单元，被配置为接收由采样锁存单元输出的比特和反转比特，并且与第一使能信号和第二使能信号相对应地输出比特和反转比特，以及数模转换器，被配置为接收由保持锁存单元输出的比特和反转比特，并产生与接收的比特和反转比特的值相对应的模拟信号。

FIG. 1