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(54) **Data driver, organic light emitting display, and method of driving the same**

Datentreiber, organische lichtemittierende Anzeige und Verfahren zu ihrer Ansteuerung

Dispositif de pilotage de données, affichage électroluminescent organique et procédé de commande de celui-ci

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- **OBORN P K ET AL: "A new digital to analog converter resistor string architecture" ASIC CONFERENCE AND EXHIBIT, 1997. PROCEEDINGS., TENTH ANNUAL IEEE INTERNATIONAL PORTLAND, OR, USA 7-10 SEPT. 1997, NEW YORK, NY, USA, IEEE, US, 7 September 1997 (1997-09-07), pages 304-307, XP010243411 ISBN: 0-7803-4283-6**

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Description**BACKGROUND OF THE INVENTION**5 **1. Field of the Invention**

[0001] The present invention relates to a data driver, an organic light emitting display, and a method of driving the same. More particularly, the present invention relates to a data driver for enhancing image quality, an organic light emitting display, and a method of driving the same.

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2. Description of the Related Art

[0002] Various flat panel display devices having reduced weight and volume compared to comparable cathode ray tubes (CRTs) have been developed. These flat panel display devices include for example, a liquid crystal display, a field emission display, a plasma display panel, an organic light emitting display, etc. These exemplary displays may operate differently to display an image.

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[0003] For example, an organic light emitting display displays an image by using an organic light emitting diode that generates light by recombining electrons and holes. During operation, such an organic light emitting display supplies a current corresponding to a data signal to organic light emitting diodes by employing driving, thin film transistors formed at each pixel so light may be emitted from the organic light emitting diodes. Such an organic light emitting display may offer certain advantages, since it may be operated with low power consumption and may provide a rapid response speed.

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[0004] An organic light emitting display may generate data signals by using data supplied from an external source. The organic light emitting display supplies the generated data signals to pixels and display an image of desired brightness. A data driver for converting the data supplied from the external source into the data signals has been considered.

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[0005] Such a data driver may include a data signal generator for converting the external data into the data signals. The data signal generator may include a digital-to-analog converter (hereinafter, referred to as "DAC"). The DAC is positioned in each channel and converts the data into the data signals. For example, the data signal generator may include first DACs for generating voltages depending on the values of the upper bits of the data and second DACs for generating voltages depending on the values of the lower bits of the data.

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[0006] FIG. 1 illustrates a circuit diagram of a second DAC. Referring to FIG. 1, the second DAC 2 receives a first reference voltage (ref1) and a second reference voltage (ref2) from a first DAC (not illustrated). The first DAC receives a plurality of reference voltages from an external source. The first DAC selects the first reference voltage (ref1) and the second reference voltage (ref2) among the plurality of reference voltages received depending on a value of the upper bits of the data. The first DAC supplies the selected first and second reference voltages (ref1) and (ref2) to the second DAC 2 via a tenth switch SW 10 and an eleventh switch SW11, as illustrated in FIG. 1. That is, the tenth switch SW10 or the eleventh switch SW11 included in the first DAC may be turned on depending on the value of the upper bits of the data. For the sake of discussion, the present invention will be described assuming that the first reference voltage (ref1) is lower than the second reference voltage (ref2).

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[0007] The second DAC 2 includes a plurality of voltage dividing resistors R1 to R7 for dividing the voltage values of the first reference voltage (ref1) and the second reference voltage (ref2). The second DAC2 also includes a plurality of switches SW1 to SW8 for supplying voltages divided from the voltage dividing resistors R1 to R7 to an output terminal (out).

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[0008] A tenth resistor R10 is arranged between the eleventh switch SW11 and the seventh resistor R7. The tenth resistor R10 compensates for the switch resistances of the tenth switch SW 10 and the eleventh switch SW11 so that the second DAC may evenly divide the reference voltages via the voltage dividing resistors R1 to R7.

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[0009] The voltage dividing resistors R1 to R7 are arranged in series. The voltage dividing resistors R1 to R7 evenly divide the first reference voltage (ref1) and the second reference voltage (ref2). In this regard, the resistance value of each of the voltage dividing resistors R1 to R7 may be identical.

[0010] The switches SW1 to SW8 are arranged to supply the voltages divided by the voltage dividing resistors R1 to R7 to the output terminal (out). In particular, the first switch SW 1 is arranged between a first node N1 and the output terminal (out) to supply the second reference voltage (ref2) to the output terminal (out). The second switch SW2 is arranged between a second node N2 and the output terminal (out) to supply the voltage value of the second node N2 to the output terminal (out). The third switch SW3 is arranged between a third node N3 and the output terminal (out) to supply the voltage value of the third node N3 to the output terminal (out). The fourth switch SW4 is arranged between a fourth node N4 and the output terminal (out) to supply the voltage value of the fourth node N4 to the output terminal (out). The fifth switch SW5 is arranged between a fifth node N5 and the output terminal (out) to supply the voltage value of the fifth node N5 to the output terminal (out). The sixth switch SW6 is arranged between a sixth node N6 and the output terminal (out) to supply the voltage value of the sixth node N6 to the output terminal (out). The seventh switch SW7 is arranged between a seventh node N7 and the output terminal (out) to supply the voltage value of the seventh

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node N7 to the output terminal (out). The eighth switch SW8 is arranged between an eighth node N8 and the output terminal (out) to supply the first reference voltage (ref1) to the output terminal (out).

[0011] During operation, one of the switches SW1 to SW8 may be turned on depending on the value of the lower bits of the data, and a predetermined voltage is supplied to the output terminal (out). The predetermined voltage value

supplied to the output terminal (out) is supplied to pixels as a data signal.

[0012] The conventional second DAC 2 may exhibit a deterioration of its driving ability when supplying a gray scale voltage, such as an intermediate gray scale voltage (e.g., voltages of node N4 or node N5) as a data signal. In other words, since the intermediate gray scale voltage is supplied to the output terminal (out) via a plurality of resistors, a period of time is required before intermediate gray scale voltages corresponding to the data signals may be supplied to the pixels. For example, some intermediate gray scale voltages (e.g., voltages of node N1, node N2, node N6 and node N7) adjacent to the first reference voltage (ref1) and the second reference voltage (ref2) may be supplied and charged in the pixels within a shorter period of time than other intermediate gray scale voltages (e.g., voltages of node N4 or node N5).

[0013] In order to resolve this deficiency, it has been proposed to lower the resistance values of the voltage dividing resistors R1 to R7 between the first reference voltage ref1 and the second reference voltage ref2. It may be understood that if the resistance value between the first reference voltage (ref1) and the second reference voltage (ref2) is lowered, the driving ability of the intermediate gray scale may be enhanced. That is, it may be possible to supply and charge the pixels with a predetermined voltage within a predetermined time period. However, if the resistance value between the first reference voltage (ref1) and the second reference voltage (ref2) is lowered, the value of constant current flowing into the voltage dividing resistors R1 to R7 increases. This increase in the value of constant current flowing may generate a phenomenon known as voltage drop. If voltage drop is generated, the voltage values of the intermediate gray scale voltages adjacent to the first reference voltage (ref1) and the second reference voltage (ref2) may be altered, as illustrated in FIG. 2. Thus, the predetermined voltage may not be supplied and charged in the pixels. The voltage values of the intermediate gray scale voltages more centered between the first reference voltage (ref1) and the second reference

voltage (ref2) may maintain approximately similar values, regardless of the voltage drop.

[0014] As discussed above, a conventional organic light emitting display may operate with certain deficiencies. That is, if the resistance values of the voltage dividing resistors R1 to R7 between the first reference voltage (ref1) and the second reference voltage (ref2) are large, the driving ability of the intermediate gray scale may be deteriorated, and if the resistance values of the voltage dividing resistors R1 to R7 are small, the gray scale voltage values adjacent to the first reference voltage (ref1) and the second reference voltage (ref2) may be altered.

[0015] US5,389,872 discloses a system for minimizing switching errors in voltages delivered to a resistive load. The system relies on varying the resistance in switches to compensate for output voltage errors.

[0016] US2003/0090402 discloses a DAC that comprises two sets of n resistors, two power-supply voltage lines maintained at different potentials and two sets of n switches.

[0017] OBORN K ET AL: "A new digital to analog converter resistor string architecture" ASIC Conference and exhibit, 1997. Proceedings., Tenth Annual IEEE International Portland, OR, USA 7-10 Sept. 1997, New York, NY, USA, IEEE, US, 7 September 1997 (1997-09-07), pages 304-307, XP010243411 ISBN:0-7803-4283-6 discloses a resistor string architecture for implementing a DAC on a CMOS circuit process. The DAC uses virtual resistance coding.

[0018] US6,037,889 discloses an apparatus which aims to improve both the matching of the integral non-linearity of multiple resistor-string based DACs connected in parallel between two different reference voltages and the charge/discharge time of the parasitic capacitances associated with middle nodes of the AC resistor strings.

SUMMARY OF THE INVENTION

[0019] The present invention is therefore directed to a data driver, an organic light emitting display, and a method of driving the same that sets out to overcome one or more of the problems due to the limitations and disadvantages of the related art.

[0020] It is therefore a feature of an embodiment of the present invention to provide a data driver and an organic light emitting display that includes a second DAC configured to enhance image quality.

[0021] It is therefore another feature of an embodiment of the present invention to provide a data driver and an organic light emitting display that includes a second DAC configured to enhance the driving ability of a data driver.

[0022] It is therefore another feature of an embodiment of the present invention to provide a data driver and an organic light emitting display that includes a second DAC that reduces the occurrence of voltage drop.

[0023] According to a first aspect of the invention, there is provided a data driver as set out in claim 1. Preferred features are set out in claims 2 to 11.

[0024] According to a second aspect of the invention, there is provided an organic light emitting display as set out in claim 12.

[0025] According to a third aspect of the invention, there is provided a method of driving an organic light emitting

display as set out in claim 13. Preferred features are set out in claims 14 to 16.

BRIEF DESCRIPTION OF THE DRAWINGS

5 **[0026]** The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing in detail embodiments thereof with reference to the attached drawings, in which:

FIG. 1 illustrates a circuit diagram of a conventional second DAC;

FIG. 2 illustrates a diagram of an alteration of gray scale voltage levels due to voltage drop;

10 FIG. 3 illustrates a block circuit diagram of an organic light emitting display according to an embodiment of the present invention;

FIGS. 4A and FIG. 4B illustrate block circuit diagrams of an embodiment of the data driving circuit illustrated in FIG. 3;

FIG. 5 illustrates a block circuit diagram of an embodiment of the data signal generator illustrated in FIGS. 4A and 4B;

FIG. 6 illustrates a circuit diagram of a second DAC according to a first embodiment of the present invention; and

15 FIG. 7 illustrates a circuit diagram of a second DAC according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

20 **[0027]** The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are illustrated. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0028] Hereinafter, embodiments according to the present invention will be described with reference to the accompanying FIGS. 3 to 7.

25 **[0029]** FIG. 3 illustrates a block circuit diagram of an organic light emitting display according to an embodiment of the present invention. Referring to FIG. 3, the organic light emitting display includes a pixel unit 230 including pixels 240 formed on a region where scan lines S 1 to S_n are intersected with data lines D1 to D_m, a scan driver 210 for driving scan lines S1 to S_n, a data driver 220 for driving data lines D1 to D_m, and a timing controller 250 for controlling the scan driver 210 and the data driver 220. The data driver 220 includes at least one data driving circuit 222.

30 **[0030]** The scan driver 210 generates scan signals in response to scan driving control signals SCS from the timing controller 250. The scan driver 210 may supply the generated scan signals to the scan lines S 1 to S_n in sequence. The scan driver 210 generates light emitting control signals in response to the scan driving control signals SCS. The scan driver may supply the generated light emitting control signals to light emitting control lines E1 to E_n in sequence.

35 **[0031]** The data driver 220 generates data signals in response to data driving control signals DCS from the timing controller 250. The data driver 220 may supply the generated data signals to the data lines D1 to D_m in sequence. The data driving circuit 222 converts data supplied from an external source into data signals and supplies the data signals to the data lines D 1 to D_m. The data driving circuit 222 will be described in more detail below.

40 **[0032]** The timing controller 250 generates a data driving control signal DCS and a scan driving control signal SCS depending on synchronization signals supplied from an external source. The data driving control signal DCS and the scan driving control signal SCS generated from the timing controller 250 are supplied to the data driver 220 and to the scan driver 210, respectively. The timing controller 250 rearranges the data supplied from the external source and supplies the rearranged data DATA to the data driver 220.

45 **[0033]** The pixel unit 230 receives a first power source ELVDD and a second power source ELVSS from an external source. The first power source ELVDD and the second power source ELVSS are supplied to the pixel unit 230, and are respectively supplied to the pixels 240. The pixels 240 receiving the first power source ELVDD and the second power source ELVSS displays images corresponding to data signals supplied from the data driving circuit 222.

[0034] FIG. 4A illustrates a block circuit diagram of an embodiment of the data driving circuit illustrated in FIG. 3. For the sake of discussion, FIG. 4A will be described assuming that the data driving circuit 222 includes "i" channels.

50 **[0035]** Referring to FIG. 4A, the data driving circuit 222 includes the following:

a shift register unit 223 for supplying sampling signals in sequence, a sampling latch unit 224 for storing data DATA in sequence in response to the sampling signals, a holding latch unit 225 for temporarily storing data stored in the sampling latch unit 224 and supplying the stored data to a level shifter 226, a level shifter 226 for raising a voltage level of the data, and a data signal generator 227 for generating data signals corresponding to bit values of data.

55 **[0036]** The shift register unit 223 receives a source shift clock SSC and a source start pulse SSP from the timing controller 250. The shift register unit 223 receiving the source shift clock SSC and the source start pulse SSP may generate "i" sampling signals in sequence, while allowing the source start pulse SSP to be shifted depending on the

source shift clock SSC. The shift register unit 223 includes "i" shift registers 2231 to 223i.

[0037] The sampling latch unit 224 stores data in sequence depending on the sampling signals supplied in sequence from the shift register unit 223. The sampling latch unit 224 includes "i" sampling latches 2241 to 224i for storing "i" data. Each size of the sampling latches 2241 to 224i may be set to store k bit data. For the sake of discussion, this exemplary sampling latch unit 224 will be described assuming that k bit is 6 bits.

[0038] The holding latch unit 225 receives and stores the data from the sampling latch unit 224 in response to a source output enable SOE signal. The holding latch unit 225 supplies the stored data to a level shifter 226. The holding latch unit 225 includes "i" holding latches 2251 to 225i. Each of the holding latches 2251 to 225i may be configured to store k bit data.

[0039] The level shifter 226 raises a voltage level of the data supplied from the holding latch unit 225 and supplies the data with a raised voltage level to the data signal generator 227. In this regard, the data driver 220 receives data having a low voltage level and raises the voltage level of the data to a high voltage level by employing the level shifter 226.

[0040] In other implementations, the data driver 220 may not include the level shifter 226. For example, circuit components necessary to raise the voltage level of the data from a low voltage level to a high voltage level may be arranged external to the data driver 220. Accordingly, the holding latch unit 225 may be directly connected to the data signal generator 227. In such an arrangement, however, manufacturing costs may be increased.

[0041] The data signal generator 227 generates data signals corresponding to bit values (or gray scale values) of the data and supplies the generated data signals to the data lines D1 to Di. The data signal generator 227 receives a plurality of reference voltages (refs) from a gamma voltage unit 229 and generates data signals by using the received reference voltages (refs). The data signal generator 227 will be described in more detail below.

[0042] The gamma voltage unit 229 supplies the plurality of reference voltages (refs) to the data signal generator 227. The gamma voltage unit 229 may be arranged inside or outside of the data driving circuit 222.

[0043] Referring to FIG. 4B, a buffer unit 228 is connected between the data signal generator 227 and the data lines D1 to Di. The buffer unit 228 supplies the data signals supplied from the data signal generator 227 to the data lines D1 to Di.

[0044] FIG. 5 illustrates a block circuit diagram of an exemplary data signal generator as illustrated in FIGS. 4A and 4B. Referring to FIG. 5, the data signal generator 227 includes, for each channel, a first DAC 300, a second DAC 302 and a decoder unit 304.

[0045] The first DAC 300 receives the plurality of reference voltages (ref) from a gamma unit 229. The first DAC 300 selects a first reference voltage (ref1) and a second reference voltage (ref2) from the plurality of reference voltages (refs) depending on, e.g., a value of upper bits of the data. The first DAC 300 receives the data from the level shifter 226, or directly from the holding latch unit 225, depending on the implementation.

[0046] The first DAC 300 supplies the first reference voltage (ref1) and the second reference voltage (ref2) to the second DAC 302 via a first line L1 and a second line L2, respectively. That is, the first DAC 300 may extract two reference voltages from the plurality of reference voltages (refs) depending on the value of the upper bits. The first DAC 300 supplies the extracted two reference voltages to the second DAC 302 as the first reference voltage (ref1) and the second reference voltage (ref2). For the sake of discussion, it will be assumed that the first reference voltage (ref1) is set to be lower than the second reference voltage (ref2).

[0047] The second DAC 302 divides the first reference voltage (ref1) and the second reference voltage (ref2) into a plurality of voltages. The second DAC 302 may supply any one of the first reference voltage (ref1), the second reference voltage (ref2) and the divided voltages to the output terminal (out) as a data signal, depending on a value of the lower bits of the data.

[0048] The decoder unit 304 controls the turning on and the turning off of switches included in the second DAC 302 depending on the value of the lower bits of the data. That is, the decoder unit 304 may control the turning on and the turning off of the switches so that a resistance value between the first line L1 and the second line L2 can be variably controlled depending on the value of the lower bits of the data.

[0049] FIG. 6 illustrates a circuit diagram of a second DAC according to a first embodiment of the present invention. Referring to FIG. 6, the second DAC 302 includes a first group of voltage dividing resistors R11 to R18, a second group of voltage dividing resistors R21 to R28, a third group of voltage dividing resistors R31 to R38, a fourth group of voltage dividing resistors R41 to R48, and a fifth group of voltage dividing resistors R51 to R58, which are arranged between the first line L1 and the second line L2. The second DAC 302 also includes an arrangement of switches. The switches will be described in more detail below.

[0050] The first group of voltage dividing resistors R11 to R18 are arranged between the first line L1 and the second line L2 in series. The first group of voltage dividing resistors R11 to R18 divide the voltages of the first reference voltage (ref1) and the second reference voltage (ref2). The resistance values of the first group of voltage dividing resistors R11 to R18 may be identical so that the first reference voltage (ref1) and the second reference voltage (ref2) may be evenly divided.

[0051] A first switch SW1 is arranged between the first group of voltage dividing resistors R11 to R18 and the first line L1. The first switch SW1 allows the first group of voltage dividing resistors R11 to R18 to be electrically connected to

the first line L1 and may remain in a turned on state. The first switch SW 1 is arranged in order to compensate for the turn on resistances of a second switch SW2, a third switch SW3, a fourth switch SW4, and a fifth switch SW5, which will be described below.

5 [0052] The second group of voltage dividing resistors R21 to R28 is arranged in parallel with the first group of voltage dividing resistors R11 to R18, and is between the first line L1 and the second line L2. The number of resistors in the second group of voltage dividing resistors R21 to R28 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The second switch SW2 is arranged between the second group of voltage dividing resistors R21 to R28 and the first line L1.

10 [0053] During an exemplary operation, a first control signal CS1 is supplied from the decoder unit 304, and the second switch SW2 may be turned on. When the second switch SW2 is turned on, the second group of voltage dividing resistors R21 to R28 may be electrically connected to the first line L1. If the second group of voltage dividing resistors R21 to R28 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become lower than the case when only the first group of voltage dividing resistors R11 to R18 is electrically connected to first line L1 and the second line L2.

15 [0054] The third group of voltage dividing resistors R31 to R38 is arranged in parallel with the second group of voltage dividing resistors R21 to R28, between the first line L1 and the second line L2. The number of resistors in the third group of voltage dividing resistors R31 to R38 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The third switch SW3 is arranged between the third group of voltage dividing resistors R31 to R38 and the first line L1.

20 [0055] During an exemplary operation, a second control signal CS2 is supplied from the decoder unit 304, and the third switch SW3 may be turned on. When the third switch SW3 is turned on, the third group of voltage dividing resistors R31 to R38 may be electrically connected to the first line L1. If the third group of voltage dividing resistors R31 to R38 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become even lower than the case when the first group of voltage dividing resistors R11 to R18 and the second group of voltage dividing resistors R21 to R28 are electrically connected to the first line L1.

25 [0056] The fourth group of voltage dividing resistors R41 to R48 is arranged in parallel with the third group of voltage dividing resistors R31 to R38, between the first line L1 and the second line L2. The number of resistors in the fourth group of voltage dividing resistors R41 to R48 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The fourth switch SW4 is arranged between the fourth group of voltage dividing resistors R41 to R48 and the first line L1.

30 [0057] During an exemplary operation, a third control signal CS3 is supplied from the decoder unit 304, and the fourth switch SW4 is turned on. When the fourth switch SW4 is turned on, the fourth group of voltage dividing resistors R41 to R48 may be electrically connected to the first line L1. If the fourth group of voltage dividing resistors R41 to R48 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become even lower than the case when the first voltage group of dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, and the third group of voltage dividing resistors R31 to R38 are electrically connected to the first line L1.

35 [0058] The fifth group of voltage dividing resistors R51 to R58 is arranged in parallel with the fourth group of voltage dividing resistors R41 to R48, and is between the first line L1 and the second line L2. The number of resistors in the fifth group of voltage dividing resistors R51 to R58 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The fifth switch SW5 is arranged between the fifth group of voltage dividing resistors R51 to R58 and the first line L1.

40 [0059] During an exemplary operation, a fourth control signal CS4 is supplied from the decoder unit 304, and the fifth switch SW5 may be turned on. When the fifth switch SW5 is turned on, the fifth group of voltage dividing resistors R51 to R58 may be electrically connected to the first line L1. If the fifth group of voltage dividing resistors R51 to R58 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become even lower than the case when the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38 and the fourth group of voltage dividing resistors R41 to R48 are electrically connected to the first line L1.

45 [0060] For the sake of discussion, FIG. 6 illustrates four voltage dividing resistor columns R21 to R28, R31 to R38, R41 to R48, and R51 to R58 that are arranged in parallel to the first group of voltage dividing resistors R11 to R18; however the present invention is not limited thereto. One or more voltage dividing resistor columns is in parallel with the first group of voltage dividing resistors R11 to R18.

50 [0061] The second DAC 302 includes a first group of switches SW11 to SW18, a second group of switches SW21 to SW27, a third group of switches SW30 to SW37, a fourth group of switches SW41 to SW47, and a fifth group of switches SW51 to SW57. The first group of switches SW11 to SW18 is arranged at each node of the first group of voltage dividing resistors R11 to R18. The first group of switches SW11 to SW18 supplies the voltage divided in the first group of voltage dividing resistors R11 to R18 to the output terminal (out).

5 [0062] In particular, an eleventh switch SW11 is arranged between a first node N1 and an output terminal (out) and supplies the second reference voltage (ref2) to the output terminal (out). A twelfth switch SW12 arranged between a second node N2 and the output terminal (out) supplies the voltage of the second node N2 to the output terminal (out). A thirteenth switch SW13 arranged between a third node N3 and the output terminal (out) supplies the voltage of the third node N3 to the output terminal (out). A fourteenth switch SW14 arranged between a fourth node N4 and the output terminal (out) supplies the voltage of the fourth node N4 to the output terminal (out). A fifteenth switch SW 15 arranged between a fifth node N5 and the output terminal (out) supplies the voltage of the fifth node N5 to the output terminal (out). A sixteenth switch SW16 arranged between a sixth node N6 and the output terminal (out) supplies the voltage of the sixth node N6 to the output terminal (out). A seventeenth switch SW17 arranged between a seventh node N7 and the output terminal (out) supplies a voltage of the seventh node N7 to the output terminal (out). An eighteenth switch SW18 arranged between an eighth node N8 and the output terminal (out) supplies the first reference voltage (ref1) to the output terminal (out).

10 [0063] The decoder unit 304 controls the turning on and the turning off of the first group of switches SW11 to SW 18 depending on the lower bits of the data.

15 In other words, the decoder unit 304 allows any one of the first group of switches SW11 to SW 18 to be turned on depending on the lower bits of the data, and the turned on switch may supply a predetermined voltage value to the output terminal (out). The voltage value supplied to the output terminal (out) is supplied to pixels 240 as a data signal. In another implementation, the data signal may be supplied to the pixels 240 via the buffer unit 228.

20 [0064] The second group of switches SW21 to SW27 is arranged between nodes of the first group of voltage dividing resistors R11 to R18 and corresponding nodes of the second group of voltage dividing resistors R21 to R28. The second group of switches SW21 to SW27 may be turned on simultaneously with the second switch SW2, in response to the first control signal CS1 supplied from the decoder unit 304. Nodes of the first group of voltage dividing resistors R11 to R18 and corresponding nodes of the second group of voltage dividing resistors R21 to R28 may be electrically connected by the respective switches of the second group of switches SW21 to SW27.

25 [0065] The third group of switches SW31 to SW37 is arranged between nodes of the second group of voltage dividing resistors R21 to R28 and corresponding nodes of the third group of voltage dividing resistors R31 to R38. The third group of switches SW31 to SW37 may be turned on simultaneously with the third switch SW3 in response to the second control signal CS2 supplied from the decoder unit 304. Nodes of the second group of voltage dividing resistors R21 to R28 and corresponding nodes of the third group of voltage dividing resistors R31 to R38 may be electrically connected by the respective switches of the third group of switches SW31 to SW37.

30 [0066] The fourth group of switches SW41 to SW47 is arranged between nodes of the third group of voltage dividing resistors R31 to R38 and corresponding nodes of the fourth group of voltage dividing resistors R41 to R48. The fourth group of switches SW41 to SW47 may be turned on simultaneously with the fourth switch SW4 in response to the third control signal CS3 supplied from the decoder unit 304. Nodes of the third group of voltage dividing resistors R31 to R38 and corresponding nodes of the fourth group of voltage dividing resistors R41 to R48 may be electrically connected by the respective switches of the fourth group of switches SW41 to SW47.

35 [0067] The fifth group of switches SW51 to SW57 is arranged between nodes of the fourth group of voltage dividing resistors R41 to R48 and corresponding nodes of the fifth group of voltage dividing resistors R51 to R58. The fifth group of switches SW51 to SW57 may be turned on simultaneously with the fifth switch SW5 in response to the fourth control signal CS4 supplied from the decoder unit 304. Nodes of the fourth group of voltage dividing resistors R41 to R48 and corresponding nodes of the fifth group of voltage dividing resistors R51 to R58 may be electrically connected by the respective switches of the fifth group of switches SW51 to SW57.

40 [0068] An operation of the second DAC 302 according to this embodiment of the present invention will be described in detail with reference to FIG. 6 and Table 1, below.

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Table 1

Data			Switches											
D2	D1	D0	SW11	SW12	SW13	SW14	SW15	SW16	SW17	SW18	SW2	SW3	SW4	SW5
0	0	0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
0	0	1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
0	1	0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
0	1	1	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
1	0	0	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON
1	0	1	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	OFF
1	1	0	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
1	1	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF

[0069] Table 1 illustrates a diagram of the on and off states of the switches controlled by the decoder unit 304. For the sake of discussion, the number of lower bits of data is 3. However, it will be appreciated that other numbers of lower bits may be used.

[0070] The decoder unit 304 turns on the eleventh switch SW11 when a lower 3 bits "000" is input. The second reference voltage (ref2) is supplied to the first node N 1 and output to the output terminal (out) via the eleventh switch SW11. The second reference voltage (ref2) is then supplied to the pixels 240 as the data signal. When the second reference voltage (ref2) is supplied to the output terminal (out), only the first group of voltage dividing resistors R11 to R18 is connected between the first line L1 and the second line L2. Thus, a high resistance may be set between the first line L1 and the second line L2. That is, when the second reference voltage (ref2) is output, the resistance value between the first line L1 and the second line L2 may be set high, thereby making it possible to prevent the generation of voltage drop, since a value of the constant current may be low and the resistance may be high.

[0071] When a lower 3 bits "100" is input (e.g., to output an intermediate gray scale voltage), the decoder unit 304 turns on the second switch SW2, the third switch SW3, the fourth switch SW4, the fifth switch SW5 and the fifteenth switch SW 15.

[0072] If the second switch SW2, the third switch SW3, the fourth switch SW4 and the fifth switch SW5 are turned on, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, the fourth group of voltage dividing resistors R41 to R48 and the fifth group of voltage dividing resistors R51 to R58 are connected to the first group of voltage dividing resistors R11 to R18 in parallel. Thus, when the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, the fourth group of voltage dividing resistors R41 to R48 and the fifth group of voltage dividing resistors R51 to R58 are connected to the first group of voltage dividing resistors R11 to R18 in parallel, the resistance value between the first line L1 and the second line L2 is set even lower compared to the resistance value when the lower 3 bits "000" are input and the second reference voltage (ref2) is output.

[0073] In detail, when the decoder unit 304 supplies the second control signal CS1 to the second switch SW2, the second group of switches SW21 to SW27 may be turned on simultaneously. Similarly, when the decoder unit 304 supplies the second control signal CS2, the third control signal CS3, and the fourth control signal CS4 to the third switch SW3, the fourth switch SW4, and the fifth switch SW5, respectively, the third group of switches SW31 to SW37, the fourth group of switches SW41 to SW47, and the fifth group of switches SW51 to SW57 may be turned on simultaneously. Thus, nodes between the corresponding first to fifth groups of voltage dividing resistors R11 to R18, R21 to R28, R31 to R38, R41 to R48, and R51 to 58 may be electrically connected.

[0074] Additionally, if the fifteenth switch SW15 is turned on, the voltage applied to the fifth node N5 is supplied to the output terminal (out) as a data signal. That is, when the lower 3 bits "100" are input, the intermediate gray scale voltage may be supplied to the output terminal (out). Accordingly, the resistance value between the first line L1 and the second line L2 may be set even lower than the resistance value when the second reference voltage (ref2) is output. Therefore, by lowering the resistance between the first line L 1 and the second line L2, the charging speed of the pixels 240 may be enhanced when an intermediate gray scale voltage is output as the data signal.

[0075] When expressing gray scale voltages corresponding to inputs "001," "010" and "011," between "000" to "100," the resistance value between the first line L1 and the second line L2 may be set correspondingly lower in sequence. Thus, the gray scale voltage may be supplied to the output terminal (out) by setting the resistance between the first line L1 and the second line L2 to a correspondingly lower value in sequence from the second reference voltage (ref2) to an intermediate gray scale voltage.

[0076] More particularly, when "001" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18 and the second group of voltage dividing resistors R21 to R28 can be connected in parallel, and the resistance value may be lower than when "000" is input. When "010" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, and the third group of voltage dividing resistors R31 to R38 may be connected in parallel, and the resistance value may be even lower than when "001" is input. Also, when "011" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, and the fourth group of voltage dividing resistors R41 to R48 may be connected in parallel, and the resistance value may be even lower than when "010" is input.

[0077] In the same manner, the decoder unit 304 supplies the gray scale voltage via the second DAC 304 by setting the resistance between the first line L1 and the second line L2 to be sequentially lowered from the first reference voltage (ref1) to an intermediate gray scale voltage.

[0078] That is, in a sequence similar to that just described, when "111" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18 and the second group of voltage dividing resistors R21 to R28 may be connected in parallel. When "110" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, and the third group of voltage dividing resistors R31 to R38 may be connected in parallel, and the resistance value may be lower than when "111" is input. Also, when "101" is input as the

lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, and the fourth group of voltage dividing resistors R41 to R48 may be connected in parallel, and the resistance value may be lower than when "110" is input.

[0079] FIG. 7 illustrates a circuit diagram of a second DAC according to a second embodiment of the present invention. In the following description, a detailed description of elements included in the second DAC 302' that are identical to those previously described in FIG. 6 will not be repeated.

[0080] Referring to FIG. 7, the first switch SW1 is arranged between the first group of voltage dividing resistors R11 to R18 and the second line L2. The second switch SW2 is arranged between the second group of voltage dividing resistors R21 to R28 and the second line L2. The third switch SW3 is arranged between the third group of voltage dividing resistors R31 to R38 and the second line L2. The fourth switch SW4 is arranged between the fourth group of voltage dividing resistors R41 to R48 and the second line L2. The fifth switch SW5 is arranged between the fifth group of voltage dividing resistors R51 to R58 and the second line L2.

[0081] Although the positions of the first to the fifth switches SW1 to SW5 may be changed, the driving process therein may be identical to the driving process of the first embodiment of the present invention, as illustrated in FIG. 6. Accordingly, a detailed description of the driving process will not be repeated.

[0082] As described above, a data driver, an organic light emitting display, and a method of driving the same according to the present invention may set the resistance value between the first line and the second line to be high when outputting the first reference voltage and the second reference voltage. Also, the resistance value between the first line and the second line may be low when outputting the intermediate gray scale voltage, which is between the first reference voltage and the second reference voltage. Thus, the present invention may enable charging of the intermediate gray scale voltage to the pixels within a short period of time, so as to enhance the driving ability. Additionally, the resistance value between the first line and the second line may be set correspondingly lower as the gray scale voltage to be output increasingly differs from the first reference voltage to an intermediate gray scale voltage, which may enable generation of the data signal without voltage drop. Also, the resistance value between the first line and the second line may be set correspondingly lower as the gray scale voltage to be output increasingly differs from the second reference voltage to the intermediate gray scale voltage, which may enable generation of the data signal without voltage drop.

[0083] Embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation.

Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A data driver, comprising:

a first digital-to-analog converter (300) configured to select first (ref1) and second (ref2) reference voltages from a plurality of reference voltages depending on upper bits of data and to supply the selected first (ref1) and second (ref2) reference voltages to a first line (L1) and a second line (L2), respectively;

a second digital-to-analog converter (302) having:

the first line (L1) and the second line (L2) configured to receive the first and the second reference voltages, respectively;

a first group of voltage dividing resistors (R11-R18) connected between the first line (L1) and the second line (L2) in series, the first group of voltage dividing resistors (R11-R18) configured to generate a plurality of gray scale voltages by dividing the first reference voltage and the second reference voltage; **characterised in that** the data driver further comprises

a voltage dividing resistor unit comprising a second group of voltage dividing resistors (R21-R28) connected between the first line (L1) and the second line (L2) in series, the voltage dividing resistor unit being connected in parallel with the first group of voltage dividing resistors (R11-R18); the voltage dividing resistor unit further comprising

a group of switches (SW21-SW27) arranged between nodes (N2-N8) of the first group of voltage dividing resistors (R11-R18) and corresponding nodes of the second group of voltage dividing resistors (R21-R28) in the voltage dividing resistor unit; and

a second switch (SW2) connected between the second group of voltage dividing resistors and one of the first line (L1) and the second line (L2), wherein the group of switches (SW21-SW27) arranged to be switched on simultaneously with the second switch (SW2); and

a decoder unit (304) configured to control on and off states of the second switch (SW2) depending on lower

bits of data.

2. A data driver as claimed in claim 1, wherein the decoder unit (304) is configured to control the on and off state of the second switch so that, when a gray scale voltage between the first reference voltage and the second reference voltage is output, a resistance value between the first line and the second line is set lower than a resistance value between the first line and the second line when either of the first reference voltage and the second reference voltage is output.
3. A data driver as claimed in claim 2, wherein the decoder unit (304) is configured to control the on and off state of the second switch so that the resistance value between the first line and the second line is correspondingly set lower as the gray scale voltage to be output increasingly differs from the first reference voltage to a predetermined gray scale voltage.
4. A data driver as claimed in claim 2, wherein the decoder unit (304) is configured to control the on and off state of the second switch so that the resistance value between first line and the second line is correspondingly set lower as the gray scale voltage to be output increasingly differs from the second reference voltage to a predetermined gray scale voltage.
5. A data driver as claimed in any preceding claim, further comprising a first group of switches (SW11-SW18) connected between nodes of the first group of voltage dividing resistors (R11-R18) and an output terminal, the first group of switches (SW11-SW18) being controlled by the decoder unit (304) and configured to supply a divided voltage to the output terminal.
6. A data driver as claimed in any preceding claim, wherein the voltage dividing resistor unit further comprises :
 - a third group of voltage dividing resistors (R31-R38),
 - a fourth group of voltage dividing resistors (R41-R48), and
 - a fifth group of voltage dividing resistors (R51-R58),
 - wherein the third, fourth and fifth groups of voltage dividing resistors are each connected between the first line and the second line in parallel with the second group of voltage dividing resistors (R21-R28).
7. A data driver as claimed in claim 6, wherein the voltage dividing resistor unit further comprises :
 - a third switch (SW3) connected between the third group of voltage dividing resistors (R31-R38) and one of the first line and the second line;
 - a fourth switch (SW4) connected between the fourth group of voltage dividing resistors (R41-R48) and one of the first line and the second line; and
 - a fifth switch (SW5) connected between the fifth group of voltage dividing resistors (R51-R58) and one of the first line and the second line.
8. A data driver as claimed in claim 7, wherein the voltage dividing resistor unit further comprises
 - a third group of switches (SW31-SW37) connected between nodes of the second group of voltage dividing resistors and corresponding nodes of the third group of voltage dividing resistors, the third group of switches (SW31-SW37) being configured to be turned on simultaneously with the third switch (SW3);
 - a fourth group of switches (SW41-SW47) connected between nodes of the third group of voltage dividing resistors (R31-R38) and corresponding nodes of the fourth group of voltage dividing resistors (R41-R48), the fourth group of switches (SW41-SW47) being configured to be turned on simultaneously with the fourth switch (SW4); and
 - a fifth group of switches (SW51-SW57) between nodes of the fourth group of voltage dividing resistors (R41-R46) and corresponding nodes of the fifth group of voltage dividing resistors (R51-R58), the fifth group of switches (SW51-SW57) being configured to be turned on simultaneously with the fifth switch (SW5).
9. A data driver as claimed in any one of claims 6 to 8, wherein the number of resistors included in each of the second group of voltage dividing resistors (R21-R28), the third group of voltage dividing resistors (R31-R38), the fourth group of voltage dividing resistors (R41-R48) and the fifth group of voltage dividing resistors (R51-R58) is identical to the number of resistors included in the first group of voltage dividing resistors (R11-R18).
10. A data driver as claimed in any preceding claim, further comprising:

a shift register unit (223) configured to supply sampling signals in sequence;
 a sampling latch unit (224) configured to store data in response to the sampling signals;
 a holding latch unit (225) configured to store data from the sampling latch unit (224); and
 a data signal generator (227) configured to receive data from the holding latch unit (225) and generate data
 signals,
 wherein each channel of the data signal generator (227) includes the first digital-to-analog converter (300) and
 the second digital-to-analog converter (302).

11. A data driver as claimed in claim 10, further comprising:

a level shifter (226) connected between the holding latch unit and the data signal generator (227), the level
 shifter (226) configured to increase a voltage level of the data; and
 a buffer unit (228) configured to receive data signals from the data signal generator (227).

12. An organic light emitting display, comprising:

a pixel unit including a plurality of pixels connected to scan lines and data lines;
 a scan driver (210) configured to drive the scan lines; and
 a data driver according to any one of claims 1 to 11 configured to drive the data lines.

13. A method of driving an organic light emitting display as claimed in claim 12, comprising **characterized in that**:

supplying first (ref1) and second (ref2) reference voltages of a plurality of reference voltages to a first line (L1)
 and a second (L2) line, respectively, depending on upper bits of data;
 dividing the first and the second reference voltages into a plurality of gray scale voltages by controlling a
 resistance value between the first line and the second line depending on lower bits of data, the method steps
 the dividing comprises:

using a first group of voltage dividing resistors (R11-R18) connected between the first line and the second
 line in series, using a voltage dividing resistor unit (R21-R58) comprising at least one group of voltage
 dividing resistors (R21-R28; R51-R58) connected, between the first line (L1) and the second line (L2) in
 series, the voltage dividing unit being connected in parallel with the first group of voltage dividing resistors
 (R11-R18), using at least one group of switches (SW21-SW27; SW51-SW57) arranged between nodes
 (N2-N8) of the first group of voltage dividing resistors (R11-R18) and corresponding nodes of the at least
 one group of voltage dividing resistors (R21-R28; R51-R58) in the voltage dividing resistor unit, using at
 least one second switch (SW2; SW5) connected between the voltage dividing resistor unit and one of the
 first line (L1) and the second line (L2), wherein the at least one group of switches (SW21-SW27; SW51-
 SW57) is arranged to be switched on simultaneously with the at least one second switch (SW2; SW5),
 wherein the first group of voltage dividing resistors (R11-R18) are configured to generate the plurality of
 gray scale voltages by dividing the first reference voltage (ref1) and the second reference voltage (ref2); and
 outputting a gray scale voltage.

14. A method as claimed in claim 13, wherein dividing comprises, when outputting a gray scale voltage that is between
 the first and the second reference voltages, setting the resistance value between the first line and the second line
 to be lower than the resistance value when outputting a gray scale voltage that is either of the first and the second
 reference voltages.

15. A method as claimed in claim 14, wherein the resistance value between the first line and the second line is corre-
 spondingly set lower as the gray scale voltage to be output increasingly differs from the first reference voltage to a
 predetermined gray scale voltage.

16. A method as claimed in claim 14, wherein the resistance value between the first line and the second line is corre-
 spondingly set lower as the gray scale voltage to be output increasingly differs from the second reference voltage
 to a predetermined gray scale voltage.

Patentansprüche

1. Datentreiber, Folgendes umfassend:

5 einen ersten D/A-Wandlez (300), der dazu konfiguriert ist, erste (ref1) und zweite (ref2) Referenzspannungen aus einer Vielzahl von Referenzspannungen in Abhängigkeit von oberen Bits von Daten auszuwählen und die ausgewählten ersten (ref1) und zweiten (ref2) Referenzspannungen an eine erste (L1) bzw. eine zweite (L2) Leitung anzulegen;

10 einen zweiten D/A-Wandler (302), der Folgendes aufweist:

die erste (L1) und die zweite Leitung (L2), die dazu konfiguriert sind, die ersten bzw. die zweiten Referenzspannungen zu empfangen;

15 eine erste Gruppe von Spannungsteilerwiderständen (R11-R18), die zwischen die erste (L1) und die zweite Leitung (L2) in Reihe geschaltet sind, wobei die erste Gruppe von Spannungsteilerwiderständen (R11-R18) dazu konfiguriert ist, eine Vielzahl von Grauskala-Spannungen durch Teilen der ersten Referenzspannung und der zweiten Referenzspannung zu generieren; **dadurch gekennzeichnet, dass** der Datentreiber außerdem umfasst:

20 eine Spannungsteiler-Widerstandseinheit, die eine zweite Gruppe von Spannungsteilerwiderständen (R21-R28) umfasst, die zwischen die erste Leitung (L1) und die zweite Leitung (L2) in Reihe geschaltet sind, wobei die Spannungsteiler-Widerstandseinheit mit der ersten Gruppe von Spannungsteilerwiderständen (R11-R18) parallel geschaltet ist; wobei die Spannungsteiler-Widerstandseinheit außerdem umfasst:

25 eine Gruppe von Schaltern (SW21-SW27), die zwischen den Knoten der ersten Gruppe von Spannungsteilerwiderständen (R11-R18) und entsprechenden Knoten der zweiten Gruppe von Spannungsteilerwiderständen (R21-R28) in der Spannungsteiler-Widerstandseinheit angeordnet sind; und

30 einen zweiten Schalter (SW2), der zwischen der zweiten Gruppe von Spannungsteilerwiderständen und einer der ersten Leitung (L1) und der zweiten Leitung (L2) angeordnet ist, worin die Gruppe von Schaltern (SW21-SW27) dazu angeordnet ist, gleichzeitig mit dem zweiten Schalter (SW2) eingeschaltet zu werden; und

eine Decodereinheit (304), die dazu konfiguriert ist, Ein- und Aus-Zustände des zweiten Schalters (SW2) in Abhängigkeit von unteren Bits von Daten zu steuern.

35 **2.** Datentreiber nach Anspruch 1, worin die Decodereinheit (304) dazu konfiguriert ist, den Ein- und Aus-Zustand des zweiten Schalters zu steuern, sodass, wenn eine Grauskala-Spannung zwischen der ersten Referenzspannung und der zweiten Referenzspannung ausgegeben wird, ein Widerstandswert zwischen der ersten Leitung und der zweiten Leitung niedriger eingestellt wird als ein Widerstandswert zwischen der ersten Leitung und der zweiten Leitung, wenn eine der ersten Referenzspannung und der zweiten Referenzspannung ausgegeben wird.

40 **3.** Datentreiber nach Anspruch 2, worin die Decodereinheit (304) dazu konfiguriert ist, den Ein- und Aus-Zustand des zweiten Schalters zu steuern, sodass der Widerstandswert zwischen der ersten Leitung und der zweiten Leitung entsprechend niedriger eingestellt wird, wenn die auszugebende Grauskala-Spannung mehr und mehr von der ersten Referenzspannung zu einer vorbestimmten Grauskala-Spannung abweicht.

45 **4.** Datentreiber nach Anspruch 2, worin die Decodereinheit (304) dazu konfiguriert ist, den Ein- und Aus-Zustand des zweiten Schalters zu steuern, sodass der Widerstandswert zwischen der ersten Leitung und der zweiten Leitung entsprechend niedriger eingestellt wird, wenn die auszugebende Grauskala-Spannung mehr und mehr von der zweiten Referenzspannung zu einer vorbestimmten Grauskala-Spannung abweicht.

50 **5.** Datentreiber nach einem vorhergehenden Anspruch, außerdem umfassend: eine erste Gruppe von Schaltern (SW11-SW18), die zwischen Knoten der ersten Gruppe von Spannungsteilerwiderständen (R11-R18) und einen Ausgangsanschluss geschaltet ist, wobei die erste Gruppe von Schaltern (SW11-SW18) durch die Decodereinheit (304) gesteuert wird und dazu konfiguriert ist, eine geteilte Spannung an den Ausgangsanschluss anzulegen.

55 **6.** Datentreiber nach einem vorhergehenden Anspruch, worin die Spannungsteiler-Widerstandseinheit außerdem umfasst:

eine dritte Gruppe von Spannungsteilerwiderständen (R31-R38),

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eine vierte Gruppe von Spannungsteilerwiderständen (R41-R48), und
eine fünfte Gruppe von Spannungsteilerwiderständen (R51-R58),
worin jede der dritten, vierten und fünften Gruppen von Spannungsteilerwiderständen zwischen die erste
Leitung und zweite Leitung parallel mit der zweiten Gruppe von Spannungsteilerwiderständen (R21-R28) ge-
schaltet ist.

7. Datentreiber nach Anspruch 6, worin die Spannungsteiler-Widerstandseinheit außerdem umfasst:

einen dritten Schalter (SW3), der zwischen die dritte Gruppe von Spannungsteilerwiderständen (R31-R38) und
eine der ersten Leitung und der zweiten Leitung geschaltet ist;
einen vierten Schalter (SW4), der zwischen die vierte Gruppe von Spannungsteilerwiderständen (R41-R48)
und eine der ersten Leitung und der zweiten Leitung geschaltet ist; und
einen fünften Schalter (SW5), der zwischen die fünfte Gruppe von Spannungsteilerwiderständen (R51-R58)
und eine der ersten Leitung und der zweiten Leitung geschaltet ist.

8. Datentreiber nach Anspruch 7, worin die Spannungsteiler-Widerstandseinheit außerdem umfasst:

eine dritte Gruppe von Schaltern (SW31-SW37), die zwischen Knoten der zweiten Gruppe von Spannungstei-
lerwiderständen und entsprechende Knoten der dritten Gruppe von Spannungsteilerwiderständen geschaltet
ist, wobei die dritte Gruppe von Schaltern (SW31-SW37) dazu konfiguriert ist, gleichzeitig mit dem dritten
Schalter (SW3) eingeschaltet zu werden;
eine vierte Gruppe von Schaltern (SW41-SW47), die zwischen Knoten der dritten Gruppe von Spannungstei-
lerwiderständen (R31-R38) und entsprechende Knoten der vierten Gruppe von Spannungsteilerwiderständen
(R41-R48) geschaltet ist, wobei die vierte Gruppe von Schaltern (SW41-SW47) dazu konfiguriert ist, gleichzeitig
mit dem vierten Schalter (SW4) eingeschaltet zu werden;
eine fünfte Gruppe von Schaltern (SW51-SW57), die zwischen Knoten der vierten Gruppe von Spannungstei-
lerwiderständen (R41-R48) und entsprechende Knoten der fünften Gruppe von Spannungsteilerwiderständen
(R51-R58) geschaltet ist, wobei die fünfte Gruppe von Schaltern (SW51-SW57) dazu konfiguriert ist, gleichzeitig
mit dem fünften Schalter (SW5) eingeschaltet zu werden.

9. Datentreiber nach einem der Ansprüche 6 bis 8, worin die Anzahl von Widerständen, die in jeder von Folgenden enthalten sind: der zweiten Gruppe von Spannungsteilerwiderständen (R21-R28), der dritten Gruppe von Span- nungsteilerwiderständen (R31-R38), der vierten Gruppe von Spannungsteilerwiderständen (R41-R48) und der fünf- ten Gruppe von Spannungsteilerwiderständen (R51-R58), mit der Anzahl von Widerständen identisch ist, die in der ersten Gruppe von Spannungsteilerwiderständen (R11-R18) enthalten sind.

10. Datentreiber nach einem vorhergehenden Anspruch, außerdem umfassend:

eine Schieberegisteereinheit (223), die dazu konfiguriert ist, Abtastsignale der Reihe nach bereitzustellen;
eine Abtast-Latcheinheit (224), die dazu konfiguriert ist, Daten als Reaktion auf die Abtastsignale zu speichern;
eine Halte-Latcheinheit (225), die dazu konfiguriert ist, Daten aus der Abtast-Latcheinheit (224) zu speichern; und
einen Datensignalgenerator (227), der dazu konfiguriert ist, Daten aus der Halte-Latcheinheit (225) zu empfan-
gen und Datensignale zu generieren,
worin jeder Kanal des Datensignalgenerators (227) den ersten D/A-Wandler (300) und den zweiten D/A-Wandler
(302) enthält.

11. Datentreiber nach Anspruch 10, außerdem umfassend;

einen Pegelschieber (226), der zwischen die Halte-Latcheinheit und den Datensignalgenerator (227) geschaltet
ist, wobei der Pegelschieber (226) dazu konfiguriert ist, einen Spannungspegel der Daten zu erhöhen; und
eine Puffereinheit (228), die dazu konfiguriert ist, Datensignale vom Datensignalgenerator (227) zu empfangen.

12. Organisches Leuchtemissionsdisplay, Folgendes umfassend:

eine Pixeleinheit, die eine Vielzahl von Pixeln enthält, die an Abtastleitungen und Datenleitungen angeschlossen
sind,
einen Abtasttreiber (210), der dazu konfiguriert ist, die Abtastleitungen anzusteuern; und
einen Datentreiber nach einem der Ansprüche 1 bis 11, der dazu konfiguriert ist, die Datenleitungen anzusteuern.

13. Verfahren zum Ansteuern eines organischen Leuchtemissionsdisplays nach Anspruch 12, **dadurch gekennzeichnet, dass** es Folgendes umfasst:

5 Anlegen von ersten (ref1) und zweiten (ref2) Referenzspannungen einer Vielzahl von Referenzspannungen an eine erste Leitung (L1) bzw. eine zweite Leitung (L2) in Abhängigkeit von oberen Bits der Daten;
Teilen der ersten und zweiten Referenzspannungen in eine Vielzahl von Grauskala-Spannungen durch Steuern eines Widerstandswerts zwischen der ersten Leitung und der zweiten Leitung in Abhängigkeit von unteren Bits der Daten, wobei das Teilen die folgenden Verfahrensschritte umfasst:

10 Verwenden einer ersten Gruppe von Spannungsteilerwiderständen (R11-R18), die zwischen die erste und die zweite Leitung in Reihe geschaltet sind, unter Verwendung einer Spannungsteiler-Widerstandseinheit (R21-R58), mindestens eine Gruppe von Spannungsteilerwiderständen (R11-R28; R51-R58) umfassend, die zwischen die erste Leitung (L1) und die zweite Leitung (L2) in Reihe geschaltet sind, wobei die Spannungsteilereinheit mit der ersten Gruppe von Spannungsteilerwiderständen (R11-R18) parallel geschaltet
15 ist, unter Verwendung von mindestens einer Gruppe von Schaltern (SW21-SW27; SW51-SW57), die zwischen Knoten (N2-N8) der ersten Gruppe von Spannungsteilerwiderständen (R11-R18) und entsprechende Knoten der mindestens einen Gruppe von Spannungsteilerwiderständen (R11-R28; R51-R58) in der Spannungsteiler-Widerstandseinheit angeordnet sind, unter Verwendung von mindestens einem zweiten Schalter (SW2; SW5), der zwischen die Spannungsteiler-Widerstandseinheit und eine der ersten Leitung (L1) und der zweiten Leitung (L2) geschaltet ist, worin die mindestens eine Gruppe von Schaltern (SW21-SW27; SW51-SW57) dazu angeordnet ist, gleichzeitig mit dem mindestens einen zweiten Schalter (SW2; SW5) eingeschaltet zu werden, worin die erste Gruppe von Spannungsteilerwiderständen (R11-R18) dazu konfiguriert ist, die Vielzahl von Grauskala-Spannungen durch Teilen der ersten Referenzspannung (ref1) und der zweiten Referenzspannung (ref2) zu generieren; und
20 Ausgeben einer Grauskala-Spannung.

14. Verfahren nach Anspruch 13, worin das Teilen Folgendes umfasst: wenn eine Grauskala-Spannung ausgegeben wird, die zwischen den ersten und den zweiten Referenzspannungen besteht, wird der Widerstandswert zwischen der ersten Leitung und der zweiten Leitung niedriger eingestellt als der Widerstandswert, wenn eine Grauskala-Spannung ausgegeben wird, die eine der ersten und der zweiten Referenzspannungen ist.

15. Verfahren nach Anspruch 14, worin der Widerstandswert zwischen der ersten Leitung und der zweiten Leitung entsprechend niedriger eingestellt wird, wenn die auszugebende Grauskala-Spannung mehr und mehr von der ersten Referenzspannung zu einer vorbestimmten Grauskala-Spannung abweicht.

16. Verfahren nach Anspruch 14, worin der Widerstandswert zwischen der ersten Leitung und der zweiten Leitung entsprechend niedriger eingestellt wird, wenn die auszugebende Grauskala-Spannung mehr und mehr von der zweiten Referenzspannung zu einer vorbestimmten Grauskala-Spannung abweicht.

Revendications

1. Dispositif de pilotage de données, comportant:

45 un premier convertisseur numérique-analogique (300) configuré de manière à sélectionner des première (ref1) et seconde (ref2) tensions de référence à partir d'une pluralité de tensions de référence, en fonction de bits de données supérieurs, et à fournir les première (ref1) et seconde (ref2) tensions de référence sélectionnées à une première ligne (L1) et à une seconde ligne (L2), respectivement;
un second convertisseur numérique-analogique (302) présentant:

50 la première ligne (L1) et la seconde ligne (L2) configurées de manière à recevoir les première et seconde tensions de référence, respectivement;

un premier groupe de résistances diviseuses de tension (R11-R18) connectées entre la première ligne (L1) et la seconde ligne (L2) en série, le premier groupe de résistances diviseuses de tension (R11-R18) étant configuré de manière à générer une pluralité de tensions d'échelle des gris en divisant la première tension de référence et la seconde tension de référence;

caractérisé en ce que le dispositif de pilotage de données comporte en outre:

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une unité de résistances diviseuses de tension comportant un second groupe de résistances diviseuses de tension (R21-R28) connectées entre la première ligne (L1) et la seconde ligne (L2) en série;
l'unité de résistances diviseuses de tension étant connectée en parallèle avec le premier groupe de résistances diviseuses de tension (R11-R18); l'unité de résistances diviseuses de tension comportant en outre:

5 un groupe de commutateurs (SW21-SW27) agencés entre des noeuds (N2-N8) du premier groupe de résistances diviseuses de tension (R11-R18) et des noeuds correspondants du second groupe de résistances diviseuses de tension (R21-R28) dans l'unité de résistances diviseuses de tension; et
10 un deuxième commutateur (SW2) connecté entre le second groupe de résistances diviseuses de tension et l'une parmi la première ligne (L1) et la seconde ligne (L2), dans lequel le groupe de commutateurs (SW21-SW27) est agencé de manière à être mis sous tension simultanément avec le deuxième commutateur (SW2); et
15 une unité de décodeur (304) configurée de manière à commander des états de mise sous tension et de mise hors tension du deuxième commutateur (SW2), en fonction de bits de données inférieurs.

2. Dispositif de pilotage de données selon la revendication 1, dans lequel l'unité de décodeur (304) est configurée de manière à commander l'état de mise sous tension et de mise hors tension du deuxième commutateur de sorte que, lorsqu'une tension d'échelle des gris entre la première tension de référence et la seconde tension de référence est générée en sortie, une valeur de résistance entre la première ligne et la seconde ligne est définie sur une valeur inférieure à une valeur de résistance entre la première ligne et la seconde ligne lorsque l'une quelconque parmi la première tension de référence et la seconde tension de référence est générée en sortie.

3. Dispositif de pilotage de données selon la revendication 2, dans lequel l'unité de décodeur (304) est configurée de manière à commander l'état de mise sous tension et de mise hors tension du deuxième commutateur, de sorte que la valeur de résistance entre la première ligne et la seconde ligne est définie de manière correspondante sur une valeur inférieure à mesure que la tension d'échelle des gris destinée à être générée en sortie diffère de manière croissante de la première tension de référence, d'une tension d'échelle des gris prédéterminée.

4. Dispositif de pilotage de données selon la revendication 2, dans lequel l'unité de décodeur (304) est configurée de manière à commander l'état de mise sous tension et de mise hors tension du deuxième commutateur de sorte que la valeur de résistance entre la première ligne et la seconde ligne est définie de manière correspondante sur une valeur inférieure à mesure que la tension d'échelle des gris destinée à être générée en sortie diffère de manière croissante de la seconde tension de référence, d'une tension d'échelle des gris prédéterminée.

5. Dispositif de pilotage de données selon l'une quelconque des revendications précédentes, comportant en outre un premier groupe de commutateurs (SW11-SW18) connectés entre des noeuds du premier groupe de résistances diviseuses de tension (R11-R18) et une borne de sortie, le premier groupe de commutateurs (SW11-SW18) étant commandé par l'unité de décodeur (304) et étant configuré de manière à fournir une tension divisée à la borne de sortie.

6. Dispositif de pilotage de données selon l'une quelconque des revendications précédentes, dans lequel l'unité de résistances diviseuses de tension comporte:

45 un troisième groupe de résistances diviseuses de tension (R31-R38);
un quatrième groupe de résistances diviseuses de tension (R41-R48); et
un cinquième groupe de résistances diviseuses de tension (R51-R58);
dans lequel les troisième, quatrième et cinquième groupes de résistances diviseuses de tension sont chacun connectés entre la première ligne et la seconde ligne en parallèle avec le second groupe de résistances diviseuses de tension (R21-R28).

7. Dispositif de pilotage de données selon la revendication 6, dans lequel l'unité de résistances diviseuses de tension comporte en outre:

55 un troisième commutateur (SW3) connecté entre le troisième groupe de résistances diviseuses de tension (R31-R38) et l'une de la première ligne et de la seconde ligne;
un quatrième commutateur (SW4) connecté entre le quatrième groupe de résistances diviseuses de tension (R41-R48) et l'une de la première ligne et de la seconde ligne; et
un cinquième commutateur (SW5) connecté entre le cinquième groupe de résistances diviseuses de tension

(R51-R58) et l'une de la première ligne et de la seconde ligne.

8. Dispositif de pilotage de données selon la revendication 7, dans lequel l'unité de résistances diviseuses de tension comporte en outre:

5 un troisième groupe de commutateurs (SW31-SW37) connectés entre des noeuds du deuxième groupe de résistances diviseuses de tension et des noeuds correspondants du troisième groupe de résistances diviseuses de tension, le troisième groupe de commutateurs (SW31-SW37) étant configuré de manière à être mis sous tension simultanément avec le troisième commutateur (SW3);
10 un quatrième groupe de commutateurs (SW41-SW47) connectés entre des noeuds du troisième groupe de résistances diviseuses de tension (R31-R38) et des noeuds correspondants du quatrième groupe de résistances diviseuses de tension (R41-R48), le quatrième groupe de commutateurs (SW41-SW47) étant configuré de manière à être mis sous tension simultanément avec le quatrième commutateur (SW4); et
15 un cinquième groupe de commutateurs (SW51-SW57) connectés entre des noeuds du quatrième groupe de résistances diviseuses de tension (R41-R46) et des noeuds correspondants du cinquième groupe de résistances diviseuses de tension (R51-R58), le cinquième groupe de commutateurs (SW51-SW57) étant configuré de manière à être mis sous tension simultanément avec le cinquième commutateur (SW5).

9. Dispositif de pilotage de données selon l'une quelconque des revendications 6 à 8, dans lequel le nombre de résistances incluses dans chacun parmi le deuxième groupe de résistances diviseuses de tension (R21-R28), le troisième groupe de résistances diviseuses de tension (R31-R38), le quatrième groupe de résistances diviseuses de tension (R41-R48) et le cinquième groupe de résistances diviseuses de tension (R51-R58) est identique au nombre de résistances incluses dans le premier groupe de résistances diviseuses de tension (R11-R18).

- 25 10. Dispositif de pilotage de données selon l'une quelconque des revendications précédentes, comportant en outre:

une unité de registre à décalage (223) configurée de manière à délivrer des signaux d'échantillonnage en séquence;
une unité de verrouillage d'échantillonnage (224) configurée de manière à stocker des données en réponse
30 aux signaux d'échantillonnage;
une unité de verrouillage de conservation (225) configurée de manière à stocker des données en provenance de l'unité de verrouillage d'échantillonnage (224); et
un générateur de signaux de données (227) configuré de manière à recevoir des données en provenance de l'unité de verrouillage de conservation (225) et à générer des signaux de données;
35 dans lequel chaque canal du générateur de signaux de données (227) comporte le premier convertisseur numérique-analogique (300) et le second convertisseur numérique-analogique (302).

11. Dispositif de pilotage de données selon la revendication 10, comportant en outre:

40 un module de rétablissement de niveau (226) connecté entre l'unité de verrouillage de conservation et le générateur de signaux de données (227), le module de rétablissement de niveau (226) étant configuré de manière à augmenter un niveau de tension des données; et
une unité de mise en mémoire tampon (228) configurée de manière à recevoir des signaux de données en provenance du générateur de signaux de données (227).

- 45 12. Écran à diodes électroluminescentes organiques, comportant:

une unité de pixels incluant une pluralité de pixels connectés à des lignes de balayage et des lignes de données;
un dispositif de pilotage de balayage (210) configuré de manière à commander les lignes de balayage; et
50 un dispositif de pilotage de données selon l'une quelconque des revendications 1 à 11 configuré de manière à commander les lignes de données.

13. Procédé de commande d'un écran à diodes électroluminescentes organiques selon la revendication 12, comportant les étapes ci-après consistant à:

55 fournir des première (ref1) et seconde (ref2) tensions de référence d'une pluralité de tensions de référence à une première ligne (L1) et une seconde ligne (L2), respectivement, en fonction de bits de données supérieurs; diviser les première et seconde tensions de référence en une pluralité de tensions d'échelle des gris en com-

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mandant une valeur de résistance entre la première ligne et la seconde ligne en fonction de bits de données inférieurs; et **caractérisé en ce que** l'étape de division comporte les étapes de procédé ci-dessous consistant à:

5 utiliser un premier groupe de résistances diviseuses de tension (R11-R18) connectées entre la première ligne et la seconde ligne en série, en utilisant une unité de résistances diviseuses de tension (R21-R58) comportant au moins un groupe de résistances diviseuses de tension (R21-R28; R51-R58) connectées entre la première ligne (L1) et la seconde ligne (L2) en série, l'unité de résistances diviseuses de tension étant connectée en parallèle avec le premier groupe de résistances diviseuses de tension (R11-R18), en utilisant au moins un groupe de commutateurs (SW21-SW27; SW51-SW57) agencés entre des noeuds (N2-N8) du premier groupe de résistances diviseuses de tension (R11-R18) et des noeuds correspondants dudit au moins un groupe de résistances diviseuses de tension (R21-R28; R51-R58) dans l'unité de résistances diviseuses de tension, en utilisant au moins un deuxième commutateur (SW2; SW5) connecté entre l'unité de résistances diviseuses de tension et l'une parmi la première ligne (L1) et la seconde ligne (L2), dans lequel ledit au moins un groupe de commutateurs (SW21-SW27; SW51-SW57) est agencé de manière à être mis sous tension simultanément avec ledit au moins un deuxième commutateur (SW2; SW5); dans lequel le premier groupe de résistances diviseuses de tension (R21-R28) est configuré de manière à générer la pluralité de tensions d'échelle des gris en divisant la première tension de référence (ref1) et la seconde tension de référence (ref2); et
20 générer en sortie une tension d'échelle des gris.

14. Procédé selon la revendication 13, dans lequel l'étape de division comporte l'étape consistant à, lors de la génération en sortie d'une tension d'échelle des gris qui se situe entre les première et seconde tensions de référence, définir la valeur de résistance entre la première ligne et la seconde ligne afin qu'elle soit inférieure à la valeur de résistance lors de la génération en sortie d'une tension d'échelle des gris provenant de l'une des première et seconde tensions de référence.

15. Procédé selon la revendication 14, dans lequel la valeur de résistance entre la première ligne et la seconde ligne est définie de manière correspondante sur une valeur inférieure à mesure que la tension d'échelle des gris destinée à être générée en sortie diffère de manière croissante de la première tension de référence d'une tension d'échelle des gris prédéterminée.

16. Procédé selon la revendication 14, dans lequel la valeur de résistance entre la première ligne et la seconde ligne est définie de manière correspondante sur une valeur inférieure à mesure que la tension d'échelle des gris destinée à être générée en sortie diffère de manière croissante de la seconde tension de référence d'une tension d'échelle des gris prédéterminée.

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FIG. 1
(RELATED ART)

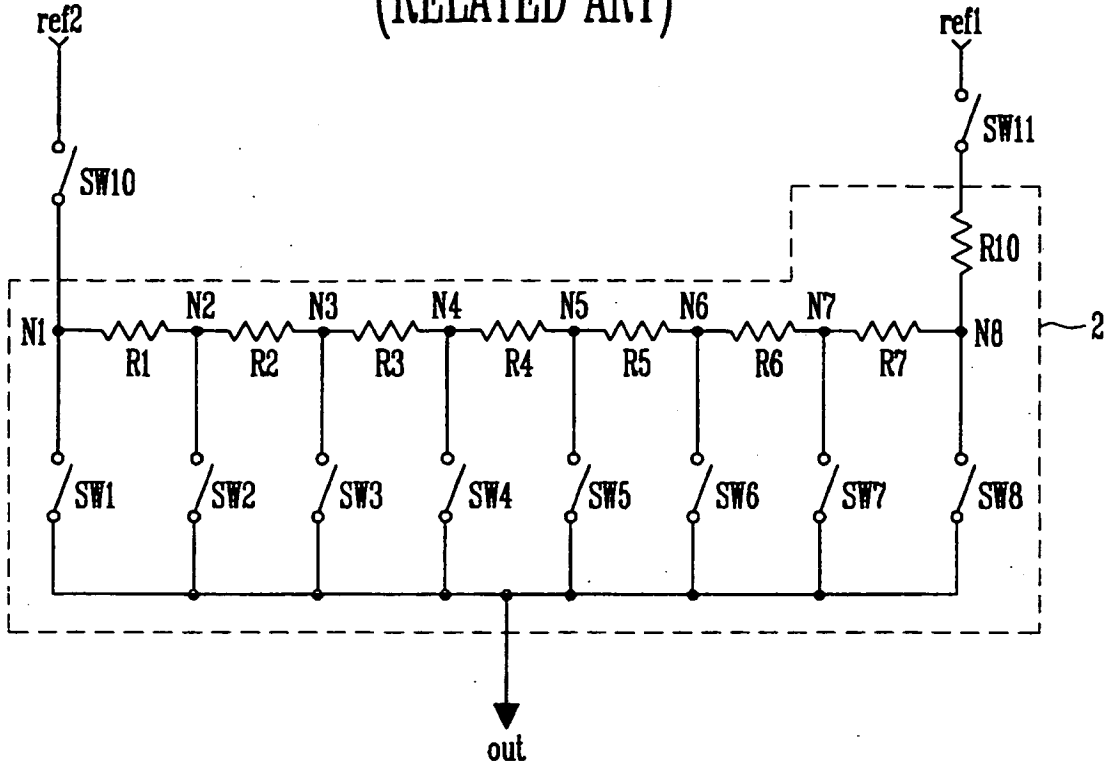


FIG. 2
(RELATED ART)

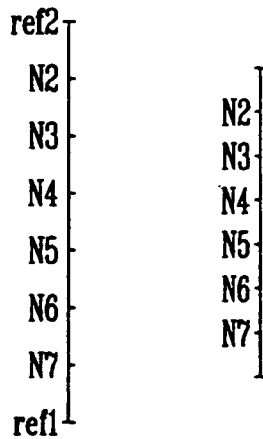


FIG. 3

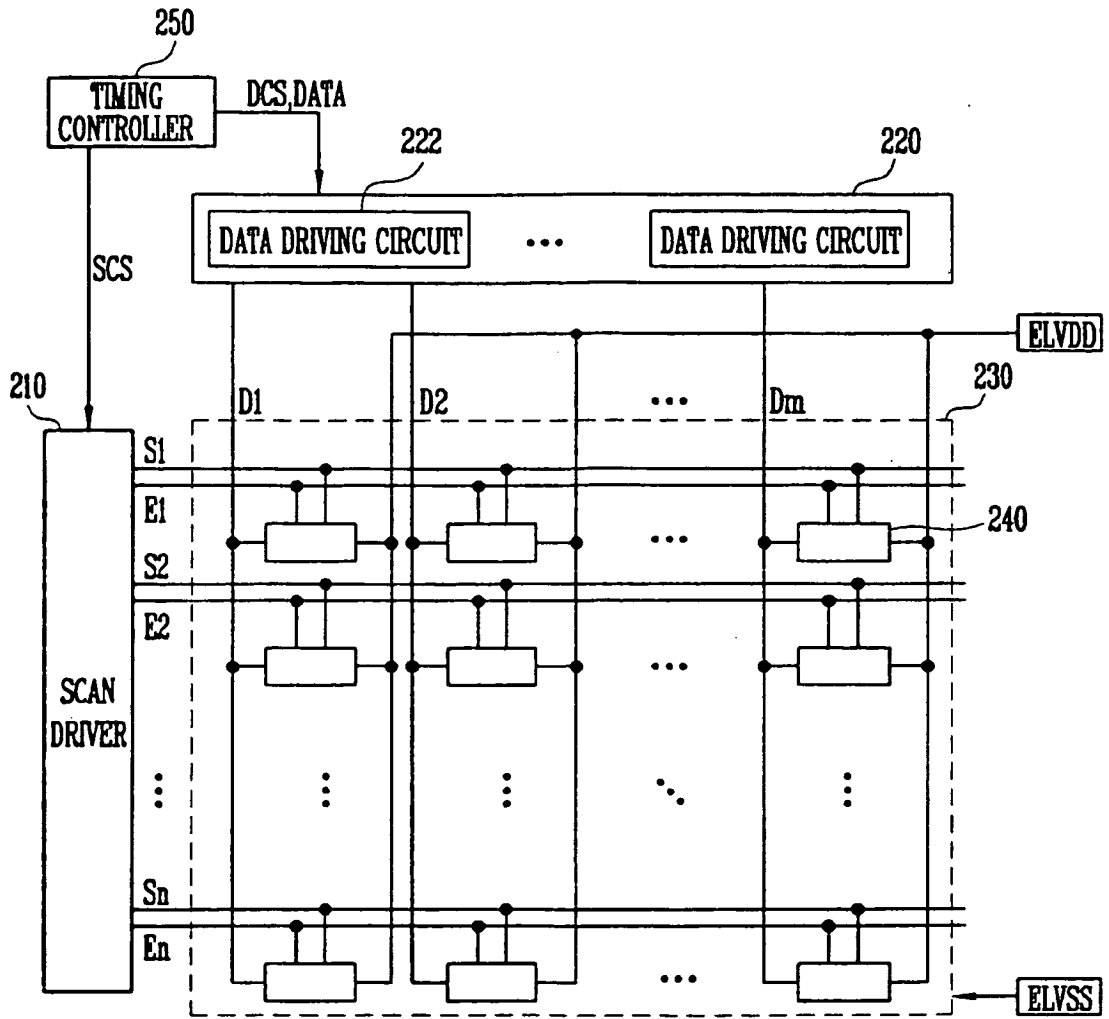


FIG. 4A

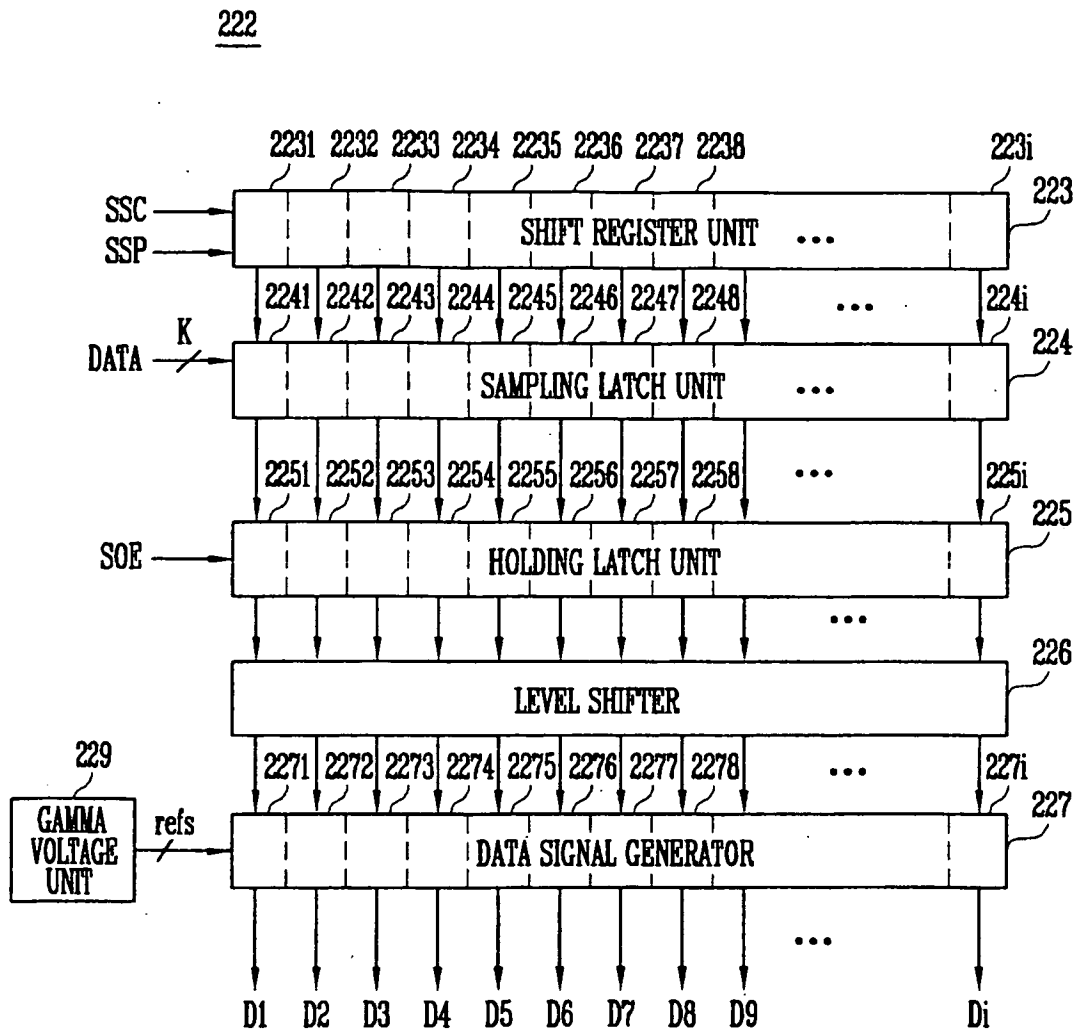


FIG. 4B

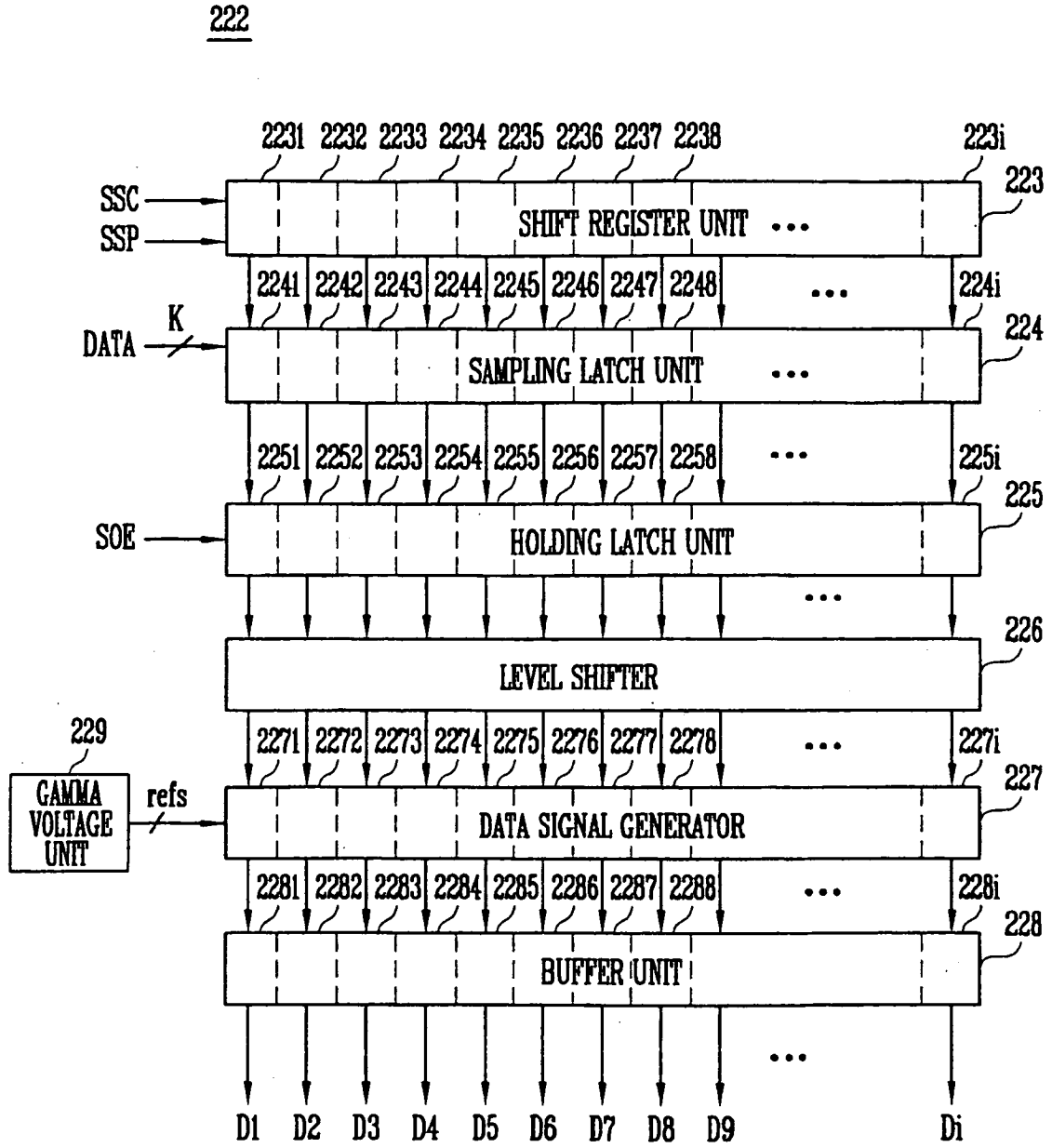


FIG. 5

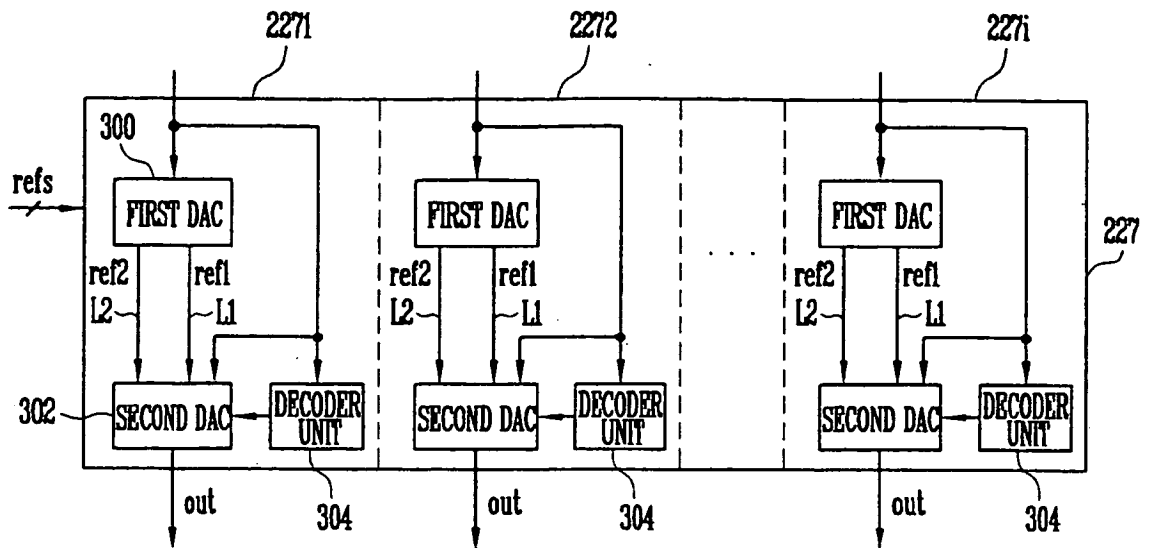
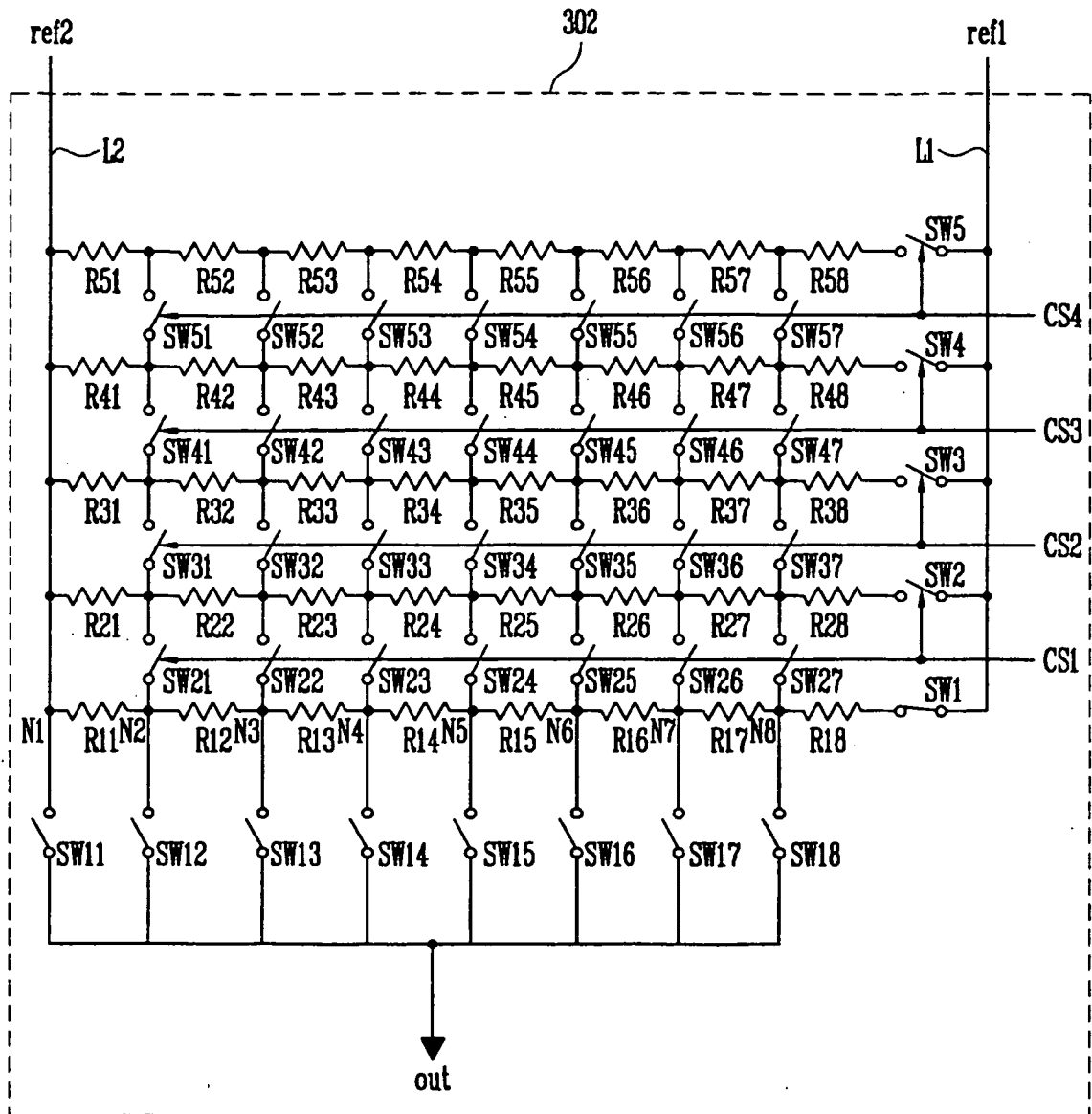


FIG. 6



REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	数据驱动器，有机发光显示器及其驱动方法		
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优先权	1020050127233 2005-12-21 KR		
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外部链接	Espacenet		

摘要(译)

一种数据驱动器，包括：第一数模转换器，被配置为根据数据的高位选择第一和第二参考电压，并将第一和第二参考电压分别提供给第一线和第二线，第二数字-模拟转换器，具有第一线和第二线，分别接收第一和第二参考电压，第一组分压电阻，位于第一线和第二线之间，用于产生多个灰阶电压，第一线和第二线之间的分压电阻器单元，以及位于分压电阻器单元和第一线和第二线之一之间的至少一个开关，并且包括解码器单元，该解码器单元被配置为控制接通和断开状态。至少一个开关取决于较低的数据位。

