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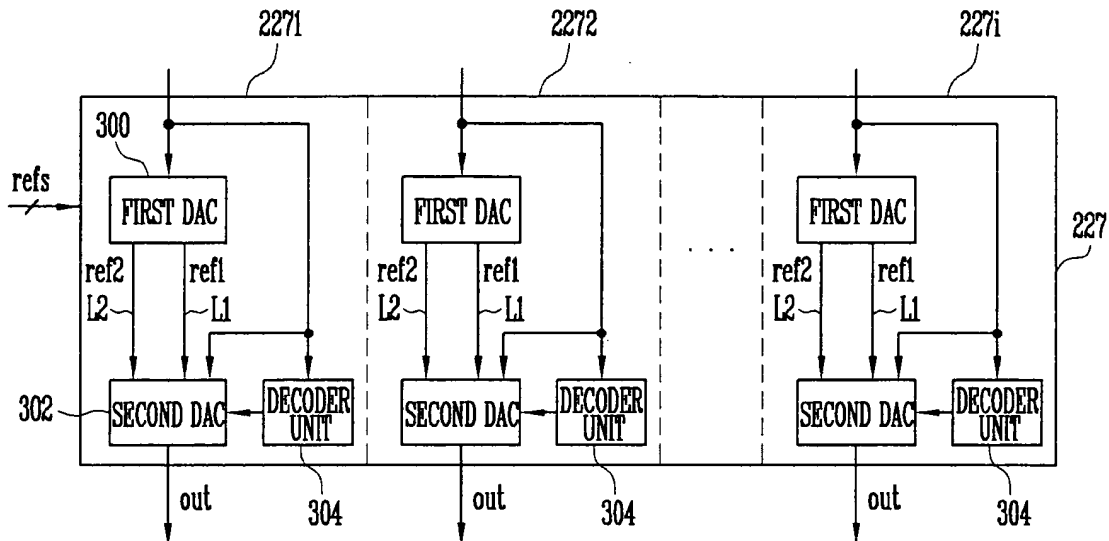
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(54) **Data driver, organic light emitting display, and method of driving the same**

(57) A data driver including a first digital-to-analog converter configured to select first and second reference voltages depending on upper bits of data and supply the first and the second reference voltages to a first line and a second line, respectively, a second digital-to-analog converter having the first line and the second line to receive the first and the second reference voltages, respectively, a first group of voltage dividing resistors between

the first line and the second line and configured to generate a plurality of gray scale voltages, a voltage dividing resistor unit between the first line and the second line, and at least one switch positioned between the voltage dividing resistor unit and one of the first line and the second line, and including a decoder unit configured to control on and off state of the at least one switch depending on lower bits of data.

FIG. 5



Description**BACKGROUND OF THE INVENTION**5 **1. Field of the Invention**

[0001] The present invention relates to a data driver, an organic light emitting display, and a method of driving the same. More particularly, the present invention relates to a data driver for enhancing image quality, an organic light emitting display, and a method of driving the same.

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2. Description of the Related Art

[0002] Various flat panel display devices having reduced weight and volume compared to comparable cathode ray tubes (CRTs) have been developed. These flat panel display devices include for example, a liquid crystal display, a field emission display, a plasma display panel, an organic light emitting display, etc. These exemplary displays may operate differently to display an image.

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[0003] For example, an organic light emitting display displays an image by using an organic light emitting diode that generates light by recombining electrons and holes. During operation, such an organic light emitting display supplies a current corresponding to a data signal to organic light emitting diodes by employing driving, thin film transistors formed at each pixel so light may be emitted from the organic light emitting diodes. Such an organic light emitting display may offer certain advantages, since it may be operated with low power consumption and may provide a rapid response speed.

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[0004] An organic light emitting display may generate data signals by using data supplied from an external source. The organic light emitting display supplies the generated data signals to pixels and display an image of desired brightness. A data driver for converting the data supplied from the external source into the data signals has been considered.

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[0005] Such a data driver may include a data signal generator for converting the external data into the data signals. The data signal generator may include a digital-to-analog converter (hereinafter, referred to as "DAC"). The DAC is positioned in each channel and converts the data into the data signals. For example, the data signal generator may include first DACs for generating voltages depending on the values of the upper bits of the data and second DACs for generating voltages depending on the values of the lower bits of the data.

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[0006] FIG. 1 illustrates a circuit diagram of a second DAC. Referring to FIG. 1, the second DAC 2 receives a first reference voltage (ref1) and a second reference voltage (ref2) from a first DAC (not illustrated). The first DAC receives a plurality of reference voltages from an external source. The first DAC selects the first reference voltage (ref1) and the second reference voltage (ref2) among the plurality of reference voltages received depending on a value of the upper bits of the data. The first DAC supplies the selected first and second reference voltages (ref1) and (ref2) to the second DAC 2 via a tenth switch SW 10 and an eleventh switch SW11, as illustrated in FIG. 1. That is, the tenth switch SW10 or the eleventh switch SW11 included in the first DAC may be turned on depending on the value of the upper bits of the data. For the sake of discussion, the present invention will be described assuming that the first reference voltage (ref1) is lower than the second reference voltage (ref2).

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[0007] The second DAC 2 includes a plurality of voltage dividing resistors R1 to R7 for dividing the voltage values of the first reference voltage (ref1) and the second reference voltage (ref2). The second DAC2 also includes a plurality of switches SW1 to SW8 for supplying voltages divided from the voltage dividing resistors R1 to R7 to an output terminal (out).

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[0008] A tenth resistor R10 is arranged between the eleventh switch SW11 and the seventh resistor R7. The tenth resistor R10 compensates for the switch resistances of the tenth switch SW 10 and the eleventh switch SW11 so that the second DAC may evenly divide the reference voltages via the voltage dividing resistors R1 to R7.

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[0009] The voltage dividing resistors R1 to R7 are arranged in series. The voltage dividing resistors R1 to R7 evenly divide the first reference voltage (ref1) and the second reference voltage (ref2). In this regard, the resistance value of each of the voltage dividing resistors R1 to R7 may be identical.

[0010] The switches SW1 to SW8 are arranged to supply the voltages divided by the voltage dividing resistors R1 to R7 to the output terminal (out). In particular, the first switch SW 1 is arranged between a first node N1 and the output terminal (out) to supply the second reference voltage (ref2) to the output terminal (out). The second switch SW2 is arranged between a second node N2 and the output terminal (out) to supply the voltage value of the second node N2 to the output terminal (out). The third switch SW3 is arranged between a third node N3 and the output terminal (out) to supply the voltage value of the third node N3 to the output terminal (out). The fourth switch SW4 is arranged between a fourth node N4 and the output terminal (out) to supply the voltage value of the fourth node N4 to the output terminal (out). The fifth switch SW5 is arranged between a fifth node N5 and the output terminal (out) to supply the voltage value of the fifth node N5 to the output terminal (out). The sixth switch SW6 is arranged between a sixth node N6 and the output terminal (out) to supply the voltage value of the sixth node N6 to the output terminal (out). The seventh switch SW7 is arranged between a seventh node N7 and the output terminal (out) to supply the voltage value of the seventh

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node N7 to the output terminal (out). The eighth switch SW8 is arranged between an eighth node N8 and the output terminal (out) to supply the first reference voltage (ref1) to the output terminal (out).

[0011] During operation, one of the switches SW1 to SW8 may be turned on depending on the value of the lower bits of the data, and a predetermined voltage is supplied to the output terminal (out). The predetermined voltage value supplied to the output terminal (out) is supplied to pixels as a data signal.

[0012] The conventional second DAC 2 may exhibit a deterioration of its driving ability when supplying a gray scale voltage, such as an intermediate gray scale voltage (e.g., voltages of node N4 or node N5) as a data signal. In other words, since the intermediate gray scale voltage is supplied to the output terminal (out) via a plurality of resistors, a period of time is required before intermediate gray scale voltages corresponding to the data signals may be supplied to the pixels. For example, some intermediate gray scale voltages (e.g., voltages of node N1, node N2, node N6 and node N7) adjacent to the first reference voltage (ref1) and the second reference voltage (ref2) may be supplied and charged in the pixels within a shorter period of time than other intermediate gray scale voltages (e.g., voltages of node N4 or node N5).

[0013] In order to resolve this deficiency, it has been proposed to lower the resistance values of the voltage dividing resistors R1 to R7 between the first reference voltage ref1 and the second reference voltage ref2. It may be understood that if the resistance value between the first reference voltage (ref1) and the second reference voltage (ref2) is lowered, the driving ability of the intermediate gray scale may be enhanced. That is, it may be possible to supply and charge the pixels with a predetermined voltage within a predetermined time period. However, if the resistance value between the first reference voltage (ref1) and the second reference voltage (ref2) is lowered, the value of constant current flowing into the voltage dividing resistors R1 to R7 increases. This increase in the value of constant current flowing may generate a phenomenon known as voltage drop. If voltage drop is generated, the voltage values of the intermediate gray scale voltages adjacent to the first reference voltage (ref1) and the second reference voltage (ref2) may be altered, as illustrated in FIG. 2. Thus, the predetermined voltage may not be supplied and charged in the pixels. The voltage values of the intermediate gray scale voltages more centered between the first reference voltage (ref1) and the second reference voltage (ref2) may maintain approximately similar values, regardless of the voltage drop.

[0014] As discussed above, a conventional organic light emitting display may operate with certain deficiencies. That is, if the resistance values of the voltage dividing resistors R1 to R7 between the first reference voltage (ref1) and the second reference voltage (ref2) are large, the driving ability of the intermediate gray scale may be deteriorated, and if the resistance values of the voltage dividing resistors R1 to R7 are small, the gray scale voltage values adjacent to the first reference voltage (ref1) and the second reference voltage (ref2) may be altered.

SUMMARY OF THE INVENTION

[0015] The present invention is therefore directed to a data driver, an organic light emitting display, and a method of driving the same that sets out to overcome one or more of the problems due to the limitations and disadvantages of the related art.

[0016] It is therefore a feature of an embodiment of the present invention to provide a data driver and an organic light emitting display that includes a second DAC configured to enhance image quality.

[0017] It is therefore another feature of an embodiment of the present invention to provide a data driver and an organic light emitting display that includes a second DAC configured to enhance the driving ability of a data driver.

[0018] It is therefore another feature of an embodiment of the present invention to provide a data driver and an organic light emitting display that includes a second DAC that reduces the occurrence of voltage drop.

[0019] According to a first aspect of the invention, there is provided a data driver as set out in claim 1. Preferred features are set out in claims 2 to 11.

[0020] According to a second aspect of the invention, there is provided an organic light emitting display as set out in claim 12.

[0021] According to a third aspect of the invention, there is provided a method of driving an organic light emitting display as set out in claim 13. Preferred features are set out in claims 14 to 16.

[0022] BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing in detail embodiments thereof with reference to the attached drawings, in which:

[0024] FIG. 1 illustrates a circuit diagram of a conventional second DAC;

[0025] FIG. 2 illustrates a diagram of an alteration of gray scale voltage levels due to voltage drop;

[0026] FIG. 3 illustrates a block circuit diagram of an organic light emitting display according to an embodiment of the present invention;

[0027] FIGS. 4A and FIG. 4B illustrate block circuit diagrams of an embodiment of the data driving circuit illustrated in FIG. 3;

[0028] FIG. 5 illustrates a block circuit diagram of an embodiment of the data signal generator illustrated in FIGS. 4A

and 4B;

[0029] FIG. 6 illustrates a circuit diagram of a second DAC according to a first embodiment of the present invention; and

[0030] FIG. 7 illustrates a circuit diagram of a second DAC according to a second embodiment of the present invention.

5 DETAILED DESCRIPTION OF THE INVENTION

[0031] Korean Patent Application No. 10-2005-0127233, filed on December 21, 2005, in the Korean Intellectual Property Office, and entitled: "Data Driver and Driving Method of Organic Light Emitting Display Using the Same," is incorporated by reference herein in its entirety.

10 **[0032]** The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are illustrated. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

15 **[0033]** Hereinafter, embodiments according to the present invention will be described with reference to the accompanying FIGS. 3 to 7.

[0034] FIG. 3 illustrates a block circuit diagram of an organic light emitting display according to an embodiment of the present invention. Referring to FIG. 3, the organic light emitting display includes a pixel unit 230 including pixels 240 formed on a region where scan lines S 1 to Sn are intersected with data lines D 1 to Dm, a scan driver 210 for driving scan lines S 1 to Sn, a data driver 220 for driving data lines D1 to Dm, and a timing controller 250 for controlling the scan driver 210 and the data driver 220. The data driver 220 includes at least one data driving circuit 222.

20 **[0035]** The scan driver 210 generates scan signals in response to scan driving control signals SCS from the timing controller 250. The scan driver 210 may supply the generated scan signals to the scan lines S1 to Sn in sequence. The scan driver 210 generates light emitting control signals in response to the scan driving control signals SCS. The scan driver may supply the generated light emitting control signals to light emitting control lines E1 to En in sequence.

25 **[0036]** The data driver 220 generates data signals in response to data driving control signals DCS from the timing controller 250. The data driver 220 may supply the generated data signals to the data lines D1 to Dm in sequence. The data driving circuit 222 converts data supplied from an external source into data signals and supplies the data signals to the data lines D 1 to Dm. The data driving circuit 222 will be described in more detail below.

30 **[0037]** The timing controller 250 generates a data driving control signal DCS and a scan driving control signal SCS depending on synchronization signals supplied from an external source. The data driving control signal DCS and the scan driving control signal SCS generated from the timing controller 250 are supplied to the data driver 220 and to the scan driver 210, respectively. The timing controller 250 rearranges the data supplied from the external source and supplies the rearranged data DATA to the data driver 220.

35 **[0038]** The pixel unit 230 receives a first power source ELVDD and a second power source ELVSS from an external source. The first power source ELVDD and the second power source ELVSS are supplied to the pixel unit 230, and are respectively supplied to the pixels 240. The pixels 240 receiving the first power source ELVDD and the second power source ELVSS displays images corresponding to data signals supplied from the data driving circuit 222.

[0039] FIG. 4A illustrates a block circuit diagram of an embodiment of the data driving circuit illustrated in FIG. 3. For the sake of discussion, FIG. 4A will be described assuming that the data driving circuit 222 includes "i" channels.

40 **[0040]** Referring to FIG. 4A, the data driving circuit 222 includes the following:

45 a shift register unit 223 for supplying sampling signals in sequence, a sampling latch unit 224 for storing data DATA in sequence in response to the sampling signals, a holding latch unit 225 for temporarily storing data stored in the sampling latch unit 224 and supplying the stored data to a level shifter 226, a level shifter 226 for raising a voltage level of the data, and a data signal generator 227 for generating data signals corresponding to bit values of data.

50 **[0041]** The shift register unit 223 receives a source shift clock SSC and a source start pulse SSP from the timing controller 250. The shift register unit 223 receiving the source shift clock SSC and the source start pulse SSP may generate "i" sampling signals in sequence, while allowing the source start pulse SSP to be shifted depending on the source shift clock SSC. The shift register unit 223 includes "i" shift registers 2231 to 223i.

[0042] The sampling latch unit 224 stores data in sequence depending on the sampling signals supplied in sequence from the shift register unit 223. The sampling latch unit 224 includes "i" sampling latches 2241 to 224i for storing "i" data. Each size of the sampling latches 2241 to 224i may be set to store k bit data. For the sake of discussion, this exemplary sampling latch unit 224 will be described assuming that k bit is 6 bits.

55 **[0043]** The holding latch unit 225 receives and stores the data from the sampling latch unit 224 in response to a source output enable SOE signal. The holding latch unit 225 supplies the stored data to a level shifter 226. The holding latch unit 225 includes "i" holding latches 2251 to 225i. Each of the holding latches 2251 to 225i may be configured to store k bit data.

[0044] The level shifter 226 raises a voltage level of the data supplied from the holding latch unit 225 and supplies the data with a raised voltage level to the data signal generator 227. In this regard, the data driver 220 receives data having a low voltage level and raises the voltage level of the data to a high voltage level by employing the level shifter 226.

[0045] In other implementations, the data driver 220 may not include the level shifter 226. For example, circuit components necessary to raise the voltage level of the data from a low voltage level to a high voltage level may be arranged external to the data driver 220. Accordingly, the holding latch unit 225 may be directly connected to the data signal generator 227. In such an arrangement, however, manufacturing costs may be increased.

[0046] The data signal generator 227 generates data signals corresponding to bit values (or gray scale values) of the data and supplies the generated data signals to the data lines D1 to Di. The data signal generator 227 receives a plurality of reference voltages (refs) from a gamma voltage unit 229 and generates data signals by using the received reference voltages (refs). The data signal generator 227 will be described in more detail below.

[0047] The gamma voltage unit 229 supplies the plurality of reference voltages (refs) to the data signal generator 227. The gamma voltage unit 229 may be arranged inside or outside of the data driving circuit 222.

[0048] Referring to FIG. 4B, a buffer unit 228 is connected between the data signal generator 227 and the data lines D1 to Di. The buffer unit 228 supplies the data signals supplied from the data signal generator 227 to the data lines D1 to Di.

[0049] FIG. 5 illustrates a block circuit diagram of an exemplary data signal generator as illustrated in FIGS. 4A and 4B. Referring to FIG. 5, the data signal generator 227 includes, for each channel, a first DAC 300, a second DAC 302 and a decoder unit 304.

[0050] The first DAC 300 receives the plurality of reference voltages (ref) from a gamma unit 229. The first DAC 300 selects a first reference voltage (ref1) and a second reference voltage (ref2) from the plurality of reference voltages (refs) depending on, e.g., a value of upper bits of the data. The first DAC 300 receives the data from the level shifter 226, or directly from the holding latch unit 225, depending on the implementation.

[0051] The first DAC 300 supplies the first reference voltage (ref1) and the second reference voltage (ref2) to the second DAC 302 via a first line L1 and a second line L2, respectively. That is, the first DAC 300 may extract two reference voltages from the plurality of reference voltages (refs) depending on the value of the upper bits. The first DAC 300 supplies the extracted two reference voltages to the second DAC 302 as the first reference voltage (ref1) and the second reference voltage (ref2). For the sake of discussion, it will be assumed that the first reference voltage (ref1) is set to be lower than the second reference voltage (ref2).

[0052] The second DAC 302 divides the first reference voltage (ref1) and the second reference voltage (ref2) into a plurality of voltages. The second DAC 302 may supply any one of the first reference voltage (ref1), the second reference voltage (ref2) and the divided voltages to the output terminal (out) as a data signal, depending on a value of the lower bits of the data.

[0053] The decoder unit 304 controls the turning on and the turning off of switches included in the second DAC 302 depending on the value of the lower bits of the data. That is, the decoder unit 304 may control the turning on and the turning off of the switches so that a resistance value between the first line L1 and the second line L2 can be variably controlled depending on the value of the lower bits of the data.

[0054] FIG. 6 illustrates a circuit diagram of a second DAC according to a first embodiment of the present invention. Referring to FIG. 6, the second DAC 302 includes a first group of voltage dividing resistors R11 to R18, a second group of voltage dividing resistors R21 to R28, a third group of voltage dividing resistors R31 to R38, a fourth group of voltage dividing resistors R41 to R48, and a fifth group of voltage dividing resistors R51 to R58, which are arranged between the first line L1 and the second line L2. The second DAC 302 also includes an arrangement of switches. The switches will be described in more detail below.

[0055] The first group of voltage dividing resistors R11 to R18 are arranged between the first line L1 and the second line L2 in series. The first group of voltage dividing resistors R11 to R18 divide the voltages of the first reference voltage (ref1) and the second reference voltage (ref2). The resistance values of the first group of voltage dividing resistors R11 to R18 may be identical so that the first reference voltage (ref1) and the second reference voltage (ref2) may be evenly divided.

[0056] A first switch SW1 is arranged between the first group of voltage dividing resistors R11 to R18 and the first line L1. The first switch SW1 allows the first group of voltage dividing resistors R11 to R18 to be electrically connected to the first line L1 and may remain in a turned on state. The first switch SW1 is arranged in order to compensate for the turn on resistances of a second switch SW2, a third switch SW3, a fourth switch SW4, and a fifth switch SW5, which will be described below.

[0057] The second group of voltage dividing resistors R21 to R28 is arranged in parallel with the first group of voltage dividing resistors R11 to R18, and is between the first line L1 and the second line L2. The number of resistors in the second group of voltage dividing resistors R21 to R28 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The second switch SW2 is arranged between the second group of voltage dividing resistors R21 to R28 and the first line L1.

[0058] During an exemplary operation, a first control signal CS1 is supplied from the decoder unit 304, and the second

switch SW2 may be turned on. When the second switch SW2 is turned on, the second group of voltage dividing resistors R21 to R28 may be electrically connected to the first line L1. If the second group of voltage dividing resistors R21 to R28 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become lower than the case when only the first group of voltage dividing resistors R11 to R18 is electrically connected to first line L1 and the second line L2.

[0059] The third group of voltage dividing resistors R31 to R38 is arranged in parallel with the second group of voltage dividing resistors R21 to R28, between the first line L1 and the second line L2. The number of resistors in the third group of voltage dividing resistors R31 to R38 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The third switch SW3 is arranged between the third group of voltage dividing resistors R31 to R38 and the first line L1.

[0060] During an exemplary operation, a second control signal CS2 is supplied from the decoder unit 304, and the third switch SW3 may be turned on. When the third switch SW3 is turned on, the third group of voltage dividing resistors R31 to R38 may be electrically connected to the first line L1. If the third group of voltage dividing resistors R31 to R38 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become even lower than the case when the first group of voltage dividing resistors R11 to R18 and the second group of voltage dividing resistors R21 to R28 are electrically connected to the first line L1.

[0061] The fourth group of voltage dividing resistors R41 to R48 is arranged in parallel with the third group of voltage dividing resistors R31 to R38, between the first line L1 and the second line L2. The number of resistors in the fourth group of voltage dividing resistors R41 to R48 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The fourth switch SW4 is arranged between the fourth group of voltage dividing resistors R41 to R48 and the first line L1.

[0062] During an exemplary operation, a third control signal CS3 is supplied from the decoder unit 304, and the fourth switch SW4 is turned on. When the fourth switch SW4 is turned on, the fourth group of voltage dividing resistors R41 to R48 may be electrically connected to the first line L1. If the fourth group of voltage dividing resistors R41 to R48 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become even lower than the case when the first voltage group of dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, and the third group of voltage dividing resistors R31 to R38 are electrically connected to the first line L1.

[0063] The fifth group of voltage dividing resistors R51 to R58 is arranged in parallel with the fourth group of voltage dividing resistors R41 to R48, and is between the first line L1 and the second line L2. The number of resistors in the fifth group of voltage dividing resistors R51 to R58 may be identical to the number of resistors in the first group of voltage dividing resistors R11 to R18. The fifth switch SW5 is arranged between the fifth group of voltage dividing resistors R51 to R58 and the first line L1.

[0064] During an exemplary operation, a fourth control signal CS4 is supplied from the decoder unit 304, and the fifth switch SW5 may be turned on. When the fifth switch SW5 is turned on, the fifth group of voltage dividing resistors R51 to R58 may be electrically connected to the first line L1. If the fifth group of voltage dividing resistors R51 to R58 is connected to the first line L1, the resistance value between the first line L1 and the second line L2 may become even lower than the case when the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38 and the fourth group of voltage dividing resistors R41 to R48 are electrically connected to the first line L1.

[0065] For the sake of discussion, FIG. 6 illustrates four voltage dividing resistor columns R21 to R28, R31 to R38, R41 to R48, and R51 to R58 that are arranged in parallel to the first group of voltage dividing resistors R11 to R18; however the present invention is not limited thereto. One or more voltage dividing resistor columns is in parallel with the first group of voltage dividing resistors R11 to R18.

[0066] The second DAC 302 includes a first group of switches SW11 to SW18, a second group of switches SW21 to SW27, a third group of switches SW30 to SW37, a fourth group of switches SW41 to SW47, and a fifth group of switches SW51 to SW57. The first group of switches SW11 to SW18 is arranged at each node of the first group of voltage dividing resistors R11 to R18. The first group of switches SW11 to SW18 supplies the voltage divided in the first group of voltage dividing resistors R11 to R18 to the output terminal (out).

[0067] In particular, an eleventh switch SW11 is arranged between a first node N1 and an output terminal (out) and supplies the second reference voltage (ref2) to the output terminal (out). A twelfth switch SW12 arranged between a second node N2 and the output terminal (out) supplies the voltage of the second node N2 to the output terminal (out). A thirteenth switch SW13 arranged between a third node N3 and the output terminal (out) supplies the voltage of the third node N3 to the output terminal (out). A fourteenth switch SW14 arranged between a fourth node N4 and the output terminal (out) supplies the voltage of the fourth node N4 to the output terminal (out). A fifteenth switch SW 15 arranged between a fifth node N5 and the output terminal (out) supplies the voltage of the fifth node N5 to the output terminal (out). A sixteenth switch SW16 arranged between a sixth node N6 and the output terminal (out) supplies the voltage of the sixth node N6 to the output terminal (out). A seventeenth switch SW17 arranged between a seventh node N7 and

the output terminal (out) supplies a voltage of the seventh node N7 to the output terminal (out). An eighteenth switch SW18 arranged between an eighth node N8 and the output terminal (out) supplies the first reference voltage (ref1) to the output terminal (out).

[0068] The decoder unit 304 controls the turning on and the turning off of the first group of switches SW11 to SW 18 depending on the lower bits of the data.

In other words, the decoder unit 304 allows any one of the first group of switches SW11 to SW 18 to be turned on depending on the lower bits of the data, and the turned on switch may supply a predetermined voltage value to the output terminal (out). The voltage value supplied to the output terminal (out) is supplied to pixels 240 as a data signal. In another implementation, the data signal may be supplied to the pixels 240 via the buffer unit 228.

[0069] The second group of switches SW21 to SW27 is arranged between nodes of the first group of voltage dividing resistors R11 to R18 and corresponding nodes of the second group of voltage dividing resistors R21 to R28. The second group of switches SW21 to SW27 may be turned on simultaneously with the second switch SW2, in response to the first control signal CS1 supplied from the decoder unit 304. Nodes of the first group of voltage dividing resistors R11 to R18 and corresponding nodes of the second group of voltage dividing resistors R21 to R28 may be electrically connected by the respective switches of the second group of switches SW21 to SW27.

[0070] The third group of switches SW31 to SW37 is arranged between nodes of the second group of voltage dividing resistors R21 to R28 and corresponding nodes of the third group of voltage dividing resistors R31 to R38. The third group of switches SW31 to SW37 may be turned on simultaneously with the third switch SW3 in response to the second control signal CS2 supplied from the decoder unit 304. Nodes of the second group of voltage dividing resistors R21 to R28 and corresponding nodes of the third group of voltage dividing resistors R31 to R38 may be electrically connected by the respective switches of the third group of switches SW31 to SW37.

[0071] The fourth group of switches SW41 to SW47 is arranged between nodes of the third group of voltage dividing resistors R31 to R38 and corresponding nodes of the fourth group of voltage dividing resistors R41 to R48. The fourth group of switches SW41 to SW47 may be turned on simultaneously with the fourth switch SW4 in response to the third control signal CS3 supplied from the decoder unit 304. Nodes of the third group of voltage dividing resistors R31 to R38 and corresponding nodes of the fourth group of voltage dividing resistors R41 to R48 may be electrically connected by the respective switches of the fourth group of switches SW41 to SW47.

[0072] The fifth group of switches SW51 to SW57 is arranged between nodes of the fourth group of voltage dividing resistors R41 to R48 and corresponding nodes of the fifth group of voltage dividing resistors R51 to R58. The fifth group of switches SW51 to SW57 may be turned on simultaneously with the fifth switch SW5 in response to the fourth control signal CS4 supplied from the decoder unit 304. Nodes of the fourth group of voltage dividing resistors R41 to R48 and corresponding nodes of the fifth group of voltage dividing resistors R51 to R58 may be electrically connected by the respective switches of the fifth group of switches SW51 to SW57.

[0073] An operation of the second DAC 302 according to this embodiment of the present invention will be described in detail with reference to FIG. 6 and Table 1, below.

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Table 1

Data			Switches											
D2	D1	D0	SW11	SW12	SW13	SW14	SW15	SW16	SW17	SW18	SW2	SW3	SW4	SW5
0	0	0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
0	0	1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
0	1	0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
0	1	1	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
1	0	0	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON
1	0	1	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
1	1	0	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
1	1	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF

[0074] Table 1 illustrates a diagram of the on and off states of the switches controlled by the decoder unit 304. For the sake of discussion, the number of lower bits of data is 3. However, it will be appreciated that other numbers of lower bits may be used.

[0075] The decoder unit 304 turns on the eleventh switch SW11 when a lower 3 bits "000" is input. The second reference voltage (ref2) is supplied to the first node N 1 and output to the output terminal (out) via the eleventh switch SW11. The second reference voltage (ref2) is then supplied to the pixels 240 as the data signal. When the second reference voltage (ref2) is supplied to the output terminal (out), only the first group of voltage dividing resistors R11 to R18 is connected between the first line L1 and the second line L2. Thus, a high resistance may be set between the first line L1 and the second line L2. That is, when the second reference voltage (ref2) is output, the resistance value between the first line L1 and the second line L2 may be set high, thereby making it possible to prevent the generation of voltage drop, since a value of the constant current may be low and the resistance may be high.

[0076] When a lower 3 bits "100" is input (e.g., to output an intermediate gray scale voltage), the decoder unit 304 turns on the second switch SW2, the third switch SW3, the fourth switch SW4, the fifth switch SW5 and the fifteenth switch SW 15.

[0077] If the second switch SW2, the third switch SW3, the fourth switch SW4 and the fifth switch SW5 are turned on, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, the fourth group of voltage dividing resistors R41 to R48 and the fifth group of voltage dividing resistors R51 to R58 are connected to the first group of voltage dividing resistors R11 to R18 in parallel. Thus, when the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, the fourth group of voltage dividing resistors R41 to R48 and the fifth group of voltage dividing resistors R51 to R58 are connected to the first group of voltage dividing resistors R11 to R18 in parallel, the resistance value between the first line L1 and the second line L2 is set even lower compared to the resistance value when the lower 3 bits "000" are input and the second reference voltage (ref2) is output.

[0078] In detail, when the decoder unit 304 supplies the second control signal CS1 to the second switch SW2, the second group of switches SW21 to SW27 may be turned on simultaneously. Similarly, when the decoder unit 304 supplies the second control signal CS2, the third control signal CS3, and the fourth control signal CS4 to the third switch SW3, the fourth switch SW4, and the fifth switch SW5, respectively, the third group of switches SW31 to SW37, the fourth group of switches SW41 to SW47, and the fifth group of switches SW51 to SW57 may be turned on simultaneously. Thus, nodes between the corresponding first to fifth groups of voltage dividing resistors R11 to R18, R21 to R28, R31 to R38, R41 to R48, and R51 to 58 may be electrically connected.

[0079] Additionally, if the fifteenth switch SW15 is turned on, the voltage applied to the fifth node N5 is supplied to the output terminal (out) as a data signal. That is, when the lower 3 bits "100" are input, the intermediate gray scale voltage may be supplied to the output terminal (out). Accordingly, the resistance value between the first line L1 and the second line L2 may be set even lower than the resistance value when the second reference voltage (ref2) is output. Therefore, by lowering the resistance between the first line L 1 and the second line L2, the charging speed of the pixels 240 may be enhanced when an intermediate gray scale voltage is output as the data signal.

[0080] When expressing gray scale voltages corresponding to inputs "001," "010" and "011," between "000" to "100," the resistance value between the first line L1 and the second line L2 may be set correspondingly lower in sequence. Thus, the gray scale voltage may be supplied to the output terminal (out) by setting the resistance between the first line L1 and the second line L2 to a correspondingly lower value in sequence from the second reference voltage (ref2) to an intermediate gray scale voltage.

[0081] More particularly, when "001" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18 and the second group of voltage dividing resistors R21 to R28 can be connected in parallel, and the resistance value may be lower than when "000" is input. When "010" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, and the third group of voltage dividing resistors R31 to R38 may be connected in parallel, and the resistance value may be even lower than when "001" is input. Also, when "011" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, and the fourth group of voltage dividing resistors R41 to R48 may be connected in parallel, and the resistance value may be even lower than when "010" is input.

[0082] In the same manner, the decoder unit 304 supplies the gray scale voltage via the second DAC 304 by setting the resistance between the first line L1 and the second line L2 to be sequentially lowered from the first reference voltage (ref1) to an intermediate gray scale voltage.

[0083] That is, in a sequence similar to that just described, when "111" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18 and the second group of voltage dividing resistors R21 to R28 may be connected in parallel. When "110" is input as the lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, and the third group of voltage dividing resistors R31 to R38 may be connected in parallel, and the resistance value may be lower than when "111" is input. Also, when "101" is input as the

lower 3 bits, the first group of voltage dividing resistors R11 to R18, the second group of voltage dividing resistors R21 to R28, the third group of voltage dividing resistors R31 to R38, and the fourth group of voltage dividing resistors R41 to R48 may be connected in parallel, and the resistance value may be lower than when "110" is input.

[0084] FIG. 7 illustrates a circuit diagram of a second DAC according to a second embodiment of the present invention. In the following description, a detailed description of elements included in the second DAC 302' that are identical to those previously described in FIG. 6 will not be repeated.

[0085] Referring to FIG. 7, the first switch SW1 is arranged between the first group of voltage dividing resistors R11 to R18 and the second line L2. The second switch SW2 is arranged between the second group of voltage dividing resistors R21 to R28 and the second line L2. The third switch SW3 is arranged between the third group of voltage dividing resistors R31 to R38 and the second line L2. The fourth switch SW4 is arranged between the fourth group of voltage dividing resistors R41 to R48 and the second line L2. The fifth switch SW5 is arranged between the fifth group of voltage dividing resistors R51 to R58 and the second line L2.

[0086] Although the positions of the first to the fifth switches SW1 to SW5 may be changed, the driving process therein may be identical to the driving process of the first embodiment of the present invention, as illustrated in FIG. 6. Accordingly, a detailed description of the driving process will not be repeated.

[0087] As described above, a data driver, an organic light emitting display, and a method of driving the same according to the present invention may set the resistance value between the first line and the second line to be high when outputting the first reference voltage and the second reference voltage. Also, the resistance value between the first line and the second line may be low when outputting the intermediate gray scale voltage, which is between the first reference voltage and the second reference voltage. Thus, the present invention may enable charging of the intermediate gray scale voltage to the pixels within a short period of time, so as to enhance the driving ability. Additionally, the resistance value between the first line and the second line may be set correspondingly lower as the gray scale voltage to be output increasingly differs from the first reference voltage to an intermediate gray scale voltage, which may enable generation of the data signal without voltage drop. Also, the resistance value between the first line and the second line may be set correspondingly lower as the gray scale voltage to be output increasingly differs from the second reference voltage to the intermediate gray scale voltage, which may enable generation of the data signal without voltage drop.

[0088] Embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation.

Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A data driver, comprising:

a first digital-to-analog converter configured to select first and second reference voltages from a plurality of reference voltages depending on upper bits of data and to supply the selected first and second reference voltages to a first line and a second line, respectively;

a second digital-to-analog converter having:

the first line and the second line configured to receive the first and the second reference voltages, respectively;

a first group of voltage dividing resistors between the first line and the second line, the first group of voltage dividing resistors configured to generate a plurality of gray scale voltages by dividing the first reference voltage and the second reference voltage;

a voltage dividing resistor unit between the first line and the second line; and

at least one switch between the voltage dividing resistor unit and one of the first line and the second line; and a decoder unit configured to control on and off states of the at least one switch depending on lower bits of data.

2. A data driver as claimed in claim 1, wherein the decoder unit is configured to control the on and off state of the at least one switch so that, when a gray scale voltage between the first reference voltage and the second reference voltage is output, a resistance value between the first line and the second line is set lower than a resistance value between the first line and the second line when either of the first reference voltage and the second reference voltage is output.

3. A data driver as claimed in claim 2, wherein the decoder unit is configured to control the on and off state of the at least one switch so that the resistance value between the first line and the second line is correspondingly set lower

as the gray scale voltage to be output increasingly differs from the first reference voltage to a predetermined gray scale voltage.

5 4. A data driver as claimed in claim 2, wherein the decoder unit is configured to control the on and off state of the at least one switch so that the resistance value between first line and the second line is correspondingly set lower as the gray scale voltage to be output increasingly differs from the second reference voltage to a predetermined gray scale voltage.

10 5. A data driver as claimed in any preceding claim, further comprising a first group of switches between nodes of the first voltage dividing resistors and an output terminal, the first group of switches controlled by the decoder unit and configured to supply a divided voltage to the output terminal.

6. A data driver as claimed in any preceding claim, wherein the voltage dividing resistor unit includes:

15 a second group of voltage dividing resistors,
a third group of voltage dividing resistors,
a fourth group of voltage dividing resistors, and
a fifth group of voltage dividing resistors,

20 wherein the second, third, fourth and fifth groups of voltage dividing resistors are respectively between the first line and the second line.

7. A data driver as claimed in claim 6, wherein the at least one switch includes:

25 a second switch between the second group of voltage dividing resistors and one of the first line and the second line;
a third switch between the third group of voltage dividing resistors and one of the first line and the second line;
a fourth switch between the fourth group of voltage dividing resistors and one of the first line and the second line; and
30 a fifth switch between the fifth group of voltage dividing resistors and one of the first line and the second line.

8. A data driver as claimed in claim 7, further comprising:

35 a second group of switches between nodes of the first voltage dividing resistors and corresponding nodes of the second voltage dividing resistors, the second group of switches configured to be turned on simultaneously with the second switch;
a third group of switches between nodes of the second voltage dividing resistors and corresponding nodes of the third voltage dividing resistors, the third group of switches configured to be turned on simultaneously with the third switch;
40 a fourth group of switches between nodes of the third voltage dividing resistors and corresponding nodes of the fourth voltage dividing resistors, the fourth group of switches configured to be turned on simultaneously with the fourth switch; and
a fifth group of switches between nodes of the fourth voltage dividing resistors and corresponding nodes of the fifth voltage dividing resistors, the fifth group of switches configured to be turned on simultaneously with the fifth
45 switch.

9. A data driver as claimed in any one of claims 6 to 8, wherein the number of resistors respectively included in the second group of voltage dividing resistors, the third group of voltage dividing resistors, the fourth group of voltage dividing resistors and the fifth group of voltage dividing resistors is identical to the number of resistors included in the first group of voltage dividing resistors.
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10. A data driver as claimed in any preceding claim, further comprising:

55 a shift register unit configured to supply sampling signals in sequence;
a sampling latch unit configured to store data in response to the sampling signals;
a holding latch unit configured to store data from the sampling latch unit; and
a data signal generator configured to receive data from the holding latch unit and generate data signals,

wherein each channel of the data signal generator includes the first digital-to-analog converter and the second digital-to-analog converter.

5 11. A data driver as claimed in claim 10, further comprising:

a level shifter between the holding latch unit and the data signal generator, the level shifter configured to increase a voltage level of the data; and
a buffer unit configured to receive data signals from the data signal generator.

10 12. An organic light emitting display, comprising:

a pixel unit including a plurality of pixels connected to scan lines and data lines;
a scan driver configured to drive the scan lines; and
a data driver according to any one of claims 1 to 11 configured to drive the data lines.

15 13. A method of driving an organic light emitting display, comprising:

supplying first and second reference voltages of a plurality of reference voltages to a first line and a second line, respectively, depending on upper bits of data;
20 dividing the first and the second reference voltages into a plurality of gray scale voltages by controlling a resistance value between the first line and the second line depending on lower bits of data; and
outputting a gray scale voltage.

25 14. The method as claimed in claim 13, wherein dividing comprises, when outputting a gray scale voltage that is between the first and the second reference voltages, setting the resistance value between the first line and the second line to be lower than the resistance value when outputting a gray scale voltage that is either of the first and the second reference voltages.

30 15. The method as claimed in claim 14, wherein the resistance value between the first line and the second line is correspondingly set lower as the gray scale voltage to be output increasingly differs from the first reference voltage to a predetermined gray scale voltage.

35 16. The method as claimed in claim 14, wherein the resistance value between the first line and the second line is correspondingly set lower as the gray scale voltage to be output increasingly differs from the second reference voltage to a predetermined gray scale voltage.

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FIG. 1
(RELATED ART)

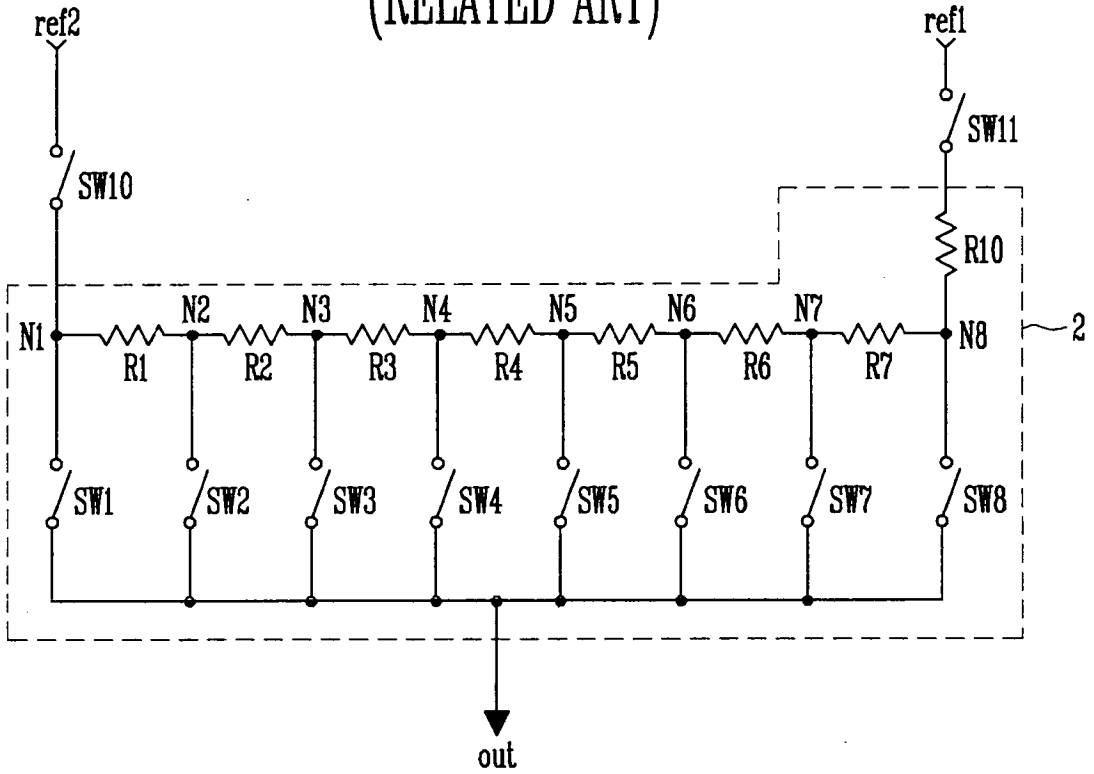


FIG. 2
(RELATED ART)

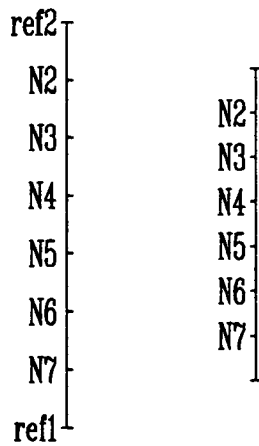


FIG. 3

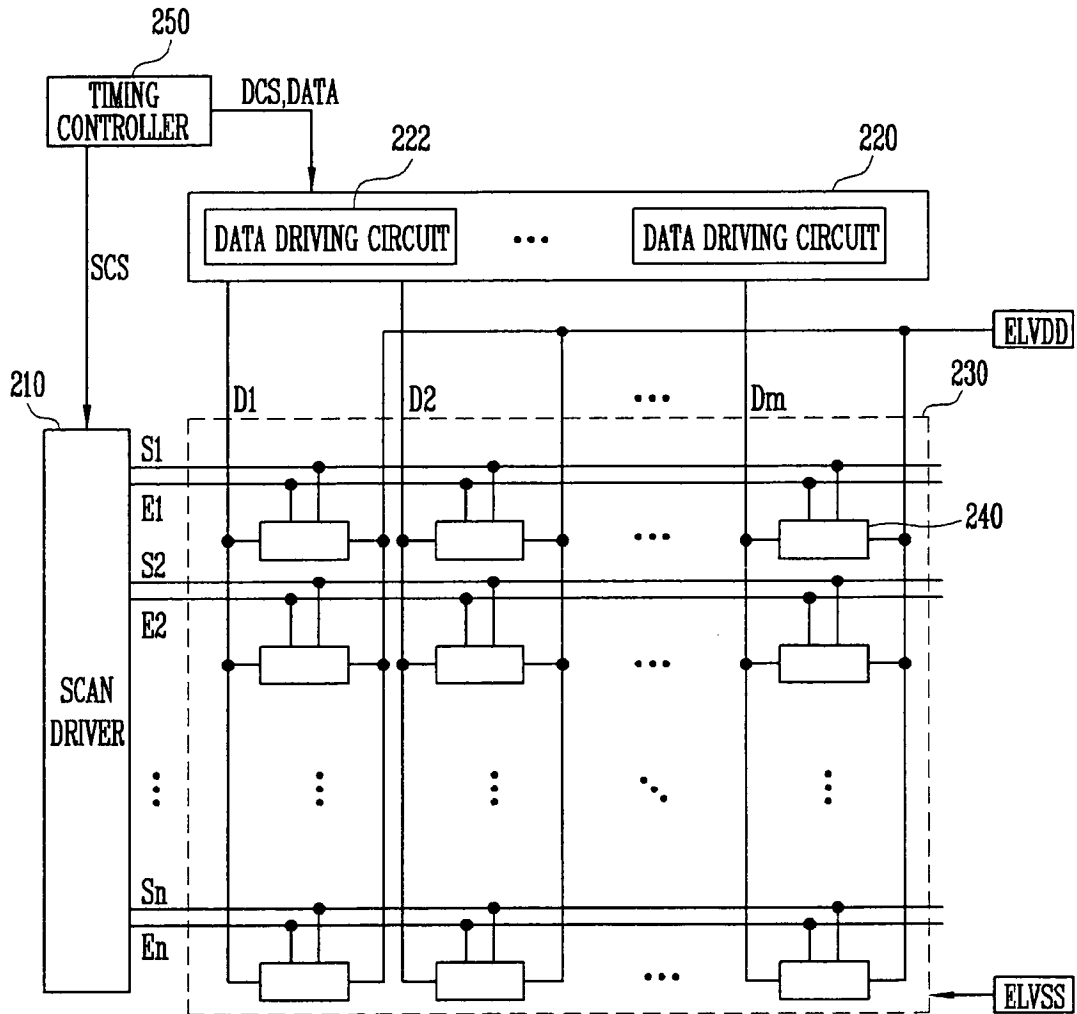


FIG. 4A

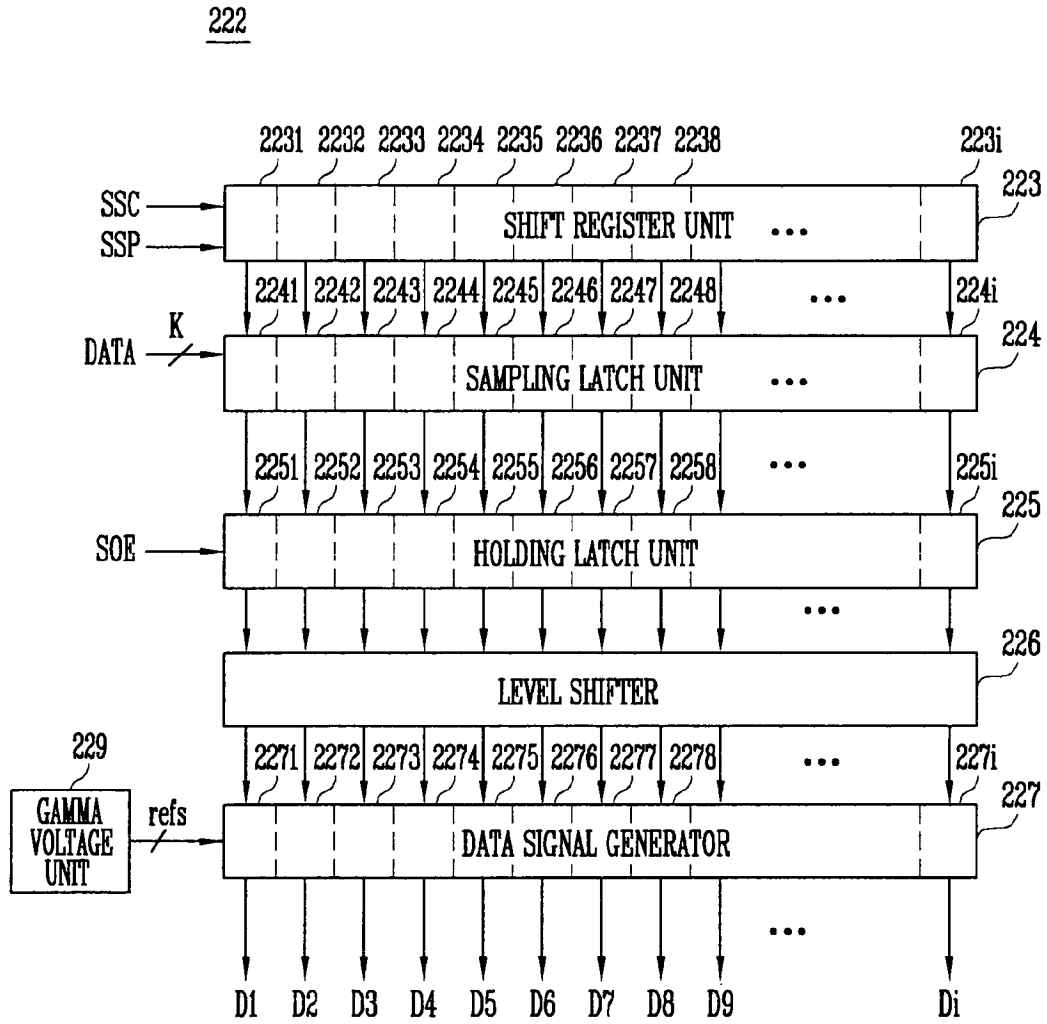


FIG. 4B

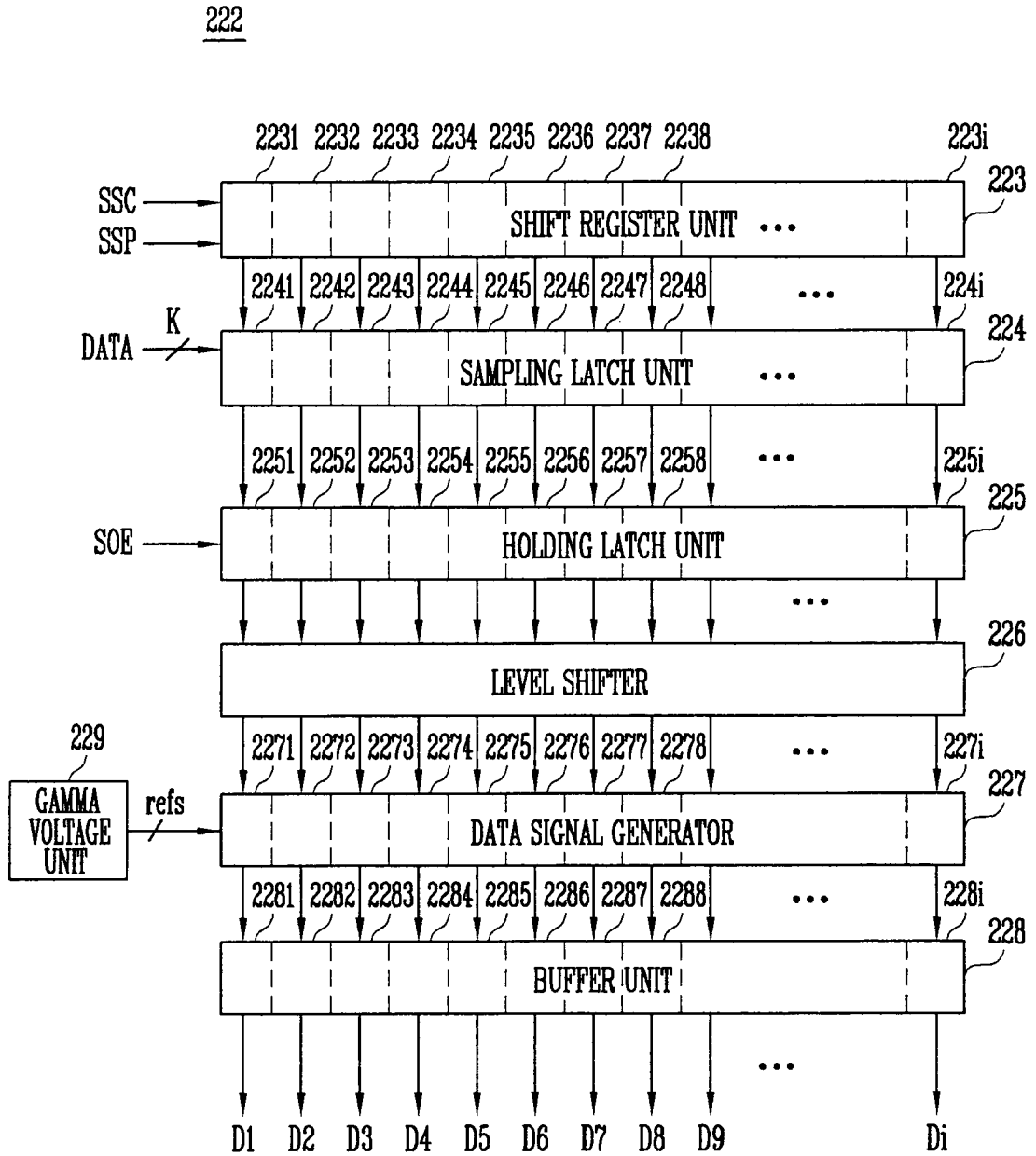


FIG. 5

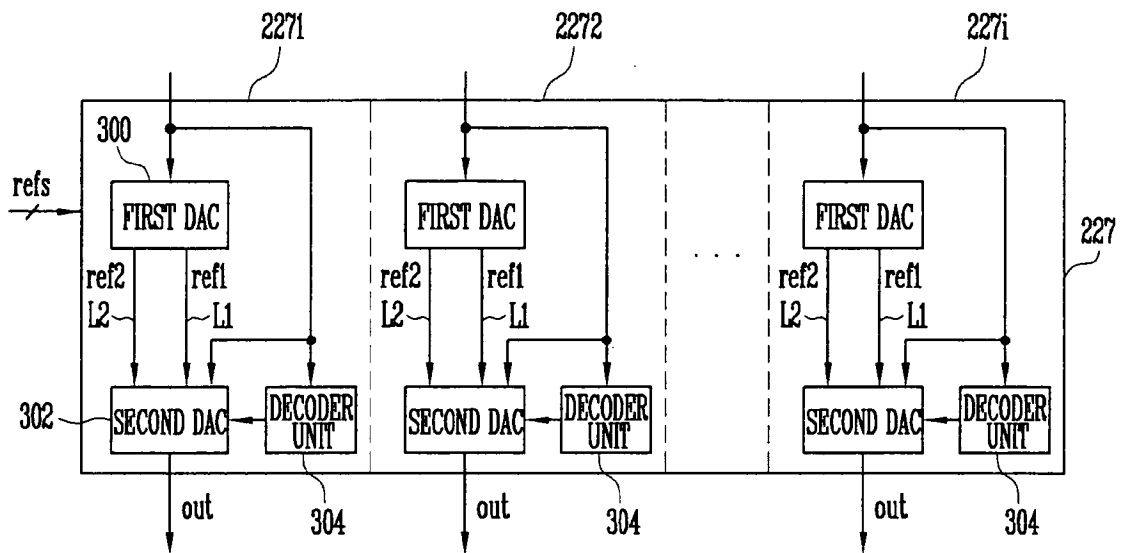


FIG. 6

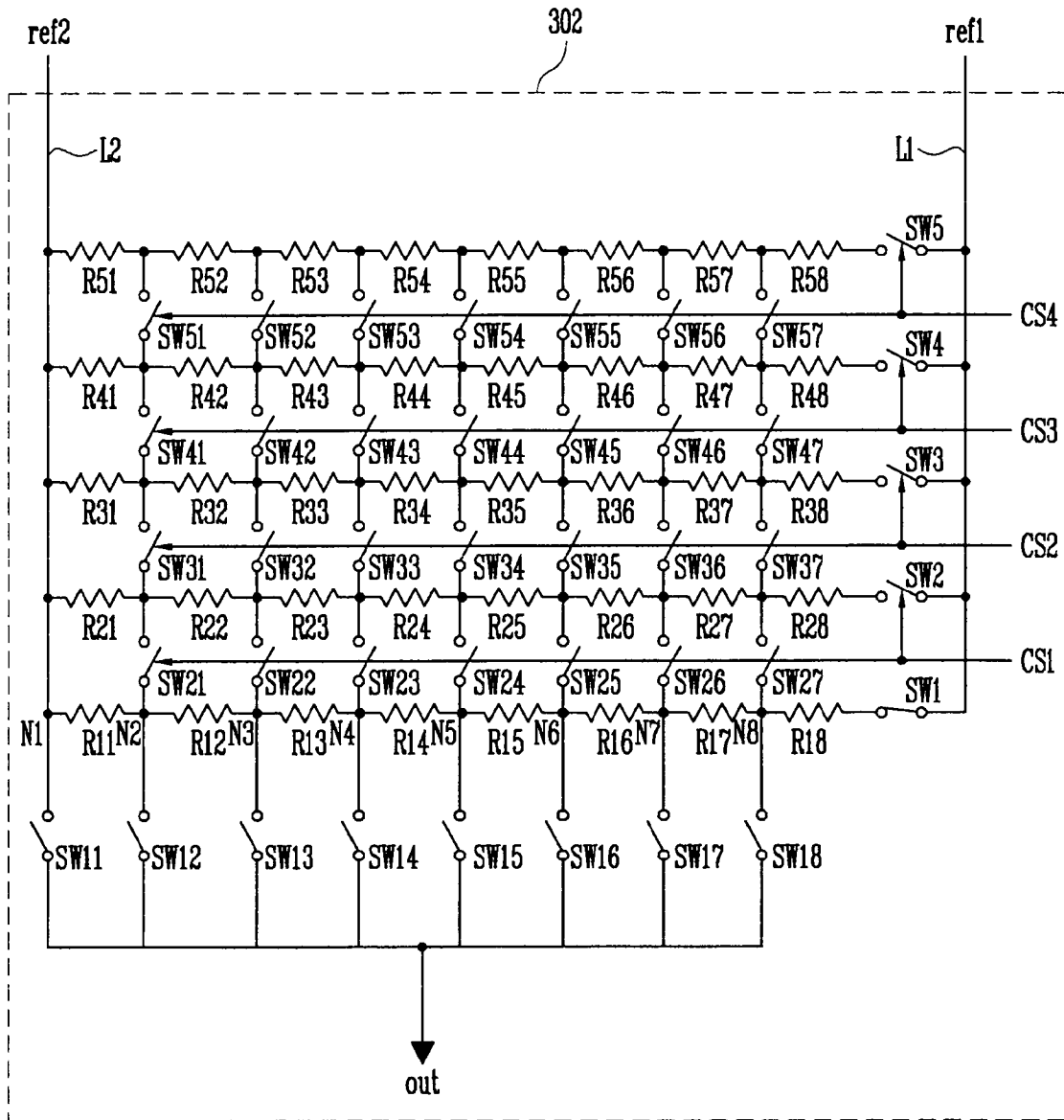
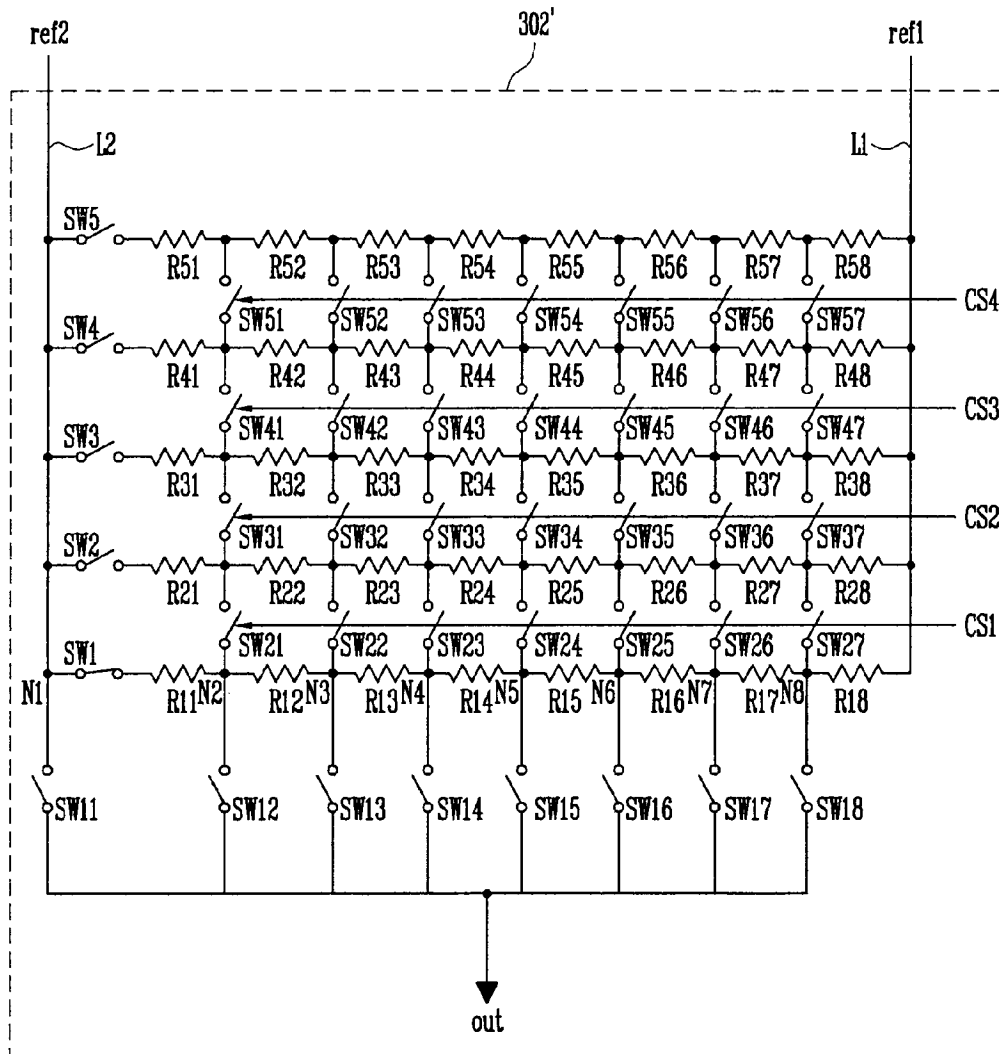


FIG. 7



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020050127233 [0031]

专利名称(译)	数据驱动器，有机发光显示器及其驱动方法		
公开(公告)号	EP1801774A2	公开(公告)日	2007-06-27
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摘要(译)

一种数据驱动器，包括：第一数模转换器，被配置为根据数据的高位选择第一和第二参考电压，并将第一和第二参考电压分别提供给第一线和第二线，第二数字-模拟转换器，具有第一线和第二线，分别接收第一和第二参考电压，第一组分压电阻，位于第一线和第二线之间，用于产生多个灰阶电压，第一线和第二线之间的分压电阻器单元，以及位于分压电阻器单元和第一线和第二线之一之间的至少一个开关，并且包括解码器单元，该解码器单元被配置为控制接通和断开状态。至少一个开关取决于较低的数据位。

FIG. 5

