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(54) Organic light emitting display device and method of fabricating the same

Organische lichtemittierende Anzeigevorrichtung und Herstellungsverfahren

Dispositif d'affichage électroluminescent organique et méthode de fabrication

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(73) Proprietor: **Samsung Display Co., Ltd.**
Gyeonggi-do (KR)

(72) Inventors:
- **Hwang, Eui-Hoon**
  Samsung SDI Co.,Ltd.
  Giheung-eup,Yongin-si,
  Gyeonggi-do (KR)
- **Lee, Sang-Gul**
  Samsung SDI Co., Ltd.
  Giheung-eup, Yongin-shi,
  Gyeonggi-do (KR)

(74) Representative: **Gulde & Partner**
Patent- und Rechtsanwaltskanzlei mbB
Wallstraße 58/59
10179 Berlin (DE)

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an organic light emitting display device (OLED) and a method of fabricating the same, and more particularly, to an OLED in which when a metal interconnection and a gate electrode are formed at the same time or when a first electrode is formed, interconnections for electrically connecting elements are formed, so that an overall fabrication process is shortened and the production cost is reduced by a decrease in the number of used masks.

2. Description of the Related Art

[0002] Among flat panel display devices (FPDs), an organic light emitting display device (OLED) is an emissive device that has a wide viewing angle and a fast response speed of 1 ms or less. Also, the OLED can be fabricated to a small thickness with low cost and has good contrast.

[0003] In the OLED having an organic emission layer (EML) interposed between an anode and a cathode, holes transported from the anode combine with electrons transported from the cathode to form hole-electron pairs, i.e., excitons. Thus, the OLED emits light by energy generated while the excitons transition from an excited state to a ground state.

[0004] In general, since each pixel of the OLED includes a thin film transistor (TFT), a certain current is supplied irrespective of the number of pixels of the OLED, so that the OLED can emit light with stable luminance and consume small power. For this reason, the OLED is quite appropriate for high-resolution large-sized display devices.

[0005] FIGs. 1A through 1K are cross-sectional views illustrating a conventional OLED having a top gate type CMOS TFT and a method of fabricating the same.

[0006] Referring to FIG. 1A, the conventional OLED having a top gate type complementary metal oxide semiconductor (CMOS) TFT includes a substrate 100 having a first TFT region A, a second TFT region B, and an opening region C. An amorphous silicon (a-Si) layer is deposited on the substrate 100, crystallized by a crystallization method, and then patterned using a first mask (not shown), thereby forming a first semiconductor layer 110 and a second semiconductor layer 115.

[0007] Typically, the mask is used to form a photoresist (PR) pattern during a photolithography process. An etching process is performed using the formed PR pattern. Thereafter, the PR pattern is removed by an ashing process using a dry etching process. After the ashing process, the remaining PR is entirely removed by a PR stripping process.

[0008] Referring to FIG. 1B, a gate insulating layer 120 is formed on the entire surface of the substrate 100 having the first and second semiconductor layers 110 and 115. A first PR pattern 125 is formed using a second mask (not shown) on the first and second semiconductor layers 110 and 115 in the first and second TFT regions A and B. A first impurity implantation process 127 may be performed to implant n-type impurity ions, such as P ions, As ions, Sb ions, or Bi ions, into the first semiconductor layer 110 of the first TFT region A. Thus, the first semiconductor layer 110 of the first TFT region A forms an NMOS transistor including first source and drain regions 110s and 110d and a first channel region 110c, which is interposed between the first source and drain regions 110s and 110d.

[0009] Referring to FIG. 1C, a gate electrode material is deposited on the gate insulating layer 120 in the first and second TFT regions A and B and then patterned using a third mask (not shown), thereby forming a first gate electrode 130 and a second gate electrode 135 corresponding to the first channel region 110c and a second channel region 115c of the first and second semiconductor layers 110 and 115. In this case, the first gate electrode 130 is patterned to a smaller size than the first channel region 110c of the first semiconductor layer 110 in the first TFT region A. A second impurity implantation process 140 is performed using the first gate electrode 130 as a mask, thereby forming lightly doped drain (LDD) regions 110e in predetermined regions of the first channel region 110c of the first semiconductor layer 110. Thus, the first semiconductor layer 110 of the first TFT region A defines the first source and drain regions 110s and 110d, which are doped with n-type impurity ions, the LDD regions 110e, and the first channel region 110c, which is interposed between the LDD regions 110e. Also, as the result of the second impurity implantation process 140, the semiconductor layer 115 of the second TFT region B defines second source and drain regions 115s and 115d and the second channel region 115c.

[0010] Referring to FIG. 1D, a second photoresist pattern 145 is formed using a fourth mask (not shown) to completely cover the first TFT region A and cover only the second gate electrode 135 in the second TFT region B. A third impurity implantation process 150 is then performed so that p-type impurity ions, such as B ions, Al ions, Ga ions, or In ions are implanted into the second source and drain regions 115s and 115d of the second TFT region B. In this case, the p-type impurity ions are implanted into the second source and drain regions 115s and 115d of the second TFT region B at a higher concentration than the LDD regions 110e. Accordingly, the second semiconductor layer 115 of the second TFT region B forms a PMOS transistor including the second source and drain regions 115s and 115d and the second channel region 115c.

[0011] In this process, a CMOS transistor having both the NMOS transistor and the PMOS transistor is formed.

[0012] Referring to FIG. 1E, an interlayer insulating layer 155 is formed on the entire surface of the substrate

100 having the first and second gate electrodes 130 and 135. Contact holes 160 are formed using a fifth mask (not shown) in the interlayer insulating layer 155 formed in the first and second TFT regions A and B to expose portions of the first and second source and drain regions 110s, 110d, 115s, and 115d.

[0013] Referring to FIG. 1F, source and drain electrode materials are deposited through the contact holes 160 of the interlayer insulating layer 155 and then patterned using a sixth mask (not shown), thereby forming first and second source and drain electrodes 165s, 165d, 170s, and 170d that are in contact with the first and second source and drain regions 110s, 110d, 115s, and 115d of the first and second semiconductor layers 110 and 115, respectively.

[0014] Referring to FIG. 1G, a passivation layer 175 is formed on the entire surface of the substrate 100 having the first and second source and drain electrodes 165s, 165d, 170s, and 170d. By performing an etching process using a seventh mask (not shown), a first via hole 180 is formed in the passivation layer 175 formed in the opening region C.

[0015] Referring to FIG. 1H, a planarization layer 185 is formed on the entire surface of the substrate 100 having the passivation layer 175 with the first via hole 180 to reduce a step. By performing a wet etching process using an eighth mask (not shown) and an etchant having a high etch selectivity with respect to the planarization layer 185, a second via hole 190 is formed in the planarization layer 185 of the opening region C.

[0016] Referring to FIGs. 1I and 1J, a first electrode 195 is formed around the second via hole 190 and on inner walls and bottom surfaces of the first and second via holes 180 and 190 of the opening region C. The first electrode 195 is a reflective anode that includes a transparent electrode 195b and a reflective layer 195a with high reflectance.

[0017] Referring to FIG. 1I the reflective layer 195a of the first electrode 195 is formed by depositing and then patterning aluminum (Al) using a ninth mask (not shown).

[0018] Referring to FIG. 1J, the transparent electrode 195b is formed by depositing indium tin oxide (ITO) or indium zinc oxide (IZO) on the reflective layer 195a and then patterning the deposited material through a wet or dry etching process using a tenth mask (not shown).

[0019] Referring to FIG. 1K, a pixel defining layer is deposited on the entire surface of the substrate 100 having the first electrode 195 and then patterned using an eleventh mask (not shown), thereby forming an opening P to expose a portion of the surface of the first electrode 195.

[0020] An organic layer (not shown) having at least an emission layer is formed on the exposed surface of the first electrode 195, and a second electrode (not shown) is deposited on the entire surface of the substrate 100 having the organic layer. The second electrode is a thin transmissive electrode, which is formed of one material selected from the group consisting of Mg, Ca, Al, Ag, and an alloy thereof.

[0021] The substrate 100 having the second electrode is encapsulated with an upper substrate by a typical method, thereby completing a top-emitting OLED having a top gate type CMOS TFT. The CMOS TFT includes LDD regions in an NMOS transistor.

[0022] Also, a method of fabricating an OLED having a bottom gate type CMOS TFT with the LDD regions is similar to the above-described method of fabricating the OLED having the top gate type CMOS TFT with the LDD regions.

[0023] First, a gate electrode material is deposited in a first TFT region and a second TFT region of a substrate and then patterned using a first mask, thereby forming a gate electrode. A semiconductor layer is formed on a gate insulating layer corresponding to the gate electrode and then patterned using a second mask. N-type impurity ions are implanted using a third mask into the semiconductor layer in the first TFT region, thereby forming an NMOS region. Also, LDD impurity ions are implanted using a fourth mask to form the LDD regions. Thereafter, p-type impurity ions are implanted using a fifth mask into the semiconductor layer in the second TFT region, thereby forming a PMOS region. As a result, a CMOS transistor having both an NMOS transistor with the LDD regions and a PMOS transistor is obtained.

[0024] Thereafter, formation of a contact hole in an interlayer insulating layer using a sixth mask, patterning of source and drain electrodes using a seventh mask, formation of a first via hole using an eighth mask, formation of a second via hole using a ninth mask, patterning of a reflective layer of a first electrode using a tenth mask, patterning of a transparent electrode of the first electrode using an eleventh mask, and formation of a pixel defining layer having an opening using a twelfth mask are the same as the above-described method of fabricating the OLED having the top gate type CMOS TFT. That is, an OLED having a bottom gate type CMOS TFT with the LDD regions is formed by performing a mask process twelve times.

[0025] As described above, the fabrication of the OLED having the top gate type or bottom gate type CMOS TFT with the LDD regions requires comparatively many process steps because a PMOS TFT and an NMOS TFT should be formed on a single substrate, a via hole should be patterned twice, and a first electrode should be patterned twice. Also, although the LDD regions are formed to reduce a leakage current of the NMOS TFT and solve a hot carrier effect caused by miniaturization, the formation of the LDD regions may result in a further increase in the number of masks used to fabricate the CMOS TFT.

[0026] The conventional OLED having the top gate type or bottom gate type CMOS TFT with the LDD regions is obtained by performing a mask process eleven to twelve times. As a result, an overall process tact time is extended, the process becomes complicated, yield decreases, and production cost increases.

[0027] US 2003/0127652 A1 describes an OLED

which fabricated in a six-mask process wherein the ground line and the power line are entirely disposed above the substrate.

[0028] EP 1 331 667 A2 discloses an OLED in which the pixel portions are surrounded by an insulating bank. An organic conductive film is covering the entire surface thereby increasing the resistance of the bank in a lateral direction to reduce crosstalk.

[0029] US 2002/0104995 discloses a OLED display comprising a switching TFT and a driving TFT. Both TFTs are covered by insulating films on which the actual OLED pixels are formed.

SUMMARY OF THE INVENTION

[0030] The present invention provides an organic light emitting display device (OLED) and a method of fabricating the same in which when a metal interconnection and a gate electrode are formed at the same time or when a first electrode is formed, interconnections for electrically connecting elements are formed, so that an overall fabrication process is shortened and the production cost is reduced by a decrease in the number of used masks.

[0031] According to the present invention an organic light emitting display device (OLED) is provided, comprising:

a substrate having a first TFT region, a second TFT region, an opening region and an interconnection region;

the substrate further having a first thin film transistor (TFT) arranged in the first TFT region, a second TFT arranged in the second TFT region, and a metal interconnection arranged in the interconnection region;

a planarization layer disposed on the substrate having the first TFT, the second TFT, and the metal interconnection;

a plurality of contact holes disposed in predetermined regions of the planarization layer to expose predetermined regions of first source and drain regions of the first TFT, second source and drain regions of the second TFT, and the metal interconnection;

a first interconnection disposed directly on the planarization layer, one of the end portions of the first interconnection being in contact with the metal interconnection and one of the first source and drain regions respectively through the contact holes, thereby electrically connecting the metal interconnection with the one of the first source and drain regions;

a second interconnection disposed directly on the planarization layer; one of the end portions of the second interconnection being in contact with the other of the first source and drain regions and one of the second source and drain regions respectively through the contact holes, thereby electrically connecting the other of the first source and drain with the one of the second source and drain regions;

a first electrode directly on the planarization layer, one of the end portions of the first electrode being in contact with the other of the second source and drain regions through the contact holes; and

wherein the first interconnection, the second interconnection, and the first electrode are formed at the same time on the same layer.

[0032] An OLED may include: a substrate having a first thin film transistor (TFT), a second TFT, and a metal interconnection; a planarization layer disposed on the substrate having the first TFT, the second TFT, and the metal interconnection; contact holes disposed in predetermined regions of the planarization layer to expose predetermined regions of first source and drain regions of the first TFT, second source and drain regions of the second TFT, and the metal interconnection; and an interconnection for electrically connecting the metal interconnection, the first source and drain regions, and the second source and drain regions through the contact holes.

[0033] An OLED may include: a metal interconnection, a first gate electrode, and a second gate electrode disposed on a substrate; a gate insulating layer disposed on the metal interconnection, the first gate electrode, and the second gate electrode; a first semiconductor layer and a second semiconductor layer disposed on the gate insulating layer, the first semiconductor layer corresponding to the first gate electrode and including first source and drain regions and a first channel region, the second semiconductor layer corresponding to the second gate electrode and including second source and drain regions and a second channel region; a planarization layer disposed on the first semiconductor layer and the second semiconductor layer; contact holes formed by etching predetermined regions of the planarization layer and exposing predetermined regions of the metal interconnection, the first source and drain regions, and the second source and drain regions; a first interconnection for connecting the metal interconnection with one of the first source and drain regions through the contact holes, a second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions through the contact holes, and a first electrode connected to the other of the second source and drain regions through the contact holes; a pixel defining layer disposed on the first interconnection, the second interconnection, and the first electrode and exposing a predetermined region of the first electrode; and an organic layer and a second electrode disposed on the exposed region of the first electrode, the organic layer including at least an organic emission layer (EML).

[0034] An OLED may include: a metal interconnection disposed on a substrate; a buffer layer disposed on the metal interconnection; a first semiconductor layer and a second semiconductor layer disposed on the buffer layer,

the first semiconductor layer including first source and drain regions and a first channel region, the second semiconductor layer including second source and drain regions and a second channel region; a gate insulating layer disposed on the first semiconductor layer and the second semiconductor layer; a first gate electrode and a second gate electrode disposed on the gate insulating layer and corresponding to the first channel region and the second channel region, respectively; a planarization layer disposed on the first gate electrode and the second gate electrode; contact holes formed by etching predetermined regions of the planarization layer and the gate insulating layer to expose predetermined regions of the first source and drain regions and the second source and drain regions, and formed by etching predetermined regions of the planarization layer, the gate insulating layer, and the buffer layer to expose predetermined regions of the metal interconnection; a first interconnection for connecting the metal interconnection with one of the first source and drain regions through the contact holes, a second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions through the contact holes, and a first electrode connected to the other of the second source and drain regions through the contact holes; a pixel defining layer disposed on the first interconnection, the second interconnection, and the first electrode and exposing a predetermined region of the first electrode; and an organic layer and a second electrode disposed on the exposed region of the first electrode, the organic layer including at least an organic emission layer.

[0035] A method of fabricating an OLED is provided, comprising:

providing a substrate having a first TFT region (A), a second TFT region (B), an opening region (C) and an interconnection region (D);

forming a metal interconnection in the interconnection region (D)on a substrate ;

forming a buffer layer on the metal interconnection and on the substrate;

forming a first semiconductor layer and a second semiconductor layer on the buffer layer;

forming a gate insulating layer on the first semiconductor layer and the second semiconductor layer;

forming a first gate electrode and a second gate electrode on the gate insulating layer such that the first gate electrode and the second gate electrode correspond to a first channel region of the first semiconductor layer and a second channel region of the second semiconductor layer, respectively;

forming a planarization layer on the first gate electrode and the second gate electrode;

forming contact holes exposing predetermined regions of first source and drain regions of the first semiconductor layer and predetermined regions of second source and drain regions of the second semiconductor layer by etching predetermined regions of the planarization layer and the gate insulating layer, and exposing predetermined regions of the metal interconnection by etching predetermined regions of the planarization layer , the gate insulating layer, and the buffer layer;

forming a reflective layer and a transparent layer on the substrate having the contact holes;

forming a first interconnection, a second interconnection, and a first electrode at the same time by patterning the reflective layer and the transparent layer, the first interconnection for connecting the metal interconnection with one of the first source and drain regions, the second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions, the first electrode connected to the other of the second source and drain regions;

forming a pixel defining layer on the substrate having the first interconnection , the second interconnection, and the first electrode to expose a predetermined region of the first electrode in the opening region (C); and

forming an organic layer having at least an organic emission layer and a second electrode on the exposed region of the first electrode.

[0036] Further, a method of fabricating an OLED is provided, comprising:

forming a metal interconnection , a first gate electrode , a second gate electrode on a substrate at the same time and forming the metal interconnection in a predetermined distance apart from the first and second electrodes on the same layer as the first and second gate electrodes;

forming a gate insulating layer on the metal interconnection, the first gate electrode and the second gate electrode ;

forming a first semiconductor layer and a second semiconductor layer on the gate insulating layer such that the first gate electrode and the second gate electrode correspond to a first channel region of the first semiconductor layer and a second channel region of the second semiconductor layer, respectively;

forming a passivation layer on the first semiconductor layer and a second semiconductor layer;

forming a planarization layer on the first gate electrode and the second gate electrode ;

forming contact holes exposing predetermined regions of first source and drain regions of the first semiconductor layer and predetermined regions of second source and drain regions of the second semiconductor layer by etching predetermined regions of the planarization layer and the passivation layer, and exposing predetermined regions of the metal interconnection by etching predetermined regions of the planarization layer, the planarization layer , and

the passivation layer;
forming a reflective layer and a transparent layer on the substrate having the contact holes;
forming at the same time a first interconnection , a second interconnection , and a first electrode by patterning the reflective layer and the transparent layer , the first interconnection for connecting the metal interconnection with one of the first source and drain regions, the second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions, the first electrode connected to the other of the second source and drain regions;
forming a pixel defining layer on the substrate having the first interconnection , the second interconnection, and the first electrode to expose a predetermined region of the first electrode ; and
forming an organic layer having at least an organic emission layer and a second electrode on the exposed region of the first electrode.

[0037] A method of fabricating an OLED may include: forming a metal interconnection on a substrate; forming a buffer layer on the metal interconnection; forming a first semiconductor layer and a second semiconductor layer on the buffer layer; forming a gate insulating layer on the first semiconductor layer and the second semiconductor layer; forming a first gate electrode and a second gate electrode on the gate insulating layer such that the first gate electrode and the second gate electrode correspond to a first channel region of the first semiconductor layer and a second channel region of the second semiconductor layer, respectively; forming a planarization layer on the first gate electrode and the second gate electrode; forming contact holes exposing predetermined regions of first source and drain regions of the first semiconductor layer and predetermined regions of second source and drain regions of the second semiconductor layer by etching predetermined regions of the planarization layer and the gate insulating layer, and exposing predetermined regions of the metal interconnection by etching predetermined regions of the planarization layer, the gate insulating layer, and the buffer layer; forming a reflective layer and a transparent layer on the substrate having the contact holes; forming a first interconnection, a second interconnection, and a first electrode by patterning the reflective layer and the transparent layer, the first interconnection for connecting the metal interconnection with one of the first source and drain regions, the second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions, the first electrode connected to the other of the second source and drain regions; forming a pixel defining layer on the substrate having the first interconnection, the second interconnection, and the first electrode to expose a predetermined region of the first electrode; and forming an organic layer having at least an organic emission layer and a second electrode on the exposed region of the first electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] The above and other features of the present invention will be described in reference to certain exemplary embodiments thereof with reference to the attached drawings in which:

FIGs. 1A through 1K are cross-sectional views illustrating a conventional organic light emitting display device (OLED) having a top gate type CMOS thin film transistor (TFT) and a method of fabricating the same;
FIGs. 2A through 2H are cross-sectional views illustrating an OLED having a bottom gate type CMOS TFT and a method of fabricating the same according to an exemplary embodiment of the present invention; and
FIGs. 3A through 3I are cross-sectional views illustrating an OLED having a top gate type CMOS TFT and a method of fabricating the same according to another exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0039] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. The same reference numerals are used to denote the same elements throughout the specification.

Embodiment 1

[0040] FIGs. 2A through 2H are cross-sectional views illustrating an organic light emitting display device (OLED) having a bottom gate type complementary metal oxide semiconductor thin film transistor (CMOS TFT) and a method of fabricating the same according to an exemplary embodiment of the present invention.

[0041] Referring to FIGs. 2A through 2H, the OLED having the bottom gate type CMOS TFT according to an exemplary embodiment of the present invention includes a substrate 200 having a first TFT region A, a second TFT region B, an opening region D, and an interconnection region C. The substrate 200 may be a transparent substrate, which is formed of glass, plastic, or quartz.

[0042] Referring to FIG. 2A, a first gate electrode 210, a second gate electrode 215, and a metal interconnection 220 are formed and then patterned using a first mask (not shown) in the first and second TFT regions A and B of the substrate 200. The first and second gate electrodes 210 and 215 may be formed of one material selected from the group consisting of molybdenum (Mo), tungsten (W), aluminum (Al), and an alloy thereof, for example,

tungsten molybdenum (MoW), molybdenum (Mo), tungsten (W), tungsten silicide (WSi_2), molybdenum silicide ($MoSi_2$), and aluminum (Al). The first and second gate electrodes 210 and 215 may be formed by a sputtering method or a vacuum deposition method. Typically, the first and second gate electrodes 210 and 215 may be formed by depositing a material using a sputtering method and then patterning the deposited material.

[0043] The first mask forms a photoresist pattern according to patterns formed on a reticle by a photolithography process, and then the photoresist pattern is removed by ashing and photoresist stripping processes.

[0044] During the formation of the first and second gate electrodes 210 and 215, the metal interconnection 220 is formed in the interconnection region C of the substrate 200. The metal interconnection 220 is formed a predetermined distance apart from the first and second gate electrodes 210 and 215 on the same layer as the first and second gate electrodes 210 and 215. The metal interconnection 220 may be formed by depositing the same material as the first and second gate electrodes 210 and 215 and then patterning the material using the first mask.

[0045] Referring to FIG. 2B, a gate insulating layer 230 is formed on the entire surface of the substrate 200 having the first and second gate electrodes 210 and 215 and the metal interconnection 220. The gate insulating layer 230 may be a silicon oxide layer, a silicon nitride layer, or a stacked layer thereof. The gate insulating layer 230 may be formed by a plasma-enhanced chemical vapor deposition (PECVD) process or a low-pressure CVD (LPCVD) process.

[0046] A first semiconductor layer 240 and a second semiconductor layer 245 are formed using a second mask (not shown) on the gate insulating layer 230 in the first and second TFT regions A and B, respectively. In this case, the first and second semiconductor layers 240 and 245 may be formed of amorphous silicon (a-Si) or polycrystalline Si (poly-Si), preferably, poly-Si. The first and second semiconductor layers 240 and 245 may be formed by depositing a-Si using a PECVD process, crystallizing the a-Si into a poly-Si layer using a crystallization method, and patterning the poly-Si layer using the second mask. In this case, the deposition of the a-Si using the PECVD process may be followed by dehydrogenation of the a-Si using an annealing process to lower the concentration of hydrogen.

[0047] Thereafter, the second mask, which is used to pattern the first and second semiconductor layers 240 and 245, is positioned under the substrate 200, and a back exposure process using the second mask and the first and second gate electrodes 210 and 215 as masks is carried out to form a first photoresist pattern 247 corresponding to the first and second gate electrodes 210 and 215 on predetermined regions of the first and second semiconductor layers 240 and 245 in the first and second TFT regions A and B.

[0048] More specifically, the back exposure process includes positioning the second mask, which is used to pattern the first and second semiconductor layers 240 and 245, under the substrate 200 and irradiating light toward a bottom of the substrate 200. Thus, the first photoresist pattern 247 is formed on the predetermined regions of the first and second semiconductor layers 240 and 245 corresponding to the first and second gate electrodes 210 and 215 in the first and second TFT regions A and B. The first photoresist pattern 247 may be formed of a positive photosensitive material. Thus, when a portion of the first photoresist pattern 247 is exposed to light, the portion changes into a material soluble in a developing solution and thus is etched. In general, the photosensitive material is composed of a solvent, which controls viscosity, a photo active compound, which reacts with ultraviolet (UV) rays, and a polymer resin, which is a chemical combination. The photosensitive material may include acrylic resin or polyimide (PI).

[0049] Accordingly, photoresist, which is positioned on the gate insulating layer 230 that transmits light incident from the bottom of the substrate 200 and on a region of the semiconductor layer that does not correspond to the gate electrode, is exposed to light, changes into a material soluble in a developing solution, and is etched during the back exposure process. On the other hand, since the first and second gate electrodes 210 and 215 formed in the first and second TFT regions A and B of the substrate 200, are formed of a metal and do not transmit light, they are not exposed to light incident from the bottom of the substrate 200, and thus the first photoresist pattern 247 is formed to the same size as the first and second electrodes 210 and 215.

[0050] By performing a first impurity implantation process 250 using the first photoresist pattern 247 obtained by the back exposure process, lightly doped drain (LDD) impurity ions are implanted into the first and second semiconductor layers 240 and 245. Thus, LDD regions 240e and a first channel region 240c are formed in the first TFT region A, and second source and drain regions 245s and 245d and a second channel region 245c are formed in the second TFT region B. The first impurity implantation process 250 may be carried out using typical n-type impurity ions, for example, PH_3 ions. In particular, the LDD regions 240e are formed to improve the characteristics of a TFT. Also, because the first photoresist pattern 247 is formed by the back exposure process after the formation of the first and second semiconductor layers 240 and 245, LDD impurity ions can be implanted into the first semiconductor layer 240 in the first TFT region A without an additional mask, so that one process mask can be saved in a number.

[0051] In a case where the back exposure process is unnecessary or cannot be used, the first photoresist pattern 247 may be formed using a mask for a photoresist pattern. However, one more mask is required at this time.

[0052] Referring to FIG. 2C, the first photoresist pattern 247 is removed, and a second photoresist pattern 255 is formed using a third mask (not shown). Specifically, the second photoresist pattern 255 is formed to have a slight-

ly greater width than the first channel region 240c on the first semiconductor 240 in the first TFT region A to completely cover the first channel region 240c and partially cover the LDD regions 240e. Also, the second photoresist pattern 255 is formed to completely cover the second semiconductor layer 245 in the second TFT region B.

[0053] Thereafter, n-type impurity ions are implanted into exposed portions of the LDD regions 240e in the first TFT region A using the second photoresist pattern 255. The n-type impurity ions include one material selected from the group consisting of phosphorus (P), arsenic (As), antimony (Sb), and bismuth (Bi). The concentration of the n-type impurity ions is higher than that of the LDD impurity ions. As a result, an NMOS transistor including the first source and drain regions 240s and 240d, which are doped with n-type impurity ions, the LDD regions 240e, which are doped with LDD impurity ions, and the first channel region 240c, which is interposed between the LDD regions 240e, is formed in the first semiconductor layer 240. On the other hand, the second semiconductor layer 245 formed in the second TFT region B, which is covered by the second photoresist pattern 255, is not doped with the n-type impurity ions.

[0054] Referring to FIG. 2D, the second photoresist pattern 255 is removed, and a third photoresist pattern 265 is formed using a fourth mask (not shown). The third photoresist pattern 265 covers the second channel region 245c, which is defined in the second semiconductor layer 245 of the second TFT region B through the first impurity implantation process 250, exposes the second source and drain regions 245s and 245d, and completely covers the first semiconductor layer 240 in the first TFT region A.

[0055] Subsequently, a third impurity implantation process 270 is performed using the third photoresist pattern 265 so that p-type impurity ions are implanted into the second source and drain regions 245s and 245d of the second TFT region B. The p-type impurity ions include one selected from the group consisting of boron (B), aluminum (Al), gallium (Ga), and indium (In). The concentration of the p-type impurity ions is higher than that of the LDD impurity ions. Thus, a PMOS transistor including the second source and drain regions 245s and 245d, which are doped with p-type impurity ions, and the second channel region 245c, which is interposed between the second source and drain regions 245s and 245d, is formed in the second semiconductor layer 245. On the other hand, the first semiconductor layer 240 formed in the first TFT region, which is covered by the third photoresist pattern 265, is not doped with the p-type impurity ions.

[0056] As a result, a CMOS TFT having both the NMOS transistor formed in the first TFT region A and the PMOS transistor formed in the second TFT region B is formed.

[0057] Referring to FIG. 2E, a passivation layer 275 is formed on the first and second semiconductor layers 240 and 245. Typically, the passivation layer 275 is formed to prevent TFTs from external contamination. The passivation layer 275 may be formed of an inorganic insulating layer, which is a silicon nitride layer, a silicon oxide layer, or a stacked layer thereof. The passivation layer 275 may be formed by a PECVD process or an LPCVD process. Preferably, the passivation layer 275 may be obtained by depositing an inorganic insulating material, annealing the material, and hydrogenating the annealed material.

[0058] A planarization layer 280 is formed on the passivation layer 275 to reduce a step. The planarization layer 280 may be typically formed of one organic material selected from the group consisting of benzocyclobutane (BCB), PI, polyamide (PA), acrylic resin, and phenolic resin. The planarization layer 280 may be formed by a spin coating process.

[0059] Thereafter, the passivation layer 275 and the planarization layer 280, which are formed in the first and second TFT regions A and B and the interconnection region C, are etched using a fifth mask (not shown), thereby forming contact holes 285 in the passivation layer 275 and the planarization layer 280 to expose portions of the first and second source and drain regions 240s, 240d, 245s, and 245d and the metal interconnection 220.

[0060] Referring to FIG. 2F, a first electrode material layer 290 including a reflective layer 290a and a transparent layer 290b is deposited in the contact holes 285 and then patterned by blanket etching, thereby forming a first electrode 291, a first interconnection 292, and a second interconnection 293.

[0061] The reflective layer 290a is formed of a metal with high reflectance, which is one selected from the group consisting of aluminum (Al), silver (Ag), and an alloy thereof. Also, the transparent layer 290b is formed of one of ITO and IZO. Thus, the first electrode 291 is formed as a reflective anode. The reflective layer 290a and the transparent layer 290b may be sequentially deposited by a sputtering method, a vacuum deposition method, or an ion plating method. Typically, the reflective layer 290a and the transparent layer 290b are formed by a sputtering method.

[0062] The reflective layer 290a of the first electrode material layer 290 may be formed of Ag such that the reflective layer 290a can be patterned with the transparent layer 290b by blanket etching, while the transparent layer 290b may be formed of ITO. The first electrode material layer 290 may be formed by sequentially depositing Ag and ITO using a sputtering method and then wet- or dry-etching the Ag layer and the ITO layer through blanket etching using a sixth mask (not shown). The blanket etching may make use of an ordinary etching process. By blanket-etching the first electrode material layer 290 including the reflective layer 290a and the transparent layer 290b, one process mask can be saved in a number during the formation of the first electrode 291.

[0063] As a result, the first electrode material layer 290 is patterned to form the first interconnection 292 and the second interconnection 293. The first interconnection 292 connects the metal interconnection 220 formed in

the interconnection region C with one of the first source and drain regions 240s and 240d (e.g., the first source region 240s) of the first semiconductor layer 240 formed in the first TFT region A. Also, the second interconnection 293 connects the other of the first source and drain regions 240s and 240d (e.g., the first drain region 240d) of the first semiconductor layer 240 formed in the first TFT region A with one of the second source and drain regions 245s and 245d (e.g. the second source region 245s) of the second semiconductor layer 245 formed in the second TFT region B.

[0064] When forming the first electrode 291, which is a reflective anode contacting the second source and drain regions 245s and 245d, the process of forming the contact holes for connecting the second source and drain regions 245s and 245 with source and drain electrodes and the process of forming the source and drain electrodes may be omitted so that one process mask can be further saved in a number.

[0065] Referring to FIG. 2G, a pixel defining layer 295 is formed on the entire surface of the substrate 200 to expose a predetermined region of the first electrode 291. The pixel defining layer 295 is typically formed of one organic material selected from the group consisting of BCB, PI, PA, acrylic resin, and phenolic resin. The pixel defining layer 295 is formed by depositing an organic material using a spin coating process and then etching using a seventh mask so that an opening P is formed in the opening region D to expose a portion of the surface of the first electrode 291. The opening P may be formed by a dry or wet etching process, typically, a wet etching process.

[0066] Referring to FIG. 2H, an organic layer 297 including at least an organic emission layer (EML) and a second electrode 299 are formed on the exposed portion of the first electrode 291 in the opening P. In addition to the EML, the organic layer 297 may further include at least one of an electron injection layer (EIL), an electron transport layer (ETL), a hole transport layer (HTL), and a hole injection layer (HIL).

[0067] The EML may be formed of a low molecular substance or a high molecular substance. The low molecular substance may be one selected from the group consisting of tris(8-hydroxyquinoline) aluminum (Alq3), anthracene, cyclo pentadiene, ZnPBO, Balq, and DPVBi. The high molecular substance may be one selected from the group consisting of polythiophene (PT), poly(p-phenylenevinylene) (PPV), polyphenylene (PPP), and derivatives thereof. The organic layer 297 may be formed by a vacuum deposition method, a spin coating method, an inkjet printing method, or a laser induced thermal imaging (LITI) method. Typically, the organic layer 297 may be formed by a spin coating method. Also, the organic layer 297 may be patterned by an LITI method or a vacuum deposition method using a shadow mask.

[0068] The second electrode 299 is a thin transmissive electrode, which may be formed of one selected from the group consisting of Mg, Ca, Al, Ag, and an alloy thereof. Also, the second electrode 299 may be formed by a vacuum deposition method.

[0069] The substrate 200 having the second electrode 299 is encapsulated with an upper substrate using an ordinary method. Thus, a top-emitting OLED having the bottom gate type CMOS TFT with the LDD regions according to the embodiment of the present invention is completed using seven masks (or using eighth masks if the back exposure process is not used).

Embodiment 2

[0070] FIGS. 3A through 3I are cross-sectional views illustrating an OLED having a top gate type CMOS TFT and a method of fabricating the same according to another exemplary embodiment of the present invention.

[0071] Referring to FIG. 3A, the OLED having a top gate type CMOS TFT according to another embodiment of the present invention includes a substrate 300 having a first TFT region A, a second TFT region B, an opening region C, and an interconnection region D. The substrate 300 may be a transparent substrate, which is formed of glass, plastic, or quartz.

[0072] A metal interconnection 310 is formed using a first mask (not shown) in the interconnection region D of the substrate 300. The metal interconnection 310 may be formed of one material selected from the group consisting of Mo, W, Al, and an alloy thereof. The metal interconnection 310 may be formed by a sputtering method or a vacuum deposition method. Typically, the metal interconnection 310 may be formed by depositing a material using a sputtering method and patterning the deposited material.

[0073] Referring to FIG. 3B, a buffer layer 320 is formed on the entire surface of the substrate 300 having the metal interconnection 310, and a first semiconductor layer 330 and a second semiconductor layer 335 are formed and then patterned using a second mask (not shown) on the buffer layer 320 in the first and second TFT regions A and B.

[0074] The buffer layer 320 is formed to protect a TFT that will be formed later from impurity ions diffusing from the substrate 300. The buffer layer 320 may be a silicon oxide layer, a silicon nitride layer, or a stacked layer thereof. The buffer layer 320 is formed by a PECVD process or an LPCVD process. The method of forming the first and second semiconductor layers 330 and 335 is the same as that described in Embodiment 1.

[0075] Referring to FIG. 3C, a first photoresist pattern 340 is formed using a third mask (not shown) to expose a predetermined region of the first semiconductor layer 330 in the first TFT region A, and a first impurity implantation process 345 is carried out using the first photoresist pattern 340 so that n-type impurity ions are implanted into the first semiconductor layer 330. The n-type impurity ions include one selected from the group consisting of P, As, Sb, and Bi. Thus, the first semiconductor layer 330 defines first source and drain regions 330s and 330d,

which are doped with the n-type impurity ions, and a first channel region 330c, which is interposed between the first source and drain regions 330s and 330d. On the other hand, the second semiconductor layer 335 formed in the second TFT region B, which is covered by the first photoresist pattern 340, is not doped with the n-type impurity ions.

[0076] Referring to FIG. 3D, after the first impurity implantation process 345, the first photoresist pattern 340 is removed by ashing and PR stripping processes, and a gate insulating layer 350 is formed on the entire surface of the substrate 300 having the first and second semiconductor layers 330 and 335. The gate insulating layer 350 may be a silicon oxide layer, a silicon nitride layer, or a stacked layer thereof. Also, the gate insulating layer 350 may be obtained by a PECVD process or an LPCVD process.

[0077] A first gate electrode 360 and a second gate electrode 365 are formed using a fourth mask (not shown) on the gate insulating layer 350 in the first and second TFT regions A and B. The first and second gate electrodes 360 and 365 are formed of one material selected from the group consisting of Mo, W, Al, and an alloy thereof. In this case, the first gate electrode 360 formed in the first TFT region A is formed to have a smaller width than the first channel region 330c shown in FIG. 3C to leave spaces for LDD regions that will be formed later. The first and second gate electrodes 360 and 365 may be formed by a sputtering method or a vacuum deposition method. Typically, the first and second gate electrodes 360 and 365 are formed by depositing a material using a sputtering method and patterning the deposited material.

[0078] A second impurity implantation process 370 is performed in the first and second TFT regions A and B using the first and second gate electrodes 360 and 365 as masks, so that LDD regions 330e are formed in the first semiconductor layer 330. Impurity ions doped into the LDD regions 330e are n-type impurity ions, typically, PH_3. The concentration of the LDD impurity ions is lower than that of the n-type impurity ions. Thus, the first semiconductor layer 330 formed in the first TFT region A forms an NMOS transistor including the first source and drain regions 330s and 330d, which are doped with n-type impurity ions, the LDD regions 330e, which are doped with low-concentration impurity ions, and the first channel region 330c, which is interposed between the LDD regions 330e. In this case, as the result of the second impurity implantation process 370, the second semiconductor layer 335 formed in the second TFT region B defines second source and drain regions 335s and 335d and a second channel region 335c, which is interposed between the second source and drain regions 335s and 335d.

[0079] Referring to FIG. 3E, a second photoresist pattern 375 is formed using a fifth mask (not shown) to completely cover the first semiconductor layer 330 in the first TFT region A and expose the second semiconductor layer 335 in the second TFT region B. A third impurity implantation process 380 is performed using the second photoresist pattern 375 on the second semiconductor layer 335 in the second TFT region B so that p-type impurity ions are implanted to form the second source and drain regions 335s and 335d. The p-type impurity ions include one selected from the group consisting of B, Al, Ga, and In. The concentration of the p-type impurity ions is higher than that of the LDD impurity ions. Thus, the second semiconductor layer 335 forms a PMOS transistor including the second source and drain regions 335s and 335d, which are doped with the p-type impurity ions, and the second channel region 335c, which is interposed between the second source and drain regions 335s and 335d.

[0080] As a result, a CMOS TFT having both the NMOS transistor formed in the first TFT region A and the PMOS transistor formed in the second TFT region B is formed.

[0081] Referring to FIG. 3F, a passivation layer 382 is formed on the first and second gate electrodes 360 and 365, and then a planarization layer 385 is formed on the passivation layer 382.

[0082] The passivation layer 382 and the planarization layer 385 are etched using a sixth mask (not shown), thereby forming contact holes 387 to expose portions of the first and second source and drain regions 330s, 330d, 335s, and 335d and the metal interconnection 310.

[0083] The methods of forming the passivation layer 382, the planarization layer 385, and the contact holes 387 are the same as those described in Embodiment 1.

[0084] Referring to FIG. 3G, a first electrode material layer 390 including a reflective layer 390a and a transparent layer 390b is stacked in the contact holes 387, and then patterned by a blanket etching process using a seventh mask (not shown), thereby forming a first electrode 391, a first interconnection 392, and a second interconnection 393.

[0085] The formation and patterning of the first electrode material layer 390 are the same as those described in Embodiment 1. The first electrode material layer 390 including the reflective layer 390a and the transparent layer 390b is blanket-etched, so that one process mask can be saved in a number during the formation of the first electrode 391.

[0086] As a result, the first electrode 391 is in contact with one of the second source and drain regions 335s and 335d of the second semiconductor layer 335 in the second TFT region B, and the first interconnection 392 is in contact with the metal interconnection 310 in the interconnection region C and one of the first source and drain regions 330s and 330d in the first TFT region A. Also, the second interconnection 393 is in contact with the other of the first source and drain regions 330s and 330d in the first TFT region A and the other of the second source and drain regions 335s and 335d in the second TFT region B.

[0087] Since the first electrode 391, the first interconnection 392, and the second interconnection 393 are formed at the same time, the process of forming the con-

tact holes for connecting the source and drain regions with source and drain electrodes and the process of forming the source and drain electrodes can be omitted. Thus, two process masks can be further saved in a number.

[0088] Referring to FIG. 3H, a pixel defining layer 395 is formed on the entire surface of the substrate 300 having the first electrode 391. The method of forming the pixel defining layer 395 is the same as that described in Embodiment 1. The pixel defining layer 395 is etched using an eighth mask (not shown) so that an opening P is formed in the opening region C to expose a portion of the surface of the first electrode 391. The opening P is formed by a dry or wet etching process.

[0089] Referring to FIG. 3I, an organic layer 397 having at least an EML and a second electrode 399 are formed on the exposed portion of the first electrode 391 in the opening P. The methods of forming the organic layer 397 and the second electrode 399 are the same as those described in Embodiment 1.

[0090] The substrate 300 having the second electrode 399 is encapsulated with an upper substrate using an ordinary method. Thus, a top-emitting OLED having the top gate type CMOS TFT with the LDD regions according to another embodiment of the present invention is completed using eighth process masks.

[0091] According to the present invention as described above, when a first electrode that is a reflective anode is formed, interconnections are brought into contact with internal devices at the same time. Thus, an OLED having a CMOS TFT with LDD regions can be formed using only 7 to 8 process masks compared to the conventional OLED using 11 to 12 process masks. As a result, an overall fabrication process can be shortened, the production cost can be reduced, and yield can increase.

Claims

1. An organic light emitting display device (OLED) comprising:

a substrate (200, 300) having a first TFT region (A), a second TFT region (B), an opening region (D), and an interconnection region (C);
the substrate (200, 300) further having a first thin film transistor (TFT) arranged in the first TFT region (A), a second TFT arranged in the second TFT region (B), and a metal interconnection (220, 310) arranged in the interconnection region (C);
a planarization layer (280, 385) disposed on the substrate (200, 300) having the first TFT, the second TFT, and the metal interconnection (220, 310);
a plurality of contact holes (285, 387) disposed in predetermined regions of the planarization layer (280, 385) to expose predetermined regions of first source (240s, 330s) and drain (240d, 330d) regions of the first TFT, second source (245s, 335s) and drain (245d, 335d) regions of the second TFT, and the metal interconnection (220, 310);
a first interconnection (292, 392) disposed directly on the planarization layer
(280, 385), one of the end portions of the first interconnection being in contact with the metal interconnection (220, 310) and one of the first source (240s, 330s) and drain (240d, 330d) regions respectively through the contact holes (285, 387), thereby electrically connecting the metal interconnection (220, 310) with the one of the first source (240s, 330s) and drain (240d, 330d) regions;
a second interconnection (293, 393) disposed directly on the planarization layer (280, 385); one of the end portions of the second interconnection (293, 393) being in contact with the other of the first source (240s, 330s) and drain (240d, 330d) regions and one of the second source (245s, 335s) and drain (245d, 335d) regions respectively through the contact holes (285, 387), thereby electrically connecting the other of the first source (240s, 330s) and drain (240d, 330d) with the one of the second source (245s, 335s) and drain (245d, 335d) regions;
a first electrode (291, 391) disposed directly on the planarization layer (280, 385), one of the end portions of the first electrode (291, 391) being in contact with the other of the second source (245s, 335s) and drain (245d, 335d) regions through the contact holes (285, 387).

2. The OLED according to claim 1, further comprising:

an organic layer (297, 397) disposed on the first electrode (291, 391); and
a second electrode (299, 399) disposed on the organic layer (297, 397).

3. The OLED according to claim 2, wherein the first electrode (291, 391) includes a reflective layer (290a, 390a) and a transparent layer (290b, 390b).

4. The OLED according to claim 3, wherein the reflective layer (290a, 390a) is formed of one selected from the group consisting of aluminum (Al), silver (Ag), and an alloy thereof.

5. The OLED according to claim 3, wherein the transparent layer (290b, 390b) is formed of one of indium tin oxide (ITO) and indium zinc oxide (IZO).

6. The OLED according to claim 1, wherein the first interconnection (292, 392) and the second interconnection (293, 393) are formed of the same material as the first electrode (291, 391).

7. The OLED according to claim 1, wherein a first gate electrode (210) of the first TFT, a second gate electrode (215) of the second TFT, and the metal interconnection (220) are disposed on the same layer.

8. The OLED according to claim 7, wherein the first gate electrode (210), the second gate electrode (215), and the metal interconnection (220) are formed of one selected from the group consisting of molybdenum (Mo), tungsten (W), aluminum (Al), and an alloy thereof.

9. The OLED according to claim 1, wherein the first TFT comprises:

a first gate electrode (210) disposed on the substrate (200);
a gate insulating layer (230) disposed on the first gate electrode (215); and
a first semiconductor layer (240) disposed on the gate insulating layer (240), corresponding to the first gate electrode (210), and including the first source (240s) and drain (240d) regions and a first channel region (240c), and

wherein the second TFT comprises:

a second gate electrode (215) disposed on the substrate (200); the gate insulating layer (230) disposed on the second gate electrode (215); and
a second semiconductor layer (245) disposed on the gate insulating layer (230), corresponding to the second gate electrode (215), and including the second source (245s) and drain (245d) regions and a second channel region (245c).

10. The OLED according to claim 1, wherein the first TFT comprises:

a first semiconductor layer (330) disposed on the substrate (300) and
including the first source (330s) and drain (330d) regions and a first channel region (330c);
a gate insulating layer (350) disposed on the first semiconductor layer (330); and
a first gate electrode (360) disposed on the gate insulating layer (350) and corresponding to the first channel region (330c), and

wherein the second TFT comprises:

a second semiconductor layer (335) disposed on the substrate (300) and including the second source (335s) and drain regions (335d) and a second channel region (335c);
the gate insulating layer (350) disposed on the second semiconductor layer (335); and
a second gate electrode (365) disposed on the gate insulating layer (350) and corresponding to the second channel region (335c).

11. The OLED according to claim 9 or 10, further comprising lightly doped drain (LDD) regions (240e, 330e), wherein the lightly doped drain regions (240e, 330e) are interposed between the first source region (240s, 330s) and the channel region (240c, 330c) and between the drain region (240d, 330d) and the channel region (240c, 330c) of the first TFT.

12. The OLED according to claim 9, further comprising: a pixel defining layer (295) is disposed on the first interconnection (292), the second interconnection (293), and the first electrode (291) exposing a predetermined region of the first electrode (291); and an organic layer (297) and a second electrode (299) are disposed on the exposed region of the first electrode (291), the organic layer (297) including at least an organic emission layer; wherein the gate insulating layer (230) is disposed on the metal interconnection (220), the first gate electrode (210); and the second gate electrode (215).

13. The OLED according to claim 12, wherein the metal interconnection (220), the first gate electrode (210), and the second gate electrode (215) are formed of the same material.

14. The OLED according to claim 12, further comprising LDD regions (240e) disposed between the first source (240s) and drain (240d) regions and the first channel region or between the second source (245s) and drain regions (245d) and the second channel region.

15. The OLED according to claim 12, wherein the first interconnection (292), the second interconnection (293), and the first electrode (291) include a reflective layer and a transparent layer.

16. The OLED according to claim 10, further comprising:

a buffer layer (320) disposed on the metal interconnection (310); the first semiconductor layer (330) and the second semiconductor layer (335) disposed on the buffer layer (320);
a pixel defining layer (395) disposed on the first interconnection (392), the second interconnection (393), and the first electrode (391) and exposing a predetermined region of the first electrode (391); and
an organic layer (397) and a second electrode (399) disposed on the exposed region of the first electrode (391), the organic layer (397) including at least an organic emission layer.

17. The OLED according to claim 16, further comprising LDD regions (330e) disposed between the first source (330s) and drain (330d) regions and the first channel region (330c) or between the second source (335s) and drain (335d) regions and the second channel region (335c).

18. The OLED according to claim 16, wherein the first interconnection (392), the second interconnection (393), and the first electrode (391) include a reflective layer and a transparent layer.

19. A method of fabricating an OLED, comprising:

providing a substrate (300) having a first TFT region (A), a second TFT region (B), an opening region (C) and an interconnection region (D);
forming a metal interconnection (310) in the interconnection region (D);
forming a buffer layer (320) on the metal interconnection (310) and on the substrate (300);
forming a first semiconductor layer (330) and a second semiconductor layer (335) on the buffer layer (320);
forming a gate insulating layer (350) on the first semiconductor layer (330) and the second semiconductor layer (335);
forming a first gate electrode (360) and a second gate electrode (365) on the gate insulating layer (350) such that the first gate electrode (360) and the second gate electrode (365) correspond to a first channel region (330c) of the first semiconductor layer (330) and a second channel region (335c) of the second semiconductor layer (335), respectively;
forming a planarization layer (385) on the first gate electrode (360) and the second gate electrode (365);
forming contact holes (387) exposing predetermined regions of first source (330s) and drain (330d) regions of the first semiconductor layer (330) and predetermined regions of second source (335s) and drain (335d) regions of the second semiconductor layer (335) by etching predetermined regions of the planarization layer (385) and the gate insulating layer (320), and exposing predetermined regions of the metal interconnection (310) by etching predetermined regions of the planarization layer (385), the gate insulating layer (350), and the buffer layer (320);
forming a reflective layer (390a) and a transparent layer (390b) on the substrate (300) having the contact holes (387);
forming a first interconnection (392), a second interconnection (393), and a first electrode (391) at the same time by patterning the reflective layer (390a) and the transparent layer (390b), the first interconnection (392) for connecting the metal interconnection (310) with one of the first source (330s) and drain (330d) regions, the second interconnection (393) for connecting the other of the first source (330s) and drain (330d) regions with one of the second source (335s) and drain (335d) regions,
the first electrode (391) connected to the other of the second source (335s) and drain (335d) regions;
forming a pixel defining layer (395) on the substrate (300) having the first interconnection (392), the second interconnection (393), and the first electrode (391) to expose a predetermined region of the first electrode (391) in the opening region (C); and
forming an organic layer (397) having at least an organic emission layer and a second electrode (399) on the exposed region of the first electrode (391).

20. A method of fabricating an OLED, comprising:

forming a metal interconnection (220), a first gate electrode (210), a second gate electrode (215) on a substrate at the same time and forming the metal interconnection (220) in a predetermined distance apart from the first and second gate electrodes (210, 215) on the same layer as the first and second gate electrodes;
forming a gate insulating layer (230) on the metal interconnection, the first gate electrode (210) and the second gate electrode (215);
forming a first semiconductor layer (240) and a second semiconductor layer (245) on the gate insulating layer such that the first gate electrode (210) and the second gate electrode (215) correspond to a first channel region (240c) of the first semiconductor layer (240) and a second channel region (245c) of the second semiconductor layer (215), respectively;
forming a passivation layer (275) on the first semiconductor layer (240) and a second semiconductor layer (245);
forming a planarization layer (280) on the first gate electrode (210) and the second gate electrode (215);
forming contact holes (285) exposing predetermined regions of first source (240s) and drain (240d) regions of the first semiconductor layer (240) and predetermined regions of second source (245s) and drain (245d) regions of the second semiconductor layer (215) by etching predetermined regions of the planarization layer (280) and the passivation layer (275), and exposing predetermined regions of the metal interconnection (220) by etching predetermined regions of the gate insulating layer (230), the planarization layer (280), and the passivation

layer (275);
forming a reflective layer (290a) and a transparent layer (290b) on the substrate (200) having the contact holes (285);
forming a first interconnection (292), a second interconnection (293), and a first electrode (291) at the same time by patterning the reflective layer (290a) and the transparent layer (290b), the first interconnection (292) for connecting the metal interconnection (220) with one of the first source (240s) and drain (240d) regions, the second interconnection (293) for connecting the other of the first source (240s) and drain (240d) regions with one of the second source (245s) and drain (245d) regions, the first electrode (291) connected to the other of the second source (245s) and drain (245d) regions;
forming a pixel defining layer (295) on the substrate (200) having the first interconnection (292), the second interconnection (293), and the first electrode (291) to expose a predetermined region of the first electrode (291); and
forming an organic layer (297) having at least an organic emission layer and a second electrode (299) on the exposed region of the first electrode (291).

21. The method according to claim 19, wherein forming the first semiconductor layer and the second semiconductor layer comprises:

forming a silicon layer on the buffer layer;
patterning the silicon layer and forming a first silicon pattern and a second silicon pattern;
forming a first photoresist pattern on predetermined regions of the first silicon pattern and the second silicon pattern and implanting first impurity ions at a low concentration;
removing the first photoresist pattern, forming a second photoresist pattern to cover the first silicon pattern to have a greater width than a region of the first silicon pattern covered by the first photoresist pattern and to completely cover the second silicon pattern, and forming a first semiconductor layer having first source and drain regions, LDD regions, and a first channel region by implanting first impurity ions at a high concentration into the first silicon pattern; and
removing the second photoresist pattern, forming a third photoresist pattern to completely cover the first semiconductor layer and cover the same region as the region of the second silicon pattern covered by the first photoresist pattern, and forming a second semiconductor layer having second source and drain regions and a second channel region by implanting second impurity ions at a high concentration.

22. The method according to claim 21, wherein the first impurity ions are n-type impurity ions.

23. The method according to claim 21, wherein the second impurity ions are p-type impurity ions.

Patentansprüche

1. Organische lichtemittierende Anzeigevorrichtung (OLED), aufweisend:

ein Substrat (200, 300), das einen ersten Dünnfilmtransistorbereich (A), einen zweiten Dünnfilmtransistorbereich (B), einen Öffnungsbereich (D) und einen Verbindungsbereich (C) aufweist;
wobei das Substrat (200, 300) weiterhin einen ersten Dünnfilmtransistor (TFT), der im ersten Dünnfilmtransistorbereich (A) angeordnet ist, einen zweiten Dünnfilmtransistor, der im zweiten Dünnfilmtransistorbereich (B) angeordnet ist und eine Metallverbindung (220, 310), die im Verbindungsbereich (C) angeordnet ist, aufweist;
eine Planarisierungsschicht (280, 385), die auf dem Substrat (200, 300), das den ersten Dünnfilmtransistor, den zweiten Dünnfilmtransistor und die Metallverbindung (220, 310) aufweist, angeordnet ist;
eine Vielzahl von Kontaktlöchern (285, 385), die in vorbestimmten Bereichen der Planarisierungsschicht (280, 385) angeordnet sind, um vorbestimmte Bereiche eines ersten Source (240s, 330)- und Drain (240d, 330d)-Gebiets des ersten Dünnfilmtransistors, eines zweiten Source (245s, 335s)- und Drain (245d, 335d)-Gebiets des zweiten Dünnfilmtransistors und der Metallverbindung (220, 310) freizulegen;
eine erste Verbindung (292, 392), die unmittelbar auf der Planarisierungsschicht (280, 385) angeordnet ist, wobei einer der Endabschnitte der ersten Verbindung über die Kontaktlöcher (285, 387) jeweils mit der Metallverbindung (220, 310) und einem des ersten Source (240s, 330s)- und Drain (240d, 330d)-Gebiets in Kontakt steht, so dass die Metallverbindung (220, 320) mit dem einen des ersten Source (240s, 330s)- und Drain (240d, 330d)-Gebiets elektrisch verbunden ist;
eine zweite Verbindung (293), die unmittelbar auf der Planarisierungsschicht (280, 385) angeordnet ist; wobei einer der Endabschnitte der zweiten Verbindung (293) über die Kontaktlöcher (285, 387) jeweils mit dem anderen des ersten Source (240s, 330s)- und Drain (240d, 330d)-Gebiets und einem des zweiten Source

(245s, 335s)- und Drain (245d, 335d)-Gebiets in Kontakt steht, so dass das andere des ersten Source (240s, 330s)- und Drain (240d, 330d)-Gebiets mit dem einen des zweiten Source (245s, 335s)- und Drain (245d, 335d)-Gebiets elektrisch verbunden ist; und
eine erste Elektrode (291, 391), die unmittelbar auf der Planarisierungsschicht (280, 385) angeordnet ist, wobei einer der Endabschnitte der ersten Elektrode (291, 391) über die Kontaktlöcher (285) mit dem anderen des zweiten Source (245s, 335s)- und Drain (245d, 335d)-Gebiets in Kontakt steht.

2. OLED nach Anspruch 1, weiterhin aufweisend:

eine organische Schicht (297, 397), die auf der ersten Elektrode (291, 391) angeordnet ist; und eine zweite Elektrode (299, 399), die auf der organischen Schicht (297, 397) angeordnet ist.

3. OLED nach Anspruch 2, wobei die erste Elektrode (291, 391) eine reflektierende Schicht (290a, 390a) und eine transparente Schicht (290b, 390b) aufweist.

4. OLED nach Anspruch 3, wobei die reflektierende Schicht (290a, 390a) auf einem ausgewählt aus der Gruppe bestehend aus Aluminium (Al), Silber (Ag) und einer Legierung derselben ausgebildet ist.

5. OLED nach Anspruch 3, wobei die transparente Schicht (290b, 390b) aus einem aus Indiumzinnoxid (ITO) und Indiumzinkoxid (IZO) ausgebildet ist.

6. OLED nach Anspruch 1, wobei die erste Verbindung (292, 392) und die zweite Verbindung (293, 393) aus dem gleichen Material wie die erste Elektrode (291, 391) ausgebildet sind.

7. OLED nach Anspruch 1, wobei eine erste Gate-Elektrode (210, 360) des ersten Dünnfilmtransistors, eine zweite Gate-Elektrode (215, 365) des zweiten Dünnfilmtransistors und die Metallverbindung (220, 320) auf derselben Schicht angeordnet sind.

8. OLED nach Anspruch 7, wobei die erste Gate-Elektrode (210, 360), die zweite Gate-Elektrode (215, 365) und die Metallverbindung (220, 320) aus einem ausgewählt aus der Gruppe bestehend aus Molybdän (Mo), Wolfram (W), Aluminium (Al) und einer Legierung derselben ausgebildet sind.

9. OLED nach Anspruch 1, wobei der erste Dünnfilmtransistor aufweist:

eine erste Gate-Elektrode (210), die auf dem Substrat (200) angeordnet ist;
eine Gate-Isolierschicht (230), die auf der ersten Gate-Elektrode (215) angeordnet ist; und
eine erste Halbleiterschicht (240), die auf der Gate-Isolierschicht (240) angeordnet ist, mit der ersten Gate-Elektrode (210) korrespondiert und das erste Source (240s)- und Drain (240d)-Gebiet und ein erstes Kanalgebiet (240c) aufweist, und

wobei der zweite Dünnfilmtransistor aufweist:

eine zweite Gate-Elektrode (215), die auf dem Substrat (200) angeordnet ist;
die Gate-Isolierschicht (230), die auf der zweiten Gate-Elektrode (215) angeordnet ist; und
eine zweite Halbleiterschicht (245), die auf der Gate-Isolierschicht (230) angeordnet ist, mit der zweiten Gate-Elektrode (215) korrespondiert und das zweite Source (245s)- und Drain (245d)-Gebiet und ein zweites Kanalgebiet (245c) aufweist.

10. OLED nach Anspruch 1, wobei der erste Dünnfilmtransistor aufweist:

eine erste Halbleiterschicht (330), die auf dem Substrat (300) angeordnet ist und das erste Source (330s)- und Drain (335d)-Gebiet und ein erstes Kanalgebiet (330c) aufweist;
eine Gate-Isolierschicht (350), die auf der ersten Halbleiterschicht (330) angeordnet ist; und
eine erste Gate-Elektrode (360), die auf der Gate-Isolierschicht (350) angeordnet ist und mit dem ersten Kanalgebiet (330c) korrespondiert, und wobei der zweite Dünnfilmtransistor aufweist:

eine zweite Halbleiterschicht (335), die auf dem Substrat (300) angeordnet ist und das zweite Source (335s)- und Drain-Gebiet (335d) und ein zweites Kanalgebiet (335c) aufweist;
die Gate-Isolierschicht (350), die auf der zweiten Halbleiterschicht (335) angeordnet ist; und
eine zweite Gate-Elektrode (365), die auf der Gate-Isolierschicht (350) angeordnet ist und mit dem zweiten Kanalgebiet (335c) korrespondiert.

11. OLED nach Anspruch 9 oder 10, weiterhin aufweisend leicht dotierte Drain (LDD)-Gebiete (240e, 330e), wobei die leicht dotierten Drain-Gebiete (240e, 330e) zwischen dem ersten Source-Gebiet (240s, 330s) und dem Kanalgebiet (240c, 330c) und zwischen dem Drain-Gebiet (240d, 330d) und dem Kanalgebiet (240c, 330c) des ersten Dünnfilmtransistors angeordnet sind.

12. OLED nach Anspruch 9, wobei die Gate-Isolierschicht (230) auf der Metallverbindung (220), der ersten Gate-Elektrode (210) und der zweiten Gate-Elektrode (215) angeordnet ist;
eine Pixeldefinitionsschicht (295) auf der ersten Verbindung (292), der zweiten Verbindung (293) und der ersten Elektrode (291) angeordnet ist und einen vorbestimmten Bereich der ersten Elektrode (291) freilegt; und
eine organische Schicht (297) und eine zweite Elektrode (299) auf dem freiliegenden Bereich der ersten Elektrode (291) angeordnet sind, wobei die organische Schicht (297) zumindest eine organische Emissionsschicht aufweist; wobei die Gate-Isolierschicht (230) auf der Metallverbindung (220), der ersten Gate-Elektrode (210) und der zweiten Gate-Elektrode (215) angeordnet ist.

13. OLED nach Anspruch 12, wobei die Metallverbindung (220), die erste Gate-Elektrode (210) und die zweite Gate-Elektrode (215) aus dem gleichen Material ausgebildet sind.

14. OLED nach Anspruch 12, weiterhin aufweisend LDD-Gebiete (240e), die zwischen dem ersten Source (240s)- und Drain (240d)-Gebiet und dem ersten Kanalgebiet oder zwischen dem zweiten Source (245s)- und Drain-Gebiet (245d) und dem zweiten Kanalgebiet angeordnet sind.

15. OLED nach Anspruch 12, wobei die erste Verbindung (292), die zweite Verbindung (293) und die erste Elektrode (291) eine reflektierende Schicht und eine transparente Schicht aufweisen.

16. OLED nach Anspruch 10, weiterhin aufweisend:

eine Pufferschicht (320), die auf der Metallverbindung (310) angeordnet ist; wobei die erste Halbleiterschicht (340) und die zweite Halbleiterschicht (345) auf der Pufferschicht (320) angeordnet sind;
eine Pixeldefinitionsschicht (395), die auf der ersten Verbindung (392), der zweiten Verbindung (393) und der ersten Elektrode (391) angeordnet ist und einen vorbestimmten Bereich der ersten Elektrode freilegt; und
eine organische Schicht (397) und eine zweite Elektrode (399), die auf dem freiliegenden Bereich der ersten Elektrode (391) angeordnet sind, wobei die organische Schicht (397) zumindest eine organische Emissionsschicht aufweist.

17. OLED nach Anspruch 16, weiterhin aufweisend LDD-Gebiete (340e), die zwischen dem ersten Source (340s)- und Drain (340d)-Gebiet und dem ersten Kanalgebiet (340c) oder zwischen dem zweiten Source (345s)- und Drain (345d)-Gebiet und dem zweiten Kanalgebiet (340c) angeordnet sind.

18. OLED nach Anspruch 16, wobei die erste Verbindung (392), die zweite Verbindung (393) und die erste Elektrode (391) eine reflektierende Schicht und eine transparente Schicht aufweisen.

19. Verfahren zur Herstellung einer OLED, aufweisend:

Bereitstellen eines Substrats (300), das einen ersten Dünnfilmtransistorbereich (A), einen zweiten Dünnfilmtransistorbereich (B), einen Öffnungsbereich (C) und einen Verbindungsbereich (D) aufweist;
Ausbilden einer Metallverbindung (310) im Verbindungsbereich (D);
Ausbilden einer Pufferschicht (320) auf der Metallverbindung (310) und auf dem Substrat (300);
Ausbilden einer ersten Halbleiterschicht (330) und einer zweiten Halbleiterschicht (335) auf der Pufferschicht (320);
Ausbilden einer Gate-Isolierschicht (350) auf der ersten Halbleiterschicht (330) und der zweiten Halbleiterschicht (335);
Ausbilden einer ersten Gate-Elektrode (360) und einer zweiten Gate-Elektrode (365) auf der Gate-Isolierschicht (350) derart, dass die erste Gate-Elektrode (360) und die zweite Gate-Elektrode (365) jeweils mit einem ersten Kanalgebiet (330c) der ersten Halbleiterschicht (330) und einem zweiten Kanalgebiet (335c) der zweiten Halbleiterschicht (335) korrespondieren;
Ausbilden einer Planarisierungsschicht (385) auf der ersten Gate-Elektrode (360) und der zweiten Gate-Elektrode (365);
Ausbilden von Kontaktlöchern (387), die vorbestimmte Bereiche des ersten Source (330s)- und Drain (330d)-Gebiets der ersten Halbleiterschicht (330) und vorbestimmte Bereiche des zweiten Source (335s)- und Drain (335d)- Gebiets der zweiten Halbleiterschicht (335) durch Ätzen vorbestimmter Bereiche der Planarisierungsschicht (385) und der Gate-Isolierschicht (320) freilegen und die vorbestimmte Bereiche der Metallverbindung (310) durch Ätzen vorbestimmter Bereiche der Planarisierungsschicht (385), der Gate-Isolierschicht (350) und der Pufferschicht (320) freilegen;
Ausbilden einer reflektierenden Schicht (390a) und einer transparenten Schicht (390b) auf dem Substrat (300), das die Kontaktlöcher (387) aufweist;
gleichzeitiges Ausbilden einer ersten Verbindung (392), einer zweiten Verbindung (393) und einer ersten Elektrode (391) durch Strukturieren der reflektierenden Schicht (390a) und der

transparenten Schicht (390b), wobei die erste Verbindung (392) zum Verbinden der Metallverbindung (310) mit einem des ersten Source (330s)- und Drain (330d)-Gebiets dient, die zweite Verbindung (393) zum Verbinden des anderen des ersten Source (330s) und Drain (330d)-Gebiets mit einem des zweiten Source (335s)- und Drain (335d)-Gebiets dient,
und wobei die erste Elektrode (391) mit dem anderen des zweiten Source (335s)-und Drain (335d)-Gebiets verbunden wird;
Ausbilden einer Pixeldefinitionsschicht (395) auf dem Substrat (300), das die erste Verbindung (392), die zweite Verbindung (393) und die erste Elektrode (391) aufweist, um einen vorbestimmten Bereich der ersten Elektrode (391) im Öffnungsbereich (C) freizulegen; und
Ausbilden einer organischen Schicht (397), die zumindest eine organische Emissionsschicht aufweist, und eine zweite Elektrode (399) auf dem freiliegenden Bereich der ersten Elektrode (391).

20. Verfahren zur Herstellung einer OLED, aufweisend:

gleichzeitiges Ausbilden einer Metallverbindung (220), einer ersten Gate-Elektrode (210), einer zweiten Gate-Elektrode (215) auf einem Substrat und Ausbilden der Metallverbindung (220) in einem vorbestimmten Abstand zur ersten und zweiten Gate-Elektrode auf derselben Schicht wie die erste und zweite Gate-Elektrode;
Ausbilden einer Gate-Isolierschicht (230) auf der Metallverbindung, der ersten Gate-Elektrode (210) und der zweiten Gate-Elektrode (215);
Ausbilden einer ersten Halbleiterschicht (240) und einer zweiten Halbleiterschicht (245) auf der Gate-Isolierschicht derart, dass die erste Gate-Elektrode (210) und die zweite Gate-Elektrode (215) jeweils mit einem ersten Kanalgebiet (240c) der ersten Halbleiterschicht (240) und einem zweiten Kanalgebiet (245c) der zweiten Halbleiterschicht (215) korrespondieren;
Ausbilden einer Passivierungsschicht (275) auf der ersten Halbleiterschicht (240) und einer zweiten Halbleiterschicht (245);
Ausbilden einer Planarisierungsschicht (280) auf der ersten Gate-Elektrode (210) und der zweiten Gate-Elektrode (215);
Ausbilden von Kontaktlöchern (285), die vorbestimmte Bereiche des ersten Source (240s)- und Drain (240d)-Gebiets der ersten Halbleiterschicht (240) und vorbestimmte Bereiche des zweiten Source (245s)- und Drain (245d)-Gebiets der zweiten Halbleiterschicht (215) durch Ätzen vorbestimmter Bereiche der Planarisierungsschicht (280) und der Passivierungsschicht (275) freilegen, und die vorbestimmte Bereiche der Metallverbindung (220) durch Ätzen vorbestimmter Bereiche der Gate-Isolierschicht (230), der Planarisierungsschicht (280) und der Passivierungsschicht (275) freilegen;
Ausbilden einer reflektierenden Schicht (290a) und einer transparenten Schicht (290b) auf dem Substrat (200), das die Kontaktlöcher (285) aufweist;
gleichzeitiges Ausbilden einer ersten Verbindung (292), einer zweiten Verbindung (293) und einer ersten Elektrode (291) durch Strukturieren der reflektierenden Schicht (290a) und der transparenten Schicht (290b), wobei die erste Verbindung (292) zum Verbinden der Metallverbindung (220) mit einem des ersten Source (240s)- und Drain (240d)-Gebiets dient, die zweite Verbindung (293) zum Verbinden des anderen des ersten Source (240s)- und Drain (240d)-Gebiets mit einem des zweiten Source (245s)- und Drain (245d)-Gebiets dient,
und wobei die erste Elektrode (291) mit dem anderen des zweiten Source (245s)- und Drain (245d)-Gebiets verbunden wird;
Ausbilden einer Pixeldefinitionsschicht (295) auf dem Substrat (200), das die erste Verbindung (292), die zweite Verbindung (293) und die erste Elektrode (291) aufweist, um einen vorbestimmten Bereich der ersten Elektrode (291) freizulegen; und
Ausbilden einer organischen Schicht (297), die zumindest eine organische Emissionsschicht aufweist, und eine zweite Elektrode (299) auf dem freiliegenden Bereich der ersten Elektrode (291).

21. Verfahren nach Anspruch 19, wobei das Ausbilden der ersten Halbleiterschicht und der zweiten Halbleiterschicht aufweist:

Ausbilden einer Siliziumschicht auf der Pufferschicht;
Strukturieren der Siliziumschicht und Ausbilden eines ersten Siliziummusters und eines zweiten Siliziummusters;
Ausbilden eines ersten Fotolackmusters auf vorbestimmten Bereichen des ersten Siliziummusters und des zweiten Siliziummusters und Implantieren erster Verunreinigungsionen mit einer niedrigen Konzentration;
Entfernen des ersten Fotolackmusters, Ausbilden eines zweiten Fotolackmusters, das das erste Siliziummuster bedeckt und das eine größere Breite als ein Bereich des mit dem ersten Fotolackmuster bedeckten ersten Siliziummusters aufweist und das das zweite Siliziummuster vollständig bedeckt; und Ausbilden einer ersten Halbleiterschicht, die ein erstes Source- und Drain-Gebiet, LDD-Gebiete und ein erstes Ka-

nalgebiet aufweist, durch Implantieren erster Verunreinigungsionen mit einer hohen Konzentration in das erste Siliziummuster; und
Entfernen des zweiten Fotolackmusters, Ausbilden eines dritten Fotolackmusters, das die erste Halbleiterschicht vollständig bedeckt und das denselben Bereich wie der Bereich des mit dem ersten Fotolackmusters bedeckten zweiten Siliziummusters bedeckt, und Ausbilden einer zweiten Halbleiterschicht, die ein zweites Source- und Drain-Gebiet und ein zweites Kanalgebiet aufweist, durch Implantieren zweiter Verunreinigungsionen mit einer hohen Konzentration.

22. Verfahren nach Anspruch 21, wobei die ersten Verunreinigungsionen n-Typ-Verunreinigungsionen sind.

23. Verfahren nach Anspruch 21, wobei die zweiten Verunreinigungsionen p-Typ-Verunreinigungsionen sind.

Revendications

1. Dispositif d'affichage électroluminescent organique (OLED) comprenant :

un substrat (200, 300) ayant une première région TFT (A), une deuxième région TFT (B), une région d'ouverture (D), et une région d'interconnexion (C) ;
le substrat (200, 300) ayant en outre un premier transistor à couches minces (TFT) agencé dans la première région TFT (A), un deuxième TFT agencé dans la deuxième région TFT (B), et une interconnexion métallique (220, 310) agencée dans la région d'interconnexion (C) ;
une couche de planarisation (280, 385) disposée sur le substrat (200, 300) ayant le premier TFT, le deuxième TFT, et l'interconnexion métallique (220, 310) ;
une pluralité de trous de contact (285, 385) disposés dans des régions prédéterminées de la couche de planarisation (280, 385) pour exposer des régions prédéterminées parmi des premières régions de source (240s, 330s) et de drain (240d, 330d) du premier TFT, des deuxièmes régions de source (245s, 335s) et de drain (245d, 335d) du deuxième TFT, et l'interconnexion métallique (220, 310) ;
une première interconnexion (292, 392) disposée directement sur la couche de planarisation (280, 385), l'une des parties d'extrémité de la première interconnexion étant en contact avec l'interconnexion métallique (220, 310) et l'une des premières régions de source (240s, 330s) et de drain (240d, 330d) respectivement à travers les trous de contact (285, 387), reliant ainsi électriquement l'interconnexion métallique (220, 320) à l'une des premières régions de source (240s, 330s) et de drain (240d, 330d) ;
une deuxième interconnexion (293) disposée directement sur la couche de planarisation (280, 385) ; l'une des parties d'extrémité de la deuxième interconnexion (293) étant en contact avec l'autre des premières régions de source (240s, 330s) et de drain (240d, 330d) et l'une des deuxièmes régions de source (245s, 335s) et de drain (245d, 335d) respectivement à travers les trous de contact (285, 387), reliant ainsi électriquement l'autre des premières régions de source (240s, 330s) et de drain (240d, 330d) à l'une des deuxièmes régions de source (245s, 335s) et de drain (245d, 335d) ; et
une première électrode (291, 391) disposée directement sur la couche de planarisation (280, 385), l'une des parties d'extrémité de la première électrode (291, 391) étant en contact avec l'autre des deuxièmes régions de source (245s, 335s) et de drain (245d, 335d) à travers les trous de contact (285).

2. OLED selon la revendication 1, comprenant en outre :

une couche organique (297, 397) disposée sur la première électrode (291, 391) ; et une deuxième électrode (299, 399) disposée sur la couche organique (297, 397).

3. OLED selon la revendication 2, dans lequel la première électrode (291, 391) comporte une couche réfléchissante (290a, 390a) et une couche transparente (290b, 390b).

4. OLED selon la revendication 3, dans lequel la couche réfléchissante (290a, 390a) est formée d'un élément choisi dans le groupe constitué de l'aluminium (Al), de l'argent (Ag), et d'un alliage de ceux-ci.

5. OLED selon la revendication 3, dans lequel la couche transparente (290b, 390b) est formée de l'un de l'oxyde d'indium-étain (ITO) et de l'oxyde d'indium-zinc (IZO).

6. OLED selon la revendication 1, dans lequel la première interconnexion (292, 392) et la deuxième interconnexion (293, 393) sont formées du même matériau que la première électrode (291, 391).

7. OLED selon la revendication 1, dans lequel une première électrode de grille (210, 360) du premier TFT, une deuxième électrode de grille (215, 365) du deuxième TFT, et l'interconnexion métallique (220, 320) sont disposées sur la même couche.

8. OLED selon la revendication 7, dans lequel la première électrode de grille (210, 360), la deuxième électrode de grille (215, 365), et l'interconnexion métallique (220, 320) sont formées d'un élément choisi dans le groupe constitué du molybdène (Mo), du tungstène (W), de l'aluminium (Al), et d'un alliage de ceux-ci.

9. OLED selon la revendication 1, dans lequel le premier TFT comprend :

une première électrode de grille (210) disposée sur le substrat (200) ;
une couche isolante de grille (230) disposée sur la première électrode de grille (215) ; et
une première couche semi-conductrice (240) disposée sur la couche isolante de grille (240), correspondant à la première électrode de grille (210), et comportant les premières régions de source (240s) et de drain (240d) et une première région de canal (240c), et

dans lequel le deuxième TFT comprend :

une deuxième électrode de grille (215) disposée sur le substrat (200) ;
la couche isolante de grille (230) disposée sur la deuxième électrode de grille (215) ; et
une deuxième couche semi-conductrice (245) disposée sur la couche isolante de grille (230), correspondant à la deuxième électrode de grille (215), et comportant les deuxièmes régions de source (245s) et de drain (245d) et une deuxième région de canal (245c).

10. OLED selon la revendication 1, dans lequel le premier TFT comprend :

une première couche semi-conductrice (330) disposée sur le substrat (300) et comportant les premières régions de source (330s) et de drain (335d) et une première région de canal (330c) ;
une couche isolante de grille (350) disposée sur la première couche semi-conductrice (330) ; et
une première électrode de grille (360) disposée sur la couche isolante de grille (350) et correspondant à la première région de canal (330c), et

dans lequel le deuxième TFT comprend :

une deuxième couche semi-conductrice (335) disposée sur le substrat (300) et comportant les deuxièmes régions de source (335s) et de drain (335d) et une deuxième région de canal (335c) ;
la couche isolante de grille (350) disposée sur la deuxième couche semi-conductrice (335) ; et
une deuxième électrode de grille (365) disposée sur la couche isolante de grille (350) et correspondant à la deuxième région de canal (335c).

11. OLED selon la revendication 9 ou 10, comprenant en outre des régions de drain légèrement dopées (LDD) (240e, 330e), où les régions de drain légèrement dopées (240e, 330e) sont interposées entre la première région de source (240s, 330s) et la région de canal (240c, 330c) et entre la région de drain (240d, 330d) et la région de canal (240c, 330c) du premier TFT.

12. OLED selon la revendication 9, dans lequel la couche isolante de grille (230) est disposée sur l'interconnexion métallique (220), la première électrode de grille (210), et la deuxième électrode de grille (215) ;
une couche de définition de pixels (295) est disposée sur la première interconnexion (292), la deuxième interconnexion (293), et la première électrode (291) expose une région prédéterminée de la première électrode (291) ; et
une couche organique (297) et une deuxième électrode (299) sont disposée sur la région exposée de la première électrode (291), la couche organique (297) comportant au moins une couche d'émission organique ; où la couche isolante de grille (230) est disposée sur l'interconnexion métallique (220), la première électrode de grille (210), et la deuxième électrode de grille (215).

13. OLED selon la revendication 12, dans lequel l'interconnexion métallique (220), la première électrode de grille (210), et la deuxième électrode de grille (215) sont formées du même matériau.

14. OLED selon la revendication 12, comprenant en outre des régions LDD (240e) disposées entre les premières régions de source (240s) et de drain (240d) et la première région de canal ou entre les deuxièmes régions de source (245s) et de drain (245d) et la deuxième région de canal.

15. OLED selon la revendication 12, dans lequel la première interconnexion (292), la deuxième interconnexion (293), et la première électrode (291) comportent une couche réfléchissante et une couche transparente.

16. OLED selon la revendication 10, comprenant en outre :

une couche tampon (320) disposée sur l'interconnexion métallique (310) ; la première couche semi-conductrice (340) et la deuxième couche semi-conductrice (345) étant disposées sur la couche tampon (320) ;
une couche de définition de pixels (395) disposée sur la première interconnexion (392), la

deuxième interconnexion (393), et la première électrode (391) et exposant une région prédéterminée de la première électrode ; et
une couche organique (397) et une deuxième électrode (399) disposées sur la région exposée de la première électrode (391), la couche organique (397) comportant au moins une couche d'émission organique.

17. OLED selon la revendication 16, comprenant en outre des régions LDD (340e) disposées entre les premières régions de source (340s) et de drain (340d) et la première région de canal (340c) ou entre les deuxièmes régions de source (345s) et de drain (345d) et la deuxième région de canal (340c).

18. OLED selon la revendication 16, dans lequel la première interconnexion (392), la deuxième interconnexion (393), et la première électrode (391) comportent une couche réfléchissante et une couche transparente.

19. Procédé de fabrication d'un OLED, comprenant le fait :

de fournir un substrat (300) ayant une première région TFT (A), une deuxième région TFT (B), une région d'ouverture (C) et une région d'interconnexion (D) ;
de former une interconnexion métallique (310) dans la région d'interconnexion (D) ;
de former une couche tampon (320) sur l'interconnexion métallique (310) et sur le substrat (300) ;
de former une première couche semi-conductrice (330) et une deuxième couche semi-conductrice (335) sur la couche tampon (320) ;
de former une couche isolante de grille (350) sur la première couche semi-conductrice (330) et la deuxième couche semi-conductrice (335) ;
de former une première électrode de grille (360) et une deuxième électrode de grille (365) sur la couche isolante de grille (350) de sorte que la première électrode de grille (360) et la deuxième électrode de grille (365) correspondent à une première région de canal (330c) de la première couche semi-conductrice (330) et une deuxième région de canal (335c) de la deuxième couche semi-conductrice (335), respectivement ;
de former une couche de planarisation (385) sur la première électrode de grille (360) et la deuxième électrode de grille (365) ;
de former des trous de contact (387) exposant des régions prédéterminées de premières régions de source (330s) et de drain (330d) de la première couche semi-conductrice (330) et des régions prédéterminées de deuxièmes régions de source (335s) et de drain (335d) de la deuxième couche semi-conductrice (335) en gravant des régions prédéterminées de la couche de planarisation (385) et de la couche isolante de grille (320), et exposant des régions prédéterminées de l'interconnexion métallique (310) en gravant de régions prédéterminées de la couche de planarisation (385), de la couche isolante de grille (350), et de la couche tampon (320) ;
de former une couche réfléchissante (390a) et une couche transparente (390b) sur le substrat (300) ayant les trous de contact (387) ;
de former une première interconnexion (392), une deuxième interconnexion (393), et une première électrode (391) en même temps en formant un motif sur la couche réfléchissante (390a) et la couche transparente (390b), la première interconnexion (392) étant destinée à relier l'interconnexion métallique (310) à l'une des premières régions de source (330s) et de drain (330d), la deuxième interconnexion (393) étant destinée à relier l'autre des premières régions de source (330s) et de drain (330d) à l'une des deuxièmes régions de source (335s) et de drain (335d), la première électrode (391) étant reliée à l'autre des deuxièmes régions de source (335s) et de drain (335d) ;
de former une couche de définition de pixels (395) sur le substrat (300) ayant la première interconnexion (392), la deuxième interconnexion (393), et la première électrode (391) pour exposer une région prédéterminée de la première électrode (391) dans la région d'ouverture (C) ; et
de former une couche organique (397) ayant au moins une couche d'émission organique et une deuxième électrode (399) sur la région exposée de la première électrode (391).

20. Procédé de fabrication d'un OLED, comprenant le fait :

de former une interconnexion métallique (220), une première électrode de grille (210), une deuxième électrode de grille (215) sur un substrat en même temps et de former l'interconnexion métallique (220) à une distance prédéterminée des première et deuxième électrodes de grille sur la même couche que les première et deuxième électrodes de grille ;
de former une couche isolante de grille (230) sur l'interconnexion métallique, la première électrode de grille (210) et la deuxième électrode de grille (215) ;
de former une première couche semi-conductrice (240) et une deuxième couche semi-conductrice (245) sur la couche isolante de grille de sorte que la première électrode de grille (210) et la deuxième électrode de grille (215) corres-

pondent à une première région de canal (240c) de la première couche semi-conductrice (240) et à une deuxième région de canal (245c) de la deuxième couche semi-conductrice (215), respectivement ;
de former une couche de passivation (275) sur la première couche semi-conductrice (240) et une deuxième couche semi-conductrice (245) ;
de former une couche de planarisation (280) sur la première électrode de grille (210) et la deuxième électrode de grille (215) ;
de former des trous de contact (285) exposant des régions prédéterminées de premières régions de source (240s) et de drain (240d) de la première couche semi-conductrice (240) et des régions prédéterminées de deuxièmes régions de source (245s) et de drain (245d) de la deuxième couche semi-conductrice (215) en gravant des régions prédéterminées de la couche de planarisation (280) et de la couche de passivation (275), et exposant des régions prédéterminées de l'interconnexion métallique (220) en gravant des régions prédéterminées de la couche isolante de grille (230), de la couche de planarisation (280) et de la couche de passivation (275) ;
de former une couche réfléchissante (290a) et une couche transparente (290b) sur le substrat (200) ayant les trous de contact (285) ;
de former une première interconnexion (292), une deuxième interconnexion (293), et une première électrode (291) en même temps en formant un motif sur la couche réfléchissante (290a) et la couche transparente (290b), la première interconnexion (292) étant destinée à relier l'interconnexion métallique (220) à l'une des premières régions de source (240s) et de drain (240d), la deuxième interconnexion (293) étant destinée à relier l'autre des premières régions de source (240s) et de drain (240d) à l'une des deuxièmes régions de source (245s) et de drain (245d), la première électrode (291) étant reliée à l'autre des deuxièmes régions de source (245s) et de drain (245d) ;
de former une couche de définition de pixels (295) sur le substrat (200) ayant la première interconnexion (292), la deuxième interconnexion (293), et la première électrode (291) pour exposer une région prédéterminée de la première électrode (291) ; et
de former une couche organique (297) ayant au moins une couche d'émission organique et une deuxième électrode (299) sur la région exposée de la première électrode (291).

21. Procédé selon la revendication 19, dans lequel la formation de la première couche semi-conductrice et de la deuxième couche semi-conductrice comprend le fait :

de former une couche de silicium sur la couche tampon ;
de former un motif sur la couche de silicium et de former un premier motif de silicium et un deuxième motif de silicium ;
de former un premier motif de résine photosensible sur des régions prédéterminées du premier motif de silicium et du deuxième motif de silicium et d'implanter des premiers ions d'impureté à une faible concentration ;
de retirer le premier motif de résine photosensible, de former un deuxième motif de résine photosensible pour couvrir le premier motif de silicium de manière à avoir une largeur supérieure à celle d'une région du premier motif de silicium recouverte par le premier motif de résine photosensible et pour couvrir complètement le deuxième motif de silicium, et de former une première couche semi-conductrice ayant des premières régions de source et de drain, des régions LDD, et une première région de canal en implantant des premiers ions d'impureté à une concentration élevée dans le premier motif de silicium ; et
de retirer le deuxième motif de résine photosensible, de former un troisième motif de résine photosensible pour couvrir complètement la première couche semi-conductrice et pour couvrir la même région que la région du deuxième motif de silicium recouverte par le premier motif de résine photosensible, et de former une deuxième couche semi-conductrice ayant des deuxièmes régions de source et de drain et une deuxième région de canal en implantant des deuxièmes ions d'impureté à une concentration élevée.

22. Procédé selon la revendication 21, dans lequel les premiers ions d'impureté sont des ions d'impureté de type n.

23. Procédé selon la revendication 21, dans lequel les deuxièmes ions d'impureté sont des ions d'impureté de type p.

FIG. 1A

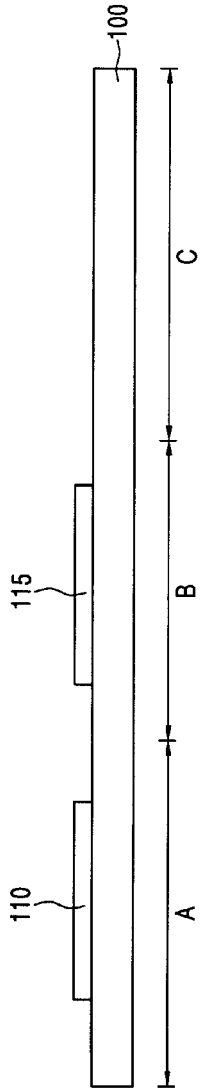


FIG. 1B

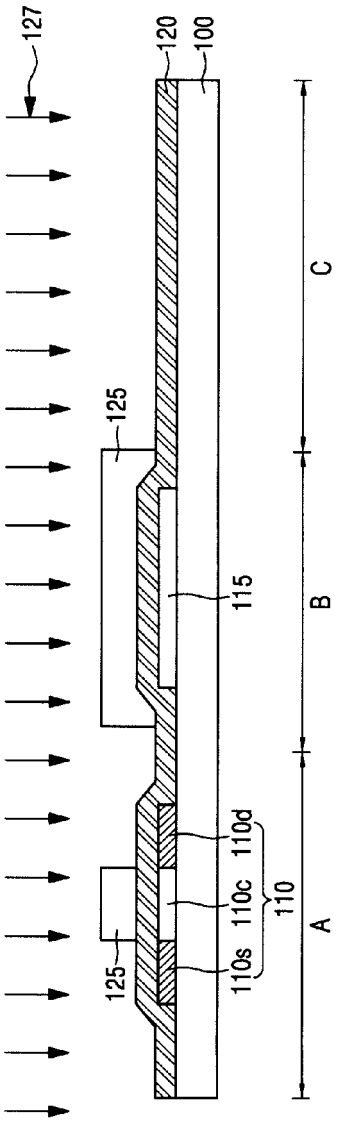


FIG. 1C

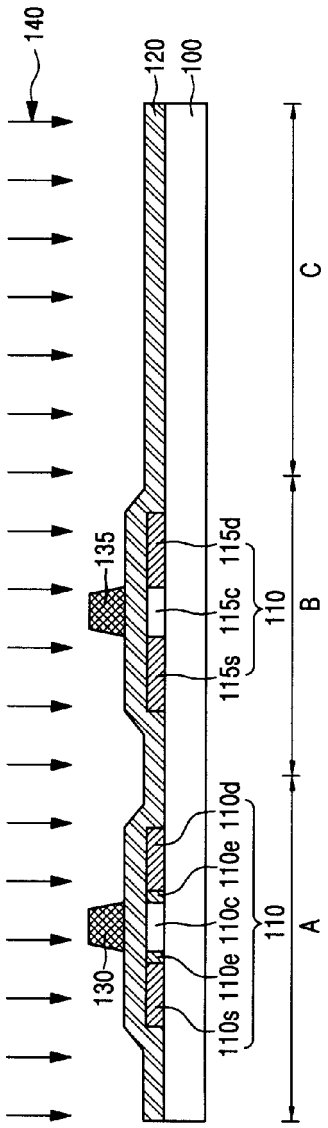

140
120
100
135
115d
115c
115s
110
B
C
110d
110e
110c
110e
110s
110
A
130

FIG. 1D

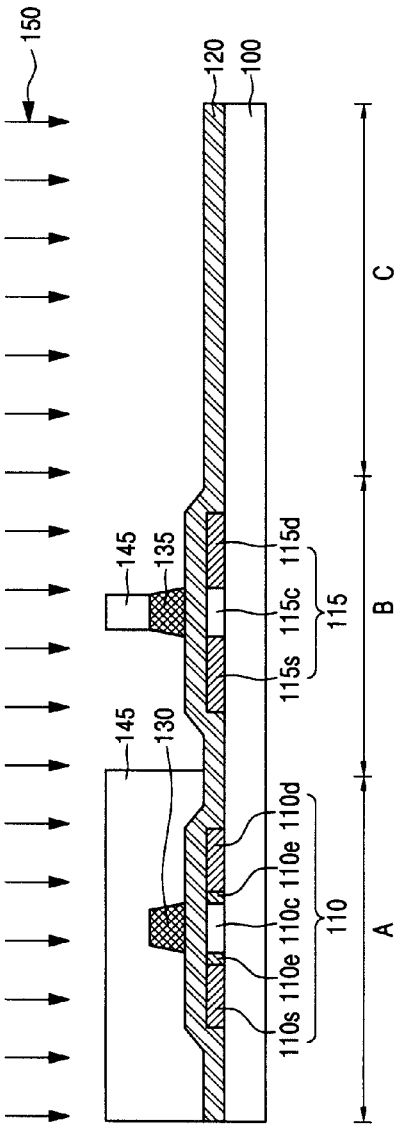

150
120
100
145
135
115d
115c
115
115s
145
130
110d
110e
110c
110e
110s
110
A
B
C

FIG. 1E

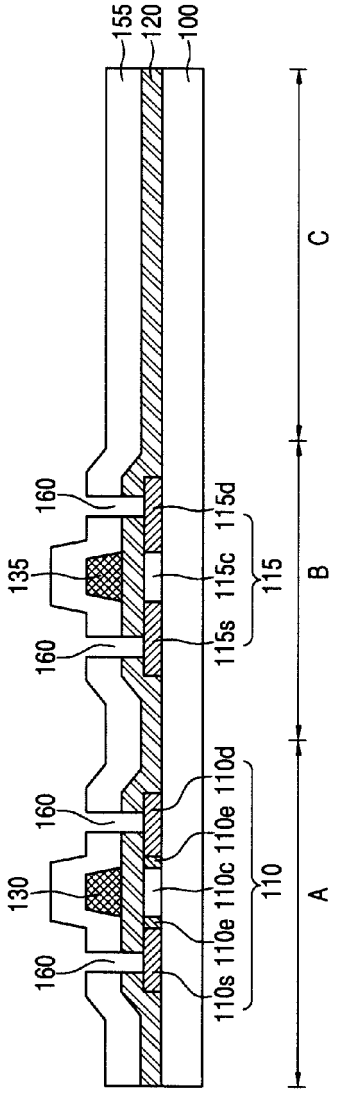

155
120
100
160
135
160
160
130
160
115d
115c
115s
115
110d
110e
110c
110e
110s
110
A
B
C

FIG. 1F

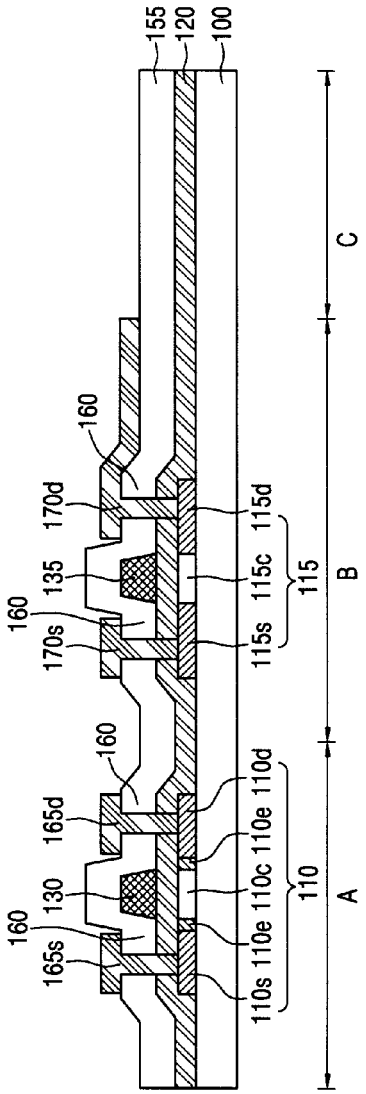

155
120
100
160
170d
135
160
170s
160
165d
130
160
165s
115d
115c
115s
115
110d
110e
110c
110e
110s
110
A
B
C

FIG. 1G

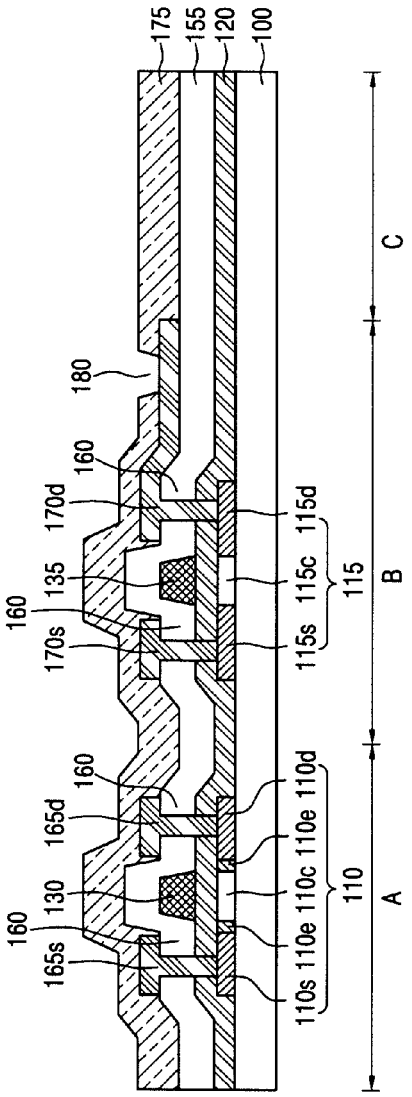

175
155
120
100
180
160
170d
135
160
170s
160
165d
130
160
165s
115d
115c
115s
115
110d
110e
110c
110e
110s
110
A
B
C

FIG. 1H

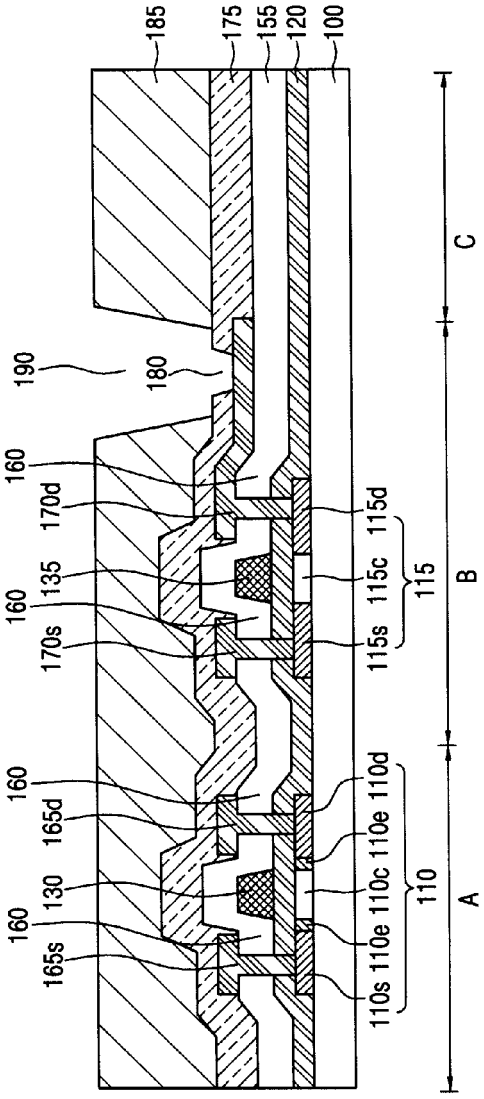

185
175
155
120
100
190
180
160
170d
135
170s
165d
130
165s
115d
115c
115s
115
110d
110e
110c
110e
110s
110
A
B
C

FIG. 11

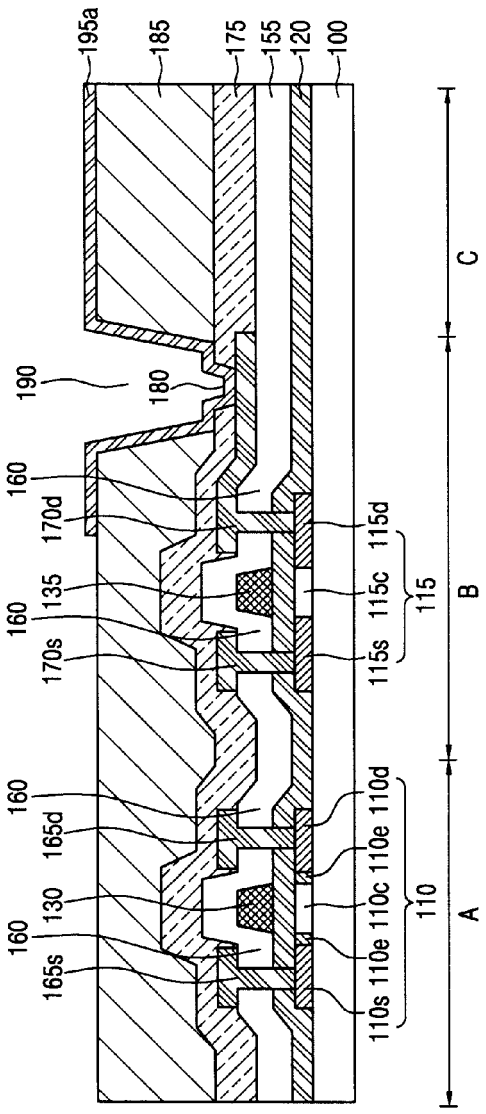

195a
185
175
155
120
100
190
180
160
170d
135
170s
165d
130
165s
115d
115c
115s
115
110d
110e
110c
110e
110s
110
A
B
C

FIG. 1J

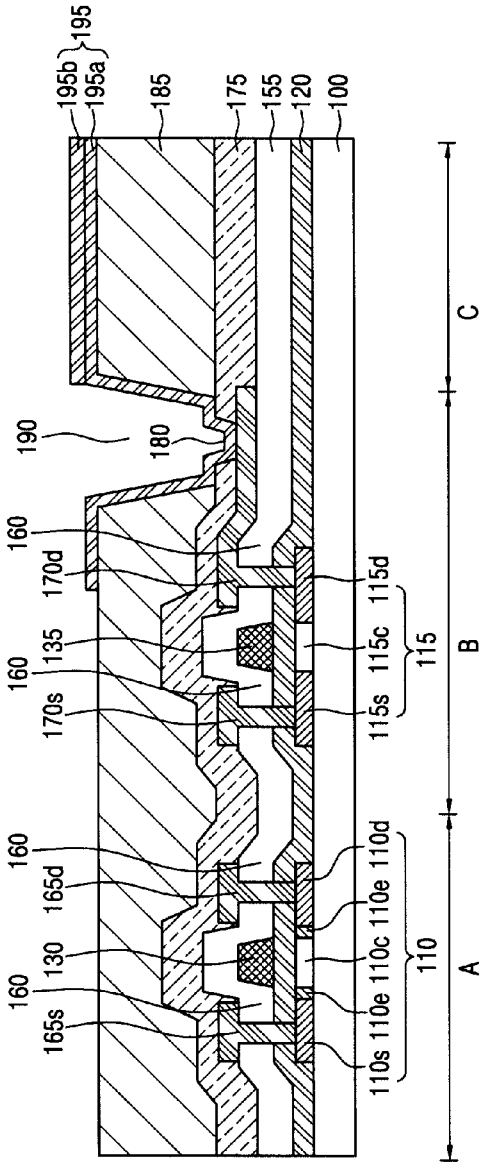

195
195b
195a
185
175
155
120
100
190
180
160
170d
135
170s
165d
130
165s
115d
115c
115s
115
110d
110e
110c
110e
110s
110
A
B
C

FIG. 1K

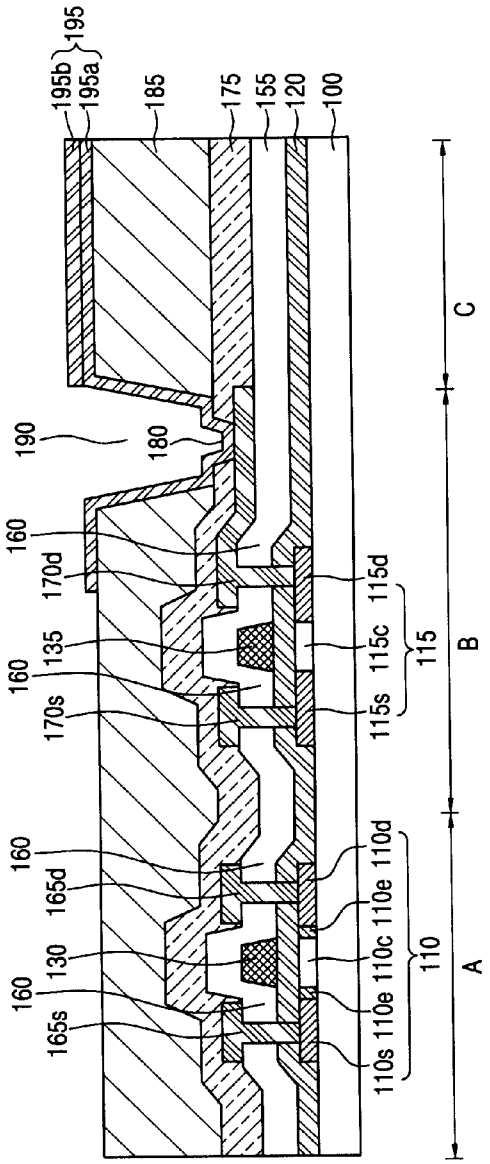

195
195b
195a
185
175
155
120
100
190
180
160
170d
115d
135
115c
115
160
170s
115s
160
165d
110d
130
110e
110c
110
160
165s
110e
110s
C
B
A

FIG. 2A

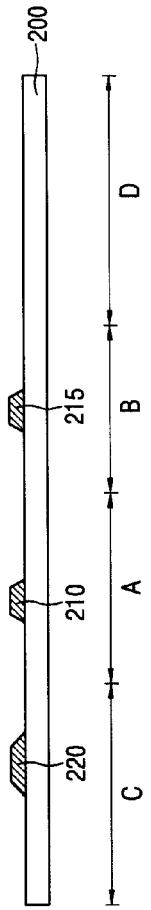


FIG. 2B

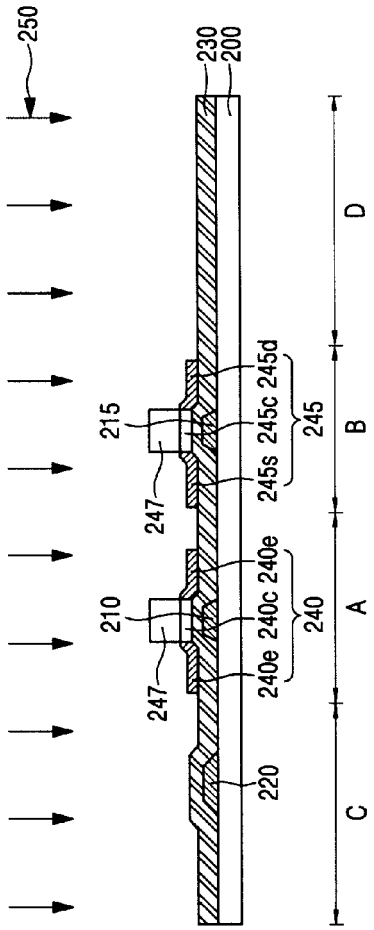

250
230
200
215
247
245d
245c
245s
245
210
240e
240c
240
247
240e
220
D
B
A
C

FIG. 2C

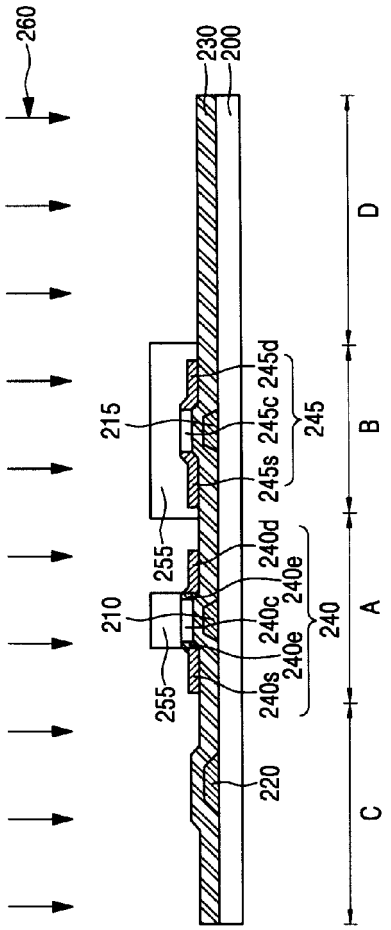

260
230
200
215
245d
245c
245
245s
255
240d
240e
210
240c
240
240e
255
240s
220
D
B
A
C

FIG. 2D

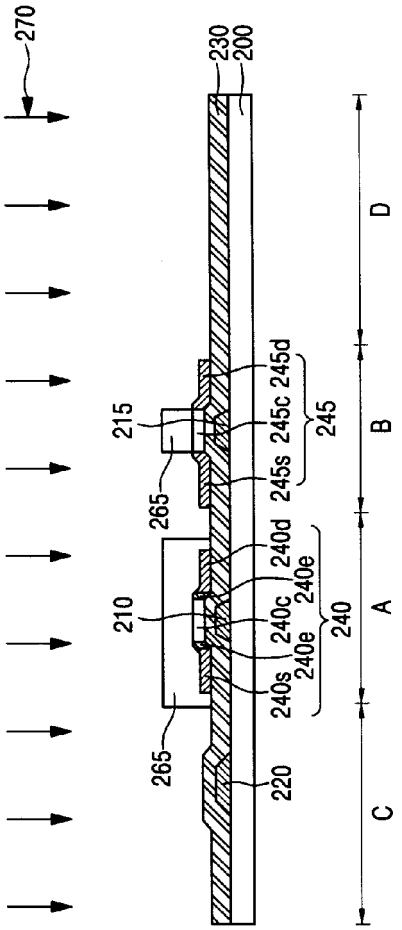

270
230
200
215
265
210
265
220
245d
245c
245s
245
240d
240e
240c
240e
240e
240s
240
A
B
C
D

FIG. 2E

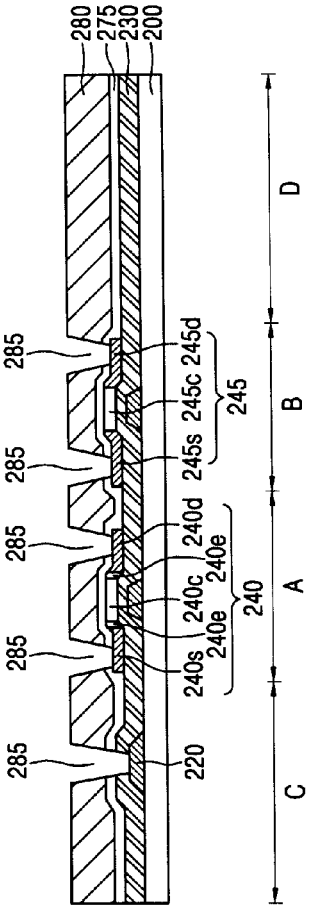

280
275
230
200
285
285
285
285
285
245d
245c
245s
245
240d
240e
240c
240e
240
240s
220
D
B
A
C

FIG. 2F

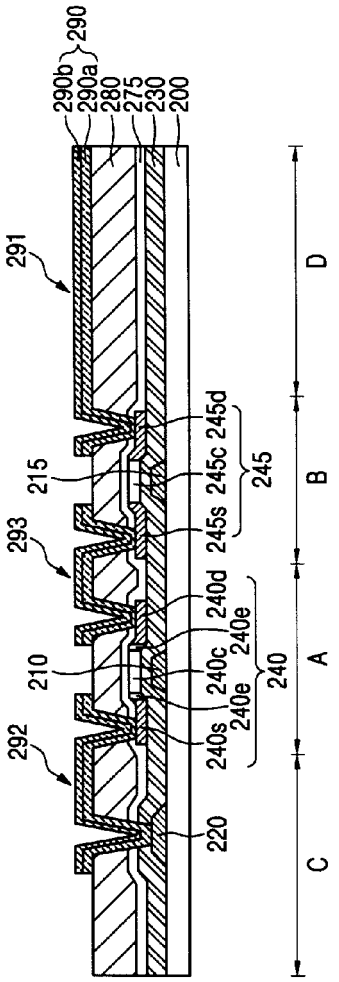

290
290b
290a
280
275
230
200
291
215
293
210
292
220
245d
245c
245s
245
240d
240e
240c
240e
240s
240
A
B
C
D

FIG. 2G

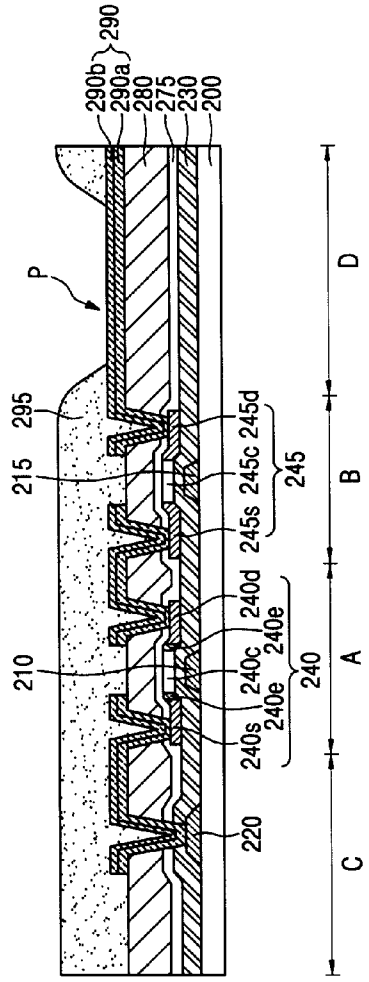

290
290b
290a
280
275
230
200
P
295
215
210
245d
245c
245s
245
240d
240e
240c
240e
240s
240
220
D
B
A
C

FIG. 2H

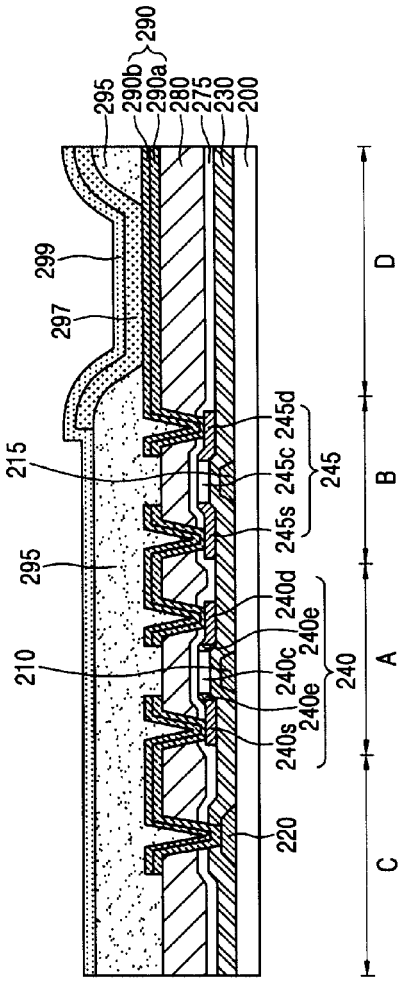

290
290b
290a
295
280
275
230
200
299
297
215
295
210
220
245d
245c
245s
245
240d
240e
240c
240e
240
240s
D
B
A
C

FIG. 3A

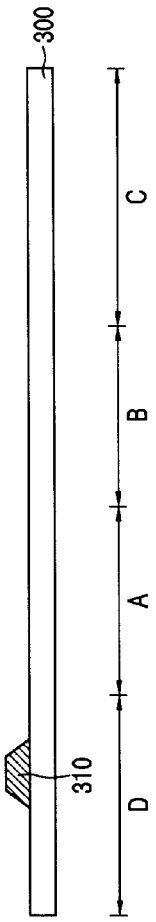


FIG. 3B

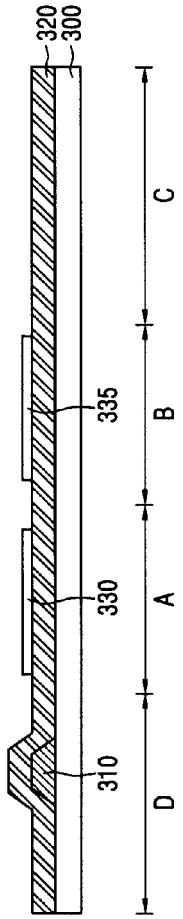


FIG. 3C

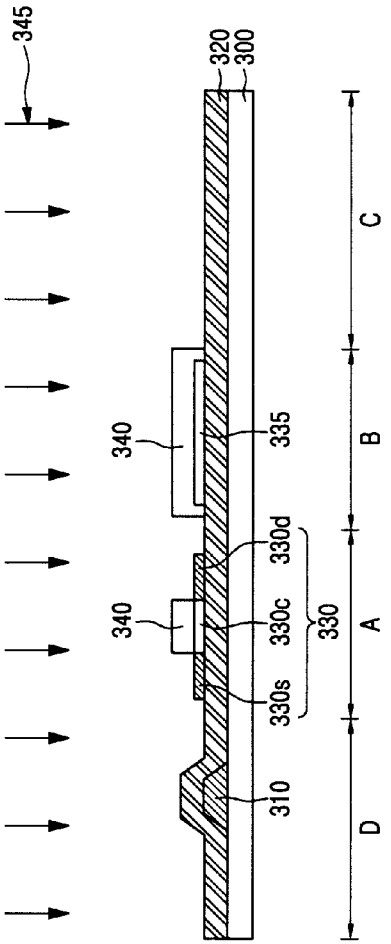


FIG. 3D

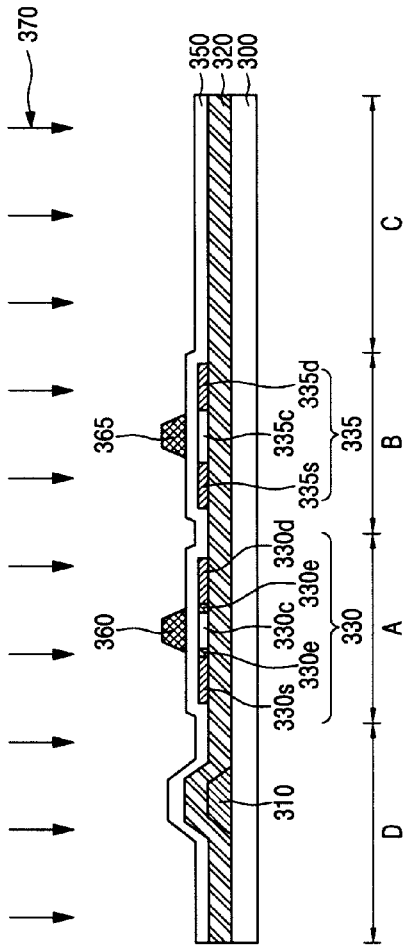

370
350
320
300
365
360
335d
335c
335s
335
330d
330e
330c
330e
330s
330
310
C
B
A
D

FIG. 3E

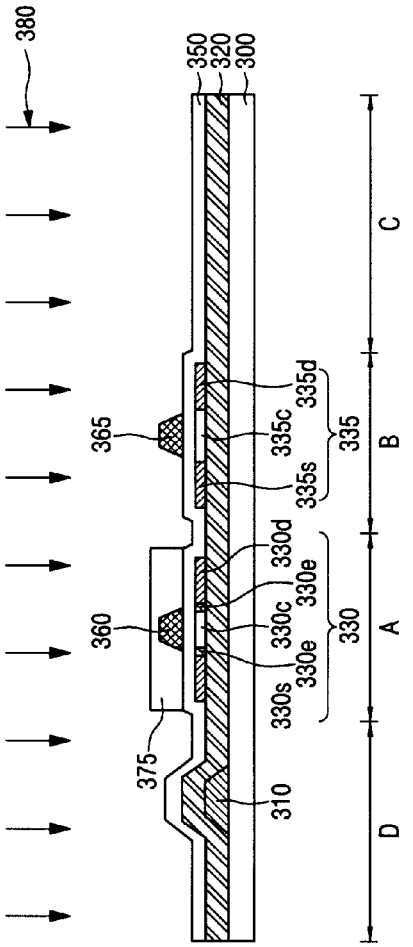

380
350
320
300
365
335d
335c
335s
335
360
330d
330e
330c
330e
330s
330
375
310
C
B
A
D

FIG. 3F

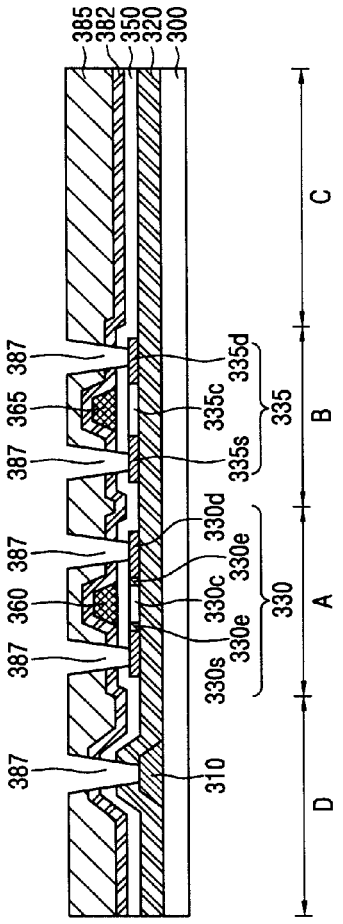

385
382
350
320
300
387
365
387
387
360
387
387
310
335d
335c
335s
335
330d
330e
330c
330e
330s
330e
330
C
B
A
D

FIG. 3G

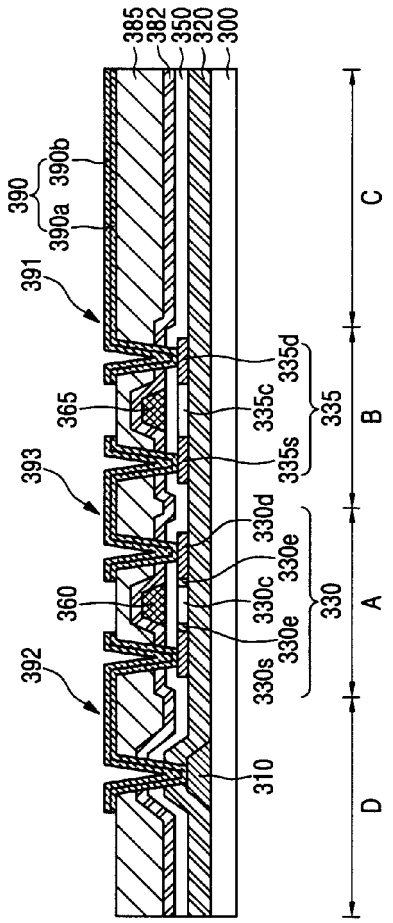

385
382
350
320
300
390
390b
390a
391
365
393
360
392
310
335d
335c
335s
335
330d
330e
330c
330e
330e
330s
330
A
B
C
D

FIG. 3H

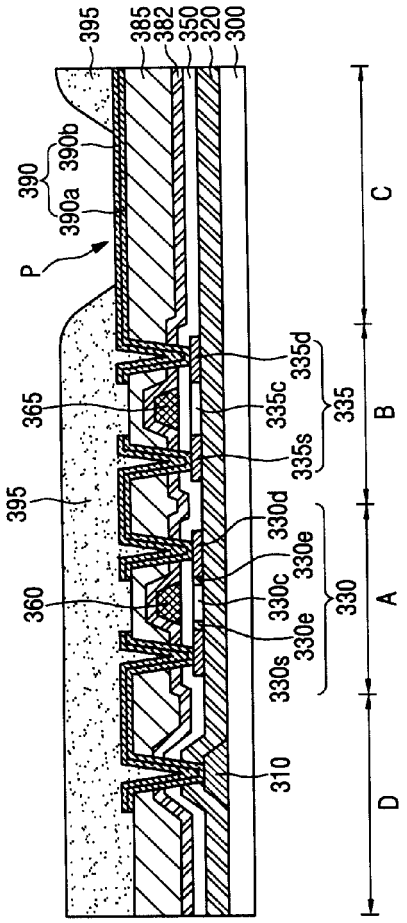
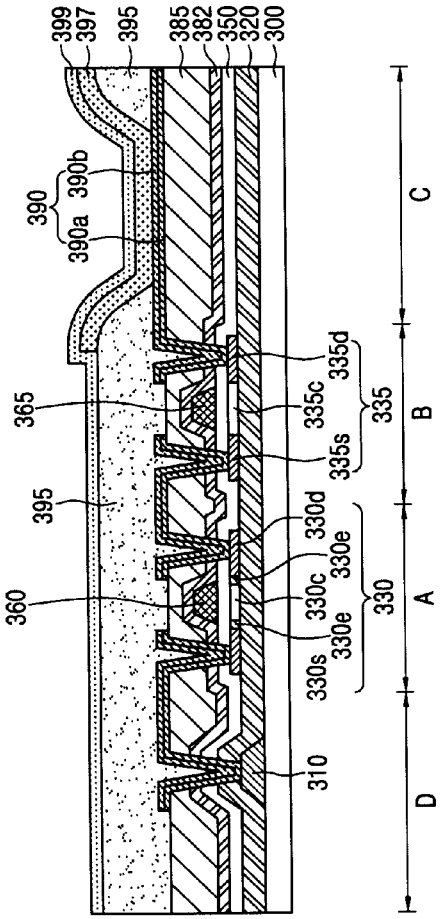

395
385
382
350
320
300
390
390b
390a
P
365
395
360
335d
335c
335s
335
330d
330e
330c
330e
330s
330
310
C
B
A
D

FIG. 3I


399
397
395
385
382
350
320
300
390
390b
390a
365
395
360
335d
335c
335s
335
330d
330e
330c
330e
330s
330
310
C
B
A
D

REFERENCES CITED IN THE DESCRIPTION

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- EP 1331667 A2 **[0028]**
- US 20020104995 A **[0029]**

专利名称(译)	有机发光显示装置及其制造方法		
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[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	HWANG EUI HOON SAMSUNG SDI CO LTD LEE SANG GUL SAMSUNG SDI CO LTD		
发明人	HWANG, EUI-HOON SAMSUNG SDI CO.,LTD. LEE, SANG-GUL SAMSUNG SDI CO., LTD.		
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外部链接	Espacenet		

摘要(译)

提供一种有机发光显示装置（OLED）及其制造方法。当同时形成金属互连（220）和栅电极（210,215）时或者当形成第一电极（290）时，形成用于电连接元件的互连。因此，可以减少使用的掩模的数量，从而可以缩短整个制造工艺并且可以降低生产成本。

FIG. 1A