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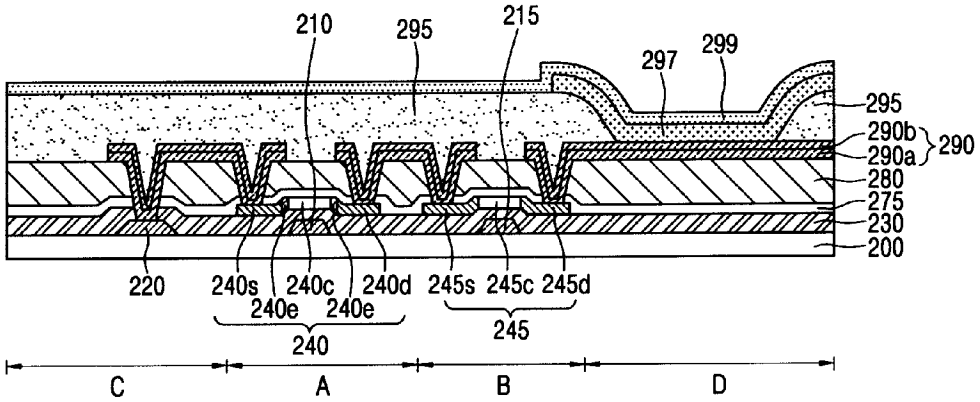
(54) Organic light emitting display device and method of fabricating the same

(57) Provided are an organic light emitting display device (OLED) and a method of fabricating the same. When a metal interconnection (220) and a gate electrode (210,215) are formed at the same time or when a first electrode (290) is formed, interconnections for electrically connecting elements are formed. Thus, the number of used masks can be reduced, so that the overall fabrication process can be shortened and the production cost can be reduced.

FIG. 2H



EP 1 737 056 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an organic light emitting display device (OLED) and a method of fabricating the same, and more particularly, to an OLED in which when a metal interconnection and a gate electrode are formed at the same time or when a first electrode is formed, interconnections for electrically connecting elements are formed, so that an overall fabrication process is shortened and the production cost is reduced by a decrease in the number of used masks.

2. Description of the Related Art

[0002] Among flat panel display devices (FPDs), an organic light emitting display device (OLED) is an emissive device that has a wide viewing angle and a fast response speed of 1 ms or less. Also, the OLED can be fabricated to a small thickness with low cost and has good contrast.

[0003] In the OLED having an organic emission layer (EML) interposed between an anode and a cathode, holes transported from the anode combine with electrons transported from the cathode to form hole-electron pairs, i.e., excitons. Thus, the OLED emits light by energy generated while the excitons transition from an excited state to a ground state.

[0004] In general, since each pixel of the OLED includes a thin film transistor (TFT), a certain current is supplied irrespective of the number of pixels of the OLED, so that the OLED can emit light with stable luminance and consume small power. For this reason, the OLED is quite appropriate for high-resolution large-sized display devices.

[0005] FIGs. 1A through 1K are cross-sectional views illustrating a conventional OLED having a top gate type CMOS TFT and a method of fabricating the same.

[0006] Referring to FIG. 1A, the conventional OLED having a top gate type complementary metal oxide semiconductor (CMOS) TFT includes a substrate 100 having a first TFT region A, a second TFT region B, and an opening region C. An amorphous silicon (a-Si) layer is deposited on the substrate 100, crystallized by a crystallization method, and then patterned using a first mask (not shown), thereby forming a first semiconductor layer 110 and a second semiconductor layer 115.

[0007] Typically, the mask is used to form a photoresist (PR) pattern during a photolithography process. An etching process is performed using the formed PR pattern. Thereafter, the PR pattern is removed by an ashing process using a dry etching process. After the ashing process, the remaining PR is entirely removed by a PR stripping process.

[0008] Referring to FIG. 1B, a gate insulating layer 120 is formed on the entire surface of the substrate 100 having the first and second semiconductor layers 110 and 115. A first PR pattern 125 is formed using a second mask (not shown) on the first and second semiconductor layers 110 and 115 in the first and second TFT regions A and B. A first impurity implantation process 127 may be performed to implant n-type impurity ions, such as P ions, As ions, Sb ions, or Bi ions, into the first semiconductor layer 110 of the first TFT region A. Thus, the first semiconductor layer 110 of the first TFT region A forms an NMOS transistor including first source and drain regions 110s and 110d and a first channel region 110c, which is interposed between the first source and drain regions 110s and 110d.

[0009] Referring to FIG. 1C, a gate electrode material is deposited on the gate insulating layer 120 in the first and second TFT regions A and B and then patterned using a third mask (not shown), thereby forming a first gate electrode 130 and a second gate electrode 135 corresponding to the first channel region 110c and a second channel region 115c of the first and second semiconductor layers 110 and 115. In this case, the first gate electrode 130 is patterned to a smaller size than the first channel region 110c of the first semiconductor layer 110 in the first TFT region A. A second impurity implantation process 140 is performed using the first gate electrode 130 as a mask, thereby forming lightly doped drain (LDD) regions 110e in predetermined regions of the first channel region 110c of the first semiconductor layer 110. Thus, the first semiconductor layer 110 of the first TFT region A defines the first source and drain regions 110s and 110d, which are doped with n-type impurity ions, the LDD regions 110e, and the first channel region 110c, which is interposed between the LDD regions 110e. Also, as the result of the second impurity implantation process 140, the semiconductor layer 115 of the second TFT region B defines second source and drain regions 115s and 115d and the second channel region 115c.

[0010] Referring to FIG. 1D, a second photoresist pattern 145 is formed using a fourth mask (not shown) to completely cover the first TFT region A and cover only the second gate electrode 135 in the second TFT region B. A third impurity implantation process 150 is then performed so that p-type impurity ions, such as B ions, Al ions, Ga ions, or In ions are implanted into the second source and drain regions 115s and 115d of the second TFT region B. In this case, the p-type impurity ions are implanted into the second source and drain regions 115s and 115d of the second TFT region B at a higher concentration than the LDD regions 110e. Accordingly, the second semiconductor layer 115 of the second TFT region B forms a PMOS transistor including the second source and drain regions 115s and 115d and the second channel region 115c.

[0011] In this process, a CMOS transistor having both the NMOS transistor and the PMOS transistor is formed.

[0012] Referring to FIG. 1E, an interlayer insulating layer 155 is formed on the entire surface of the substrate

100 having the first and second gate electrodes 130 and 135. Contact holes 160 are formed using a fifth mask (not shown) in the interlayer insulating layer 155 formed in the first and second TFT regions A and B to expose portions of the first and second source and drain regions 110s, 110d, 115s, and 115d.

[0013] Referring to FIG. 1F, source and drain electrode materials are deposited through the contact holes 160 of the interlayer insulating layer 155 and then patterned using a sixth mask (not shown), thereby forming first and second source and drain electrodes 165s, 165d, 170s, and 170d that are in contact with the first and second source and drain regions 110s, 110d, 115s, and 115d of the first and second semiconductor layers 110 and 115, respectively.

[0014] Referring to FIG. 1G, a passivation layer 175 is formed on the entire surface of the substrate 100 having the first and second source and drain electrodes 165s, 165d, 170s, and 170d. By performing an etching process using a seventh mask (not shown), a first via hole 180 is formed in the passivation layer 175 formed in the opening region C.

[0015] Referring to FIG. 1H, a planarization layer 185 is formed on the entire surface of the substrate 100 having the passivation layer 175 with the first via hole 180 to reduce a step. By performing a wet etching process using an eighth mask (not shown) and an etchant having a high etch selectivity with respect to the planarization layer 185, a second via hole 190 is formed in the planarization layer 185 of the opening region C.

[0016] Referring to FIGs. 1I and 1J, a first electrode 195 is formed around the second via hole 190 and on inner walls and bottom surfaces of the first and second via holes 180 and 190 of the opening region C. The first electrode 195 is a reflective anode that includes a transparent electrode 195b and a reflective layer 195a with high reflectance.

[0017] Referring to FIG. 1I, the reflective layer 195a of the first electrode 195 is formed by depositing and then patterning aluminum (Al) using a ninth mask (not shown).

[0018] Referring to FIG. 1J, the transparent electrode 195b is formed by depositing indium tin oxide (ITO) or indium zinc oxide (IZO) on the reflective layer 195a and then patterning the deposited material through a wet or dry etching process using a tenth mask (not shown).

[0019] Referring to FIG. 1K, a pixel defining layer 197 is deposited on the entire surface of the substrate 100 having the first electrode 195 and then patterned using an eleventh mask (not shown), thereby forming an opening P to expose a portion of the surface of the first electrode 195.

[0020] An organic layer (not shown) having at least an emission layer is formed on the exposed surface of the first electrode 195, and a second electrode (not shown) is deposited on the entire surface of the substrate 100 having the organic layer. The second electrode is a thin transmissive electrode, which is formed of one material selected from the group consisting of Mg, Ca, Al, Ag, and an alloy thereof.

[0021] The substrate 100 having the second electrode is encapsulated with an upper substrate by a typical method, thereby completing a top-emitting OLED having a top gate type CMOS TFT. The CMOS TFT includes LDD regions in an NMOS transistor.

[0022] Also, a method of fabricating an OLED having a bottom gate type CMOS TFT with the LDD regions is similar to the above-described method of fabricating the OLED having the top gate type CMOS TFT with the LDD regions.

[0023] First, a gate electrode material is deposited in a first TFT region and a second TFT region of a substrate and then patterned using a first mask, thereby forming a gate electrode. A semiconductor layer is formed on a gate insulating layer corresponding to the gate electrode and then patterned using a second mask. N-type impurity ions are implanted using a third mask into the semiconductor layer in the first TFT region, thereby forming an NMOS region. Also, LDD impurity ions are implanted using a fourth mask to form the LDD regions. Thereafter, p-type impurity ions are implanted using a fifth mask into the semiconductor layer in the second TFT region, thereby forming a PMOS region. As a result, a CMOS transistor having both an NMOS transistor with the LDD regions and a PMOS transistor is obtained.

[0024] Thereafter, formation of a contact hole in an interlayer insulating layer using a sixth mask, patterning of source and drain electrodes using a seventh mask, formation of a first via hole using an eighth mask, formation of a second via hole using a ninth mask, patterning of a reflective layer of a first electrode using a tenth mask, patterning of a transparent electrode of the first electrode using an eleventh mask, and formation of a pixel defining layer having an opening using a twelfth mask are the same as the above-described method of fabricating the OLED having the top gate type CMOS TFT. That is, an OLED having a bottom gate type CMOS TFT with the LDD regions is formed by performing a mask process twelve times.

[0025] As described above, the fabrication of the OLED having the top gate type or bottom gate type CMOS TFT with the LDD regions requires comparatively many process steps because a PMOS TFT and an NMOS TFT should be formed on a single substrate, a via hole should be patterned twice, and a first electrode should be patterned twice. Also, although the LDD regions are formed to reduce a leakage current of the NMOS TFT and solve a hot carrier effect caused by miniaturization, the formation of the LDD regions may result in a further increase in the number of masks used to fabricate the CMOS TFT.

[0026] The conventional OLED having the top gate type or bottom gate type CMOS TFT with the LDD regions is obtained by performing a mask process eleven to twelve times. As a result, an overall process tact time is extended, the process becomes complicated, yield decreases, and production cost increases.

SUMMARY OF THE INVENTION

[0027] The present invention provides an organic light emitting display device (OLED) and a method of fabricating the same in which when a metal interconnection and a gate electrode are formed at the same time or when a first electrode is formed, interconnections for electrically connecting elements are formed, so that an overall fabrication process is shortened and the production cost is reduced by a decrease in the number of used masks.

[0028] In an exemplary embodiment of the present invention, an OLED includes: a substrate having a first thin film transistor (TFT), a second TFT, and a metal interconnection; a planarization layer disposed on the substrate having the first TFT, the second TFT, and the metal interconnection; contact holes disposed in predetermined regions of the planarization layer to expose predetermined regions of first source and drain regions of the first TFT, second source and drain regions of the second TFT, and the metal interconnection; and an interconnection for electrically connecting the metal interconnection, the first source and drain regions, and the second source and drain regions through the contact holes.

[0029] In another exemplary embodiment of the present invention, an OLED includes: a metal interconnection, a first gate electrode, and a second gate electrode disposed on a substrate; a gate insulating layer disposed on the metal interconnection, the first gate electrode, and the second gate electrode; a first semiconductor layer and a second semiconductor layer disposed on the gate insulating layer, the first semiconductor layer corresponding to the first gate electrode and including first source and drain regions and a first channel region, the second semiconductor layer corresponding to the second gate electrode and including second source and drain regions and a second channel region; a planarization layer disposed on the first semiconductor layer and the second semiconductor layer; contact holes formed by etching predetermined regions of the planarization layer and exposing predetermined regions of the metal interconnection, the first source and drain regions, and the second source and drain regions; a first interconnection for connecting the metal interconnection with one of the first source and drain regions through the contact holes, a second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions through the contact holes, and a first electrode connected to the other of the second source and drain regions through the contact holes; a pixel defining layer disposed on the first interconnection, the second interconnection, and the first electrode and exposing a predetermined region of the first electrode; and an organic layer and a second electrode disposed on the exposed region of the first electrode, the organic layer including at least an organic emission layer (EML).

[0030] In still another exemplary embodiment of the present invention, an OLED includes: a metal interconnection disposed on a substrate; a buffer layer disposed on the metal interconnection; a first semiconductor layer and a second semiconductor layer disposed on the buffer layer, the first semiconductor layer including first source and drain regions and a first channel region, the second semiconductor layer including second source and drain regions and a second channel region; a gate insulating layer disposed on the first semiconductor layer and the second semiconductor layer; a first gate electrode and a second gate electrode disposed on the gate insulating layer and corresponding to the first channel region and the second channel region, respectively; a planarization layer disposed on the first gate electrode and the second gate electrode; contact holes formed by etching predetermined regions of the planarization layer and the gate insulating layer to expose predetermined regions of the first source and drain regions and the second source and drain regions, and formed by etching predetermined regions of the planarization layer, the gate insulating layer, and the buffer layer to expose predetermined regions of the metal interconnection; a first interconnection for connecting the metal interconnection with one of the first source and drain regions through the contact holes, a second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions through the contact holes, and a first electrode connected to the other of the second source and drain regions through the contact holes; a pixel defining layer disposed on the first interconnection, the second interconnection, and the first electrode and exposing a predetermined region of the first electrode; and an organic layer and a second electrode disposed on the exposed region of the first electrode, the organic layer including at least an organic emission layer.

[0031] In yet another exemplary embodiment of the present invention, a method of fabricating an OLED includes: forming a metal interconnection on a substrate; forming a buffer layer on the metal interconnection; forming a first semiconductor layer and a second semiconductor layer on the buffer layer; forming a gate insulating layer on the first semiconductor layer and the second semiconductor layer; forming a first gate electrode and a second gate electrode on the gate insulating layer such that the first gate electrode and the second gate electrode correspond to a first channel region of the first semiconductor layer and a second channel region of the second semiconductor layer, respectively; forming a planarization layer on the first gate electrode and the second gate electrode; forming contact holes exposing predetermined regions of first source and drain regions of the first semiconductor layer and predetermined regions of second source and drain regions of the second semiconductor layer by etching predetermined regions of the planarization layer and the gate insulating layer, and exposing predetermined regions of the metal interconnection by etching predetermined regions of the planarization layer, the gate insulating layer, and the buffer layer; forming a reflective layer and a transparent layer on the substrate

having the contact holes; forming a first interconnection, a second interconnection, and a first electrode by patterning the reflective layer and the transparent layer, the first interconnection for connecting the metal interconnection with one of the first source and drain regions, the second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions, the first electrode connected to the other of the second source and drain regions; forming a pixel defining layer on the substrate having the first interconnection, the second interconnection, and the first electrode to expose a predetermined region of the first electrode; and forming an organic layer having at least an organic emission layer and a second electrode on the exposed region of the first electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The above and other features of the present invention will be described in reference to certain exemplary embodiments thereof with reference to the attached drawings in which:

FIGs. 1A through 1K are cross-sectional views illustrating a conventional organic light emitting display device (OLED) having a top gate type CMOS thin film transistor (TFT) and a method of fabricating the same;

FIGs. 2A through 2H are cross-sectional views illustrating an OLED having a bottom gate type CMOS TFT and a method of fabricating the same according to an exemplary embodiment of the present invention; and

FIGs. 3A through 3I are cross-sectional views illustrating an OLED having a top gate type CMOS TFT and a method of fabricating the same according to another exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0033] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. The same reference numerals are used to denote the same elements throughout the specification.

Embodiment 1

[0034] FIGs. 2A through 2H are cross-sectional views illustrating an organic light emitting display device (OLED) having a bottom gate type complementary metal oxide semiconductor thin film transistor (CMOS TFT) and a method of fabricating the same according to an exemplary embodiment of the present invention.

[0035] Referring to FIGs. 2A through 2H, the OLED having the bottom gate type CMOS TFT according to an exemplary embodiment of the present invention includes a substrate 200 having a first TFT region A, a second TFT region B, an opening region C, and an interconnection region D. The substrate 200 may be a transparent substrate, which is formed of glass, plastic, or quartz.

[0036] Referring to FIG. 2A, a first gate electrode 210, a second gate electrode 215, and a metal interconnection 220 are formed and then patterned using a first mask (not shown) in the first and second TFT regions A and B of the substrate 200. The first and second gate electrodes 210 and 215 may be formed of one material selected from the group consisting of molybdenum (Mo), tungsten (W), aluminum (Al), and an alloy thereof, for example, tungsten molybdenum (MoW), molybdenum (Mo), tungsten (W), tungsten silicide (WSi_2), molybdenum silicide ($MoSi_2$), and aluminum (Al). The first and second gate electrodes 210 and 215 may be formed by a sputtering method or a vacuum deposition method. Typically, the first and second gate electrodes 210 and 215 may be formed by depositing a material using a sputtering method and then patterning the deposited material.

[0037] The first mask forms a photoresist pattern according to patterns formed on a reticle by a photolithography process, and then the photoresist pattern is removed by ashing and photoresist stripping processes.

[0038] During the formation of the first and second gate electrodes 210 and 215, the metal interconnection 220 is formed in the interconnection region D of the substrate 200. The metal interconnection 220 is formed a predetermined distance apart from the first and second gate electrodes 210 and 215 on the same layer as the first and second gate electrodes 210 and 215. The metal interconnection 220 may be formed by depositing the same material as the first and second gate electrodes 210 and 215 and then patterning the material using the first mask.

[0039] Referring to FIG. 2B, a gate insulating layer 230 is formed on the entire surface of the substrate 200 having the first and second gate electrodes 210 and 215 and the metal interconnection 220. The gate insulating layer 230 may be a silicon oxide layer, a silicon nitride layer, or a stacked layer thereof. The gate insulating layer 230 may be formed by a plasma-enhanced chemical vapor deposition (PECVD) process or a low-pressure CVD (LPCVD) process.

[0040] A first semiconductor layer 240 and a second semiconductor layer 245 are formed using a second mask (not shown) on the gate insulating layer 230 in the first and second TFT regions A and B, respectively. In this case, the first and second semiconductor layers 240 and 245 may be formed of amorphous silicon (a-Si) or polycrystalline Si (poly-Si), preferably, poly-Si. The first and second semiconductor layers 240 and 245 may be formed by depositing a-Si using a PECVD process, crystallizing the a-Si into a poly-Si layer using a crystallization method, and patterning the poly-Si layer using the second mask. In this case, the deposition of the a-Si using the PECVD process may be followed by dehydrogena-

tion of the a-Si using an annealing process to lower the concentration of hydrogen.

[0041] Thereafter, the second mask, which is used to pattern the first and second semiconductor layers 240 and 245, is positioned under the substrate 200, and a back exposure process using the second mask and the first and second gate electrodes 210 and 215 as masks is carried out to form a first photoresist pattern 247 corresponding to the first and second gate electrodes 210 and 215 on predetermined regions of the first and second semiconductor layers 240 and 245 in the first and second TFT regions A and B.

[0042] More specifically, the back exposure process includes positioning the second mask, which is used to pattern the first and second semiconductor layers 240 and 245, under the substrate 200 and irradiating light toward a bottom of the substrate 200. Thus, the first photoresist pattern 247 is formed on the predetermined regions of the first and second semiconductor layers 240 and 245 corresponding to the first and second gate electrodes 210 and 215 in the first and second TFT regions A and B. The first photoresist pattern 247 may be formed of a positive photosensitive material. Thus, when a portion of the first photoresist pattern 247 is exposed to light, the portion changes into a material soluble in a developing solution and thus is etched. In general, the photosensitive material is composed of a solvent, which controls viscosity, a photo active compound, which reacts with ultraviolet (UV) rays, and a polymer resin, which is a chemical combination. The photosensitive material may include acrylic resin or polyimide (PI).

[0043] Accordingly, photoresist, which is positioned on the gate insulating layer 230 that transmits light incident from the bottom of the substrate 200 and on a region of the semiconductor layer that does not correspond to the gate electrode, is exposed to light, changes into a material soluble in a developing solution, and is etched during the back exposure process. On the other hand, since the first and second gate electrodes 210 and 215 formed in the first and second TFT regions A and B of the substrate 200, are formed of a metal and do not transmit light, they are not exposed to light incident from the bottom of the substrate 200, and thus the first photoresist pattern 247 is formed to the same size as the first and second electrodes 210 and 215.

[0044] By performing a first impurity implantation process 250 using the first photoresist pattern 247 obtained by the back exposure process, lightly doped drain (LDD) impurity ions are implanted into the first and second semiconductor layers 240 and 245. Thus, LDD regions 240e and a first channel region 240c are formed in the first TFT region A, and second source and drain regions 245s and 245d and a second channel region 245c are formed in the second TFT region B. The first impurity implantation process 250 may be carried out using typical n-type impurity ions, for example, PH_3 ions. In particular, the LDD regions 240e are formed to improve the characteristics of a TFT. Also, because the first photoresist pattern 247 is formed by the back exposure process after the formation of the first and second semiconductor layers 240 and 245, LDD impurity ions can be implanted into the first semiconductor layer 240 in the first TFT region A without an additional mask, so that one process mask can be saved in a number.

[0045] In a case where the back exposure process is unnecessary or cannot be used, the first photoresist pattern 247 may be formed using a mask for a photoresist pattern. However, one more mask is required at this time.

[0046] Referring to FIG. 2C, the first photoresist pattern 247 is removed, and a second photoresist pattern 255 is formed using a third mask (not shown). Specifically, the second photoresist pattern 255 is formed to have a slightly greater width than the first channel region 240c on the first semiconductor 240 in the first TFT region A to completely cover the first channel region 240c and partially cover the LDD regions 240e. Also, the second photoresist pattern 255 is formed to completely cover the second semiconductor layer 245 in the second TFT region B.

[0047] Thereafter, n-type impurity ions are implanted into exposed portions of the LDD regions 240e in the first TFT region A using the second photoresist pattern 255. The n-type impurity ions include one material selected from the group consisting of phosphorus (P), arsenic (As), antimony (Sb), and bismuth (Bi). The concentration of the n-type impurity ions is higher than that of the LDD impurity ions. As a result, an NMOS transistor including the first source and drain regions 240s and 240d, which are doped with n-type impurity ions, the LDD regions 240e, which are doped with LDD impurity ions, and the first channel region 240c, which is interposed between the LDD regions 240e, is formed in the first semiconductor layer 240. On the other hand, the second semiconductor layer 245 formed in the second TFT region B, which is covered by the second photoresist pattern 255, is not doped with the n-type impurity ions.

[0048] Referring to FIG. 2D, the second photoresist pattern 255 is removed, and a third photoresist pattern 265 is formed using a fourth mask (not shown). The third photoresist pattern 265 covers the second channel region 245c, which is defined in the second semiconductor layer 245 of the second TFT region B through the first impurity implantation process 250, exposes the second source and drain regions 245s and 245d, and completely covers the first semiconductor layer 240 in the first TFT region A.

[0049] Subsequently, a third impurity implantation process 270 is performed using the third photoresist pattern 265 so that p-type impurity ions are implanted into the second source and drain regions 245s and 245d of the second TFT region B. The p-type impurity ions include one selected from the group consisting of boron (B), aluminum (Al), gallium (Ga), and indium (In). The concentration of the p-type impurity ions is higher than that of the LDD impurity ions. Thus, a PMOS transistor including the second source and drain regions 245s and 245d,

which are doped with p-type impurity ions, and the second channel region 245c, which is interposed between the second source and drain regions 245s and 245d, is formed in the second semiconductor layer 245. On the other hand, the first semiconductor layer 240 formed in the first TFT region, which is covered by the third photoresist pattern 265, is not doped with the p-type impurity ions.

[0050] As a result, a CMOS TFT having both the NMOS transistor formed in the first TFT region A and the PMOS transistor formed in the second TFT region B is formed.

[0051] Referring to FIG. 2E, a passivation layer 275 is formed on the first and second semiconductor layers 240 and 245. Typically, the passivation layer 275 is formed to prevent TFTs from external contamination. The passivation layer 275 may be formed of an inorganic insulating layer, which is a silicon nitride layer, a silicon oxide layer, or a stacked layer thereof. The passivation layer 275 may be formed by a PECVD process or an LPCVD process. Preferably, the passivation layer 275 may be obtained by depositing an inorganic insulating material, annealing the material, and hydrogenating the annealed material.

[0052] A planarization layer 280 is formed on the passivation layer 275 to reduce a step. The planarization layer 280 may be typically formed of one organic material selected from the group consisting of benzocyclobutane (BCB), PI, polyamide (PA), acrylic resin, and phenolic resin. The planarization layer 280 may be formed by a spin coating process.

[0053] Thereafter, the passivation layer 275 and the planarization layer 280, which are formed in the first and second TFT regions A and B and the interconnection region D, are etched using a fifth mask (not shown), thereby forming contact holes 285 in the passivation layer 275 and the planarization layer 280 to expose portions of the first and second source and drain regions 240s, 240d, 245s, and 245d and the metal interconnection 220.

[0054] Referring to FIG. 2F, a first electrode material layer 290 including a reflective layer 290a and a transparent layer 290b is deposited in the contact holes 285 and then patterned by blanket etching, thereby forming a first electrode 291, a first interconnection 292, and a second interconnection 293.

[0055] The reflective layer 290a is formed of a metal with high reflectance, which is one selected from the group consisting of aluminum (Al), silver (Ag), and an alloy thereof. Also, the transparent layer 290b is formed of one of ITO and IZO. Thus, the first electrode 291 is formed as a reflective anode. The reflective layer 290a and the transparent layer 290b may be sequentially deposited by a sputtering method, a vacuum deposition method, or an ion plating method. Typically, the reflective layer 290a and the transparent layer 290b are formed by a sputtering method.

[0056] The reflective layer 290a of the first electrode material layer 290 may be formed of Ag such that the reflective layer 290a can be patterned with the transparent layer 290b by blanket etching, while the transparent layer 290b may be formed of ITO. The first electrode material layer 290 may be formed by sequentially depositing Ag and ITO using a sputtering method and then wet- or dry-etching the Ag layer and the ITO layer through blanket etching using a sixth mask (not shown). The blanket etching may make use of an ordinary etching process. By blanket-etching the first electrode material layer 290 including the reflective layer 290a and the transparent layer 290b, one process mask can be saved in a number during the formation of the first electrode 291.

[0057] As a result, the first electrode material layer 290 is patterned to form the first interconnection 292 and the second interconnection 293. The first interconnection 292 connects the metal interconnection 220 formed in the interconnection region C with one of the first source and drain regions 240s and 240d (e.g., the first source region 240s) of the first semiconductor layer 240 formed in the first TFT region A. Also, the second interconnection 293 connects the other of the first source and drain regions 240s and 240d (e.g., the first drain region 240d) of the first semiconductor layer 240 formed in the first TFT region A with one of the second source and drain regions 245s and 245d (e.g. the second source region 245s) of the second semiconductor layer 245 formed in the second TFT region B.

[0058] When forming the first electrode 291, which is a reflective anode contacting the second source and drain regions 245s and 245d, the process of forming the contact holes for connecting the second source and drain regions 245s and 245 with source and drain electrodes and the process of forming the source and drain electrodes may be omitted so that one process mask can be further saved in a number.

[0059] Referring to FIG. 2G, a pixel defining layer 295 is formed on the entire surface of the substrate 200 to expose a predetermined region of the first electrode 291. The pixel defining layer 295 is typically formed of one organic material selected from the group consisting of BCB, PI, PA, acrylic resin, and phenolic resin. The pixel defining layer 295 is formed by depositing an organic material using a spin coating process and then etching using a seventh mask so that an opening P is formed in the opening region C to expose a portion of the surface of the first electrode 291. The opening P may be formed by a dry or wet etching process, typically, a wet etching process.

[0060] Referring to FIG. 2H, an organic layer 297 including at least an organic emission layer (EML) and a second electrode 299 are formed on the exposed portion of the first electrode 291 in the opening P. In addition to the EML, the organic layer 297 may further include at least one of an electron injection layer (EIL), an electron transport layer (ETL), a hole transport layer (HTL), and a hole injection layer (HIL).

[0061] The EML may be formed of a low molecular substance or a high molecular substance. The low molecular substance may be one selected from the group

consisting of tris(8-hydroxyquinoline) aluminum (Alq3), anthracene, cyclo pentadiene, ZnPBO, Balq, and DPVBi. The high molecular substance may be one selected from the group consisting of polythiophene (PT), poly(p-phenylenevinylene) (PPV), polyphenylene (PPP), and derivatives thereof. The organic layer 297 may be formed by a vacuum deposition method, a spin coating method, an inkjet printing method, or a laser induced thermal imaging (LITI) method. Typically, the organic layer 297 may be formed by a spin coating method. Also, the organic layer 297 may be patterned by an LITI method or a vacuum deposition method using a shadow mask.

[0062] The second electrode 299 is a thin transmissive electrode, which may be formed of one selected from the group consisting of Mg, Ca, Al, Ag, and an alloy thereof. Also, the second electrode 299 may be formed by a vacuum deposition method.

[0063] The substrate 200 having the second electrode 299 is encapsulated with an upper substrate using an ordinary method. Thus, a top-emitting OLED having the bottom gate type CMOS TFT with the LDD regions according to the embodiment of the present invention is completed using seven masks (or using eighth masks if the back exposure process is not used).

Embodiment 2

[0064] FIGS. 3A through 3I are cross-sectional views illustrating an OLED having a top gate type CMOS TFT and a method of fabricating the same according to another exemplary embodiment of the present invention.

[0065] Referring to FIG. 3A, the OLED having a top gate type CMOS TFT according to another embodiment of the present invention includes a substrate 300 having a first TFT region A, a second TFT region B, an opening region C, and an interconnection region D. The substrate 300 may be a transparent substrate, which is formed of glass, plastic, or quartz.

[0066] A metal interconnection 310 is formed using a first mask (not shown) in the interconnection region D of the substrate 300. The metal interconnection 310 may be formed of one material selected from the group consisting of Mo, W, Al, and an alloy thereof. The metal interconnection 310 may be formed by a sputtering method or a vacuum deposition method. Typically, the metal interconnection 310 may be formed by depositing a material using a sputtering method and patterning the deposited material.

[0067] Referring to FIG. 3B, a buffer layer 320 is formed on the entire surface of the substrate 300 having the metal interconnection 310, and a first semiconductor layer 330 and a second semiconductor layer 335 are formed and then patterned using a second mask (not shown) on the buffer layer 320 in the first and second TFT regions A and B.

[0068] The buffer layer 320 is formed to protect a TFT that will be formed later from impurity ions diffusing from the substrate 300. The buffer layer 320 may be a silicon oxide layer, a silicon nitride layer, or a stacked layer thereof. The buffer layer 320 is formed by a PECVD process or an LPCVD process. The method of forming the first and second semiconductor layers 330 and 335 is the same as that described in Embodiment 1.

[0069] Referring to FIG. 3C, a first photoresist pattern 340 is formed using a third mask (not shown) to expose a predetermined region of the first semiconductor layer 330 in the first TFT region A, and a first impurity implantation process 345 is carried out using the first photoresist pattern 340 so that n-type impurity ions are implanted into the first semiconductor layer 330. The n-type impurity ions include one selected from the group consisting of P, As, Sb, and Bi. Thus, the first semiconductor layer 330 defines first source and drain regions 330s and 330d, which are doped with the n-type impurity ions, and a first channel region 330c, which is interposed between the first source and drain regions 330s and 330d. On the other hand, the second semiconductor layer 335 formed in the second TFT region B, which is covered by the first photoresist pattern 340, is not doped with the n-type impurity ions.

[0070] Referring to FIG. 3D, after the first impurity implantation process 345, the first photoresist pattern 340 is removed by ashing and PR stripping processes, and a gate insulating layer 350 is formed on the entire surface of the substrate 300 having the first and second semiconductor layers 330 and 335. The gate insulating layer 350 may be a silicon oxide layer, a silicon nitride layer, or a stacked layer thereof. Also, the gate insulating layer 350 may be obtained by a PECVD process or an LPCVD process.

[0071] A first gate electrode 360 and a second gate electrode 365 are formed using a fourth mask (not shown) on the gate insulating layer 350 in the first and second TFT regions A and B. The first and second gate electrodes 360 and 365 are formed of one material selected from the group consisting of Mo, W, Al, and an alloy thereof. In this case, the first gate electrode 360 formed in the first TFT region A is formed to have a smaller width than the first channel region 330c shown in FIG. 3C to leave spaces for LDD regions that will be formed later. The first and second gate electrodes 360 and 365 may be formed by a sputtering method or a vacuum deposition method. Typically, the first and second gate electrodes 360 and 365 are formed by depositing a material using a sputtering method and patterning the deposited material.

[0072] A second impurity implantation process 370 is performed in the first and second TFT regions A and B using the first and second gate electrodes 360 and 365 as masks, so that LDD regions 330e are formed in the first semiconductor layer 330. Impurity ions doped into the LDD regions 330e are n-type impurity ions, typically, PH_3. The concentration of the LDD impurity ions is lower than that of the n-type impurity ions. Thus, the first semiconductor layer 330 formed in the first TFT region A forms an NMOS transistor including the first source and drain regions 330s and 330d, which are doped with n-

type impurity ions, the LDD regions 330e, which are doped with low-concentration impurity ions, and the first channel region 330c, which is interposed between the LDD regions 330e. In this case, as the result of the second impurity implantation process 370, the second semiconductor layer 335 formed in the second TFT region B defines second source and drain regions 335s and 335d and a second channel region 335c, which is interposed between the second source and drain regions 335s and 335d.

[0073] Referring to FIG. 3E, a second photoresist pattern 375 is formed using a fifth mask (not shown) to completely cover the first semiconductor layer 330 in the first TFT region A and expose the second semiconductor layer 335 in the second TFT region B. A third impurity implantation process 380 is performed using the second photoresist pattern 375 on the second semiconductor layer 335 in the second TFT region B so that p-type impurity ions are implanted to form the second source and drain regions 335s and 335d. The p-type impurity ions include one selected from the group consisting of B, Al, Ga, and In. The concentration of the p-type impurity ions is higher than that of the LDD impurity ions. Thus, the second semiconductor layer 335 forms a PMOS transistor including the second source and drain regions 335s and 335d, which are doped with the p-type impurity ions, and the second channel region 335c, which is interposed between the second source and drain regions 335s and 335d.

[0074] As a result, a CMOS TFT having both the NMOS transistor formed in the first TFT region A and the PMOS transistor formed in the second TFT region B is formed.

[0075] Referring to FIG. 3F, a passivation layer 382 is formed on the first and second gate electrodes 360 and 365, and then a planarization layer 385 is formed on the passivation layer 382.

[0076] The passivation layer 382 and the planarization layer 385 are etched using a sixth mask (not shown), thereby forming contact holes 387 to expose portions of the first and second source and drain regions 330s, 330d, 335s, and 335d and the metal interconnection 310.

[0077] The methods of forming the passivation layer 382, the planarization layer 385, and the contact holes 387 are the same as those described in Embodiment 1.

[0078] Referring to FIG. 3G, a first electrode material layer 390 including a reflective layer 390a and a transparent layer 390b is stacked in the contact holes 387, and then patterned by a blanket etching process using a seventh mask (not shown), thereby forming a first electrode 391, a first interconnection 392, and a second interconnection 393.

[0079] The formation and patterning of the first electrode material layer 390 are the same as those described in Embodiment 1. The first electrode material layer 390 including the reflective layer 390a and the transparent layer 390b is blanket-etched, so that one process mask can be saved in a number during the formation of the first electrode 391.

[0080] As a result, the first electrode 391 is in contact with one of the second source and drain regions 335s and 335d of the second semiconductor layer 335 in the second TFT region B, and the first interconnection 392 is in contact with the metal interconnection 310 in the interconnection region C and one of the first source and drain regions 330s and 330d in the first TFT region A. Also, the second interconnection 393 is in contact with the other of the first source and drain regions 330s and 330d in the first TFT region A and the other of the second source and drain regions 335s and 335d in the second TFT region B.

[0081] Since the first electrode 391, the first interconnection 392, and the second interconnection 393 are formed at the same time, the process of forming the contact holes for connecting the source and drain regions with source and drain electrodes and the process of forming the source and drain electrodes can be omitted. Thus, two process masks can be further saved in a number.

[0082] Referring to FIG. 3H, a pixel defining layer 395 is formed on the entire surface of the substrate 300 having the first electrode 391. The method of forming the pixel defining layer 395 is the same as that described in Embodiment 1. The pixel defining layer 395 is etched using an eighth mask (not shown) so that an opening P is formed in the opening region C to expose a portion of the surface of the first electrode 391. The opening P is formed by a dry or wet etching process.

[0083] Referring to FIG. 3I, an organic layer 397 having at least an EML and a second electrode 399 are formed on the exposed portion of the first electrode 391 in the opening P. The methods of forming the organic layer 397 and the second electrode 399 are the same as those described in Embodiment 1.

[0084] The substrate 300 having the second electrode 399 is encapsulated with an upper substrate using an ordinary method. Thus, a top-emitting OLED having the top gate type CMOS TFT with the LDD regions according to another embodiment of the present invention is completed using eighth process masks.

[0085] According to the present invention as described above, when a first electrode that is a reflective anode is formed, interconnections are brought into contact with internal devices at the same time. Thus, an OLED having a CMOS TFT with LDD regions can be formed using only 7 to 8 process masks compared to the conventional OLED using 11 to 12 process masks. As a result, an overall fabrication process can be shortened, the production cost can be reduced, and yield can increase.

[0086] Although the present invention has been described with reference to certain exemplary embodiments thereof, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the present invention without departing from the scope of the present invention defined in the appended claims, and their equivalents.

Claims

1. An organic light emitting display device (OLED) comprising:

   a substrate having a first thin film transistor (TFT), a second TFT, and a metal interconnection;
   a planarization layer disposed on the substrate having the first TFT, the second TFT, and the metal interconnection;
   contact holes disposed in predetermined regions of the planarization layer to expose predetermined regions of first source and drain regions of the first TFT, second source and drain regions of the second TFT, and the metal interconnection; and
   an interconnection for electrically connecting the metal interconnection, the first source and drain regions, and the second source and drain regions through the contact holes.

2. The OLED according to claim 1, further comprising:

   a first electrode connected to one of the first source and drain regions and the second source and drain regions;
   an organic layer disposed on the first electrode; and
   a second electrode disposed on the organic layer.

3. The OLED according to claim 2, wherein the first electrode includes a reflective layer and a transparent layer.

4. The OLED according to claim 3, wherein the reflective layer is formed of one selected from the group consisting of aluminum (Al), silver (Ag), and an alloy thereof.

5. The OLED according to claim 3, wherein the transparent layer is formed of one of indium tin oxide (ITO) and indium zinc oxide (IZO).

6. The OLED according to claim 1, wherein the interconnection is disposed on the same layer as the first electrode and formed of the same material as the first electrode.

7. The OLED according to claim 1, wherein a first gate electrode of the first TFT, a second gate electrode of the second TFT, and the metal interconnection are disposed on the same layer.

8. The OLED according to claim 7, wherein the first gate electrode, the second gate electrode, and the metal interconnection are formed of one selected from the group consisting of molybdenum (Mo), tungsten (W), aluminum (Al), and an alloy thereof.

9. The OLED according to claim 1, wherein the first TFT comprises:

   a first gate electrode disposed on the substrate;
   a gate insulating layer disposed on the first gate electrode; and
   a first semiconductor layer disposed on the gate insulating layer, corresponding to the first gate electrode, and including the first source and drain regions and a first channel region, and
   wherein the second TFT comprises:

      a second gate electrode disposed on the substrate;
      the gate insulating layer disposed on the second gate electrode; and
      a second semiconductor layer disposed on the gate insulating layer, corresponding to the second gate electrode, and including the second source and drain regions and a second channel region.

10. The OLED according to claim 1, wherein the first TFT comprises:

    a first semiconductor layer disposed on the substrate and including the first source and drain regions and a first channel region;
    a gate insulating layer disposed on the first semiconductor layer; and
    a first gate electrode disposed on the gate insulating layer and corresponding to the first channel region, and
    wherein the second TFT comprises:

       a second semiconductor layer disposed on the substrate and including the second source and drain regions and a second channel region;
       the gate insulating layer disposed on the second semiconductor layer; and
       a second gate electrode disposed on the gate insulating layer and corresponding to the second channel region.

11. The OLED according to claim 9 or 10, further comprising lightly doped drain (LDD) regions disposed between the first and second drain regions and the first channel region.

12. An organic light emitting display device (OLED) comprising:

    a metal interconnection, a first gate electrode, and a second gate electrode disposed on a sub-

strate;
a gate insulating layer disposed on the metal interconnection, the first gate electrode, and the second gate electrode;
a first semiconductor layer and a second semiconductor layer disposed on the gate insulating layer, the first semiconductor layer corresponding to the first gate electrode and including first source and drain regions and a first channel region, the second semiconductor layer corresponding to the second gate electrode and including second source and drain regions and a second channel region;
a planarization layer disposed on the first semiconductor layer and the second semiconductor layer;
contact holes formed by etching predetermined regions of the planarization layer and exposing predetermined regions of the metal interconnection, the first source and drain regions, and the second source and drain regions;
a first interconnection for connecting the metal interconnection with one of the first source and drain regions through the contact holes, a second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions through the contact holes, and a first electrode connected to the other of the second source and drain regions through the contact holes;
a pixel defining layer disposed on the first interconnection, the second interconnection, and the first electrode and exposing a predetermined region of the first electrode; and
an organic layer and a second electrode disposed on the exposed region of the first electrode, the organic layer including at least an organic emission layer.

13. The OLED according to claim 12, wherein the metal interconnection, the first gate electrode, and the second gate electrode are formed of the same material.

14. The OLED according to claim 12, further comprising LDD regions disposed between the first source and drain regions and the first channel region or between the second source and drain regions and the second channel region.

15. The OLED according to claim 12, wherein the first interconnection, the second interconnection, and the first electrode include a reflective layer and a transparent layer.

16. An organic light emitting display device (OLED) comprising:

a metal interconnection disposed on a substrate;
a buffer layer disposed on the metal interconnection;
a first semiconductor layer and a second semiconductor layer disposed on the buffer layer, the first semiconductor layer including first source and drain regions and a first channel region, the second semiconductor layer including second source and drain regions and a second channel region;
a gate insulating layer disposed on the first semiconductor layer and the second semiconductor layer;
a first gate electrode and a second gate electrode disposed on the gate insulating layer and corresponding to the first channel region and the second channel region, respectively;
a planarization layer disposed on the first gate electrode and the second gate electrode;
contact holes formed by etching predetermined regions of the planarization layer and the gate insulating layer to expose predetermined regions of the first source and drain regions and the second source and drain regions, and formed by etching predetermined regions of the planarization layer, the gate insulating layer, and the buffer layer to expose predetermined regions of the metal interconnection;
a first interconnection for connecting the metal interconnection with one of the first source and drain regions through the contact holes, a second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions through the contact holes, and a first electrode connected to the other of the second source and drain regions through the contact holes;
a pixel defining layer disposed on the first interconnection, the second interconnection, and the first electrode and exposing a predetermined region of the first electrode; and
an organic layer and a second electrode disposed on the exposed region of the first electrode, the organic layer including at least an organic emission layer.

17. The OLED according to claim 16, further comprising LDD regions disposed between the first source and drain regions and the first channel region or between the second source and drain regions and the second channel region.

18. The OLED according to claim 16, wherein the first interconnection, the second interconnection, and the first electrode include a reflective layer and a transparent layer.

19. A method of fabricating an OLED, comprising:

forming a metal interconnection on a substrate;
forming a buffer layer on the metal interconnection;
forming a first semiconductor layer and a second semiconductor layer on the buffer layer;
forming a gate insulating layer on the first semiconductor layer and the second semiconductor layer;
forming a first gate electrode and a second gate electrode on the gate insulating layer such that the first gate electrode and the second gate electrode correspond to a first channel region of the first semiconductor layer and a second channel region of the second semiconductor layer, respectively;
forming a planarization layer on the first gate electrode and the second gate electrode;
forming contact holes exposing predetermined regions of first source and drain regions of the first semiconductor layer and predetermined regions of second source and drain regions of the second semiconductor layer by etching predetermined regions of the planarization layer and the gate insulating layer, and exposing predetermined regions of the metal interconnection by etching predetermined regions of the planarization layer, the gate insulating layer, and the buffer layer;
forming a reflective layer and a transparent layer on the substrate having the contact holes;
forming a first interconnection, a second interconnection, and a first electrode by patterning the reflective layer and the transparent layer, the first interconnection for connecting the metal interconnection with one of the first source and drain regions, the second interconnection for connecting the other of the first source and drain regions with one of the second source and drain regions, the first electrode connected to the other of the second source and drain regions;
forming a pixel defining layer on the substrate having the first interconnection, the second interconnection, and the first electrode to expose a predetermined region of the first electrode; and
forming an organic layer having at least an organic emission layer and a second electrode on the exposed region of the first electrode.

20. The method according to claim 19, wherein forming the first semiconductor layer and the second semiconductor layer comprises:

forming a silicon layer on the buffer layer;
patterning the silicon layer and forming a first silicon pattern and a second silicon pattern;
forming a first photoresist pattern on predetermined regions of the first silicon pattern and the second silicon pattern and implanting first impurity ions at a low concentration;
removing the first photoresist pattern, forming a second photoresist pattern to cover the first silicon pattern to have a greater width than a region of the first silicon pattern covered by the first photoresist pattern and to completely cover the second silicon pattern, and forming a first semiconductor layer having first source and drain regions, LDD regions, and a first channel region by implanting first impurity ions at a high concentration into the first silicon pattern; and
removing the second photoresist pattern, forming a third photoresist pattern to completely cover the first semiconductor layer and cover the same region as the region of the second silicon pattern covered by the first photoresist pattern, and forming a second semiconductor layer having second source and drain regions and a second channel region by implanting second impurity ions at a high concentration.

21. The method according to claim 19, wherein the first impurity ions are n-type impurity ions.

22. The method according to claim 19, wherein the second impurity ions are p-type impurity ions.

FIG. 1A

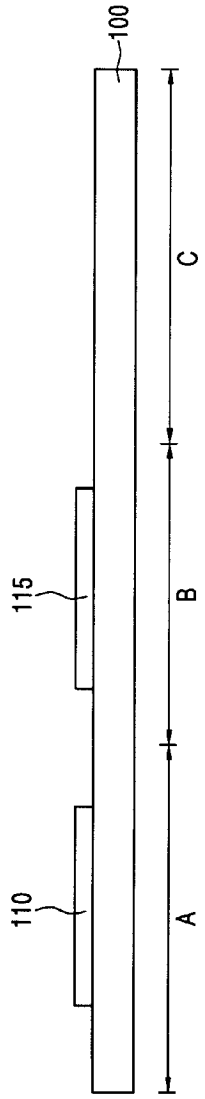


FIG. 1B

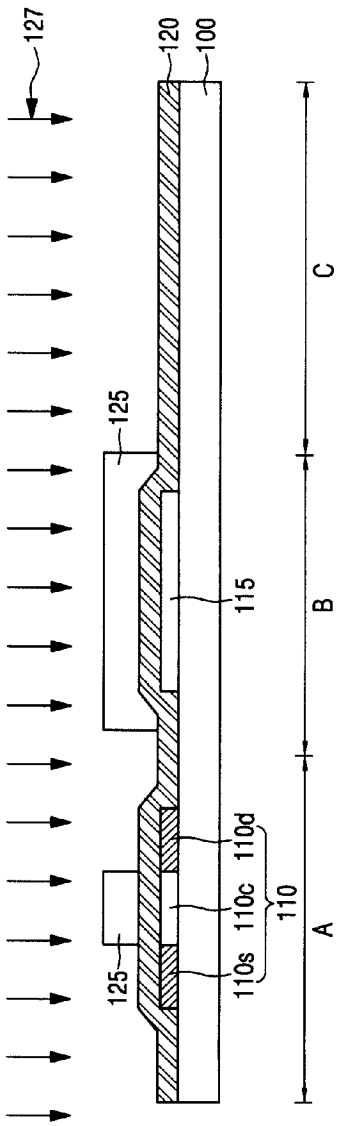
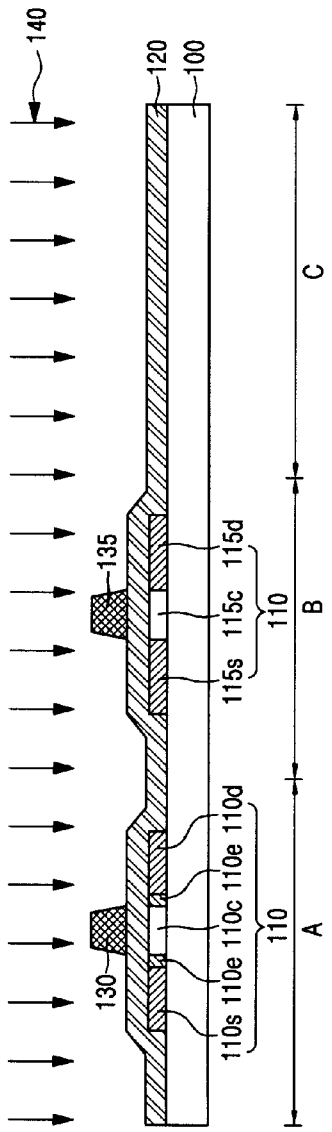


FIG. 1C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120
100
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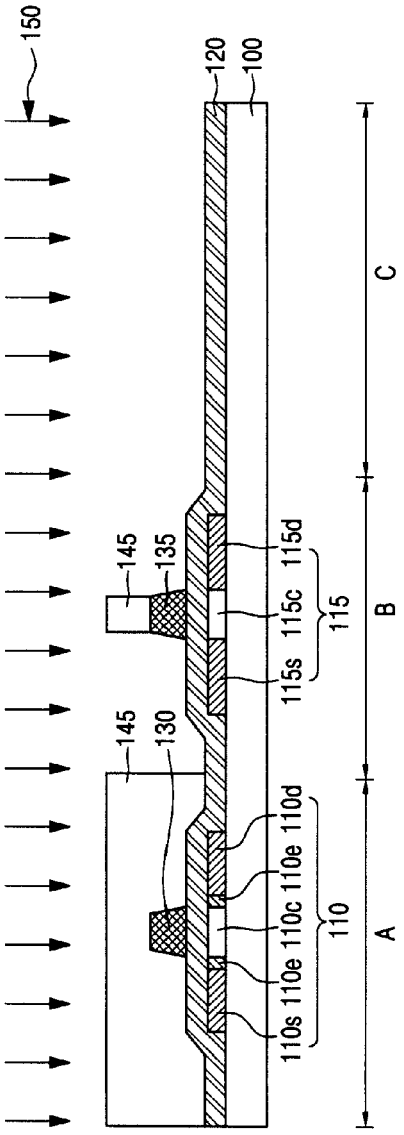
115c
115s
110
B
C
110d
110e
110c
110e
110s
110
A
130

FIG. 1D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115d
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110d
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110e
110s
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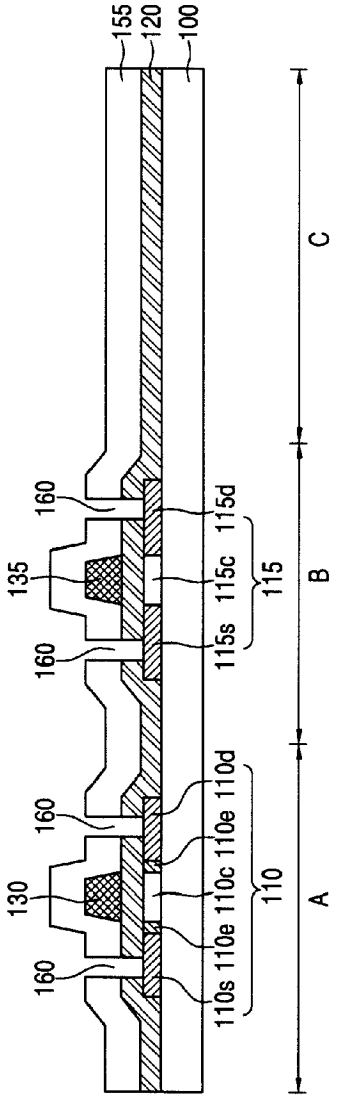
A
B
C

FIG. 1E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135
160
160
130
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110d
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110c
110e
110s
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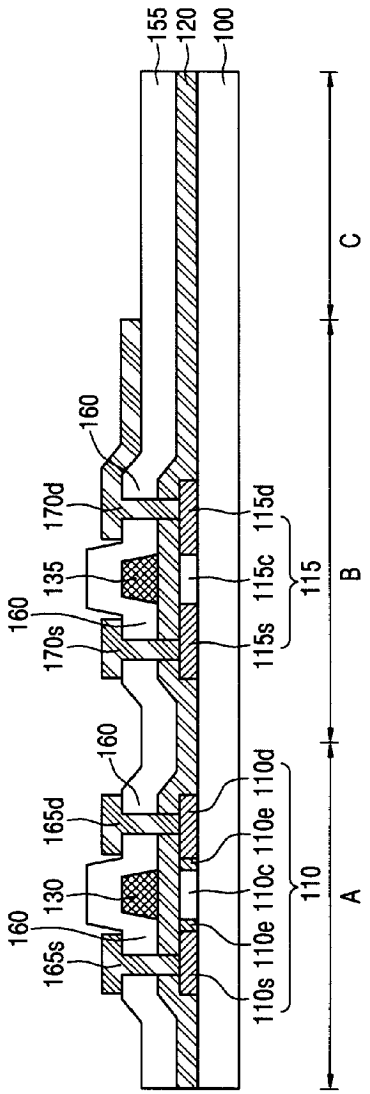
A
B
C

FIG. 1F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110c
110e
110s
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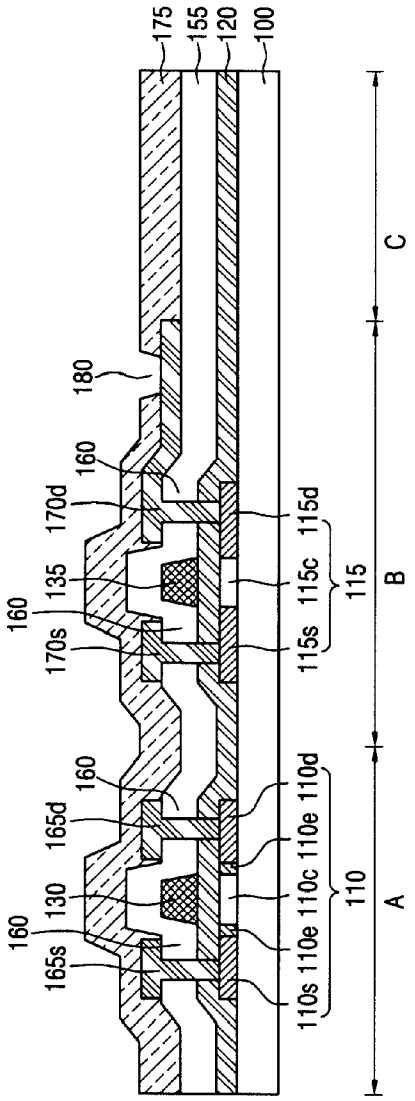
A
B
C

FIG. 1G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165d
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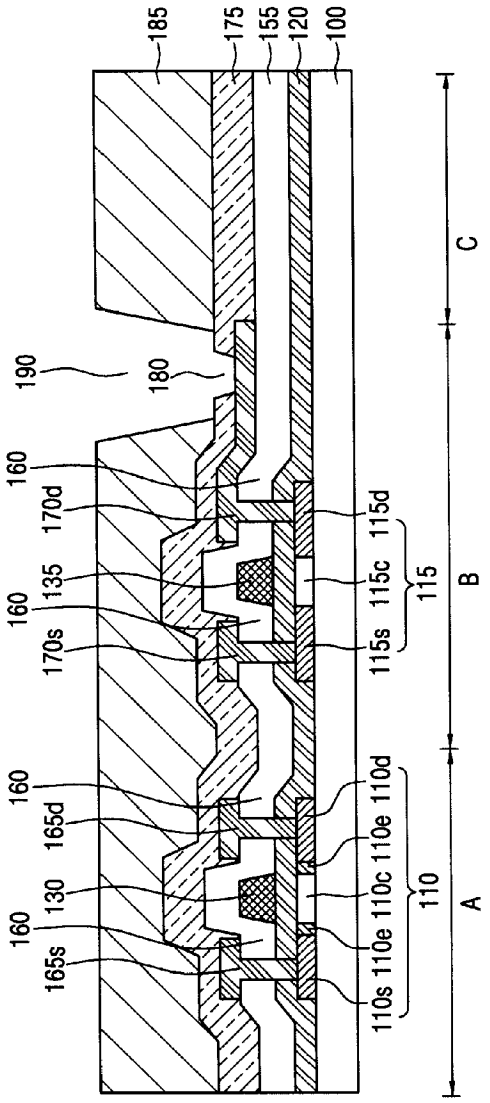
110c
110e
110s
110
C
B
A

FIG. 1H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170d
135
170s
165d
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115s
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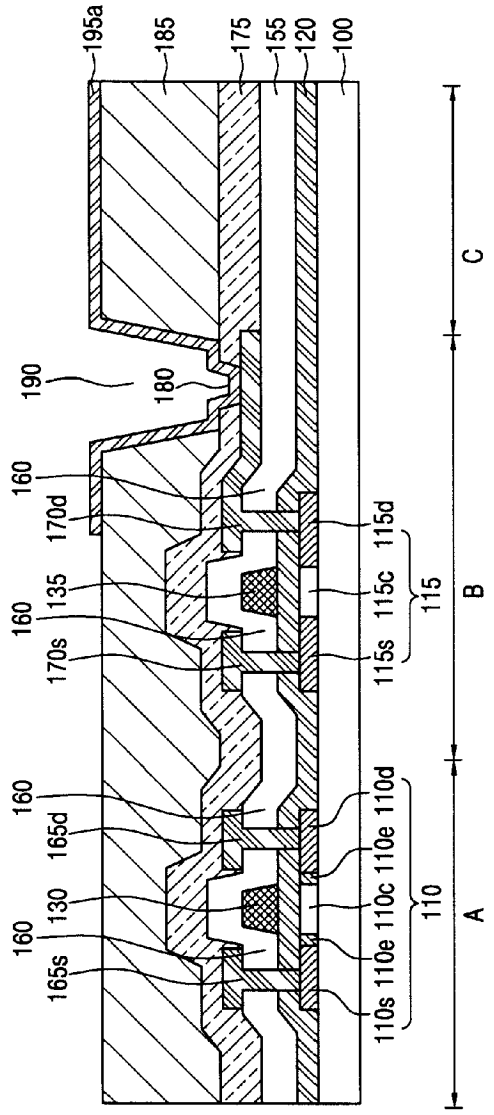
110e
110c
110e
110s
110
C
B
A

FIG. 1I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180
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170d
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170s
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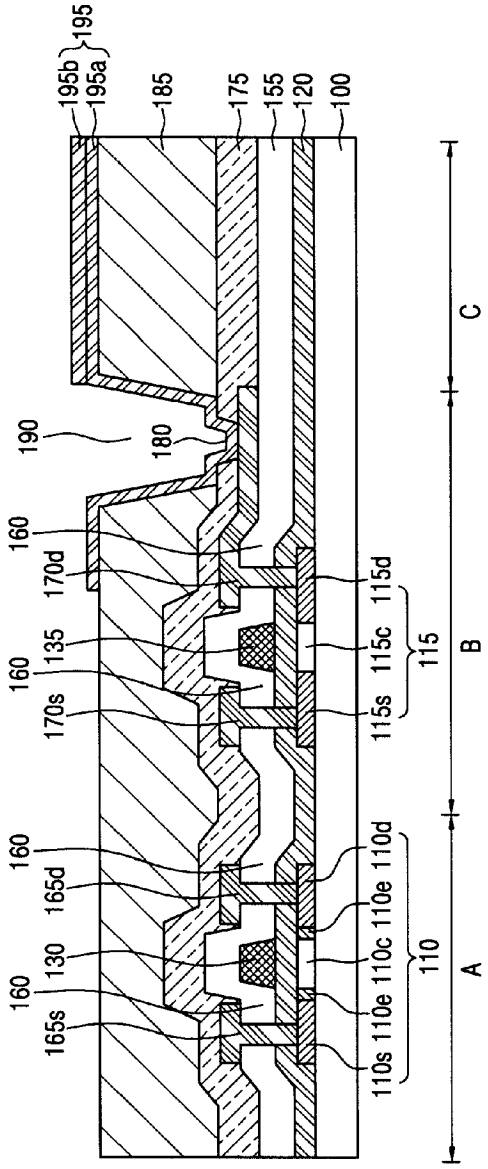
110c
110e
110s
110
A
B
C

FIG. 1J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195a
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175
155
120
100
190
180
160
170d
135
170s
165d
130
165s
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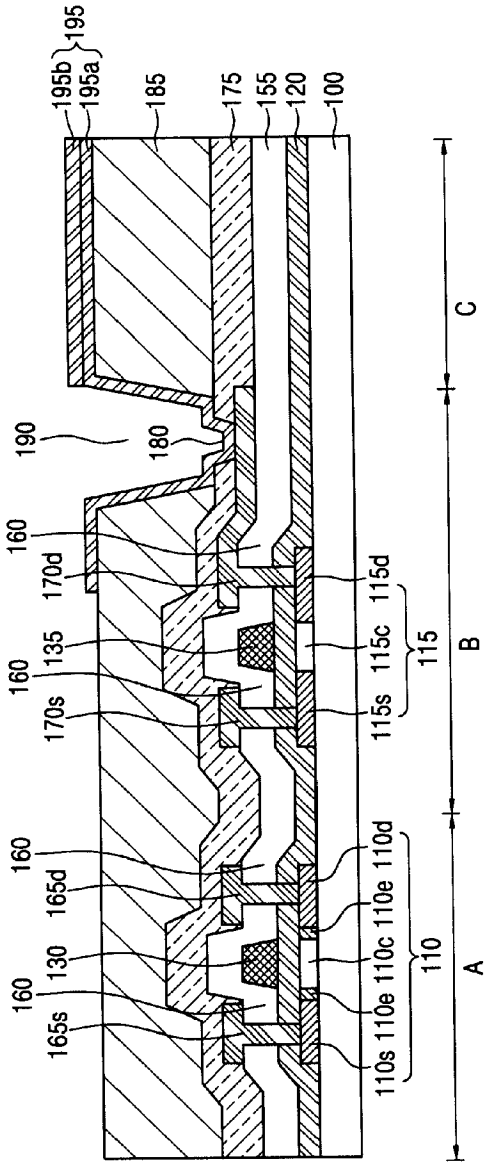
115c
115s
115
110d
110e
110c
110e
110s
110
C
B
A

FIG. 1K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180
160
170d
135
170s
165d
130
165s
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115
110d
110e
110c
110e
110s
110
A
B
C

FIG. 2A

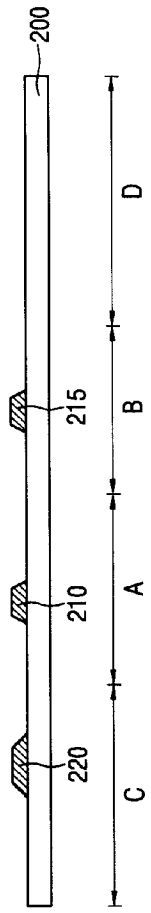
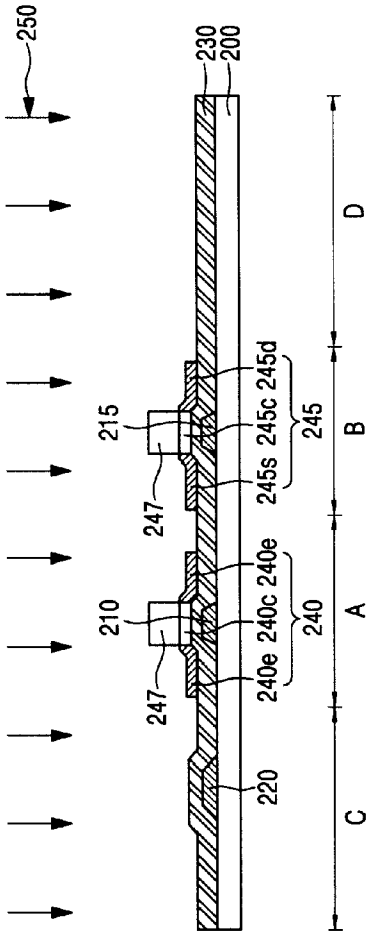


FIG. 2B


250
230
200
215
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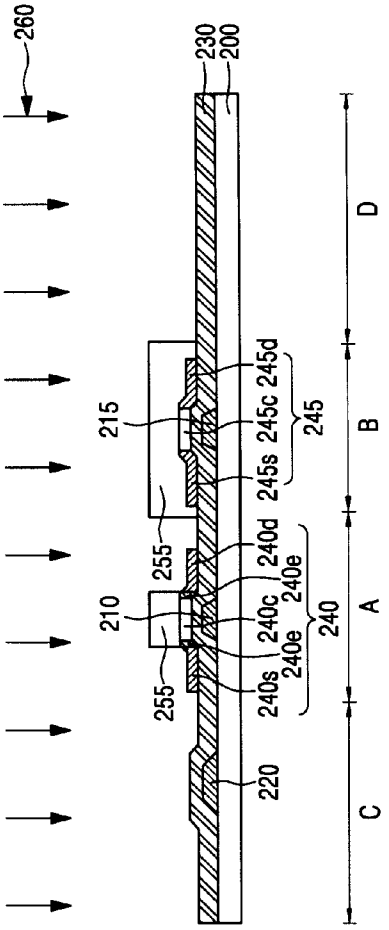
245s
245
210
247
240e
240c
240e
240
220
D
B
A
C

FIG. 2C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230
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215
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245s
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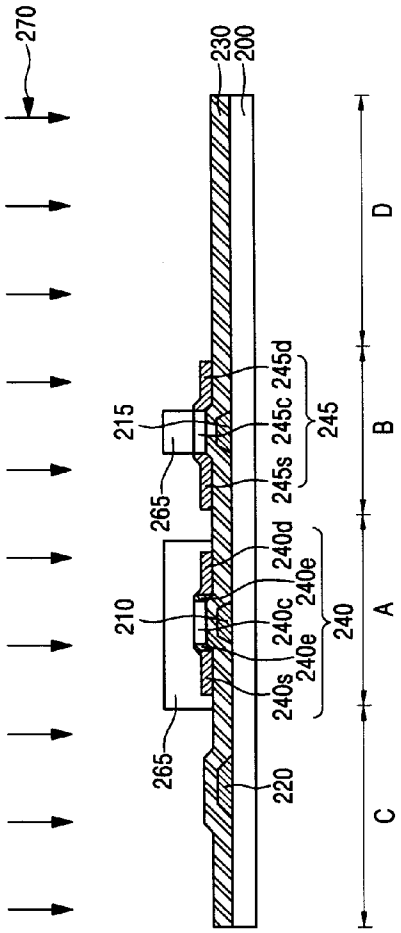
240e
240
240e
240s
255
220
D
B
A
C

FIG. 2D


270
230
200
215
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245d
245c
245s
245
240d
240e
240c
240e
240s
240
210
265
220
D
B
A
C

FIG. 2E

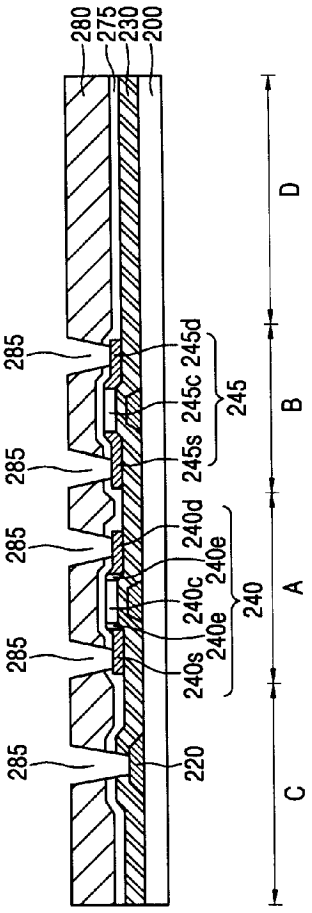
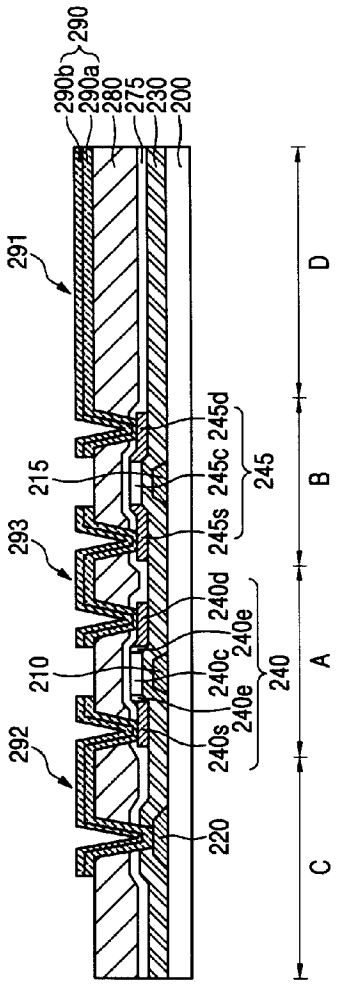

280
275
230
200
285
285
285
285
285
245d
245c
245s
245
240d
240e
240c
240e
240s
240
220
D
B
A
C

FIG. 2F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290b
290a
280
275
230
200
291
215
293
210
292
220
245d
245c
245
245s
240d
240e
240c
240e
240
240s
D
B
A
C

FIG. 2G

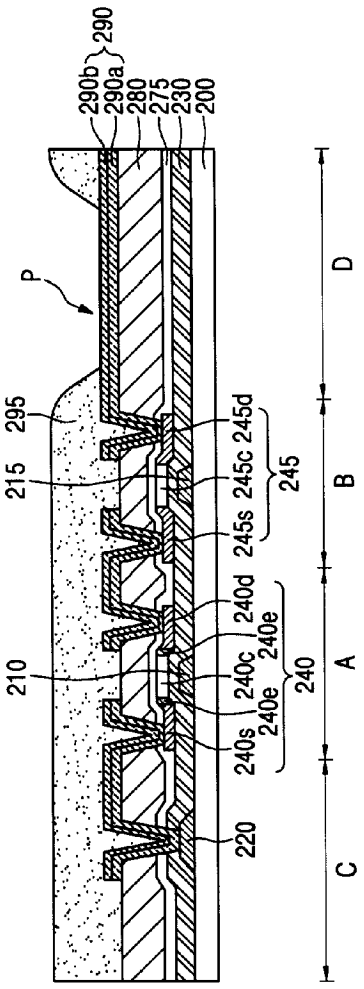
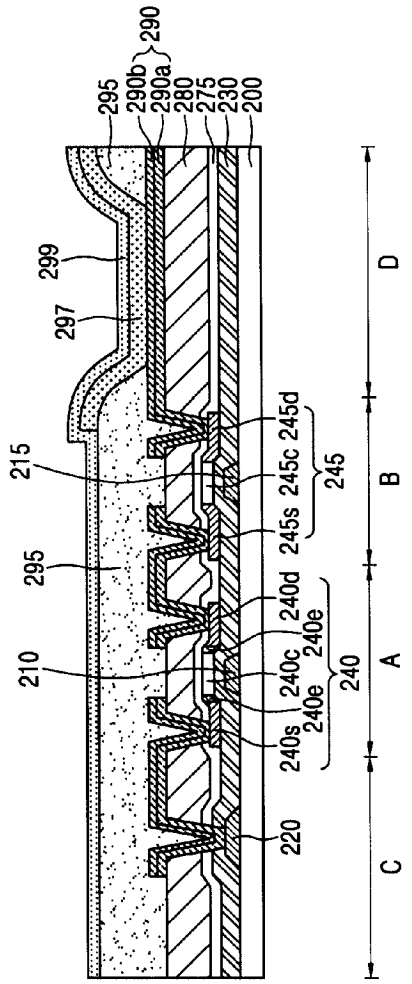

290
290b
290a
280
275
230
200
P
295
215
210
245d
245c
245s
245
240d
240e
240c
240e
240s
240
220
D
B
A
C

FIG. 2H


290
290b
290a
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280
275
230
200
299
297
215
295
210
220
245d
245c
245s
245
240d
240e
240c
240e
240s
240e
240
D
B
A
C

FIG. 3A

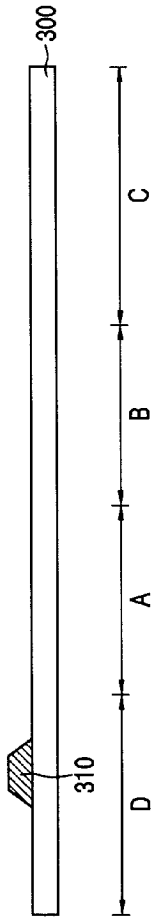


FIG. 3B

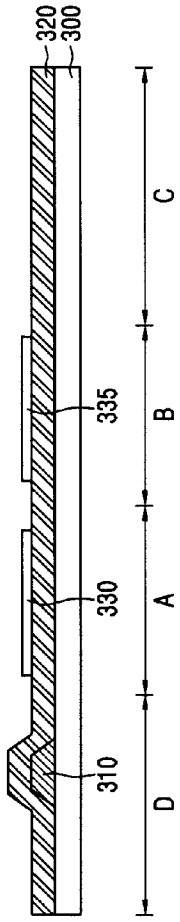


FIG. 3C

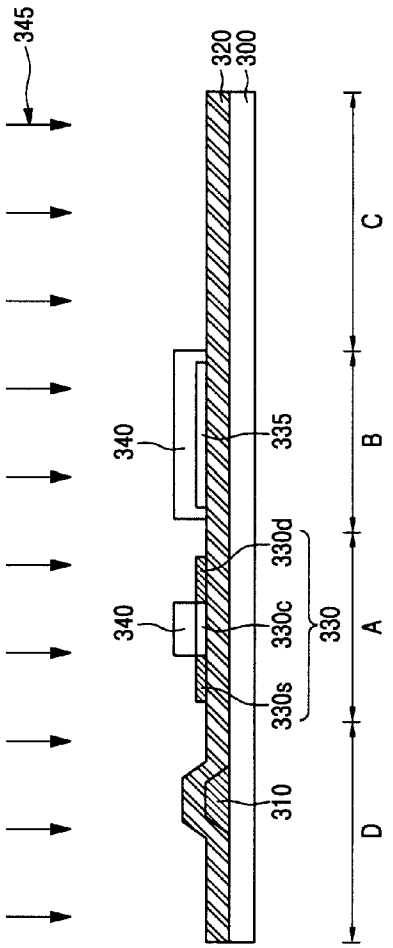


FIG. 3D

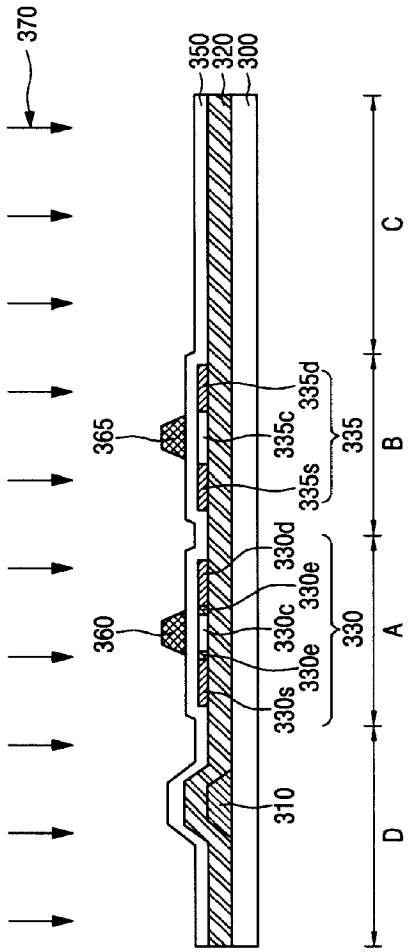
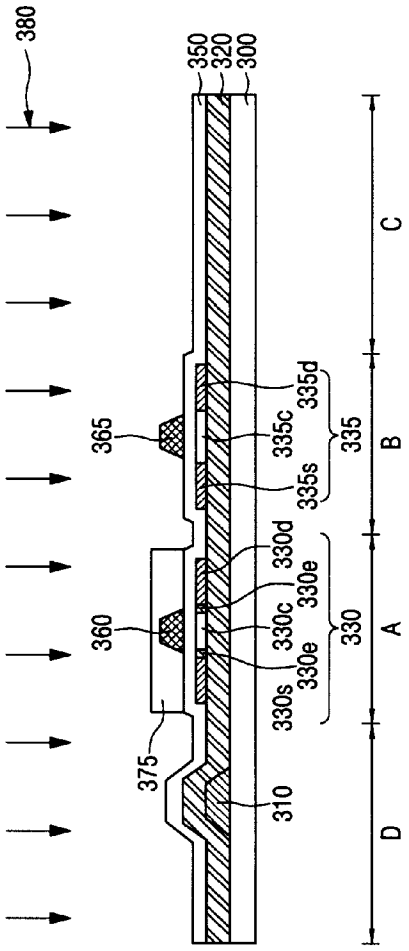

370
350
320
300
365
360
335d
335c
335s
335
330d
330e
330c
330e
330s
330
310
A
B
C
D

FIG. 3E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365
335d
335c
335s
335
360
330d
330e
330c
330e
330e
330s
330
375
310
A
B
C
D

FIG. 3F

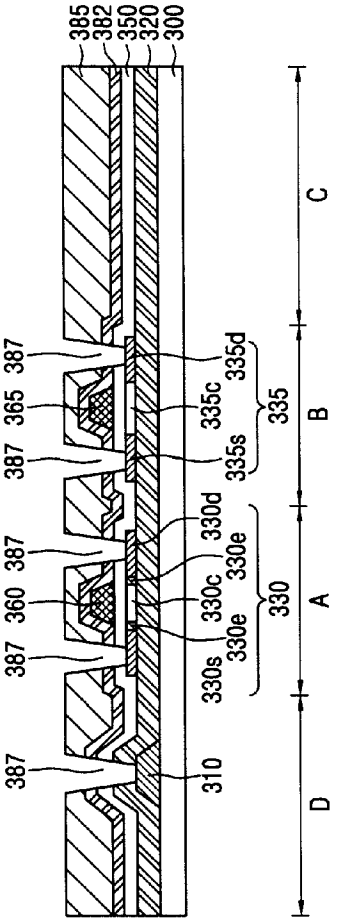
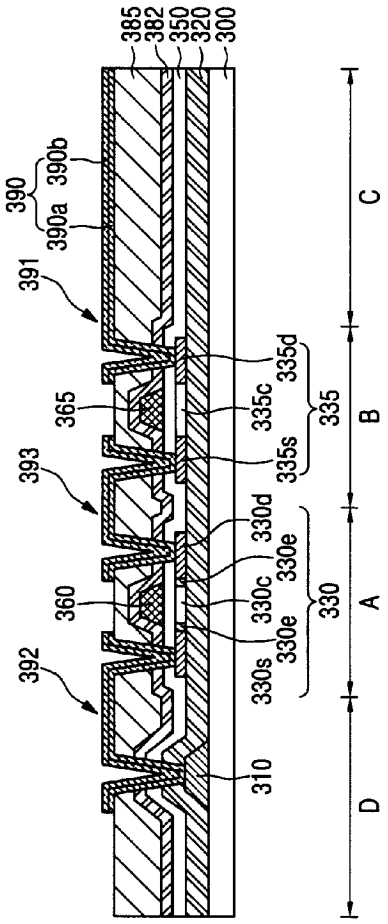

385
382
350
320
300
387
365
387
387
360
387
387
310
335d
335c
335s
335
330d
330e
330c
330e
330s
330
C
B
A
D

FIG. 3G


385
382
350
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390b
390a
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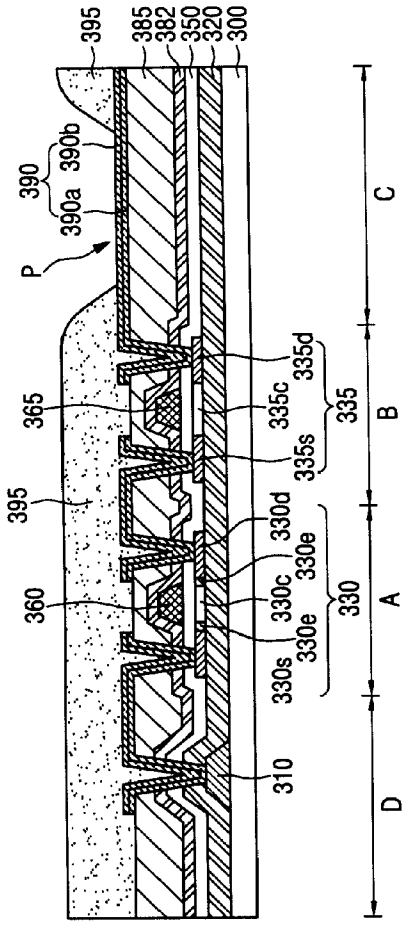
365
393
360
392
310
335d
335c
335s
335
330d
330e
330c
330e
330s
330
A
B
C
D

FIG. 3H


395
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382
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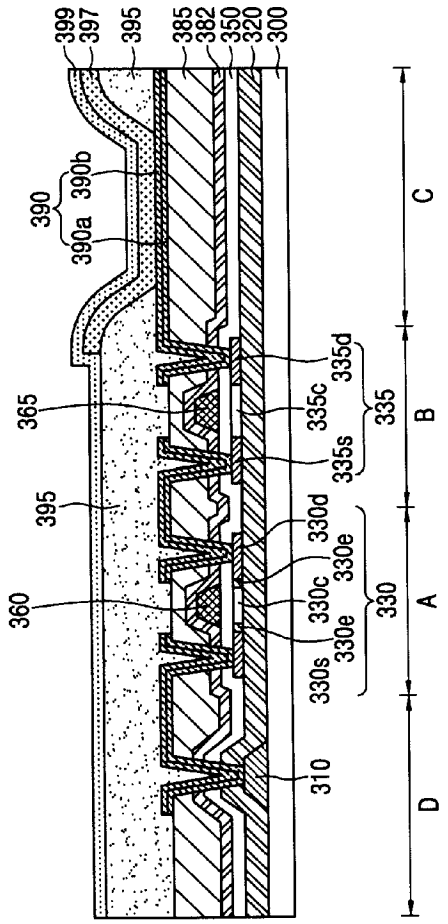
320
300
390
390b
390a
P
C
365
335d
335c
335s
335
B
395
330d
330e
330c
330e
330s
330
A
360
310
D

FIG. 3I


399
397
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382
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320
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390
390b
390a
365
395
360
310
335d
335c
335s
335
330d
330e
330c
330e
330s
330
C
B
A
D

专利名称(译)	有机发光显示装置及其制造方法		
公开(公告)号	EP1737056A2	公开(公告)日	2006-12-27
申请号	EP2006115788	申请日	2006-06-21
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	HWANG EUI HOON SAMSUNG SDI CO LTD LEE SANG GUL SAMSUNG SDI CO LTD		
发明人	HWANG, EUI-HOON SAMSUNG SDI CO.,LTD. LEE, SANG-GUL SAMSUNG SDI CO., LTD.		
IPC分类号	H01L51/56 H01L27/32		
CPC分类号	H01L27/3276 H01L27/3244 H01L51/5218 H01L51/56 H01L2251/5315		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020050054165 2005-06-22 KR		
其他公开文献	EP1737056A3 EP1737056B1		
外部链接	Espacenet		

摘要(译)

提供一种有机发光显示装置（OLED）及其制造方法。当同时形成金属互连（220）和栅电极（210,215）时或者当形成第一电极（290）时，形成用于电连接元件的互连。因此，可以减少使用的掩模的数量，从而可以缩短整个制造工艺并且可以降低生产成本。

FIG. 2H