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# (54) Scan driver, organic light emitting display using the same, and method of driving the organic light emitting display

Zeilentreiber, organische lichtemittierende Anzeige damit und Verfahren zur Ansteuerung der organischen lichtemittierenden Anzeige

Commande de capture, affichage à diodes électroluminescentes organiques l'utilisant, et procédé de commande de l'affichage à diodes électroluminescentes organiques

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## Description

### BACKGROUND

### 1. Field of the Invention

**[0001]** The present invention relates to a scan driver, an organic light emitting display using the same, and a method of driving the organic light emitting display.

### 2. Discussion of the Related Technology

**[0002]** Various flat panel displays (FPD) having smaller weight and volume compared with cathode ray tubes (CRT) have been developed recently. In particular, of FPDs, the class of light emitting displays have high emission efficiency, brightness, and response speed and large viewing angles.

**[0003]** Light emitting displays can be classified into two categories: (1) organic light emitting displays using organic light emitting diodes (OLEDs) and (2) inorganic light emitting displays using inorganic light emitting diodes. In the first category, the OLED display includes an anode electrode, a cathode electrode, and an organic emission layer. The organic emission layer is positioned between the anode electrode and the cathode electrode where it emits light by a combination of electrons and holes. In the second category, the inorganic light emitting diode referred to as a light emitting diode (LED) includes an emission layer formed of inorganic material such as a PN-junction semiconductor, as opposed to the organic emission layer of the OLED.

**[0004]** FIG. 1 schematically illustrates the structure of a conventional scan driver for a display composed of OLED pixels.

**[0005]** Referring to FIG. 1, the conventional scan driver includes a shift register 10 and a signal generator 20. The shift register 10 sequentially shifts a start pulse received from an external source in response to a clock signal CLK to generate sampling pulses. The signal generator 20 generates scan signals and emission control signals in response to the sampling pulses supplied from the shift register 10, the start pulse SP, and an output enable signal OE supplied from an external source.

**[0006]** The shift register 10 includes n (where 'n' is a natural number) D flip-flops (DF). Here, the D flip-flops DF1 to DFn are driven when the clock signal CLK and the sampling pulses (or the start pulse) are supplied from the outside. The odd D flip-flops DF1, DF3, ... are driven at the rising edge of the clock signal CLK and the even D flip-flops DF2, DF4, ... are driven at the falling edge of the clock signal CLK. That is, in the conventional shift register 10, the D flip-flops driven at the rising edge and the D flip-flops driven at the falling edge are alternately arranged.

**[0007]** The signal generator 20 includes a plurality of logic gates. Specifically, the signal generator 20 includes n NAND gates provided in scan lines S1 to Sn, respectively, and n NOR gates provided in emission control signal lines EM1 to EMn, respectively.

**[0008]** The $k^{th}$ (where 'k' is a natural number less than or equal to n; $k \leq n$) NAND gate NANDk is driven by the output enable signal OE, the sampling pulse of the $k^{th}$ D flip-flop DFk, and the sampling pulse of the $k\text{-}1^{th}$ D flip-flop DFk-1. Here, the output of the $k^{th}$ NAND gate NANDk is supplied to the $k^{th}$ scan line Sk via at least one inverter IN and buffer BU.

**[0009]** The $k^{th}$ NOR gate NORk is driven by the sampling pulse of the $k\text{-}1^{th}$ D flip-flop DFk-1 and the sampling pulse of the $k^{th}$ D flip-flop DFk. Here, the output of the $k^{th}$ NOR gate NORk is supplied to the $k^{th}$ emission control line, EMk via at least one inverter IN.

**[0010]** FIG. 2 illustrates waveforms that describe a method of driving the conventional scan driver illustrated in FIG. 1.

**[0011]** Referring to FIG. 2, the clock signal CLK and the output enable signal OE are externally supplied to the scan driver. Here, the period of the output enable signal OE is twice the frequency of the clock signal CLK, and the high voltage periods of the output enable signal OE overlap with the high voltage periods of the clock signal CLK. The output enable signal OE is supplied to control the width of the scan signals SS. Consequently, the width of the scan signals SS is equal to the width of the high voltage period of the output enable signal OE.

**[0012]** When the clock signal CLK is supplied to the shift register 10 and the output enable signal OE is supplied to the signal generator 20, the start pulse SP is externally supplied to the shift register 10 and the signal generator 20.

**[0013]** Specifically, the start pulse SP is supplied to the first D flip-flop, DF1, the first NAND gate NAND1, and the first NOR gate NOR1. The first D flip-flop DF1 that received the start pulse SP is driven at the rising edge of the clock signal CLK to generate a first sampling pulse SA1. The first sampling pulse SA1 generated by the first D flip-flop DF1 is supplied to the first NAND gate NAND1, the first NOR gate NOR1, the second D flip-flop, DF2, and the second NAND gate NAND2.

**[0014]** The first NAND gate NAND1, which received the start pulse SP, the output enable signal OE, and the first sampling pulse SA1, outputs a low voltage when all three supplied signals have a high voltage. Specifically, the first NAND gate NAND1 outputs a low voltage in a period where the first sampling pulse SA1 and the start pulse SP have a high voltage by a period in which the output enable signal OE has a high voltage. The low voltage output from the first NAND gate NAND1 is supplied to the first scan line S1 via a first inverter IN1 and a first buffer BU1. The low voltage supplied to the first scan line S1 is supplied to pixels as the scan signal SS. In the other cases, the first NAND gate NAND1 outputs a high voltage.

**[0015]** The first NOR gate NOR1 that received the start pulse SP and the first sampling pulse SA1 outputs a high voltage when both supplied signals have a low voltage.

However, the first NOR gate NOR1 outputs a low voltage when at least one of the start pulse SP and the first sampling pulse SA1 signals has a high voltage. The low voltage output from the first NOR gate NOR1 is subsequently changed into a high voltage through the second inverter IN2, and then supplied to the first emission control signal line EM1. This high voltage supplied to the first emission control signal line EM1 is supplied to the pixels as an emission control signal EMI.

**[0016]** The conventional scan driver repeats the above processes to sequentially supply the scan signals SS to the first $n^{th}$ scan lines S1 to Sn and to sequentially supply the emission control signals EMI to the first $n^{th}$ emission control lines EM1 to EMn. The scan signals SS sequentially select the pixels and the emission control signals EMI control the emission time of the pixels.

**[0017]** In an organic light emitting display, the width of the emission control signals EMI must be freely controlled regardless of the scan signals SS in order to control the brightness of the pixels. Conventionally, the width of the start pulse SP must be increased in order to increase the width of the emission control signals EMI. However, in this case, it is not possible to generate the desired scan signals SS.

**[0018]** The above explanation will be described in detail with reference to FIG. 3, in which the width of the start pulse SP is increased. The width of the start pulse SP must be increased as illustrated in FIG. 3 in order to increase the width of the emission control signals EMI. This occurs because when the width of the start pulse SP increases, the width of the emission control signal EMI, generated by the first NOR gate NOR1 performing a NOR operation on the start pulse SP and the output of the first D flip-flop DF1, increases. However, in this case, the increase in width of the start pulse SP generates undesired scan signals SS. Since the scan signals SS are generated when the start pulse SP, the first sampling pulse SA1, and the output enable signal OE, all have high voltage in the first NAND gate NAND1, the increase in width of the start pulse SP causes a plurality of low voltages to be output from the first NAND gate NAND1. In other words, a plurality of scan signals SS are generated in one frame 1F so that it is not possible to obtain desired scan signals SS.

**[0019]** When the width of the start pulse SP overlaps about two periods of the clock signal CLK, as illustrated in FIG. 3, a plurality of low voltages are output from the first NAND gate NAND1. In the conventional art, since the plurality of scan signals SS are supplied to each of the scan lines S1 to Sn when the width of the start pulse SP increases, the width of the emission control signals EMI is no more than two periods of the clock signal CLK. Also, when the width of the emission control signals EMI increases, non-emission periods increase so that flicker is generated.

**[0020]** EP 1 667 092 A1 discloses a scan driver for an organic light emitting display device which is capable of selectively performing progressive scanning and interlaced scanning.

## SUMMARY OF CERTAIN INVENTIVE ASPECTS

**[0021]** To overcome some of the shortcomings of the prior art the present invention provides an organic light emitting diode display driver as set forth in claim 1. A preferred embodiment is subject of dependent claim 2.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0022]** These and/or other objects and advantages of the invention will become apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawings of which:

**[0023]** FIG. 1 schematically illustrates the structure of a conventional scan driver;

**[0024]** FIG 2 illustrates waveforms that describe a method of driving the scan driver illustrated in FIG 1;

**[0025]** FIG. 3 illustrates waveforms that describe scan signals generated when a start pulse whose width is increased is supplied to the scan driver illustrated in FIG. 1;

**[0026]** FIG. 4 illustrates an organic light emitting display according to an embodiment of the present invention;

**[0027]** FIG. 5 schematically illustrates a scan driver according to an embodiment of the present invention;

**[0028]** FIG. 6 illustrates the structure of the scan driver illustrated in FIG. 5; and

**[0029]** FIG. 7 illustrates waveforms that describe a method of driving the scan driver illustrated in FIG. 6.

## DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

**[0030]** Hereinafter, preferred embodiments of the present invention will be described with reference to the attached drawings, that is, FIGs. 4 to 7.

**[0031]** FIG. 4 illustrates the structure of an organic light emitting display according to an embodiment of the present invention.

**[0032]** Referring to FIG. 4, the organic light emitting display according to the embodiment of the present invention includes an image display unit 130 having pixels 140 formed in the regions partitioned by scan lines S1 to Sn and data lines D1 to Dm, a scan driver 110 for driving the scan lines S1 to Sn, a data driver 120 for driving the data lines D1 to Dm, and a timing controller 150 for controlling the scan driver 110 and the data driver 120.

**[0033]** The scan driver 110 receives scan driving control signals SCS from the timing controller 150 to generate the scan signals. The generated scan signals are sequentially supplied to the scan lines S2 to Sn. The scan driver 110 also generates emission control signals in response to the scan driving control signals SCS. The generated emission control signals are supplied to emission control signal lines EM1 to EMn. Here, the scan driver

110 freely sets the width of the emission control signals to control the emission time of the pixels 140. The scan driver 110 supplies the plurality of emission control signals to the emission control lines E, respectively, in one frame, which will be described hereinafter.

**[0034]** The data driver 120 receives data driving control signals DCS from the timing controller 150 to generate the data signals. The generated data signals are supplied to the data lines D1 to Dm in synchronization with the scan signal.

**[0035]** The timing controller 150 generates the scan driving control signals SCS and the data driving control signals DCS in response to synchronizing signals supplied from the outside. The scan driving control signals SCS generated by the timing controller 150 are supplied to the scan driver 110 and the data driving control signals DCS generated by the timing controller 150 are supplied to the data driver 120. The timing controller 150 supplies data Data received from the outside to the data driver 120.

**[0036]** The image display unit 130 receives a first power source ELVDD and a second power source ELVSS from the outside to supply the first and second power sources ELVDD and ELVSS to the pixels 140. The pixels 140 that received the first and second power sources ELVDD and ELVSS generate light components corresponding to the data signals. Here, the emission time of the pixels 140 is controlled by the emission control signals.

**[0037]** FIG. 5 schematically illustrates the scan driver 110 according to an embodiment of the present invention.

**[0038]** Referring to FIG. 5, according to the embodiment of the present invention, a plurality of output enable signals OE are applied to the scan driver. For convenience sake, FIG. 5 illustrates the scan driver when two output enable signals OE are applied.

**[0039]** FIG. 6 illustrates the structure of the scan driver illustrated in FIG. 5.

**[0040]** Referring to FIG. 6, the scan driver 110 according to the embodiment of the present invention includes a shift register 162 and two signal generators 165 and 166. The scan driver 110 includes a number of signal generators equal to the number of output enable signals OE applied thereto. Here, the signal generator that receives the first output enable signal OE1 is referred to as the first signal generator 165 and the signal generator that receives the second output enable signal OE2 is referred to as the second signal generator 166. The first and second output enable signals OE1 and OE2 are sequentially applied so that the periods in which the first and second output enable signals OE1 and OE2 are supplied do not overlap.

**[0041]** The shift register 162 sequentially shifts the start pulse SP, which is externally supplied, to generate sampling pulses. The first signal generator 165 combines the sampling pulses (or the start pulse SP) supplied from the shift register 162 and the first output enable signal OE1, which is externally supplied, so as to generate the scan signals and the emission control signals. The second signal generator 166 combines the sampling pulses supplied from the shift register 162 and the second output enable signal OE2, which is externally supplied, so as to generate the scan signals and the emission control signals.

**[0042]** The shift register 162 includes n (where n is a natural number) D flip-flops DF1 to DFn. The shift register 162 sequentially generates sampling pulses using the start pulse SP supplied from the outside in the same manner as the manner in which the conventional shift register 10 sequentially generates sampling pulses. Here, the odd D flip-flops DF1, DF3, ... are driven at the rising edge of the clock signal CLK and the even D flip-flops DF2, DF4, ... are driven at the falling edge of the clock signal CLK.

**[0043]** According to aspects of the present invention, the D flip-flops DF1, DF3, ... driven at the rising edge of the clock signal CLK and the D flip-flops DF2, DF4, ... driven at the falling edge of the clock signal CLK are alternately arranged in the shift register 162. In another embodiment, and according to aspects of the present invention, the odd D flip-flops DF1, DF3, ... may be driven at the falling edge of the clock signal CLK and the even D flip-flops DF2, DF4, ... may be driven at the rising edge of the clock signal CLK.

**[0044]** The first and second signal generators 165 and 166 include a plurality of logic gates. The two signal generators 165 and 166 include a NOR gate NORk provided between a $k^{th}$ (where k is a natural number equal to or smaller than n; $k \leq n$) D flip-flop DFk and a $k^{th}$ emission control signal line EMk. They also include at least one inverter IN connected between the kth NOR gate NORk and the kth emission control signal line EMk, in order to generate the emission control signals in the same manner as the signal generator 20 of the conventional scan driver generates these signals.

**[0045]** The difference between the scan driver according to the embodiment of the present invention and the conventional scan driver lies in signals input to the NAND gates of the signal generators 165 and 166. In a conventional signal generator, the $k^{th}$ NAND gate NANDk is driven by the output enable signal OE, the sampling pulse of the $k^{th}$ D flip-flop DFk, and the sampling pulse of the $k\text{-}1^{th}$ D flip-flop DFk-1. On the other hand, in a signal generator according to the embodiment of the present invention, the $k^{th}$ NAND gate NANDk is driven by one of the output enable signals OE, e.g., OE1 and OE2, the sampling pulse of the $k^{th}$ D flip-flop DFk, and the sampling pulse of an inverted $k+1^{th}$ D flip-flop DFk+1.

**[0046]** To be specific, the first signal generator 165 according to the above embodiment includes the NAND gate NANDk, provided between the $k^{th}$ D flip-flop DFk and the $k^{th}$ scan line Sk, and at least one inverter IN and buffer BU, connected between the NAND gate NANDk and the $k^{th}$ scan line Sk. The $k^{th}$ NAND gate NANDk operates a NAND operation on the sampling pulse of the $k^{th}$ D flip-flop DFk, the first output enable signal OE1, and

the sampling pulse obtained by inverting the sampling pulse of a k+1$^{th}$ NAND gate identified as NANDk+1.

**[0047]** The second signal generator 166 includes the NAND gate NANDk, provided between the k$^{th}$ D flip-flop DFk and the k$^{th}$ scan line Sk, and at least one inverter IN and buffer BU, connected between the NAND gate NANDk and the k$^{th}$ scan line Sk. The k$^{th}$ NAND gate NANDk performs a NAND operation on the sampling pulse of the k$^{th}$ D flip-flop DFk, the second output enable signal OE2, and the sampling pulse obtained by inverting the sampling pulse of the k+1$^{th}$ NAND gate NANDk+1. As described above, according to the embodiment of the present invention, it is possible to freely control the width of the emission control signals. The scan driver 110, according to the embodiment of the present invention, which receives the two output enable signals OE1 to OE2 receives the start pulse SP twice in one frame. That is, the scan driver 110 receives a number of start pulses SP equal to the number of received output enable signals OE in one frame. Here, the output enable signal OE is applied twice in order to prevent two scan signals from being generated in one frame, which will be described in detail in FIG. 7.

**[0048]** FIG. 7 illustrates a method of driving the scan driver illustrated in FIG. 6.

**[0049]** Referring to FIG. 7, the clock signal CLK and the first and second output enable signals OE1 and OE2 are sequentially supplied externally to the scan driver 110. Here, the period of the first and second output enable signals OE1 and OE2 is 1/2 of the period of the clock signal CLK. The high level voltage of the two output enable signals OE1 and OE2 overlaps the high level voltage of the clock signal CLK.

**[0050]** The clock signal CLK is supplied to the shift register 112, the first output enable signal OE1 is supplied to the first signal generator 165, and the second output enable signal OE2 is supplied to the second signal generator 166. First and second start pulses SP1 and SP2 are sequentially supplied externally to the shift register 162 and the first signal generator 165 in one frame. The first signal generator 165 receives the first output enable signal OE1 to generate the scan signals SS and first and second emission control signals EMI1 and EMI2. The second signal generator 166 receives the second output enable signal OE2 to generate the scan signals SS and the first and second emission control signals EMI1 and EMI2. Here, when the two output enable signals OE1 and OE2 are supplied to the first and second signal generators 165 and 166, the two start pulses SP1 and SP2 are supplied to the scan driver 110 in one frame.

**[0051]** The first start pulse SP1 is supplied to the first D flip-flop DF1 and the first NOR gate NOR1. The first D flip-flop DF1 that received the first start pulse SP1 is driven at the rising edge of the clock signal CLK to generate the first sampling pulse SA1. The first sampling pulse SA1 is supplied to the first NOR gate NOR1, the first NAND gate NAND1, the second D flip-flop DF2, and the second NOR gate NOR2.

**[0052]** The first NOR gate NOR1 performs a NOR operation on the received first start pulse SP1 and first sampling pulse SA1 to generate the first emission control signal EMI1. Here, the width of the emission control signal EMI is equal to or larger than the width of the first start pulse SP1.

**[0053]** The second D flip-flop DF2 that received the first sampling pulse SA1 is driven at the falling edge of the clock signal CLK to generate the second sampling pulse SA2. The second sampling pulse SA2 is input to the first NAND gate NAND1, the second NOR gate NOR2, the second NAND gate NAND2, the third D flip-flop DF3, and the third NOR gate NOR3.

**[0054]** The first NAND gate NAND1 performs a NAND operation on the first sampling pulse SA1, the first output enable signal OE1, and the inverted second sampling pulse SA2 supplied via an inverter IN3. The first NAND gate NAND1 outputs a low level voltage when the first sampling pulse SA1, the first output enable signal OE1, and the inverted second sampling pulse SA2 are all received having a high level voltage, and outputs a high level voltage in the other cases. The first NAND gate NAND1 outputs a low level voltage by the period in which the first output enable signal OE1 has a high level voltage. At this time, the inverted second sampling pulse SA2 is supplied to the first NAND gate NAND1 so that the width of the low level voltage output from the first NAND gate NAND1 is equal to the period in which the first output enable signal OE1 has a high level voltage. That period is half of a period of the first output enable signal OE1, regardless of the width of the emission control signal EMI (or the start pulse SP). The low level voltage output from the first NAND gate NAND1 is supplied to the first scan line S1 via at least one inverter IN2 and buffer BU1, and the first scan line S 1 supplies the low level voltage supplied thereto to the pixels 140 as the scan signal SS.

**[0055]** According to the embodiment of the present invention, the above processes are repeated so that the scan driver 110 generates the scan signals SS and the emission control signals EMI. The NAND gates NAND that receive the second output enable signal OE2 combine the second output enable signal OE2 and at least two sampling pulses SA with each other to generate the scan signals SS.

**[0056]** On the other hand, when the second start pulse SP2 is supplied, the first NOR gate NOR1 performs a NOR operation on the second start pulse SP2 and the sampling pulse SA generated by the first D flip-flop to generate the second emission control signal EMI2. That is, according to the above embodiment, the two emission control signals EMI are supplied to the emission control signal lines EM1 to EMn in one frame 1F.

**[0057]** In this case, since the first output enable signal OE1 is not supplied, another scan signal SS is not generated by the first NAND gate NAND1. That is, according to the embodiment of the present invention, although the two start pulses SP1 and SP2 are applied in one frame 1F, only one scan signal SS is generated.

**[0058]** The reason why the plurality of output enable signals OE are applied will now be described in detail. Let us assume that the plurality of start pulses SP are applied in one frame 1F in order to generate the plurality of emission control signals EMI in a state where one output enable signal OE is applied. For example, when the start pulse SP is applied twice in one frame 1F, the two sampling pulses SA are generated. In this case, the signal generator receives the two sampling pulses SA and output enable signals OE to generate the two scan signals SS. That is, the two scan signals SS are supplied to the scan lines S1 to Sn in one frame 1F. However, to prevent the two scan signals SS from being supplied to the scan lines S1 to Sn in one frame 1F, the output enable signals OE (there are as many of these as there are emission control signals EMI which are supplied to the emission control signal lines EM1 to EMn) are sequentially supplied in one frame so that they do not overlap one another.

**[0059]** According to the embodiment of the present invention, the emission control signals EMI applied in one frame 1F are divided at least twice to be applied, and the width of the emission control signals is freely controlled so that it is possible to change brightness without generating flicker on a screen. Also, according to the above embodiment, it is possible to supply stable scan signals SS to the scan lines S1 to Sn regardless of the width of the start pulse SP and the number of times where the start pulse SP is applied in one frame 1F.

**[0060]** As described above, in various embodiments, it is possible to freely set the width of the emission control signals and to supply at least two emission control signals to the emission control signal lines in one frame according to the scan driver, the organic light emitting display using the same, and the method of driving the organic light emitting display. Therefore, it is possible to change the brightness of the display without generating a flicker.

## Claims

1. An organic light emitting diode display scan driver adapted to control pixel brightness by controlling the width of emission control signals including:

   a shift register (162) comprising n D flip-flops, each of the n D flip-flops receives the output of the previous D flip-flop, the input of the first D flip-flop of the shift register being adapted to receive a start pulse (SP); the shift register being adapted to generate a plurality of sampling pulses by shifting the start pulse through the n D flip-flops; each of the n D flip-flops being adapted to generate a sampling pulse,
   a first signal generator (165) adapted to receive a first output enable signal (OE1),
   a second signal generator (166) adapted to receive a second output enable signal (OE2), the first and second signal generators comprising a plurality of logic gates being adapted to combine the plurality of sampling pulses or to combine the plurality of sampling pulses and the start pulse thereby generating a plurality of scan signals and a plurality of emission control signals, said emission control signals controlling the emission time of the pixels (EM1, EM2);
   the plurality of logic gates comprising n NOR-gates (NORn), the $k^{th}$ NOR-gate having a first input connected to the input of the $k^{th}$ D flip-flop and a second input connected to the output of the $k^{th}$ D flip-flop,
   the plurality of logic gates further comprising n first inverters, the $k^{th}$ first inverter having an input connected to the output of the $k^{th}$ NOR-gate and an output connected to an emission control signal line,
   the plurality of logic gates further comprising n NAND gates (NANDn), having each a first input, a second input, a third input and an output connected to a scan signal line through a second inverter and a buffer,
   **characterised in that**
   the first input of the $k^{th}$ NAND-gate is connected to the output of the $k^{th}$ D flip-flop,
   the second input of each of the NAND-gates of the first signal generator is connected to the first output enable signal and the second input of each of the NAND-gates of the second signal generator is connected to the second output enable signal,
   and the third input of the $k^{th}$ NAND-gate is connected to an inverted output of the $(k+1)^{th}$ D flip-flop, k=1 to n and k being an integer.

2. An organic light emitting diode display (130) comprising:

   a pixel unit comprising a plurality of pixels (140) connected to a plurality of scan lines, a plurality of emission control signal lines, and a plurality of data lines (Dm);
   a data driver configured to apply data signals to the data lines (120); and
   a scan driver (110) according to claim 1.

## Patentansprüche

1. Ein Abtasttreiber für eine organische Leuchtdiodenanzeigevorrichtung, der dazu ausgelegt ist, die Pixelhelligkeit durch Steuern der Breite von Emissionssteuersignalen zu steuern, umfassend:

   ein Schieberegister (162), umfassend n D-Flip-Flops, jedes der n D-Flip-Flops empfängt den Ausgang des vorherigen D-Flip-Flops, wobei

der Eingang des ersten D-Flip-Flops des Schieberegisters dazu ausgelegt ist, einen Startimpuls (SP) zu empfangen; wobei das Schieberegister dazu ausgelegt ist, durch Verschieben des Startimpulses durch die n D-Flip-Flops eine Vielzahl von Abtastimpulsen zu generieren; wobei jedes der n D-Flip-Flops dazu ausgelegt ist, einen Abtastimpuls zu generieren,
einen ersten Signalgenerator (165), der dazu ausgelegt ist, ein erstes Ausgangsfreigabesignal (OE1) zu empfangen,
einen zweiten Signalgenerator (166), der dazu ausgelegt ist, ein zweites Ausgangsfreigabesignal (OE2) zu empfangen, wobei die ersten und zweiten Signalgeneratoren eine Vielzahl von Logikgattern umfassen, die dazu ausgelegt sind, die Vielzahl von Abtastimpulsen zu kombinieren oder die Vielzahl von Abtastimpulsen und den Startimpuls zu kombinieren und **dadurch** eine Vielzahl von Abtastsignalen und eine Vielzahl von Emissionssteuersignalen zu generieren, wobei besagte Emissionssteuersignale die Emissionszeit der Pixel (EM1, EM2) steuern;
wobei die Vielzahl von Logikgattern n NOR-Gatter (NORn) umfasst, wobei das k-te NOR-Gatter einen mit dem Eingang des k-ten D-Flip-Flops verbundenen ersten Eingang sowie einen mit dem Ausgang des k-ten D-Flip-Flops verbundenen zweiten Eingang aufweist,
wobei die Vielzahl von Logikgattern ferner n erste Inverter umfasst, wobei der k-te erste Inverter einen mit dem Ausgang des k-ten NOR-Gatters verbundenen Eingang sowie einen mit einer Emissionssteuersignalleitung verbundenen Ausgang aufweist,
wobei die Vielzahl von Logikgattern ferner n NAND-Gatter (NANDn) umfasst, deren jedes einen ersten Eingang, einen zweiten Eingang, einen dritten Eingang sowie einen durch einen zweiten Inverter und einen Puffer mit einer Abtastsignalleitung verbundenen Ausgang aufweist,
**dadurch gekennzeichnet, dass**
der erste Eingang des k-ten NAND-Gatters mit dem Ausgang des k-ten D-Flip-Flops verbunden ist,
der zweite Eingang jedes der NAND-Gatter des ersten Signalgenerators mit dem ersten Ausgangsfreigabesignal verbunden ist und der zweite Eingang jedes der NAND-Gatter des zweiten Signalgenerators mit dem zweiten Ausgangsfreigabesignal verbunden ist und der dritte Eingang des k-ten NAND-Gatters mit einem invertierten Ausgang des (k+1)-ten D-Flip-Flops verbunden ist, wobei k=1 bis n und k eine ganze Zahl ist.

**2.** Eine organische Leuchtdiodenanzeige (130), umfassend:

eine Pixeleinheit, umfassend eine mit einer Vielzahl von Abtastleitungen verbundene Vielzahl von Pixeln (140), eine Vielzahl von Emissionssteuersignalleitungen sowie eine Vielzahl von Datenleitungen (Dm);
einen Datentreiber, der dazu ausgelegt ist, Datensignale an die Datenleitungen (120) anzulegen; und
einen Abtasttreiber (110) gemäß Anspruch 1.

**Revendications**

**1.** Unité de commande de balayage pour un affichage à diodes électroluminescentes organiques adaptée pour commander la luminosité de pixels en commandant la largeur de signaux de commande d'émission comportant :

un registre à décalage (162) comprenant n bascules D, chacune des n bascules D reçoit la sortie de la bascule D précédente, l'entrée de la première bascule D du registre à décalage étant adaptée pour recevoir une impulsion de déclenchement (SP) ; le registre à décalage étant adapté pour générer une pluralité d'impulsions d'échantillonnage en décalant l'impulsion de déclenchement à travers les n bascules D ; chacune des n bascules D étant adaptée pour générer une impulsion d'échantillonnage,
un premier générateur (165) de signaux adapté pour recevoir un premier signal d'autorisation de sortie (OE1), un deuxième générateur (166) de signaux adapté pour recevoir un deuxième signal d'autorisation de sortie (OE2), les premier et deuxième générateurs de signaux comprenant une pluralité de portes logiques qui sont adaptées pour combiner la pluralité d'impulsions d'échantillonnage ou pour combiner la pluralité d'impulsions d'échantillonnage et l'impulsion de déclenchement générant de ce fait une pluralité de signaux de balayage et une pluralité de signaux de commande d'émission, lesdits signaux de commande d'émission commandant le temps d'émission des pixels (EM1, EM2) ;
la pluralité de portes logiques comprenant n portes NON-OU (NORn), la $k^{ième}$ porte NON-OU ayant une première entrée connectée à l'entrée de la $k^{ième}$ bascule D et une deuxième entrée connectée à la sortie de la $k^{ième}$ bascule D,
la pluralité de portes logiques comprenant en plus n premiers inverseurs, le $k^{ième}$ premier inverseur ayant une entrée connectée à la sortie de la $k^{ième}$ porte NON-OU et une sortie connectée à une ligne de signaux de commande

d'émission,
la pluralité de portes logiques comprenant en plus n portes NON-ET (NANDn), ayant chacune une première entrée, une deuxième entrée, une troisième entrée et une sortie connectée à la ligne de signaux de balayage à travers un deuxième inverseur et un tampon,
**caractérisée en ce que**
la première entrée de la $k^{ième}$ porte NON-ET est connectée à la sortie de la $k^{ième}$ bascule D, la deuxième entrée de chacune des portes NON-ET du premier générateur de signaux est connectée au premier signal d'autorisation de sortie et la deuxième entrée de chacune des portes NON-ET du deuxième générateur de signaux est connectée au deuxième signal d'autorisation de sortie, et la troisième entrée de la $k^{ième}$ porte NON-ET est connectée à une sortie inversée de la $(k+1)^{ième}$ bascule D, k=1 n et k étant un entier.

**2.** Affichage à diodes électroluminescentes organiques (130) comprenant :

une unité de pixels comprenant une pluralité de pixels (140) connectés à une pluralité de lignes de balayage, une pluralité de lignes de signaux de commande d'émission, et une pluralité de lignes de données (Dm) ;
une unité de commande de données configurée pour appliquer des signaux de données aux lignes de données (120) ; et
une unité commande de balayage (110) selon la revendication 1.

FIG. 1
(PRIOR ART)

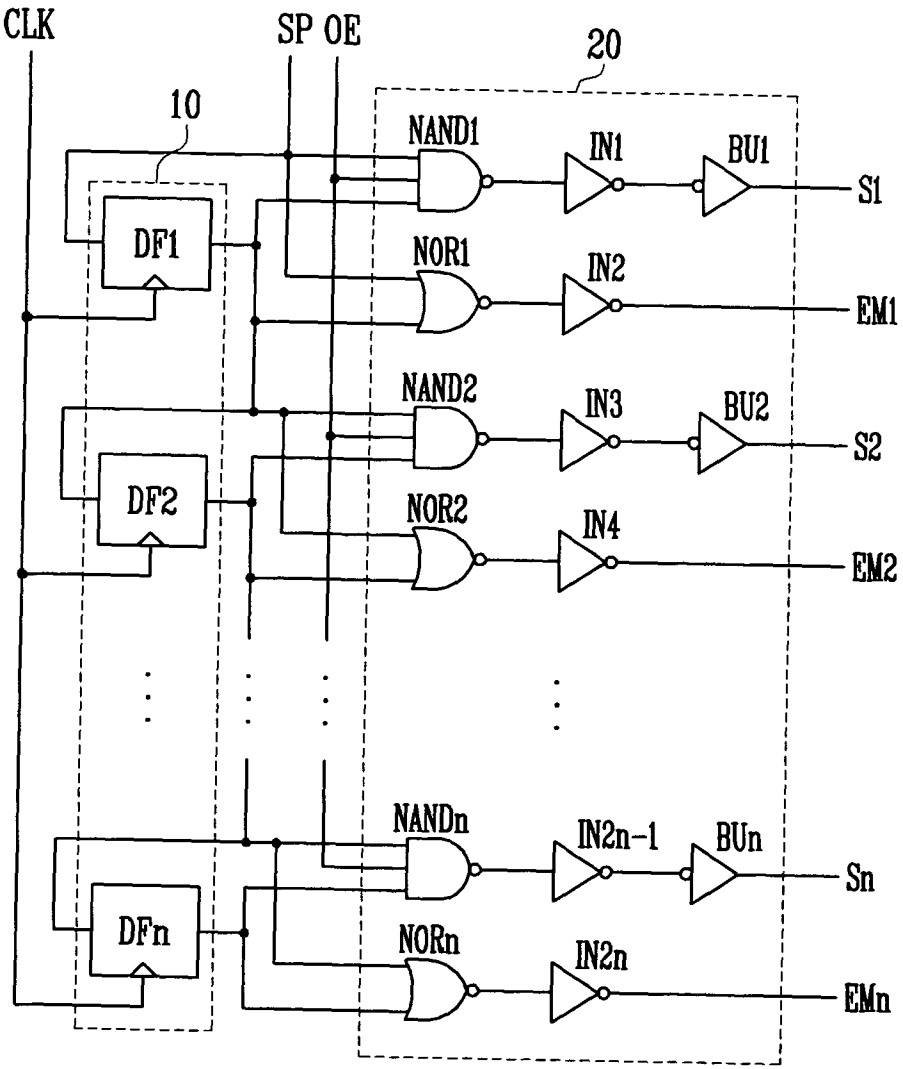


FIG. 2
(PRIOR ART)

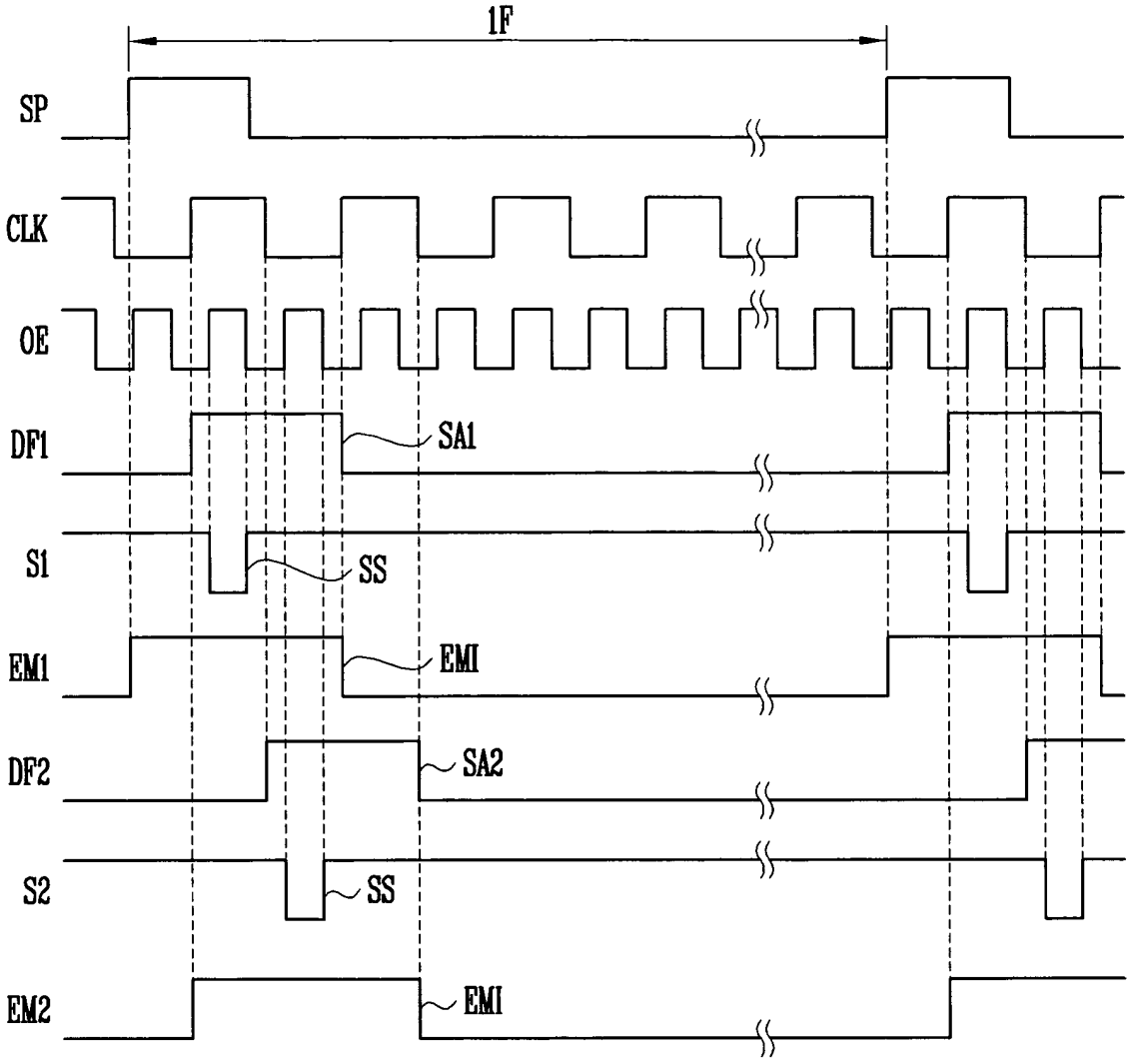


FIG. 3
(PRIOR ART)

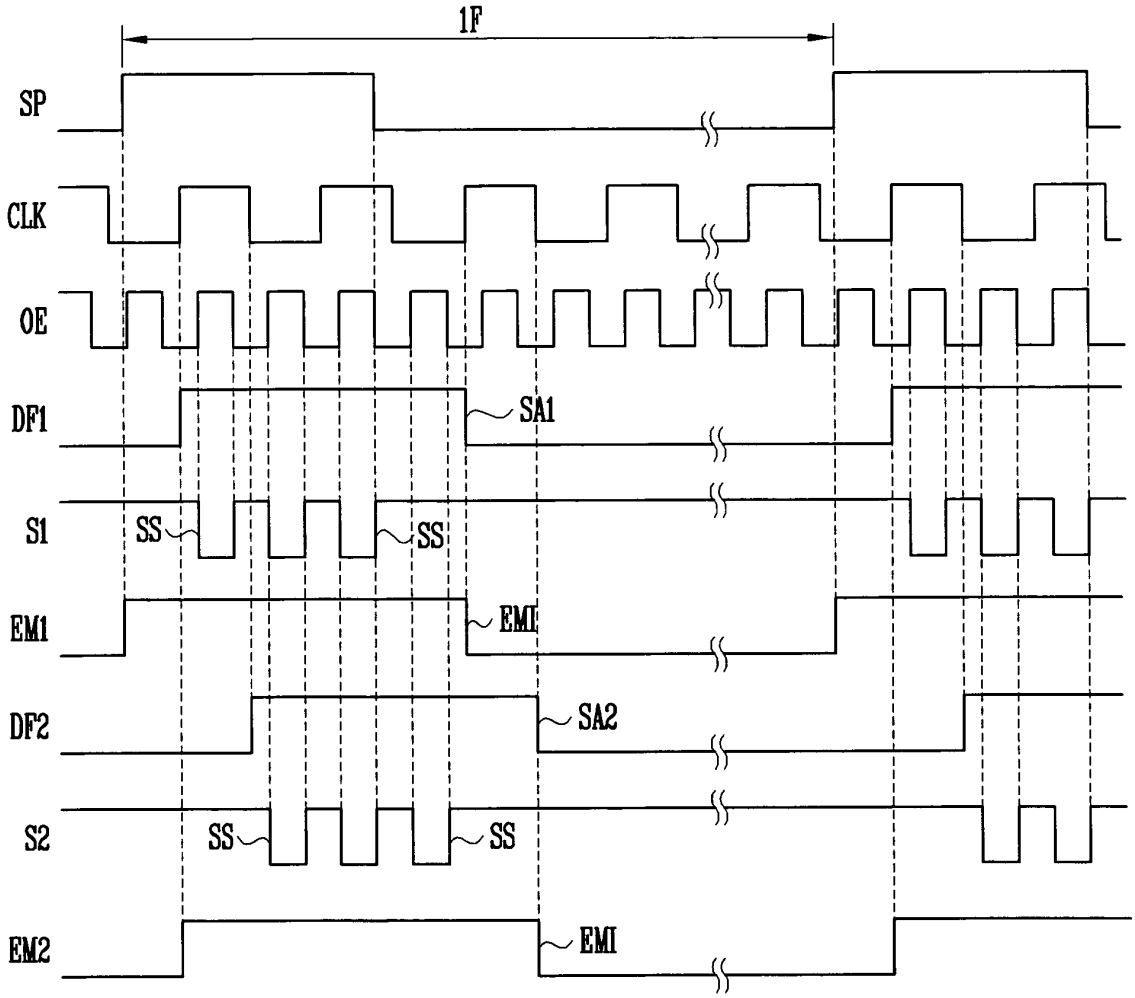


FIG. 4

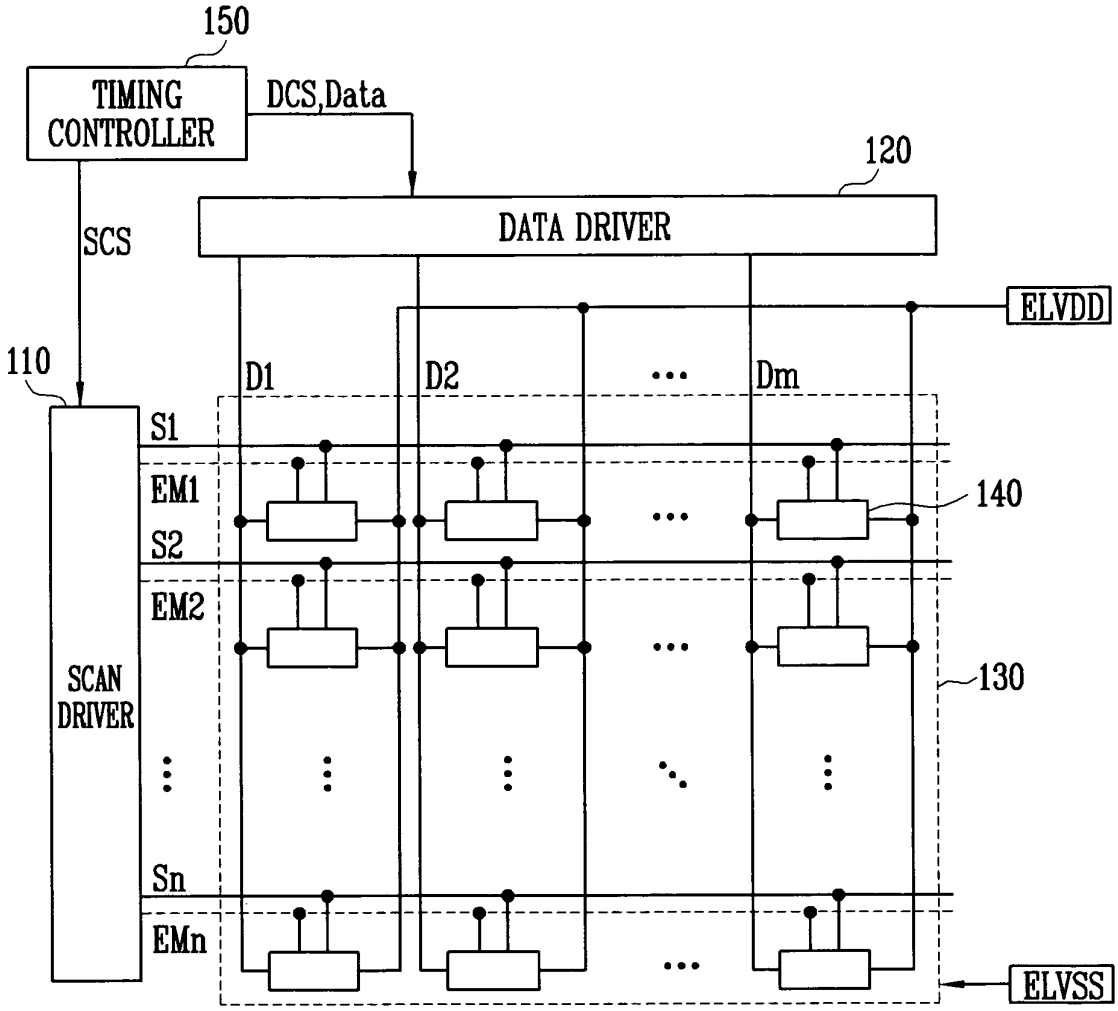

150
TIMING CONTROLLER
DCS,Data
120
DATA DRIVER
SCS
ELVDD
110
D1
D2
Dm
S1
EM1
S2
EM2
140
SCAN DRIVER
130
Sn
EMn
ELVSS

FIG. 5

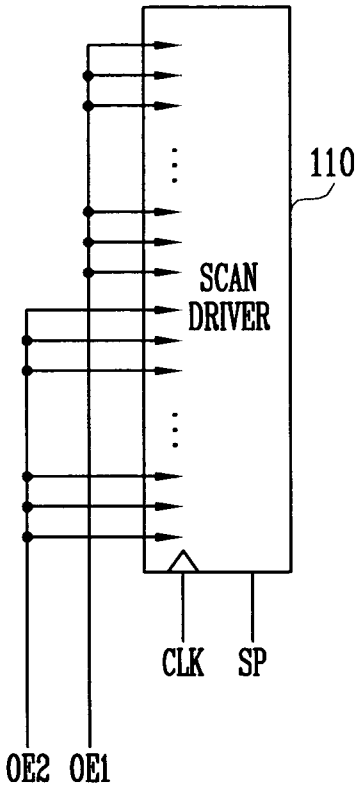


FIG. 6

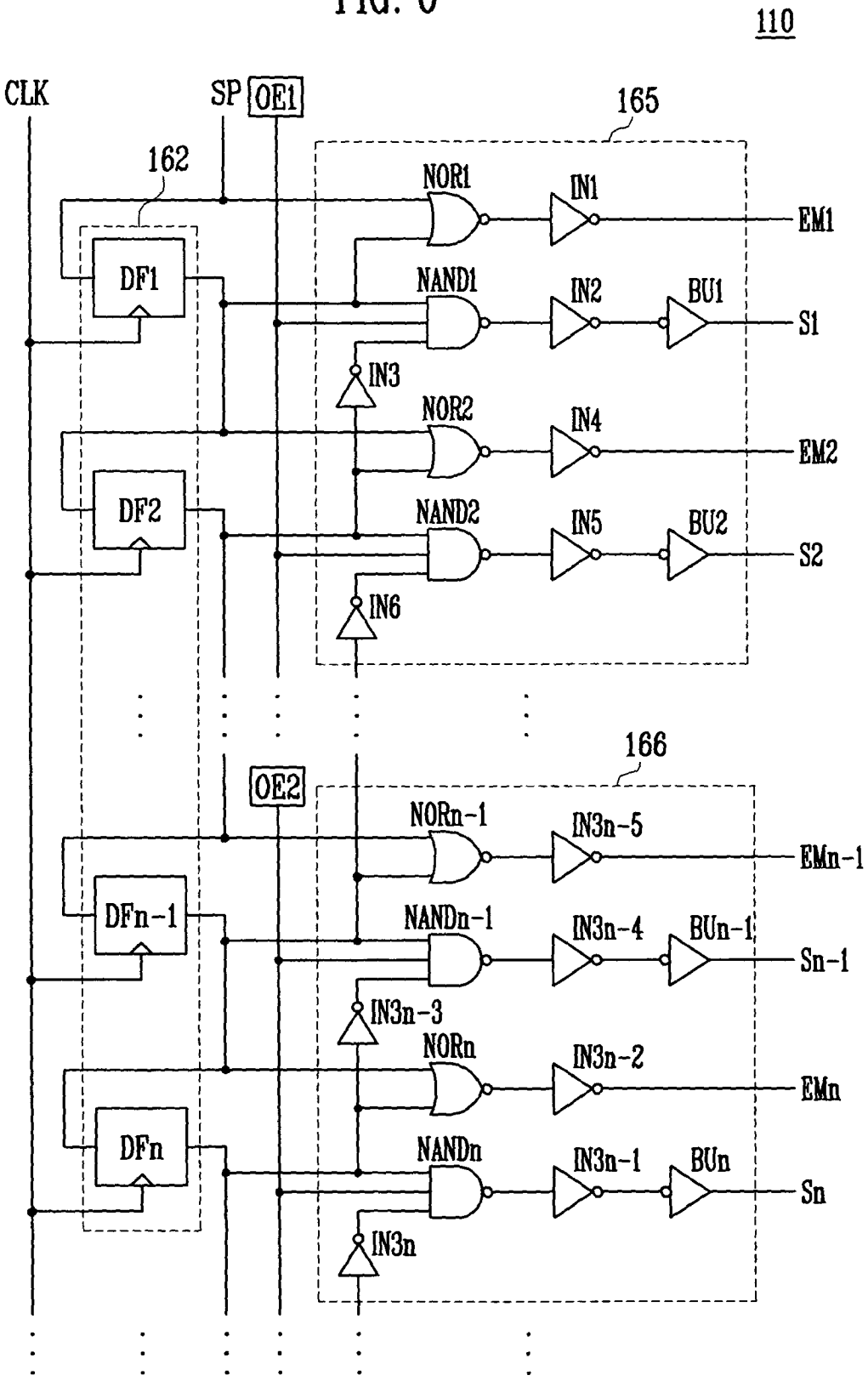
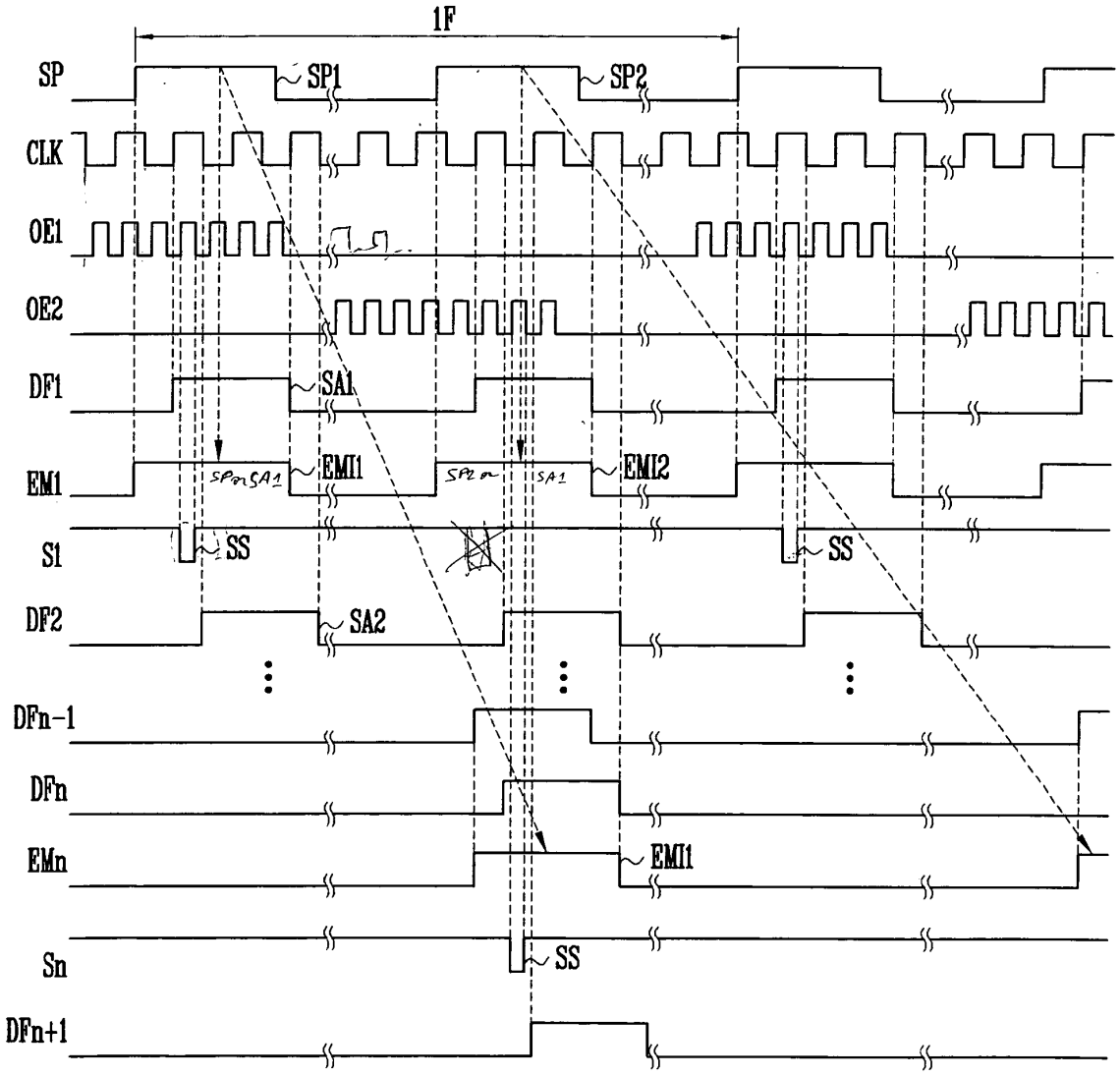

110
CLK
SP
OE1
165
162
NOR1
IN1
EM1
DF1
NAND1
IN2
BU1
S1
IN3
NOR2
IN4
EM2
DF2
NAND2
IN5
BU2
S2
IN6
166
OE2
NORn-1
IN3n-5
EMn-1
DFn-1
NANDn-1
IN3n-4
BUn-1
Sn-1
IN3n-3
NORn
IN3n-2
EMn
DFn
NANDn
IN3n-1
BUn
Sn
IN3n

FIG. 7


1F
SP
SP1
SP2
CLK
OE1
OE2
DF1
SA1
EM1
EMI1
EMI2
S1
SS
SS
DF2
SA2
DFn-1
DFn
EMn
EMI1
Sn
SS
DFn+1

## REFERENCES CITED IN THE DESCRIPTION

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### Patent documents cited in the description


- EP 1667092 A1 **[0020]**

| | | | |
|---|---|---|---|
| 专利名称(译) | 扫描驱动器，使用其的有机发光显示器，以及驱动有机发光显示器的方法 | | |
| 公开(公告)号 | EP1717790B1 | 公开(公告)日 | 2010-06-02 |
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| [标]申请(专利权)人(译) | 三星斯笛爱股份有限公司 | | |
| 申请(专利权)人(译) | 三星SDI CO.，LTD. | | |
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| [标]发明人 | CHOI SANG MOO SAMSUNG SDI CO LTD | | |
| 发明人 | CHOI, SANG MOO, SAMSUNG SDI CO., LTD. | | |
| IPC分类号 | G09G3/32 | | |
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| 代理机构(译) | hengelhaupt，Jürgen | | |
| 优先权 | 1020050035769 2005-04-28 KR | | |
| 其他公开文献 | EP1717790A8<br>EP1717790A2<br>EP1717790A3 | | |
| 外部链接 | Espacenet | | |


摘要(译)

公开了一种扫描驱动器，其能够自由地设置发射控制信号的宽度并且在一帧中将发射控制信号分成至少两次以施加发射控制信号。扫描驱动器的实施例包括移位寄存器，在一帧中接收至少两个起始脉冲以响应于时钟信号顺序地移位起始脉冲并因此产生至少两个采样脉冲，并且至少两个信号发生器用于组合至少两个采样脉冲和至少两个输出使能信号彼此提供扫描信号到扫描线，并且用于将从移位寄存器输出的至少两个采样脉冲相互组合以向发射提供至少两个发射控制信号控制一帧中的信号线。至少两个发射控制信号被提供给一帧中的发射控制信号线，使得可以改变显示器的亮度而不产生闪烁。


FIG. 1
(PRIOR ART)