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(54) **Pixel circuit**

Pixelschaltung

Circuit de pixel

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- **S.M. CHOI AND O.K.KWON: "a self-compensated voltage programming pixel structure for active-matrix organic light emitting diodes" 2003, IDW. PROCEEDINGS OF THE INTERNATIONAL DISPLAY WORKSHOPS, XX, XX, PAGE(S) 535-538 , XP008057381 * figure 5 ***

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Description

[0001] The present invention relates, in general, to a pixel circuit of a type employed in a display system using a current driven organic or other light-emission device as a light source.

[0002] Display systems commonly comprise an array of pixel circuits having an organic light-emitting device (OLED) as a light source and a driving circuit for driving the OLED in accordance with a received data signal. The OLED consists of a light-emitting polymer (LEP) layer sandwiched between an anode layer and a cathode layer. Electrically, the OLED operates as a diode whilst optically, the OLED emits light when forward biased with the brightness of the emitted light increasing as the forward bias current increases. By integrating the driving circuits of individual pixel circuits in the array using low-temperature polysilicon Thin Film Transistor (TFT) technology, it is possible to control the brightness of each individual OLED in order to provide a still or a moving image on the display.

[0003] Since an OLED is a current driven device, if the pixel circuit receives a voltage signal, a driver transistor or the like is required to supply an appropriate level of current to the OLED in response to the received voltage signal. An example of a known voltage driven pixel circuit for an active matrix OLED display is illustrated in Figure 1. Referring to Figure 1, a pixel circuit 10 comprises a first p-channel TFT T_1 and a second p-channel TFT T_2 per pixel. The first TFT T_1 is a switch for addressing the pixel circuit 10 and comprises a terminal coupled to a first supply line 12 for receiving a voltage data signal VData. The first TFT T_1 also comprises a gate terminal coupled to a second supply line 14 for receiving a supply voltage VSEL, and a terminal coupled to a gate terminal of the second TFT T_2. The second TFT T_2 comprises a terminal coupled to a third supply line 16 for receiving a supply voltage VDD, and a terminal coupled to an anode terminal of an OLED 18, a cathode terminal of the OLED 18 being coupled to ground. The second TFT T_2 is an analogue driver TFT for converting the voltage data signal VData into a current signal that in turn drives the OLED 18 at a designated brightness.

[0004] Display systems employing an array of voltage driven pixel circuits as illustrated in Figure 1 can experience non-uniformity problems in their displayed images even though individual driving TFTs in the array are supplied with an identical voltage data signal and supply voltage. The non-uniformity arises due to a spatial variation in the threshold voltage of individual driving TFTs within the array of pixel circuits that form the display. Each OLED is therefore driven at a different brightness corresponding to the difference in threshold voltage between the driving TFTs. One approach to solving the non-uniformity problem has been disclosed by S. M. Choi, et al. in "A self-compensated voltage programming pixel structure for active-matrix organic light emitting diodes", International Display Workshop 2003, p535-538. A pixel circuit embodiment as disclosed by Choi et al., is illustrated in Figure 2.

[0005] Referring to Figure 2, a pixel circuit 20 for compensating voltage threshold variations of individual driving TFTs comprises six TFTs M1, M2, M3, M4, M5 and M6, one capacitor C1 and two horizontal control lines, scan[n-1] and scan[n]. M2, M3, M4, M5 and M6 are switching TFTs, and M1 is an analogue driver TFT for providing a current that in turn drives an OLED 22 at a designated brightness during a time period of one frame.

[0006] In operation, the fourth TFT M4 provides a current path to establish a gate terminal voltage of the driver TFT M1 at a predetermined value. The capacitor C1 is a storage capacitor and stores the gate terminal voltage of the driver TFT M1. Since the pixel circuit 20 requires two row line time to complete data programming operation, the scan[n] (present row scan) and the scan[n-1] (previous row scan) signals are applied to program the pixel circuit 20.

[0007] During the previous row scan, when the scan [n-1] signal is logic low, a gate terminal voltage of the driver TFT M1 is charged to a voltage VI in a step referred to as initialisation. Next and during the present row scan, when the scan[n] signal is logic low, TFT M2 and TFT M3 are turned on so that the voltage data signal data[m] is programmed to a gate node of the driver TFT M1 through diode connected driver TFT M1. At this time, the programmed voltage at the gate node of the driver TFT M1 is automatically reduced to a value data signal voltage data[m] less a threshold voltage V_{TH} of the driver TFT M1. During initialisation and programming TFTs M5 and M6 are turned off.

[0008] Following the previous and present row scans, TFT M5 and TFT M6 are turned on by an em[n] signal to establish a current path from VDD to ground so that current can flow through the driver TFT M1 and drive the OLED 22. The driver TFT M1 therefore moderates the current independently of the voltage threshold V_{TH}.

[0009] Although the above pixel circuit 20 provides a means for compensating voltage threshold variations of individual driving TFTs, there is a need to increase the speed at which a pixel circuit can be programmed because an increase in programming speed is necessary in order that display systems can perform adequately when supplied with high bandwidth data or when employed in large size displays. Furthermore, there is a need for smaller display systems featuring lower power consumption in order to prolong the life of the power supply and expand the functionality of the system.

[0010] The paper "Pixel-Driving Methods for Large-Sized Poly-Si AM-OLED Displays" by A. Yumoto et al., Asia Display, XP-001134248, pp. 1395-1398, describes a pixel-driving circuit, in which scan drivers are placed on both sides of the pixel matrix. Each scan driver consists of four shift registers. There is one write scan line and three erase scan lines to each row, so that the emission hold time of the three colors (RGB) can be controlled separately. Integrated data-line drivers are also em-

ployed.

[0011] In accordance with a first aspect of the present invention there is provided a pixel circuit as defined in claim 1.

[0012] A display apparatus as recited in claim 10 constitutes a second aspect of the present invention.

[0013] In a third aspect of the invention a method for driving a pixel circuit comprises the steps set forth in claim 12.

[0014] When in use, the time taken for initialisation and programming of the pixel circuit according to the present invention is reduced thereby providing a more efficient, faster and more versatile display system than in the prior art. The third signal em[n] used in the prior art is no longer required since the arrangement of the pixel circuit permits signals em[n] and scan[n] to be replaced by a single control signal. In a preferred embodiment, a reference signal supply line is no longer required thereby providing a more compact display system. The number of control lines can also be reduced thereby also providing a more compact and efficient display system than is known from the prior art.

[0015] Embodiments of the present invention will now be described by way of further example only and with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a prior art voltage driven pixel circuit for an active matrix OLED display;

Figure 2 is a schematic diagram of a prior art self-compensated voltage programming pixel structure for an active-matrix OLED display;

Figure 3 is a schematic diagram illustrating two ways to diode connect a transistor;

Figure 4 is a schematic diagram of a pixel circuit according to a first embodiment of the present invention;

Figure 5 is a schematic diagram illustrating a section of the pixel circuit of Figure 4 at a steady state voltage;

Figure 6 is a schematic diagram of a pixel circuit according to a second embodiment of the present invention;

Figure 7 is a schematic diagram of a pixel circuit according to a third embodiment of the present invention;

Figure 8 is a schematic diagram of a pixel circuit according to a fourth embodiment of the present invention;

Figure 9 is a schematic diagram of a pixel circuit according to a fifth embodiment of the present invention;

Figure 10 is a schematic diagram of general driving waveforms for the pixel circuits as illustrated in Figures 4, 6, 7, 8 and 9;

Figure 11 is a schematic diagram of general driving waveforms for the pixel circuits as illustrated in Figures 6, 7, 8 and 9;

Figure 12 is a schematic diagram of architecture for the pixel circuits as illustrated in Figures 4, 6, 7 and 8;

Figure 13 is a schematic diagram of architecture for the pixel circuits as illustrated in Figure 9;

Figure 14 is a schematic diagram of a simulation of a voltage at the node newdg for the pixel circuit as illustrated in Figure 4;

Figure 15 is a schematic diagram of a simulation of an output current for varying values of ΔV_T;

Figure 16 is a schematic diagram of a simulation of an output current for different input voltages and for varying values of ΔV_T;

Figure 17 is a schematic view of a mobile telephone incorporating a display system according to the present invention;

Figure 18 is a schematic view of a mobile personal computer incorporating a display system according to the present invention; and

Figure 19 is a schematic view of a digital camera incorporating a display system according to the present invention.

[0016] Throughout the following description like reference numerals shall be used to identify like parts.

[0017] Referring to Figure 3, a driver transistor 74 having pins 1, 2, 3 can be diode-connected in two ways although in either configuration of a diode-connected transistor, a gate terminal is always connected to a drain terminal. Pins 1 and 2 can be connected thereby forming a cathode terminal with pin 3 forming an anode terminal. Alternatively, pins 2 and 3 can be connected thereby forming a cathode terminal with pin 1 forming an anode terminal.

[0018] As noted above, similar TFTs have varying threshold voltages even when they are manufactured at the same time and by the same process. All TFTs in an array can be considered to have a common nominal threshold voltage V_T. In addition, individual TFTs can be considered to have different threshold voltage variations ΔV_T. Thus, the actual threshold voltage for each TFT is $V_T + \Delta V_T$, with ΔV_T varying between TFTs.

[0019] In the present invention, driver transistors have the property that the threshold voltage $V_T + \Delta V_T$ is the same irrespective of the direction in which current flows - in other words, which terminal is set as the source and which terminal is set as the drain.

[0020] Driver transistors that are symmetrical between the source and the drain terminal and which have not been stressed have this property. In symmetrical transistors, the source and drain terminal are equally doped and are symmetrical with respect to the gate terminal. Such transistors are commonly self-aligned. For a symmetrical driver transistor 74 with a nominal threshold voltage V_T and a threshold voltage variation ΔV_T, the observed threshold voltage of the driver transistor 74 when diode connected remains $V_T + \Delta V_T$ and is independent of the way the driver transistor 74 is diode connected.

Referring to Figure 4, a pixel circuit 50 according to a first embodiment of the present invention comprises a first rail 52 having a first node 54 coupled to a first terminal of a first capacitor 56. A second terminal of the first capacitor 56 is coupled to a second node 58 (referred to as *newdg)* which is coupled to a source terminal of a first n-channel transistor 60 and a third node 62. The first n-channel transistor 60 comprises a gate terminal and also a drain terminal that is coupled to a second rail 64.

[0021] The first rail 52 comprises a fourth node. 66 coupled to a source terminal of a first p-channel transistor 68 comprising a gate terminal coupled to a fifth node 70 and a drain terminal coupled to a sixth node 72 (referred to as *int*). The sixth node 72 *int* is coupled to a first terminal of the driver transistor 74 comprising a gate terminal and a third terminal. The driver transistor 74 is a second p-channel transistor. As best seen with reference to Figure 3 and also described in detail later with reference to Figure 5, the first terminal and the third terminal of the driver transistor 74 can interchange as a source and a drain terminal depending upon whether the driver transistor 74 is diode-connected. The third terminal of the driver transistor 74 is coupled to a seventh node 76 (referred to as *ipn)* and the gate terminal is coupled to the third node 62.

[0022] The sixth node 72 *int* is also coupled to a source terminal of a second n-channel transistor 78 comprising a gate terminal coupled to an eighth node 80 and a drain terminal coupled to the third node 62. The eighth node 80 is coupled to an ninth node 82 which is coupled to a gate terminal of a third n-channel transistor 84 and to a gate terminal of a third p-channel transistor 86. A drain terminal of the third n-channel transistor 84 is coupled to the seventh node 76 *ipn* and a source terminal is coupled to a third rail 88. A source terminal of the third p-channel transistor 86 is coupled to the seventh node 76 *ipn* and a drain terminal is coupled to an anode terminal of an OLED 96 comprising a cathode terminal coupled to the fourth rail 94. A second capacitor 92 is also included in the pixel circuit 50 to represent an associated parasitic capacitance of the OLED 96.

[0023] With reference to the description above and throughout the following description, a reference to a node in the pixel circuit 50 is descriptive only. As an example, nodes 70, 80, and 82 of Figure 4 can, alternatively, be illustrated as one connection.

[0024] In operation, a voltage V_{DD} for example of 5V is applied across the pixel circuit 50 to drive the OLED 96, although other voltages can be used. As discussed above with reference to Figure 3, the driver transistor 74 has a nominal threshold voltage V_T and a threshold voltage variation ΔV_T. The observed threshold voltage of the driver transistor 74 when diode connected is therefore $V_T + \Delta V_T$. The threshold voltage variation ΔV_T is represented in Figure 4 and those following by a variable voltage source connected in series with the gate terminal of the driver transistor 74. The first n-channel transistor 60, second n-channel transistor 78 and third n-channel transistor 84 together with the first p-channel transistor 68 and third p-channel transistor 86 operate as switches under the control of a first signal $\phi 1$ and a second signal $\phi 2$ whilst the second p-channel transistor is the driver transistor 74 for supplying a controlled level of current to the OLED 96.

[0025] The pixel circuit 50 has three stages of operation: a pre-charge stage, a self-adjustment stage and an output stage.

[0026] In the pre-charge stage, the first signal $\phi 1$ is logic 1 and is applied to the gate terminal of the second n-channel transistor 78, the third n-channel transistor 84, the first p-channel transistor 68 and the third p-channel transistor 86. The second n-channel transistor 78 and the third n-channel transistor are therefore switched on whilst the first p-channel transistor 68 and the third p-channel transistor 86 are switched off. Also in the pre-charge stage, the second signal $\phi 2$ is logic 1 and is applied to the gate terminal of the first n-channel transistor 60 thereby switching on the first n-channel transistor 60. The driver transistor 74 is therefore diode-connected using the second n-channel transistor 78, isolated from the V_{DD} to ground path by the switching off of the first p-channel transistor 68 and the second node 58 *newdg* is earthed through the switching on of the first n-channel transistor 60.

[0027] The third rail 88 is at a voltage V_{DAT} that in the pre-charge stage of the present embodiment is, for example, 0V although other voltages can be used. Consequently, the second node 58, *newdg*, is pre-charged to a voltage V*newdg* equal to that of the second rail 64 such as ground (0V) and the pixel circuit 50 can be represented by the pixel circuit 50 illustrated in Figure 5(a). As such, the voltage across the first capacitor 56 which is given by V_{DD} - V*newdg* = 5V.

[0028] The second node 58 *newdg* and the sixth node 72 *int* are connected through the second n-channel transistor 78 and the voltage across the second node 58 V*newdg* equals the voltage across the sixth node 72 V*int.* The supply rail 88 that supplies the voltage V_{DAT} is connected to the seventh node 76 *ipn* through the third n-channel transistor 84 and the voltage across the seventh node 76 V*ipn* equals V_{DAT}. As such, the second node 58

newdg is the cathode terminal and the seventh node 76 *ipn* is the anode terminal of the diode-connected driver transistor 74.

[0029] In the self-adjustment stage, and more particularly during data transfer of the self-adjustment stage, the first signal $\phi 1$ remains logic 1 applied to the gate terminal of the second n-channel transistor 78, the third n-channel transistor 84, the first p-channel transistor 68 and the third p-channel transistor 86. The second n-channel transistor 78 and the third n-channel transistor remain switched on whilst the first p-channel transistor 68 and the third p-channel transistor 86 remain switched off.

[0030] The second signal $\phi 2$ becomes logic 0 applied to the gate terminal of the first n-channel transistor 60 thereby switching off the first n-channel transistor 60 causing the second node, *newdg* to no longer be earthed.

[0031] Voltage V_{DAT} now pulses to a required value of V_{DAT} for driving the OLED 96, for example 3V. Preferably, the commencement of the pulse to the required value of V_{DAT} occurs simultaneously or later than the switching off of the first n-channel transistor 60.

[0032] Since the second node 58, *newdg,* is pre-charged to ground (0V) and is less than V_{DAT} (3V), the diode-connected driver transistor 74 is forward-biased and current, I, flows to the first capacitor 56 to discharge the first capacitor 56 until a steady state is reached.

[0033] At steady state, V*newdg* = V_{DAT} - (V_T + ΔV_T). The voltage across the first capacitor 56 is therefore: V_{DD} - V*newdg* = V_{DD} - (V_{DAT} - (V_T + ΔV_T)) If a value of 1.1V is provided for the nominal threshold voltage V_T, the voltage across the first capacitor 56 at steady state equals 3.1V + ΔV_T. The time taken for steady state to be reached is primarily dependent upon the RC time constant generated between the first capacitor 56 and the impedance of the second n-channel transistor 78 that enables the driving transistor 74 to be diode-connected. Although less significant, the resistance of the driver transistor 74 and the third n-channel transistor 84 also contribute to the time taken for steady state to be reached.

[0034] The effective voltage of the gate terminal, V*dg* = V*newdg* + ΔV_T. Therefore, when steady. state is reached, the effective voltage of the gate terminal V*dg* can be written as V*dg* = V_{DAT} - V_T, = 1.9V which is independent of any threshold variation ΔV_T.

[0035] In the output stage, the first signal $\phi 1$ is logic 0 and is applied to the gate terminal of the second n-channel transistor 78, the third n-channel transistor 84, the first p-channel transistor 68 and the third p-channel transistor 86. The second n-channel transistor 78 and the third n-channel transistor are therefore switched off whilst the first p-channel transistor 68 and the third p-channel transistor 86 are switched on. In the output stage, the second signal $\phi 2$ remains logic 0.

[0036] As best shown in Figure 5(b), in the output stage, the driver transistor 74 is no longer diode-connected between the first terminal and the gate terminal and therefore acts as a constant current source for the OLED 96. The amplitude of the current passed to the OLED 96 by the driver transistor 74 is dependent on the value of V_{DAT} (more specifically, the value that V_{DAT} pulses to in the self-adjustment stage) and not the threshold variation ΔV_T. Therefore, all pixel circuits 50 in an array forming a display are driven to the same brightness for the same value of V_{DAT}.

[0037] Exemplary driving waveforms for the pixel circuit 50 as illustrated in Figure 4 are illustrated in Figure 10. Referring to Figure 10(a), the first signal $\phi 1$ and the second signal ϕ 2 are both logic 1 indicating the commencement of the pre-charge stage in order to set the second node 58 *newdg* to a voltage equal to ground as described above. As the second signal $\phi 2$ drops to logic 0, the self-adjustment stage commences and V_{DAT} pulses to a value of e.g., 3V. Since, the second node 58, *newdg,* is pre-charged to a voltage equal to that of ground and is less than V_{DAT} (3V), the diode-connected driver transistor 74 is forward-biased and current, I, flows to the first capacitor 56 to discharge the first capacitor 56 until a steady state is reached. On reaching a steady state, the first signal $\phi 1$ becomes logic 0 and the output stage commences so as to drive the OLED 96 independently of threshold variation ΔV_T. As should be appreciated by a person skilled in the art, the driving waveforms illustrated in Figures 10(b) to (d) are also equally applicable for use with the pixel circuit 50 described above.

[0038] In common with the arrangements discussed below, the arrangement shown in figure 4 has the advantages that the time taken for initialisation and programming of the pixel circuit is significantly reduced compared with prior art arrangements, thereby providing a more efficient, faster and more versatile display system. Moreover, the size of an individual pixel circuit is reduced in the present invention, thereby providing a more compact and efficient display with an improved aperture ratio.

[0039] In an alternative embodiment to the pixel circuit 50 of Figure 4, the first n-channel transistor 60 is coupled to a supply line V_{SS} instead of the second rail 64. The cathode terminal of the OLED 96 can also or instead be coupled to the supply line V_{SS} rather than to the fourth rail 94.

[0040] Referring to Figure 6, the pixel circuit 50 of Figure 4 according to a second embodiment of the present invention comprises an additional fourth p-channel transistor 98 comprising a source terminal coupled to the drain terminal of the third p-channel transistor 86 and a drain terminal coupled to the anode terminal of the OLED 96.

[0041] In operation, in the pre-charge stage, the second signal $\phi 2$ is applied to a gate terminal of the fourth p-channel transistor 98. The first n-channel transistor 60 is switched on and the fourth p-channel transistor 98 is switched off thereby isolating the OLED 96 during the pre-charge stage even if the first signal ϕ 1 is logic 0 when the second signal $\phi 2$ is logic 1. The second embodiment therefore allows different driving waveforms to be used as described below with reference to Figures 11(a) and 11(b).

[0042] Referring to Figure 11 (a) and (b), the second signal $\phi 2$ is logic 1 prior to the first signal $\phi 1$ becoming logic 1. If these driving waveforms were to be used in the circuit of Figure 4, then when the second signal $\phi 2$ is logic 1 node newdg 58 is earthed and the gate voltage of the p-type driving transistor is earthed as well. Thus, the driving transistor 74 may be briefly switched on before the first signal $\phi 1$ is logic 1 and transistors 68 and 86 are switched off. At that time, the OLED 96 would be briefly driven to the maximum brightness. However, in the pixel circuit of Figure 6 this does not matter since switch 98 is switched off when switch 60 is switched on and the OLED 96 is isolated, as discussed above.

[0043] Referring to Figure 7, the pixel circuit 50 of Figure 4 according to a third embodiment of the present invention comprises an additional fifth p-channel transistor 102 and an additional fourth n-channel transistor 104. The fourth n-channel transistor 104 comprises a source terminal coupled to the first rail 52 and a drain terminal coupled to a node 108 referred to as *newdg2.* The node *newdg2* is coupled to the third node 62 - that is, node *newdg2* and the third node 62 are technically the same - and to a first terminal of the fifth p-channel transistor 102. The fifth p-channel transistor 102 comprises a second terminal coupled to the second node 58 *(newdg).*

[0044] In operation, in the pre-charge stage, the second signal $\phi 2$ is applied to a gate terminal of the fourth n-channel transistor 104 and a gate terminal of the fifth p-channel transistor 102. When the second signal $\phi 2$ is logic 1 and the first n-channel transistor 60 is switched on, the fifth p-channel transistor 102 is switched off and the fourth n-channel transistor 104 is switched on thereby ensuring that the driver transistor 74 is also off in order to isolate the OLED 96.

[0045] Driving waveforms described above and below with reference to Figures 11(a) and 11(b) can also be used with the pixel circuit 50 shown in Figure 7. More specifically, in Figure 7 node newdg2 108 is held at V_{DD} all the time that node newdg 58 is earthed, so the gate voltage of the driving transistor equals V_{DD} and the driving transistor is not switched on. Accordingly, there is no need for transistor 98 provided in Figure 6.

[0046] In an alternative to the arrangement shown in Figure 7, transistor 104 can be changed from an n-channel transistor to a p-channel transistor and transistor 102 can be changed from a p-channel transistor to an n-channel transistor. This is beneficial for drawing current from the power supply V_{DD}. However, with the gates of both of the thus altered transistors connected to the second signal $\phi 2$, the two transistors act as an inverter. If only this change were to be made, the resultant inverter would output the inverted second signal $\phi 2$bar at node *newdg2.* Thus, at the same time $\phi 2$ is high so that transistor 60 is switched on and node *newdg* is earthed, the inverter formed by transistors 104, 102 would output the inverted $\phi 2$bar (in other words a low) at *newdg2.* In that circumstance, the p-type driving transistor would be switched on and the OLED would emit before $\phi 1$ goes high and before the driving transistor is diode connected.

[0047] To counter this, a further inverter is added between the second signal line and the inverter formed by altered transistors 104, 102. Accordingly, the signal input to the inverter formed by altered transistors 104, 102 is $\phi 2$bar. Thus, at the same time $\phi 2$ is high so that transistor 60 is switched on and node *newdg* is earthed, the inverter formed by transistors 104, 102 has $\phi 2$bar as an input and outputs the $\phi 2$ (in other words a high) at *newdg2.* Consequently, the p-type driving transistor is switched off so the OLED 96 does not emit before $\phi 1$ goes high and before the driving transistor is diode connected.

[0048] Referring to Figure 8, a fourth embodiment of the present invention comprises the pixel circuit 50 of Figure 7 with the fourth n-channel transistor 104 in an alternative configuration as transistor 107. The fourth n-channel transistor 104 comprises a terminal coupled to the sixth node 72 *int* and a terminal coupled to the second node *newdg.* The fourth n-channel transistor 104 comprises a gate terminal coupled to the eighth node 80 for receiving the first signal $\phi 1$.

[0049] In operation and when the first signal $\phi 1$ is logic 1 during the pre-charge stage and the self-adjustment stage, the fourth n-channel transistor 104 is switched on in order to improve the conductive path between the seventh node *ipn* and the second node *newdg.*

[0050] Referring to Figure 9, the pixel circuit 50 of Figure 4 according to a fifth embodiment of the present invention comprises a terminal of the first n-channel transistor 60 coupled to the seventh node *ipn* instead of being coupled to the second rail 64. Therefore, the driver transistor 74 is coupled to a terminal of the third p-channel transistor 86 and a terminal of the third n-channel transistor 84.

[0051] In operation, the voltage V_{DAT} provides a pre-charge stage voltage to the second node *newdg* through the first n-channel transistor 60 and the third n-channel resistor 84. Therefore the second rail 64 is no longer needed as ground (0V) nor as replaced by a supply line V_{SS}. During the pre-charge stage, the voltage V_{DAT} must be less than the voltage that V_{DAT} pulses to in the self-adjustment stage so that the driver transistor 74 can behave as a forward-biased diode-connected transistor.

[0052] Exemplary driving waveforms for the pixel circuit 50 as illustrated in Figure 9 are illustrated in Figure 11(b). In the pre-charge stage, when the first signal $\phi 1$ is logic 0 and the second signal $\phi 2$ becomes logic 1, node *newdg* initially discharges through the first n-channel transistor 60, the third p-channel transistor 86 and the OLED 96 to ground. The first signal $\phi 1$ becomes logic 1 and V_{DAT} increases to a value V_{DAT} low. As such, the driver transistor 74 becomes diode connected and the node *newdg* is initialised to the voltage V_{DAT} low through the third n-channel transistor 84 and the first n-channel transistor 60, the driver transistor 74 and the second n-channel transistor 78.

[0053] As the second signal $\phi 2$ drops to logic 0, and in the self-adjustment stage, V_{DAT} low increases to a val-

ue V_{DAT} high. As such, the node *newdg* increases to a value V_{DAT} high - (V_T + ΔV_T) through the third n-channel transistor 84, the driver transistor 74 and the second n-channel transistor 78.

[0054] At the output stage, the first signal ϕ1 is logic 0 and the driver transistor 74 is no longer diode-connected between the first terminal and the gate terminal. The driver transistor 74 therefore acts as a constant current source for the OLED 96 through the first p-channel transistor 68, the driver transistor 74 and the third p-channel transistor 86. The amplitude of the current passed to the OLED 96 by the driver transistor 74 is dependent on the value of V_{DAT} (more specifically, the value of V_{DAT} high in the self-adjustment stage) and not the threshold variation ΔV_T. Therefore, all pixel circuits 50 in an array forming a display are driven to the same brightness.

[0055] In a further alternative, the transistor 98 shown in Figure 6 can also be included in each of the arrangements shown in Figures 7 to 9. Thus, in each case the pixel circuit includes p-channel transistor 98 coupled in series between transistor 86 and the OLED 96. The control signal ϕ2 is applied to the gate of p-channel transistor 98 so that p-channel transistor 98 is switched off whilst n-channel transistor 60 is switched on.

[0056] Referring to Figure 12, an architecture for the pixel circuit 50 as illustrated in Figures 4, 6, 7, and 8 is shown in an array 150 forming a display system. The array 150 is driven by any one of the exemplary waveforms of Figure 10 or Figures 11(a). Each pixel circuit 50 of the array 150 comprises a ground line Gnd, which can be replaced by a supply line V_{SS} as discussed above. The architecture also comprises two separate horizontal control lines to supply the first and second supply signals ϕ 1 and ϕ2.

[0057] Referring to Figure 13, an architecture for the pixel circuit 50 as illustrated in Figure 9 is shown in an array 200 forming a display system. By employing a waveform as illustrated in Figure 11(d) in the case of the pixel circuit 50 as illustrated in Figure 9 a reduction in the number of horizontal control lines is demonstrated when compared to the architecture of Figure 12.

[0058] The reduction in the number of horizontal control lines is realised since the control line SEL,2 (referred to as a control signal V_{SELn+1} in Figures 11(c) and (d)) provides both the first control signal ϕ 1 and the second control signal ϕ2 for adjacent pixel circuits 50.

[0059] Of course, the architecture shown in Figure 12, in which two signal lines are provided for each row of pixels, could be adjusted so that the capacitor in each pixel circuit discharges to a data line VDAT instead of to ground Gnd, similar to Figure 13. By employing a waveform as illustrated in Figure 11(c) in the case of the pixel circuit 50 as illustrated in Figures 6, 7 and 8 a reduction in the number of horizontal lines would be demonstrated when compared to the architecture of Figure 12.

[0060] Similarly, the architecture shown in Figure 13, in which signal lines are shared between adjacent rows of pixels, could be adjusted so that the capacitor in each pixel circuit discharges to ground Gnd instead of to a data line VDAT, similar to Figure 12. By employing a waveform as illustrated in Figure 11(b) in the case of the pixel circuit 50 as illustrated in Figure 9 a reduction in the number of horizontal control lines would be demonstrated when compared to the architecture of Figure 12.

[0061] Of course, the arrays in Figures 12 and 13 are also applicable to all suitable alternatives of the pixel circuits of the present invention, whether or not described above.

[0062] It is noted that in each of Figures 11(a) to (d) the first and second control signals ϕ1 and ϕ2 are overlapping. That is, ϕ1 is high for a part of the time that ϕ2 is high and ϕ2 is high for a part of the time that ϕ1 is high. However, ϕ1 is also high for a part of the time that ϕ2 is low and ϕ2 is also high for a part of the time that ϕ1 is low. This possibility of using overlapping control signals, which is hitherto unknown, allows increased scanning speeds and consequently improves the quality of displayed moving images.

[0063] Referring to Figure 14, a simulation of the voltage *Vnewdg* at the second node 58 for the pixel circuit 50 as illustrated in Figure 4 is shown graphically against time in microseconds. In the pre-charge stage (labelled as PRESET in Figure 12) the voltage *Vnewdg* drops substantially to ground (0V). In the self-adjustment stage (labelled as PROGRAM) in Figure 12 the voltage *Vnewdg* climbs to a value V_{DAT} - (V_T + ΔV_T) as V_{DAT} pulses to a voltage for driving the OLED 96. In the output stage (referred to as LOCK DOWN) in Figure 12, the voltage *Vnewdg* is maintained by the first capacitor 56 until the process is repeated. As can be readily appreciated from Figure 12, the voltage V*newdg* varies with respect to varying values of ΔV_T.

[0064] From Figure 14 it can be seen that the pre-charge and self-adjustment stages can be completed in a matter of only a few microseconds. This is approximately two orders of magnitude (or 100 times) faster than that achieved in the prior art. In addition, lower voltages can be used. Accordingly, the present invention provides improved display quality and reduced power consumption. Moreover, a pixel circuit and a display device according to the present invention are smaller and more compact than those of the prior art.

[0065] Referring to Figure 15, a simulation of an output current (IOLED) for driving the OLED 96 is plotted against varying values of ΔV_T. As such, Figure 15 demonstrates that the output current IOLED is the same, irrespective of ΔV_T, so the pixel circuits forming an array can be driven to the same brightness despite varying values of ΔV_T.

[0066] Figure 16, illustrates a similar effect. In Figure 16(a), the output current IOLED is plotted graphically against time in microseconds for varying values of input voltages, V_{DD}, which result in varying amplitudes of output current IOLED, and varying values of ΔV_T, which do not affect output IOLED. Figure 16(b) shows variation of IOLED with variation in V_{DAT}, for different ΔV_T. The output current IOLED is substantially equal, irrespective of ΔV_T,

and therefore output currents IOLED for respective values of ΔV_T are superimposed. The pixel circuits forming an array can therefore be driven to the same brightness despite varying values of ΔV_T.

[0067] A display system 1000 using the pixel circuit 50 as described above is advantageous for use in small, mobile electronic products such as mobile phones, personal digital assistants (PDA), computers, CD players, DVD players and the like - although it is not limited thereto.

[0068] Several terminal devices in which the display system 1000 can be embedded will now be described.

[0069] An example in which the display system 1000 is applied to a portable or mobile phone will be described. Figure 17 is an isometric view illustrating the configuration of the portable phone. In the drawing, the portable phone 1200 is provided with a plurality of operation keys 1202, an earpiece 1204, a mouthpiece 1206, and the display system 1000 in the form of a display panel. The mouthpiece 1206 or earpiece 1204 may be used for outputting speech.

[0070] An example in which the display system 1000 according to one of the above embodiments is applied to a mobile personal computer will now be described.

[0071] Figure 18 is an isometric view illustrating the configuration of this personal computer. In the drawing, the personal computer 1100 is provided with a body 1104 including a keyboard 1102 and the display system 1000 in the form of a display panel.

[0072] Next, a digital still camera using the display system 1000 will be described. Figure 19 is an isometric view illustrating the configuration of the digital still camera and the connection to external devices in brief.

[0073] Typical cameras sensitise films based on optical images from objects, whereas the digital still camera 1300 generates imaging signals from the optical image of an object by photoelectric conversion using, for example, a charge coupled device (CCD). The digital still camera 1300 is provided with the display system 1000 in the form of a display panel at the back face of a case 1302 to perform display based on the imaging signals from the CCD. Thus, the display system 1000 functions as a finder for displaying the object. A photo acceptance unit 1304 including optical lenses and the CCD is provided at the front side (behind in the drawing) of the case 1302. The display system 1000 may be embodied in the digital still camera.

[0074] Further examples of terminal devices, other than the portable phone shown in Figure 17, the personal computer shown in Figure 18, and the digital still camera shown in Figure 19, include a personal digital assistant (PDA), television sets, view-finder-type and monitoring-type video tape recorders, car navigation systems, pagers, electronic notebooks, portable calculators, word processors, workstations, TV telephones, point-of-sales system (POS) terminals, and devices provided with touch panels. Of course, the display system of the present invention can be applied to any of these terminal devices.

[0075] The aforegoing description has been given by way of example only and a person skilled in the art will appreciate that modifications can be made without departing from the scope of the present invention.

Claims

1. A pixel circuit for driving a current-driven element, the pixel circuit including:

a capacitor (56);
a current-driven element (96);
a first transistor (60), which is connected in series with the capacitor (56) and has a first gate terminal arranged to receive a first control signal (ϕ_2);
a second transistor (74) for driving the current-driven element (96), the second transistor (74) having a second gate terminal connected to a first node (58) between the first transistor (60) and the capacitor (56);
a third transistor (78), which is arranged to diode-connect the second transistor (74) in response to a second control signal (ϕ_1) received at a third gate terminal of the third transistor (78), and which is further arranged to control an electrical connection between a second node (72) between the second and fourth transistors (74, 68) and the first node (58);
a fourth transistor (68), which is connected in series with the second transistor (74) and is connected between a power supply line (V_{DD}) and the second transistor (74);
a fifth transistor (86), which is connected in series with the current-driven element (96) and the second transistor (74), and
a sixth transistor (84), which is arranged to control an electrical connection between a data signal line (V_{DAT}) and a third node (76) between the second transistor (74) and the fifth transistor (86), the sixth transistor having a sixth gate terminal that receives the second control signal (ϕ_1);
characterized in that:

the fourth transistor (68) has a fourth gate terminal, which receives the second control signal (ϕ_1);
the fifth transistor (86) has a fifth gate terminal that receives the second control signal (ϕ_1), and
the sixth transistor (84) has a channel-type different from that of the fifth transistor (86).

2. The pixel circuit according to claim 1,
wherein the sixth transistor (84) is of an n-channel type.

3. The pixel circuit according to claim 1 or claim 2, further comprising:

a seventh transistor (98), which is connected between the fifth transistor (86) and the current-driven element (96).

4. The pixel circuit according to any one of claims 1 to 3, further comprising:

an eighth transistor (102), which is connected between the first node (58) and the second gate terminal.

5. The pixel circuit according to claim 4, further comprising:

a ninth transistor (104), which is connected between the eighth transistor (102) and the power supply line (V_{DD}).

6. The pixel circuit according to claim 5, wherein the ninth transistor (104) has a channel-type different from that of the eighth transistor (102).

7. The pixel circuit according to claim 5 or claim 6, wherein the second gate terminal is connected to a fourth node (108) between the eighth transistor (102) and the ninth transistor (104).

8. The pixel circuit according to any one of the preceding claims, further comprising:

a tenth transistor (105), which is connected between the first node (58) and one of a source and a drain of the third transistor (78), and
an eleventh transistor (107), which is connected between the first node (58) and the other the source and drain of the third transistor (78).

9. The pixel circuit according to any one of the preceding claims, wherein the current-driven element (96) is a light-emitting element.

10. A display apparatus comprising the pixel circuit according to any one of the preceding claims.

11. A display apparatus according to claim 10, further comprising:

a first control-signal line (SEL,1), a second control-signal line (SEL,2), a third control-signal line (SEL,3) and a data-signal line (VDAT,1) in a matrix, the first control-signal line (SEL,1) providing the second control signal (ϕ_1) for a first pixel circuit (50) and the second control-signal line (SEL, 2) providing the first control signal (ϕ_2) for the first pixel circuit;
wherein a second control signal (ϕ_1) for a second pixel circuit is the first control signal (ϕ_2) for the first pixel circuit provided by the second control-signal line (SEL,2), and the third control-signal line (SEL,3) provides a first control signal (ϕ_2) for the second pixel circuit.

12. A method for driving a pixel circuit, the method comprising:

applying a first control signal (ϕ_2) to switch on a first transistor (60) via a first gate terminal of said first transistor (60), the first transistor (60) being connected between a power supply line (V_{DD}) and a reference line (64; 88) and in series with a first capacitor (56);
applying a second control signal (ϕ_1) to switch on a third transistor (78) to diode-connect a second transistor (74), the second transistor (74) being a driving transistor for a current-driven element (96) and having a second gate terminal, which is connected to a first node (58) between the first transistor (60) and the capacitor (56), the second transistor (74) being connected in series with the current-driven element (96) and having a first terminal for receiving a data signal (V_{DAT});
applying the first control signal (ϕ_2) to switch off the first transistor (60);
applying the data signal (V_{DAT}) to the first terminal of the second transistor (74);
applying the second control signal (ϕ_1) to switch off the third transistor (78), and
applying the second control signal (ϕ_1) to a fourth transistor (68), which is connected in series between the power supply line (V_{DD}) and the second transistor (74) and to a fifth transistor (86), which is connected in series between the current-driven device (96) and the second transistor (74), to switch off the fourth and fifth transistors (68, 86) while the third transistor (78) is switched on, and to switch on the fourth and fifth transistors (68, 86) while the third transistor (78) is switched off, wherein one terminal of the third transistor (78) is coupled to one terminal of the second transistor (74) at a second node (72) between the second transistor (74) and the fourth transistor (68);
wherein the step of applying the data signal (V_{DAT}) to the first terminal of the second transistor (74) is carried out by applying the second control signal (ϕ_1) to a sixth transistor (84), which is connected between a data-signal line (88) and a third node (76) between the second transistor (74) and the fifth transistor (86) to switch on the sixth transistor (84) while the third transistor (78) is switched on and to switch off the sixth tran-

sistor (84) while the third transistor (78) is switched off,
and the method further comprises:

providing the fifth and sixth transistors (86, 84) such that they have different channel-types.

13. A method according to claim 12, further comprising:

applying the first control signal (ϕ_2) to a seventh transistor (98), which is coupled in series between the fifth transistor (86) and the current-driven device (96), to switch off the seventh transistor (98) while the first transistor (60) is switched on, wherein the seventh transistor (98) is of the opposite channel-type to the first transistor (60).

14. A method according to claim 12 or claim 13, further comprising:

applying the first control signal (ϕ_2) to an eighth transistor (102), which is coupled in series between the second gate terminal and the first node (58), and to a ninth transistor (104), which is coupled between the power supply line (V_{DD}) and a fourth node (108) between one terminal of the eighth transistor (102) and the second gate terminal, wherein the ninth transistor (104) is of the same channel-type as the first transistor (60) and the eighth transistor (102) is of the opposite channel-type to the first transistor (60), to switch off the eighth transistor (102) and switch on the ninth transistor (104) while the first transistor (60) is switched on.

15. A method according to any one of claims 12 to 14, further comprising:

applying the first control signal (ϕ_2) to a tenth transistor (105), which is connected between the first node (58) and the terminal of the third transistor (78) which is connected to the second gate terminal, and
applying the second control signal (ϕ_1) to an eleventh transistor (107), which is coupled between the first node (58) and the other terminal of the third transistor, which is connected to a second terminal of the second transistor, wherein the tenth transistor (105) is of an opposite channel-type to the eleventh transistor (107), to switch off the tenth transistor (105) when the first transistor (60) is switched on and to switch on the eleventh transistor (107) when the third transistor (78) is switched on.

16. A method according to claim 12, wherein the reference line is a data-signal line (88), wherein the first transistor (60) is connected in series between the sixth transistor (84) and the capacitor (56), the method comprising:

after applying the first control signal (ϕ_2) to switch on the first transistor (60) and before the applying the first control signal (ϕ_2) to switch off the first transistor (60), applying a pre-charge signal on the data-signal line, the pre-charge signal having a value lower than that of the data signal (V_{DAT}).

Patentansprüche

1. Pixelschaltung zum Ansteuern eines stromgesteuerten Elements, wobei die Pixelschaltung enthält:

einen Kondensator (56);
ein stromgesteuertes Element (96);
eine erster Transistor (60), der in Serie mit dem Kondensator (56) geschaltet ist und eine erste Gate-Anschlussklemme aufweist, die zum Empfangen eines ersten Steuersignals (ϕ_2) angeordnet ist;
einen zweiten Transistor (74) zum Ansteuern des stromgesteuerten Elements (96), wobei der zweite Transistor (74) eine zweite Gate-Anschlussklemme aufweist, die an einen ersten Knoten (58) zwischen dem ersten Transistor (60) und dem Kondensator (56) angeschlossen ist;
einen dritten Transistor (78), der so angeordnet ist, dass der zweite Transistor (74) als Reaktion auf ein zweites Steuersignal (ϕ_1) als Diode geschaltet wird, das an einer dritte Gate-Anschlussklemme des dritten Transistors (78) empfangen wird, und der des Weiteren so angeordnet ist, dass er eine elektrisch Verbindung zwischen einem zweiten Knoten (72) zwischen dem zweiten und vierten Transistoren (74, 68) und dem ersten Knoten (58) steuert;
einen vierten Transistor (68), der in Serie mit dem zweiten Transistor (74) geschaltet ist und zwischen einer Energieversorgungsleitung (V_{DD}) und dem zweiten Transistor (74) angeschlossen ist;
einen fünften Transistor (86), der in Serie mit dem stromgesteuerten Element (96) und dem zweiten Transistor (74) geschaltet ist, und
einen sechsten Transistor (84), der zur Steuerung einer elektrischen Verbindung zwischen einer Datensignalleitung (V_{DAT}) und einem dritten Knoten (76) zwischen dem zweiten Transistor (74) und dem fünften Transistor (86) angeordnet ist, wobei der sechste Transistor eine sechste Gate-Anschlussklemme aufweist, die das zwei-

te Steuersignal (Φ_1) empfängt;
dadurch gekennzeichnet, dass:

der vierte Transistor (68) eine vierte Gate-Anschlussklemme aufweist, die das zweite Steuersignal (ϕ_1) empfängt;
der fünfte Transistor (86) eine fünfte Gate-Anschlussklemme aufweist, die das zweite Steuersignal (ϕ_1) empfängt, und
der sechste Transistor (84) einen Kanaltyp aufweist, der sich von jenem des fünften Transistors (86) unterscheidet.

2. Pixelschaltung nach Anspruch 1,
wobei der sechste Transistor (84) vom n-Kanaltyp ist.

3. Pixelschaltung nach Anspruch 1 oder Anspruch 2, des Weiteren umfassend:

einen siebenten Transistor (98), der zwischen dem fünften Transistor (86) und dem stromgesteuerten Element (96) angeschlossen ist.

4. Pixelschaltung nach einem der Ansprüche 1 bis 3, des Weiteren umfassend:

einen achten Transistor (102), der zwischen dem ersten Knoten (58) und der zweiten Gate-Anschlussklemme angeschlossen ist.

5. Pixelschaltung nach Anspruch 4, des Weiteren umfassend:

einen neunten Transistor (104), der zwischen dem achten Transistor (102) und der Energieversorgungsleitung (V_{DD}) angeschlossen ist.

6. Pixelschaltung nach Anspruch 5,
wobei der neunte Transistor (104) einen Kanaltyp aufweist, der sich von jenem des achten Transistors (102) unterscheidet.

7. Pixelschaltung nach Anspruch 5 oder Anspruch 6,
wobei die zweite Gate-Anschlussklemme an einen vierten Knoten (108) zwischen dem achten Transistor (102) und dem neunten Transistor (104) angeschlossen ist.

8. Pixelschaltung nach einem der vorangehenden Ansprüche, des Weiteren umfassend:

einen zehnten Transistor (105), der zwischen dem ersten Knoten (58) und einem von einer Source und einem Drain des dritten Transistors (78) angeschlossen ist, und
einen elften Transistor (107), der zwischen dem ersten Knoten (58) und dem anderen von der Source und dem Drain des dritten Transistors (78) angeschlossen ist.

9. Pixelschaltung nach einem der vorangehenden Ansprüche,
wobei das stromgesteuerte Element (96) ein Lichtemissionselement ist.

10. Anzeigevorrichtung, umfassend die Pixelschaltung nach einem der vorangehenden Ansprüche.

11. Anzeigevorrichtung nach Anspruch 10, des Weiteren umfassend:

eine erste Steuersignalleitung (SEL,1), eine zweite Steuersignalleitung (SEL,2), eine dritte Steuersignalleitung (SEL,3) und eine Datensignalleitung (VDAT,1) in einer Matrix, wobei die erste Steuersignalleitung (SEL,1) das zweite Steuersignal (ϕ_1) für eine erste Pixelschaltung (50) bereitstellt, und die zweite Steuersignalleitung (SEL,2) das erste Steuersignal (ϕ_2) für die erste Pixelschaltung bereitstellt;
wobei ein zweites Steuersignal (ϕ_1) für eine zweite Pixelschaltung das erste Steuersignal (ϕ_2) für die erste Pixelschaltung ist, das von der zweiten Steuersignalleitung (SEL,2) bereitgestellt wird, und die dritte Steuersignalleitung (SEL,3) ein erstes Steuersignal (ϕ_2) für die zweite Pixelschaltung bereitstellt.

12. Verfahren zum Ansteuern eines Pixelschaltung, wobei das Verfahren umfasst:

Anlegen eines ersten Steuersignals (ϕ_2) zum Einschalten eines ersten Transistors (60) über eine erste Gate-Anschlussklemme des ersten Transistors (60), wobei der erste Transistor (60) zwischen einer Energieversorgungsleitung (V_{DD}) und einer Referenzleitung (64; 88) und in Serie mit einem ersten Kondensator (56) angeschlossen ist;
Anlegen eines zweiten Steuersignals (ϕ_1) zum Einschalten eines dritten Transistors (78), um einen zweiten Transistor (74) als Diode zu schalten, wobei der zweite Transistor (74) ein Ansteuerungstransistor für ein stromgesteuertes Element (96) ist und eine zweite Gate-Anschlussklemme aufweist, die an einen ersten Knoten (58) zwischen dem ersten Transistor (60) und dem Kondensator (56) angeschlossen ist, wobei der zweite Transistor (74) in Serie mit dem stromgesteuerten Element (96) geschaltet ist und eine erste Anschlussklemme zum Empfangen eines Datensignals (V_{DAT}) aufweist;
Anlegen des ersten Steuersignals (ϕ_2) zum Ausschalten des ersten Transistors (60);
Anlegen des Datensignals (V_{DAT}) an die erste

Anschlussklemme des zweiten Transistors (75);
Anlegen des zweiten Steuersignals (ϕ_1) zum Ausschalten des dritten Transistors (78), und
Anlegen des zweiten Steuersignals (ϕ_1) an einen vierten Transistor (68), der in Serie zwischen der Energieversorgungsleitung (V_{DD}) und dem zweiten Transistor (74) geschaltet ist, und an einen fünften Transistor (86), der in Serie zwischen der stromgesteuerten Vorrichtung (96) und dem zweiten Transistor (74) geschaltet ist, um den vierten und fünften Transistor (68, 86) auszuschalten, während der dritte Transistor eingeschaltet ist, und um den vierten und fünften Transistor (68, 86) einzuschalten, während der dritte Transistor (78) ausgeschaltet ist, wobei eine Anschlussklemme des dritten Transistors (78) an eine Anschlussklemme des zweiten Transistors (74) an einem zweiten Knoten (72) zwischen dem zweiten Transistor (74) und dem vierten Transistor (68) gekoppelt ist;
wobei der Schritt des Anlegens des Datensignals (V_{DAT}) an die erste Anschlussklemme des zweiten Transistors (74) durch Anlegen des zweiten Steuersignals (ϕ_1) an einen sechsten Transistor (84) ausgeführt wird, der zwischen einer Datensignalleitung (88) und einem dritten Knoten (76) zwischen dem zweiten Transistor (74) und dem fünften Transistor (86) angeschlossen ist, um den sechsten Transistor (84) einzuschalten, während der dritte Transistor (78) eingeschaltet ist, und um den sechsten Transistor (84) auszuschalten, während der dritte Transistor (78) ausgeschaltet ist,
wobei das Verfahren des Weiteren umfasst:

Bereitstellen des fünften und sechsten Transistors (85, 84) in einer solchen Weise, dass sie unterschiedliche Kanaltypen aufweisen.

13. Verfahren nach Anspruch 12, des Weiteren umfassend:

Anlegen des ersten Steuersignals (ϕ_2) an einen siebenten Transistor (98), der in Serie zwischen dem fünften Transistor (86) und der stromgesteuerten Vorrichtung (96) gekoppelt ist, um den siebenten Transistor (98) auszuschalten, während der erste Transistor (60) eingeschaltet ist, wobei der siebente Transistor (98) den entgegen gesetzten Kanaltyp zu dem ersten Transistor (60) hat.

14. Verfahren nach Anspruch 12 oder Anspruch, des Weiteren umfassend:

Anlegen des ersten Steuersignals (ϕ_2) an einen achten Transistor (102), der in Serie zwischen der zweiten Gate-Anschlussklemme und dem ersten Knoten (58) gekoppelt ist, an einen neunten Transistor (104), der zwischen der Energieversorgungsleitung (V_{DD}) und einem vierten Knoten (108) zwischen einer Anschlussklemme des achten Transistors (102) und der zweiten Gate-Anschlussklemme gekoppelt ist, wobei der neunte Transistor (104) von demselben Kanaltyp ist wie der erste Transistor (60) und der achte Transistor (102) vom entgegen gesetzten Kanaltyp zu dem ersten Transistor (60) ist, um den achten Transistor (102) auszuschalten und den neunten Transistor (104) einzuschalten, während der erste Transistor (60) eingeschaltet ist.

15. Verfahren, nach einem der Ansprüche 12 bis 14, des Weiteren umfassend:

Anlegen des ersten Steuersignals (ϕ_2) an einen zehnten Transistor (105), der zwischen dem ersten Knoten (58) und der Anschlussklemme des dritten Transistors (78) angeschlossen ist, die an die zweite Gate-Anschlussklemme angeschlossen ist, und
Anlegen des zweiten Steuersignals (ϕ_1) an einen elften Transistor (107), der zwischen dem ersten Knoten (58) und der anderen Anschlussklemme des dritten Transistors gekoppelt ist, die an eine zweite Anschlussklemme des zweiten Transistors angeschlossen ist, wobei der zehnte Transistor (105) vom entgegen gesetzten Kanaltyp zu dem elften Transistor (107) ist, um den zehnten Transistor (105) auszuschalten, wenn der erste Transistor (60) eingeschaltet ist, und den elften Transistor (107) einzuschalten, wenn der dritte Transistor (78) eingeschaltet ist.

16. Verfahren nach Anspruch 12, wobei die Referenzleitung eine Datensignalleitung (88) ist, wobei der erste Transistor (60) in Serie zwischen dem sechsten Transistor (84) und dem Kondensator (56) angeschlossen ist, wobei das Verfahren umfasst:

nach dem Anlegen des ersten Steuersignals (ϕ_2) zum Einschalten des ersten Transistors (60) und vor dem Anlegen des ersten Steuersignals (ϕ_2) zum Ausschalten des ersten Transistors (60), Anlegen eines Vor-Ladungssignals auf der Datensignalleitung, wobei das Vor-Ladungssignal einen geringeren Wert als das Datensignal (V_{DAT}) hat.

Revendications

1. Circuit de pixel pour exciter un élément commandé

par courant, le circuit de pixel incluant :

un condensateur (56) ;
un élément commandé par courant (96) ;
un premier transistor (60), lequel est connecté en série avec le condensateur (56) et possède une première borne de grille étudiée pour recevoir un premier signal de commande (ϕ_2) ;
un deuxième transistor (74) pour exciter l'élément commandé par courant (96), le deuxième transistor (74) possédant une deuxième borne de grille connectée à un premier noeud (58) entre le premier transistor (60) et le condensateur (56) ;
un troisième transistor (78), lequel est étudié pour connecter en diode le deuxième transistor (74) en réponse à un deuxième signal de commande (ϕ_1) reçu au niveau d'une troisième borne de grille du troisième transistor (78), et qui est par ailleurs étudié pour contrôler une connexion électrique entre un deuxième noeud (72) entre les deuxième et quatrième transistors (74, 68) et le premier noeud (58);
un quatrième transistor (68), lequel est connecté en série avec le deuxième transistor (74) et est connecté entre une ligne d'alimentation (V_{DD}) et le deuxième transistor (74) ;
un cinquième transistor (86), lequel est connecté en série avec l'élément commandé par courant (96) et le deuxième transistor (74), et
un sixième transistor (84), lequel est étudié pour contrôler une connexion électrique entre une ligne de transfert de signaux de données (V_{DAT}) et un troisième noeud (76) entre le deuxième transistor (74) et le cinquième transistor (86), le sixième transistor possédant une sixième borne de grille qui reçoit le deuxième signal de commande (ϕ_1) ;
caractérisé en ce que :

le quatrième transistor (68) possède une quatrième borne de grille, laquelle reçoit le deuxième signal de commande (ϕ_1);
le cinquième transistor (86) possédant une cinquième borne de grille qui reçoit le deuxième signal de commande (ϕ_1), et
le sixième transistor (84) possédant un type de canal différent de celui du cinquième transistor (86).

2. Circuit de pixel selon la revendication 1, le sixième transistor (84) étant de type à canal n.

3. Circuit de pixel selon la revendication 1 ou la revendication 2, comprenant par ailleurs :

un septième transistor (98), lequel est connecté entre le cinquième transistor (86) et l'élément commandé par courant (96).

4. Circuit de pixel selon l'une quelconque des revendications 1 à 3, comprenant par ailleurs :

un huitième transistor (102), lequel est connecté entre le premier noeud (58) et la deuxième borne de grille.

5. Circuit de pixel selon la revendication 4, comprenant par ailleurs :

un neuvième transistor (104), lequel est connecté entre le huitième transistor (102) et la ligne d'alimentation (V_{DD}).

6. Circuit de pixel selon la revendication 5, le neuvième transistor (104) possédant un type de canal différent de celui du huitième transistor (102).

7. Circuit de pixel selon la revendication 5 ou la revendication 6,
la deuxième borne de grille étant connectée à un quatrième noeud (108) entre le huitième transistor (102) et le neuvième transistor (104).

8. Circuit de pixel selon l'une quelconque des revendications précédentes, comprenant par ailleurs :

un dixième transistor (105), lequel est connecté entre le premier noeud (58) et l'un/une parmi une source et un drain du troisième transistor (78), et
un onzième transistor (107), lequel est connecté entre le premier noeud (58) et l'autre parmi la source et le drain du troisième transistor (78).

9. Circuit de pixel selon l'une quelconque des revendications précédentes,
l'élément commandé par courant (96) étant un élément d'émission de lumière.

10. Appareil d'affichage comprenant le circuit de pixel selon l'une quelconque des revendications précédentes.

11. Appareil d'affichage selon la revendication 10, comprenant par ailleurs :

une première ligne de transfert de signaux de commande (SEL,1), une deuxième ligne de transfert de signaux de commande (SEL,2), une troisième ligne de transfert de signaux de commande (SEL,3), et une ligne de transfert de signaux de données (VDAT, 1) dans une matrice, la première ligne de transfert de signaux de commande (SEL,1) fournissant le deuxième signal de commande (ϕ_1) pour un premier circuit de

pixel (50) et la deuxième ligne de transfert de signaux de commande (SEL,2) fournissant le premier signal de commande (ϕ_2) pour le premier circuit de pixel ;
un deuxième signal de commande (ϕ_1) pour un deuxième circuit de pixel étant le premier signal de commande (ϕ_2) pour le premier circuit de pixel fournit par la deuxième ligne de transfert de signaux de commande (SEL,2), et la troisième ligne de transfert de signaux de commande (SEL,3) fournissant un premier signal de commande (ϕ_2) pour le deuxième circuit de pixel.

12. Procédé pour exciter un circuit de pixel, le procédé comprenant :

l'application d'un premier signal de commande (ϕ_2) pour allumer un premier transistor (60) via une première borne de grille dudit premier transistor (60), le premier transistor (60) étant connecté entre une ligne d'alimentation (V_{DD}) et une ligne de référence (64, 88) et en série avec un premier condensateur (56) ;
l'application d'un deuxième signal de commande (ϕ_1) pour allumer un troisième transistor (78) afin de connecter en diode un deuxième transistor (74), le deuxième transistor (74) étant un transistor d'attaque pour un élément commandé par courant (96) et possédant une deuxième borne de grille, laquelle est connectée à un premier noeud (58) entre le premier transistor (60) et le condensateur (56), le deuxième transistor (74) étant connecté en série avec l'élément commandé par courant (96) et possédant une première borne pour recevoir un signal de données (V_{DAT}) ;
l'application du premier signal de commande (ϕ_2) pour éteindre le premier transistor (60) ;
l'application du signal de données (V_{DAT}) à la première borne du deuxième transistor (74);
l'application du deuxième signal de commande (ϕ_1) pour éteindre le troisième transistor (78), et
l'application du deuxième signal de commande (ϕ_1) à un quatrième transistor (68), lequel est connecté en série entre la ligne d'alimentation (VDD) et le deuxième transistor (74), et à un cinquième transistor (86), lequel est connecté en série entre le dispositif commandé par courant (96) et le deuxième transistor (74), afin d'éteindre les quatrième et cinquième transistors (68, 86) alors que le troisième transistor (78) est allumé, et pour allumer les quatrième et cinquième transistors (68, 86) alors que le troisième transistor (78) est éteint, une borne du troisième transistor (78) étant couplée à une borne du deuxième transistor (74) au niveau d'un deuxième noeud (72) entre le deuxième transistor (74) et le quatrième transistor (68) ;
l'étape d'application du signal de données (V_{DAT}) à la première borne du deuxième transistor (74) étant effectuée en appliquant le deuxième signal de commande (ϕ_1) à un sixième transistor (84), lequel est connecté entre une ligne de transfert de signaux de données (88) et un troisième noeud (76) entre le deuxième transistor (74) et le cinquième transistor (86), afin d'allumer le sixième transistor (84) alors que le troisième transistor (78) est allumé et d'éteindre le sixième transistor (84) alors que le troisième transistor (78) est éteint,
le procédé comprenant par ailleurs :

la fourniture des cinquième et sixième transistors (84, 86) de manière à ce qu'ils possèdent des types de canal différents.

13. Procédé selon la revendication 12, comprenant par ailleurs :

l'application du premier signal de commande (ϕ_2) à un septième transistor (98), lequel est couplé en série entre le cinquième transistor (86) et le dispositif commandé par courant (96), afin d'éteindre le septième transistor (98) alors que le premier transistor (60) est allumé, le septième transistor (98) étant d'un type de canal opposé à celui du premier transistor (60).

14. Procédé selon la revendication 12 ou la revendication 13, comprenant par ailleurs :

l'application du premier signal de commande (ϕ_1) à un huitième transistor (102), lequel est couplé en série entre la deuxième borne dé grille et le premier noeud (58), et à un neuvième transistor (104), lequel est couplé entre la ligne d'alimentation (V_{DD}) et un quatrième noeud (108) entre une borne du huitième transistor (102) et la deuxième borne de grille, le neuvième transistor (104) étant de même type de canal que le premier transistor (60) et le huitième transistor (102) étant d'un type de canal opposé à celui du premier transistor (60), afin d'éteindre le huitième transistor (102) et d'allumer le neuvième transistor (104) alors que le premier transistor (60) est allumé.

15. Procédé selon l'une quelconque des revendications 12 à 14, comprenant par ailleurs :

l'application du premier signal de commande (ϕ_2) à un dixième transistor (105), lequel est connecté entre le premier noeud (58) et la borne du troisième transistor (78) lequel est connecté à la deuxième borne de grille, et
l'application du deuxième signal de commande

(ϕ_1) à un onzième transistor (107), lequel est couplé entre le premier noeud (58) et l'autre borne du troisième transistor, lequel est connecté à une deuxième borne du deuxième transistor, le dixième transistor (105) étant d'un type de canal opposé à celui du onzième transistor (107), afin d'éteindre le dixième transistor (105) lorsque le premier transistor (60) est allumé et d'allumer le onzième transistor (107) lorsque le troisième transistor (78) est allumé.

16. Procédé selon la revendication 12, la ligne de référence étant une ligne de transfert de signaux de données (88), le premier transistor (60) étant connecté en série entre le sixième transistor (84) et le condensateur (56), le procédé comprenant :

après application du premier signal de commande (ϕ_2) afin d'allumer le premier transistor (60) et avant d'appliquer le premier signal de commande (ϕ_2) pour éteindre le premier transistor (60), l'application d'un signal de précharge à la ligne de transfert de signaux de données, le signal de précharge ayant une valeur inférieure à celle du signal de données (V_{DAT}).

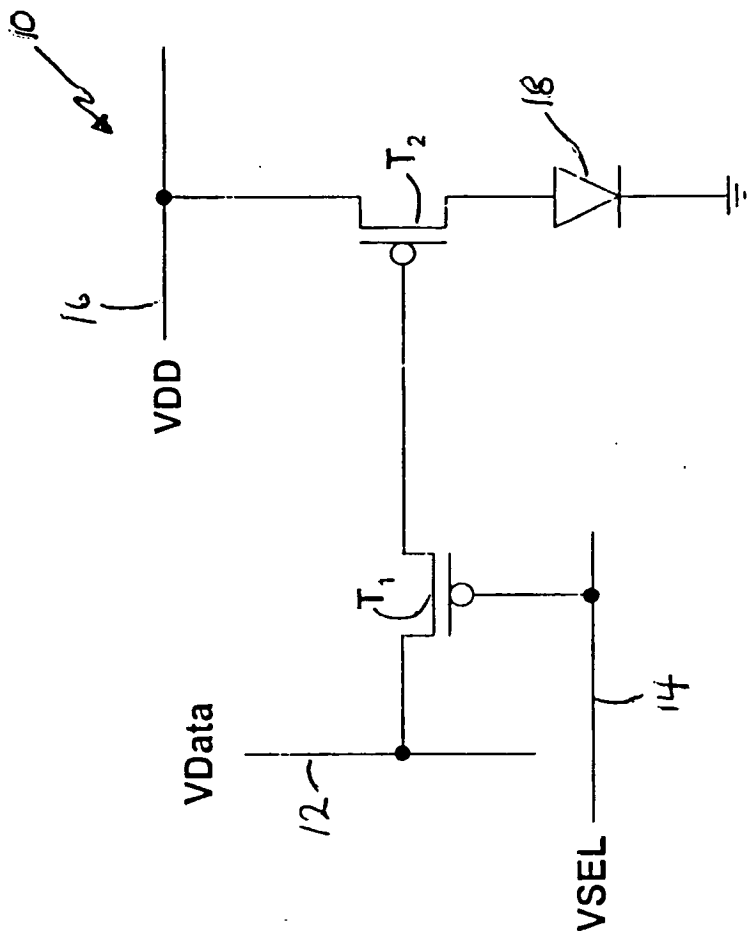
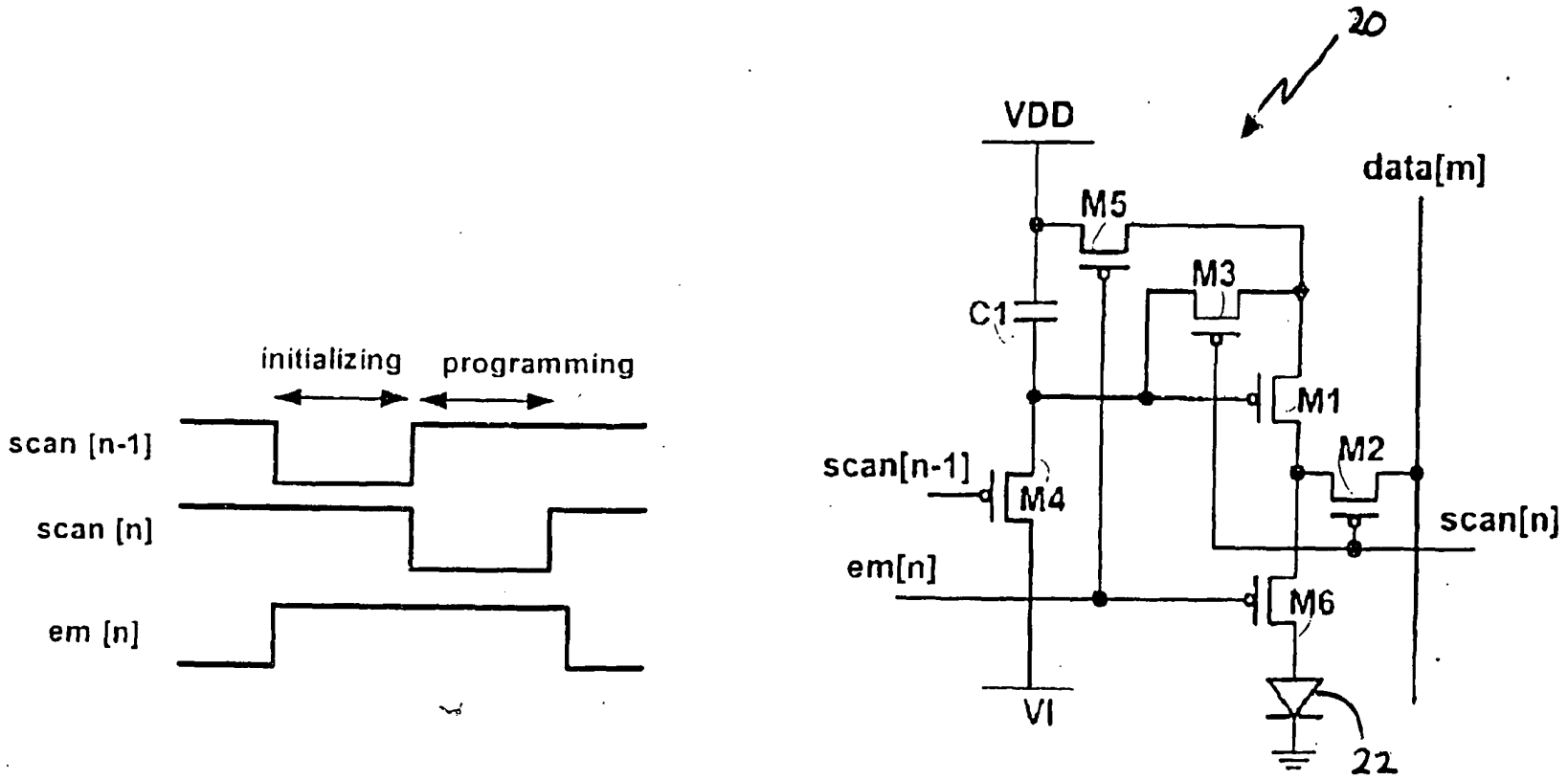


Figure 1: Prior Art



"A self-compensated voltage programming pixel structure for active-matrix organic light emitting diodes," by S.M. Choi, et.al., International Display Workshop 2003, Pp.535-538 (2003)..

Figure 2: Prior Art

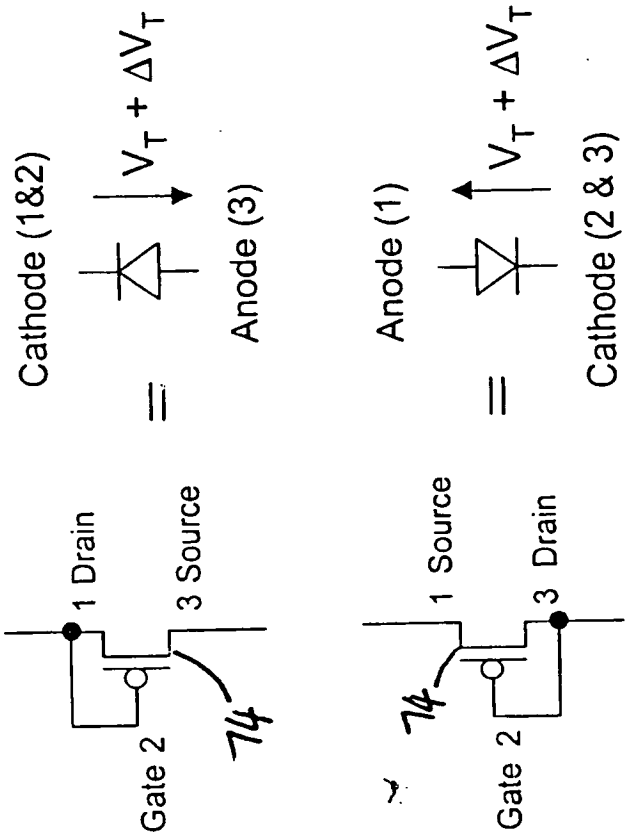

Cathode (1&2)
$V_T + \Delta V_T$
Anode (3)
1 Drain
3 Source
Gate 2
74
Anode (1)
$V_T + \Delta V_T$
Cathode (2 & 3)
1 Source
3 Drain
Gate 2
74

Figure 3

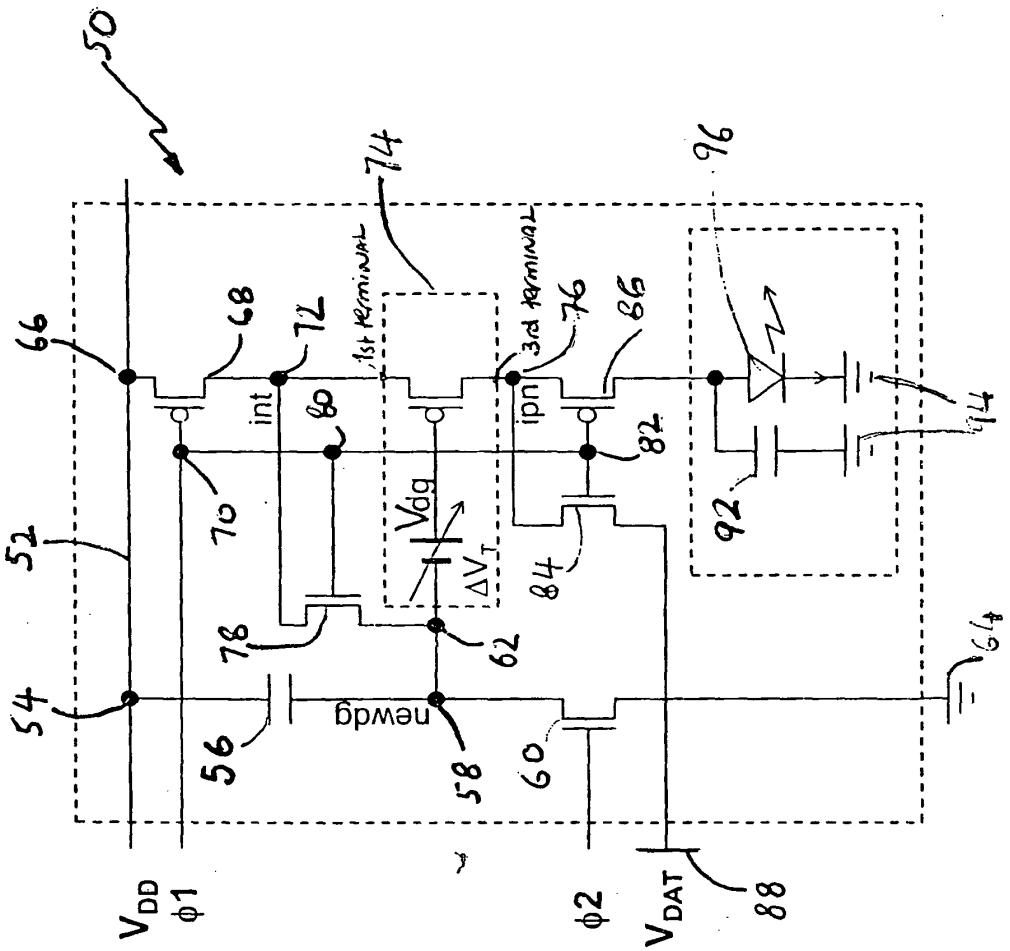

50
66
68
72
74
1st terminal
76
3rd terminal
86
96
int
80
ipn
82
52
70
Vdg
ΔVT
84
94
92
78
62
54
56
newdg
58
60
64
VDD
ϕ1
ϕ2
VDAT
88

Figure 4

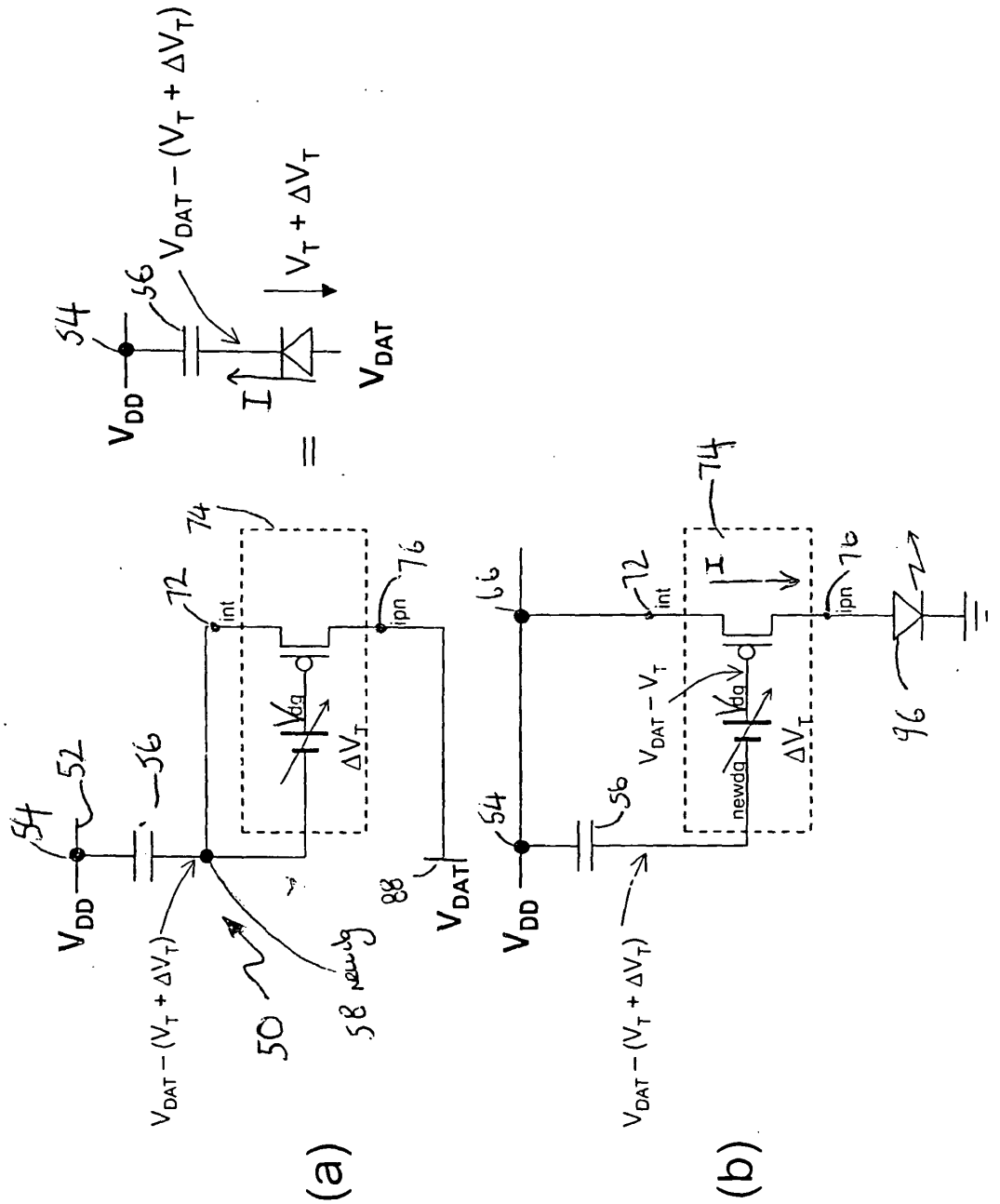

V_{DD}
54
56
$V_{DAT} - (V_T + \Delta V_T)$
$V_T + \Delta V_T$
I
V_{DAT}
=
74
72
int
ipn
76
52
V_{dg}
ΔV_T
50
58
newdg
88
V_{DAT}
(a)
66
$V_{DAT} - V_T$
newdg
96
(b)

Figure 5

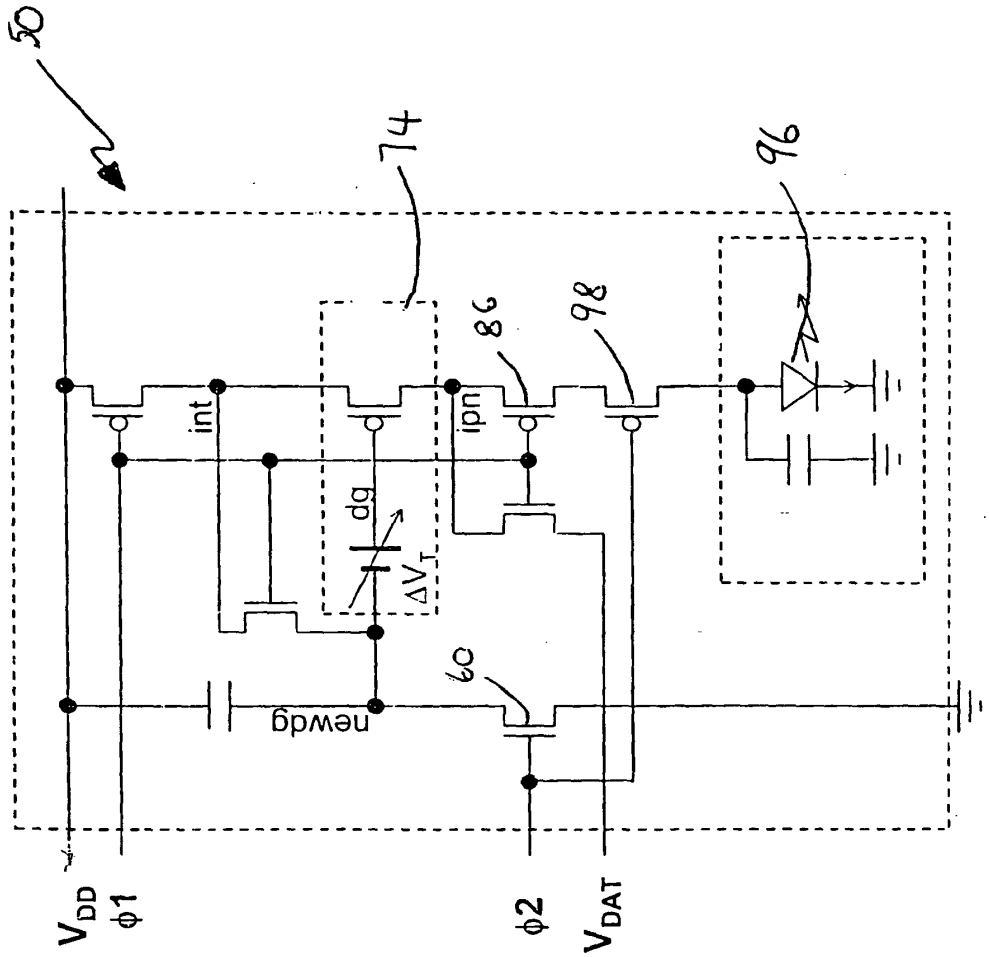


Figure 6

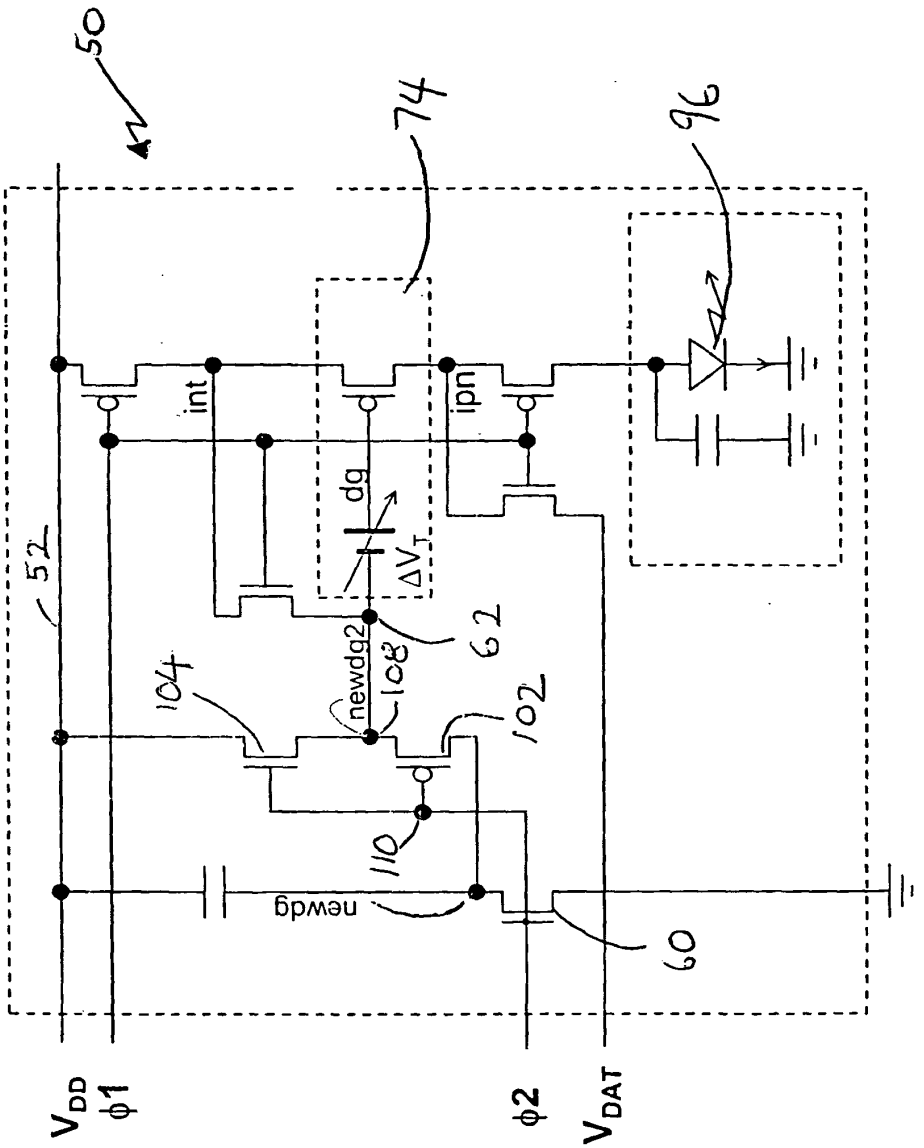

50
74
96
52
int
ipn
dg
ΔV_T
newdg2
62
104
108
102
110
newdg
60
V_{DD}
$\phi 1$
$\phi 2$
V_{DAT}

Figure 7

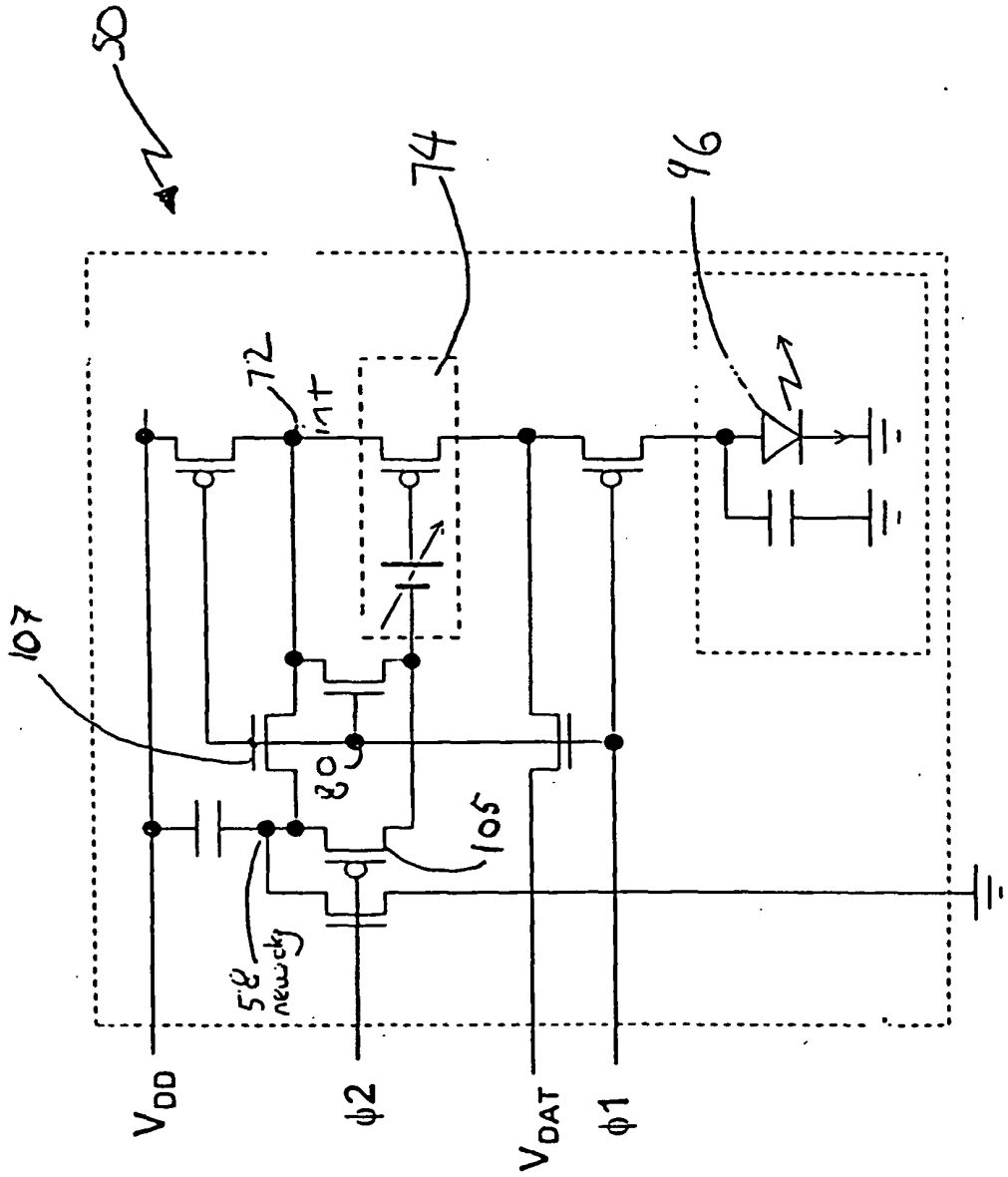


Figure 8

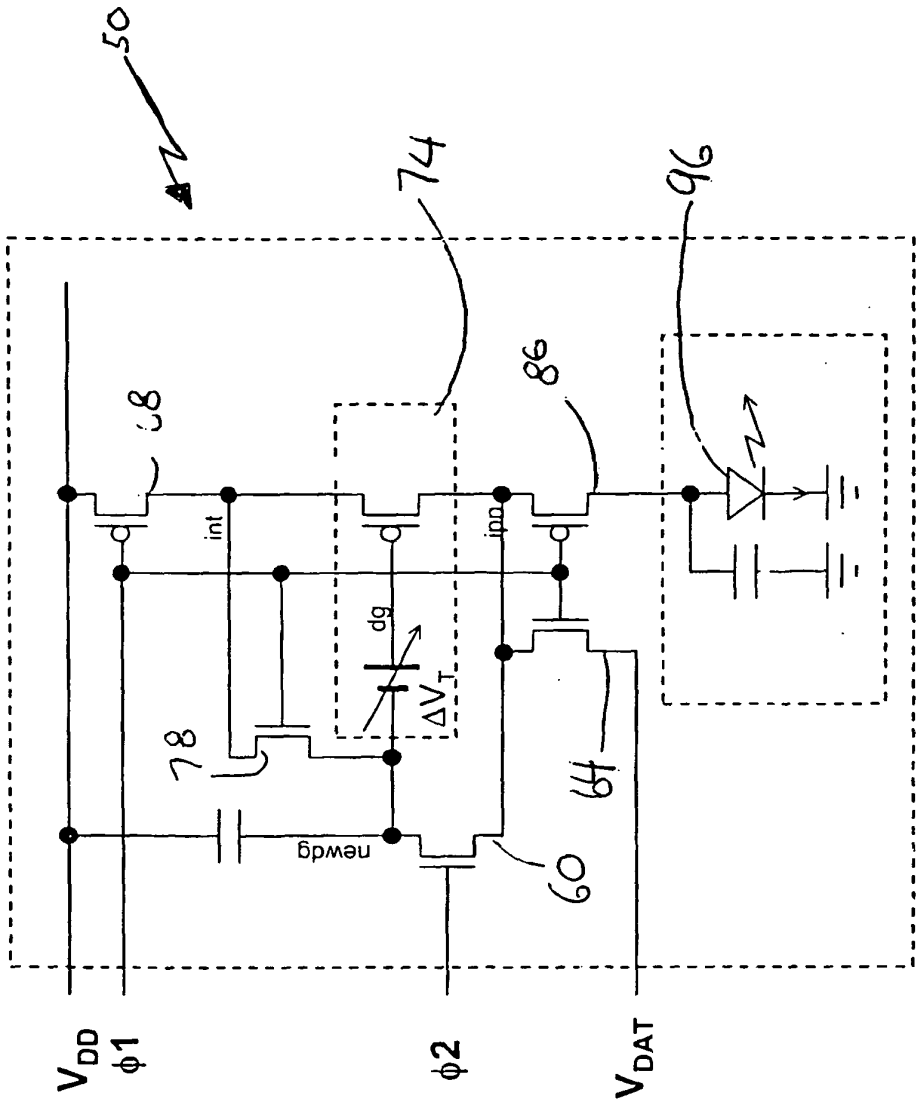


Figure 9

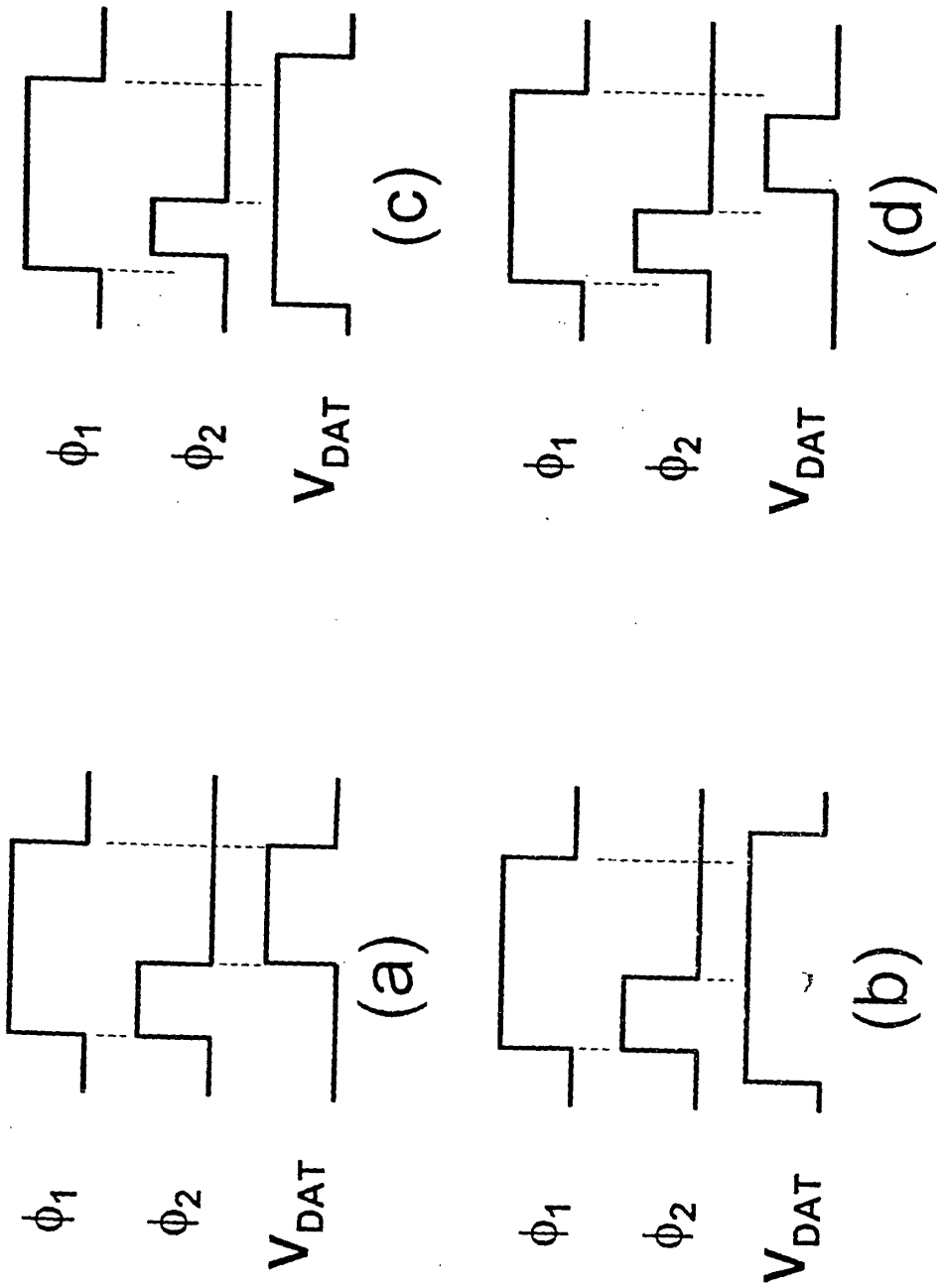

(c)
ϕ_1
ϕ_2
V_{DAT}
(d)
ϕ_1
ϕ_2
V_{DAT}
(a)
ϕ_1
ϕ_2
V_{DAT}
(b)
ϕ_1
ϕ_2
V_{DAT}

Figure 10

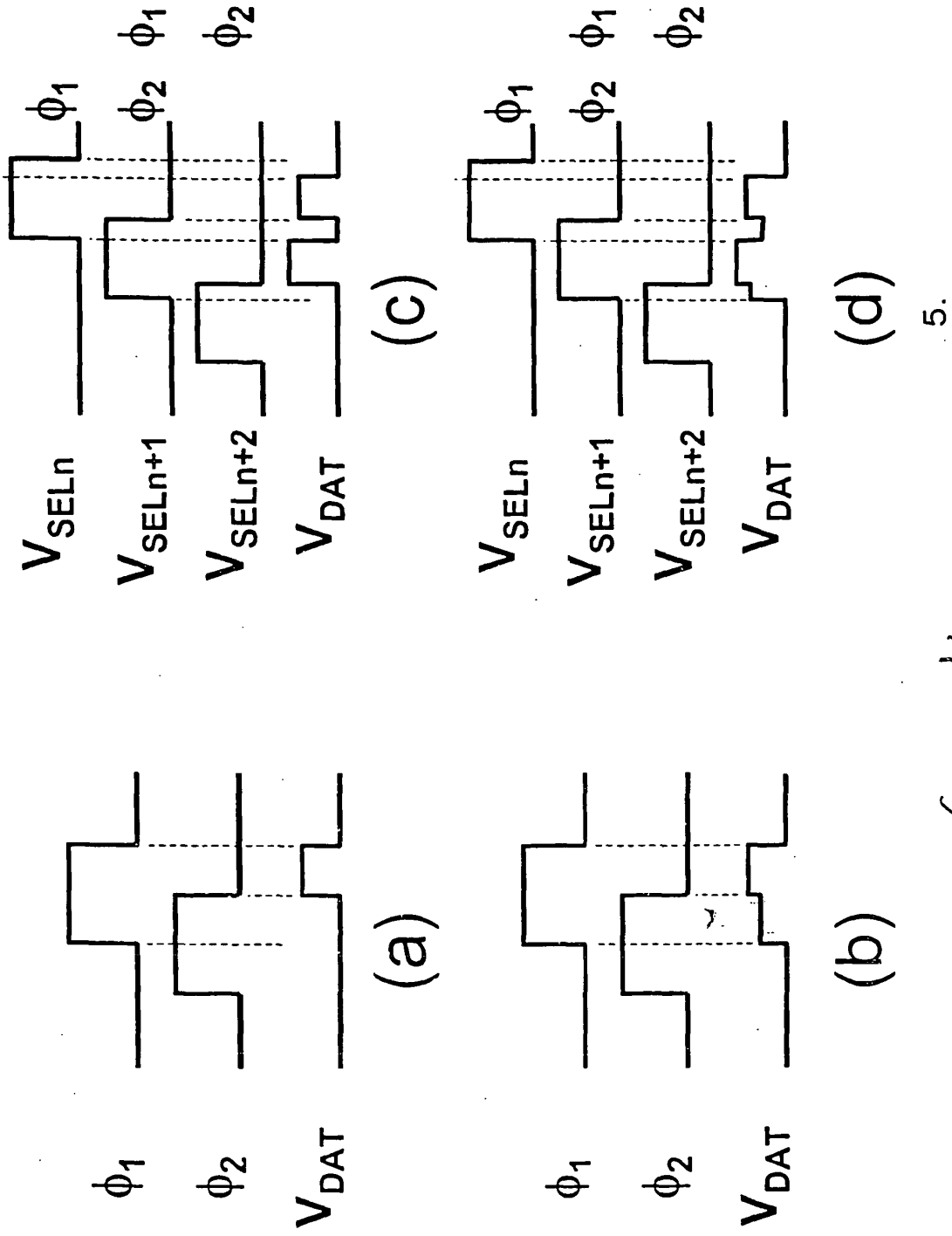

ϕ_1
ϕ_2
V_{DAT}
(a)
ϕ_1
ϕ_2
V_{DAT}
(b)
V_{SELn}
V_{SELn+1}
V_{SELn+2}
V_{DAT}
ϕ_1
ϕ_2
ϕ_1
ϕ_2
(c)
V_{SELn}
V_{SELn+1}
V_{SELn+2}
V_{DAT}
ϕ_1
ϕ_2
ϕ_1
ϕ_2
(d)

Figure 11

5.

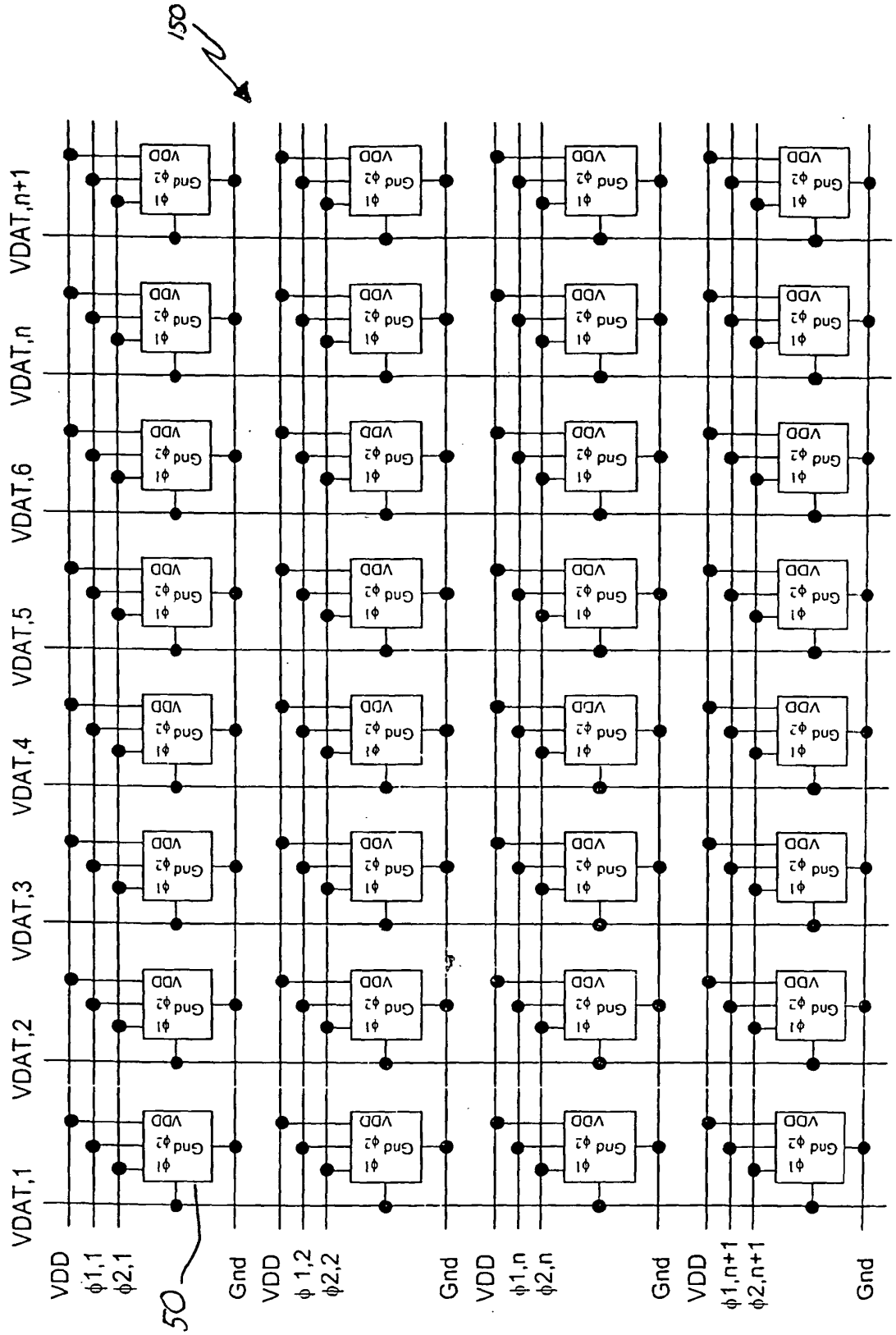

150
VDAT,1
VDAT,2
VDAT,3
VDAT,4
VDAT,5
VDAT,6
VDAT,n
VDAT,n+1
VDD
ϕ1,1
ϕ2,1
50
Gnd
VDD
ϕ 1,2
ϕ2,2
Gnd
VDD
ϕ1,n
ϕ2,n
Gnd
VDD
ϕ1,n+1
ϕ2,n+1
Gnd
ϕ1
Gnd ϕ2
VDD

Figure 12

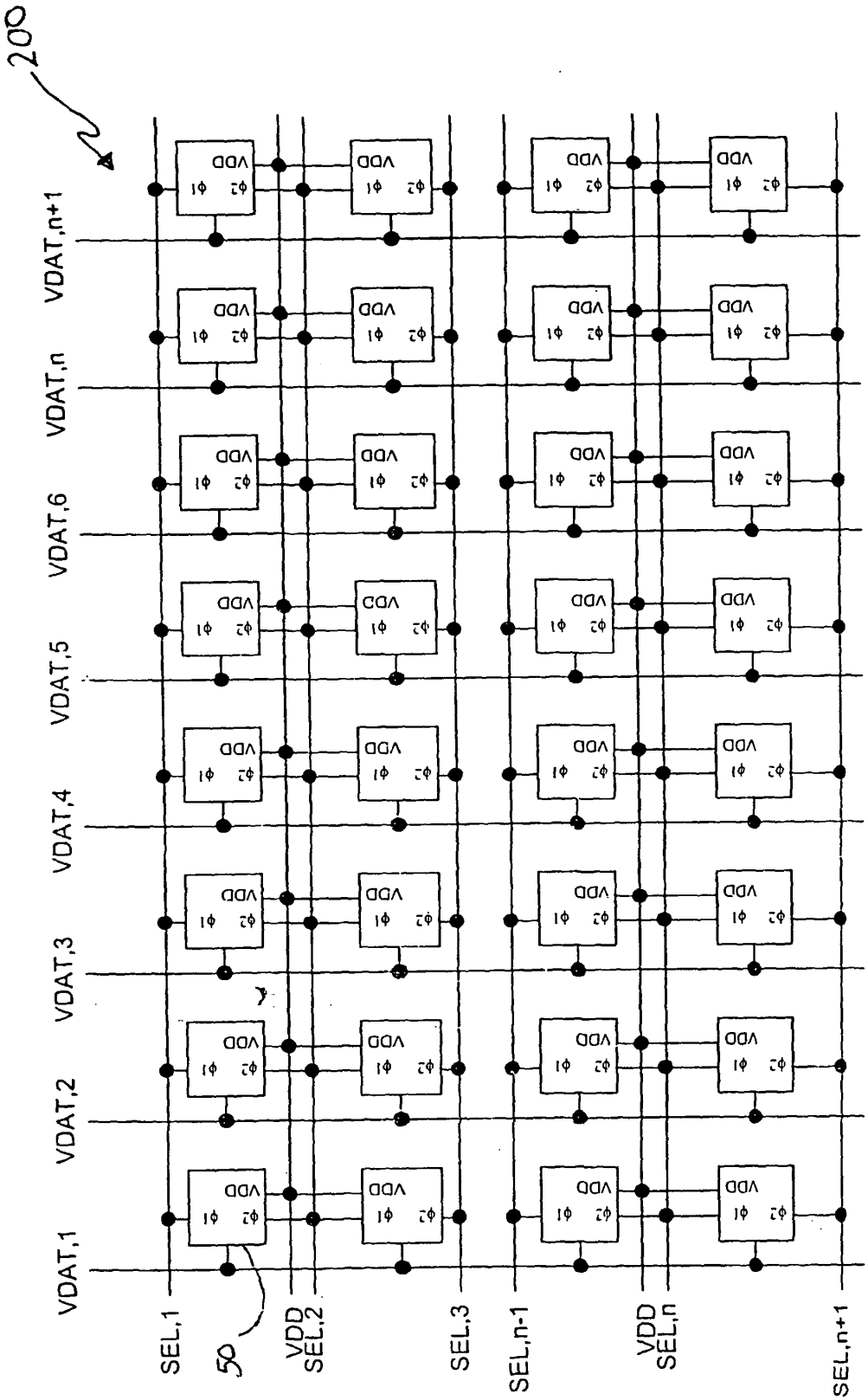

200
VDAT,1
VDAT,2
VDAT,3
VDAT,4
VDAT,5
VDAT,6
VDAT,n
VDAT,n+1
SEL,1
50
VDD
SEL,2
SEL,3
SEL,n-1
VDD
SEL,n
SEL,n+1
VDD
φ1
φ2

Figure 13

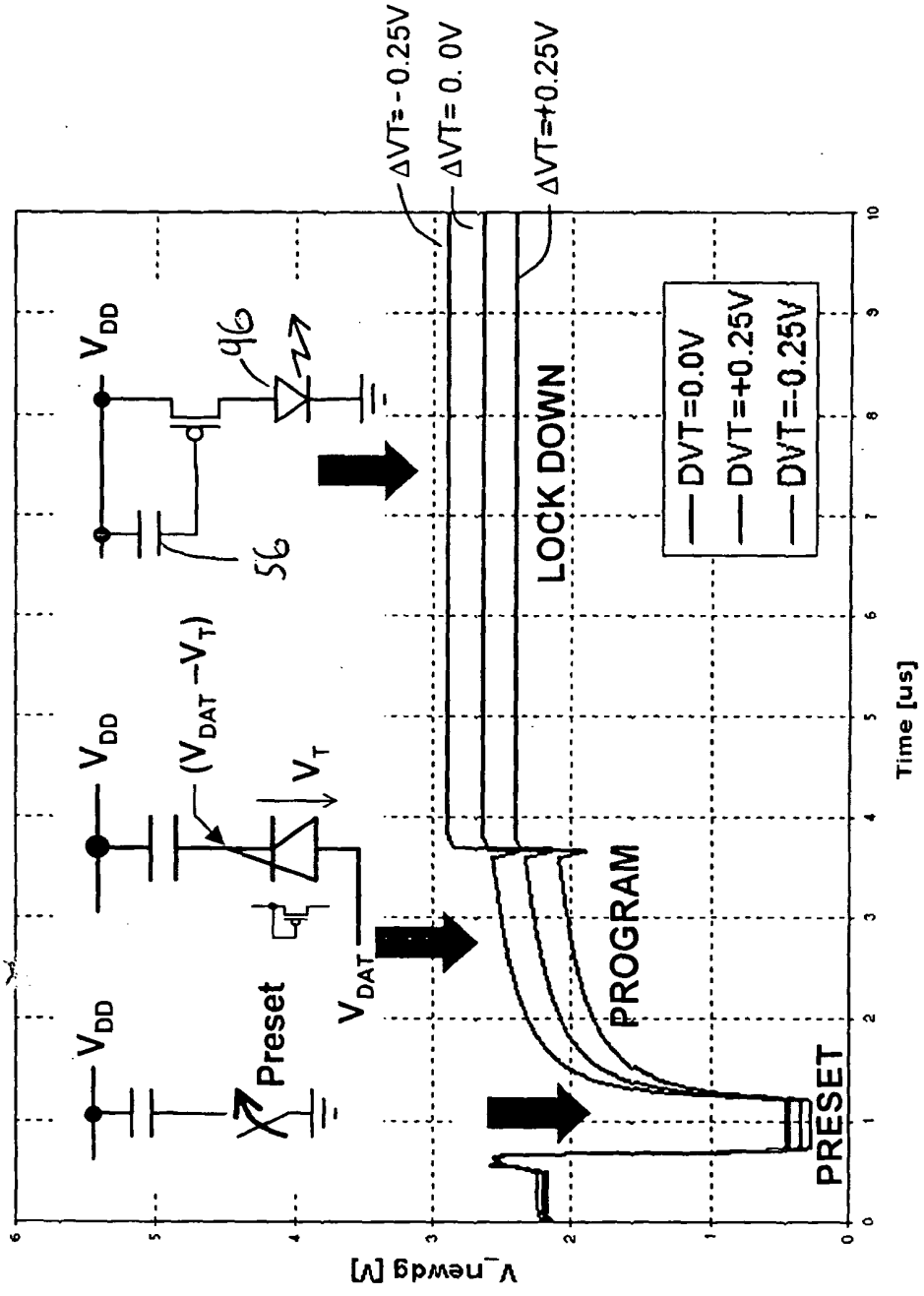

ΔVT= - 0.25V
ΔVT= 0. 0V
ΔVT=+0.25V
V_newg [V]
Time [us]
LOCK DOWN
PROGRAM
PRESET
DVT=0.0V
DVT=+0.25V
DVT=-0.25V
V_DD
Preset
V_DAT
V_T
(V_DAT -V_T)
96
56

Figure 14

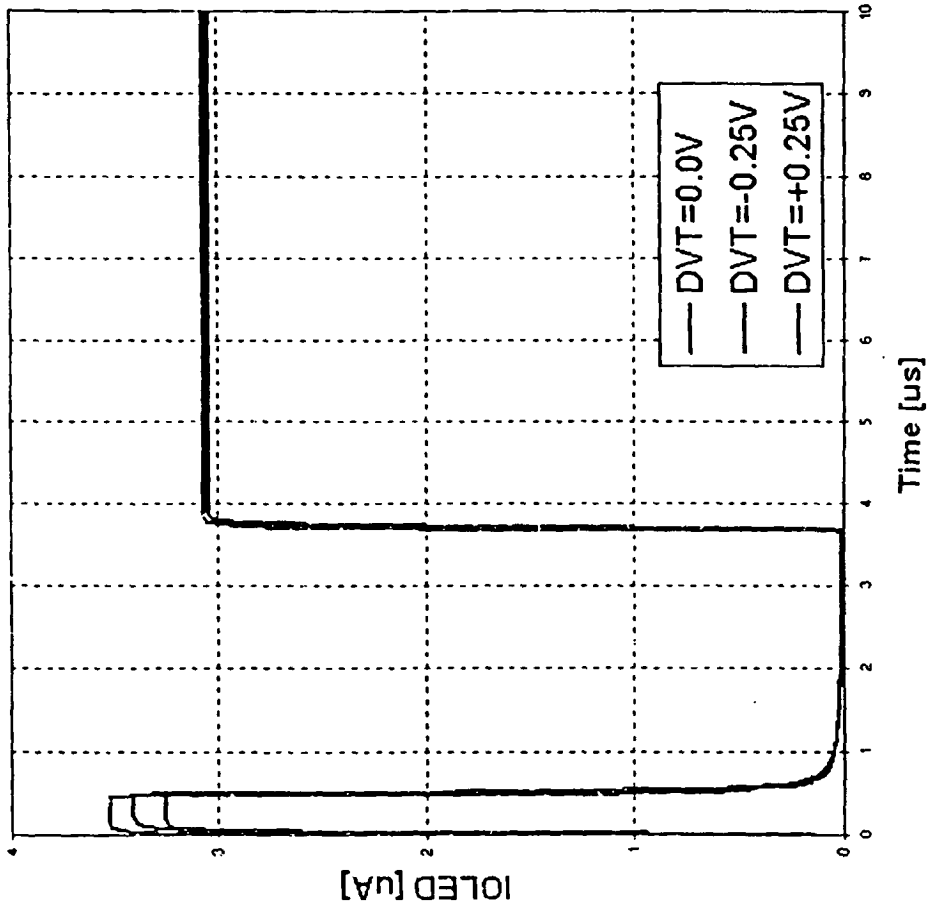


Figure 15

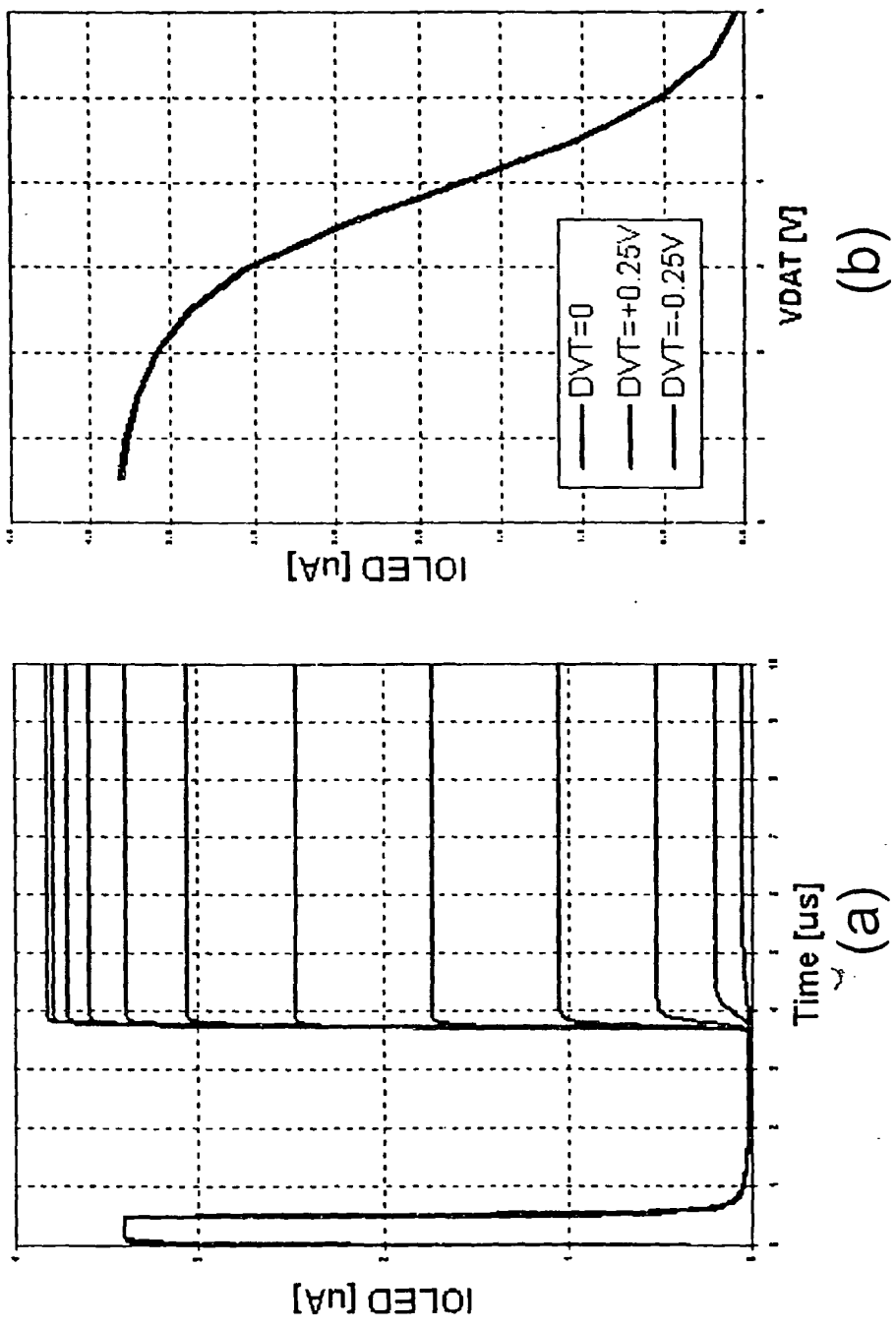


Figure 16

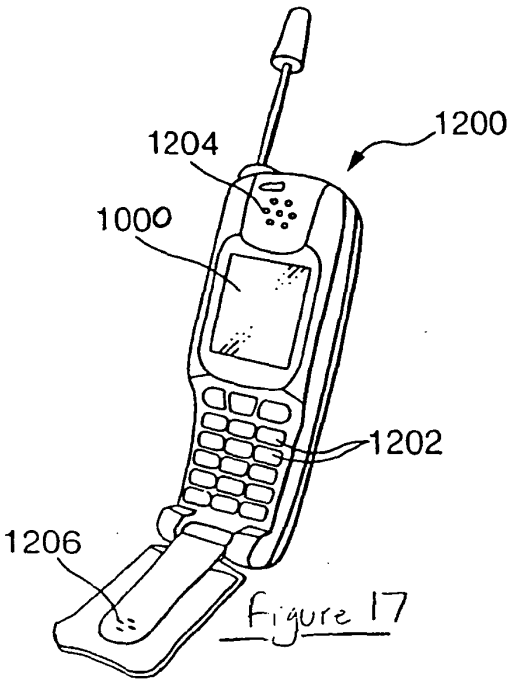


Figure 17

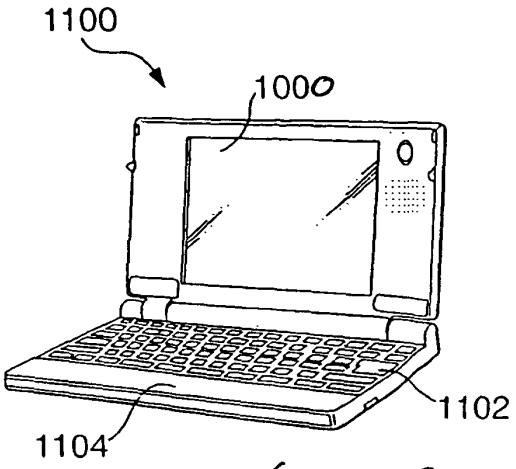


Figure 18

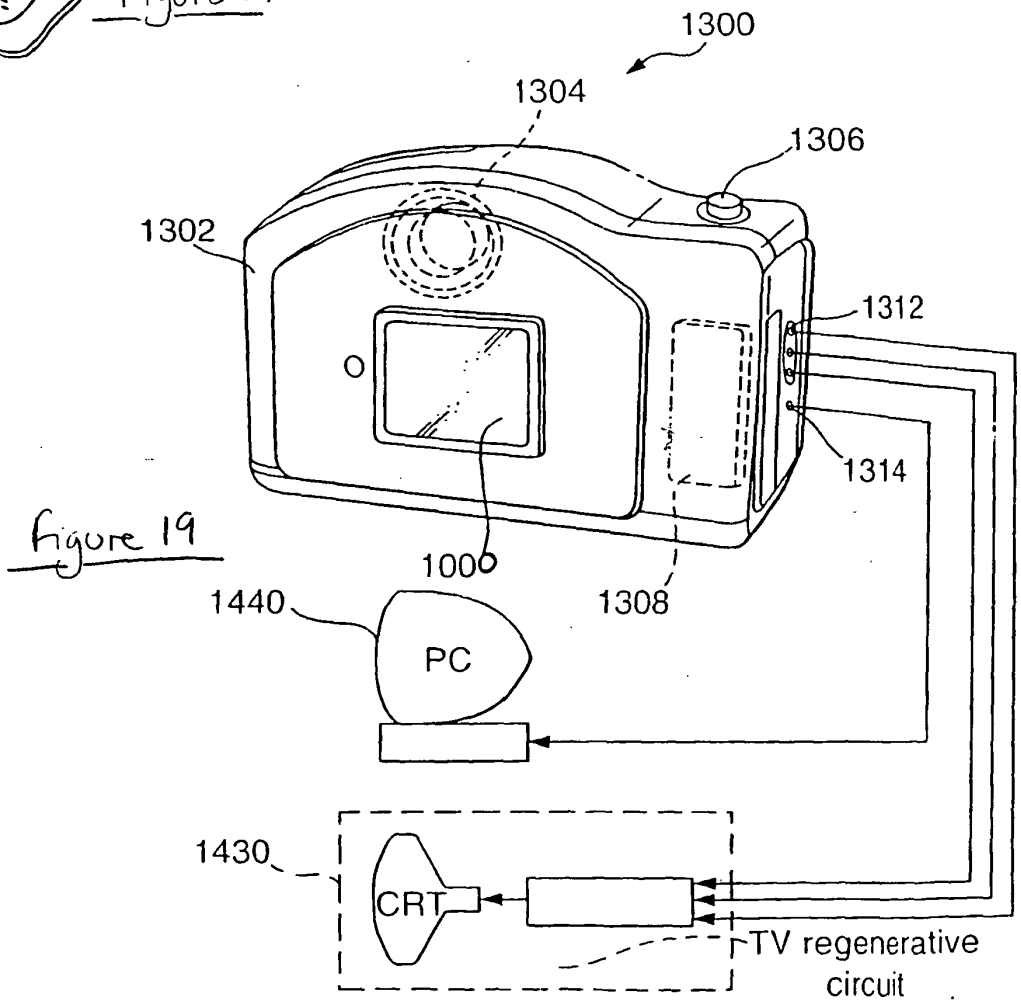


Figure 19

REFERENCES CITED IN THE DESCRIPTION

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Non-patent literature cited in the description

- **S. M. CHOI et al.** A self-compensated voltage programming pixel structure for active-matrix organic light emitting diodes. *International Display Workshop,* 2003, 535-538 **[0004]**
- **A. YUMOTO et al.** Pixel-Driving Methods for Large-Sized Poly-Si AM-OLED Displays. *Asia Display,* 1395-1398 **[0010]**

专利名称(译)	像素电路		
公开(公告)号	EP1580722B1	公开(公告)日	2008-04-30
申请号	EP2005250947	申请日	2005-02-18
[标]申请(专利权)人(译)	精工爱普生株式会社		
申请(专利权)人(译)	SEIKO EPSON CORPORATION		
当前申请(专利权)人(译)	SEIKO EPSON CORPORATION		
[标]发明人	TAM SIMON C O CAMBRIDGE RES LAB OF EPSON		
发明人	TAM, SIMON, C/O CAMBRIDGE RESEARCH LAB. OF EPSON		
IPC分类号	G09G3/32 H01L51/50 G09G3/20 G09G3/30		
CPC分类号	G09G3/3233 G09G2300/0426 G09G2300/0819 G09G2300/0842 G09G2310/0262 G09G2320/0233 G09G2320/0252 G09G2320/043		
优先权	2004004919 2004-03-04 GB		
其他公开文献	EP1580722A3 EP1580722A2		
外部链接	Espacenet		

摘要(译)

已知补偿驱动诸如电流驱动有机发光器件的发光器件的像素电路中的驱动晶体管的阈值电压变化。然而，这种像素电路的编程和初始化可能较慢并且需要多个控制或信号线。本发明提供一种像素电路，包括用于二极管连接驱动晶体管的n沟道晶体管和用于减少信号线和控制线数量的装置。

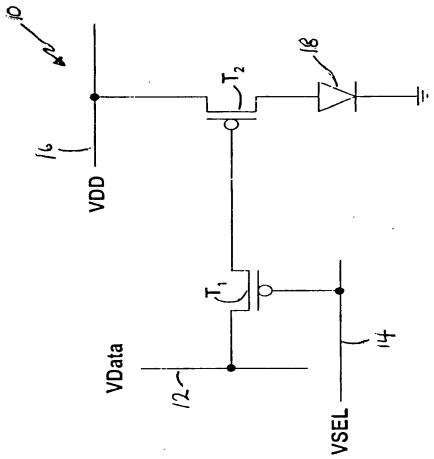

Figure 1: Prior Art