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(54) SCANNING DRIVE CIRCUIT AND ORGANIC LIGHT-EMITTING DISPLAY

ABTASTUNGSANSTEUERUNGSSCHALTUNG UND ORGANISCHE LICHTEMITTIERENDE ANZEIGE

CIRCUIT D'ENTRAÎNEMENT DE BALAYAGE ET DISPOSITIF D'AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE

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(56) References cited:
EP-A2- 1 763 003
EP-A2- 1 965 371
CN-A- 101 256 736
CN-A- 102 857 207
CN-A- 103 021 358
CN-A- 104 183 219
US-A1- 2012 139 962
US-A1- 2012 139 962
US-A1- 2012 212 517
US-B2- 8 368 675

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Description

FIELD

[0001] The present disclosure relates to the field of scanning drive circuit, and particularly to a scanning drive circuit for scanning driving an organic light emitting device pixel circuit, and an organic light-emitting display.

BACKGROUND

[0002] An organic light-emitting display is a display that is equipped with Organic Light-emitting Diodes (OLED) as its light-emitting device. Compared to the current mainstream flat-panel display technology of Thin Film Transistor Liquid Crystal Display (TFT-LCD), the organic light-emitting displays have the advantages of high contrast, wide angle of view, low power consumption and thinner volume, etc. As one of the technologies that draw the most attention, it is expected to become the next generation of flat display technology after LCD.

[0003] A traditional organic light-emitting display includes a data driver for supplying data signals to a data bus, a first scan driver for sequentially supplying scanning signals to one scan line, a second scan driver for sequentially supplying scanning signals to another scan line, a timing controller for supplying timing signals and high and low level (Here "level" refers to "electrical level", the same below.) signals to the first scan driver and the second scan driver, and a multiple-pixel display unit. The function of the first scan driver and the second scan driver is to sequentially generate driver signals to be supplied to a display panel, and control the brightness of the pixels of the display panel. One example of organic light emitting display and driving circuit is described in European Patent Publication No. EP1965371A2, and other scanning drive circuits known in the art, relating to organic light-emitting displays, are also known from the European Patent Publication No. EP1763003A2, U.S. Patent Publication No.US2012/0139962A1 and U.S. Patent Publication No. US2012/0212517A1.

SUMMARY

[0004] Based on the above, the invention provides an alternative scanning drive circuit controlled by two clock signals where a stage comprises nine transistors. Further, an organic light-emitting display is also provided.

[0005] According to an aspect of the disclosure, a scanning drive circuit includes a first scan driver for sequentially outputting selection signals and a second scan driver for sequentially outputting transmission signals, the first scan driver including a plurality of first cascade structures and the second scan driver including a plurality of second cascade structures, each cascade structure of the first cascade structures and/or the second cascade structures including: a scanning signal input terminal; a scanning signal output terminal; a first transistor including an input terminal connected to the scanning signal input terminal of the cascade structure or to a scanning signal output terminal of a precedent cascade structure, a gate terminal connected to a first clock end, and an output terminal; a second transistor including a gate terminal connected to the output terminal of the first transistor, an input terminal connected to a second clock end, and an output terminal connected to the scanning signal output terminal; a third transistor including an input terminal connected to a first level end, a gate terminal connected to the scanning signal output terminal, and an output terminal; a fourth transistor including an input terminal connected to the output terminal of the third transistor, a gate terminal connected to the first clock end, and an output terminal connected to a second level end; a fifth transistor including an input terminal connected to the first level end, a gate terminal connected to the output terminal of the third transistor, and an output terminal connected to the scanning signal output terminal; a sixth transistor including an input terminal connected to the first level end, a gate terminal connected to the scanning signal output terminal, and an output terminal; a seventh transistor including an input terminal connected to the output terminal of the sixth transistor, a gate terminal connected to the first clock end, and an output terminal connected to the second level end; an eighth transistor including an input terminal connected to the first level end, a gate terminal connected to the scanning signal output terminal, and an output terminal connected to a driving signal output terminal; a ninth transistor including an input terminal connected to the driving signal output terminal, a gate terminal connected to the output terminal of the sixth transistor, and an output terminal connected to a third level end; and a first capacitor connected between the gate terminal and the output terminal of the second transistor.

[0006] In one embodiment, a timing controller is arranged to supply signals to the first clock end and the second clock end of each cascade structure of the first cascade structures and the second cascade structures such that the signals received are the same in frequency. The signal received by the second clock end is at low level when the signal received by the first clock end is at high level, and the signal received by the second clock end is at high level when the signal received by the first clock end is at low level.

[0007] In one embodiment, the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, the seventh transistor, the eighth transistor and the ninth transistor are Thin Film Field Effect Transistors.

[0008] In one embodiment, a second capacitor is connected between the first level end and the gate terminal of the sixth transistor.

[0009] In one embodiment, a third capacitor is connected between the second level end and the gate terminal of the ninth transistor.

[0010] In one embodiment, a third capacitor is connected between the driving signal output terminal and the

gate terminal of the ninth transistor.

[0011] In one embodiment, the third level end and the second level end are the same level end.

[0012] In one embodiment, the voltage value inputted from the third level end is smaller than the voltage value inputted from the second level end.

[0013] In one embodiment, the voltage inputted from the first level end is high level, and the voltages inputted from the second and the third level ends are high level.

[0014] Only two clock signals and nine transistors are used in the above scan drive circuit, less than the traditional scan drive circuits. This can greatly enhance the reliability of the circuit, and reduce costs of design and manufacture.

[0015] According to an aspect of the disclosure, an organic light-emitting display includes a pixel circuit, a data driver and a timing controller, and further includes the above scanning drive circuit, the timing controller supplying timing signals and high and low level signals to the first clock end, the second clock end, the scanning signal input terminal, the first level end, the second level end and the third level end of the scanning drive circuit, the driving signal output terminal of the scanning drive circuit being connected to the driving signal input terminal of the pixel circuit to output driving signals for driving the pixel circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016]

Fig. 1 is a module schematic diagram of a first scan driver of a scanning drive circuit according to Example 1 of the disclosure.

Fig. 2 is a circuit diagram of a cascade structure of the first scan driver of Fig. 1.

Fig.3 is a timing diagram of a portion of the signals of the first scan driver of Fig. 1.

Fig. 4 is a circuit diagram of a cascade structure of a first scan driver of a scanning drive circuit according to Example 2 of the disclosure.

Fig. 5 is a circuit diagram of a cascade structure of a first scan driver of a scanning drive circuit according to Example 3 of the disclosure.

Fig. 6 is schematic diagram of the circuit module of an organic light-emitting display of according to an embodiment of the disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] The embodiments of the disclosure will now be described in detail with reference to the accompany drawings. To facilitate understanding, the terminal numerals are used in the description to represent corresponding signals.

Example 1

[0018] Referring to Fig. 1 and Fig. 2, a scanning drive circuit is provided in this embodiment. The scanning drive circuit includes a first scan driver for sequentially outputting selection signals and a second scan driver for sequentially outputting transmission signals. The first scan driver includes a plurality of first cascade structures and the second scan driver includes a plurality of second cascade structures. Each cascade structure of the first cascade structures and/or the second cascade structures may have the following structure. In this embodiment, each cascade structure of the first cascade structures and the second cascade structures includes a first transistor M1, a second transistor M2, a third transistor M3, a fourth transistor M4, a fifth transistor M5, a sixth transistor M6, a seventh transistor M7, an eighth transistor M8, a ninth transistor M9, a first capacitor C1, a second capacitor C2, a third capacitor C3, a scanning signal input terminal IN, a scanning signal output terminal OUT, a first clock end CKL1, a second clock end CLK2, a first level end VGH, a second level end VGL1, a third level end VGL2 and a driving signal output terminal EM.

[0019] The first transistor M1 includes an input terminal connected to the scanning signal input terminal IN or to the scanning signal output terminal OUT of a precedent cascade structure, a gate terminal connected to the first clock end CKL1, and an output terminal. The second transistor M2 includes a gate terminal connected to the output terminal of the first transistor M1, an input terminal connected to the second clock end CKL2, and an output terminal connected to the scanning signal output terminal OUT. The third transistor M3 includes an input terminal connected to the first level end VGH, a gate terminal connected to the scanning signal output terminal OUT, and an output terminal. The fourth transistor M4 includes an input terminal connected to the output terminal of the third transistor M3, a gate terminal connected to the first clock end CKL1, and an output terminal connected to the second level end VGL1. The fifth transistor M5 includes an input terminal connected to the first level end VGH, a gate terminal connected to the output terminal of the third transistor M3, and an output terminal connected to the scanning signal output terminal OUT. The sixth transistor M6 includes an input terminal connected to the first level end VGH, a gate terminal connected to the scanning signal output terminal OUT, and an output terminal. The seventh transistor M7 includes an input terminal connected to the output terminal of the sixth transistor M6, a gate terminal connected to the first clock end CKL1, and an output terminal connected to the second level end VGL1. The eighth transistor M8 includes an input terminal connected to the first level end VGH, a gate terminal connected to the scanning signal output terminal OUT, and an output terminal connected to a driving signal output terminal EM. The ninth transistor M9 includes an input terminal connected to the driving signal output terminal EM, a gate terminal connected to the output terminal of

the sixth transistor M6, and an output terminal connected to the third level end VGL2.

[0020] The gate electrode of the first transistor M1, the gate electrode of the fourth transistor M4 and the gate electrode of the seventh transistor M7 are shorted, a second electrode of the first transistor M1, the gate electrode of the second transistor M2 and the first side of the first capacitor C1 are shorted, the second electrode of the second transistor M2, the gate electrode of the third transistor M3, the second electrode of the fifth transistor M5, the gate electrode of the sixth transistor M6, the gate electrode of the eighth transistor M8, the first side of the first capacitor C1 and the second side of the second capacitor C2 are shorted, the first electrode of the third transistor M3, the first electrode of the fifth transistor M5, the first electrode of the sixth transistor M6, the first electrode of the eighth transistor M8 and the first side of the second capacitor C2 are shorted, the second electrode of the third transistor M3, the first electrode of the fourth transistor M4 and the gate electrode of the fifth transistor M5 are shorted, the second electrode of the fourth transistor M4, the second electrode of the seventh transistor M7 and the second side of the third capacitor C3 are shorted, the second electrode of the sixth transistor M4, the first electrode of the seventh transistor M7, the first side of the third transistor M3 and the gate electrode of the ninth transistor M9 are shorted, the second electrode of the eighth transistor M8 and the first electrode of the ninth transistor M9 are shorted.

[0021] The first electrode of the first transistor M1 is connected to the scanning signal input terminal IN, the second electrode of the second transistor M2 is connected to the scanning signal output terminal OUT, the gate electrode of the first transistor M1 is connected to the clock end CLK1, the first electrode of the second transistor M2 is connected to the second clock end CLK2, the first electrode of the third transistor M3 is connected to the first level end VGH, the second electrode of the fourth transistor M4 is connected to the second level end VGL1, the second electrode of the ninth transistor M9 is connected to the second low level signal input terminal VGL2, and the second electrode of the eighth transistor M8 is connected to the scanning signal output terminal EM.

[0022] High level signals are inputted from the first level end VGH (which means the input voltage of the first level end VGH is positive), the first clock signal is inputted from the first clock end CLK1, the second clock signal is inputted from the second clock end CLK2, the scanning signal is inputted from the scanning signal input terminal IN, the first low level signal is inputted from the second level end VGL1 (which means that the input voltage of the second level end VGL1 is negative), the second low level signal is inputted from the second low level signal input terminal VGL2 (which means that the input voltage of the second level signal input terminal VGL2 is negative), the driving signal is outputted from the driving signal output terminal EM, and the output scanning signal is outputted from the scanning signal output terminal OUT.

[0023] The first transistor M1, the second transistor M2, the third transistor M3, the fourth transistor M4, the fifth transistor M5, the sixth transistor M6, the seventh transistor M7, the eighth transistor M8 and the ninth transistor M9 are Field Effect Transistors, preferably are P-channel type Field Effect Transistors. More specifically, they are Thin Film Field Effect Transistors (TFT), and preferably are P-channel type Thin Film Field Effect Transistors.

[0024] Since each of the cascade structures of the first scan driver and the second scan driver of the scanning drive circuit includes nine transistors and requires only two clock signals, it is possible to reduce the number of transistors used by the scanning drive circuit. Therefore, this greatly enhances the reliability of the product, and reduces the costs of design and manufacture. In addition, the presence of the sixth transistor M6, the seventh transistor M7, the eighth transistor M8 and the ninth transistor M9 enables more a precise and reliable output terminal of the driving signal output terminal EM of the scanning drive circuit.

[0025] It should be noted that the second capacitor C2 and the third capacitor C3 can also be omitted when there is a load capacitance connected to the scanning signal output terminal OUT. In this embodiment, the second capacitor C2 and the third capacitor C3 are provided to reduce the current of the first level end VGH, the second level end VGL1 and the third level end VGL2.

[0026] The connection relationship of the plurality of cascade structures will now be described taken the first scan driver as an example.

[0027] The first scan driver includes N levels of cascade structures. The scanning signal output terminal of the first level cascade structure is connected to the scanning signal input terminal of the second level cascade structure, and the scanning signal output terminal of the second level cascade structure is connected to the scanning signal input terminal of the third level cascade structure, and so on. The scanning signal output terminal of the N-1 level cascade structure is connected to the scanning signal input terminal of the N level cascade structure.

[0028] The first clock end of an odd numbered level cascade structure is shorted to the second clock end of an even numbered level cascade structure, and the second clock end of an odd numbered level cascade structure is shorted to the first clock end of an even numbered level cascade structure.

[0029] The first clock signal CLK1 is inputted into the first clock end of the first level cascade structure, and the second clock signal CLK2 is inputted into the second clock end of the first level cascade structure.

[0030] The driving signal output terminals of each levels of the cascade structures output respectively output the driving signals EM.1, EM.2, EM.3...EM.N to the plurality of pixel circuits of the organic light-emitting display to drive the pixel circuits.

[0031] The working principle of the circuit in a scanning

cycle T will now be described with reference to the drawings. Referring to Fig. 1, Fig. 2 and Fig. 3, the voltage inputted from the first level end VGH is high, and the voltage inputted from the second level end VGL1 and the third level end VGL2 is low. The signals received by the first clock end CLK1 and the second clock end CLK2 of each cascade structure of the first cascade structures and the second cascade structures are the same in frequency. The signal received by the second clock end CLK2 is low level when the signal received by the first clock end CLK1 is high level, and the signal received by the second clock end CLK2 is high level when the signal received by the first clock end CLK1 is low level. This means that the signals received by the first clock end CLK1 and the second clock end CLK2 of each cascade structure of the first cascade structures and the second cascade structures are opposite in phase. To better understand, the terminal numerals are used to represent corresponding signals, e.g. the scanning signal IN, the output scanning signal OUT, the first clock signal CKL1, the second clock signal CKL2, and the driving signal EM. Different components are distinguished by using reference numerals, for example, the first transistor M1 as transistor M1, the first capacitor C1 as capacitor C1.

[0032] In the first clock cycle t1: the clock signal (CLK1) received by the first clock end CLK1 is low level, the transistors M1, M4 and M7 are ON, IN is low level (capacitor C1 is being charged), the clock signal (CLK2) received by the second clock end CLK2 is high level, and thus transistor M2 is ON, with the output scanning signal OUT being high level; the transistor M7 is ON and thus the gate terminal of the transistor M9 is low level; M9 is ON and EM is low level.

[0033] In the second clock cycle t2: CLK1 is high level, Transistors M1, M4 and M7 are OFF, and capacitor C1 discharges and CLK2 is low level. Due to the coupling of the capacitor C1, the gate terminal of the transistor M2 becomes lower level, such that M2 is ON, M3 is ON, and M5 is OFF, thus OUT is low level; M2 is ON, causing M6 and M8 to be ON and M9 to be OFF, and thus EM is high level.

[0034] In the third clock cycle t3: CLK1 is low level, and CLK2 is high level. Transistors M1, M4 and M7 are ON, IN is high level, and thus M2 is OFF; M4 is ON and thus M5 is ON (capacitor C2 being charged), and OUT is high level; the transistor M7 is ON and thus the gate terminal of the transistor M9 is low level ((Capacitor C3 being charged), M9 is ON, and EM is low level.

[0035] In the fourth clock cycle t4: CLK1 is high level, CLK2 is low level, and IN is high level. Transistors M1, M2, M4 and M7 are OFF, so M3 and M5 are OFF, and the capacitor C2 discharges, and thus OUT is high level; capacitor C3 discharges and thus M9 is ON, and EM is low level.

[0036] Accordingly, OUT is at high level in the rest of the scanning cycle, and EM is at low level in the rest of the scanning cycle, which enables the output of the driving signal EM and the shift of one clock signal of the scanning signal IN (i.e., OUT is shifted backward by one clock signal cycle than IN).

[0037] OUT is shifted backward by one clock signal cycle than IN. In addition, because each of the cascade structures are connected in opposite parity by CLK1 and CLK2, and CLK1 and CLK2 are also staggered by their opposition in high and low levels, i.e., the synchronized shifting of CLK1, CLK2 and OUT is realized. Thus, each cascade structure can output the required driving signal (EM.1, EM.2, EM.3...EM.N).

[0038] Only two clock signals and nine transistors are used in the above scanning drive circuit, less than the traditional scan drive circuits. This can greatly enhance the reliability of the circuit, and reduce costs of design and manufacture.

Example 2

[0039] Referring to Fig. 4, in this embodiment, the first low level signal (VGL1) and the second low level signal (VGL2) are the same low level signal. That is, the second low level signal input terminal VGL2 is connected to the second low level VGL1, which is equivalent to that the second electrode of the ninth transistor M9 is connected directly to the second level end VGL1, and at this time the input voltage of the first low level signal (VGL1) and the second low level signal (VGL2) are the same. During the operation of the circuit, when the seventh Transistor M7 is ON, the gate electrode of the ninth transistor M9 is low level vgl1+Vth (vgl1 is the voltage value of the first low level signal, and Vth is the absolute value of the threshold voltage of the P-channel type Thin Film Field Effect Transistor), thus, the ninth transistor M9 is ON, and at this time the source of the ninth transistor M9 is low level (vgl1). This is equivalent to that the gate electrode and drain of the ninth transistor M9 are shorted, and the ninth transistor M9 forms a diode connection. The source output voltage of the ninth transistor M9 is vgl1+Vth, which causes the driving signal to be higher than the required vgl1 by Vth. As a result, in order to keep the driving signal outputted by the driving signal output terminal EM as vgl1, the voltage value (vgl2) of the second low level signal is smaller than the voltage value (vgl1) of the first low level signal in other embodiments, and preferably the voltage value (vgl2) of the second low level signal is smaller by Vth than the voltage value (vgl1) of the first low level signal.

[0040] It should be noted that the second capacitor C2 can be omitted when there is a load capacitance connected to the scanning signal output terminal OUT, but the third capacitor C3 cannot be omitted. The function of the third capacitor C3 is to stabilize the gate electrode voltage of the ninth transistor M9.

[0041] The scanning signal IN is a low level signal in the first clock cycle t of a scanning cycle T of the scanning signal IN, and is a high level signal in the rest of the time; when the scanning signal IN is a low level signal, the first clock signal CLK1 is also a low level signal. The first clock

signal CLK1 and the second clock signal CLK2 are the same in frequency. When the first clock signal CLK1 is high level, the second clock signal CLK2 is low level, and when the first clock signal CLK1 is low level, the second clock signal CLK2 is high level. That is, the scanning signal IN is synchronized in the first clock cycle t of a scanning cycle T to low level with the first clock signal CLK1.

Example 3

[0042] In this embodiment, it is possible to improve the swift high level transformation of the input signal EM by only changing the connection of the third capacitor C3. Specifically, the third capacitor C3 is connected between the driving signal output terminal EM and the gate terminal of the ninth transistor M9, as illustrated in Fig. 5.

[0043] It should be noted that the second capacitor C2 can be omitted when there is a load capacitance connected to the scanning signal output terminal OUT, but the third capacitor C3 cannot be omitted. The third capacitor C3 has a positive feedback effect.

[0044] During the operation of the circuit, when flipping from the first clock cycle t1 to the second clock cycle t2, the output signal EM is changed swiftly from the low level to the high level by the voltage jumping across the third capacitor C3 and the positive feedback effect. When flipping from the second clock cycle t2 to the third clock cycle t3, the output signal EM is changed swiftly from the high level to the low level by the voltage jumping across the third capacitor C3 and the positive feedback effect. In the present embodiment the third capacitor C3 is used to provide positive feedback for stable and swift output terminal of high and low level. Thus, it is possible to enhance the load capacity and transformation ability between the high and low levels of the drive circuit, making the output terminal of high and low levels closer to the power level.

[0045] Referring to Fig. 6, an organic light-emitting display is provided, which includes a scanning drive circuit of any of the above Embodiments One to Three, and a plurality of pixel circuits 112 of the organic light-emitting display. The scanning drive circuit includes a first scan driver 110 and a second scan driver 116. The driving signal output terminal (EM.1, EM.2, EM.3...EM.N) of each cascade structure of the first scan driver 110 is connected a driving signal input terminal of the pixel circuit 112 of the organic light-emitting display, so as to output driving signal (EM.1, EM.2, EM.3... EM.N) to drive the pixel circuit 112 of the organic light-emitting display.

[0046] The organic light-emitting display further includes a data driver 114 and a timing controller 118. The data driver 114 is configured to supply data signal to the pixel circuit 112 of the organic light-emitting display, the second scan driver 116 is configured to supply scanning signal to the pixel circuit 112 of the organic light-emitting display, the timing controller 118 is configured to supply timing signal and high and low level signals to the first clock end, the second clock end, the scanning signal input terminal, the first level end, the second level end and the third level end of the first scan driver 110 and the second scan driver 116, and ELVDD is configured to supply power signal to all the pixel circuits 112 of the organic light-emitting display.

[0047] The above are embodiments of the invention described in detail, and should not be deemed as limitations to the scope of the present invention. It should be noted that variations and improvements will become apparent to those skilled in the art to which the present invention pertains. Therefore, the scope of the present disclosure is defined by the appended claims.

Claims

1. A scanning drive circuit, comprising a first scan driver (110) for sequentially outputting selection signals and a second scan driver (116) for sequentially outputting transmission signals, wherein the first scan driver comprises a plurality of first cascade structures and the second scan driver comprises a plurality of second cascade structures, each cascade structure of the first cascade structures and/or the second cascade structures comprises:

   a scanning signal input terminal (IN);
   a scanning signal output terminal (OUT);
   a first transistor (M1), comprising an input terminal connected to the scanning signal input terminal (IN) of the cascade structure or to a scanning signal output terminal (OUT) of a precedent cascade structure, a gate terminal connected to a first clock end (CKL1), and an output terminal;
   a second transistor (M2), comprising a gate terminal connected to the output terminal of the first transistor, an input terminal connected to a second clock end (CKL2), and an output terminal connected to the scanning signal output terminal;
   a third transistor (M3), comprising an input terminal connected to a first level end (VGH), a gate terminal connected to the scanning signal output terminal, and an output terminal;
   a fourth transistor (M4), comprising an input terminal connected to the output terminal of the third transistor, a gate terminal connected to the first clock end, and an output terminal connected to a second level end (VGL1);
   a fifth transistor (M5), comprising an input terminal connected to the first level end, a gate terminal connected to the output terminal of the third transistor, and an output terminal connected to the scanning signal output terminal;
   a sixth transistor (M6), comprising an input terminal connected to the first level end, a gate terminal connected to the scanning signal output terminal, and an output terminal;

a seventh transistor (M7), comprising an input terminal connected to the output terminal of the sixth transistor, a gate terminal connected to the first clock end, and an output terminal connected to the second level end;
an eighth transistor (M8), comprising an input terminal connected to the first level end, a gate terminal connected to the scanning signal output terminal, and an output terminal connected to a driving signal output terminal (EM);
a ninth transistor (M9), comprising an input terminal connected to the driving signal output terminal, a gate terminal connected to the output terminal of the sixth transistor, and an output terminal connected to a third level end (VGL2); and
a first capacitor (C1) connected between the gate terminal and the output terminal of the second transistor.

2. The scanning drive circuit of claim 1, wherein the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, the seventh transistor, the eighth transistor and the ninth transistor are Thin Film Field Effect Transistors.

3. The scanning drive circuit of claim 1, wherein a second capacitor (C2) is connected between the first level end and the gate terminal of the sixth transistor.

4. The scanning drive circuit of any one of claims 1-3, wherein a third capacitor is connected between the driving signal output terminal and the gate terminal of the ninth transistor.

5. The scanning drive circuit of any one of claims 1-3, wherein a third capacitor (C3) is connected between the second level end and the gate terminal of the ninth transistor.

6. The scanning drive circuit of claim 5, wherein the third level end and the second level end are the same level end.

7. An organic light-emitting display, comprising a pixel circuit (112), a data driver (114) and a timing controller (118), wherein the organic light-emitting display further comprises the scanning drive circuit of any one of claims 1-6, the timing controller supplies timing signals and high and low level signals to the first clock end, the second clock end, the scanning signal input terminal, the first level end, the second level end and the third level end of the scanning drive circuit, the driving signal output terminal of the scanning drive circuit is connected to the driving signal input terminal of the pixel circuit so as to output driving signals for driving the pixel circuit to operate.

8. The organic light-emitting display of claim 7, wherein the timing controller is arranged to supply signals to the first clock end and the second clock end of each cascade structure of the first cascade structures and the second cascade structures such that the signals received are the same in frequency, the signal received by the second clock end is at low level when the signal received by the first clock end is at high level, and the signal received by the second clock end is at high level when the signal received by the first clock end is at low level.

9. The organic light-emitting display of claim 7 or 8, wherein the voltage value inputted at the third level end is smaller than the voltage value inputted at the second level end.

10. The organic light-emitting display of claim 7 or 8, wherein the voltage value inputted at the first level end is high level, and the voltages inputted at the second and third level ends are high level.

Patentansprüche

1. Abtastungsansteuerungsschaltung, die eine erste Abtastungsansteuerung (110) zum aufeinander folgenden Ausgeben von Auswahlsignalen und eine zweite Abtastungsansteuerung (116) zum aufeinander folgenden Ausgeben von Übertragungssignalen umfasst, wobei die erste Abtastungsansteuerung eine Vielzahl von ersten Kaskadenstrukturen aufweist und die zweite Abtastungsansteuerung eine Vielzahl von zweiten Kaskadenstrukturen aufweist, wobei jede Kaskadenstruktur der ersten Kaskadenstrukturen und/oder der zweiten Kaskadenstrukturen Folgendes umfasst:

einen Abtastsignaleingangsanschluss (IN);
einen Abtastsignalausgangsanschluss (OUT);
einen ersten Transistor (M1) mit einem mit dem Abtastsignaleingangsanschluss (IN) der Kaskadenstruktur oder mit einem Abtastsignalausgangsanschluss (OUT) einer vorhergehenden Kaskadenstruktur verbundenen Eingangsanschluss, einem mit einem ersten Taktende (CKL1) verbundenen Gate-Anschluss, und einem Ausgangsanschluss;
einen zweiten Transistor (M2) mit einem mit dem Ausgangsanschluss des ersten Transistors verbundenen Gate-Anschluss, einem mit einem zweiten Taktende (CKL2) verbundenen Eingangsanschluss, und einem mit dem Abtastsignalausgangsanschluss verbundenen Ausgangsanschluss;
einen dritten Transistor (M3) mit einem mit einem ersten Niveauende (VGH) verbundenen Eingangsanschluss, einem mit dem Abtastsig-

nalausgangsanschluss verbundenen Gate-Anschluss, und einem Ausgangsanschluss;
einen vierten Transistor (M4) mit einem mit dem Ausgangsanschluss des dritten Transistors verbundenen Eingangsanschluss, einem mit dem ersten Taktende verbundenen Gate-Anschluss, und einem mit einem zweiten Niveauende (VGL1) verbundenen Ausgangsanschluss;
einen fünften Transistor (M5) mit einem mit dem ersten Niveauende verbundenen Eingangsanschluss, einem mit dem Ausgangsanschluss des dritten Transistors verbundenen Gate-Anschluss, und einem mit dem Abtastsignalausgangsanschluss verbundenen Ausgangsanschluss;
einen sechsten Transistor (M6) mit einem mit dem ersten Niveauende verbundenen Eingangsanschluss, einem mit dem Abtastsignalausgangsanschluss verbundenen Gate-Anschluss, und einem Ausgangsanschluss;
einen siebten Transistor (M7) mit einem mit dem Ausgangsanschluss des sechsten Transistors verbundenen Eingangsanschluss, einem mit dem ersten Taktende verbundenen Gate-Anschluss, und einem mit dem zweiten Niveauende verbundenen Ausgangsanschluss;
einen achten Transistor (M8) mit einem mit dem ersten Niveauende verbundenen Eingangsanschluss, einem mit dem Abtastsignalausgangsanschluss verbundenen Gate-Anschluss, und einem mit einem Ansteuersignalausgangsanschluss (EM) verbundenen Ausgangsanschluss;
einen neunten Transistor (M9) mit einem mit dem Ansteuersignalausgangsanschluss verbundenen Eingangsanschluss, einem mit dem Ausgangsanschluss des sechsten Transistors verbundenen Gate-Anschluss, und einem mit einem dritten Niveauende (VGL2) verbundenen Ausgangsanschluss; und
einen ersten Kondensator (C1), der zwischen dem Gate-Anschluss und dem Ausgangsanschluss des zweiten Transistors verbunden ist.

2. Abtastungsansteuerungsschaltung nach Anspruch 1, wobei es sich bei dem ersten Transistor, dem zweiten Transistor, dem dritten Transistor, dem vierten Transistor, dem fünften Transistor, dem sechsten Transistor, dem siebten Transistor, dem achten Transistor und dem neunten Transistor um Dünnfilm-Feldeffekttransistoren handelt.

3. Abtastungsansteuerungsschaltung nach Anspruch 1, wobei ein zweiter Kondensator (C2) zwischen dem ersten Niveauende und dem Gate-Anschluss des sechsten Transistors verbunden ist.

4. Abtastungsansteuerungsschaltung nach einem der Ansprüche 1 bis 3, wobei ein dritter Kondensator zwischen dem Ansteuersignalausgangsanschluss und dem Gate-Anschluss des neunten Transistors verbunden ist.

5. Abtastungsansteuerungsschaltung nach einem der Ansprüche 1 bis 3, wobei ein dritter Kondensator (C3) zwischen dem zweiten Niveauende und dem Gate-Anschluss des neunten Transistors verbunden ist.

6. Abtastungsansteuerungsschaltung nach Anspruch 5, wobei es sich bei dem dritten Niveauende und dem zweiten Niveauende um das gleiche Niveauende handelt.

7. Organische lichtemittierende Anzeige mit einer Pixelschaltung (112), einer Datenansteuerung (114) und einer Zeitsteuerung (118), wobei die organische lichtemittierende Anzeige weiterhin die Abtastungsansteuerungsschaltung nach einem der Ansprüche 1 bis 6 umfasst, wobei die Zeitsteuerung Zeitsignale und Signale mit hohem und niedrigem Niveau an das erste Taktende, das zweite Taktende, den Abtastsignaleingangsanschluss, das erste Niveauende, das zweite Niveauende und das dritte Niveauende der Abtastungsansteuerungsschaltung liefert, wobei der Ansteuersignalausgangsanschluss der Abtastungsansteuerungsschaltung mit dem Ansteuersignaleingangsanschluss der Pixelschaltung verbunden ist, um Ansteuersignale zur Ansteuerung des Betriebs der Pixelschaltung auszugeben.

8. Organische lichtemittierende Anzeige nach Anspruch 7, wobei die Zeitsteuerung dazu ausgerichtet ist, Signale an das erste Taktende und das zweite Taktende jeder Kaskadenstruktur der ersten Kaskadenstrukturen und der zweiten Kaskadenstrukturen zu liefern, so dass die empfangenen Signale die gleiche Frequenz aufweisen, wobei das von dem zweiten Taktende empfangene Signal einen niedrigen Niveau aufweist, wenn das von dem ersten Taktende empfangene Signal ein hohes Niveau aufweist, und das von dem zweiten Taktende empfangene Signal ein hohes Niveau aufweist, wenn das von dem ersten Taktende empfangene Signal ein niedriges Niveau aufweist.

9. Organische lichtemittierende Anzeige nach Anspruch 7 oder 8, wobei der an dem dritten Niveauende eingegebene Spannungswert kleiner ist als der an dem zweiten Niveauende eingegebene Spannungswert.

10. Organische lichtemittierende Anzeige nach Anspruch 7 oder 8, wobei der an dem ersten Niveauende eingegebene Spannungswert ein hohes Niveau aufweist und die an dem zweiten Niveauende

und an dem dritten Niveauende eingegebenen Spannungswerte ein hohes Niveau aufweisen.

Revendications

1. Circuit de commande de balayage, comprenant un premier organe de commande de balayage (110) destiné à émettre séquentiellement des signaux de sélection et un deuxième organe de commande de balayage (116) destiné à émettre séquentiellement des signaux de transmission, ledit premier organe de commande de balayage comprenant une pluralité de premières structures en cascade et ledit deuxième organe de commande de balayage comprenant une pluralité de deuxièmes structures en cascade, chaque structure en cascade des premières structures en cascade et/ou des deuxièmes structures en cascade comprenant :

une borne d'entrée de signaux de balayage (IN) ;
une borne de sortie de signaux de balayage (OUT) ;
un premier transistor (M1), comprenant une borne d'entrée reliée à la borne d'entrée de signaux de balayage (IN) de la structure en cascade ou à une borne de sortie de signaux de balayage (OUT) d'une structure en cascade précédente, une borne de grille reliée à une première extrémité d'horloge (CKL1), et une borne de sortie ;
un deuxième transistor (M2), comprenant une borne de grille reliée à la borne de sortie du premier transistor, une borne d'entrée reliée à une deuxième extrémité d'horloge (CKL2), et une borne de sortie reliée à la borne de sortie de signaux de balayage ;
un troisième transistor (M3), comprenant une borne d'entrée reliée à une extrémité de premier niveau (VGH), une borne de grille reliée à la borne de sortie de signaux de balayage, et une borne de sortie ;
un quatrième transistor (M4), comprenant une borne d'entrée reliée à la borne de sortie du troisième transistor, une borne de grille reliée à la première extrémité d'horloge, et une borne de sortie reliée à une extrémité de deuxième niveau (VGL1) ;
un cinquième transistor (M5), comprenant une borne d'entrée reliée à l'extrémité de premier niveau, une borne de grille reliée à la borne de sortie du troisième transistor, et une borne de sortie reliée à la borne de sortie de signaux de balayage ;
un sixième transistor (M6), comprenant une borne d'entrée reliée à l'extrémité de premier niveau, une borne de grille reliée à la borne de sortie de signaux de balayage, et une borne de sortie ;
un septième transistor (M7), comprenant une borne d'entrée reliée à la borne de sortie du sixième transistor, une borne de grille reliée à la première extrémité d'horloge, et une borne de sortie reliée à l'extrémité de deuxième niveau ;
un huitième transistor (M8), comprenant une borne d'entrée reliée à l'extrémité de premier niveau, une borne de grille reliée à la borne de sortie de signaux de balayage, et une borne de sortie reliée à une borne de sortie de signaux de commande (EM) ;
un neuvième transistor (M9), comprenant une borne d'entrée reliée à la borne de sortie de signal de commande, une borne de grille reliée à la borne de sortie du sixième transistor, et une borne de sortie reliée à une extrémité de troisième niveau (VGL2) ; et
un premier condensateur (C1) branché entre la borne de grille et la borne de sortie du deuxième transistor.

2. Circuit de commande de balayage selon la revendication 1, dans lequel le premier transistor, le deuxième transistor, le troisième transistor, le quatrième transistor, le cinquième transistor, le sixième transistor, le septième transistor, le huitième transistor et le neuvième transistor sont des transistors à effet de champ à film mince.

3. Circuit de commande de balayage selon la revendication 1, dans lequel un deuxième condensateur (C2) est branché entre l'extrémité de premier niveau et la borne de grille du sixième transistor.

4. Circuit de commande de balayage selon l'une quelconque des revendications 1 à 3, dans lequel un troisième condensateur est branché entre la borne de sortie de signaux de commande et la borne de grille du neuvième transistor.

5. Circuit de commande de balayage selon l'une quelconque des revendications 1 à 3, dans lequel un troisième condensateur (C3) est branché entre l'extrémité de deuxième niveau et la borne de grille du neuvième transistor.

6. Circuit de commande de balayage selon la revendication 5, dans lequel l'extrémité de troisième niveau et l'extrémité de deuxième niveau sont la même extrémité de niveau.

7. Écran à diodes électroluminescentes organiques, comprenant un circuit à pixels (112), un organe de commande de données (114) et un organe de commande de rythme (118), ledit écran à diodes électroluminescentes organiques comprenant en outre le circuit de commande de balayage selon l'une quel-

conque des revendications 1 à 6, l'organe de commande de rythme fournissant des signaux de rythme ainsi que des signaux de niveaux élevé et bas à la première extrémité d'horloge, la deuxième extrémité d'horloge, la borne d'entrée de signaux de balayage, l'extrémité de premier niveau, l'extrémité de deuxième niveau et l'extrémité de troisième niveau du circuit de commande de balayage ; la borne de sortie de signaux de commande du circuit de commande de balayage étant reliée à la borne d'entrée de signaux de commande du circuit à pixels de façon à émettre des signaux de commande destinés à commander le fonctionnement du circuit à pixels.

8. Écran à diodes électroluminescentes organiques selon la revendication 7, dans lequel l'organe de commande de rythme est agencé pour fournir des signaux à la première extrémité d'horloge et à la deuxième extrémité d'horloge de chaque structure en cascade des premières structures en cascade et deuxièmes structures en cascade de manière que les signaux reçus soient de la même fréquence, le signal reçu par la deuxième extrémité d'horloge étant de bas niveau lorsque le signal reçu par la première extrémité d'horloge est de haut niveau, et le signal reçu par la deuxième extrémité d'horloge étant de haut niveau lorsque le signal reçu par la première extrémité d'horloge est de bas niveau.

9. Écran à diodes électroluminescentes organiques selon la revendication 7 ou 8, dans lequel la valeur de tension entrée à l'extrémité de troisième niveau est inférieure à la valeur de tension entrée à l'extrémité de deuxième niveau.

10. Écran à diodes électroluminescentes organiques selon la revendication 7 ou 8, dans lequel la valeur de tension entrée à l'extrémité de premier niveau est de haut niveau, et les tensions entrées aux extrémités de deuxième et troisième niveau sont de haut niveau.

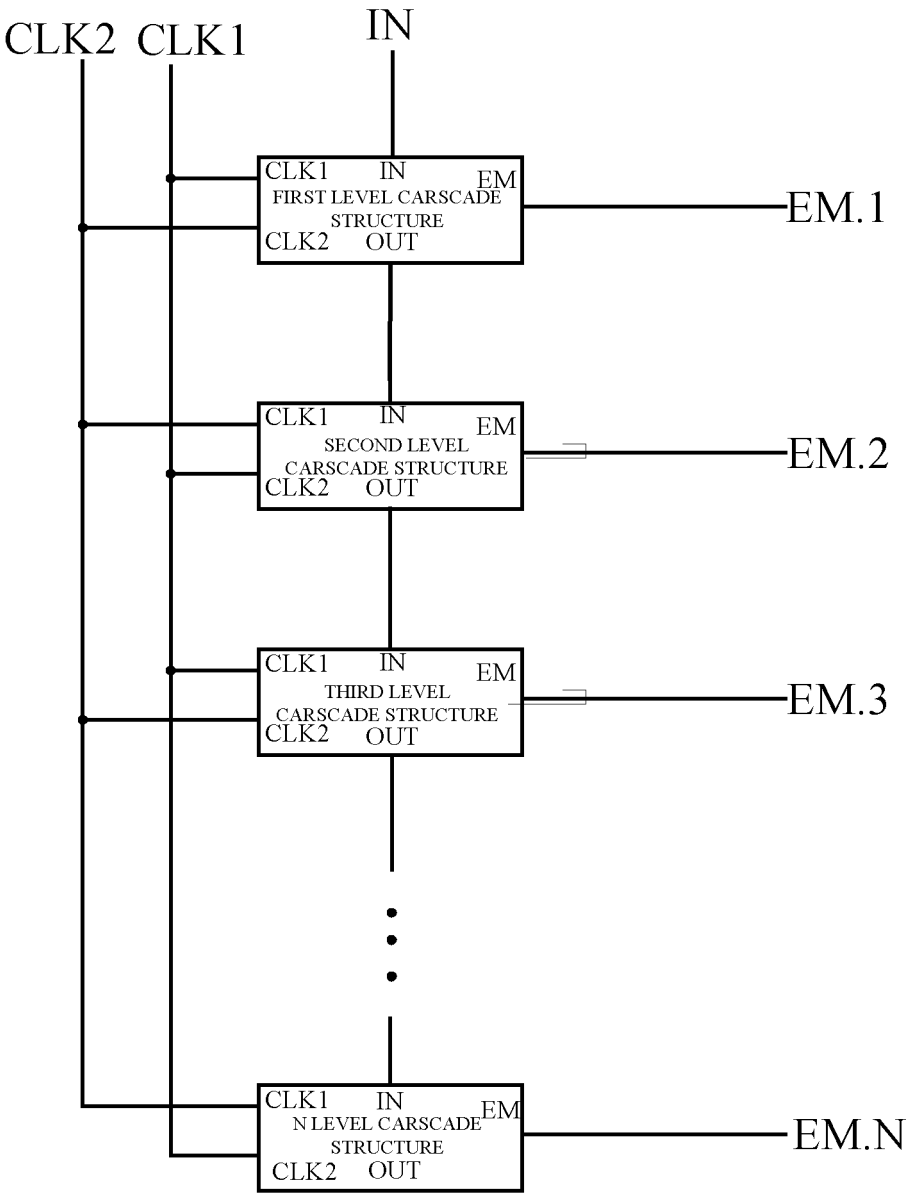
CLK2
CLK1
IN
CLK1
IN
EM
FIRST LEVEL CARSCADE STRUCTURE
CLK2
OUT
EM.1
CLK1
IN
EM
SECOND LEVEL CARSCADE STRUCTURE
CLK2
OUT
EM.2
CLK1
IN
EM
THIRD LEVEL CARSCADE STRUCTURE
CLK2
OUT
EM.3
CLK1
IN
EM
N LEVEL CARSCADE STRUCTURE
CLK2
OUT
EM.N

Fig. 1

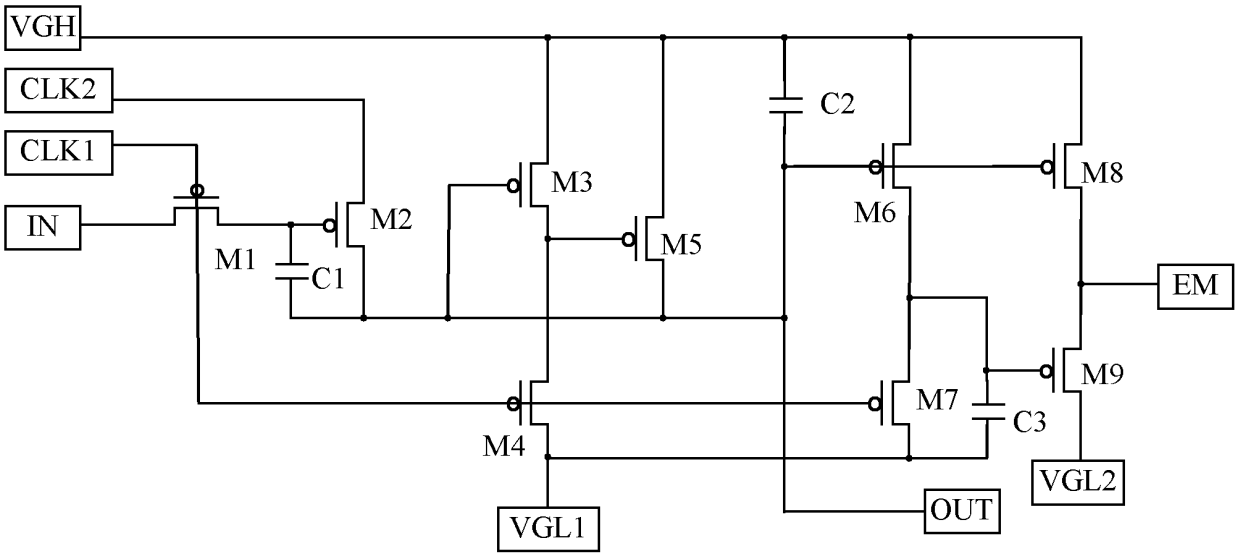
VGH
CLK2
CLK1
IN
M1
C1
M2
M3
M5
C2
M6
M8
EM
M4
M7
C3
M9
VGL1
OUT
VGL2

Fig. 2

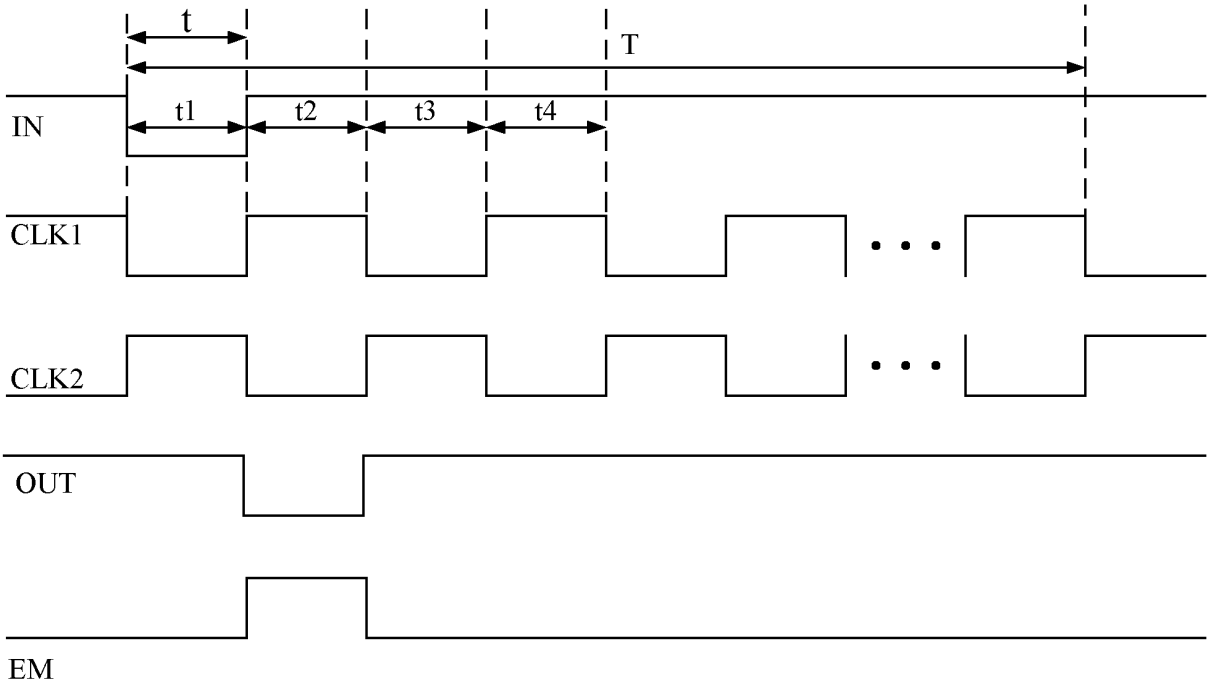
t
T
IN
t1
t2
t3
t4
CLK1
CLK2
OUT
EM

Fig. 3

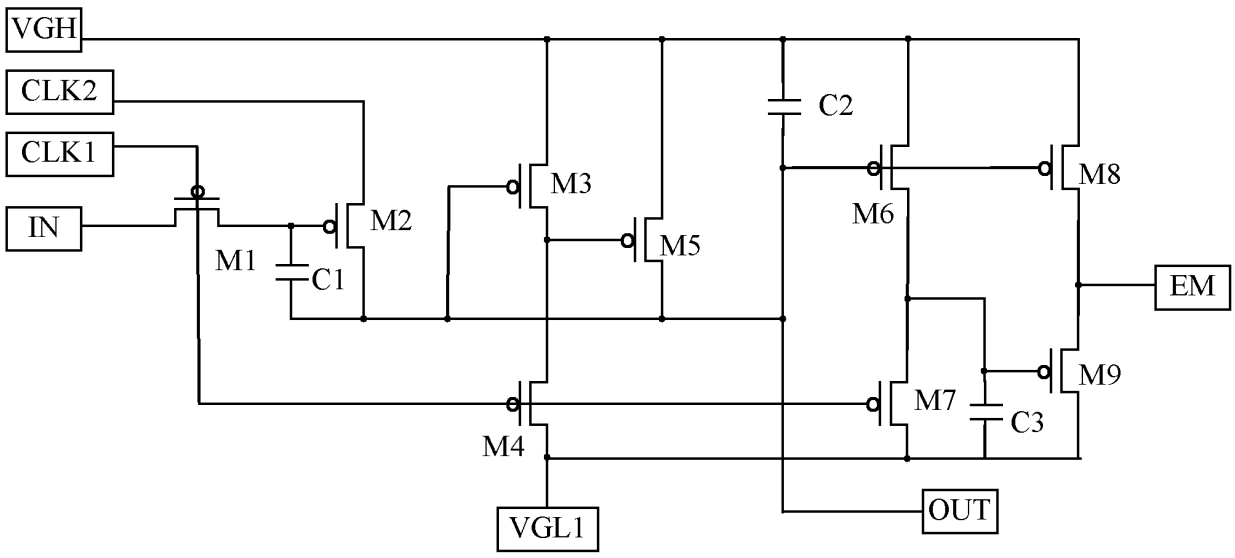
VGH
CLK2
CLK1
IN
M1
M2
C1
M3
M5
C2
M6
M8
EM
M9
M7
C3
M4
VGL1
OUT

Fig. 4

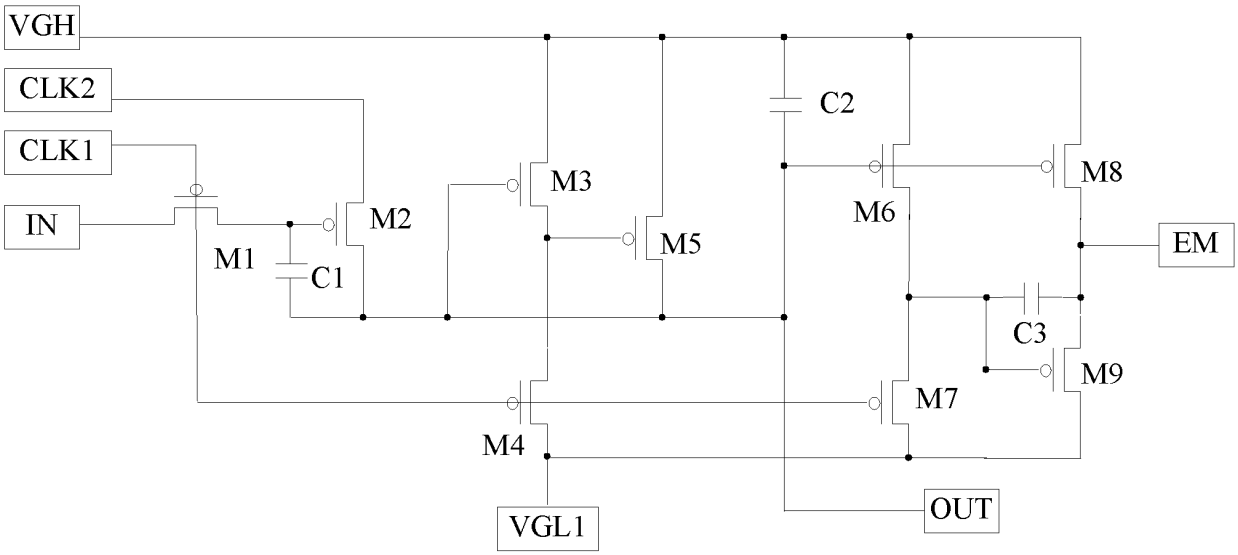
VGH
CLK2
CLK1
IN
M1
M2
C1
M3
M5
C2
M6
M8
EM
C3
M9
M7
M4
VGL1
OUT

Fig. 5

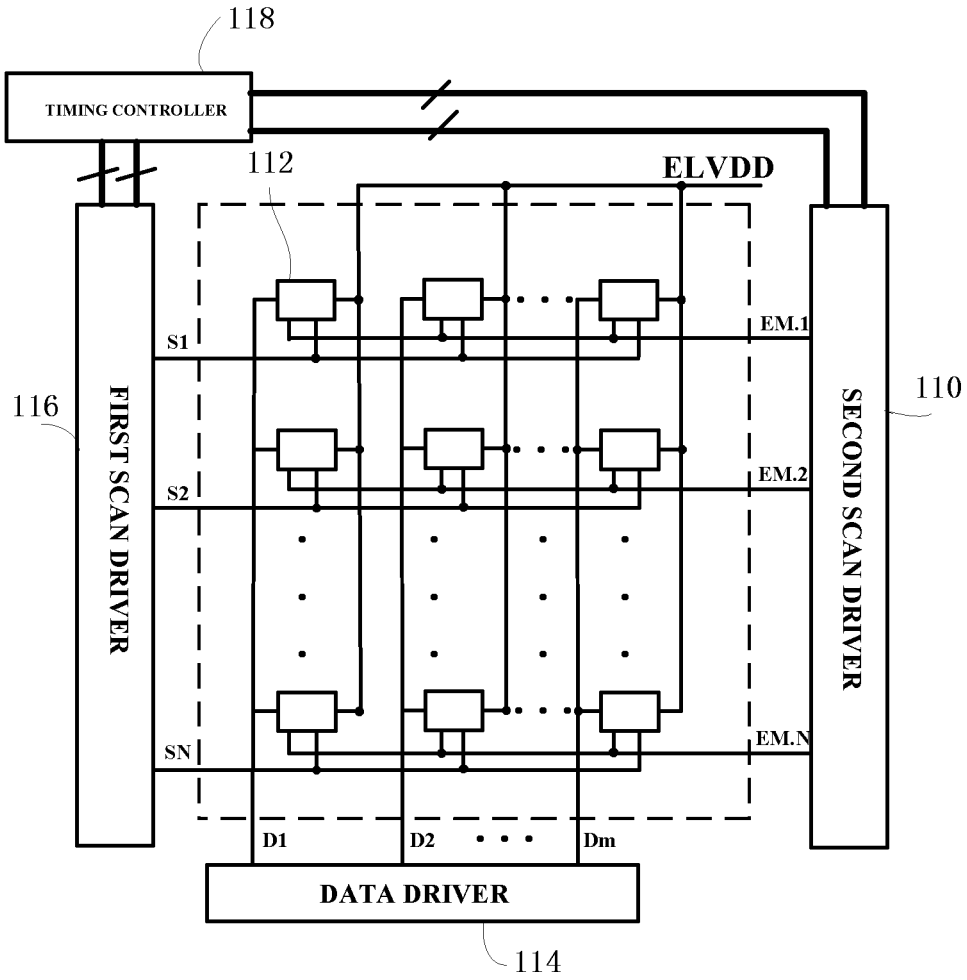
118
TIMING CONTROLLER
112
ELVDD
116
FIRST SCAN DRIVER
S1
S2
SN
EM.1
EM.2
EM.N
110
SECOND SCAN DRIVER
D1
D2
Dm
DATA DRIVER
114

Fig. 6

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1965371 A2 **[0003]**
- EP 1763003 A2 **[0003]**
- US 20120139962 A1 **[0003]**
- US 20120212517 A1 **[0003]**

专利名称(译)	扫描驱动电路及有机发光显示器		
公开(公告)号	EP3091532B1	公开(公告)日	2020-04-08
申请号	EP2014876723	申请日	2014-12-29
[标]申请(专利权)人(译)	昆山工研院新型平板显示技术中心有限公司 昆山国显光电有限公司		
申请(专利权)人(译)	昆山新型平板显示技术中心CO.LTD 昆山GO-维信诺光电科技有限公司.		
当前申请(专利权)人(译)	昆山新型平板显示技术中心有限公司. 昆山GO-维信诺光电科技有限公司.		
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发明人	YANG, NAN HU, SIMING ZHANG, TINGTING ZHANG, XIAOBAO NAGAI, HAJIME HUANG, XIUQI		
IPC分类号	G09G3/3266 G11C19/28		
CPC分类号	G09G3/3266 G09G2300/0861 G09G2310/0286 G11C19/28 G09G2310/0262 G09G2310/08		
优先权	201310744988.8 2013-12-30 CN 201410464972.6 2014-09-12 CN		
其他公开文献	EP3091532A1 EP3091532A4		
外部链接	Espacenet		

摘要(译)

扫描驱动电路和有机发光显示器。 扫描驱动电路包括顺序输出选择信号的第一扫描驱动器和顺序输出发送信号的第二扫描驱动器。 第一扫描驱动器包括多个第一级联结构，第二扫描驱动器包括多个第二级联结构。 第一级联结构或/和第二级联结构的每个级联结构包括九个晶体管和一个电容器。 扫描驱动电路采用较少的时钟信号和晶体管，可以显着提高产品电路的可靠性，同时也降低了产品的设计成本和生产成本。

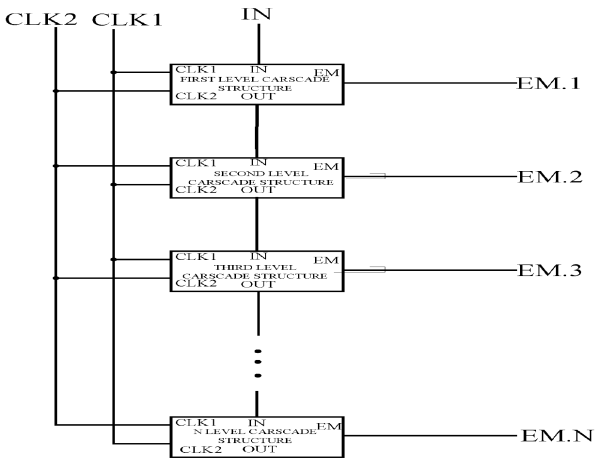

Fig. 1