



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
11.07.2012 Bulletin 2012/28

(51) Int Cl.:
G09G 3/32^(2006.01) G11C 19/28^(2006.01)

(21) Application number: **11193980.7**

(22) Date of filing: **16.12.2011**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
 Designated Extension States:
BA ME

(72) Inventors:
 • **Jang, Hwan-Soo**
Chungcheongnam-do (KR)
 • **Pyon, Chang-Soo**
Chungcheongnam-do (KR)

(30) Priority: **06.01.2011 KR 20110001419**

(74) Representative: **Walaski, Jan Filip**
Venner Shipley LLP
200 Aldersgate
London
EC1A 4HD (GB)

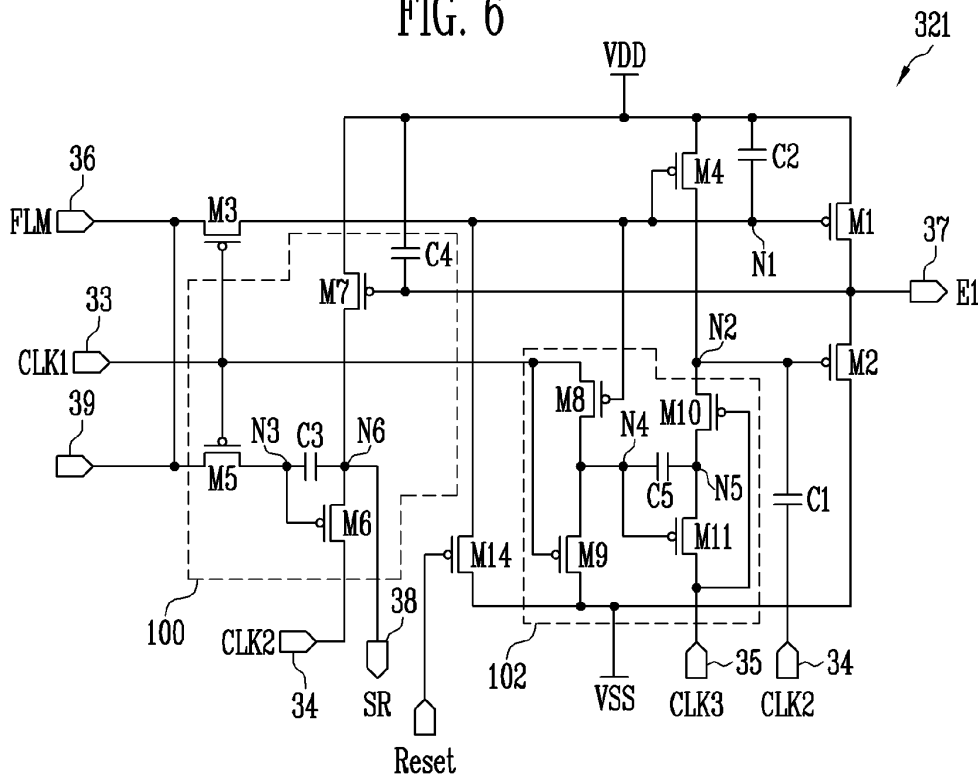
(71) Applicant: **Samsung Mobile Display Co., Ltd.**
Gyunggi-Do 446-711 (KR)

(54) **Emission control line driver and organic light emitting display using the same**

(57) An emission control line driver is capable of securing the stability of an output and of freely controlling the width of emission control signals. The emission control line driver includes a plurality of stages (321) respectively coupled to emission control lines (E1). Each of the

stages includes a plurality of transistors (M1-M14) that are configured to output the emission control signal. The width of the emission control signal may be controlled to correspond to the width of a start signal. Furthermore, a circuit structure of the stages is simplified.

FIG. 6



Description

[0001] The present invention relates to an emission control line driver and an organic light emitting display using the same.

[0002] Recently, various flat panel displays (FPDs) with reduced weight and volume as compared to cathode ray tube (CRT) displays have been developed. The FPDs include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), and an organic light emitting display.

[0003] Among the FPDs, the organic light emitting display displays an image using organic light emitting diodes (OLEDs) that generate light by re-combination of electrons and holes. The organic light emitting display has a fast response speed and is driven with low power consumption. A typical organic light emitting display supplies current corresponding to data signals to the OLEDs by using transistors formed in pixels so that light is emitted by the OLEDs.

[0004] The typical organic light emitting display includes a data driver for supplying the data signals to data lines, a scan driver for sequentially supplying scan signals to scan lines, an emission control line driver for supplying emission control signals to emission control lines, and a display unit including a plurality of pixels coupled to the data lines, the scan lines, and the emission control lines.

[0005] The pixels included in the display unit are selected, when the scan signals are supplied to the scan lines, to receive the data signals from the data lines. The pixels that receive the data signals generate light with brightness (e.g., predetermined brightness) corresponding to the data signals and display a predetermined image. Here, the emission times of the pixels are controlled by the emission control signals that are supplied from the emission control lines. In general, the emission control signals are supplied to overlap the scan signals that are supplied to one scan line or two scan lines to set the pixels, to which the data signals are supplied, in a non-emission state.

[0006] Therefore, the emission control line driver includes stages coupled to the emission control lines. The stages receive at least four clock signals and output high or low voltages to output lines.

[0007] However, since the stages included in the typical emission control line driver are driven by at least four clock signals, a large number of transistors are included. Therefore, manufacturing cost increases and it is difficult to secure the reliability of driving. In addition, when the emission control line driver is formed of a PMOS transistor, a low level output is unstable.

[0008] To be specific, when a low signal is supplied to an emission control line, the gate electrode of the transistor that outputs the low signal is maintained at a lower voltage than the low signal. However, the voltage of the gate electrode of the transistor increases due to leakage current and the output of the low signal is unstable.

[0009] Accordingly, embodiments of the present invention are directed toward an emission control line driver capable of securing the stability of an output and of freely controlling the width of emission control signals, and an organic light emitting display using the same.

[0010] According to an embodiment of the present invention, there is provided an emission control line driver including a plurality of stages. Each of the stages includes a first transistor coupled between a first output terminal and a first power source, the first transistor being configured to be turned on or off to correspond to a voltage applied to a first node that is coupled to a gate electrode of the first transistor, a second transistor coupled between the first output terminal and a second power source that outputs a voltage that is lower than the first power source, the second transistor being configured to be turned on or off to correspond to a voltage applied to a second node that is coupled to a gate electrode of the second transistor, a third transistor coupled between a fourth input terminal and the first node, and having a gate electrode coupled to a first input terminal, a fourth transistor coupled between the first power source and the second node, and having a gate electrode coupled to the first node, a first controller coupled to the first input terminal and a second input terminal to supply a sampling signal to a second output terminal, a second controller coupled to the first input terminal and a third input terminal to control the voltage of the second node, and a first capacitor coupled between the second input terminal and the second node.

[0011] The emission control line driver may further include a second capacitor coupled between the first node and the first power source. The first input terminal may be configured to receive a first clock signal. The second input terminal may be configured to receive a second clock signal. The third input terminal may be configured to receive a third clock signal. The fourth input terminal may be configured to receive a start signal or a sampling signal of a previous stage. The first clock signal, the second clock signal, and the third clock signal may not overlap each other. Each of the first clock signal and the second clock signal may be set in a period of i (i is a natural number) horizontal periods. The third clock signal may be set in a period of $i/2$ horizontal periods. The third clock signal may be supplied in a horizontal period after the first clock signal or the second clock signal is supplied in the horizontal period.

[0012] The first controller may include a fifth transistor coupled between the fourth input terminal and a third node, and having a gate electrode coupled to the first input terminal, a sixth transistor coupled between a sixth node and the second input terminal, and having a gate electrode coupled to the third node, a seventh transistor coupled between the sixth node and the first power source, and having a gate electrode coupled to the first output terminal, a third capacitor coupled between the third node and the sixth node, and a fourth capacitor coupled between the first output terminal and the first power

source. The second output terminal may be electrically coupled to the sixth node.

[0013] The second controller may include an eighth transistor coupled between the first input terminal and a fourth node, and having a gate electrode coupled to the first node, a ninth transistor coupled between the fourth node and the second power source, and having a gate electrode coupled to the first input terminal, a tenth transistor coupled between the second node and a fifth node, and having a gate electrode coupled to the third input terminal, an eleventh transistor coupled between the fifth node and the third input terminal, and having a gate electrode coupled to the fourth node, and a fifth capacitor coupled between the fourth node and the fifth node.

[0014] The emission control line driver may further include a twelfth transistor coupled between the fourth input terminal and the third transistor, the twelfth transistor being configured to be turned on when a first control signal is supplied to a gate electrode of the twelfth transistor, and a thirteenth transistor coupled between a fifth input terminal and the first controller, the thirteenth transistor being configured to be turned on when a second control signal is supplied to a gate electrode of the thirteenth transistor. The first control signal and the second control signal may not overlap each other. The emission control line driver may further include a fourteenth transistor coupled between the first node and the second power source, the fourteenth transistor being configured to be turned on when a reset signal is supplied to a gate electrode of the fourteenth transistor. The reset signal may be commonly supplied to all of the stages.

[0015] According to an embodiment, an organic light emitting display includes a scan driver for sequentially supplying scan signals to scan lines, a data driver for supplying data signals to data lines, an emission control line driver for supplying emission control signals to emission control lines, and pixels positioned at crossing regions of the scan lines, the data lines, and the emission control lines. The emission control line driver includes stages respectively coupled to the emission control lines. Each of the stages includes a first transistor coupled between a first output terminal and a first power source, the first transistor being configured to be turned on or off to correspond to a voltage applied to a first node that is coupled to a gate electrode of the first transistor, a second transistor coupled between the first output terminal and a second power source that outputs a voltage that is lower than the first power source, the second transistor being configured to be turned on or off to correspond to a voltage applied to a second node that is coupled to a gate electrode of the second transistor, a third transistor coupled between a fourth input terminal and the first node, and having a gate electrode coupled to a first input terminal, a fourth transistor coupled between the first power source and the second node, and having a gate electrode coupled to the first node, a first controller coupled to the first input terminal and a second input terminal to supply a sampling signal to a second output terminal, a second

controller coupled to the first input terminal and a third input terminal to control the voltage of the second node, and a first capacitor coupled between the second input terminal and the second node.

[0016] According to the emission control line driver illustrated in the embodiments of the present invention and the organic light emitting display using the same, the voltage of the gate electrode of the transistor that outputs the low signal is periodically reduced using the clock signal so that the stability of an output may be secured. In addition, according to the embodiments of the present invention, the width of the emission control signal may be controlled to correspond to the width of the start signal. Furthermore, according to the embodiments of the present invention, since the stages receive three clock signals, the circuit structure may be simplified.

[0017] The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention, and, together with the description, serve to explain the principles of the present invention.

FIG. 1 is a block diagram illustrating an organic light emitting display according to an embodiment of the present invention;

FIG. 2 is a block diagram schematically illustrating stages of an emission control line driver of FIG. 1; FIG. 3 is a circuit diagram illustrating a first embodiment of one of the stages of FIG. 2;

FIG. 4 is a waveform chart illustrating the operation processes of one of the stages of FIG. 3;

FIG. 5 is a circuit diagram illustrating a second embodiment of one of the stages of FIG. 2; and

FIG. 6 is a circuit diagram illustrating a third embodiment of one of the stages of FIG. 2.

[0018] Referring to FIG. 1, the organic light emitting display according to an embodiment of the present invention includes a display unit 40 that includes pixels 50 positioned at the crossing regions of scan lines S1 to Sn, data lines D1 to Dm, and emission control lines E1 to En, a scan driver 10 for driving the scan lines S1 to Sn, a data driver 20 for driving the data lines D1 to Dm, an emission control line driver 30 for driving the emission control lines E1 to En, and a timing controller 60 for controlling the drivers 10, 20, and 30.

[0019] The scan driver 10 sequentially supplies scan signals to the scan lines S1 to Sn. When the scan signals are supplied to the scan lines S1 to Sn, the pixels 50 are selected in units of horizontal lines (e.g., line-by-line).

[0020] The data driver 20 supplies data signals to the data lines D1 to Dm in synchronization with the scan signals. The data signals supplied to the data lines D1 to Dm are supplied to the pixels 50 that are selected by the scan signals.

[0021] The emission control line driver 30 sequentially supplies emission control signals to the emission control lines E1 to En. Here, the emission control line driver 30 supplies the emission control signals so that the pixels

50 are set in a non-emission state during a period when the voltages corresponding to the data signals are charged. Therefore, the emission control signal supplied to the i th (i is a natural number) emission control line E_i overlaps the scan signal supplied to the i th scan line S_i . On the other hand, the width of the emission control signal may be suitably set to correspond to the structure of the pixel 50 and the brightness to be realized.

[0022] FIG. 2 is a block diagram schematically illustrating stages of the emission control line driver of FIG. 1.

[0023] Referring to FIG. 2, the emission control line driver 30 according to an embodiment of the present invention includes n stages 321 to 32 n in order to supply emission control signals to the n emission control lines E_1 to E_n . The stages 321 to 32 n are coupled (connected) to the emission control lines E_1 to E_n , respectively, and are driven by three clock signals CLK1, CLK2, and CLK3.

[0024] Each of the stages 321 to 32 n includes a first input terminal 33, a second input terminal 34, a third input terminal 35, and a fourth input terminal 36.

[0025] The first input terminal 33 of a k th (k is an odd or even number) stage 32 k receives the first clock signal CLK1 and the second input terminal 34 receives the second clock signal CLK2. The first input terminal 33 of a ($k+1$)th stage 32 $k+1$ receives the second clock signal CLK2, and the second input terminal 34 receives the first clock signal CLK1. The third clock signal CLK3 is supplied to the third input terminal 35 of each of the stages 321 to 32 n , and a start signal FLM or a sampling signal of a previous stage is supplied to the fourth input terminal 36.

[0026] The stages 321 to 32 n may be formed of the same circuit and generate the emission control signals having width that is changed to correspond to the start signal FLM.

[0027] FIG. 3 is a circuit diagram illustrating a first embodiment of one of the stages of FIG. 2. In FIG. 3, for convenience, the first stage 321 will be illustrated.

[0028] Referring to FIG. 3, the stage 321, according to the first embodiment of the present invention, includes a first transistor M1, a second transistor M2, a third transistor M3, a fourth transistor M4, a first capacitor C1, a second capacitor C2, a first controller 100, and a second controller 102.

[0029] The first transistor M1 is coupled between a first output terminal 37 and a first power source VDD. The gate electrode of the first transistor M1 is coupled to a first node N1. The first transistor M1 controls the voltage of the first output terminal 37 to correspond to the voltage applied to the first node N1. Here, when the first transistor M1 is turned on, the first power source VDD (e.g., a high voltage) is supplied to the first output terminal 37. Since the first output terminal 37 is coupled to the emission control line E_1 , the high voltage supplied to the first output terminal 37 is used as an emission control signal.

[0030] The second transistor M2 is coupled between the first output terminal 37 and a second power source VSS. The gate electrode of the second transistor M2 is coupled to a second node N2. The second transistor M2

controls the voltage of the first output terminal 37 to correspond to the voltage applied to the second node N2. Here, when the second transistor M2 is turned on, the second power source VSS (e.g., a low voltage) is supplied to the first output terminal 37.

[0031] The third transistor M3 is coupled between the fourth input terminal 36 and the first node N1. The gate electrode of the third transistor M3 is coupled to the first input terminal 33. The third transistor M3 is turned on or off to correspond to the first clock signal CLK1 supplied to the first input terminal 33. When the third transistor M3 is turned on, the fourth input terminal 36 and the first node N1 are electrically coupled to each other. When the start signal FLM (or a previous stage sampling signal) is supplied to the fourth input terminal 36, the first transistor M1 is turned on.

[0032] The fourth transistor M4 is coupled between the first power source VDD and the second node N2. The gate electrode of the fourth transistor M4 is coupled to the first node N1. The fourth transistor M4 is turned on or off to correspond to the voltage that is applied to the first node N1 in order to control the voltage of the second node N2. That is, the fourth transistor M4 is turned on when a low voltage is applied to the first node N1 in order to supply the voltage of the first power source VDD to the second node N2. When the low voltage is supplied to the first node N1, the high voltage of the first power source VDD is supplied to the second node N2 so that the first transistor M1 and the second transistor M2 are turned on or off at different times.

[0033] The first capacitor C1 is coupled between the second input terminal 34 and the second node N2. The first capacitor C1 controls the voltage of the second node N2 to correspond to the second clock signal CLK2 supplied to the second input terminal 34. The operation processes of the first capacitor C1 will be described later in more detail.

[0034] The second capacitor C2 is coupled between the first node N1 and the first power source VDD. The second capacitor C2 is charged with the voltage corresponding to the turning on or off of the first transistor M1.

[0035] A first controller 100 supplies a sampling signal to a second output terminal 38 to correspond to the first clock signal CLK1 and the second clock signal CLK2. Therefore, the first controller 100 includes a fifth transistor M5, a sixth transistor M6, a seventh transistor M7, a third capacitor C3, and a fourth capacitor C4.

[0036] The fifth transistor M5 is coupled between the fourth input terminal 36 and a third node N3. The gate electrode of the fifth transistor M5 is coupled to the first input terminal 33. The fifth transistor M5 is turned on or off to correspond to the first clock signal CLK1 supplied to the first input terminal 33 in order to control the voltage of the third node N3.

[0037] The sixth transistor M6 is coupled between a sixth node N6 and the second input terminal 34. The gate electrode of the sixth transistor M6 is coupled to the third node N3. The sixth transistor M6 controls the voltage of

the sixth node N6 to correspond to the voltage applied to the third node N3.

[0038] The seventh transistor M7 is coupled between the first power source VDD and the sixth node N6. The gate electrode of the seventh transistor M7 is coupled to the first output terminal 37. The seventh transistor M7 is turned on or off to correspond to the voltage applied to the first output terminal 37 in order to control the voltage of the sixth node N6.

[0039] The third capacitor C3 is coupled between the third node N3 and the sixth node N6. The third capacitor C3 is charged with the voltage corresponding to the turning on or turning off of the sixth transistor M6.

[0040] The fourth capacitor C4 is coupled between the first power source VDD and the first output terminal 37. The fourth capacitor C4 is charged with the voltage corresponding to the turning on or off of the seventh transistor M7.

[0041] In FIG. 3, the second output terminal 38 is coupled to the sixth node N6. The second output terminal 38 supplies the voltage applied to the sixth node N6 as a sampling signal to a next stage 322.

[0042] The second controller 102 controls the voltage of the second node N2 to correspond to the first clock signal CLK1 and the third clock signal CLK3. Here, in a period when the emission control signal is not supplied to the first output terminal 37, the second controller 102 maintains the voltage of the second node N2 as a low voltage. In FIG. 3, the second controller 102 includes an eighth transistor M8, a ninth transistor M9, a tenth transistor M10, an eleventh transistor M11, and a fifth capacitor C5.

[0043] The eighth transistor M8 is coupled between the first input terminal 33 and a fourth node N4. The gate electrode of the eighth transistor M8 is coupled to the first node N1. The eighth transistor M8 is turned on or off to correspond to the voltage applied to the first node N1 in order to control the voltage of the fourth node N4.

[0044] The ninth transistor M9 is coupled between the fourth node N4 and the second power source VSS. The gate electrode of the ninth transistor M9 is coupled to the first input terminal 33. The ninth transistor M9 is turned on or off to correspond to the first clock signal CLK1 supplied to the first input terminal 33 in order to control the voltage of the fourth node N4.

[0045] The tenth transistor M10 is coupled between the second node N2 and a fifth node N5. The gate electrode of the tenth transistor M10 is coupled to a third input terminal 35. The tenth transistor M10 is turned on or off to correspond to the third clock signal CLK3 supplied to the third input terminal 35 in order to control the voltage of the second node N2.

[0046] The eleventh transistor M11 is coupled between the fifth node N5 and the third input terminal 35. The gate electrode of the eleventh transistor M11 is coupled to the fourth node N4. The eleventh transistor M11 is turned on or off to correspond to the voltage applied to the fourth node N4 in order to control the voltage of

the fifth node N5.

[0047] The fifth capacitor C5 is coupled between the fourth node N4 and the fifth node N5. The fifth capacitor C5 is charged with the voltage corresponding to the turning on or off of the eleventh transistor M11.

[0048] FIG. 4 is a waveform chart illustrating the operation processes of the stage of FIG. 3.

[0049] Referring to FIG. 4, the first clock signal CLK1 and the second clock signal CLK2 are supplied in the period of iH (i is a natural number, e.g., a horizontal period), and the third clock signal CLK3 is supplied in the period of $i/2H$. In FIG. 4, for convenience sake, the first clock signal CLK1 and the second clock signal CLK2 are set in the period of $2H$ and the third clock signal CLK3 is set in the period of $1H$.

[0050] In FIG. 4, the first clock signal CLK1 and the second clock signal CLK2 are supplied in different horizontal periods H , and the third clock signal CLK3 is supplied every horizontal period H so that the first clock signal CLK1 does not overlap the third clock signal CLK3. Then, in the horizontal period H , after the first clock signal CLK1 or the second clock signal CLK2 is supplied, the third clock signal CLK3 is supplied. That is, in an exemplary horizontal period, the third clock signal CLK3 is supplied after the first clock signal CLK1 is supplied. In the next horizontal period, the third clock signal CLK3 is supplied after the second clock signal CLK2 is supplied.

[0051] Operation processes will be described in more detail as follows. First, the start signal FLM (e.g., the low signal) is supplied to the fourth input terminal 36. After the start signal FLM is supplied to the fourth input terminal 36, the first clock signal CLK1 is supplied to the first input terminal 33. When the first clock signal CLK1 is supplied, the third transistor M3, the fifth transistor M5, and the ninth transistor M9 are turned on.

[0052] When the third transistor M3 is turned on, the start signal FLM is supplied to the first node N1. When the start signal FLM is supplied to the first node N1, the first transistor M1, the fourth transistor M4, and the eighth transistor M8 are turned on. When the first transistor M1 is turned on, the voltage corresponding to the turning on of the first transistor M1 is charged at the second capacitor C2.

[0053] When the first transistor M1 is turned on, the voltage of the first power source VDD is supplied to the first output terminal 37. In this case, the emission control signal is supplied to the emission control line E1.

[0054] When the fourth transistor M4 is turned on, the first power source VDD is supplied to the second node N2. When the first power source VDD is supplied to the second node N2, the second transistor M2 is turned off. When the second transistor M2 is turned off, the first power source VDD may be stably supplied to the first output terminal 37.

[0055] When the eighth transistor M8 is turned on, the fourth node N4 and the first input terminal 33 are electrically coupled to each other. Here, since the first clock signal CLK1 is supplied to the first input terminal 33, the

fourth node N4 receives a low voltage.

[0056] When the fifth transistor M5 is turned on, the start signal is supplied to the third node N3. When the start signal is supplied to the third node N3, the sixth transistor M6 is turned on. When the sixth transistor M6 is turned on, the sixth node N6 and the second input terminal 34 are electrically coupled to each other. Here, since the second clock signal CLK2 is not supplied to the second input terminal 34, the sixth node N6 maintains a high voltage so that a sampling signal is not supplied to the second output terminal 38. On the other hand, since the sixth transistor M6 is turned on, the voltage corresponding to the turning on of the sixth transistor M6 is charged at the third capacitor C3.

[0057] When the ninth transistor M9 is turned on, the voltage of the second power source VSS is supplied to the fourth node N4. When the second power source VSS is supplied to the fourth node N4, the eleventh transistor M11 is turned on. When the eleventh transistor M11 is turned on, the fifth node N5 and the third input terminal 35 are electrically coupled to each other. Here, since the third clock signal CLK3 is not supplied to the third input terminal 35, the fifth node N5 maintains a high voltage. On the other hand, since the eleventh transistor M11 is turned on, the voltage corresponding to the turning on of the eleventh transistor is charged at the fifth capacitor C5.

[0058] Then, the supply of the first clock signal CLK1 to the first input terminal 33 is stopped. When the supply of the first clock signal CLK1 is stopped, the third transistor M3, the fifth transistor M5, and the ninth transistor M9 are turned off.

[0059] When the third transistor M3 is turned off, the fourth input terminal 36 and the first node N1 are electrically isolated from each other. Here, the first node N1 maintains a low voltage by the second capacitor C2. Therefore, the first transistor M1 maintains a turn on state so that the voltage of the first power source VDD is output to the first output terminal 37. Since the fourth transistor M4 maintains a turn on state by the voltage of the second capacitor C2, the second transistor M2 stably maintains a turn off state.

[0060] When the fifth transistor M5 is turned off, the fourth input terminal 36 and the third node N3 are electrically isolated from each other. Here, the sixth transistor M6 maintains a turn on state to correspond to the voltage charged at the third capacitor C3 so that the second output terminal 38 maintains a previous voltage.

[0061] When the ninth transistor M9 is turned off, the fourth node N4 and the second power source VSS are electrically isolated from each other. Here, since the eighth transistor M8 maintains a turned on state to correspond to the voltage applied to the first node N1, the fourth node N4 and the first input terminal 33 are electrically coupled to each other. Therefore, the voltage of the fourth node N4 increases to the voltage supplied to the first input terminal 33 (e.g., the voltage of a high signal). When the fourth node N4 receives the voltage of the high signal, the eleventh transistor M11 is turned off. Here,

the fifth capacitor C5 is charged with the voltage corresponding to the turning off of the eleventh transistor M11.

[0062] Then, the third clock signal CLK3 is supplied to the third input terminal 35. When the third clock signal CLK3 is supplied, the tenth transistor M10 is turned on. When the tenth transistor M10 is turned on, the second node N2 and the fifth node N5 are electrically coupled to each other. At this time, since the fourth transistor M4 maintains a turned on state and the eleventh transistor M11 maintains a turned off state, the second node N2 maintains the voltage of the first power source VDD.

[0063] After the third clock signal CLK3 is supplied, the second clock signal CLK2 is supplied to the second input terminal 34 in the next horizontal period. Here, since the sixth transistor M6 is set in a turn on state, the second clock signal CLK2 is supplied to the sixth node N6. The second clock signal CLK2 supplied to the sixth node N6 as a sampling signal is supplied to the next stage via the second output terminal 38. On the other hand, when the second clock signal CLK2 is supplied to the sixth node N6, the voltage of the third node N3 is reduced by the coupling of the third capacitor C3. Therefore, the sixth transistor M6 stably maintains a turned on state.

[0064] Additionally, the second clock signal CLK2 supplied to the second input terminal 34 is transmitted to the second node N2 by the coupling of the first capacitor C1. Here, since the second node N2 receives the first power source VDD, the voltage of the first power source VDD is maintained without a change in a voltage.

[0065] Then, the third clock signal CLK3 is supplied to the third input terminal 35. When the third clock signal CLK3 is supplied, the tenth transistor M10 is turned on. When the tenth transistor M10 is turned on, the second node N2 and the fifth node N5 are electrically coupled to each other. Here, since the fourth transistor M4 maintains a turned on state and the eleventh transistor M11 maintains a turned off state, the second node N2 maintains the voltage of the first power source VDD. After the third clock signal CLK3 is supplied, the supply of the start signal FLM is stopped (e.g., a high voltage) in the next horizontal period, and the first clock signal CLK1 is supplied to the first input terminal 33.

[0066] When the first clock signal CLK1 is supplied, the third transistor M3, the fifth transistor M5, and the ninth transistor M9 are turned on.

[0067] When the third transistor M3 is turned on, the first node N1 and the fourth input terminal 36 are electrically coupled to each other. Here, since a high voltage is supplied to the first node N1, the first transistor M1, the fourth transistor M4, and the eighth transistor M8 are turned off. When the first transistor M1 is turned off, the first output terminal 37 is set in a floating state. In this case, the first output terminal 37 maintains the high voltage that is an output signal of a previous period.

[0068] Since the emission control signal supplied to the emission control line E1 is supplied to the pixels 50, charging is performed by the capacitors of the pixels. Therefore, although the first output terminal 37 is set in

a floating state, the output voltage of a previous period is maintained by the parasitic capacitors of the pixels 50 and the emission control line.

[0069] When the fifth transistor M5 is turned on, a high voltage is supplied to the third node N3 so that the sixth transistor M6 is turned off. When the sixth transistor M6 is turned off, the sixth node N6 and the second input terminal 34 are electrically isolated from each other. Here, the third capacitor C3 is charged with the voltage corresponding to the turning off of the sixth transistor M6.

[0070] When the ninth transistor M9 is turned on, the fourth node N4 and the second power source VSS are electrically coupled to each other. Here, the fourth node N4 receives the voltage of the second power source VSS so that the eleventh transistor M11 is turned on. When the eleventh transistor M11 is turned on, the fifth node N5 and the third input terminal 35 are electrically coupled to each other. On the other hand, the voltage corresponding to the turning on of the eleventh transistor M11 is stored at the fifth capacitor C5.

[0071] Then, the third clock signal CLK3 is supplied to the third input terminal 35. When the third clock signal CLK3 is supplied, the tenth transistor M10 is turned on. When the tenth transistor M10 is turned on, the second node N2 and the third input terminal 35 are electrically coupled to each other via the fifth node N5. Here, the third clock signal CLK3 (e.g., a low voltage) is supplied to the second node N2. When the low voltage is supplied to the second node N2, the second transistor M2 is turned on so that the voltage of the second power source VSS is output to the first output terminal 37. In this case, the supply of the emission control signal to the emission control line E1 is stopped. When the second power source VSS is supplied to the first output terminal 37, the seventh transistor M7 is turned on. When the seventh transistor M7 is turned on, the voltage of the first power source VDD is supplied to the sixth node N6.

[0072] According to an embodiment of the present invention, the third clock signal CLK3 may be set as a voltage lower than the second power source VSS so that the second transistor M2 may be stably turned on. Then, the stage 321 outputs the voltage of the first power source VDD to the first output terminal 37 until the next start signal FLM is supplied.

[0073] Additionally, according to embodiments of the present invention, whenever the second clock signal CLK2 is supplied, the voltage of the second node N2 is reduced by the coupling of the first capacitor C1. Therefore, the voltage of the second node N2 stably maintains a low voltage so that the voltage of the second power source VSS may be stably output to the first output terminal 37.

[0074] On the other hand, a sampling signal is supplied to the next stage in synchronization with the second clock signal CLK2 (In the next stage, the second clock signal CLK2 is supplied to the first input terminal). In this case, the next stage stably outputs the emission control signal using the sampling signal. Additionally, in FIG. 4, it is

illustrated that one sampling signal is generated to correspond to the start signal FLM. However, the present invention is not limited to the above. For example, when the start signal FLM overlaps two first clock signals CLK1, two sampling signals are supplied to the next stage. Therefore, according to embodiments of the present invention, the width of the start signal FLM is controlled so that the width of the emission control signal may be freely controlled.

[0075] FIG. 5 is a circuit diagram illustrating a second embodiment of the stage of FIG. 2. In FIG. 5, the same elements as those of FIG. 3 are denoted by the same reference numerals and detailed description thereof will be omitted.

[0076] Referring to FIG. 5, the stage 321, according to the second embodiment of the present invention, further includes a twelfth transistor M12 and a thirteenth transistor M13 for bidirectional driving.

[0077] The twelfth transistor M12 is coupled between the fourth input terminal 36 and the third transistor M3. The gate electrode of the twelfth transistor M12 receives a first control signal CS1. The twelfth transistor M12 is turned on when the first control signal CS1 is supplied.

[0078] The thirteenth transistor M13 is coupled between a fifth input terminal 39 and the fifth transistor M5 (or a first controller 100). Then, the gate electrode of the thirteenth transistor M13 receives a second control signal CS2. The thirteenth transistor M13 is turned on when the second control signal CS2 is supplied. The fifth input terminal 39 receives the start signal or the sampling signal of the next stage.

[0079] Here, the first control signal CS1 and the second control signal CS2 are supplied at different times (e.g., not overlapped with each other). For example, when the emission control signals are supplied in a first direction (from top to bottom of a panel), the first control signal CS1 is supplied so that the twelfth transistor M12 is turned on and so that the thirteenth transistor M13 maintains a turned off state. When the emission control signals are supplied in a second direction (from bottom to top of the panel), the second control signal CS2 is supplied so that the thirteenth transistor M13 is turned on and so that the twelfth transistor M12 maintains a turned off state.

[0080] The stage 321, according to the second embodiment of the present invention, further includes the twelfth transistor M12 and the thirteenth transistor M13 for bidirectional driving, and the operation processes are substantially the same as the first embodiment illustrated in FIG. 3.

[0081] FIG. 6 is a circuit diagram illustrating a third embodiment of the stage of FIG. 2. In FIG. 6, the same elements as those of FIG. 3 are denoted by the same reference numerals, and detailed description thereof will be omitted.

[0082] Referring to FIG. 6, the stage 321, according to the third embodiment of the present invention, further includes a fourteenth transistor M14 coupled between

the first node N1 and the second power source VSS. The fourteenth transistor M14 is turned on to supply the voltage of the second power source VSS to the first node N1 when a reset signal (Reset) is supplied to the gate of the fourteenth transistor M14. When the second power source VSS is supplied to the first node N1, the first transistor M1 is turned on so that the voltage of the first power source VDD is supplied to the first output terminal 37.

[0083] Here, the reset signal (Reset) is commonly supplied to all of the stages 321 to 32n when a power source is turned on and/or off. As described above, when the reset signal (Reset) is supplied and the power source is turned on and/or off, the emission control signals are supplied to the emission control lines E1 to En so that the pixels 50 are set in a non-emission state. That is, according to the third embodiment of the present invention, it is possible to prevent over-current from flowing or unnecessary light from being generated when the power source is turned on and/or off using the reset signal.

[0084] Additionally, in FIG. 2, the third clock signal CLK3 is supplied to all of the stages 321 to 32n. However, the present invention is not limited to the above. For example, the third clock signal CLK3 may be supplied to even and odd stages via different lines. Then, the load of the third clock signal CLK3 is minimized or reduced so that the stability of driving the stages may be improved.

[0085] Although the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

Claims

1. An emission control line driver comprising a plurality of stages, wherein each of the stages comprises:

a first transistor coupled between a first output terminal and a first power source, the first transistor being configured to be turned on or off to correspond to a voltage applied to a first node that is coupled to a gate electrode of the first transistor;

a second transistor coupled between the first output terminal and a second power source that outputs a voltage that is lower than the first power source, the second transistor being configured to be turned on or off to correspond to a voltage applied to a second node that is coupled to a gate electrode of the second transistor;

a third transistor coupled between a fourth input terminal and the first node, and having a gate electrode coupled to a first input terminal;

a fourth transistor coupled between the first power source and the second node, and having a

gate electrode coupled to the first node;
a first controller coupled to the first input terminal and a second input terminal to supply a sampling signal to a second output terminal;
a second controller coupled to the first input terminal and a third input terminal to control the voltage of the second node; and
a first capacitor coupled between the second input terminal and the second node.

2. The emission control line driver as claimed in claim 1, further comprising a second capacitor coupled between the first node and the first power source.

3. The emission control line driver as claimed in claim 1 or 2, wherein the first input terminal is configured to receive a first clock signal, wherein the second input terminal is configured to receive a second clock signal, wherein the third input terminal is configured to receive a third clock signal, and wherein the fourth input terminal is configured to receive a start signal or a sampling signal of a previous stage.

4. The emission control line driver as claimed in claim 3, wherein the first clock signal, the second clock signal, and the third clock signal do not overlap each other.

5. The emission control line driver as claimed in claim 3, wherein each of the first clock signal and the second clock signal are set in a period of i horizontal periods, and wherein the third clock signal is set in a period of $i/2$ horizontal periods, and/or wherein the third clock signal is supplied in a horizontal period after the first clock signal or the second clock signal is supplied in the horizontal period.

6. The emission control line driver as claimed in any one of the preceding claims, wherein the first controller comprises:

a fifth transistor coupled between the fourth input terminal and a third node, and having a gate electrode coupled to the first input terminal;

a sixth transistor coupled between a sixth node and the second input terminal, and having a gate electrode coupled to the third node;

a seventh transistor coupled between the sixth node and the first power source, and having a gate electrode coupled to the first output terminal;

a third capacitor coupled between the third node and the sixth node; and

a fourth capacitor coupled between the first out-

- put terminal and the first power source, wherein the second output terminal may be coupled to the sixth node.
7. The emission control line driver as claimed in any one of the preceding claims, wherein the second controller comprises:
- an eighth transistor coupled between the first input terminal and a fourth node, and having a gate electrode coupled to the first node;
- a ninth transistor coupled between the fourth node and the second power source, and having a gate electrode coupled to the first input terminal;
- a tenth transistor coupled between the second node and a fifth node, and having a gate electrode coupled to the third input terminal;
- an eleventh transistor coupled between the fifth node and the third input terminal, and having a gate electrode coupled to the fourth node; and
- a fifth capacitor coupled between the fourth node and the fifth node.
8. The emission control line driver as claimed in any one of the preceding claims, further comprising:
- a twelfth transistor coupled between the fourth input terminal and the third transistor, the twelfth transistor being configured to be turned on when a first control signal is supplied to a gate electrode of the twelfth transistor; and
- a thirteenth transistor coupled between a fifth input terminal and the first controller, the thirteenth transistor being configured to be turned on when a second control signal is supplied to a gate electrode of the thirteenth transistor.
9. The emission control line driver as claimed in claim 8, wherein the first control signal and the second control signal do not overlap each other.
10. The emission control line driver as claimed in claim 8 or 9, wherein the fifth input terminal is configured to receive a start signal or a sampling signal of a next stage.
11. The emission control line driver as claimed in any one of the preceding claims, further comprising a fourteenth transistor coupled between the first node and the second power source, the fourteenth transistor being configured to be turned on when a reset signal is supplied to a gate electrode of the fourteenth transistor.
12. The emission control line driver as claimed in claim 11, wherein the reset signal is commonly supplied to all of the stages.
13. An organic light emitting display comprising:
- a scan driver for sequentially supplying scan signals to scan lines;
- a data driver for supplying data signals to data lines;
- an emission control line driver according to any one of the preceding claims for supplying emission control signals to emission control lines; and
- pixels positioned at crossing regions of the scan lines, the data lines, and the emission control lines.
14. The organic light emitting display as claimed in claim 13, wherein the first input terminal of an i^{th} stage of the stages is configured to receive a first clock signal, wherein the second input terminal of the i^{th} stage is configured to receive a second clock signal, wherein the third input terminal of the i^{th} stage is configured to receive a third clock signal, and wherein the fourth input terminal of the i^{th} stage is configured to receive a start signal or a sampling signal of a previous stage.
15. The organic light emitting display as claimed in claim 14, wherein the first input terminal of an $(i+1)^{\text{th}}$ stage of the stages is configured to receive the second clock signal, wherein the second input terminal of the $(i+1)^{\text{th}}$ stage is configured to receive the first clock signal, wherein the third input terminal of the $(i+1)^{\text{th}}$ stage is configured to receive the third clock signal, and wherein the fourth input terminal of the $(i+1)^{\text{th}}$ stage is configured to receive the start signal or the sampling signal of a previous stage, wherein the third clock signal supplied to the i^{th} stage and the $(i+1)^{\text{th}}$ stage may be supplied via different transmission lines.

FIG. 1

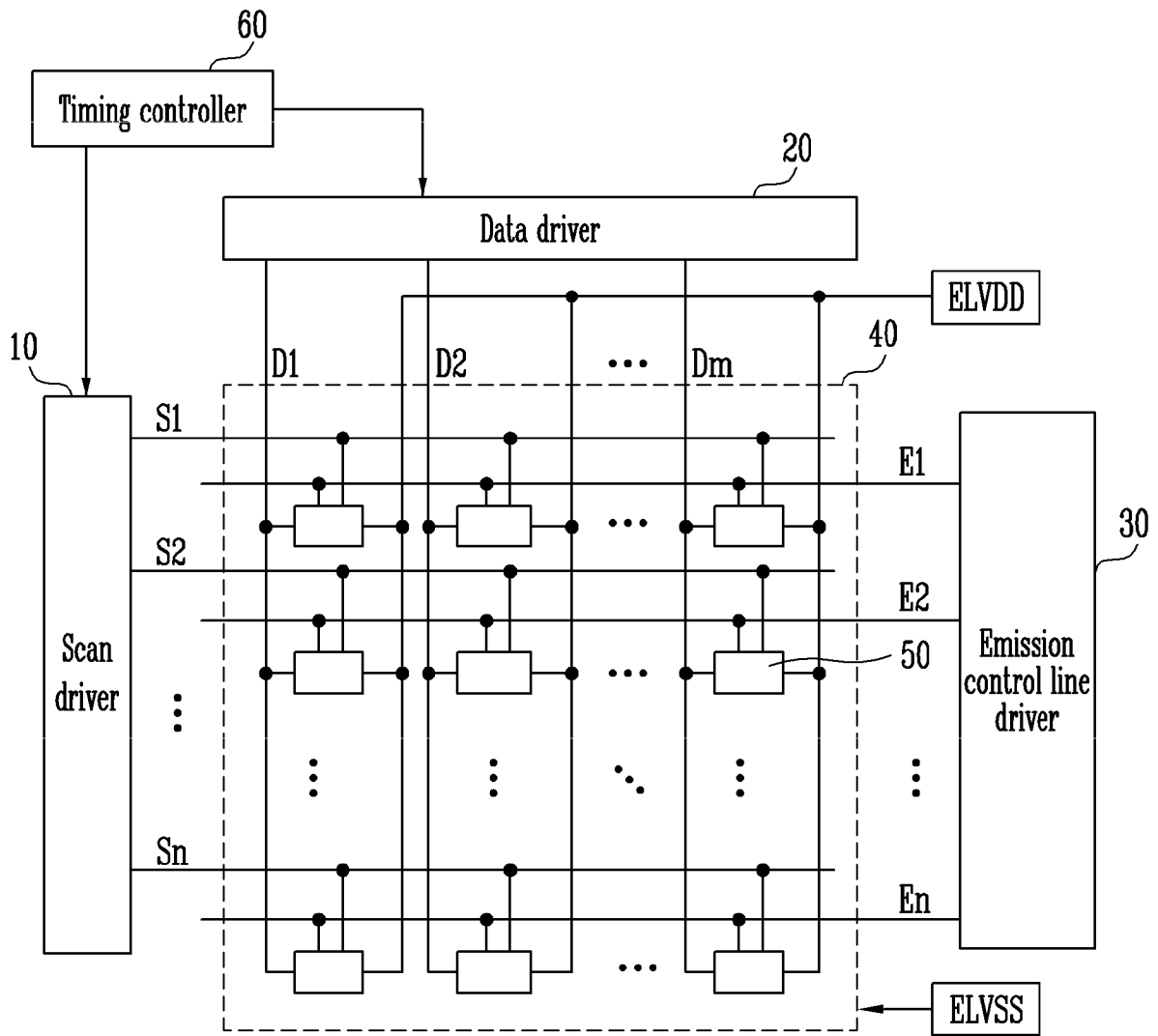


FIG. 2

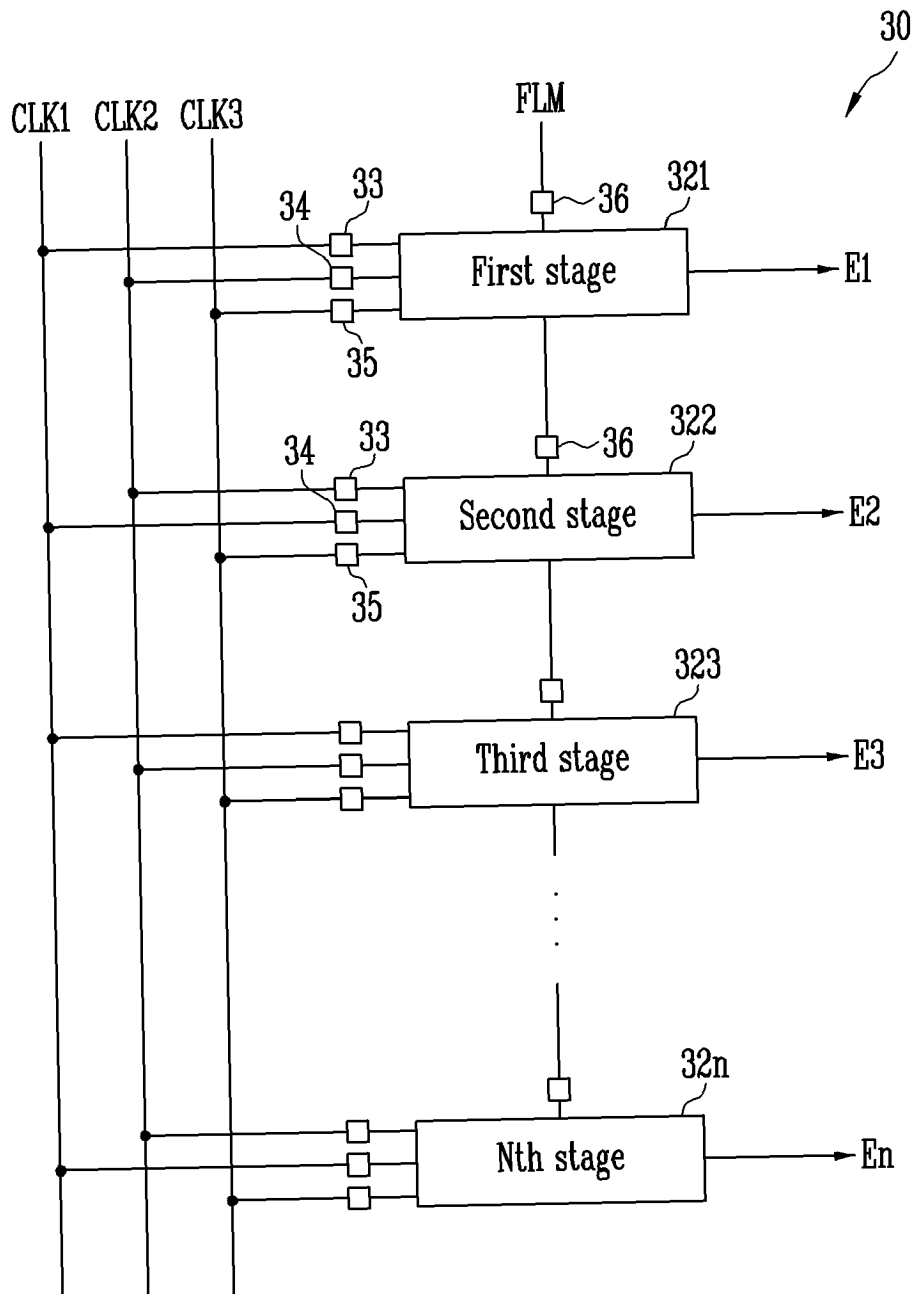


FIG. 3

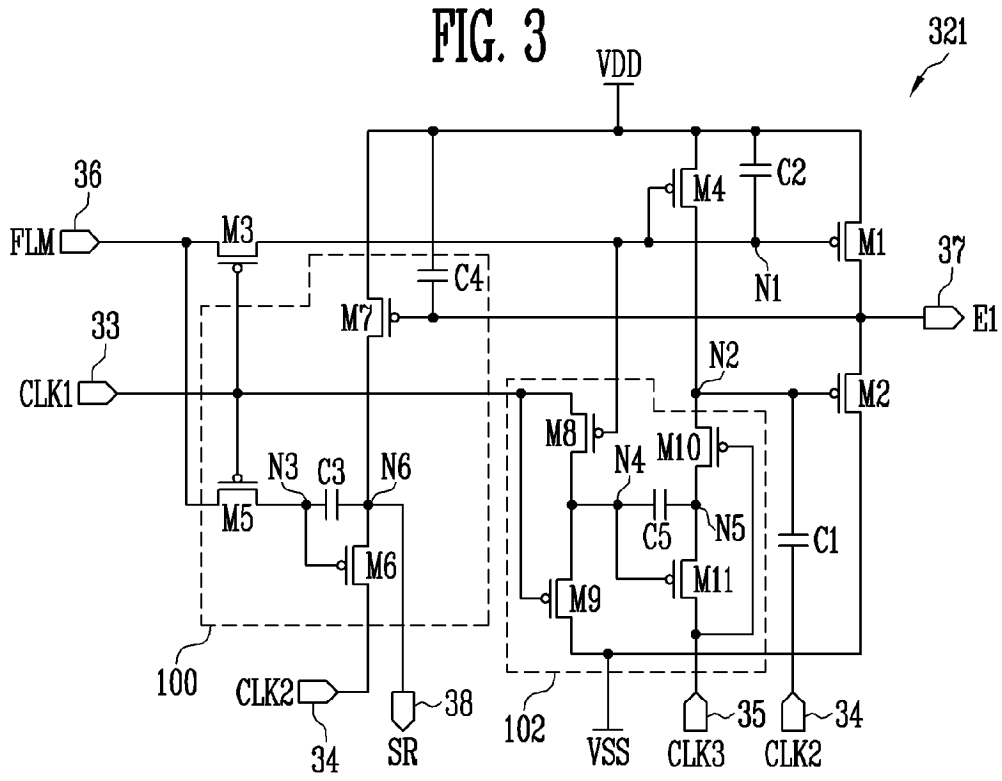


FIG. 4

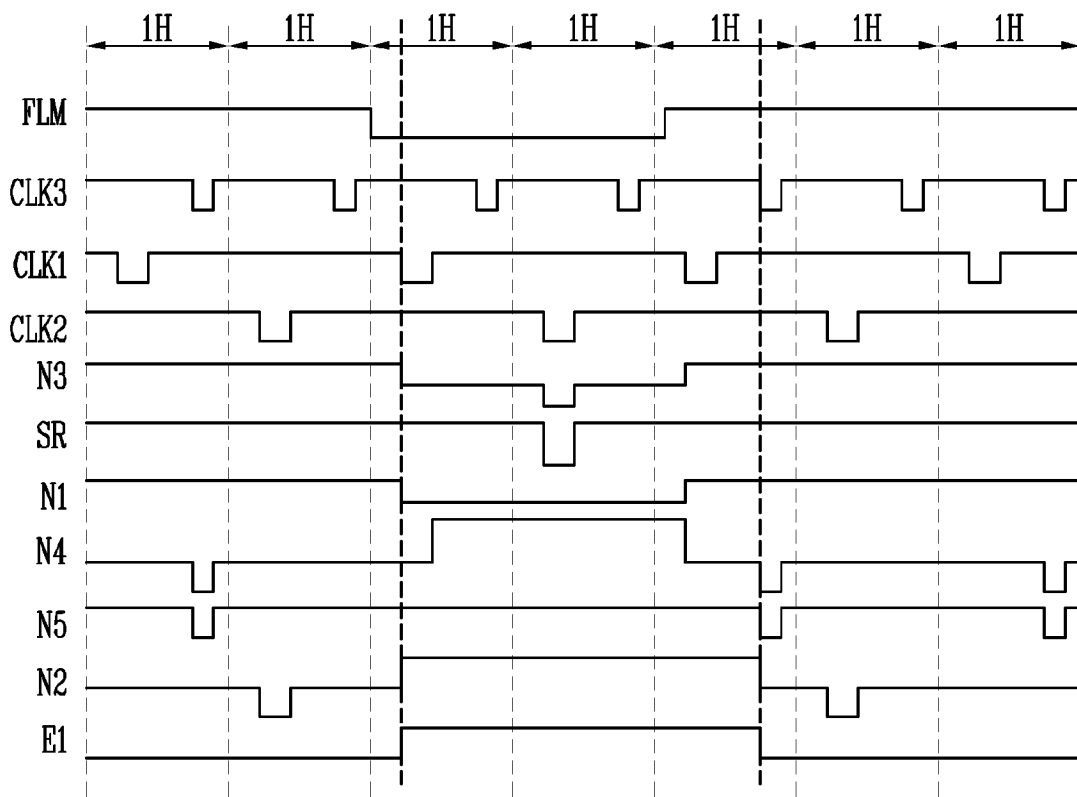


FIG. 5

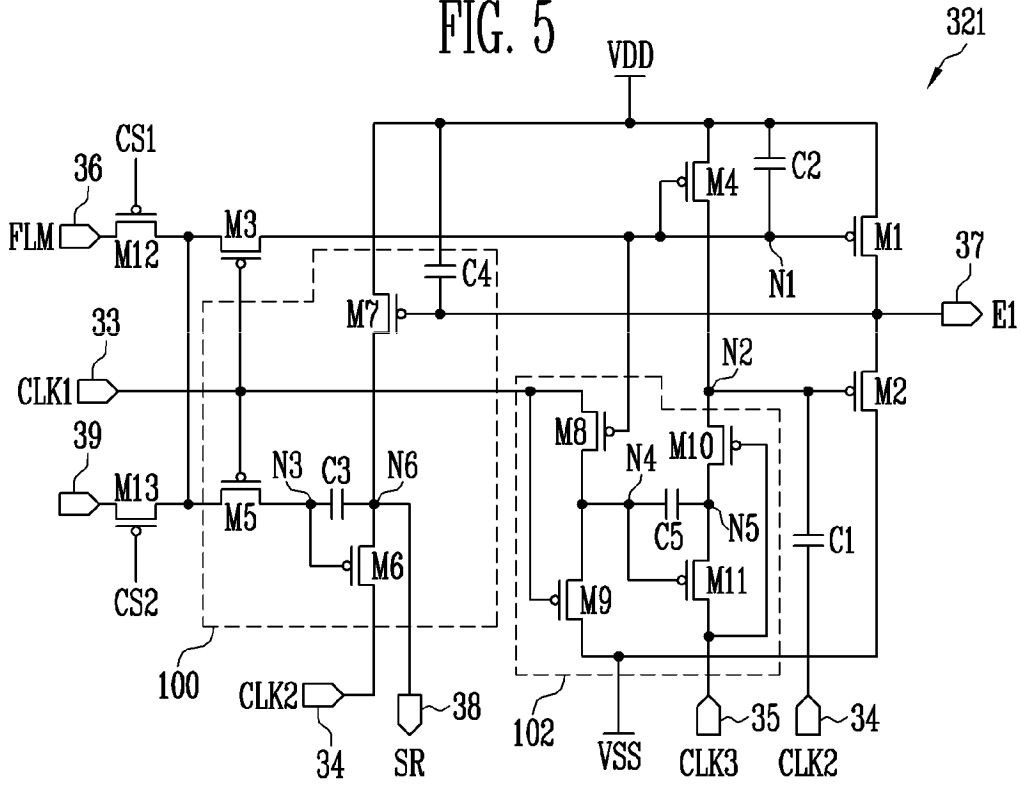
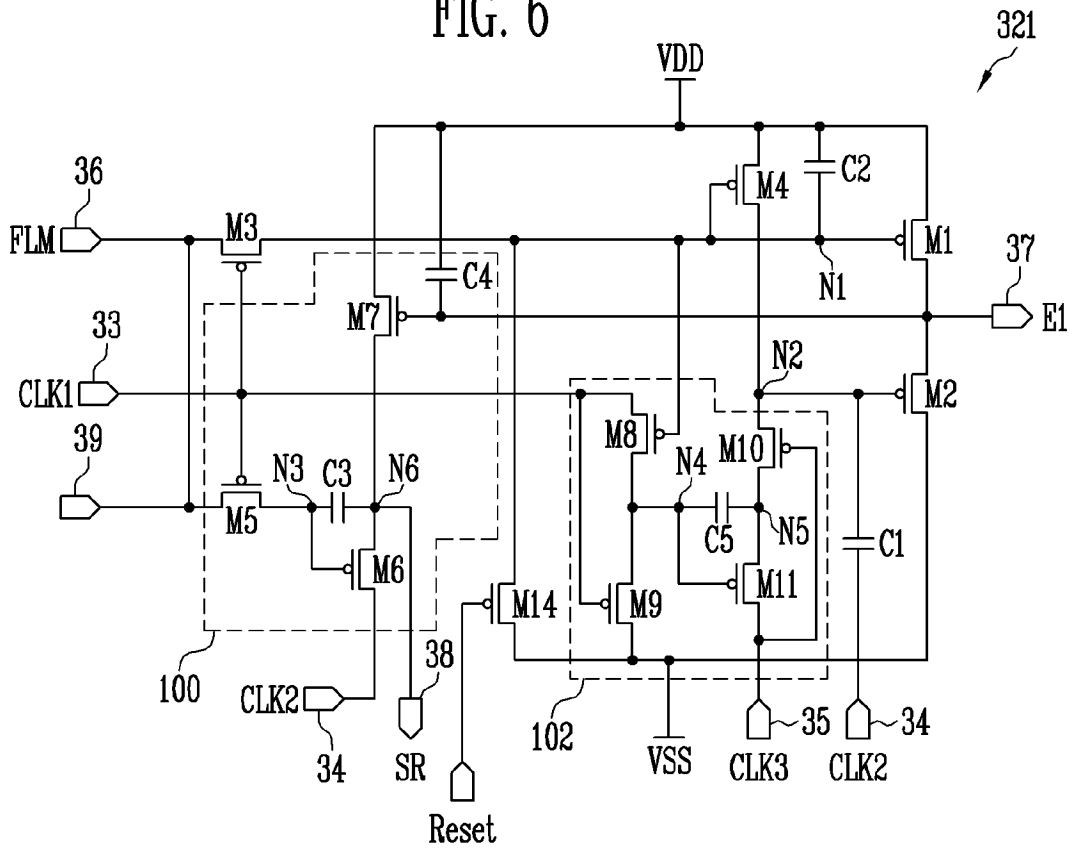


FIG. 6





EUROPEAN SEARCH REPORT

Application Number
EP 11 19 3980

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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A	US 2007/262935 A1 (SHIN DONG YONG [KR]) 15 November 2007 (2007-11-15) * figures 10,13-15 * -----	1-15	
A	US 2010/188316 A1 (JANG HWAN-SOO [KR]) 29 July 2010 (2010-07-29) * the whole document * -----	1-15	
			TECHNICAL FIELDS SEARCHED (IPC)
			G09G G11C
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 27 March 2012	Examiner Demin, Stefan
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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EPO FORM 1503 03 82 (P04G01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 11 19 3980

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27-03-2012

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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	发射控制线驱动器和使用其的有机发光显示器		
公开(公告)号	EP2474969A1	公开(公告)日	2012-07-11
申请号	EP2011193980	申请日	2011-12-16
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星DISPLAY CO., LTD.		
[标]发明人	JANG HWAN SOO PYON CHANG SOO		
发明人	JANG, HWAN-SOO PYON, CHANG-SOO		
IPC分类号	G09G3/32 G11C19/28 G09G3/3266 G11C19/18		
CPC分类号	G09G3/3266 G09G2300/0861 G09G2310/0262 G09G2310/0283 G09G2310/0286 G09G2330/025 G09G2330/027 G11C19/184 G11C19/28		
优先权	1020110001419 2011-01-06 KR		
其他公开文献	EP2474969B1		
外部链接	Espacenet		

摘要(译)

发射控制线驱动器能够确保输出的稳定性并且能够自由地控制发射控制信号的宽度。发射控制线驱动器包括分别耦合到发射控制线 (E1) 的多个级 (321)。每个级包括多个晶体管 (M1-M14)，其被配置为输出发射控制信号。可以控制发射控制信号的宽度以对应于开始信号的宽度。此外，简化了级的电路结构。

