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(54) **Method and system for programming, calibrating and driving a light emitting device display**

Verfahren und System zur Programmierung, Kalibrierung und Ansteuerung einer lichtemittierenden Vorrichtungsanzeige

Procédé et système pour programmer, étalonner et commander un affichage de dispositif électroluminescent

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(56) References cited:
EP-A1- 1 450 341
WO-A2-2004/047058
KR-A- 20040 100 887
US-A1- 2003 122 813

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Description

FIELD OF INVENTION

[0001] The present invention relates to display technologies, more specifically a method and system for programming, calibrating and driving a light emitting device display.

BACKGROUND OF THE INVENTION

[0002] Recently active-matrix organic light-emitting diode (AMOLED) displays with amorphous silicon (a-Si), poly-silicon, organic, or other driving backplane have become more attractive due to advantages over active matrix liquid crystal displays. For example, the advantages include: with a-Si besides its low temperature fabrication that broadens the use of different substrates and makes feasible flexible displays, its low cost fabrication, high resolution, and a wide viewing angle.

[0003] An AMOLED display includes an array of rows and columns of pixels, each having an organic light-emitting diode (OLED) and backplane electronics arranged in the array of rows and columns. Since the OLED is a current driven device, the pixel circuit of the AMOLED should be capable of providing an accurate and constant drive current.

[0004] U.S. patent No. 6,594, 606 discloses a method and system for calibrating passive pixels. U.S. patent No. 6,594, 606 measures data line voltage and uses the measurement for pre-charge. However, this technique does not provide the accuracy needed for active matrix, since the active matrix calibration should work for both backplane aging and OLED aging. Further, after pre-charge, current programming must be performed. Current-programming of current driven pixels is slow due to parasitic line capacitances and suffers from non-uniformity for large displays. The speed may be an issue when programming with small currents.

[0005] US 2004/0257353 A1 describes an electro-optical device having circuits for driving electro-optical elements, such as organic EL elements, and a driving device, which can employ driving elements having low driving ability, such as α-TFTs. By providing a charge storage capacitor between the source electrode and the gate electrode of a driving transistor which is between power sources, the electro-optical device can allow the driving transistor to control a driving current, even when an electro-optical element is connected to the source side of the driving transistor. In addition, driving data can be stored in the charge storage capacitor by applying a predetermined voltage to the source electrode of the driving transistor.

[0006] WO 2004/047058 A2 relates to a method of improving the output uniformity of a display device, such as a self light emitting display device, comprising the following steps; detecting a first emitted brightness of at least one pixel of said display device; by means of the detected first brightness, determining the non-uniformity of an output of a driver circuit being connected with said at least one pixel; and based on said first detected brightness, generating a calibration factor for the at least one pixel, to be used to modify the output of the driver circuit, in order to improve the uniformity.

[0007] Other compensation techniques have been introduced. However, there is still a need to provide a method and system which is capable of providing constant brightness, achieving high accuracy and reducing the effect of the aging of the pixel circuit.

SUMMARY OF THE INVENTION

[0008] It is an object of the invention to provide e method and system that obviates or mitigates at least one of the disadvantages of existing systems.

[0009] This object is solved by the present invention as claimed in the independent claims. Advantageous embodiments of the present invention are defined by the dependent claims.

[0010] In accordance with an illustrative example for understanding of the present invention there is provided a method of real-time calibration for a display array having a plurality of pixel circuits arranged in row and column, including the steps of: generating a priority list of pixels, which is used to prioritize pixels for calibration based on display and previous calibration data, the priority list being used to select one or more (n) pixels which are programmed with currents higher than a threshold current for calibration; selecting n pixels in a selected column of the display array from the linked list; implementing programming to the pixels in the selected column, including: monitoring a pixel current for the n pixels and obtaining calibration data; updating a compensation memory based on the calibration data for calibration; sorting the priority list for the next programming.

[0011] In accordance with a further illustrative example for understanding the present invention there is provided a system for real-time calibration for a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having a light emitting device and a driving transistor, the system including: a calibration scheduler for controlling programming and calibration of the display array, including: a priority list for listing one or more pixels for calibration based on display data; module for enabling, during a programming cycle, calibration mode for one or more pixels in the selected column, which are selected from the priority list, and during a progamming cycle, enabling normal operation mode for the rest of the pixels in the selected column; a monitor for monitoring a pixel current for the pixels in the calibration mode through the selected column; a generator for generating a calibration data based on the monitoring result; a memory for storing calibration data; and an adjuster for adjusting a programming data applied to the display array based on the calibration data when the pixel on the normal operation mode is programmed.

[0012] In accordance with a further illustrative example for understanding the present invention there is provided a system for a display array having a pixel circuit, the pixel circuit being programmed through a data line, the system including: a data source for providing a programming data into the pixel circuit; a current-controlled voltage source associated with the voltage source for converting a current on the data line to a voltage associated with the current to extract a time dependent parameter of the pixel circuit.

[0013] In accordance with a further illustrative example for understanding the present invention there is provided a system for a display array including a plurality of pixel circuits, each pixel circuit including a driving transistor, at least one switch transistor, a storage capacitor and a light emitting device, the system including: a monitor for monitoring a current or voltage on the pixel circuit; a data process unit for controlling the operation of the display array, the data process unit extracting information on an aging of the pixel circuit, based on the monitored current or voltage and determining a state of the pixel circuit; a driver controlled by the data process unit and for providing programming and calibration data to the pixel circuit, based on the state of the pixel circuit.

[0014] In accordance with a further illustrative example for understanding the present invention there is provided a method of driving a display array, the display array including a plurality of pixel circuits, each pixel circuit including a driving transistor, at least one switch transistor, a storage capacitor and a light emitting device, the method including the steps of: applying a current or voltage to the pixel circuit; monitoring a current or voltage flowing through the pixel circuit; extracting information on an aging of the pixel circuit, based on the monitored current or voltage and determining the state of the pixel circuit; providing operation voltage to the pixel circuit, including determining programming and calibration data for the pixel circuit based on the state of the pixel circuit.

[0015] In accordance with a further illustrative example for understanding the present invention there is provided a method of driving a display array, the display array including a plurality of pixel circuits, each pixel circuit including a driving transistor, at least one switch transistor, a storage capacitor and a light emitting device, the method including the steps of: applying a current or voltage to the light emitting device; monitoring a current or voltage flowing through the light emitting device; predicting a shift in the voltage of the light emitting device, based on the monitored current or voltage and determining the state of the pixel circuit; and providing, to the light emitting device, a bias associated with the shift in the voltage of the light emitting device.

[0016] In accordance with a further illustrative example for understanding the present invention there is provided a system for driving a display array, the display array including a plurality of pixel circuits, each pixel circuit including a driving transistor, at least one switch transistor, a storage capacitor and a light emitting device, the system including: a monitor for monitoring a current or voltage on the pixel circuit; a data process unit for predicting a shift in the voltage of the light emitting device, based on the monitored current or voltage and determining the state of the pixel circuit; and a circuit for providing, to the light emitting device, a bias associated with the shift in the voltage of the light emitting device.

[0017] In accordance with an illustrative example for understanding the present invention there is provided a system for a display array including a plurality of pixel circuits, each pixel circuit having a driving transistor, at least one switch transistor, a storage capacitor and a light emitting device, the light emitting device being located at a programming path for programming the pixel circuit, the system including: a controller for controlling the operation of the display array; a driver for providing operation voltage to the pixel circuit based on the control of the controller; and the driver providing the operation voltage to the pixel circuit during a programming cycle such that the light emitting device being removed from the programming path.

[0018] This summary of the invention does not necessarily describe all features of the invention.

[0019] Other aspects and features of the present invention will be readily apparent to those skilled in the art from a review of the following detailed description of preferred embodiments in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

Figure 1 is a flow chart showing a process for calibration-scheduling in accordance with an embodiment of the present invention;

Figure 2 is a diagram showing an example of a system structure for implementing the calibration-scheduling of Figure 1;

Figure 3 is a diagram showing a system architecture for a voltage-extracting, programming and driving in accordance with an embodiment of the present invention;

Figure 4 is a diagram showing an example of the extracting, programming and driving system of Figure 3 and a pixel circuit;

Figure 5 is a diagram showing a further example of the extracting, programming and driving system of Figure 3 and a pixel circuit;

Figure 6 is a diagram showing a further example of

the extracting, programming and driving system of Figure 3 and a pixel circuit;

Figure 7 is a diagram showing a further example of the extracting, programming and driving system of Figure 3 and a pixel circuit;

Figure 8 is a diagram showing a pixel circuit to which a step-calibration driving in accordance with an embodiment of the present invention is applied;

Figure 9 is a diagram showing an example of a driver and extraction block and the driving transistor of Figure 8;

Figure 10 is a diagram showing an example of an extraction algorithm implemented by a DPU block of Figure 9;

Figure 11 is a diagram showing a further example of the extraction algorithm implemented by the DPU block of Figure 9;

Figure 12 is a timing diagram showing an example of waveforms for the step-calibration driving;

Figure 13 is a timing diagram showing a further example of waveforms for the step-calibration driving;

Figure 14 is a diagram showing a pixel circuit to which the step-calibration driving is applicable;

Figure 15 is a graph showing the results of simulation for the step-calibration driving;

Figure 16 is a diagram showing an example of a system architecture for the step-calibration driving with a display array;

Figure 17 is a timing diagram showing an example of waveforms applied to the system architecture of Figure 16;

Figure 18 is a timing diagram showing an example of waveforms for a voltage/current extraction;

Figure 19 is a timing diagram showing a further example of waveforms for the voltage/current extraction;

Figure 20 is a diagram showing a pixel circuit to which the voltage/current extraction of Figure 19 is applicable;

Figure 21 is a timing diagram showing a further example of waveforms for the voltage/current extraction;

Figure 22 is a diagram showing a pixel circuit to which the voltage/current extraction of Figure 21 is applicable;

Figure 23 is a diagram showing a mirror based pixel circuit to which OLED removing in accordance with an embodiment of the present invention is applied;

Figure 24 is a diagram showing a programming path of Figure 23 when applying the OLED removing;

Figure 25 is a diagram showing an example of a system architecture for the OLED removing; and

Figure 26 is a graph showing the simulation result for the voltage on IDATA line for different threshold voltage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

[0021] Embodiments of the present invention are described using a pixel including a light emitting device and a plurality of transistors. The light emitting device may be an organic light emitting diode (OLED). It is noted that "pixel" and "pixel circuit" may be used interchangeably.

[0022] Real-time calibration-scheduling for a display array having a plurality of pixels is described in detail. Figure 1 illustrates a process for a calibration-scheduling in accordance with an embodiment of the present invention. According to this technique, the pixels are calibrated based on their aging and/or usage during the normal operation of the display array.

[0023] A linked list of pixels is generated in step S2. The linked list contains an identification of a pixel with high brightness for calibration. The linked list is used to schedule the priority in calibration.

[0024] In step S4, "***n***" is chosen based on the display size and expected instability with time (e.g. shift in characteristics of transistors and light emitting device). "***n***" represents the number of pixels that are calibrated in each programming cycle. "***n***" may be one or more than one.

[0025] Then programming cycle starts at step S6. The step S6 includes steps S8-S16. The steps S8-S16 are implemented on a selected column of the display array.

[0026] In step S8, "***n***" pixels in the selected column are selected from the beginning of the linked list, hereinafter referred to as "Selected Pixels".

[0027] In step S10, "Calibration Mode" is enabled for the Selected Pixels, and "Normal Operation Mode" is enabled for the rest of the pixels in the selected column of the display array.

[0028] In step S12, all pixels in the selected column are programmed by a voltage source driver (e.g. 28 of Figure 2) which is connected to a data line of the pixel.

[0029] For the Selected Pixels, current flowing through the data line is monitored during the programming cycle.

For the pixels other than the Selected Pixels in the selected column, the corresponding programming voltage is boosted using data stored in a memory (e.g. 34 of Figure 2), hereinafter referred to as "ΔV compensation memory".

[0030] In step S14, the monitored current is compared with the expected current that must flow through the data line. Then, a calibration data curve for the Selected Pixels is generated. The ΔV compensation memory is updated based on the calibration data curve.

[0031] The calibration data curve stored in the ΔV compensation memory for a pixel will be used to boost programming voltage for that pixel in the next programming cycles when that pixel is in the Normal Operation Mode.

[0032] In step S 16, the identifications of the Selected Pixels are sent to the end of the linked list. The Selected Pixels have the lowest priority in the linked list for calibration.

[0033] During display operation (S6-S16), the linked list will provide a sorted priority list of pixels that must be calibrated. It is noted that in the description, the term "linked list" and the term "priority list" may be used interchangeably.

[0034] The operation goes back (S18) to the step S8. The next programming cycle starts. A new column in the display array is activated (selected), and, new "***n***" pixels in the new activated column are selected from the top of the linked list. The ΔV compensation memory is updated using the calibration data obtained for the new Selected Pixels.

[0035] The number of the Selected Pixels, "***n***", is now described in detail. As described above, the number "***n***" is determined based on the display size and expected instability in device characteristics with time. It is assumed that the total number of pixels N is $N = 3 \times m_1 \times m_2$, where m_1 and m_2 are the number of rows and columns in the display, respectively.

[0036] The highest rate in characteristics shift is K ($=\Delta I/\Delta t.I$). Each programming cycle takes $t=1/f.m_2$. The maximum expected shift in characteristics after the entire display is calibrated is $\Delta I/I = K.t.N/n < e$, where e is the allowed error. After this the calibration can be redone from the beginning, and the error is eliminated. This shows that $n > K.t.N/e$ or $n > 3.K.m_1/f.e$. For instance, if K = 1%/hr, m_1 = 1024, f = 60 Hz, and e =0.1%, then n > 0.14, which implies that it is needed to calibrate once in 5 programming cycles. This is achievable with one calibration unit, which operates only one time in 5 programming cycles. Each calibration unit enables calibration of one pixel at a programming cycle. If e = 0.01 %, n > 1.4. This means that two calibration units calibrating two pixels in each programming cycle are required. This shows that it is feasible to implement this calibration system with very low cost.

[0037] The frequency of calibration can be reduced automatically as the display ages, since shifts in characteristics will become slower as the time progresses. In addition, the pixels that are selected for calibration can be programmed with different currents depending on display data. The only condition is that their programming current is larger than a reference current. Therefore, the calibration can be performed at multiple brightness levels for one pixel to achieve higher accuracy.

[0038] The linked list is described in detail. In the linked list, the pixels with high brightness for calibration are listed. The display data is used to determine the pixels with high brightness for calibration. Calibration at low currents is slow and often not accurate. In addition, maximum shift in characteristics occurs for pixels with high current. Thus, in order to improve the accuracy and speed of calibration, the pixels, which must be programmed with currents higher than a threshold current I_{TH}, are selected and stored in the linked list.

[0039] I_{TH} is a variable and may be "0". For $I_{TH} = 0$, all pixels are listed in the linked list, and the calibration is performed for all pixels irrespective of their programming current.

[0040] The calibration-scheduling technique described above is applicable to any current programmed pixels, for example, but not limited to, a current mirror based pixel.

[0041] Figure 2 illustrates an example of a system structure for implementing the calibration-scheduling of Figure 1. A system 30 of Figure 2 for implementing calibration-scheduling algorithm is provided to a display array 10 having a plurality of pixel circuits 12. The pixel circuit 12 is a current programmed pixel circuit, such as, but not limited to a current mirror based pixel. The pixel circuits 12 are arranged in row and column.

[0042] The pixel circuit 12 may include an OLED and a plurality of transistors (e.g. TFTs). The transistor may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET). The display array 10 may be an AMOLED display array.

[0043] The pixel circuit 12 is operated by a gate line 14 connected to a gate driver 20, a data line 16 connected to a voltage data driver 28, and a power line connected to a power supply 24. In Figure 2, two data lines, two gate lines and two power lines are shown as an example. It is apparent that more than two data lines, two gate lines and two power lines may be provided to the display array 10.

[0044] The system 30 includes a calibration scheduler and memory block 32 for controlling programming and calibration of the display array 10, and a ΔV compensation memory 34 for storing ΔV compensation voltage (value). In each programming cycle, a column of the display array 10 is selected. The calibration scheduler and memory block 32 enables Normal Operation Mode or Calibration Mode for the selected column (i.e., data line) during that programming cycle.

[0045] The system 30 further includes a monitoring system for monitoring and measuring a pixel current. The monitoring system includes switches 36 and 38 and a

voltage sensor 40 with an accurate resistor 42. In Figure 2, the switches 36 and 38 are provided for each data line as an example.

[0046] The system 30 further includes a generator for generating ΔV compensation voltage based on the monitoring result. The generator includes an analog/digital converter (A/D) 44, a comparator 46, and a translator 48. The A/D 44 converts the analog output of the voltage sensor 40 into a digital output. The comparator 46 compares the digital output to an output from the translator 48. The translator 48 implements function f(V) on a digital data input 52. The translator 48 converts the current data input 52 to the voltage data input through f(v). The result of the comparison by the comparator 46 is stored in the ΔV compensation memory 34.

[0047] The system 30 further includes an adder 50 for adding the digital data input 52 and the ΔV compensation voltage stored in the ΔV compensation memory 34. The voltage data driver 28 drives a data line based on the output of the adder 50. The programming data for the data line is adjusted by adding the ΔV compensation voltage.

[0048] When the calibration scheduler and memory block 32 enables the Normal Operation Mode for a selected data line, the switch 36 is activated. The voltage output from the voltage data driver 28 is directly applied to the pixel on that data line.

[0049] When the calibration scheduler and memory block 32 enables the Calibration Mode for that data line, the switch 38 is activated. The voltage is applied to the pixel on that data line through the accurate resistor 42. The voltage drop across the resistor 42 at the final stages of the programming time (i.e. when initial transients are finished) is measured by the voltage sensor 40. The voltage drop monitored by the voltage sensor 40 is converted to digital data by the A/D 44. The resulting value of the voltage drop is proportional to the current flowing through the pixel if the pixel is a current programmed pixel circuit. This value is compared by the comparator 46 to the expected value obtained by the translator 48.

[0050] The difference between the expected value and the measured value is stored in the ΔV compensation memory 34, and will be used for a subsequent programming cycle. The difference will be used to adjust the data voltage for programming of that pixel in future.

[0051] The calibration scheduler and memory block 32 may include the linked list described above. In the beginning, the linked list is generated automatically. It may be just a list of pixels. However, during the operation it is modified.

[0052] The calibration of the pixel circuits with high brightness guarantees the high speed and accurate calibration that is needed in large or small area displays.

[0053] Since the display array 10 is driven using a voltage programming technique, it is fast and can be used for high-resolution and large area displays.

[0054] Due to speed, accuracy, and ease of implementation, the applications of the calibration-scheduling technique ranges from electroluminescent devices used for cellphones, personal organizers, monitors, TVs, to large area display boards.

[0055] The system 30 monitors and measures voltage drop which depends on time dependent parameters of the pixel, and generates a desirable programming data. However, the time dependent parameters of the pixel may be extracted by any mechanisms other than that of Figure 2.

[0056] A further technique for programming, extracting time dependent parameters of a pixel and driving the pixel is described in detail with reference to Figures 3-7. This technique includes voltage-extracting for calibration. Programming data is calibrated with the extracted information, resulting in a stable pixel current over time. Using this technique, the aging of the pixel is extracted.

[0057] Figure 3 illustrates a system architecture for implementing a voltage-extracting, programming and driving in accordance with an embodiment of the present invention. The system of Figure 3 implements the voltage-extracting and programming to a current mode pixel circuit 60. The pixel circuit 60 includes a light emitting device and a plurality of transistors having a driving transistor (not shown). The transistors maybe TFTs.

[0058] The pixel circuit 60 is selected by a select line SEL and is driven by DATA on a data line 61. A voltage source 62 is provided to write a programming voltage V_P into the pixel circuit 60. A current-controlled voltage source (CCVS) 63 having a positive node and a negative node is provided to convert the current on the data line 61 to a voltage Vext. A display controller and scheduler 64 operates the pixel circuit 60. The display controller and scheduler 64 monitors an extracted voltage Vext output from the CCVS 63 and then controls the voltage source 62.

[0059] The resistance of CCVS 63 is negligible. Thus the current on the data line 61 is written as:

$$I_{Line} = I_{piexl} = \beta (V_P - V_T)^2 \qquad \ldots(1)$$

where I_{Line} represents the current on the data line 61, I_{piexl} represents a pixel current, V_T represents the threshold voltage of the driving transistor included in the pixel circuit 60, and β represents the gain parameter in the TFT characteristics.

[0060] As the threshold voltage of the driving TFT increases during the time, the current on the data line 61 decreases. By monitoring the extracted voltage Vext, the display controller and scheduler 64 determines the amount of shift in the threshold voltage.

[0061] The threshold voltage V_T of the driving transistor can be calculate as:

$$V_T = V_P - (I_{Line}/\beta)^{0.5} \qquad \ldots(2)$$

[0062] The programming voltage V_P is modified with the extracted information. The extraction procedure can be implemented for one or several pixels during each frame time.

[0063] Figure 4 illustrates an example of a system for the voltage-extracting, programming and driving of Figure 3, which is employed with a top-emission current-cell pixel circuit 70. The pixel circuit 70 includes an OLED 71, a storage capacitor 72, a driving transistor 73 and switch transistors 74 and 75.

[0064] The transistors 73, 74 and 75 may be n-type TFTs. However, these transistors 73, 74 and 75 may be p-type transistors. The voltage-extracting and programming technique applied to the pixel circuit 70 is also applicable to a pixel circuit having p-type transistors.

[0065] The driving transistor 73 is connected to a data line 76 through the switch transistor 75, and is connected to the OLED 71, and also is connected to the storage capacitor 72 through the switch transistor 74. The gate terminal of the driving transistor 73 is connected to the storage capacitor 72. The gate terminals of the switch transistors 74 and 75 are connected to a select line SEL. The OLED 71 is connected to a voltage supply electrode or line VDD. The pixel circuit 70 is selected by the select line SEL and is driven by DATA on the data line 76.

[0066] A current conveyor (CC) 77 has X, Y and Z terminals, and is used to extract a current on the data line 76 without loading it. A voltage source 78 applies programming voltage to the Y terminal of the CC 77. In the CC 77, the X terminal is forced by feedback to have the same voltage as that of the Y terminal. Also, the current on the X terminal is duplicated into the Z terminal of the CC 77. A current-controlled voltage source (CCVS) 79 has a positive node and a negative node. The CCVS 79 converts the current on the Z terminal of the CC 77 into a voltage Vext.

[0067] Vext is provided to the display controller and scheduler 64 of Figure 3, where the threshold voltage of the driving transistor 73 is extracted. The display controller and scheduler 64 controls the voltage source 78 based on the extracted threshold voltage.

[0068] Figure 5 illustrates a further example of a system for the voltage-extracting, programming, and driving of Figure 3, which is employed with a bottom-emission current-cell pixel circuit 80. The pixel circuit 80 includes an OLED 81, a storage capacitor 82, a driving transistor 83, and switch transistors 84 and 85. The transistors 83, 84 and 85 may be n-type TFTs. However, these transistors 83, 84 and 85 may be p-type transistors.

[0069] The driving transistor 83 is connected to a data line 86 through the switch transistor 85, and is connected to the OLED 81, and also is connected to the storage capacitor 82. The gate terminal of the driving transistor 83 is connected to a voltage supply line VDD through the switch transistor 84. The gate terminals of the switch transistors 84 and 85 are connected to a select line SEL. The pixel circuit 80 is selected by the select line SEL and is driven by DATA on the data line 86.

[0070] A current conveyor (CC) 87 has X, Y and Z terminals, and is used to extract a current on the data line 86 without loading it. A voltage source 88 applies a negative programming voltage at the Y terminal of the CC 87. In the CC 87, the X terminal is forced by feedback to have the same voltage as that of the Y terminal. Also, the current on the X terminal is duplicated into the Z terminal of the CC 87. A current-controlled voltage source (CCVS) 89 has a positive node and a negative node. The CCVS 89 converts the current of the Z terminal of the CC 87 into a voltage Vext.

[0071] Vext is provided to the display controller and scheduler 64 of Figure 3, where the threshold voltage of the driving transistor 83 is extracted. The display controller and scheduler 64 controls the voltage source 88 based on the extracted threshold voltage.

[0072] Figure 6 illustrates a further example of a system for the voltage-extracting, programming and driving of Figure 3, which is employed with a top-emission current-mirror pixel circuit 90. The pixel circuit 90 includes an OLED 91, a storage capacitor 92, mirror transistors 93 and 94, and switch transistors 95 and 96. The transistors 93, 94, 95 and 96 may be n-type TFTs. However, these transistors 93, 94, 95 and 96 maybe p-type transistors.

[0073] The mirror transistor 93 is connected to a data line 97 through the switch transistor 95, and is connected to the storage capacitor 92 through the switch transistor 96. The gate terminals of the mirror transistors 93 and 94 are connected to the storage capacitor 92 and the switch transistor 96. The mirror transistor 94 is connected to a voltage supply electrode or line VDD through the OLED 91. The gate terminals of the switch transistors 85 and 86 are connected to a select line SEL. The pixel circuit 90 is selected by the select line SEL and is driven by DATA on the data line 97.

[0074] A current conveyor (CC) 98 has X, Y and Z terminals, and is used to extract the current of the data line 97 without loading it. A voltage source 99 applies a positive programming voltage at the Y terminal of the CC 98. In the CC 98, the X terminal is forced by feedback to have the same voltage as the voltage of the Y terminal. Also, the current on the X terminal is duplicated into the Z terminal of the CC 98. A current-controlled voltage source (CCVS) 100 has a positive node and a negative node. The CCVS 100 converts a current on the Z terminal of the CC 98 into a voltage Vext.

[0075] Vext is provided to the display controller and scheduler 64 of Figure 3, where the threshold voltage of the driving transistor 93 is extracted. The display controller and scheduler 64 controls the voltage source 99 based on the extracted threshold voltage.

[0076] Figure 7 illustrates a further example of a system for the voltage-extracting, programming and driving of Figure 3, which is employed with a bottom-emission current-mirror pixel circuit 110. The pixel circuit 110 includes an OLED 111, a storage capacitor 112, mirror transistors 113 and 116, and switch transistors 114 and

115. The transistors 113,114, 115 and 116 may be n-type TFTs. However, these transistors 113, 114, 115 and 116 may be p-type transistors.

[0077] The mirror transistor 113 is connected to a data line 117 through the switch transistor 114, and is connected to the storage capacitor 112 through the switch transistor 115. The gate terminals of the mirror transistors 113 and 116 are connected to the storage capacitor 112 and the switch transistor 115. The mirror transistor 116 is connected to a voltage supply line VDD. The mirror transistors 113, 116 and the storage capacitor 112 are connected to the OLED 111. The gate terminals of the switch transistors 114 and 115 are connected to a select line SEL. The pixel circuit 110 is selected by the select line SEL and is driven by DATA on the data line 117.

[0078] A current conveyor (CC) 118 has X, Y and Z terminals, and is used to extract the current of the data line 117 without loading it. A voltage source 119 applies a positive programming voltage at the Y terminal of the CC 118. In the CC 118, the X terminal is forced by feedback to have the same voltage as the voltage of the Y terminal of the CC 118. Also, the current on the X terminal is duplicated into the Z terminal of the CC 118. A current-controlled voltage source (CCVS) 120 has a positive node and a negative node. The 120 converts the current on the Z terminal of the CC 118 into a voltage Vext.

[0079] Vext is provided to the display controller and scheduler 64 of Figure 3, where the threshold voltage of the driving transistor 113 is extracted. The display controller and scheduler 64 controls the voltage source 119 based on the extracted threshold voltage.

[0080] Referring to Figures 3-7, using the voltage-extracting technique, time dependent parameters of a pixel (e.g. threshold shift) can be extracted. Thus, the programming voltage can be calibrated with the extracted information, resulting in a stable pixel current over time. Since the voltage of the OLED (i.e. 71 of Figure 4, 81 of Figure 5, 91 of Figure 6, 111 of Figure 7) affects the current directly, the voltage-extracting driving technique described above can also be used to extract OLED degradation as well as the threshold shift.

[0081] The voltage-extracting technique described above can be used with any current-mode pixel circuit, including current-mirror and current-cell pixel circuit architectures, and are applicable to the display array 10 of Figure 2. A stable current independent of pixel aging under prolonged display operation can be provided using the extracted information. Thus, the display operating lifetime is efficiently improved.

[0082] It is noted that the transistors in the pixel circuits of Figures 3-7 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET). The pixel circuits of Figures 3-7 may form AMOLED display arrays.

[0083] A further technique for programming, extracting time dependent parameters of a pixel and driving the pixel is described in detail with reference to Figures 8-17. The technique includes a step-calibration driving technique. In the step-calibration driving technique, information on the aging of a pixel (e.g. threshold shift) is extracted. The extracted information will be used to generate a stable pixel current/luminance. Despite using the one-bit extraction technique, the resolution of the extracted aging is defined by display drivers. Also, the dynamic effects are compensated since the pixel aging is extracted under operating condition, which is similar to the driving cycle.

[0084] Figure 8 illustrates a pixel circuit 160 to which a step-calibration driving in accordance with an embodiment of the present invention is applied. The pixel circuit 160 includes an OLED 161, a storage capacitor 162, and a driving transistor 163 and switch transistors 164 and 165. The pixel circuit 160 is a current-programmed, 3-TFT pixel circuit. A plurality of the pixel circuits 160 may form an AMOLED display.

[0085] The transistors 163, 164 and 165 are n-type TFTs. However, the transistors 163, 164 and 165 may be p-type TFTs. The step-calibration driving technique applied to the pixel circuit 160 is also applicable to a pixel circuit having p-type transistors. The transistors 163,164 and 165 maybe fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0086] The gate terminal of the driving transistor 163 is connected to a signal line VDATA through the switch transistor 164, and also connected to the storage capacitor 162. The source terminal of the driving transistor 163 is connected to a common ground. The drain terminal of the driving transistor 163 is connected to a monitor line MONITOR through the switch transistor 165, and also is connected to the cathode electrode of the OLED 161.

[0087] The gate terminal of the switch transistor 164 is connected to a select line SEL1. The source terminal of the switch transistor 164 is connected to the gate terminal of the driving transistor 163, and is connected to the storage capacitor 162. The drain terminal of the switch transistor 164 is connected to VDATA.

[0088] The gate terminal of the switch transistor 165 is connected to a select line SEL2. The source terminal of the switch transistor 165 is connected to MONITOR. The drain terminal of the switch transistor 165 is connected to the drain terminal of the driving transistor 163 and the cathode electrode of the OLED 161. The anode electrode of the OLED 161 is connected to a voltage supply electrode or line VDD.

[0089] The transistors 163 and 164 and the storage capacitor 162 are connected at node A3. The transistors 163 and 165 and the OLED 161 are connected at node B3.

[0090] Figure 9 illustrates an example of a driver and extraction block 170 along with the driving transistor 163 of Figure 8. In Figure 9, each of Rs 171a and Rs 171b represents the ON resistance of the switch transistors (e.g. 164, 165 of Figure 8). Cs represents the storage

capacitor of the pixel, C_{OLED} represents the OLED capacitance, and CP represents the line parasitic capacitance. In Figure 9, the OLED is presented as a capacitance.

[0091] A block 173 is used to extract the threshold voltage of the driving transistor, during the extraction cycle. The block 173 may be a current sense amplifier (SA) or a current comparator. In the description, the block 173 is referred to as "SA block 173".

[0092] If the current of the MONITOR line is higher than a reference current (IREF), the output of the SA block 173 (i.e. Triggers of Figure 10, 11) becomes one. If the current of the MONITOR line is less than the reference current (IREF), the output of the SA block 173 becomes zero.

[0093] It is noted that the SA block 173 can be shared between few columns result in less overhead. Also, the calibration of the pixel circuit can be done one at a time, so the extraction circuits can be shared between the all columns.

[0094] A data process unit (DPU) block 172 is provided to control the programming cycle, contrast, and brightness, to perform the calibration procedure and to control the driving cycle. The DPU block 172 implements extraction algorithm to extract (estimate) the threshold voltage of the driving transistor based on the output from the SA block 173, and controls a driver 174 which is connected to the driving transistor 163.

[0095] Figure 10 illustrates an example of the extraction algorithm implemented by the DPU block 172 of Figure 9. The algorithm of Figure 10 is in a part of the DPU block 172. In Figure 10, $V_T(i, j)$ represents the extracted threshold voltage for the pixel (i, j) at the previous extraction cycle, V_S represents the resolution of the driver 174, "i" represents a row of a pixel array and "j" represents a column of a pixel array. Trigger conveys the comparison results of the SA block 173 of Figure 9. Less_state 180 determines the situation in which the actual V_T of the pixel is less than the predicted $V_T(V_{TM})$, Equal_state 181 determines the situation in which the predicted V_T (V_{TM}) and the actual V_T of the pixel are equal, and Great_state 182 determines the situation in which the actual V_T of the pixel is greater than the predicted V_T (V_{TM}).

[0096] The DPU block 172 of Figure 9 determines an intermediate threshold voltage V_{TM} as follows:

(A1) When s(i, j)=Less_state (180), the actual threshold voltage is less than $V_T(i, j)$, V_{TM} is set to (V_T (i, j)-Vs).

(A2) When s(i, j)=Equal_state (181), the actual threshold voltage is equal to $V_T(i, j)$, V_{TM} is set to V_T (i, j).

(A3) When s(i, j)=Greater_state (182), the actual threshold voltage is greater than $V_T(i, j)$, V_{TM} is set to ($V_T(i, j)+ V_S$).

where s(i, j) represents the previous state of the pixel (i, j) stored in a calibration memory (e.g. 208 of Figure 16).

[0097] Figure 11 illustrates a further example of the extraction algorithm implemented by the DPU block 172 of Figure 9. The algorithm of Figure 11 is in a part of the DPU block 172 of Figure 9. In Figure 11, $V_T(i, j)$ represents the extracted threshold voltage for the pixel (i, j) at the previous extraction cycle, V_S represents the resolution of the driver 174, "i" represents a row of a pixel array and "j" represents a column of a pixel array. Trigger conveys the comparison results of the SA block 173.

[0098] Further, in Figure 11, Vres represents the step that will be added/subtracted to the predicted V_T (V_{TM}) in order achieve the actual V_T of the pixel, A represents the reduction gain of a prediction step, and K represents the increase gain of the prediction step.

[0099] The operation of Figure 11 is the same as that of Figure 10, except that it has gain extra states L2 and G2 for rapid extraction of abrupt changes. In the gain states, the step size is increased to follow the changes more rapidly. L1 and G1 are the transition states which define the V_T change is abrupt or normal.

[0100] Figure 12 illustrates an example of waveforms applied to the pixel circuit 160 of Figure 8. In Figure 12, $V_{Call}=V_B+V_{TM}$, and $V_{DR} =V_P+ V_T(i, j) +V_{REF}$, where V_B represents the bias voltage during the extraction cycle, V_{TM} is defined based on the algorithm shown in Figure 10 or 11, Vp represents a programming voltage, $V_T(i, j)$ represents the extracted threshold voltage at the previous extraction cycle, V_{REF} represents the source voltage of the driving transistor during the programming cycle.

[0101] Referring to Figures 8-12, the operation of the pixel circuit 160 includes operating cycles X51, X52, X53, and X54. In Figure12, an extraction cycle is separated from a programming cycle. The extraction cycle includes X51 and X52, and the programming cycle includes X53. X54 is a driving cycle. At the end of the programming cycle, node A3 is charged to ($V_P+ V_T$) where V_P is a programming voltage and V_T is the threshold voltage of the driving transistor 163.

[0102] In the first operating cycle X51: SEL1 and SEL 2 are high. Node A3 is charged to V_{cal}, and node B3 is charged to V_{REF}. V_{cal} is V_B+V_{TM} in which V_B is a bias voltage, and V_{TM} the predicted V_T, and V_{REF} should be larger than $V_{DD}-V_{OLED0}$ where V_{OLED0} is the ON voltage of the OLED 161.

[0103] In the second operating cycle X52: SEL1 goes to zero. The gate-source voltage of the driving transistor 163 is given by:

$$VGS=V_B+V_{TM}+\Delta V_B+\Delta V_{TM}-\Delta V_{T2}-\Delta V_H$$

where VGS represents the gate-source voltage of the driving transistor 163, ΔV_B, ΔV_{TM}, $\Delta VT2$ and ΔV_H are the dynamic effects depending on V_B, V_{TM}, V_{T2} and V_H, respectively. V_{T2} represents the threshold voltage of the

switch transistor 164, and V_H represents the change in the voltage of SEL1 at the beginning of second operating cycle X52 when it goes to zero.

[0104] The SA block 173 is tuned to sense the current larger than $\beta(V_B)^2$, so that the gate-source voltage of the driving transistor 163 is larger than $(V_B + V_T)$, where β is the gain parameter in the I-V characteristic of the driving transistor 163.

[0105] As a result, after few iterations, V_{TM} and the extracted threshold voltage $V_T(i, j)$ for the pixel (i, j) converge to:

$$V_{TM}=V_T-\gamma\cdot(V_B+V_T+V_{T2}-V_H)$$

$$\gamma=\frac{C_{g2}/(2\cdot C_S)}{1+C_{g2}/(2\cdot C_S)}$$

where C_{g2} represents the gate capacitance of the switch transistor 164.

[0106] In the third operating cycle X53: SEL1 is high. VDATA goes to V_{DR}. Node A3 is charged to $[V_P+V_T(i, j)-\gamma(V_P-V_B)]$.

[0107] In the fourth operating cycle X54: SEL1 and SEL2 go to zero. Considering the dynamic effects, the gate-source voltage of the driving transistor 163 can be written as:

$$VGS=V_P+V_T$$

[0108] Therefore, the pixel current becomes independent of the static and dynamic effects of the threshold voltage shift.

[0109] In Figure 12, the extraction cycle and the programming cycle are shown as separated cycles. However, the extraction cycle and the programming cycle may be merged as shown in Figure 13. Figure 13 illustrates a further example of waveforms applied to the pixel circuit 160 of Figure 8.

[0110] Referring to Figures 8-11 and 13, the operation of the pixel circuit 160 includes operating cycles X61, X62 and X63. Programming and extraction cycles are merged into the operating cycles X61 and X62. The operating cycle X63 is a driving cycle.

[0111] During the programming cycle, the pixel current is compared with the desired current, and the threshold voltage of the driving transistor is extracted with the algorithm of Figure 10 or 11. The pixel circuit 160 is programmed with $V_{DR}=V_P+ V_T (i,j)+V_{REF}$ during the operating cycle X61. Then the pixel current is monitored through the MONITOR line, and is compared with the desired current. Based on the comparison result and using the extraction algorithm of Figures 10 or 11, the threshold voltage V_T (i, j) is updated.

[0112] In Figure 8, two select lines SEL1 and SEL2 are shown. However, a signal select line (e.g. SEL1) can be used as a common select line to operate the switch transistors 164 and 165. When using the common select line, SEL1 of Figure 12 stays at high in the second operating cycle X52, and the VGS remains at (V_B+V_{TM}). Therefore, the dynamic effects are not detected.

[0113] The step-calibration driving technique described above is applicable to the pixel circuit 190 of Figure 14. The pixel circuit 190 includes an OLED 191, a storage capacitor 192, and a driving transistor 193 and switch transistors 194 and 195. The pixel circuit 190 is a current-programmed, 3-TFT pixel circuit. A plurality of the pixel circuits 190 may form an AMOLED display.

[0114] The transistors 193, 194 and 195 are n-type TFTs. However, the transistors 193, 194 and 195 may be p-type TFTs. The step-calibration driving technique applied to the pixel circuit 190 is also applicable to a pixel circuit having p-type transistors. The transistors 193, 194 and 195 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0115] The gate terminal of the driving transistor 193 is connected to a signal line VDATA through the switch transistor 194, and also connected to the storage capacitor 192. The source terminal of the driving transistor 193 is connected to the anode electrode of the OLED 191, and is connected to a monitor line MONITOR through the switch transistor 195. The drain terminal of the driving transistor 193 is connected to a voltage supply line VDD. The gate terminals of the transistors 194 and 195 are connected to select lines SEL1 and SEL2, respectively.

[0116] The transistors 193 and 194 and the storage capacitor 192 are connected at node A4. The transistor 195, the OLED 191 and the storage capacitor 192 are connected at node B4.

[0117] The structure of the pixel circuit 190 is similar to that of Figure 8, except that the OLED 191 is at the source terminal of the driving transistor 193. The operation of the pixel circuit 190 is the same as that of Figure 12 or 13.

[0118] Since the source terminal of the drive TFT 193 is forced to VREF during the extraction cycle (X51 and X52 or X62), the extracted data is independent of the ground bouncing. Also, during the programming cycle (X53 or X61), the source terminal of the drive TFT is forced to VREF, the gate-source voltage of the drive TFT becomes independent of the ground bouncing. As a result of these conditions, the pixel current is independent of ground bouncing.

[0119] Figure 15 illustrates the results of simulation for the step-calibration driving technique. In Figure 15, "Case I" represents an operation of Figure 8 where SEL1 goes to zero in the second operating cycle (X52 of Figure 12); "Case II" represents an operation of Figure 8 where SEL1 stays at high in the second operating cycle.

[0120] In Figure 15, ΔV_{TR} is the minimum detectable shift in the threshold voltage of the driving transistor (e.g. 163 of Figure 8), ΔV_{T2R} is the minimum detectable shift in the threshold voltage of the switch transistor (e.g. 164 of Figure 8), and I_{PL} is the pixel current of the pixel during the driving cycle.

[0121] The pixel current of Case II is smaller than that of Case I for a given programming voltage due to the dynamic effects of the threshold voltage shift. Also, the pixel current of Case II increases as the threshold voltage of the driving transistor increases (a), and decreases as the threshold voltage of the switch transistor decreases (b). However, the pixel current of Case I is stable. The maximum error induced in the pixel current is less than %0.5 for any shift in the threshold voltage of the driving and switch TFTs. It is obvious that ΔV_{T2R} is larger than ΔV_{TR} because the effect of a shift in V_T on the pixel current is dominant. These two parameters are controlled by the resolution (V_S) of the driver (e.g. 174 of Figure 9), and the SNR of the SA block (e.g. 193 of Figure 9). Since a shift smaller than ΔV_{TR} cannot be detected, and also the time constant of threshold-shift is large, the extraction cycles (e.g. X51, X52 of Figure 12) can be done after a long time interval consisting of several frames, leading to lower power consumption. Also, the major operating cycles become the other programming cycle (e.g. X53 of Figure 12) and the driving cycle (e.g. X54 of Figure 12). As a result, the programming time reduces significantly, providing for high-resolution, large-area AMOLED displays where a high-speed programming is prerequisite.

[0122] Figure 16 illustrates an example of a system architecture for the step-calibration driving with a display array 200. The display array 200 includes a plurality of the pixel circuits (e.g. 160 of Figure 8 or 190 of Figure 14).

[0123] A gate driver 202 for selecting the pixel circuits, a drivers/SAs block 204, and a data process and calibration unit block 206 are provided to the display array 200. The drivers/SAs block 204 includes the driver 174 and the SA block 173 of Figure 9. The data process and calibration unit block 206 includes the DPU block 172 of Figure 9. "Calibration" in Figure 16 includes the calibration data from a calibration memory 208, and may include some user defined constants for setting up calibration data processing. The contrast and the brightness inputs are used to adjust the contrast and the brightness of the panel by the user. Also, gamma-correction data is defined based on the OLED characteristic and human eye. The gamma-correction input is used to adjust the pixel luminance for human eyes.

[0124] The calibration memory 208 stores the extracted threshold voltage $V_T(i, j)$ and the state s(i, j) of each pixel. A memory 210 stores the other required data for the normal operation of a display including gamma correction, resolution, contrast, and etc. The DPU block performs the normal tasks assigned to a controller and scheduler in a display. Besides, the algorithm of Figure 10 or 11 is added to it to perform the calibration.

[0125] Figure 17 illustrates an example of waveforms applied to the system architecture of Figure 16. In Figure 17, each of ROW[1], ROW[2], and ROW[3] represents a row of the display array 200, "E" represents an extraction operation, "P" represents a programming operation and "D" represents a driving operation. It is noted that the extraction cycles (E) are not required to be done for all the frame cycle. Therefore, after a long time interval (extraction interval), the extraction is repeated for a pixel.

[0126] As shown in Figure 17, only one extraction procedure occurs during a frame time. Also, the VT extraction of the pixel circuits at the same row is preformed at the same time.

[0127] Therefore, the maximum time required to refresh a frame is:

$$\tau_F = n \cdot \tau_P + \tau_E$$

where τ_F represents the frame time, τ_P represents the time required to write the pixel data into the storage capacitor (e.g. 162 of Figure 8), τ_E represents the extraction time, and n represents the number of row in the display array (e.g. 200 of Figure 16).

[0128] Assuming $\tau_E = m \cdot \tau_P$, the frame time τ_F can be written as:

$$\tau_F = (n + m) \cdot \tau_P$$

where m represents the timing required for the extraction cycles in the scale of programming cycle timing (τ_P).

[0129] For example, for a Quarter Video Graphics Array (QVGA) display (240x320) with frame rate of 60Hz, if m=10, the programming time of each row is 66μs, and the extraction time is 0.66ms.

[0130] It is noted that the step-calibration driving technique described above is applicable to any current-programmed pixel circuit other than those of Figures 8 and 14.

[0131] Using the step-calibration driving technique, the time dependent parameter(s) of a pixel, such as threshold shift, is extracted. Then, the programming-voltage is calibrated with the extracted information, resulting in a stable pixel current over time. Further, a stable current independent of the pixel aging under prolonged display operation can be is provided to the pixel circuit, which efficiently improves the display operating lifetime.

[0132] A technique for programming, extracting time dependent parameters of a pixel and driving the pixel in accordance with a further embodiment of the present invention is described in detail. The technique includes extracting information on the aging of a pixel (e.g. OLED luminance) by monitoring OLED voltage or OLED current, and generating luminance. The programming voltage is calibrated with the extracted information, resulting in stable brightness over time.

[0133] Since the OLED voltage/current has been reported to be correlated with the brightness degradation in the OLED (e.g. 161 of Figure 8, 191 of Figure 14), the programming voltage can be modified by the OLED voltage/current to provide a constant brightness.

[0134] For example, during the driving cycle, the voltage/current of the OLED (161 of Figure 8 or 191 of Figure 14) is extracted while SEL2 is high. Since the OLED voltage or current has been reported to be correlated with the brightness degradation in the OLED, the programming voltage can be modified by the OLED voltage to provide a constant brightness.

[0135] Figure 18 illustrates an example of waveforms for the voltage/current extraction. The waveforms of Figure 18 are applicable to the pixel circuit 160 of Figure 8 and the pixel circuit 190 of Figure 14 to extract OLED voltage/current. The operation of Figure 18 includes operating cycles X71, X72 and X73. The operating cycles X71 and X72 are an OLED extraction cycle. The operating cycle X73 is one of the operating cycles shown in Figure 12 and 13.

[0136] During the first operating cycle X71, SEL1 and SEL2 are high, and VDATA is zero. The gate-source voltage of the driving transistor (e.g. 163 of Figure 8) becomes zero. A current or voltage is applied to the OLED (161 of Figure 8) through the MONITOR line.

[0137] During the second operating cycle X72, SEL2 is high and SEL1 is low. The OLED voltage or current is extracted through the MONITOR line using the algorithm presented in Figures 10 or 11. This waveform can be combined with any other driving waveform.

[0138] In the above description, the algorithm of Figure 10 and 11 is used to predict the aging data, i.e. V_T shift, based on the comparison results (current with current or voltage with voltage). However, the algorithm of Figures 10 and 11 is applicable to predict the shift in the OLED voltage V_{OLED} by replacing V_T with the V_{OLED} and the comparison result of OLED current/voltage with a reference current/voltage. In the description above, the system architecture shown in Figure 9 is used to compensate for the threshold shift. However, it is understood that the OLED data is also extracted when the architecture of Figure 9, i.e. DPU 172, block 173, driver 174, is used. This data can be used to compensate for the OLED shift.

[0139] The operating cycle X73 can be any operating cycle including the programming cycle. This depends on the status of the panel after OLED extraction. If it is during the operation, then X73 is the programming cycle of the waveforms in Figures 12 and 13. The OLED voltage can be extracted during the driving cycle X55/X63 of Figure 12/13. During the driving cycle X55/X63, the SEL2 of Figure 8 or 14 goes to a high voltage, and so the voltage of the OLED can be read back through the MONITOR for a specific pixel current.

[0140] Figure 19 illustrates a further example of waveforms for the voltage/current extraction. Figure 20 illustrates a pixel circuit 220 to which the voltage/current extraction of Figure 19 is applied.

[0141] Referring to Figure 20, the pixel circuit 220 includes an OLED 221, a storage capacitor 222, and a driving transistor 223 and switch transistors 224 and 225. A plurality of the pixel circuits 220 may form an AMOLED display.

[0142] The transistors 223, 224 and 225 are n-type TFTs. However, the transistors 223, 224 and 225 may be p-type TFTs. The voltage/current extraction technique applied to the pixel circuit 220 is also applicable to a pixel circuit having p-type transistors. The transistors 223, 224 and 225 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0143] The gate terminal of the driving transistor 223 is connected to the source terminal of the switch transistor 224, and also connected to the storage capacitor 222. The one terminal of the driving transistor 223 is connected to a common ground. The other terminal of the driving transistor 223 is connected to a monitor and data line MONITOR/DATA through the switch transistor 235, and is also connected to the cathode electrode of the OLED 221.

[0144] The gate terminal of the switch transistor 224 is connected to a select line SEL1. The one terminal of the switch transistor 224 is connected to the gate terminal of the driving transistor 223, and is connected to the storage capacitor 222. The other terminal of the switch transistor 224 is connected to the cathode electrode of the OLED 221.

[0145] The gate terminal of the switch transistor 225 is connected to a select line SEL2. The one terminal of the switch transistor 225 is connected to MONITOR/DATA. The other terminal of the switch transistor 225 is connected to the driving transistor 223 and the cathode electrode of the OLED 221. The anode electrode of the OLED 221 is connected to a voltage supply electrode or line VDD.

[0146] The transistors 223 and 224 and the storage capacitor 222 are connected at node A5. The transistors 223 and 225 and the OLED 221 are connected at node B5.

[0147] The pixel circuit 220 is similar to the pixel circuit 160 of Figure 8. However, in the pixel circuit 220, the MONITOR/DATA line is used for monitoring and programming purpose.

[0148] Referring to Figures 19-20, the operation of the pixel circuit 220 includes operating cycles X81, X82 and X83.

[0149] During the first operating cycle X81, SEL1 and SEL2 are high and MONITOR/DATA is zero. The gate-source voltage of the driving transistor (223 of Figure 20) becomes zero.

[0150] During the second operating cycle X82, a current or voltage is applied to the OLED through the MONITOR/DATA line, and its voltage or current is extracted. As described above, the shift in the OLED voltage is extracted using the algorithm presented in Figure 10 or 11

based on the monitored voltage or current. This waveform can be combined with any driving waveform.

[0151] The operating cycle X83 can be any operating cycle including the programming cycle. This depends on the status of the panel after OLED extraction..

[0152] The OLED voltage/current can be extracted during the driving cycle of the pixel circuit 220 of Figure 20 after it is programmed for a constant current using any driving technique. During the driving cycle the SEL2 goes to a high voltage, and so the voltage of the OLED can be read back through the MONITOR/DATA line for a specific pixel current.

[0153] Figure 21 illustrates a further example of waveforms for the voltage/current extraction technique. Figure 22 illustrates a pixel circuit 230 to which the voltage/current extraction of Figure 21 is applied. The waveforms of Figure 21 is also applicable to the pixel circuit 160 of Figure 8 to extract OLED voltage/current.

[0154] Referring to Figure 22, the pixel circuit 230 includes an OLED 231, a storage capacitor 232, and a driving transistor 233 and switch transistors 234 and 235. A plurality of the pixel circuits 230 may form an AMOLED display.

[0155] The transistors 233, 234 and 235 are n-type TFTs. However, the transistors 233, 234 and 235 may be p-type TFTs. The voltage/current extraction technique applied to the pixel circuit 230 is also applicable to a pixel circuit having p-type transistors. The transistors 233, 234 and 235 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0156] The gate terminal of the driving transistor 233 is connected to the source terminal of the switch transistor 234, and also connected to the storage capacitor 232. The one terminal of the driving transistor 233 is connected to a voltage supply line VDD. The other terminal of the driving transistor 233 is connected to a monitor and data line MONITOR/DATA through the switch transistor 235, and is also connected to the anode electrode of the OLED 231.

[0157] The gate terminal of the switch transistor 234 is connected to a select line SELL The one terminal of the switch transistor 234 is connected to the gate terminal of the driving transistor 233, and is connected to the storage capacitor 232. The other terminal of the switch transistor 234 is connected to VDD.

[0158] The gate terminal of the switch transistor 225 is connected to a select line SEL2. The one terminal of the switch transistor 235 is connected to MONITOR/DATA. The other terminal of the switch transistor 235 is connected to the driving transistor 233 and the anode electrode of the OLED 231. The anode electrode of the OLED 231 is connected to VDD.

[0159] The transistors 233 and 234 and the storage capacitor 232 are connected at node A6. The transistors 233 and 235 and the OLED 231 are connected at node B5.

[0160] The pixel circuit 230 is similar to the pixel circuit 190 of Figure 14. However, in the pixel circuit 230, the MONITOR/DATA line is used for monitoring and programming purpose.

[0161] Referring to Figures 21-22, the operation of Figure 22 includes operating cycles X91, X92 and X93.

[0162] During the first operating cycle X91, SEL1 and SEL2 are high and VDD goes to zero. The gate-source voltage of the driving transistor (e.g. 233 of Figure 21) becomes zero.

[0163] During the second operating cycle X92, a current (voltage) is applied to the OLED (e.g. 231 of Figure 21) through the MONITOR/DATA line, and its voltage (current) is extracted. As described above, the shift in the OLED voltage is extracted using the algorithm presented in Figure 10 or 11 based on the monitored voltage or current. This waveform can be combined with any other driving waveform.

[0164] The operating cycle X93 can be any operating cycle including the programming cycle. This depends on the status of the panel after OLED extraction.

[0165] The OLED voltage can be extracted during the driving cycle of the pixel circuit 230 of Figure 21 after it is programmed for a constant current using any driving technique. During the driving cycle the SEL2 goes to a high voltage, and so the voltage of the OLED can be read back through the MONITOR/DATA line for a specific pixel current.

[0166] As reported, the OLED characteristics improve under negative bias stress. As a result, a negative bias related to the stress history of the pixel, extracted from the OLED voltage/current, can be applied to the OLED during the time in which the display is not operating. This method can be used for any pixel circuit presented herein.

[0167] Using the OLED voltage/current extraction technique, a pixel circuit can provide stable brightness that is independent of pixel aging under prolonged display operation, to efficiently improve the display operating lifetime.

[0168] A technique for reducing the unwanted emission in a display array having a light emitting device in accordance with an embodiment of the present invention is described in detail. This technique includes removing OLED from a programming path during a programming cycle. This technique can be adopted in hybrid driving technique to extract information on the precise again of a pixel, e.g. the actual threshold voltage shift/mismatch of the driving transistor. The light emitting device is turned off during the programming/calibration cycle so that it prevents the unwanted emission and effect of the light emitting device on the pixel aging. This technique can be applied to any current mirror pixel circuit fabricated in any technology including poly silicon, amorphous silicon, crystalline silicon, and organic materials.

[0169] Figure 23 illustrates a mirror based pixel circuit 250 to which a technique for removing OLED from a programming path during a programming cycle is applied. The pixel circuit 250 includes an OLED 251, a storage

capacitor 252, a programming transistor 253, a driving transistor 254, and switch transistors 255 and 256. The gate terminals of the transistors 253 and 254 are connected to IDATA through the switch transistors 255 and 256.

[0170] The transistors 253,254,255 and 256 are n-type TFTs. However, the transistors 253,254,255 and 256 may be p-type TFTs. The OLED removing technique applied to the pixel circuit 250 is also applicable to a pixel circuit having p-type transistors. The transistors 253, 254, 255 and 256 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0171] The transistors 253, 254 and 256 and the storage capacitor 252 are connected at node A10. The transistors 253 and 254, the OLED 251 and the storage capacitor 252 are connected at node B10.

[0172] In the conventional current programming, SEL goes high, and a programming current (IP) is applied to IDATA. Considering that the width of the mirror transistor 253 is "m" times larger than the width of the mirror transistor 254, the current flowing through the OLED 251 during the programming cycle is (m+1)IP. When "m" is large to gain significant speed improvement, the unwanted emission may become considerable.

[0173] By contrast, according to the OLED removing technique, VDD is brought into a lower voltage. This ensures the OLED 251 to be removed from a programming path as shown in Figure 24.

[0174] During a programming cycle, SEL is high and VDD goes to a reference voltage (Vref) in which the OLED 251 is reversely biased. Therefore, the OLED 251 is removed from the current path during the programming cycle.

[0175] During the programming cycle, the pixel circuit 250 may be programmed with scaled current through IDATA without experiencing unwanted emission.

[0176] During the programming cycle, the pixel circuit 250 may be programmed with current and using one of the techniques describe above. The voltage of the IDATA line is read back to extract the threshold voltage of the mirror transistor 253 which is the same as threshold voltage of the driving transistor 254.

[0177] Also, during the programming cycle, the pixel circuit 250 may be programmed with voltage through the IDATA line, using one of the techniques describe above. The current of the IDATA line is read back to extract the threshold voltage of the mirror transistor 253 which is the same as threshold voltage of the driving transistor 254.

[0178] The reference voltage Vref is chosen so that the voltage at node B10 becomes smaller than the ON voltage of the OLED 251. As a result, the OLED 251 turns off and the unwanted emission is zero. The voltage of the IDATA line includes

$$V_P+V_T+\Delta VT \quad ...(3)$$

where V_P includes the drain-source voltage of the driving transistor 254 and the gate-source voltage of the transistor 253, V_T is the threshold voltage of the transistor 253 (254), and ΔVT is the V_T shift/mismatch.

[0179] At the end of the programming cycle, VDD goes to its original value, and so voltage at node B10 goes to the OLED voltage VOLED. At the driving cycle, SEL is low. The gate voltage of the transistor 254/253 is fixed and stored in the storage capacitor 252, since the switch transistors 255 and 256 are off. Therefore, the pixel current during the driving cycle becomes independent of the threshold voltage V_T.

[0180] The OLED removing technique can be adopted in hybrid driving technique to extract the V_T -shift or V_T -mismatch. From (3), if the pixel is programmed with the current, the only variant parameter in the voltage of the IDATA line is the V_T shift/mismatch (ΔVT). Therefore, ΔVT can be extracted and the programming data can be calibrated with ΔVT.

[0181] Figure 25 illustrates an example of a system architecture for implementing the OLED removing technique. A display array 260 includes a plurality of pixel circuits, e.g. pixel circuit 250 of Figure 26. A display controller and scheduler 262 controls and schedules the operation of the display array 260. A driver 264 provides operation voltages to the pixel circuit. The driver provides the operation voltage(s) to the pixel circuit based on instructions/commands from the display controller and scheduler 262 such that the OLED is removed from a programming path of the pixel circuit, as described above.

[0182] The controller and scheduler 262 may include functionality of the display controller and scheduler 64 of Figure 3, or may include functionality of the data process and calibration unit 206 of Figure 16. The system of Figure 25 may have any of these functionalities, the calibration-scheduling described above, the voltage/current extraction described above, or combinations thereof.

[0183] The simulation result for the voltage on IDATA line for different V_T is illustrated in Figure 26. Referring to Figures 23-26, the voltage of the IDATA line includes the shift in the threshold voltage of the transistors 253 and 254. The programming current is 1 μA.

[0184] The unwanted emission is reduced significantly resulting in a higher resolution. Also, individual extraction of circuit aging and light emitting device aging become possible, leading in a more accurate calibration.

[0185] It is noted that each of the transistors shown in Figures 4-8, 14, 20, 21, 23 and 24 can be replaced with a p-type transistor using the concept of complementary circuits.

[0186] All citations are hereby incorporated by reference.

[0187] The present invention has been described with

regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

Claims

1. A system for a display array including a pixel circuit, the pixel circuit (70; 80; 90; 110) including a driving transistor (73; 83; 94; 96), at least one switch transistor (74, 75; 84, 85; 95, 96; 114, 115), a storage capacitor (72; 82; 92; 112) and a light emitting device (71; 81; 91; 111), the system comprising:

a data process unit (64) for controlling the operation of the display array; and
a driver (78; 88; 99; 119) controlled by the data process unit (64) for providing programming data on a data line (76; 86; 97; 117) coupled to the pixel circuit (70; 80; 90; 110);
characterized by
the system further comprising:

a monitor (77, 79; 87, 89; 118, 120) for monitoring a current applied on the data line (76; 86; 97; 117) or a voltage associated with the applied current;
wherein the data process unit (64) is configured to extract information indicative of an aging of the pixel circuit (70; 80; 90; 110), based on the monitored current or voltage, and to control the driver (78; 88; 99; 119) for providing programming and calibration data to the pixel circuit (70; 80; 90; 110) based on the extracted aging information;
wherein the monitor (77, 79; 87, 89; 118, 120) comprises:

a current conveyor (77; 87; 98; 118) for extracting the current of the data line (76; 86; 97; 117) coupled to the pixel circuit (70; 80; 90; 110), the current conveyor (77; 87; 98; 118) including X, Y and Z terminals, the driver (74; 88; 99; 119) applying a programming voltage to the Y terminal, the X terminal being connected to the data line (76; 86; 97; 117) and being forced by feedback to have the same voltage as that of the Y terminal, the current of the X terminal being duplicated to the Z terminal; and a current-controlled voltage source (79; 89; 100; 120) connected to the Z terminal of the current conveyor (77; 87; 98; 118) and adapted to convert the current at the Z terminal into an associated voltage, said associated voltage being provided to the data process unit (64) for extracting a time dependent parameter of the pixel circuit (70; 80; 90; 110), the time dependent parameter including degradation of the light emitting device (71; 81; 91; 111) and/or a threshold shift.

2. The system according to claim 1, wherein the pixel circuit is a current-mirror based pixel circuit (250), the current-mirror based pixel circuit including:

first and second mirror transistors (253, 254), each having a gate terminal, a first terminal and a second terminal;
first and second switch transistors (255, 256), each having a gate terminal, a first terminal and a second terminal;
a storage capacitor (252) having a first terminal and a second terminal; and
a light emitting device (251),
wherein the first terminal of the first mirror transistor (253) is connected to the data line through the first switch transistor (255) and is connected to the first terminal of the storage capacitor (252) through the second switch transistor (256), the second terminal of the first mirror transistor (253) is connected to the second terminal of the storage capacitor (252) and the light emitting device (251), the gate terminals of the first and second mirror transistors (253, 254) are connected to the first terminal of the storage capacitor (252) and are connected to the data line through the first and second switch transistors (255, 256), the first terminal of the second mirror transistor (254) is connected to a voltage supply line, the second terminal of the second mirror transistor (254) is connected to the second terminal of the storage capacitor (252) and the light emitting device (251).

3. The system according to claim 1, wherein the data process unit (64) is configured to determine a state of the pixel circuit (70; 80; 90; 110) based on a comparison between the monitored current or voltage and an expected value, and wherein the data process unit (64) is configured to estimate a threshold voltage of the driving transistor (73; 83; 94; 96) based on the determined state of the pixel circuit (70; 80; 90; 110) or based on the determined state of the pixel circuit (70; 80; 90; 110) and a resolution of the driver (78; 88; 99; 119).

4. The system according to claim 3, wherein a programming voltage provided to the pixel circuit (70; 80; 90; 110) is determined based on a programming data and the estimated threshold voltage.

5. The system according to any of claims 1, 3 and 4, wherein the pixel circuit (160) includes first and second switch transistors (164, 165),
each of the driving transistor (163), the first switch transistor (164) and the second switch transistor (165) including a gate terminal, a first terminal and a second terminal,
the gate terminal of the driving transistor (163) being connected to a signal line through the first switch transistor (164) and being connected at a first terminal of the storage capacitor (162), the first terminal of the driving transistor (163) being connected to the light emitting device (161) and being connected to a monitor line through the second switch transistor (165), the monitor (77, 79; 87, 89; 118, 120) being coupled to the monitor line, the monitor (77, 79; 87, 89; 118, 120) being configured to sense the current or voltage through the monitor line,
the gate terminal of the first switch transistor (164) being connected to a first select line, the gate terminal of the second switch transistor (165) being connected to the first select line or a second select line.

6. The system according to any of claims 1 to 5, wherein the data process unit (64) is further configured to predict a shift in an operating voltage of the light emitting device (71; 81; 91; 111), based on the monitored current or voltage, the system further comprising: a circuit for providing, to the light emitting device (71; 81; 91; 111), a bias associated with the predicted shift in the operating voltage of the light emitting device (71; 81; 91; 111).

7. A method of driving a display array, the display array including a pixel circuit (70; 80; 90; 110), the pixel circuit (70; 80; 90; 110) including a driving transistor (73; 83; 94; 96), at least one switch transistor (74, 75; 84, 85; 95, 96; 114, 115), a storage capacitor (72; 82; 92; 112) and a light emitting device (71; 81; 91; 111), the method comprising:

applying a current or voltage on a data line coupled to the pixel circuit (70; 80; 90; 110);
monitoring the applied current or a voltage associated with the applied current by a monitor comprising: a current conveyor (77; 87; 98; 118) for extracting the current of the data line (76; 86; 97; 117) coupled to the pixel circuit (70; 80; 90; 110), the current conveyor (77; 87; 98; 118) including X, Y and Z terminals, the driver (74; 88; 99; 119) applying a programming voltage to the Y terminal, the X terminal being connected to the data line (76; 86; 97; 117) and being forced by feedback to have the same voltage as that of the Y terminal, the current of the X terminal being duplicated to the Z terminal; and a current-controlled voltage source (79; 89; 100; 120) connected to the Z terminal of the current conveyor (77; 87; 98; 118) and adapted to convert the current at the Z terminal into an associated voltage, said associated voltage being provided to a data process unit (64) for extracting a time dependent parameter of the pixel circuit (70; 80; 90; 110), the time dependent parameter including degradation of the light emitting device (71; 81; 91; 111) and/or a threshold shift. extracting the time dependent parameter as information indicative of an aging of the pixel circuit (70; 80; 90; 110), based on the monitored current or voltage; and
programming the pixel circuit (70; 80; 90; 110) to emit light according to programming and calibration data based on the extracted aging information.

8. The method according to claim 7, further comprising determining a state of the pixel circuit (70; 80; 90; 110) based on the extracted aging information, and wherein the programming is carried out based on the determined state.

9. The method according to claim 8, wherein the extracting includes estimating a threshold voltage of the driving transistor (73; 83; 94; 96) based on the determined state of the pixel circuit (70; 80; 90; 110) or based on the determined state of the pixel circuit (70; 80; 90; 110) and a resolution of a driver (78; 88; 99; 119) configured to program the pixel circuit (70; 80; 90; 110).

10. The method according to any of claims 7 to 9, further comprising:

predicting a shift in an operating voltage of the light emitting device (71; 81; 91; 111), based on the monitored current or voltage; and
providing, to the light emitting device (71; 81; 91; 111), a bias associated with the shift in the voltage of the light emitting device (71; 81; 91; 111).

11. The system according to claim 1, the system comprising:

the pixel circuit (70; 80; 90; 110), the driving transistor (73; 83; 94; 96) driving current through the light emitting device (71; 81; 91; 111) according to a driving voltage on a gate terminal of the driving transistor (73; 83; 94; 96); and
a voltage supply line connected to the pixel circuit (70; 80; 90; 110) for reverse biasing the light emitting device (71; 81; 91; 111) by adjusting the voltage supply line to a reference voltage during a programming operation cycle, thereby removing the light emitting device (71; 81; 91; 111) from a programming path of the applied current or volta-ge, wherein

the driver (78; 88; 99; 119) is adapted to program the pixel circuit (70; 80; 90; 110) by applying the current or voltage to the data line (76; 86; 97; 117) connected to the pixel circuit (70; 80; 90; 110), and
the data process unit (64) is adapted to control: (i) the voltage of the voltage supply line, and (ii) the current or voltage applied by the driver (78; 88; 99; 119), the data process unit (64) being configured to adjust the voltage supply line to an original voltage following the programming of the pixel.

12. The system according to claim 11, wherein the pixel circuit (70; 80; 90; 110) is a current mirror pixel circuit (70; 80; 90; 110), the pixel circuit (70; 80; 90; 110) comprising:

a mirror transistor having a gate terminal connected to the gate terminal of the driving transistor (73; 83; 94; 96);
a storage capacitor (72; 82; 92; 112) for being charged with the driving voltage responsive to a programming current flowing through the mirror transistor, the programming current being provided via the data line (76; 86; 97; 117);
a first switching transistor for connecting the pixel circuit (70; 80; 90; 110) to the data line (76; 86; 97; 117) during a programming operation cycle and disconnecting the pixel circuit (70; 80; 90; 110) from the data line (76; 86; 97; 117) during an emission operation cycle, the first switching transistor being connected between the data line (76; 86; 97; 117) and the mirror transistor; and
a second switching transistor for connecting the gate terminals of the mirror transistor and the driving transistor (73; 83; 94; 96) to the data line (76; 86; 97; 117) during a programming operation cycle, the second switching transistor having a gate terminal connected to a gate terminal of the first switching transistor and a common select line.

13. The system or method according to any of claims 1 to 12, wherein the light emitting device (71; 81; 91; 111) is an organic light emitting diode and wherein the display array is an AMOLED display array.

14. The system or method according to any of claims 1 to 13, wherein at least one of the transistors is an n-type or p-type thin film transistor.

Patentansprüche

1. System für eine Anzeigeanordnung die eine Pixelschaltung umfasst, wobei die Pixelschaltung (70; 80; 90; 110) einen Treibertransistor (73; 83; 94; 96), wenigstens einen Schalttransistor (74, 75; 84, 85; 95, 96; 114, 115), einen Speicherkondensator (72; 82; 92; 112) und eine lichtemittierende Vorrichtung (71; 81; 91; 111) beinhaltet, wobei das System umfasst:

eine Datenverarbeitungseinheit (64) zum Steuern des Betriebs der Anzeigeanordnung; und
einen Treiber (78; 88; 99; 119), der von der Datenverarbeitungseinheit (64) gesteuert wird, um Programmierdaten auf einer Datenleitung (76; 86; 97; 117) bereitzustellen, die mit der Pixelschaltung (70; 80; 90; 110) gekoppelt ist;
dadurch gekennzeichnet, dass das System weiterhin umfasst:

einen Monitor (77, 79; 87, 89; 118, 120) zum Überwachen eines Stroms, der an die Datenleitung (76; 86; 97; 117) angelegt wird, oder einer Spannung, die mit dem angelegten Strom assoziiert ist;
wobei die Datenverarbeitungseinheit (64) dazu eingerichtet ist, Informationen zu extrahieren, die eine Alterung der Pixelschaltung (70; 80; 90; 110) auf der Grundlage des überwachten Stroms oder der überwachten Spannung anzeigen, und den Treiber (78; 88; 99; 119) zum Bereitstellen von Programmier- und Kalibrierungsdaten für die Pixelschaltung (70; 80; 90; 110) basierend auf den extrahierten Alterungsinformationen zu steuern;
wobei der Monitor (77, 79; 87, 89; 118, 120) umfasst:

einen Stromförderer (77; 87; 98; 118) zum Extrahieren des Stroms aus der mit der Pixelschaltung (70; 80; 90; 110) gekoppelten Datenleitung (76; 86; 97; 117), wobei der Stromförderer (77; 87, 98; 118) X-, Y- und Z-Anschlüsse umfasst, der Treiber (74; 88; 99; 119) eine Programmierspannung an den Y-Anschluss anlegt, der X-Anschluss mit der Datenleitung (76; 86; 97; 117) verbunden ist, und durch Rückkopplung gezwungen wird, dieselbe Spannung wie die des Y-Anschlusses zu haben, wobei der Strom des X-Anschlusses zu dem Z-Anschluss dupliziert wird; und
eine stromgesteuerte Spannungsquelle (79; 89; 100; 120), die mit dem Z-Anschluss des Stromförderers (77; 87; 98; 118) verbunden ist und den Strom an dem Z-Anschluss in eine zugehörige Spannung umwandeln kann, wobei diese zugehörige Spannung der Datenverarbeitungseinheit (64) bereitge-

stellt wird, um einen zeitabhängigen Parameter der Pixelschaltung (70; 80; 90; 110) zu extrahieren, wobei der zeitabhängige Parameter eine Verschlechterung der lichtemittierenden Vorrichtung (71; 81; 91; 111) und/oder eine Schwellenwertverschiebung umfasst.

2. System nach Anspruch 1, bei dem die Pixelschaltung eine stromspiegel-basierte Pixelschaltung (250) ist, wobei die stromspiegel-basierte Pixelschaltung umfasst:

erste und zweite Spiegeltransistoren (253, 254), die jeweils einen Gate-Anschluss, einen ersten Anschluss und einen zweiten Anschluss aufweisen;
erste und zweite Schalttransistoren (255, 256), die jeweils einen Gate-Anschluss, einen ersten Anschluss und einen zweiten Anschluss aufweisen;
einen Speicherkondensator (252) mit einem ersten Anschluss und einem zweiten Anschluss;
und eine lichtemittierende Vorrichtung (251),
wobei der erste Anschluss des ersten Spiegeltransistors (253) über den ersten Schalttransistor (255) mit der Datenleitung verbunden ist und über den zweiten Schalttransistor (256) mit dem ersten Anschluss des Speicherkondensators (252) verbunden ist, der zweite Anschluss des ersten Spiegeltransistors (253) mit dem zweiten Anschluss des Speicherkondensators (252) und der lichtemittierenden Vorrichtung (251) verbunden ist, die Gate-Anschlüsse des ersten und des zweiten Spiegeltransistors (253, 254) mit dem ersten Anschluss des Speicherkondensators (252) verbunden sind und über den ersten und zweiten Schalttransistor (255, 256) an die Datenleitung angeschlossen sind, der erste Anschluss des zweiten Spiegeltransistors (254) an eine Spannungsversorgungsleitung angeschlossen ist und der zweite Anschluss des zweiten Spiegeltransistors (254) mit dem zweiten Anschluss des Speicherkondensators (252) und der lichtemittierenden Vorrichtung (251) verbunden ist.

3. System nach Anspruch 1, bei dem die Datenverarbeitungseinheit (64) dazu eingerichtet ist, einen Zustand der Pixelschaltung (70; 80; 90; 110) basierend auf einem Vergleich zwischen dem überwachten Strom oder der Spannung und einem erwarteten Wert zu bestimmen, und die Datenverarbeitungseinheit (64) dazu eingerichtet ist, eine Schwellenspannung des Treibertransistors (73; 83; 94; 96) auf der Grundlage des bestimmten Zustands der Pixelschaltung (70; 80; 90; 110) oder auf der Grundlage des bestimmten Zustands der Pixelschaltung (70; 80; 90; 110) und einer Auflösung des Treibers (78; 88; 99; 119) zu schätzen.

4. System nach Anspruch 3, bei dem eine Programmierspannung, die der Pixelschaltung (70; 80; 90; 110) bereitgestellt wird, auf der Grundlage von Programmierdaten und der geschätzten Schwellenspannung bestimmt wird.

5. System nach einem der Ansprüche 1, 3 und 4, bei dem die Pixelschaltung (160) erste und zweite Schalttransistoren (164, 165) umfasst,
wobei jeder des Treibertransistors (163), des ersten Schalttransistors (164) und des zweiten Schalttransistors (165) einen Gate-Anschluss, einen ersten Anschluss und einen zweiten Anschluss aufweisen,
wobei der Gate-Anschluss des Treibertransistors (163) über den ersten Schalttransistor (164) mit einer Signalleitung verbunden ist und an einem ersten Anschluss des Speicherkondensators (162) angeschlossen ist, der erste Anschluss des Treibertransistors (163) mit der lichtemittierenden Vorrichtung (161) verbunden ist und über den zweiten Schalttransistor (165) mit einer Überwachungsleitung verbunden ist, der Monitor (77, 79; 87, 89; 118, 120) mit der Monitorleitung verbunden ist und der Monitor (77, 79; 87, 89; 118, 120) dazu eingerichtet ist, den Strom oder die Spannung durch die Überwachungsleitung zu erfassen,
wobei der Gate-Anschluss des ersten Schalttransistors (164) mit einer ersten Auswahlleitung verbunden ist und der Gate-Anschluss des zweiten Schalttransistors (165) mit der ersten Auswahlleitung oder einer zweiten Auswahlleitung verbunden ist.

6. System nach einem der Ansprüche 1 bis 5, bei dem die Datenverarbeitungseinheit (64) weiterhin dazu eingerichtet ist, eine Verschiebung einer Betriebsspannung der lichtemittierenden Vorrichtung (71; 81; 91; 111) auf der Grundlage des überwachten Stroms oder der überwachten Spannung vorherzusagen, wobei das System ferner umfasst:

eine Schaltung zum Bereitstellen einer mit der vorhergesagten Verschiebung der Betriebsspannung der lichtemittierenden Vorrichtung (71; 81; 91; 111) verbundenen Vorspannung für die lichtemittierende Vorrichtung (71; 81; 91; 111).

7. Verfahren zum Ansteuern einer Anzeigeanordnung, bei dem die Anzeigeanordnung eine Pixelschaltung (70; 80; 90; 110) umfasst, wobei die Pixelschaltung (70; 80; 90; 110) einen Treibertransistor (73; 83; 94; 96), wenigstens einen Schalttransistor (74, 75; 84, 85; 95, 96; 114, 115), einen Speicherkondensator (72; 82; 92; 112) und eine lichtemittierende Vorrich-

tung (71; 81; 91; 111) aufweist, wobei das Verfahren umfasst:

Anlegen eines Stroms oder einer Spannung an eine Datenleitung, die mit der Pixelschaltung (70; 80; 90; 110) gekoppelt ist;
Überwachen des angelegten Stroms oder einer Spannung, die mit dem angelegten Strom assoziiert ist, durch einen Monitor der umfasst: einen Stromförderer (77; 87; 98; 118) zum Extrahieren des Stroms aus der mit der Pixelschaltung (70; 80; 90; 110) gekoppelten Datenleitung (76; 86; 97; 117), wobei der Stromförderer (77; 87, 98; 118) X-, Y- und Z-Anschlüsse umfasst, der Treiber (74; 88; 99; 119) eine Programmierspannung an den Y-Anschluss anlegt, der X-Anschluss mit der Datenleitung (76; 86; 97; 117) verbunden ist, und durch Rückkopplung gezwungen wird, dieselbe Spannung wie die des Y-Anschlusses zu haben, wobei der Strom des X-Anschlusses zu dem Z-Anschluss dupliziert wird; und eine stromgesteuerte Spannungsquelle (79; 89; 100; 120), die mit dem Z-Anschluss des Stromförderers (77; 87; 98; 118) verbunden ist und den Strom an dem Z-Anschluss in eine zugehörige Spannung umwandeln kann, wobei diese zugehörige Spannung der Datenverarbeitungseinheit (64) bereitgestellt wird, um einen zeitabhängigen Parameter der Pixelschaltung (70; 80; 90; 110) zu extrahieren, wobei der zeitabhängige Parameter eine Verschlechterung der lichtemittierenden Vorrichtung (71; 81; 91; 111) und/oder eine Schwellenwertverschiebung umfasst,
Extrahieren des zeitabhängigen Parameters als Informationen, die eine Alterung der Pixelschaltung (70; 80; 90; 110) basierend auf dem überwachten Strom oder der überwachten Spannung anzeigen; und
Programmieren der Pixelschaltung (70; 80; 90; 110) zum Emittieren von Licht gemäß Programmier- und Kalibrierungsdaten basierend auf den extrahierten Alterungsinformationen.

8. Verfahren nach Anspruch 7, weiterhin umfassend das Bestimmen eines Zustands der Pixelschaltung (70; 80; 90; 110) auf der Grundlage der extrahierten Alterungsinformationen, und wobei das Programmieren auf der Grundlage des bestimmten Zustands ausgeführt wird.

9. Verfahren nach Anspruch 8, bei dem das Extrahieren das Schätzen einer Schwellenspannung des Treibertransistors (73; 83; 94; 96) basierend auf dem bestimmten Zustand der Pixelschaltung (70; 80; 90; 110) oder basierend auf dem bestimmten Zustand der Pixelschaltung (70; 80; 90; 110) und einer Auflösung eines Treibers (78; 88; 99; 119) umfasst, der dazu eingerichtet ist, die Pixelschaltung (70; 80; 90; 110) zu programmieren.

10. Verfahren nach einem der Ansprüche 7 bis 9, weiterhin umfassend:

Vorhersagen einer Verschiebung einer Betriebsspannung der lichtemittierenden Vorrichtung (71; 81; 91; 111) basierend auf dem überwachten Strom oder der überwachten Spannung;und
Bereitstellen einer mit der Verschiebung der Spannung der lichtemittierenden Vorrichtung (71; 81; 91; 111) verbundenen Vorspannung für die lichtemittierende Vorrichtung (71; 81; 91; 111).

11. System nach Anspruch 1, wobei das System umfasst:

die Pixelschaltung (70; 80; 90; 110), wobei der Treibertransistor (73; 83; 94; 96) Strom durch die lichtemittierende Vorrichtung (71; 81; 91; 111) gemäß einer Treiberspannung an einem Gate-Anschluss des Treibertransistors (73; 83; 94; 96) treibt; und
eine Spannungsversorgungsleitung, die mit der Pixelschaltung (70; 80; 90; 110) verbunden ist, um die lichtemittierende Vorrichtung (71; 81; 91; 111) umgekehrt vorzuspannen, indem die Spannungsversorgungsleitung während eines Programmierbetriebszyklus auf eine Referenzspannung eingestellt wird, wodurch die lichtemittierende Vorrichtung (71; 81; 91; 111) aus einem Programmierpfad des angelegten Stroms oder angelegten Spannung entfernt wird, wobei
der Treiber (78; 88; 99; 119) dazu eingerichtet ist, die Pixelschaltung (70; 80; 90; 110) durch Anlegen des Stroms oder der Spannung an die mit der Pixelschaltung (70; 80; 90; 110) verbundene Datenleitung (76; 86; 97; 117) zu programmieren, und
die Datenverarbeitungseinheit (64) dazu eingerichtet ist: (i) die Spannung der Spannungsversorgungsleitung und (ii) den Strom oder die Spannung, die von dem Treiber (78; 88; 99; 119) angelegt werden zu steuern, und die Datenverarbeitungseinheit (64) dazu eingerichtet ist, die Spannungsversorgungsleitung nach der Programmierung des Pixels an eine ursprüngliche Spannung anzupassen.

12. System nach Anspruch 11, bei dem die Pixelschaltung (70; 80; 90; 110) eine Stromspiegel-Pixelschaltung (70; 80; 90; 110) ist, wobei die Pixelschaltung (70; 80; 90; 110) umfasst:

einen Spiegeltransistor mit einem Gate-Anschluss, der mit dem Gate-Anschluss des Treibertransistors (73; 83; 94; 96) verbunden ist;
einen Speicherkondensator (72; 82; 92; 112), der mit der Treiberspannung in Abhängigkeit von einem Programmierstrom zu laden ist, der durch den Spiegeltransistor fließt, wobei der Programmierstrom über die Datenleitung (76; 86; 97; 117) bereitgestellt wird;
einen ersten Schalttransistor zum Verbinden der Pixelschaltung (70; 80; 90; 110) mit der Datenleitung (76; 86; 97; 117) während eines Programmiervorgangszyklus' und Trennen der Pixelschaltung (70; 80; 90; 110) von der Datenleitung (76; 86; 97; 117) während eines Sendebetriebszyklus', wobei der erste Schalttransistor zwischen die Datenleitung (76; 86; 97; 117) und den Spiegeltransistor geschaltet ist; und
einen zweiten Schalttransistor zum Verbinden der Gate-Anschlüsse des Spiegeltransistors und des Treibertransistors (73; 83; 94; 96) mit der Datenleitung (76; 86; 97; 117) während eines Programmiervorgangszyklus', wobei der zweite Schalttransistor einen Gate-Anschluss hat, der mit einem Gate-Anschluss des ersten Schalttransistors und einer gemeinsamen Auswahlleitung verbunden ist.

13. System oder Verfahren nach einem der Ansprüche 1 bis 12, bei dem die lichtemittierende Vorrichtung (71; 81; 91; 111) eine organische lichtemittierende Diode ist und die Anzeigeanordnung eine AMOLED-Anzeigeanordnung ist.

14. System oder Verfahren nach einem der Ansprüche 1 bis 13, wobei wenigstens einer der Transistoren ein Dünnfilmtransistor vom n-Typ oder p-Typ ist.

Revendications

1. Système pour une matrice d'affichage comprenant un circuit de pixel, le circuit de pixel (70 ; 80 ; 90 ; 110) incluant un transistor de commande (73 ; 83 ; 94 ; 96), au moins un transistor de commutation (74, 75 ; 84, 85 ; 95, 96 ; 114, 115), un condensateur de stockage (72 ; 82 ; 92 ; 112) et un dispositif électroluminescent (71 ; 81 ; 91 ; 111), le système comprenant :

une unité de traitement de données (64) pour le contrôle du fonctionnement de la matrice d'affichage ; et
un pilote (78 ; 88 ; 99 ; 119) contrôlé par l'unité de traitement de données (64) pour la mise à disposition de données de programmation sur une ligne de données (76 ; 86 ; 97 ; 117) couplée au circuit de pixel (70 ; 80 ; 90 ; 110) ;

caractérisé par
le système comprenant en outre :

un moniteur (77, 79 ; 87, 89 ; 118, 120) pour la surveillance d'un courant appliqué à la ligne de données (76 ; 86 ; 97 ; 117) ou d'une tension associée au courant appliqué ;
dans lequel l'unité de traitement de données (64) est configurée pour extraire des informations indicatives d'un vieillissement du circuit de pixel (70 ; 80 ; 90 ; 110), en fonction du courant ou de la tension surveillé, et pour contrôler le pilote (78 ; 88 ; 99 ; 119) pour mettre des données de programmation et d'étalonnage à la disposition du circuit de pixel (70 ; 80 ; 90 ; 110) en fonction des informations de vieillissement extraites ;
dans lequel le moniteur (77, 79 ; 87, 89 ; 118, 120) comprend :

un convoyeur de courant (77 ; 87 ; 98 ; 118) pour l'extraction du courant de la ligne de données (76 ; 86 ; 97 ; 117) couplé au circuit de pixel (70 ; 80 ; 90 ; 110), le convoyeur de courant (77 ; 87 ; 98 ; 118) incluant des bornes X, Y et Z, le pilote (74 ; 88 ; 99 ; 119) appliquant une tension de programmation à la borne Y, la borne X étant connectée à la ligne de données (76 ; 86 ; 97 ; 117) et étant contrainte par rétroaction de présenter la même tension que celle de la borne Y, le courant de la borne X étant dupliqué vers la borne Z ; et
une source de tension à contrôle de courant (79 ; 89 ; 100 ; 120) connectée à la borne Z du convoyeur de courant (77 ; 87 ; 98 ; 118) et adaptée pour convertir le courant au niveau de la borne Z en une tension associée, une dite tension associée étant fournie à l'unité de traitement de données (64) pour l'extraction d'un paramètre dépendant du temps du circuit de pixel (70 ; 80 ; 90 ; 110), le paramètre dépendant du temps incluant une dégradation du dispositif électroluminescent (71 ; 81 ; 91 ; 111) et/ou un déplacement de seuil.

2. Le système selon la revendication 1, dans lequel le circuit de pixel est un circuit de pixel en miroir de courant (250), le circuit de pixel en miroir de courant incluant :

un premier et un deuxième transistors miroir (253, 254), chacun disposant d'une borne en

grille, d'une première borne et d'une deuxième borne ;
un premier et un deuxième transistors de commutation (255, 256), chacun disposant d'une borne en grille, d'une première borne et d'une deuxième borne ;
un condensateur de stockage (252) disposant d'une première borne et d'une deuxième borne ; et
un dispositif électroluminescent (251),
dans lequel la première borne du premier transistor miroir (253) est connectée à la ligne de données via le premier transistor de commutation (255) et est connectée à la première borne du condensateur de stockage (252) via le deuxième transistor de commutation (256), la deuxième borne du premier transistor miroir (253) est connectée à la deuxième borne du condensateur de stockage (252) et au dispositif électroluminescent (251), les bornes en grille du premier et du deuxième transistors miroir (253, 254) sont connectées à la première borne du condensateur de stockage (252) et sont connectées à la ligne de données via le premier et le deuxième transistors de commutation (255, 256), la première borne du deuxième transistor miroir (254) est connectée à une ligne d'alimentation en tension, la deuxième borne du deuxième transistor miroir (254) est connectée à la deuxième borne du condensateur de stockage (252) et au dispositif électroluminescent (251).

3. Le système selon la revendication 1, dans lequel l'unité de traitement de données (64) est configurée pour déterminer un état du circuit de pixel (70 ; 80 ; 90 ; 110) en fonction d'une comparaison entre le courant ou la tension surveillé et une valeur attendue, et dans lequel l'unité de traitement de données (64) est configurée pour estimer une tension de seuil du transistor de commande (73 ; 83 ; 94 ; 96) en fonction de l'état déterminé du circuit de pixel (70 ; 80 ; 90 ; 110) ou en fonction de l'état déterminé du circuit de pixel (70 ; 80 ; 90 ; 110) et d'une résolution du pilote (78 ; 88 ; 99 ; 119).

4. Le système selon la revendication 3, dans lequel une tension de programmation fournie au circuit de pixel (70 ; 80 ; 90 ; 110) est déterminée en fonction de données de programmation et de la tension de seuil estimée.

5. Le système selon une des revendications 1, 3 et 4, dans lequel le circuit de pixel (160) comprend un premier et un deuxième transistors de commutation (164, 165),
chacun du transistor de commande (163), du premier transistor de commutation (164) et du deuxième transistor de commutation (165) comprenant une borne en grille, une première borne et une deuxième borne,
la borne en grille du transistor de commande (163) étant connectée à une ligne de signal via le premier transistor de commutation (164) et étant connecté à une première borne du condensateur de stockage (162), la première borne du transistor de commande (163) étant connectée au dispositif électroluminescent (161) et étant connectée à une ligne de moniteur via le deuxième transistor de commutation (165), le moniteur (77, 79 ; 87, 89 ; 118, 120) étant couplé à la ligne de moniteur, le moniteur (77, 79 ; 87, 89 ; 118, 120) étant configuré pour détecter le courant ou la tension via la ligne de moniteur,
la borne en grille du premier transistor de commutation (164) étant connectée à une première ligne de sélection, la borne en grille du deuxième transistor de commutation (165) étant connectée à la première ligne de sélection ou à une deuxième ligne de sélection.

6. Le système selon une des revendications 1 à 5, dans lequel l'unité de traitement de données (64) est configurée en outre pour prévoir un changement dans une tension d'exploitation du dispositif électroluminescent (71 ; 81 ; 91 ; 111), en fonction du courant ou de la tension surveillé, le système comprenant en outre :

un circuit pour mettre à la disposition du dispositif électroluminescent (71 ; 81 ; 91 ; 111), une polarisation associée au changement prévu dans la tension d'exploitation du dispositif électroluminescent (71 ; 81 ; 91 ; 111).

7. Procédé pour commander une matrice d'affichage, la matrice d'affichage comprenant un circuit de pixel (70 ; 80 ; 90 ; 110), le circuit de pixel (70 ; 80 ; 90 ; 110) incluant un transistor de commande (73 ; 83 ; 94 ; 96), au moins un transistor de commutation (74, 75 ; 84, 85 ; 95, 96 ; 114, 115), un condensateur de stockage (72 ; 82 ; 92 ; 112) et un dispositif électroluminescent (71 ; 81 ; 91 ; 111), le procédé comprenant :

l'application d'un courant ou d'une tension à une ligne de données couplée au circuit de pixel (70 ; 80 ; 90 ; 110) ;
la surveillance du courant appliqué ou d'une tension associée au courant appliqué par un moniteur comprenant :

un convoyeur de courant (77 ; 87 ; 98 ; 118) pour l'extraction du courant de la ligne de données (76 ; 86 ; 97 ; 117) couplé au circuit de pixel (70 ; 80 ; 90 ; 110), le convoyeur de courant (77 ; 87 ; 98 ; 118) incluant des bornes X, Y et Z, le pilote (74 ;

88 ; 99 ; 119) appliquant une tension de programmation à la borne Y, la borne X étant connectée à la ligne de données (76 ; 86 ; 97 ; 117) et étant contrainte par rétroaction de présenter la même tension que celle de la borne Y,
le courant de la borne X étant dupliqué vers la borne Z ; et une source de tension à contrôle de courant (79 ; 89 ; 100 ; 120) connectée à la borne Z du convoyeur de courant (77 ; 87 ; 98 ; 118) et adaptée pour convertir le courant au niveau de la borne Z en une tension associée, une dite tension associée étant fournie à l'unité de traitement de données (64) pour l'extraction d'un paramètre dépendant du temps du circuit de pixel (70 ; 80 ; 90 ; 110), le paramètre dépendant du temps incluant une dégradation du dispositif électroluminescent (71 ; 81 ; 91 ; 111) et/ou un déplacement de seuil.

l'extraction du paramètre dépendant du temps en tant qu'informations indicatives d'un vieillissement du circuit de pixel (70 ; 80 ; 90 ; 110), en fonction du courant ou de la tension surveillé ; et
la programmation du circuit de pixel (70 ; 80 ; 90 ; 110) pour émettre une lumière en fonction de données de programmation et d'étalonnage reposant sur les informations de vieillissement extraites.

8. Le procédé selon la revendication 7, comprenant en outre la détermination d'un état du circuit de pixel (70 ; 80 ; 90 ; 110) en fonction des informations de vieillissement extraites, et dans lequel la programmation s'effectue en fonction de l'état déterminé.

9. Le procédé selon la revendication 8, dans lequel l'extraction comprend une tension de seuil du transistor de commande (73 ; 83 ; 94 ; 96) reposant sur l'état déterminé du circuit de pixel (70 ; 80 ; 90 ; 110) ou reposant sur l'état déterminé du circuit de pixel (70 ; 80 ; 90 ; 110) et une résolution d'un pilote (78 ; 88 ; 99 ; 119) configuré pour programmer le circuit de pixel (70 ; 80 ; 90 ; 110).

10. Le procédé selon une des revendications 7 à 9, comprenant en outre :

la prévision d'un changement dans une tension d'exploitation du dispositif électroluminescent (71 ; 81 ; 91 ; 111), en fonction du courant ou de la tension surveillé ; et
la mise à la disposition du circuit du dispositif électroluminescent (71 ; 81 ; 91 ; 111), d'une polarisation associée au changement prévu dans la tension du dispositif électroluminescent (71 ; 81 ; 91 ; 111).

11. Le système selon la revendication 1, le système comprenant :

le circuit de pixel (70 ; 80 ; 90 ; 110), le transistor de commande (73 ; 83 ; 94 ; 96) pilotant un courant à travers le dispositif électroluminescent (71; 81; 91 ; 111) en fonction d'une tension de pilotage sur une borne en grille du transistor de commande (73 ; 83 ; 94 ; 96) ; et
une ligne d'alimentation en tension connectée au circuit de pixel (70 ; 80 ; 90 ; 110) pour inverser la polarisation du dispositif électroluminescent (71 ; 81 ; 91 ; 111) en ajustant la ligne d'alimentation en tension sur une tension de référence pendant un cycle d'opération de programmation, retirant ainsi le dispositif électroluminescent (71 ; 81 ; 91 ; 111) d'une voie de programmation du courant ou de la tension appliqué, dans lequel le pilote (78 ; 88 ; 99 ; 119) est adapté pour programmer le circuit de pixel (70 ; 80 ; 90 ; 110) en appliquant le courant ou la tension à la ligne de données (76 ; 86 ; 97 ; 117) connectée au circuit de pixel (70 ; 80 ; 90 ; 110), et l'unité de traitement de données (64) est adaptée pour contrôler : (i) la tension de la ligne d'alimentation en tension, et (ii) le courant ou la tension appliqué au pilote (78 ; 88 ; 99 ; 119), l'unité de traitement de données (64) étant configurée pour ajuster la ligne d'alimentation en tension à une tension originale suivant la programmation du pixel.

12. Le système selon la revendication 11, dans lequel le circuit de pixel (70 ; 80 ; 90 ; 110) est un circuit de pixel en miroir de courant (70 ; 80 ; 90 ; 110), le circuit de pixel (70 ; 80 ; 90 ; 110) comprenant :

un transistor miroir disposant d'une borne en grille connectée à la borne en grille du transistor de commande (73 ; 83 ; 94 ; 96) ;
un condensateur de stockage (72 ; 82 ; 92 ; 112) destiné à être chargé avec la tension de pilotage réactive à un courant de programmation traversant le transistor miroir, le courant de programmation étant fourni via la ligne de données (76 ; 86 ; 97 ; 117) ;
un premier transistor de commutation pour la connexion du circuit de pixel (70 ; 80 ; 90 ; 110) à la ligne de données (76 ; 86 ; 97 ; 117) pendant un cycle d'opération de programmation et la déconnexion du circuit de pixel (70 ; 80 ; 90 ; 110) de la ligne de données (76 ; 86 ; 97 ; 117) pendant un cycle d'opération d'émission, le premier transistor de commutation étant connecté entre la ligne de données (76 ; 86 ; 97 ; 117) et le transistor miroir ; et

un deuxième transistor de commutation pour la connexion des bornes en grille du transistor miroir et du transistor de commande (73 ; 83 ; 94 ; 96) à la ligne de données (76 ; 86 ; 97 ; 117) pendant un cycle d'opération de programmation, le deuxième transistor de commutation présentant une borne en grille connectée à une borne en grille du premier transistor de commutation et à une ligne de sélection commune.

13. Le système ou procédé selon une des revendications 1 à 12, dans lequel le dispositif électroluminescent (71 ; 81 ; 91 ; 111) est une diode électroluminescente organique et dans lequel la matrice d'affichage est une matrice d'affichage AMOLED.

14. Le système ou procédé selon une des revendications 1 à 13, dans lequel au moins un des transistors est un transistor à couche mince de type n ou de type p.

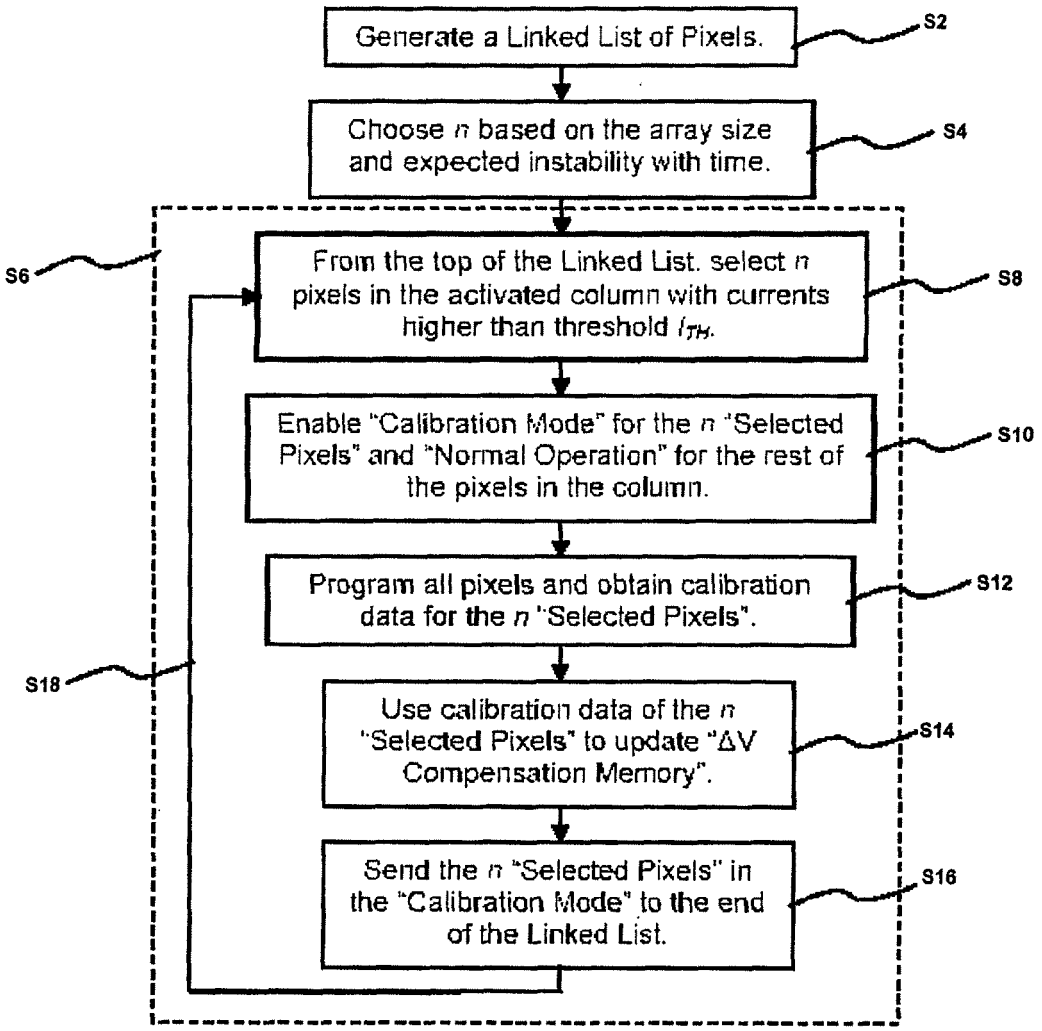
Generate a Linked List of Pixels.
S2
Choose n based on the array size and expected instability with time.
S4
S6
From the top of the Linked List, select n pixels in the activated column with currents higher than threshold I_{TH}.
S8
Enable "Calibration Mode" for the n "Selected Pixels" and "Normal Operation" for the rest of the pixels in the column.
S10
Program all pixels and obtain calibration data for the n "Selected Pixels".
S12
S18
Use calibration data of the n "Selected Pixels" to update "ΔV Compensation Memory".
S14
Send the n "Selected Pixels" in the "Calibration Mode" to the end of the Linked List.
S16

FIG.1

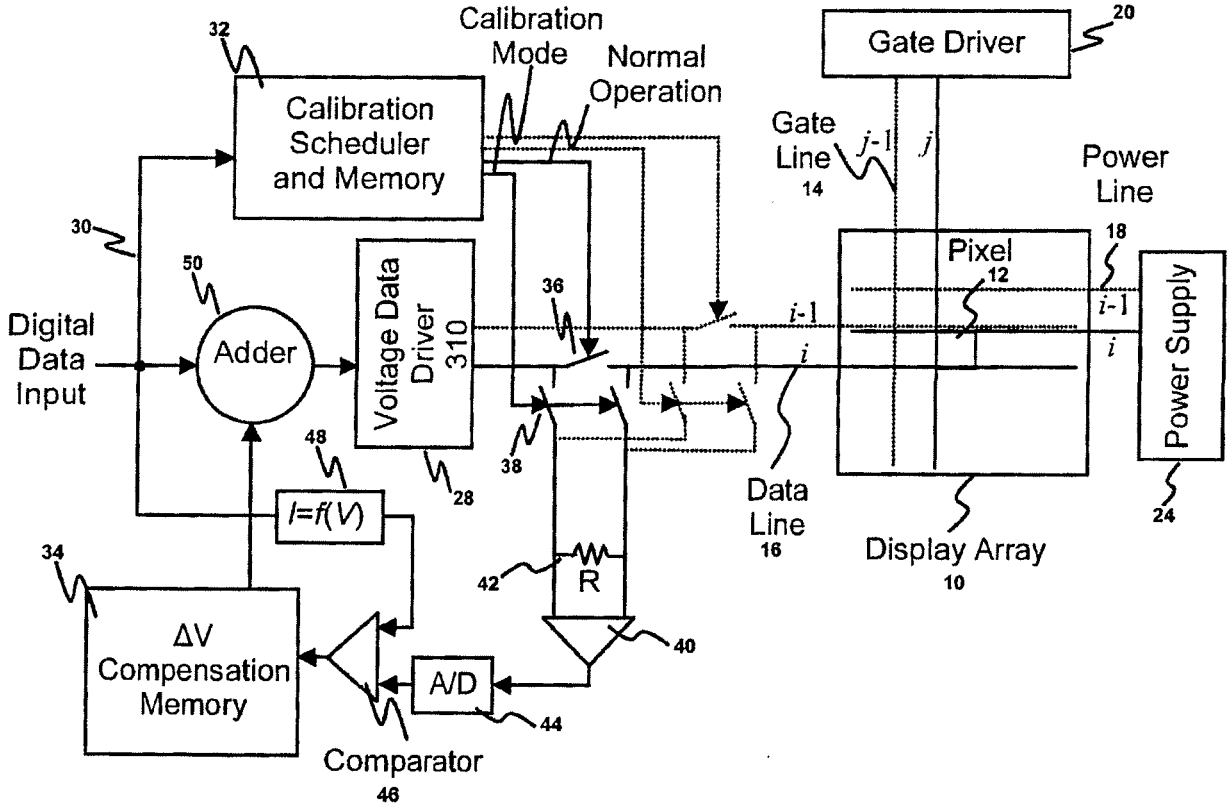
32
Calibration
Mode
Normal
Operation
Calibration
Scheduler
and Memory
Gate Driver
20
Gate
Line
14
j-1
j
Power
Line
30
50
Pixel
12
18
36
Digital
Data
Input
Adder
Voltage Data
Driver
310
i-1
i
i-1
i
Power Supply
48
38
28
I=f(V)
Data
Line
16
Display Array
10
24
34
42
R
40
ΔV
Compensation
Memory
A/D
44
Comparator
46

FIG.2

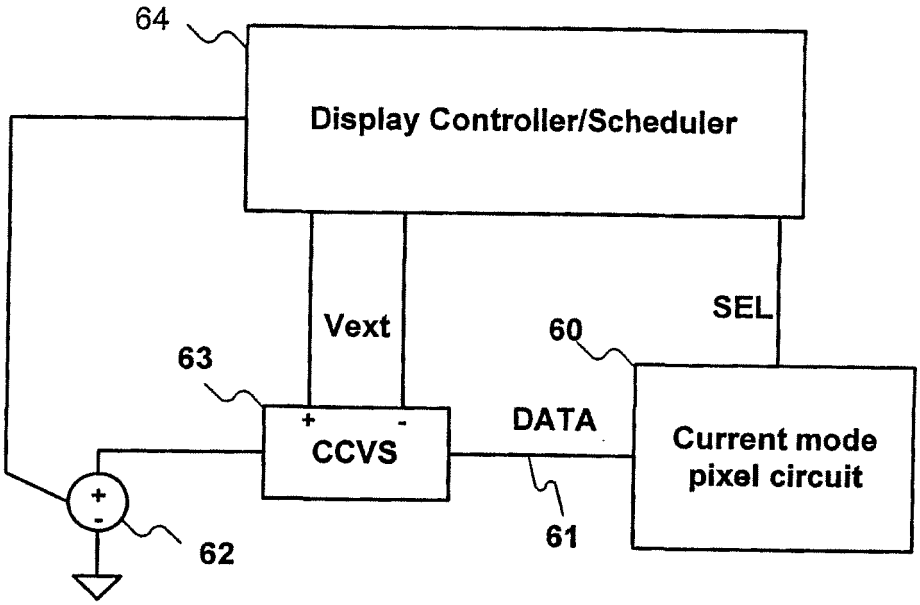
64
Display Controller/Scheduler
Vext
SEL
60
63
+
-
CCVS
DATA
Current mode pixel circuit
+
-
62
61

FIG.3

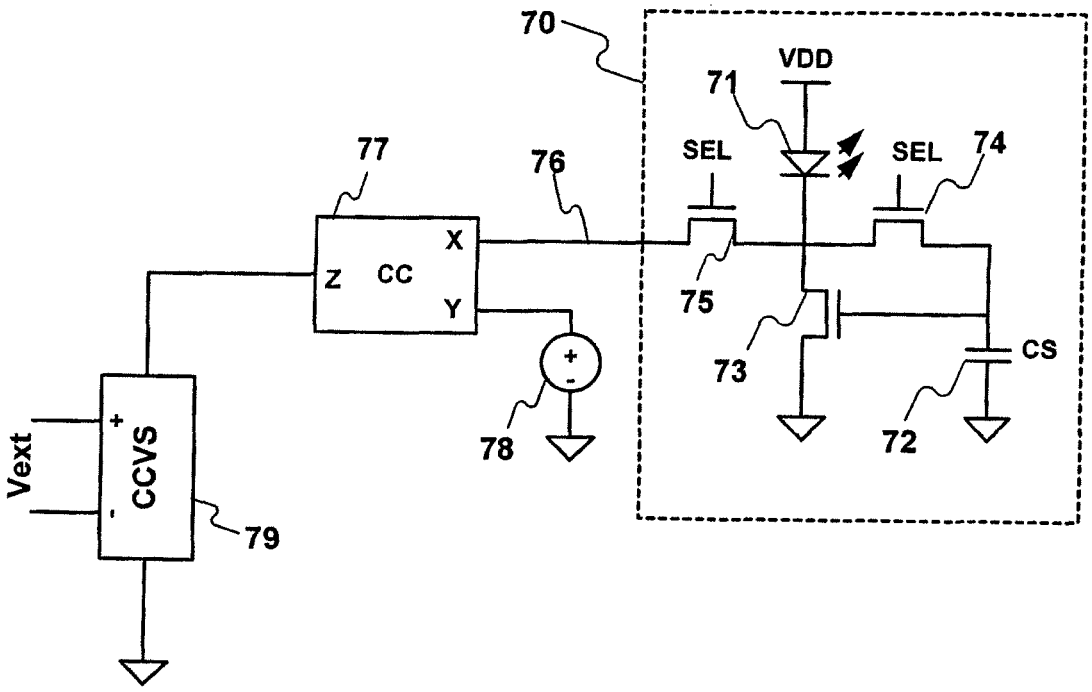

FIG.4

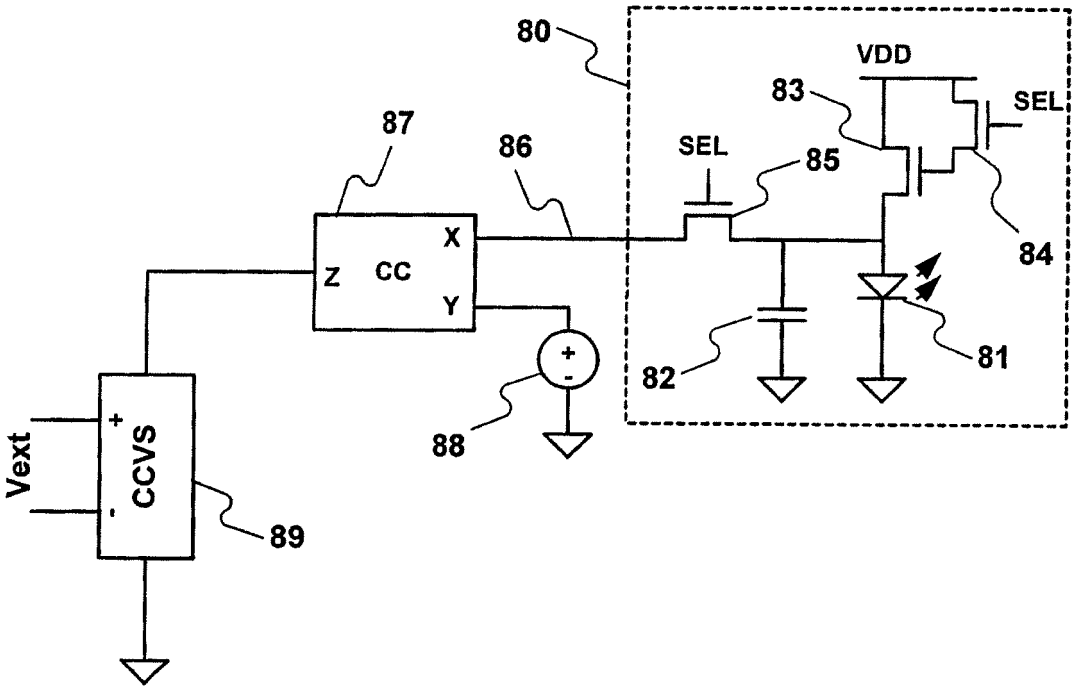

FIG.5

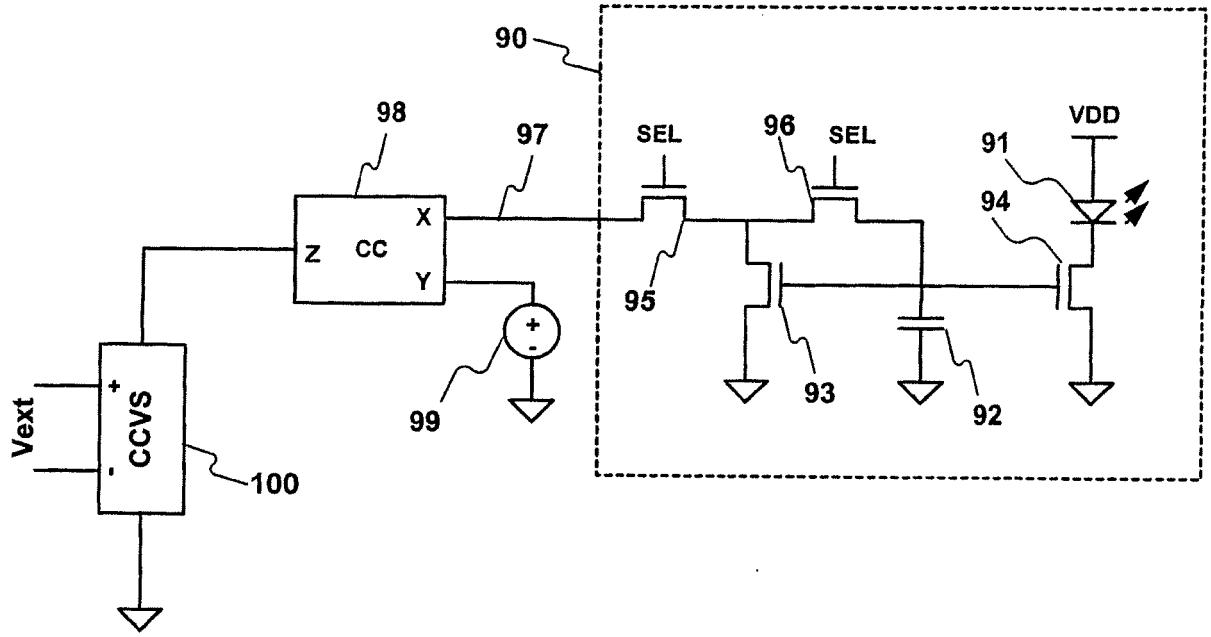

FIG. 6

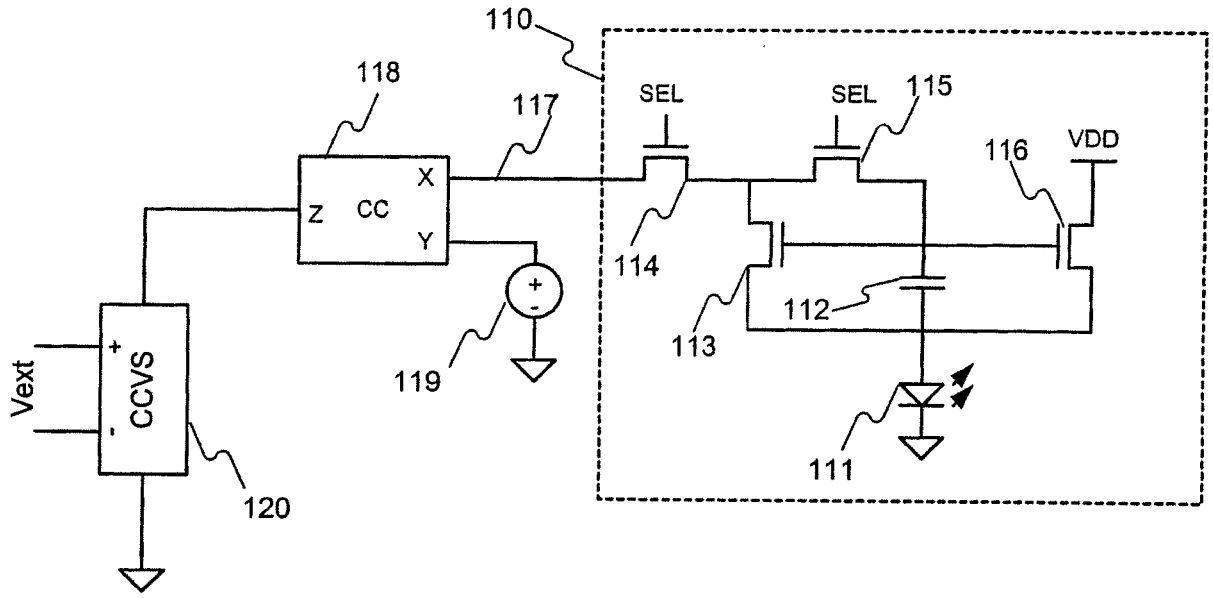
110
118
117
SEL
SEL
115
116
VDD
X
Z
CC
Y
114
112
113
119
Vext
CCVS
120
111

FIG. 7

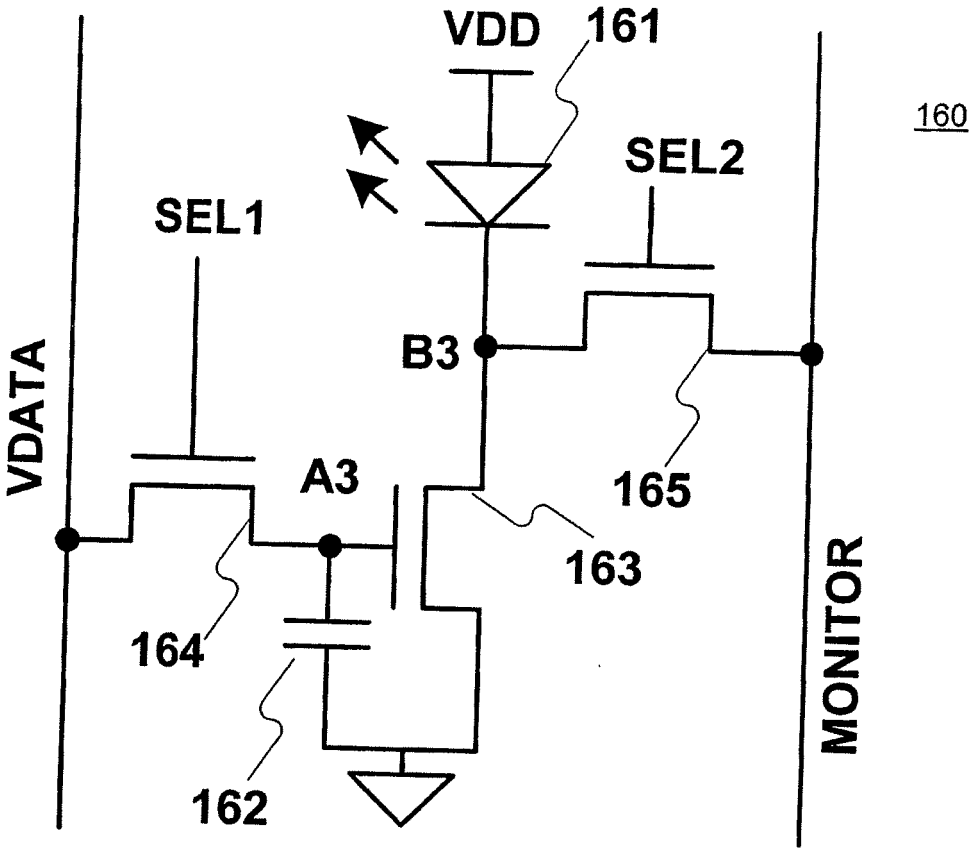

FIG. 8

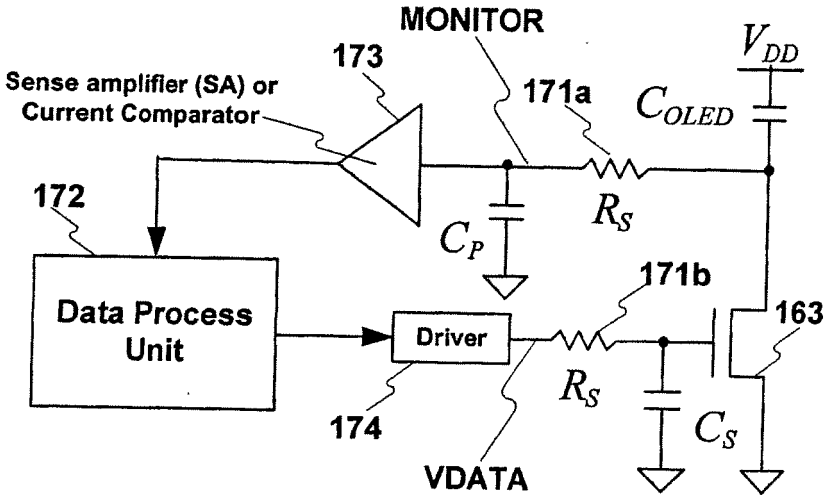
MONITOR
173
Sense amplifier (SA) or
Current Comparator
171a
V_{DD}
C_{OLED}
172
R_S
C_P
171b
163
Data Process
Unit
Driver
R_S
174
C_S
VDATA

FIG. 9

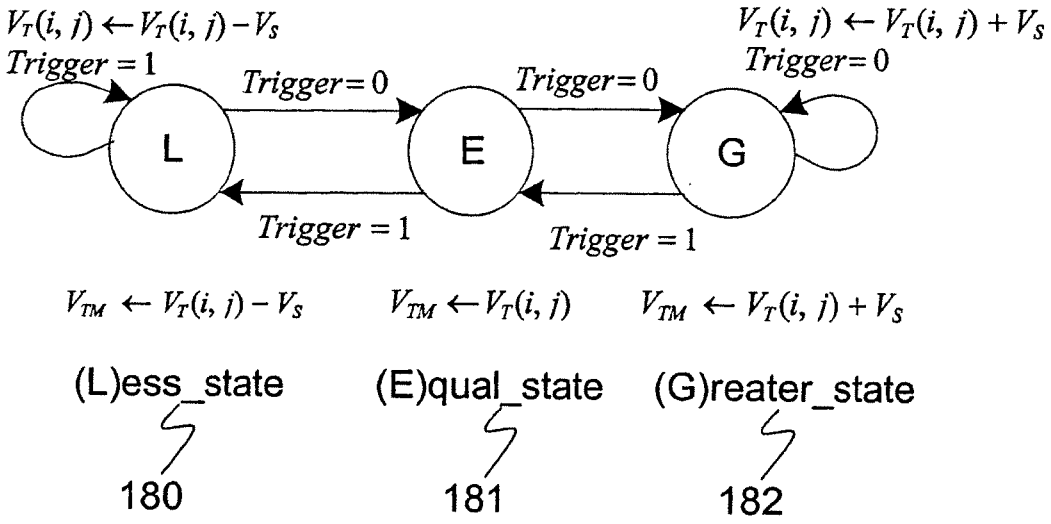
$V_T(i, j) \leftarrow V_T(i, j) - V_S$
Trigger = 1
Trigger= 0
Trigger= 0
$V_T(i, j) \leftarrow V_T(i, j) + V_S$
Trigger= 0
L
E
G
Trigger = 1
Trigger = 1
$V_{TM} \leftarrow V_T(i, j) - V_S$
$V_{TM} \leftarrow V_T(i, j)$
$V_{TM} \leftarrow V_T(i, j) + V_S$
(L)ess_state
(E)qual_state
(G)reater_state
180
181
182

FIG. 10

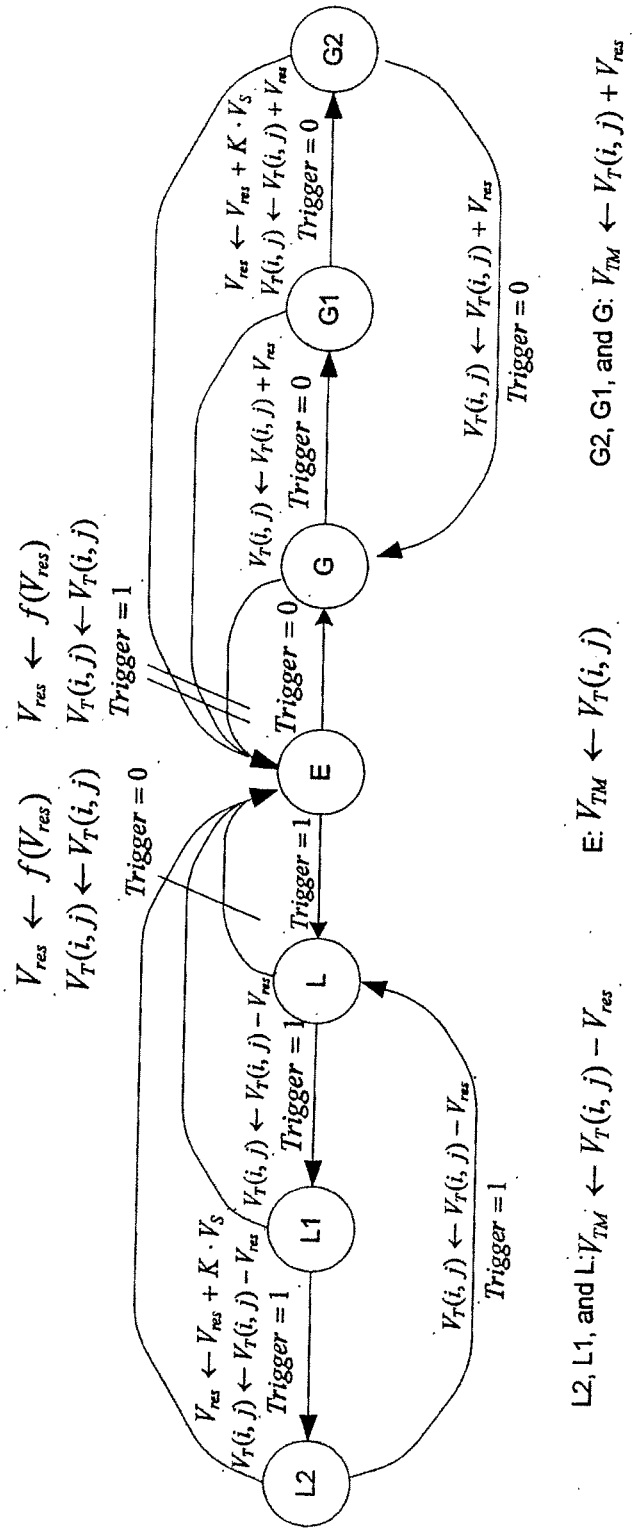
L2
L1
L
E
G
G1
G2
$V_{res} \leftarrow f(V_{res})$
$V_T(i,j) \leftarrow V_T(i,j)$
$Trigger = 0$
$V_{res} \leftarrow V_{res} + K \cdot V_S$
$V_T(i,j) \leftarrow V_T(i,j) - V_{res}$
$Trigger = 1$
$V_T(i,j) \leftarrow V_T(i,j) + V_{res}$
L2, L1, and L: $V_{TM} \leftarrow V_T(i,j) - V_{res}$
E: $V_{TM} \leftarrow V_T(i,j)$
G2, G1, and G: $V_{TM} \leftarrow V_T(i,j) + V_{res}$
$f(V_{res}) = \begin{cases} V_S & V_{res} \leq (A-1)V_S \\ \dfrac{V_{res} - V_S}{A} & V_{res} > (A-1)V_S \end{cases}$

FIG. 11

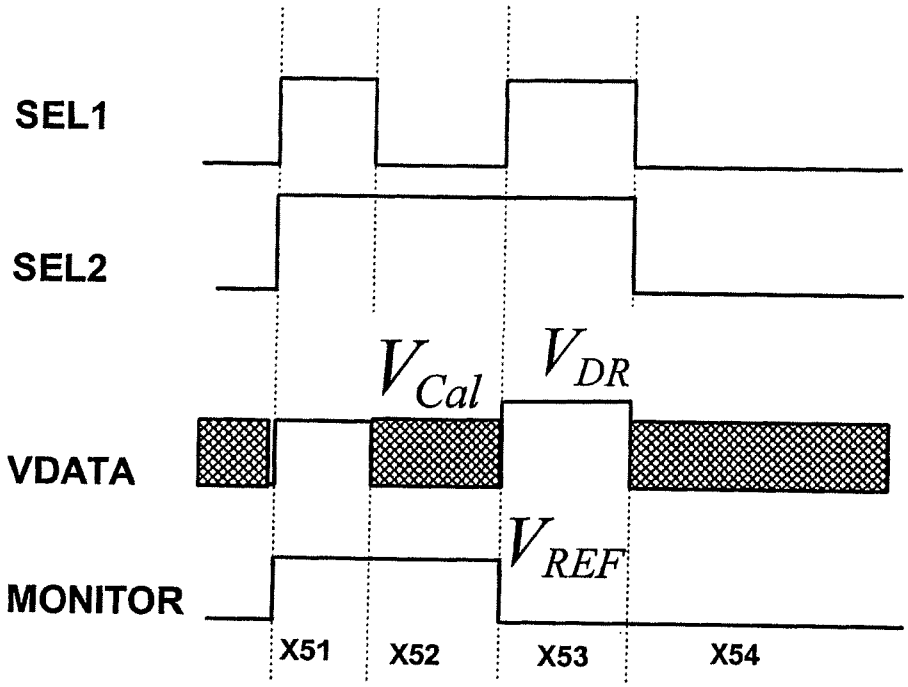

FIG. 12

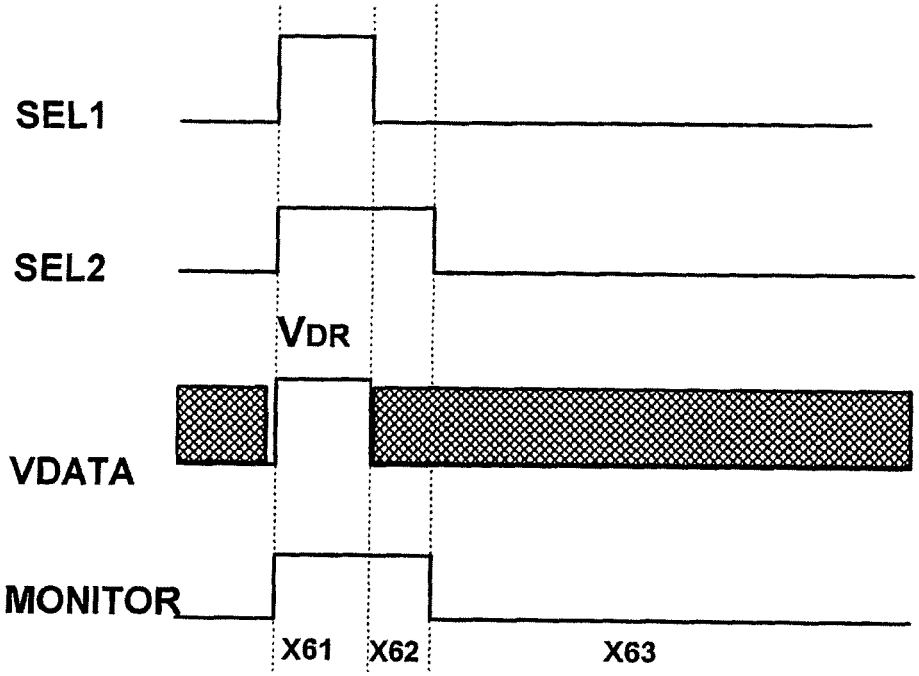

FIG. 13

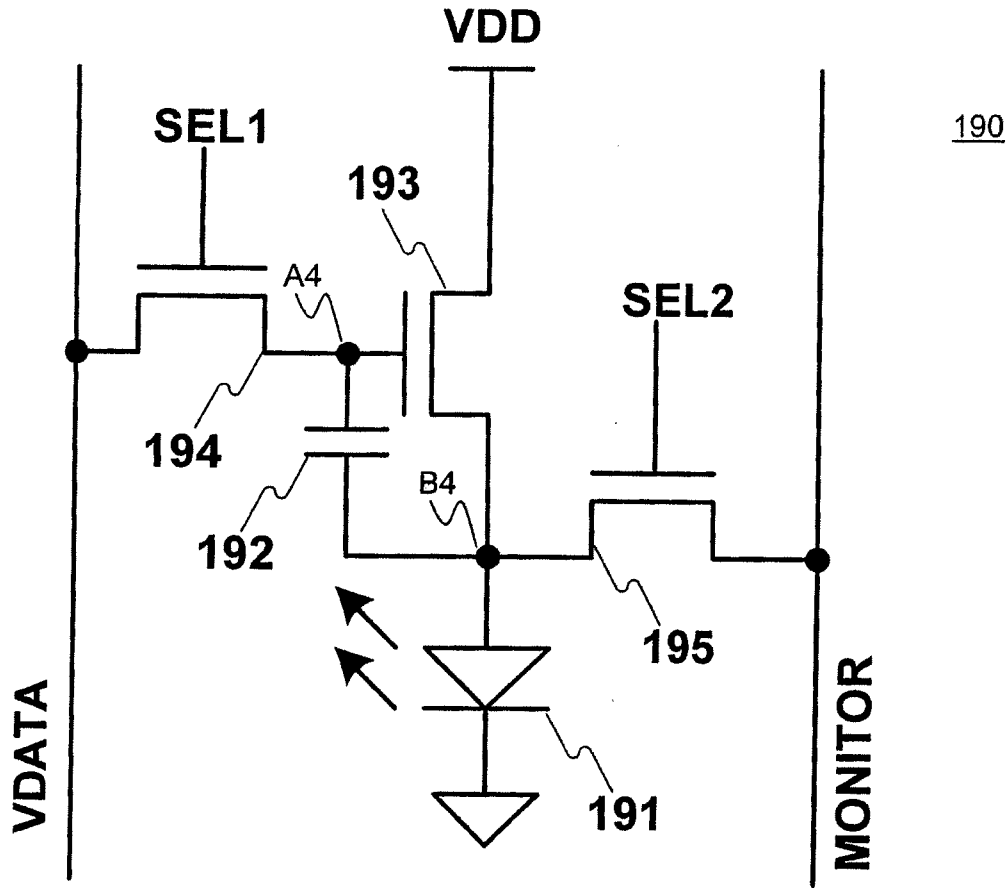

FIG. 14

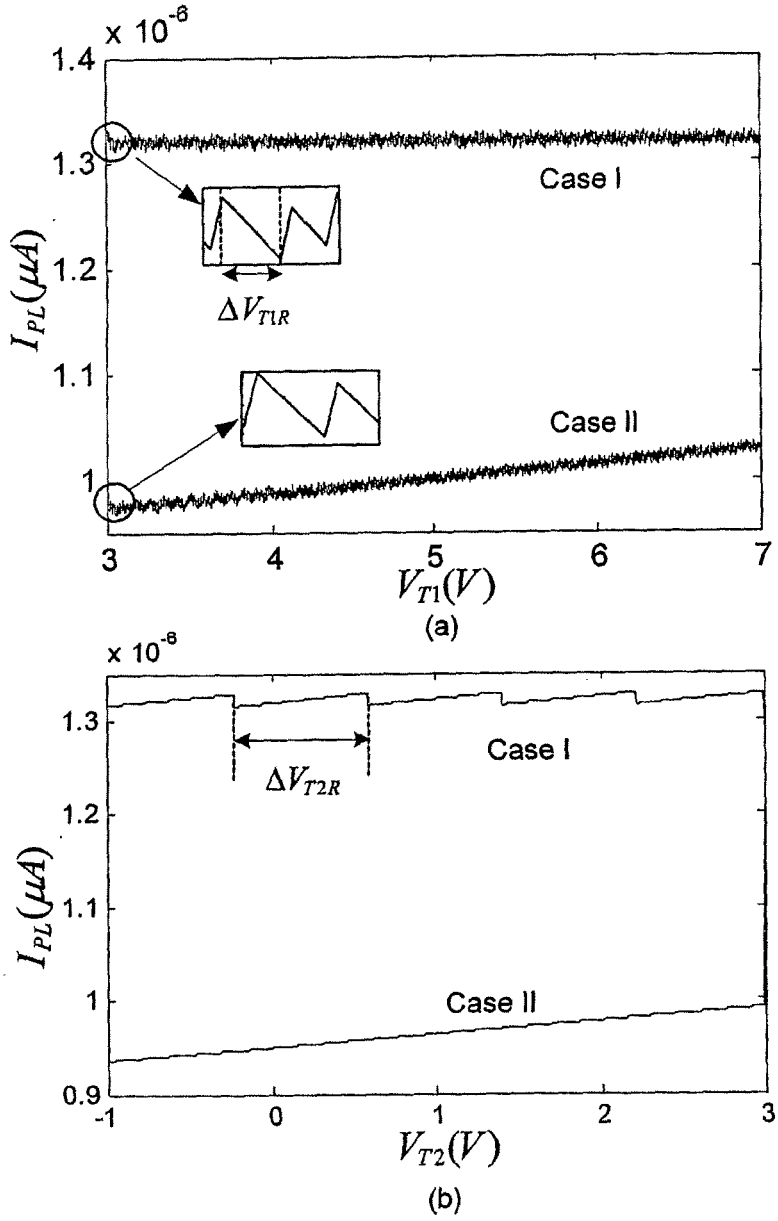
x 10^-6
1.4
1.3
1.2
1.1
1
$I_{PL}(\mu A)$
Case I
ΔV_{T1R}
Case II
3
4
5
6
7
$V_{T1}(V)$
(a)
x 10^-6
1.3
1.2
1.1
1
0.9
$I_{PL}(\mu A)$
Case I
ΔV_{T2R}
Case II
-1
0
1
2
3
$V_{T2}(V)$
(b)

FIG. 15

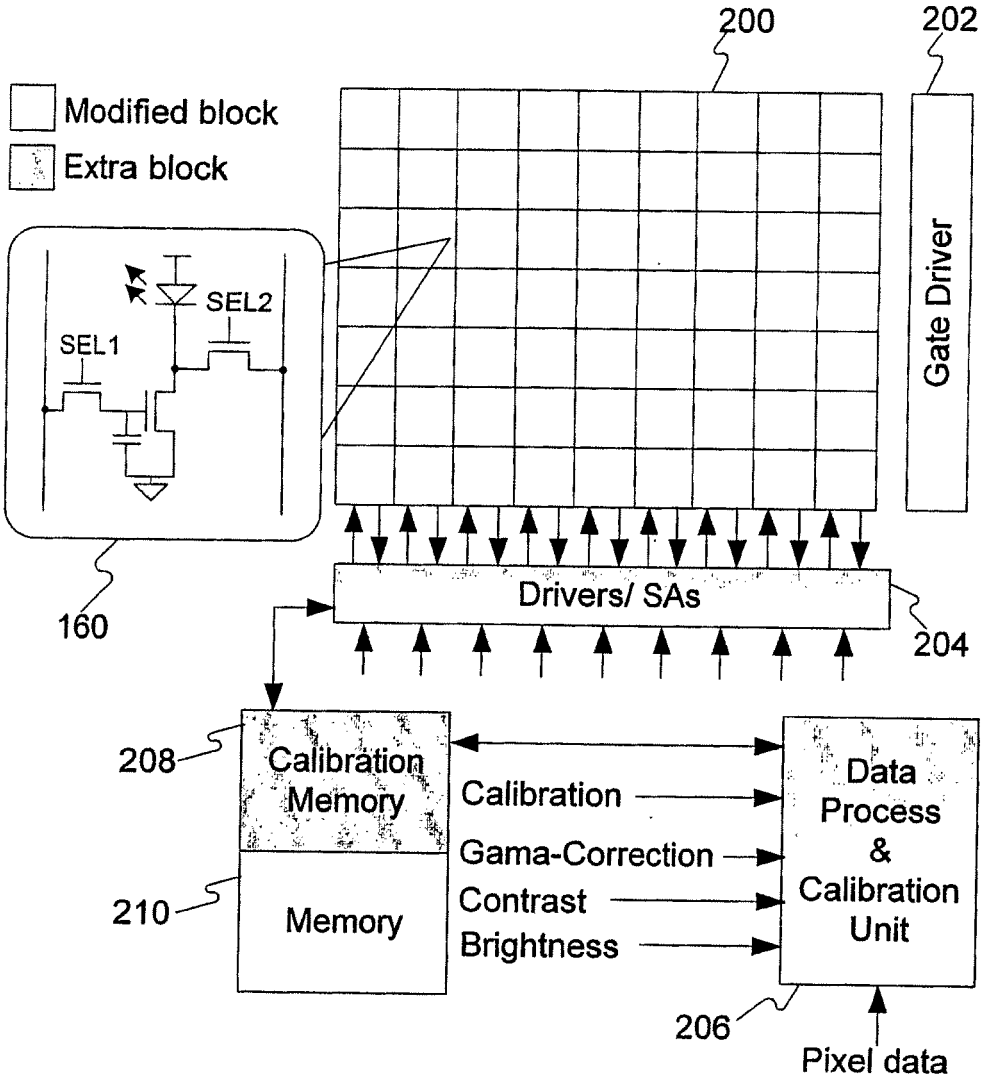
Modified block
Extra block
SEL1
SEL2
160
200
202
Gate Driver
Drivers/ SAs
204
208
Calibration Memory
210
Memory
Calibration
Gama-Correction
Contrast
Brightness
Data Process & Calibration Unit
206
Pixel data

FIG. 16

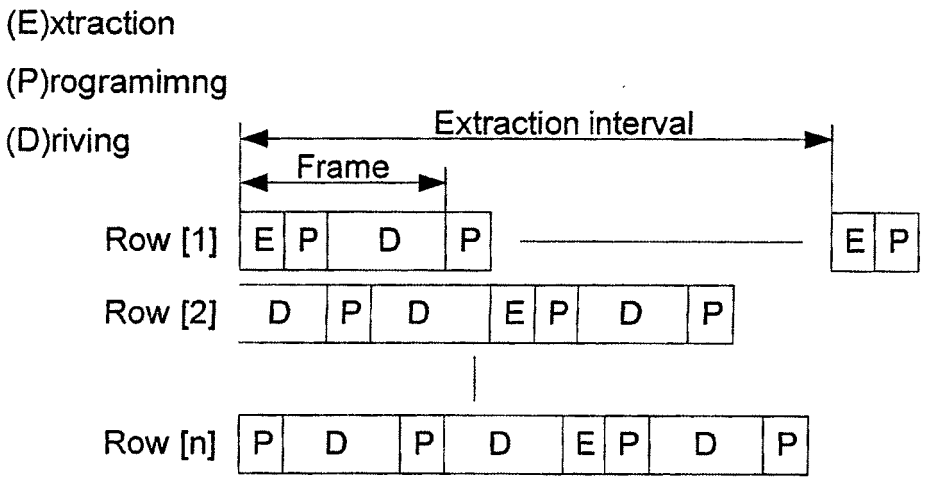
(E)xtraction
(P)rogramimng
(D)riving
Extraction interval
Frame
Row [1]
E P D P
E P
Row [2]
D P D E P D P
Row [n]
P D P D E P D P

FIG. 17

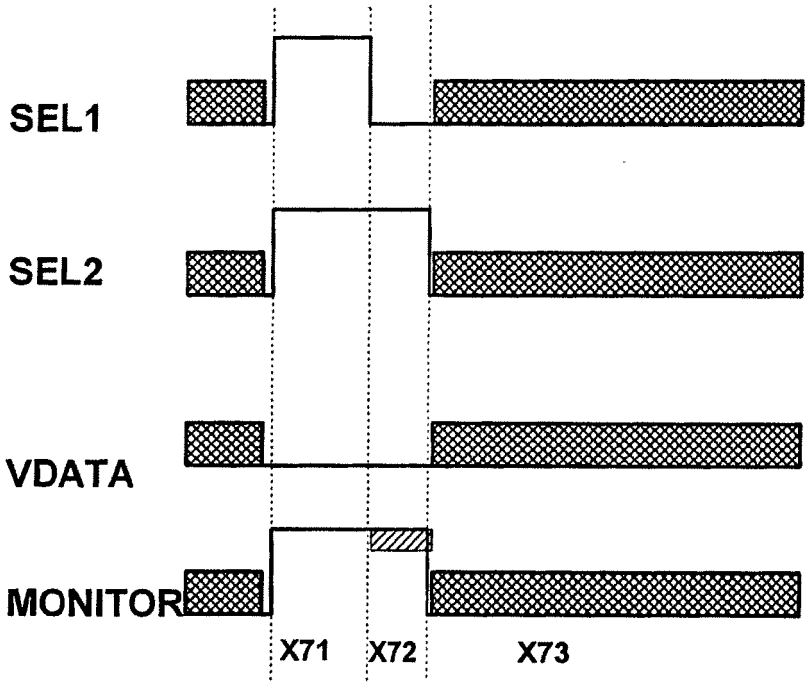

FIG. 18

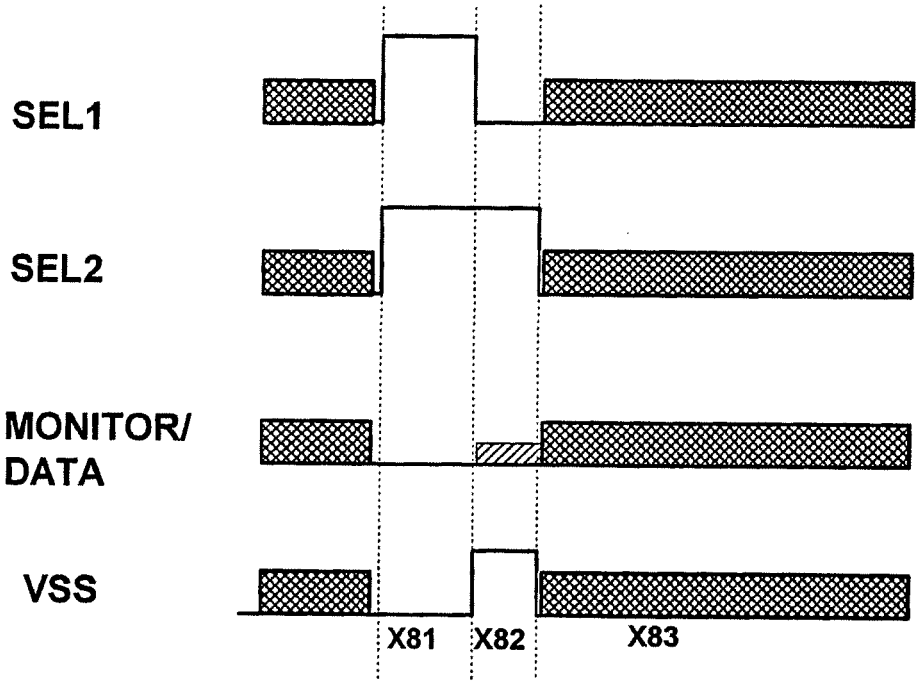

FIG. 19

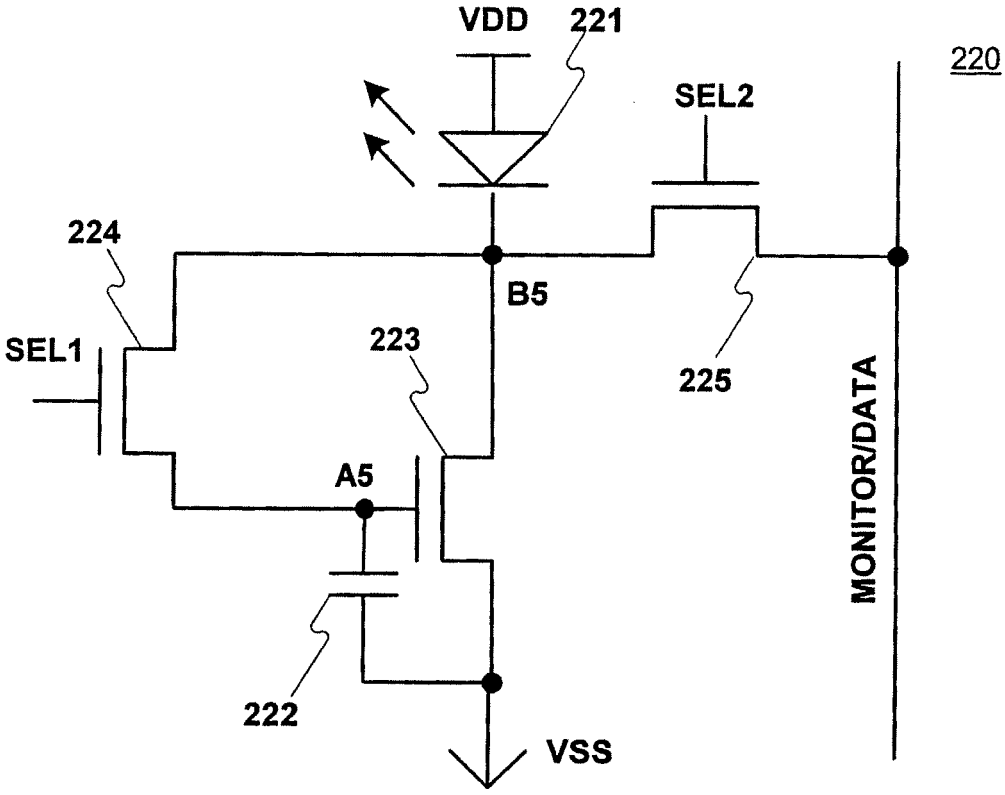

FIG. 20

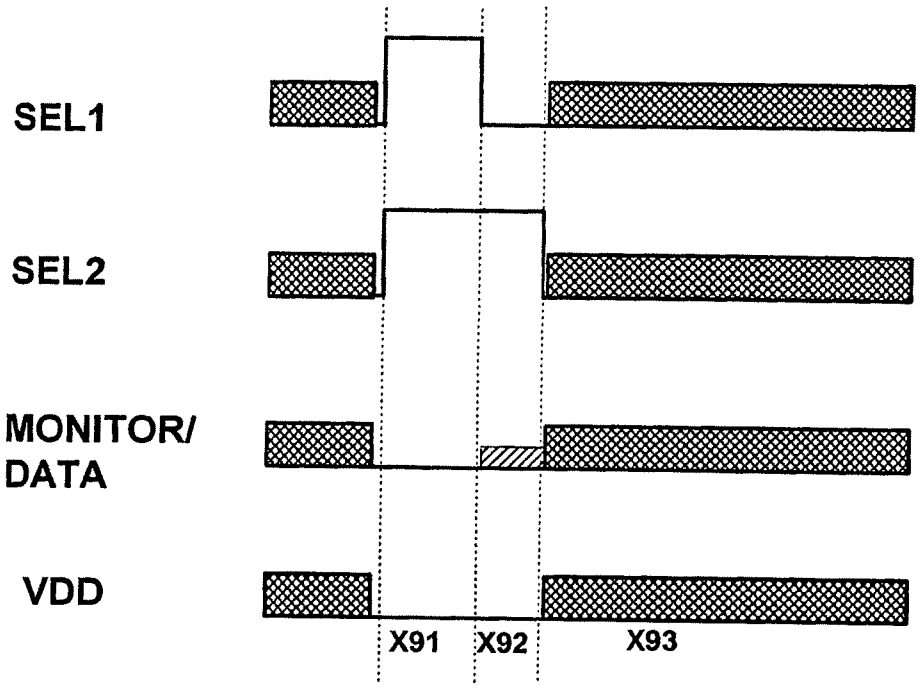

FIG. 21

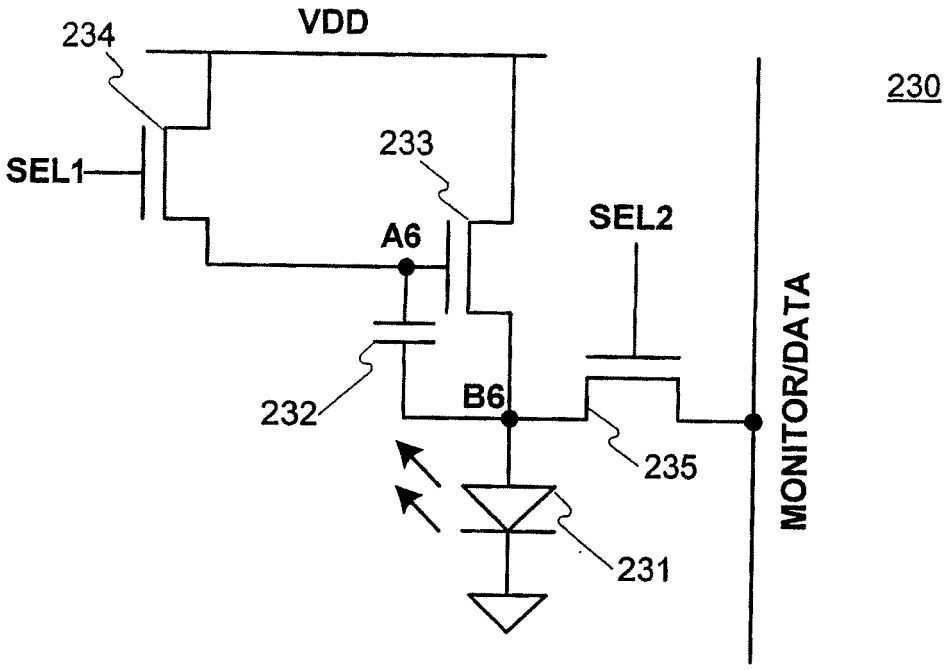

FIG. 22

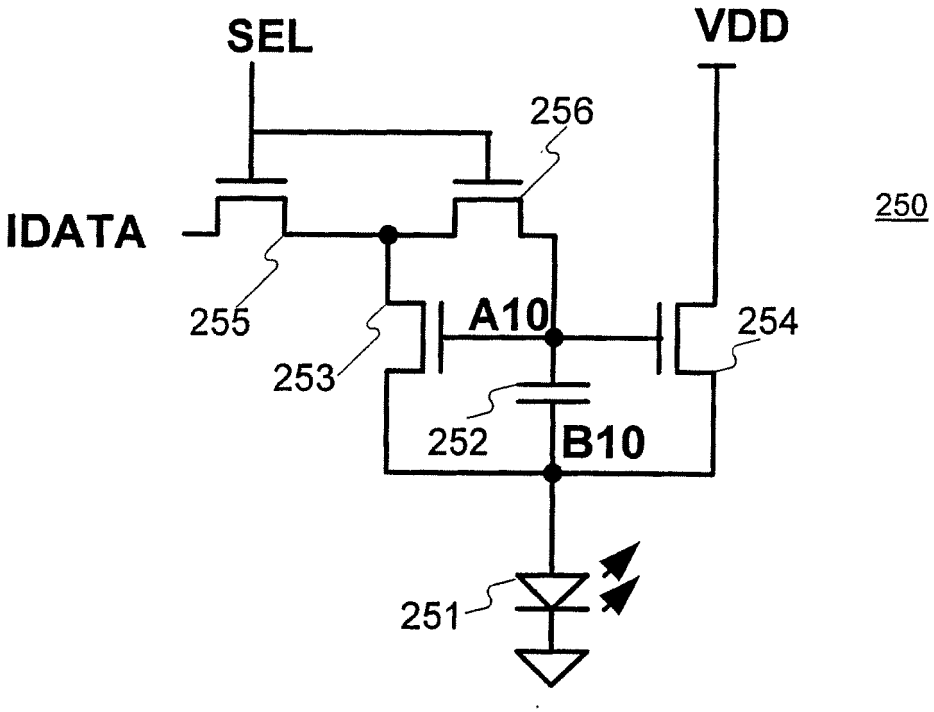

FIG. 23

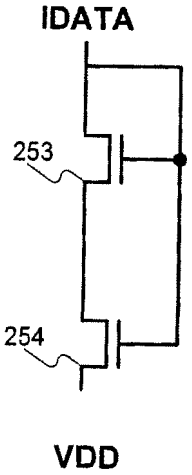

FIG. 24

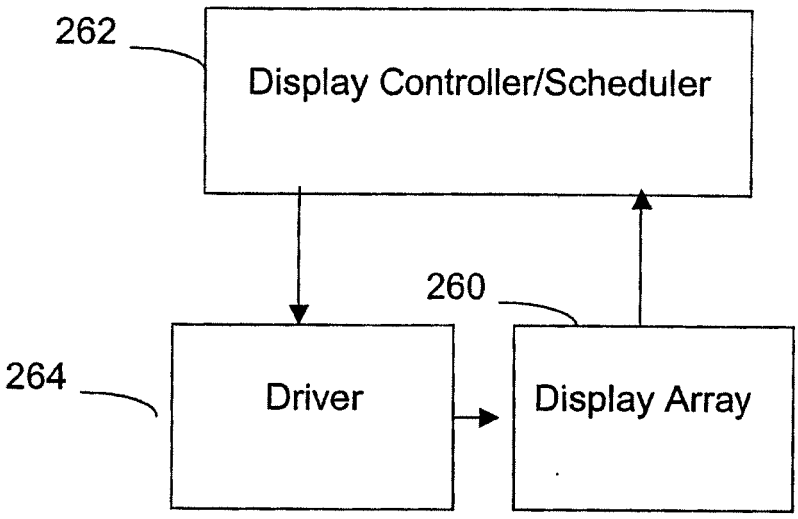
262
Display Controller/Scheduler
260
264
Driver
Display Array

FIG. 25

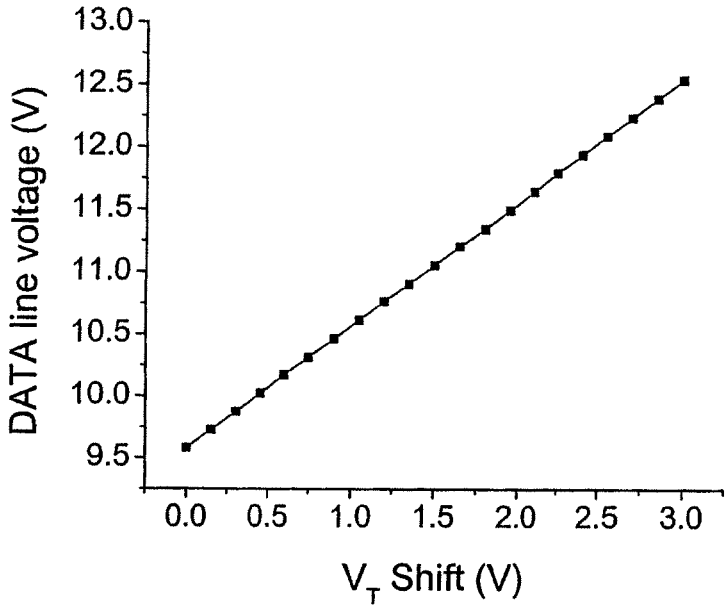
13.0
12.5
12.0
11.5
11.0
10.5
10.0
9.5
DATA line voltage (V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
V_T Shift (V)

FIG. 26

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 6594606 A **[0004]**
- US 20040257353 A1 **[0005]**
- WO 2004047058 A2 **[0006]**

专利名称(译)	用于编程，校准和驱动发光器件显示器的方法和系统		
公开(公告)号	EP2383720B1	公开(公告)日	2018-02-14
申请号	EP2011168677	申请日	2005-12-15
[标]申请(专利权)人(译)	伊格尼斯创新公司		
申请(专利权)人(译)	IGNIS创新INC.		
当前申请(专利权)人(译)	IGNIS创新INC.		
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发明人	NATHAN, AROKIA CHAJI, GHOLAMREZA SERVATI, PEYMAN		
IPC分类号	G09G3/20 G09G3/32		
CPC分类号	G01R19/0092 G09G3/006 G09G3/3208 G09G3/3233 G09G3/3241 G09G3/3258 G09G3/3283 G09G3/3291 G09G2300/0819 G09G2300/0842 G09G2310/0262 G09G2310/027 G09G2320/0285 G09G2320/029 G09G2320/0295 G09G2320/043 G09G2320/045 G09G2320/0693		
优先权	2503237 2005-04-08 CA 2490860 2004-12-15 CA 2521986 2005-10-17 CA 2509201 2005-06-08 CA		
其他公开文献	EP2383720A3 EP2383720A2		
外部链接	Espacenet		

摘要(译)

一种用于显示阵列的系统，包括像素电路，所述像素电路包括驱动晶体管，至少一个开关晶体管，存储电容器和发光器件。该系统包括用于监视与像素电路相关联的电流或电压的监视器，用于控制显示阵列的操作的数据处理单元，数据处理单元被配置为基于提取指示像素电路老化的信息。监控的电流或电压以及由数据处理单元控制的驱动器，用于基于提取的老化信息向像素电路提供编程和校准数据。