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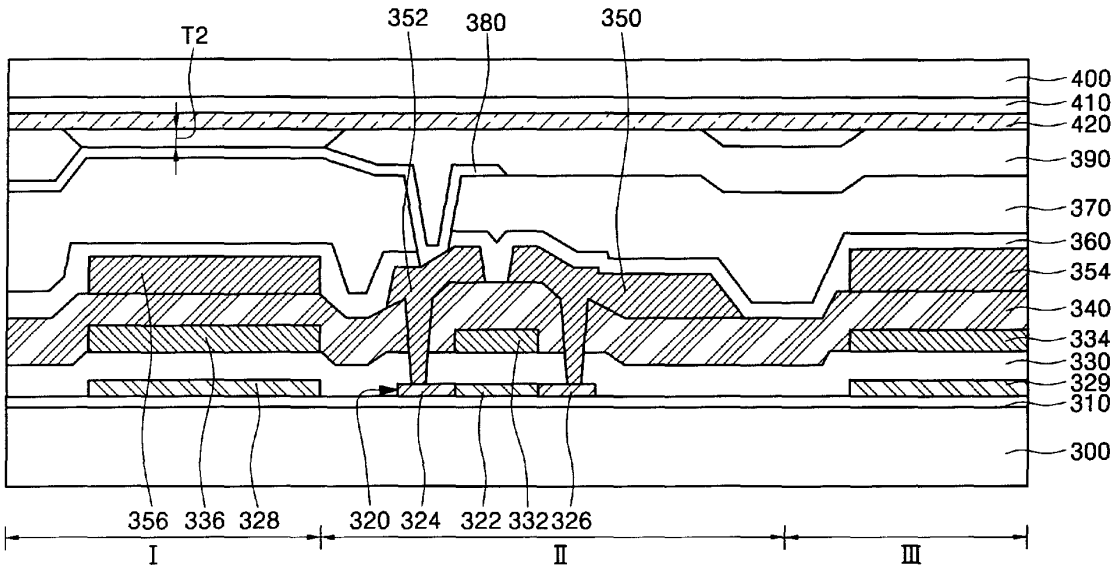
(54) Organic light emitting display device and method of fabricating the same

(57) An organic light emitting display device and a method of fabricating the same. A dummy pattern (328,336,356) is formed in an emission region (I) to increase the step height of the emission region (I) by an electrode material while a thin film transistor is fabricated, so that a distance between a pixel electrode and a donor film (T2) is decreased during fabrication of an organic layer. This reduced distance (T2) reduces laser energy for transfer using laser-induced thermal imaging, thus improving life span and efficiency of the device. Further, the pixel electrode (380) can extend into a thin film transistor region (II) and a capacitor region (III), thus enhancing an aperture ratio.

FIG. 2



EP 1 670 081 A2

Description

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U. S.C. § 119 from an application earlier filed in the Korean Intellectual Property Office on 13 December 2004 and there duly assigned Serial No. 10-2004-0105146.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an organic light emitting display device and a method of fabricating the same, and more particularly, to an organic light emitting display device with a pixel region having an increased step difference to facilitate the deposition of an organic layer using a laser-induced thermal imaging method.

Description of the Related Art

[0003] Among flat panel display devices, an organic light emitting display device has a fast response time shorter than 1ms, consumes little power, and has a wide viewing angle range because it can emit light by itself. As a result, the organic light emitting display device has the advantage of a moving picture displaying medium regardless of the size thereof. Further, the organic light emitting display device can be fabricated at a low temperature, and its fabricating process is simple based on the existing semiconductor processing technology, thus attracting attention as a next generation flat panel display device.

[0004] According to materials and processes, the organic light emitting display device can be widely classified into a polymer device using a wet process, and a small molecule device using a deposition process. As a method for patterning a polymer or small molecule emission layer, an inkjet printing method is applied using limited materials for organic layers except for the emission layer, and has a complicated structure to be applied to a substrate. Further, a metal mask is needed to pattern the emission layer by the deposition process, so that there is much trouble in fabricating a large-sized device.

[0005] Meanwhile, a laser-induced thermal imaging (LITI) method has been recently developed as an alternative to the foregoing patterning method. The laser-induced thermal imaging method converts laser light from a light source into heat energy, and uses the heat energy to transfer a pattern forming material to an objective substrate, thus forming a pattern on the substrate. In the laser-induced thermal imaging method, a donor substrate formed with a transfer layer, a light source and an objective substrate are needed. Further, in the laser-induced thermal imaging method, the donor substrate and the objective substrate are laminated so that the donor substrate is adhered to the highest portion of the objective substrate.

[0006] However, in typical LITI processes for forming an organic light emitting display device, a large gap exists between the donor substrate and the pixel electrode. This large gap requires more laser energy for the LITI process, leading to damage and deterioration of the organic emission layer. Therefore, what is needed is an improved structure where this large gap is not apt to occur.

SUMMARY OF THE INVENTION

[0007] It is therefore an object of the present invention to provide an improved design for an organic light emitting display device and an improved method of making the same.

[0008] It is further an object of the present invention to provide an improved design and method of making that reduces the gap in the LITI process.

[0009] These and other objects can be achieved by an organic light emitting display device and a method of fabricating the same, in which a dummy pattern is provided under a pixel electrode of an emission region, so that a distance between a donor substrate and the pixel electrode is minimized, thus enhancing the efficiency of laser energy in a LITI process, and improving the life span and efficiency of an organic layer.

[0010] In an exemplary embodiment of the present invention, an organic light emitting display device includes an emission region including a pixel electrode, an organic layer that includes at least an emission layer, and an opposite electrode on a substrate, the emission region being defined by a pixel defining layer, a dummy pattern being arranged in the emission region under the pixel electrode, a thin film transistor region including a gate electrode and source and drain electrodes, and a capacitor region including a lower electrode and an upper electrode.

Preferably the pixel electrode includes a reflective electrode, and the opposite electrode includes a transparent electrode.

Preferably the pixel electrode extends into the thin film transistor region and into the capacitor region.

Preferably the organic layer further includes at least one layer selected from the group consisting of a hole injection layer, a hole transporting layer, a hole blocking layer, an electron transporting layer and an electron injection layer.

Preferably the dummy pattern has a laminated structure of at least two materials selected from the group consisting of a polysilicon layer pattern, a gate electrode material, and source and drain electrode materials.

Preferably the pixel defining layer has a thickness of 3,000Å or less.

[0011] In another exemplary embodiment of the present invention, a method of fabricating an organic light emitting display device includes forming first conductive

layer patterns on a substrate that is divided into a first region, a second region and a third region, respectively, forming a first insulating layer on the substrate and on the first conductive layer patterns, forming second conductive layer patterns on the first insulating layer in the first region, the second region and the third region, respectively, forming a second insulating layer on an entire surface of the second conductive layer and on exposed portions of the first insulating layer, forming third conductive layer patterns on the second insulating layer in first region, the second region and the third region, respectively, forming a third insulating layer on an entire surface of the third conductive layer and on exposed portions of the second insulating layer, forming a pixel electrode on the third insulating layer in the first region, the pixel electrode adapted to be connected to the third conductive pattern in the second region, forming a fourth insulating layer on the pixel electrode and on exposed portions of the third insulating layer, patterning the fourth insulating layer to expose at least a portion of the pixel electrode in the first region, forming an organic layer on the exposed portion of the pixel electrode, the organic layer including at least an emission layer and forming an opposite electrode on at least the organic layer.

Preferably the first region is an emission region, the second region is a thin film transistor region, and the third region is a capacitor region.

Preferably the first conductive layer patterns include a first dummy pattern, a polysilicon layer pattern including a channel region and source and drain regions, and a first electrode of a capacitor.

Preferably the first insulating layer is a gate insulating layer.

Preferably the second conductive layer patterns include a second dummy pattern, a gate electrode, and a second electrode of a capacitor.

Preferably the second insulating layer is an interlayer insulating layer.

Preferably the third conductive layer patterns include a third dummy pattern, source and drain electrodes, and a third electrode of a capacitor.

Preferably the third insulating layer includes either a passivation layer and a planarization layer or a laminated layer of the passivation layer and the planarization layer.

Preferably the pixel electrode comprises reflective material.

Preferably the pixel electrode is formed throughout the first region, the second region and the third region.

Preferably the patterned fourth insulating layer is a pixel defining layer.

Preferably the patterned fourth insulating layer has a thickness of 3,000Å or less.

Preferably the organic layer further includes at least one thin layer selected from the group consisting of a hole injection layer, a hole transporting layer, an electron transporting layer and an electron injection layer.

Preferably the organic layer is produced by a laser-induced thermal imaging (LITI) process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] A more complete appreciation of the invention and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0013] FIG. 1 is a cross-sectional view of an organic light emitting display device; and

[0014] FIG. 2 is a cross-sectional view of an organic light emitting display device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] A method of fabricating an organic light emitting display device will be described in conjunction with FIG. 1. FIG. 1 is a cross-sectional view of an organic light emitting display device, which includes an emission region I, a thin film transistor region II, and a capacitor region III.

[0016] To begin, a buffer layer 110 is formed on a substrate 100. Preferably, the buffer layer 110 is used to prevent impurities in the substrate 100 from migrating into the device formed in a subsequent process. Subsequently, an amorphous silicon layer (not shown) is formed as a semiconductor layer having a predetermined thickness on the buffer layer 110. Then, the amorphous silicon layer is crystallized by excimer laser annealing (ELA), sequential lateral solidification (SLS), metal induced crystallization (MIC), metal induced lateral crystallization (MILC), or the like. The crystallized silicon layer is patterned by a photolithography process, thus forming a polysilicon layer pattern 120 in the thin film transistor region II of a unit pixel. At this time, the polysilicon layer pattern can be additionally formed as a capacitor electrode in the capacitor region III.

[0017] Next, a gate insulating layer 130 is formed on the entire surface of the resultant structure. At this time, the gate insulating layer 130 can be formed of a silicon oxide (SiO_2) layer, a silicon nitride (SiN_x) or a laminated layer thereof.

[0018] Then, the polysilicon layer pattern 120 of the thin film transistor region II is doped with impurities. At this time, source and drain regions 126 and 124 are formed in the thin film transistor region II. Further, a channel region 122 is formed between the source and drain regions 126 and 124.

[0019] Then, a conductive layer (not shown) for a gate electrode is formed on the entire surface of the resultant structure. The conductive layer for the gate electrode is formed of a single layer of molybdenum (Mo) or an alloy such as molybdenum-tungsten (MoW), a single layer of aluminum (Al) or an alloy such as aluminum-neodymium (Al-Nd), or a double layer of the above-mentioned metals.

[0020] Then, the conductive layer for the gate elec-

trode is etched by photolithography and etching processes, thus forming a gate electrode 132 in the thin film transistor region II and a lower electrode 134 in the capacitor region III, respectively. In the case where the thin film transistor is an n-channel metal oxide semiconductor (NMOS), impurity ions can be lightly doped using the gate electrode 132 as an ion implantation mask, thus forming a lightly-doped drain (LDD) region (not shown).

[0021] Then, an interlayer insulating layer 140 is formed on the entire surface of the resultant structure. Subsequently, the interlayer insulating layer 140 and the gate insulating layer 130 are etched by photolithography and etching processes, thus forming a contact hole for exposing the source and drain regions 126 and 124.

[0022] Then, a material for forming source and drain electrodes is formed on the interlayer insulating layer 140. The source and drain electrode material is etched by photolithography and etching processes, thus forming source and drain electrodes 150 and 152 in the thin film transistor region II and an upper electrode 154 in the capacitor region III, respectively. Here, the source and drain electrodes 150 and 152 are connected to the source and drain regions 124 and 126 respectively.

[0023] Then, a passivation layer 160 and a planarization layer 170 are formed on the entire surface of the resultant structure. Then, the planarization layer 170 and the passivation layer 160 are etched by photolithography and etching processes, thus forming a via contact hole to expose one of the source and drain electrodes 150 and 152. In FIG. 1, the drain electrode 152 and not the source electrode 150 is shown to be exposed by the via contact hole.

[0024] A pixel electrode 180 is then formed to be connected to the drain electrode 152 through the via contact hole. At this time, the pixel electrode 180 is formed as a reflective electrode. Then, a pixel defining layer 190 is formed on the entire surface of the resultant structure, and is patterned to expose a portion of the pixel electrode 180 in emission region I.

[0025] Then, an organic layer (not shown) including at least the emission layer is formed on the pixel electrode 180. The organic layer is formed by an LITI method using the donor substrate that includes base substrate 200, a light-to-heat conversion layer 210 and a transfer layer 220. Then, an opposite electrode (not shown) is formed, and an encapsulating process is performed, thus completing the organic light emitting display device of FIG. 1.

[0026] In the organic light emitting display device of FIG. 1, the thin film transistor region II and the capacitor region III are formed to be lower than the emission region I. In other words, the thin film transistor region II and the capacitor region III are different in height by the metal electrodes, the gate electrode 132, the source and drain electrodes 150 and 152, the lower electrode 134 and the upper electrode 154, which are laminated in the thin film transistor region II and the capacitor region III but not in the emission region I.

[0027] The step difference manifests itself at interconnections around the unit pixel and a peripheral portion thereof. For example, the thickness of a data line causes a data line region to be relatively higher than the emission region I. Such a structure can cause some problems in the LITI process for forming the organic layer. As the height T1 for detaching the emission region I and the transfer layer 220 from the donor substrate becomes larger, laser energy needed for transfer increases. A high laser energy is likely to damage the emission layer of the organic light emitting display device. Thus, the efficiency and life span of the resultant organic light emitting display device are decreased.

[0028] Turning now to FIG. 2, FIG. 2 is a cross-sectional view of an organic light emitting display device according to an embodiment of the present invention. The organic light emitting display device is divided into an emission region I, a thin film transistor region II, and a capacitor region III for convenience.

[0029] Referring to FIG. 2, a first dummy pattern 328 formed of a polysilicon layer, a second dummy pattern 336 formed of a gate electrode material, and a third dummy pattern 356 formed of a material for forming source and drain electrodes are laminated in the emission region I of a substrate 300, and a pixel electrode 380 is formed above the dummy patterns. Further, a thin film transistor including a gate electrode 332 and source and drain electrodes 350 and 352 are formed in the thin film transistor region II of the substrate 300. Also, a first capacitor includes a first electrode 329 formed of a poly silicon layer pattern, a second electrode 334 formed of a gate electrode material, and a gate insulating layer 330 between the first and second electrodes 329 and 334. And, a second capacitor includes a third electrode 354 made of the source and drain electrode material, and an interlayer insulating layer 340 between the second electrode 334 and the third electrode 354 and located in the capacitor region III. To form an organic layer (not shown) in the emission region I by a LITI method, a donor substrate including a base substrate 400, a light-to-heat conversion layer 410 and a transfer layer 420 are arranged and laminated on the substrate 300.

[0030] As shown in FIG. 2, the first dummy pattern 328, the second dummy pattern 336 and the third dummy pattern 356 are laminated in the emission region I, but the present invention is not limited thereto. Alternatively, two or more patterns among the dummy patterns can be laminated. Here, the pixel electrode 380 can be formed of a reflective electrode or a laminated layer including a reflective electrode so that the organic light emitting display device is a top emission type. The pixel electrode 380 can extend into the thin film transistor region II and the capacitor region III, thus enlarging an aperture ratio. Further, the double capacitor structure in the capacitor region III can be replaced by a single capacitor structure including the second electrode 334 and the third electrode 354.

[0031] Meanwhile, a pixel defining layer 390 defining the emission region is formed on the pixel electrode 380.

Here, the pixel defining layer 390 is formed to a thickness of 3,000Å or less. Preferably, a distance T2 between the transfer layer 420 of the donor substrate and the pixel electrode 380 is 3,000Å or less. Even though the emission region I, the thin film transistor region II and the capacitor region III have the same step difference, the transfer layer 420 and the pixel electrode 380 are spaced apart from each other by a distance as much as the thickness of the pixel defining layer 390.

[0032] A method of fabricating the organic light emitting display of FIG. 2 according to an embodiment of the present invention will now be described. A buffer layer 310 is formed on the substrate 300 including in the emission region I, in the thin film transistor region II and in the capacitor region III. The buffer layer 310 is formed to prevent impurities in the substrate 300 from migrating into the device formed above in a subsequent process.

[0033] Subsequently, an amorphous silicon layer (not shown) is formed as a semiconductor layer having a predetermined thickness on the buffer layer 310. Then, the amorphous silicon layer is crystallized by excimer laser annealing (ELA), sequential lateral solidification (SLS), metal induced crystallization (MIC), metal induced lateral crystallization (MILC), or the like. The crystallized silicon layer is patterned by a photolithography process, thus forming the first dummy pattern 328, the polysilicon layer pattern 320 and the first electrode 329 in the emission region I, the thin film transistor region II and the capacitor region III, respectively.

[0034] Then, a gate insulating layer 330 is formed on the entire surface of the resultant structure. At this time, the gate insulating layer 330 can be formed of a silicon oxide (SiO_2) layer, a silicon nitride (SiN_x) or a laminated layer thereof.

[0035] Then, the polysilicon layer pattern 320 in the thin film transistor region II and in the first electrode 329 of the capacitor region III are doped with impurities on the gate insulating layer 330. At this time, source and drain regions 326 and 324 are formed in the thin film transistor region II. Further, a channel region 322 is formed between the source and drain regions 326 and 324.

[0036] Then, a conductive layer (not shown) for a gate electrode is formed on the entire surface of the resultant structure. The conductive layer for the gate electrode is formed of a single layer of molybdenum (Mo) or an alloy such as molybdenum-tungsten (MoW), a single layer of aluminum (Al) or an alloy such as aluminum-neodymium (Al-Nd), or a double layer of the above-mentioned metals. Then, the conductive layer for the gate electrode is etched by photolithography and etching processes, thus forming the second dummy pattern 336, the gate electrode 332 and the second electrode 334 in the emission region I, the thin film transistor region II and the capacitor region III, respectively. In the case where a thin film transistor is an n-channel metal oxide semiconductor (NMOS), impurity ions can be lightly doped using the gate electrode 332 as an ion implantation mask, thus forming a lightly-doped drain (LDD) region (not shown).

[0037] Then, an interlayer insulating layer 340 is formed on the entire surface of the resultant structure. Subsequently, the interlayer insulating layer 340 and the gate insulating layer 330 are etched by photolithography and etching processes, thus forming a contact hole for exposing the source and drain regions 326 and 324. Then, a material for forming source and drain electrodes is formed on the interlayer insulating layer 340.

[0038] Then, the source and drain electrode material is etched by photolithography and etching processes, thus forming the third dummy pattern 356, the source and drain electrodes 350 and 352 and the third electrode 354 in the emission region I, the thin film transistor region II and the capacitor region III, respectively. Here, the source and drain electrodes 350 and 352 are connected to the source and drain regions 326 and 324.

[0039] Next, a passivation layer 360 and a planarization layer 370 are formed on the entire surface of the resultant structure. Then, the planarization layer 370 and the passivation layer 360 are etched by photolithography and etching processes, thus forming a via contact hole which exposes one of the source and drain electrodes 350 and 352. In FIG. 2, the drain electrode 352 and not the source electrode 350 is shown to be exposed by the via contact hole.

[0040] Then, a pixel electrode 380 is formed to be connected to the drain electrode 352 through the via contact hole. At this time, the pixel electrode 380 is made of a reflective material. Here, the pixel electrode 380 can be formed of a single layer of the reflective material or a laminated layer that includes a reflective electrode. The single layer of the reflective electrode can include Ag or an Ag alloy. The laminated layer can include a structure of transparent/reflective/transparent electrodes or reflective/transparent electrodes, wherein the reflective electrode can include Ag or an Ag alloy, and the transparent electrode can include indium tin oxide (ITO), indium zinc oxide (IZO) or In_2O_3. Because the reflective electrode is employed as the pixel electrode 380, the pixel electrode 380 can be provided only in the emission region I. Alternatively, the pixel electrode 380 can extend into the thin film transistor region II and the capacitor region III.

[0041] Then, a pixel defining layer 390 is formed on the entire surface of the resultant structure, thus exposing a portion of the pixel electrode 380 in the emission region I. At this time, the pixel defining layer 390 is formed to a thickness of 3,000Å or less in the emission region I to thus facilitate the following organic layer forming process.

[0042] Then, an organic layer (not shown) including at least the emission layer is formed on the pixel electrode 380. Further, the organic layer can further include at least one layer among a hole injection layer, a hole transporting layer, an electron transporting layer, and an electron injection layer. Also, the organic layer can be formed by an LITI method.

[0043] The LITI method is performed as follows. The substrate 300 is disposed opposite to the donor substrate

that includes the base substrate 400, the light-to-heat conversion layer 410 and the transfer layer 420, and then arranged and laminated. Radiation from a laser is applied to the base substrate 400 of the laminated donor substrate, thus transferring the transfer layer 420 under the light-to-heat conversion layer 410 to the exposed portion of the pixel electrode 380 on substrate 300. Preferably, the distance T2 between the transfer layer 420 of the donor substrate and the pixel electrode 380 is 3,000Å or less, allowing for less laser energy needed for transferring the transfer layer 420. Then, an opposite electrode is formed over the transferred structure and an encapsulation process is performed, thus completing the organic light emitting display device.

[0044] As described above, according to the present invention, the dummy pattern is formed under the pixel electrode of the emission region so as to increase the step difference, and thus minimize the distance between the pixel electrode and the donor substrate when the organic layer is formed, thus minimizing the laser energy needed for the transfer, and enhancing the efficiency of the laser energy during the LITI process. As the laser energy is minimized, the life span and efficiency of the emission layer are improved. Further, the pixel electrode can extend to the thin film transistor region and the capacitor region, thus improving an aperture ratio.

Claims

1. An organic light emitting display device, comprising:

   an emission region including a pixel electrode, an organic layer that includes at least an emission layer, and an opposite electrode on a substrate, the emission region being defined by a pixel defining layer, a dummy pattern being arranged in the emission region under the pixel electrode;
   a thin film transistor region including a gate electrode and source and drain electrodes; and a capacitor region including a lower electrode and an upper electrode.

2. The organic light emitting display device of claim 1, wherein the pixel electrode includes a reflective electrode, and the opposite electrode includes a transparent electrode.

3. The organic light emitting display device according to one of the preceding claims, wherein the pixel electrode extends into the thin film transistor region and into the capacitor region.

4. The organic light emitting display device according to one of the preceding claims , wherein the organic layer further includes at least one layer selected from the group consisting of a hole injection layer, a hole transporting layer, a hole blocking layer, an electron transporting layer and an electron injection layer.

5. The organic light emitting display device according to one of the preceding claims , wherein the dummy pattern has a laminated structure of at least two materials selected from the group consisting of a polysilicon layer pattern, a gate electrode material, and source and drain electrode materials.

6. The organic light emitting display device according to one of the preceding claims , wherein the pixel defining layer has a thickness of 3,000Å or less.

7. A method of fabricating an organic light emitting display device, comprising:

   forming first conductive layer patterns on a substrate that is divided into a first region, a second region and a third region, respectively;
   forming a first insulating layer on the substrate and on the first conductive layer patterns;
   forming second conductive layer patterns on the first insulating layer in the first region, the second region and the third region, respectively;
   forming a second insulating layer on an entire surface of the second conductive layer and on exposed portions of the first insulating layer;
   forming third conductive layer patterns on the second insulating layer in first region, the second region and the third region, respectively;
   forming a third insulating layer on an entire surface of the third conductive layer and on exposed portions of the second insulating layer;
   forming a pixel electrode on the third insulating layer in the first region, the pixel electrode adapted to be connected to the third conductive pattern in the second region;
   forming a fourth insulating layer on the pixel electrode and on exposed portions of the third insulating layer;
   patterning the fourth insulating layer to expose at least a portion of the pixel electrode in the first region;
   forming an organic layer on the exposed portion of the pixel electrode, the organic layer including at least an emission layer; and
   forming an opposite electrode on at least the organic layer.

8. The method of claim 7, wherein the first region is an emission region, the second region is a thin film transistor region, and the third region is a capacitor region.

9. The method according to one of the claims 7 or 8, wherein the first conductive layer patterns include a first dummy pattern, a polysilicon layer pattern in-

cluding a channel region and source and drain regions, and a first electrode of a capacitor, and / or the second conductive layer patterns include a second dummy pattern, a gate electrode, and a second electrode of a capacitor.

10. The method according to one of the claims 7 to 9 , wherein the first insulating layer is a gate insulating layer.

11. The method according to one of the claims 7 to 10 , wherein the second insulating layer is an interlayer insulating layer.

12. The method according to one of the claims 7 to 11 , wherein the third conductive layer patterns include a third dummy pattern, source and drain electrodes, and a third electrode of a capacitor.

13. The method according to one of the claims 7 to 12 , wherein the third insulating layer includes either a passivation layer and a planarization layer or a laminated layer of the passivation layer and the planarization layer.

14. The method according to one of the claims 7 to 13 , wherein the pixel electrode comprises reflective material.

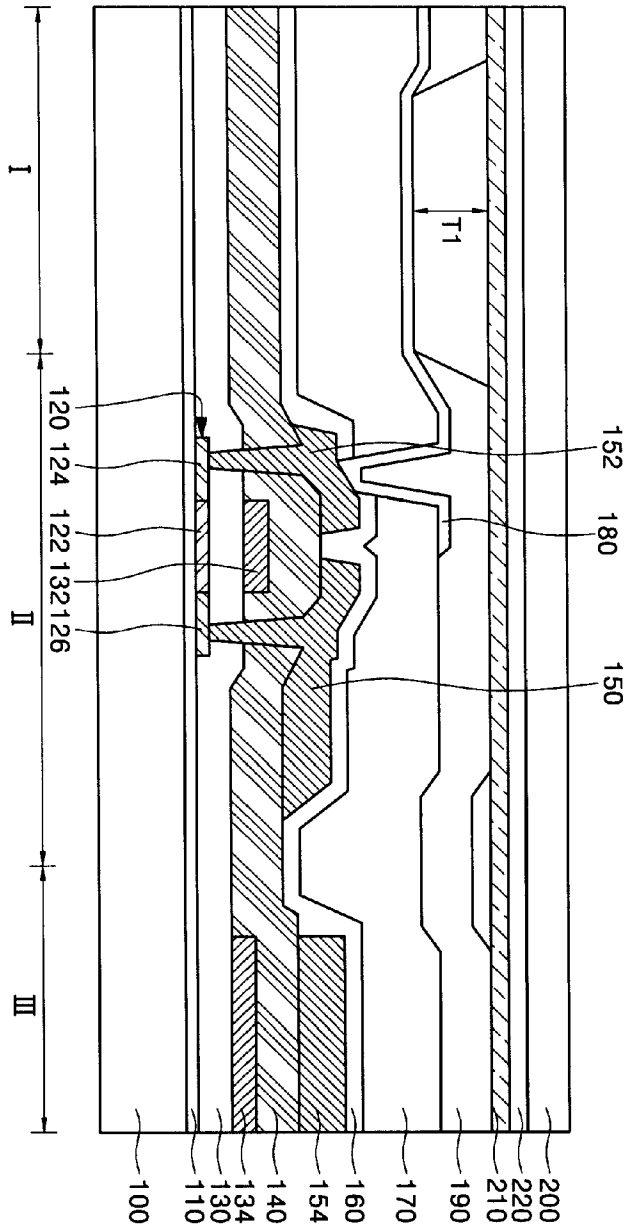
15. The method according to one of the claims 7 to 14 , wherein the pixel electrode is formed throughout the first region, the second region and the third region.

16. The method according to one of the claims 7 to 15 , wherein the patterned fourth insulating layer is a pixel defining layer.

17. The method according to one of the claims 7 to 16 , wherein the patterned fourth insulating layer has a thickness of 3,000Å or less.

18. The method according to one of the claims 7 to 17 , wherein the organic layer further includes at least one thin layer selected from the group consisting of a hole injection layer, a hole transporting layer, an electron transporting layer and an electron injection layer.

19. The method according to one of the claims 7 to 18 , wherein the organic layer is produced by a laser-induced thermal imaging (LITI) process.


I
II
III
T1
120
124
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132
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152
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110
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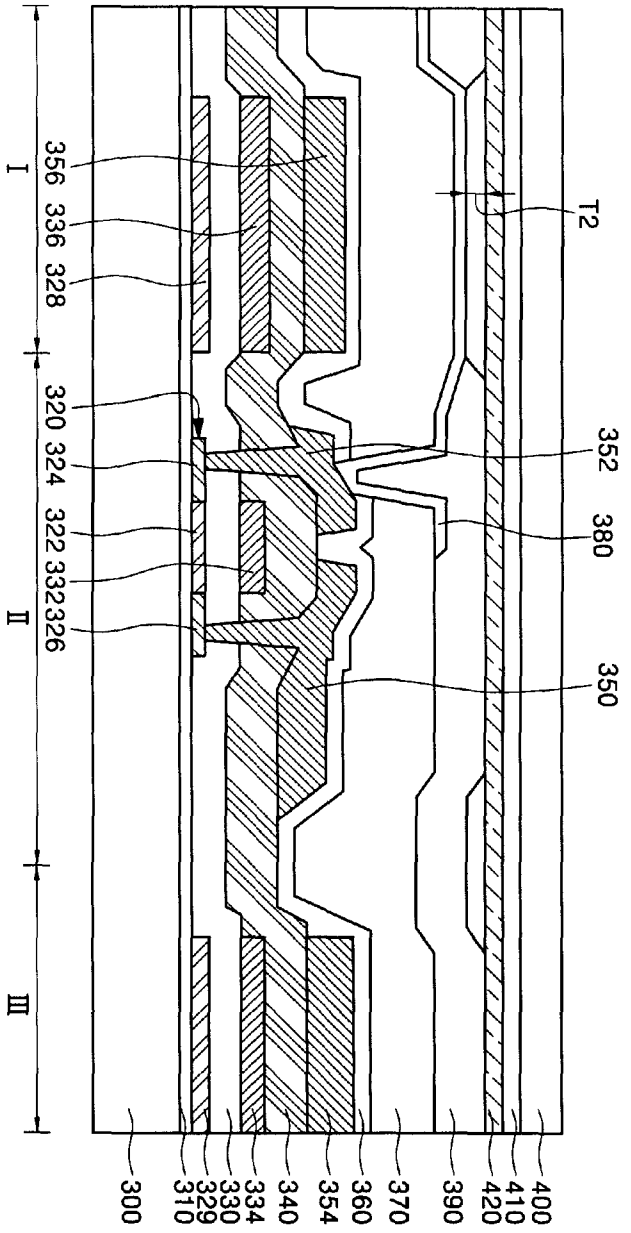
170
190
210
220
200

FIG. 1


I
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328
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324
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332
326
T2
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380
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310
329
330
334
340
354
360
370
390
420
410
400

FIG. 2

专利名称(译)	有机发光显示装置及其制造方法		
公开(公告)号	EP1670081A2	公开(公告)日	2006-06-14
申请号	EP2005111816	申请日	2005-12-08
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
[标]发明人	KANG TAE WOOK		
发明人	KANG, TAE-WOOK		
IPC分类号	H01L51/40 H01L27/32 H01L51/56		
CPC分类号	H01L27/3244 H01L27/1214 H01L27/1255 H01L27/13 H01L27/3223 H01L51/0013 H01L51/56 H01L2251/5315		
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优先权	1020040105146 2004-12-13 KR		
其他公开文献	EP1670081B1 EP1670081A3		
外部链接	Espacenet		

摘要(译)

有机发光显示装置及其制造方法。在制造薄膜晶体管的同时，在发光区域（I）中形成虚设图案（328,336,356）以通过电极材料增加发光区域（I）的台阶高度，使得像素电极和施主之间的距离在制造有机层期间，膜（T2）减少。这种减小的距离（T2）使用激光诱导的热成像减少了用于转移的激光能量，从而改善了器件的寿命和效率。此外，像素电极（380）可以延伸到薄膜晶体管区域（II）和电容器区域（III）中，从而增强孔径比。

FIG. 2