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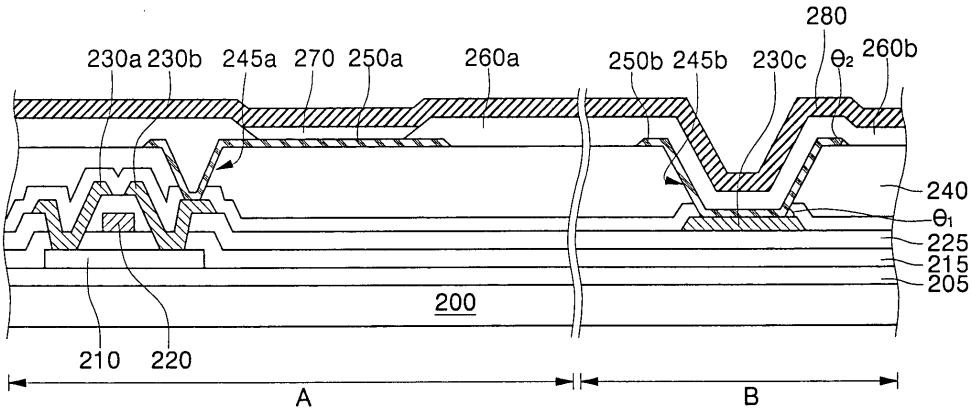
(54) Organic light emitting display with circuit measuring pad and method of fabricating the same

(57) An organic light emitting display and method of fabricating the same are disclosed. The light emitting display includes: a substrate having a display region and a circuit measuring pad region; source and drain electrodes arranged above the display region and a first conductive layer arranged above the circuit measuring pad region on the same layer as the source and drain electrodes; a first insulating layer on the source and drain electrodes and the first conductive layer; first and second via holes formed in the first insulating layer, the first via hole exposing the source or drain electrode, the second via hole exposing the first conductive layer; a pixel electrode contacting the source or drain electrode through the first via hole, and a second conductive layer contacting the first conductive layer through the second via hole; and a pixel defining layer which exposes the pixel electrode and formed on the second conductive layer.

FIG. 5



EP 1 635 407 A1

Description

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 2004-70087, filed September 2, 2004, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to an organic light emitting display with a circuit measuring pad and method of fabricating the same and, more particularly, to an organic light emitting display with a circuit measuring pad which may prevent a short circuit between the circuit measuring pad and an opposite electrode and method of fabricating the same.

2. Description of the Related Art

[0003] Among flat panel displays, an organic light emitting display (OLED) has a fast response speed of 1ms or less, low power consumption, and a wide viewing angle due to an emissive display, and thus it has an advantage as a medium displaying a moving picture regardless of its size. Also, the OLED may be fabricated at low temperature and has a simplified manufacturing process since it employs the existing semiconductor manufacturing process technologies, and thus it attracts public attention as the next flat panel display.

[0004] The OLED is fabricated by forming a thin film transistor (TFT) array having a plurality of TFTs and capacitors on a substrate using a semiconductor manufacturing process, and depositing an organic layer having an emission layer on an emission region of the substrate on which the TFT array is formed.

[0005] In the OLED, a silicon semiconductor and metal electrodes are organically connected to each other through contact holes, and a pixel electrode which is patterned corresponding to each unit pixel is supplied with an electrical current for driving a light emitting element by the TFT connected thereto through a via hole.

[0006] Driving circuit measuring pads are arranged at the periphery of a display region in which the unit pixels of the OLED are formed. The driving circuit measuring pads are formed to check if circuit operation of the OLED is normally performed, during a manufacturing process.

[0007] However, the driving circuit measuring pad may cause a short circuit with an opposite electrode formed on the display region of the OLED, leading to failure of the OLED and low reliability of the OLED.

SUMMARY OF THE INVENTION

[0008] The present invention, therefore, solves aforementioned problems associated with conventional devices by providing a circuit measuring pad which may prevent a short circuit between the circuit measuring pad and an opposite electrode to thereby improve reliability of a display, an OLED with the circuit measuring pad, and method of fabricating the same.

[0009] The present invention also provides a method of improving a manufacturing process of the OLED by implementing the OLED having a thin pixel defining layer.

[0010] In an exemplary embodiment of the present invention, an organic light emitting display includes: a substrate having a display region and a circuit measuring pad region; source and drain electrodes arranged above the display region, and a first conductive layer arranged above the circuit measuring pad region on the same layer as the source and drain electrodes; a first insulating layer arranged on the source and drain electrodes and the first conductive layer; first and second via holes formed in the first insulating layer, the first via hole exposing the source or drain electrode, the second via hole exposing the first conductive layer; a pixel electrode contacting the source or drain electrode through the first via hole, and a second conductive layer contacting the first conductive layer through the second via hole; and a pixel defining layer which exposes the pixel electrode and formed on the second conductive layer.

[0011] In another exemplary embodiment according to the present invention, a method of fabricating an organic light emitting display includes: preparing a substrate having a display region and a circuit measuring pad region; depositing and patterning a conductive layer on the substrate to form a first conductive layer above the circuit measuring pad region while forming source and drain electrodes above the display region; forming a first insulating layer on the source and drain electrodes and the first conductive layer; simultaneously forming first and second via holes in the first insulating layer, the first via hole exposing the source or drain electrode, the second via hole exposing the first conductive layer; depositing and patterning a conductive layer to form a pixel electrode contacting the source or drain electrode through the first via hole, and a second conductive layer contacting the first conductive layer through the second via hole; and depositing and patterning an insulating layer to form a pixel defining layer which exposes the pixel electrode above the display region and covers the second conductive layer above the circuit measuring pad region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The above and other features of the present invention will be described in reference to certain exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a plan view of an OLED according to the present invention;

FIGS. 2 to 5 are cross-sectional views taken along

the line I - I ' in FIG. 1, which illustrate a method of fabricating an OLED according to a first embodiment of the present invention; and

FIGS. 6 to 8 are cross-sectional views illustrating a method of fabricating an OLED according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0014] FIG. 1 is a plan view of an organic light emitting display (OLED) according to the present invention.

[0015] Referring to FIG. 1, the OLED includes a display region 5 having unit pixels and circuit portions 3a and 3b for driving the display region 5. The circuit portions 3a and 3b include a data driver region 3a and a scan driver region 3b. Each of the circuit portions 3a and 3b includes thin film transistors (TFTs) corresponding to the respective pixels, and is connected to the display region 5 via an interconnection line. Scan lines and data lines are arranged in the display region 5 to transfer signals from the data driver region 3a and the scan driver region 3b of the circuit portions 3a and 3b, and each signal is applied to a designated pixel to operate the OLED.

[0016] A circuit measuring pad 15 may be arranged on a region 15a between an emission region and the data driver region 3a or on one side 15b of an edge of the OLED. The circuit measuring pad 15 is formed at the same time as the TFTs in the OLED. The circuit measuring pad 15 is connected to the data lines, and thus it is possible to determine if circuit operation is normally performed by checking electrical characteristics through the circuit measuring pad 15.

[0017] FIG. 5 is a cross-sectional view of an OLED according to a first embodiment of the present invention, taken along the line - ' in FIG. 1.

[0018] Referring to FIG. 5, a substrate 200 includes a display region A and a circuit measuring pad region B.

[0019] A buffer layer 205 is arranged on the display region A and the circuit measuring pad region B, and a TFT is arranged on the buffer layer 205 of the display region A. The TFT includes a semiconductor layer 210, a gate insulating layer 215, a gate electrode 220, an inter insulating layer 220, and source and drain electrodes 230a and 230b.

[0020] Insulating layers which are deposited at the same time as the gate insulating layer 215 and the interlayer insulating layer 225 are arranged on the buffer layer 205 of the circuit measuring pad region B.

[0021] A first conductive layer 230c is arranged on the interlayer insulating layer 225 of the circuit measuring pad region B.

[0022] A first insulating layer is arranged on the source and drain electrodes 230a and 230b and the first conductive layer 230c. The first insulating layer may be a passivation layer 235. The first insulating layer may further include a planarization layer 240.

[0023] A first via hole 245a which exposes the source electrode 230a or the drain electrode 230b and a second via hole 245b which exposes the conductive layer 230c are arranged in the first insulating layer. A pixel electrode 250a which is in contact with the source electrode 230a or drain electrode 230b through the first via hole 245a and a second conductive layer 250b which is in contact with the first conductive layer 230c through the second via hole 245b are arranged.

[0024] A taper angle $\theta 1$ of the second via hole 245b may be 50° or less.

[0025] Thickness of the second conductive layer 250b may be in a range of 100 to 1,000 .

[0026] A taper angle $\theta 2$ of an edge of the second conductive layer 250b may be 50° or less.

[0027] A pixel defining layer 260a which exposes the pixel electrode 250a is arranged, an organic layer 270 having an emission layer is arranged on the exposed pixel electrode 260b. A pixel defining layer 260b is also arranged on the second conductive layer 250b. The pixel defining layers 260a and 26b are formed of thin layers and preferably have a thickness of 3,000 or less.

[0028] An opposite electrode 280 is arranged on the pixel defining layers 260a and 260b.

[0029] Even though the pixel defining layers 260a and 260b are formed of thin layers, since the taper angles $\theta 1$ and $\theta 2$ are 50° or less, an insulating layer may be formed to a uniform thickness even on a tapered portion, thereby preventing a short circuit between the circuit measuring pad and the opposite electrode.

[0030] Therefore, the OLED having the thin pixel defining layer may be implemented, and such a structure may improve characteristics of a laser induced thermal imaging process of the OLED.

[0031] Also, reliability of the OLED may be improved by preventing the short circuit.

[0032] FIGS. 2 to 5 are cross-sectional views illustrating a method of fabricating an OLED according to the present invention.

[0033] Referring to FIG. 2, a buffer layer 205 is formed on a substrate 200 having a display region A and a circuit measuring pad region B. Forming the buffer layer 205 is not necessary, but since it serves to prevent impurities from being come into a TFT element from the substrate 200, it is preferable that the buffer layer 205 is formed. The buffer layer 205 may be formed of silicon nitride (SiNx), silicon oxide (SiO_2) or silicon oxynitride (SiO_xN_y).

[0034] A semiconductor layer 210 is formed on a portion of the buffer layer 205 corresponding to the display region A. The semiconductor layer 210 may be formed of amorphous silicon or crystalline silicon.

[0035] A gate insulating layer 215 is formed over the substrate 200 having the semiconductor layer 210. The

gate insulating layer 215 is formed of a typical insulating layer such as a silicon oxide (SiO_2) layer. A gate electrode 220 is formed over the substrate 200 having the gate insulating layer 215.

[0036] Referring to FIG. 3, an inter insulating layer 225 is formed over the substrate 200 having the gate electrode 220. Contact holes are formed in the inter insulating layer 225 to expose source and drain regions of the semiconductor layer 210, respectively. A conductive layer is deposited and patterned on the interlayer insulating layer 225 to form source and drain electrodes 230a and 230b which are in contact with the exposed source and drain regions respectively while forming a first conductive layer 230c above the circuit measuring pad region B.

[0037] A first insulating layer is formed over the substrate 200 having the source and drain electrodes 230a and 230b and the first conductive layer 230c.

[0038] The first insulating layer may be a passivation layer 235. The passivation layer 235 may be formed of a silicon nitride (SiNx) layer or silicon oxide (SiO_2) layer. The passivation layer 235 is preferably formed of a silicon nitride (SiNx) layer for passivation effect and light blocking effect of the semiconductor layer 210.

[0039] A planarization layer 240 may be formed on the passivation layer 235. The planarization layer 240 may be formed of a material selected from a group consisting of polyacrylates resin, epoxy resin, phenolic resin, polyamides resin, polyimides resin, unsaturated polyesters resin, polyphenylenethers resin, polyphenylenesulfides resin, and benzocyclobutene (BCB).

[0040] Referring to FIG. 4, first and second via holes 245a and 245b are formed in the first insulating layer to expose the drain electrode 230b and the first conductive layer 230c.

[0041] A taper angle $\theta 1$ of the first or second via hole may be 50° or less.

[0042] A conductive layer is deposited and patterned over the substrate 200 having the first and second via holes 245a and 245b to form a pixel electrode 250a and a second conductive layer 250b on the first and second via holes 245a and 245b, respectively.

[0043] The electrical characteristics of the circuit measuring pad region B on which the second conductive layer 250b is formed is checked to see if circuit operation is normally performed.

[0044] A reflecting layer may be interposed between the pixel electrode 250a and the planarization layer 240.

[0045] The pixel electrode 250a and the second conductive layer 250b may be formed of indium tin oxide (ITO) or indium zinc oxide (IZO). A taper angle $\theta 2$ of an edge of the second conductive layer 250b may be 50° or less.

[0046] An insulating layer is formed on the pixel electrode 250a and the second conductive layer 250b. The insulating layer is patterned to form pixel defining layers 260a and 260b. The pixel defining layer 260a exposes the pixel electrode 260a, and the pixel defining layer 260b covers and protects the second conductive layer 250b.

[0047] Due to the taper angles $\theta 1$ and $\theta 2$, the pixel defining layer 260b formed above the circuit measuring pad region B may be conformally formed without being broken.

[0048] Referring to FIG. 5, an organic layer 270 is formed on the exposed pixel electrode 250a. The organic layer 270 includes at least one selected from a group consisting of a hole injection layer, a hole transport layer, a hole blocking layer, and an electron injection layer in addition to an emission layer.

[0049] An opposite electrode 280 is formed on the organic layer 270 of the display region A and the pixel defining layer 260b of the circuit measuring pad region B, thereby completing the OLED.

[0050] Therefore, the pixel defining layer 260b is conformally formed without being broken and thus prevents a short circuit between the circuit measuring pad 260b and the opposite electrode 280.

[0051] As a result, the OLED having a thin pixel defining layer may be implemented, and a laser induced thermal imaging process of the OLED to which the thin pixel defining layer should be subjected may be easily performed.

[0052] Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0053] FIG. 6 is a cross-sectional view of an OLED according to a second embodiment of the present invention.

[0054] Referring to FIG. 6, like the first embodiment of the present invention, a substrate 300 includes a display region A on which source and drain electrodes 330a and 330b are arranged and a circuit measuring pad region B on which a first conductive layer 330c is arranged.

[0055] A first insulating layer is arranged on the source and drain electrodes 330a and 330b and the first conductive layer 330c. The first insulating layer may be a passivation layer 335. In the second embodiment of the present invention, a planarization layer 340 is formed above only the display region A except the circuit measuring pad region B.

[0056] A taper angle $\theta 1$ of a second via hole may be 50° or less.

[0057] Thickness of a second conductive layer 350b may be in a range of 100 to 1,000 .

[0058] A taper angle $\theta 2$ of an edge of the second conductive layer 350b may be 50° or less.

[0059] A second insulating layer 360b arranged to cover the second conductive layer 350b may be formed of a thin layer having a thickness of 3,000 or less.

[0060] Therefore, like the first embodiment of the present invention, even though a pixel defining layer 360b is a thin layer, since a taper angle $\theta 1$ of the via hole and a taper angle $\theta 2$ of an edge of the second conductive layer 350b are 50° or less, the pixel defining layer 360b may be formed to a uniform thickness even at a tapered portion, thereby preventing a short circuit between the circuit measuring pad B and an opposite electrode 380.

[0061] As a result, the OLED having a thin pixel defin-

ing layer may be implemented, and a laser induced thermal imaging process of the OLED to which the thin pixel defining layer should be subjected may be easily performed. Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0062] FIGS. 6 to 8 are cross-sectional views illustrating a method of fabricating an OLED according to a second embodiment of the present invention.

[0063] Referring to FIG. 7, like the first embodiment, a buffer layer 305 is formed on a substrate 300 having a display region A and a circuit measuring pad region B. A semiconductor layer 310, a gate electrode 320, and source and drain electrodes 330a and 330b are formed on a portion of the buffer layer 305 above the display region A, thereby forming a TFT.

[0064] Like the first embodiment, a first conductive layer 330c is formed at the same time as the source and drain electrodes 330a and 330b, above the circuit measuring pad region B. Then, a first insulating layer is formed over the substrate having the source and drain electrodes 330a and 330b and the first conductive layer 330c. The first insulating layer may be a passivation layer 335.

[0065] A planarization layer 340 may be formed on the passivation layer 335.

[0066] The planarization layer 340 is subjected to an exposure process using a halftone mask 400 which has portions 400a to 400c different in exposure level based on via holes of the display region and the circuit measuring pad region, and portions of the display regions and the circuit measuring pad region around the via holes.

[0067] Referring to FIG. 8, by the exposure process, a first via hole which exposes the drain electrode 330b and a second via hole which exposes the first conductive layer 330c are formed while forming an opening which exposes the circuit measuring pad region in the planarization layer 340. That is, using the halftone mask 400, a portion of the planarization layer 340 corresponding to the display region A remains, and a portion of the planarization layer 340 corresponding to the circuit measuring pad region B is removed.

[0068] A taper angle $\theta 1$ of the first or second via hole may be 50° or less.

[0069] A conductive layer is deposited over the substrate having the first and second via hole and then patterned to form a pixel electrode 350a on the first via hole and a second conductive layer 350b on the second via hole.

[0070] The electrical characteristics of the circuit measuring pad portion B on which the second conductive layer 350b is formed are check to see if circuit operation is normally performed.

[0071] Like the first embodiment of the present invention, a reflecting layer may be interposed between the pixel electrode 350a and the planarization layer 340.

[0072] Also, the pixel electrode 350a and the second conductive layer 350b may be formed of ITO or IZO, and a taper angle of an edge of the second conductive layer 350b may be 50° or less.

[0073] Referring to FIG. 6, an insulating layer is formed on the pixel electrode 350a and the conductive layer 350b. The insulating layer is patterned to form pixel defining layers 360a and 360b. The pixel defining layer 360a exposes the pixel electrode 350a, and the pixel defining layer 360b covers and protects the second conductive layer 350b.

[0074] Due to the taper angles $\theta 1$ and $\theta 2$, the pixel defining layer 360b formed above the circuit measuring pad region B may be conformably formed without being broken.

[0075] An organic layer 370 is formed on the exposed pixel electrode 350a. The organic layer 370 includes at least one selected from a group consisting of a hole injection layer, a hole transport layer, a hole blocking layer, and an electron injection layer in addition to an emission layer.

[0076] An opposite electrode 380 is formed on the organic layer 370 of the display region A and the pixel defining layer 360b of the circuit measuring pad region B, thereby completing the OLED.

[0077] Therefore, the pixel defining layer 360b is conformally formed without being broken and thus prevents a short circuit between the circuit measuring pad 360b and the opposite electrode 380.

[0078] As a result, the OLED having a thin pixel defining layer may be implemented, and a laser induced thermal imaging process of the OLED to which the thin pixel defining layer should be subjected may be easily performed.

[0079] Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0080] As described above, the OLED of the present invention may prevent a short circuit between the circuit measuring pad and the opposite electrode even at the tapered portion of the circuit measuring pad due to its uniform thickness. The OLED having a thin pixel defining layer may be implemented, and characteristics of the laser induced thermal imaging process of the OLED may be improved. Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0081] Although the present invention has been described with reference to certain exemplary embodiments thereof, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the present invention without departing from the spirit or scope of the present invention defined in the appended claims, and their equivalents.

Claims

1. An organic light emitting display comprising:

a substrate having a display region and a circuit measuring pad region;
source and drain electrodes arranged above the display region, and a first conductive layer ar-

ranged above the circuit measuring pad region on the same layer as the source and drain electrodes;
a first insulating layer arranged on the source and drain electrodes and the first conductive layer;
first and second via holes formed in the first insulating layer, the first via hole exposing the source or drain electrode, the second via hole exposing the first conductive layer;
a pixel electrode contacting the source or drain electrode through the first via hole, and a second conductive layer contacting the first conductive layer through the second via hole; and
a pixel defining layer which exposes the pixel electrode and formed on the second conductive layer.

2. The display of claim 1, wherein the second conductive layer has a thickness in a range of 100 to 1,000 .

3. The display of claim 1, wherein the pixel defining layer has a thickness of 3,000 or less.

4. The display of claim 1, wherein the second via hole has a taper angle of 50° or less.

5. The display of claim 1, wherein an edge of the first conducive layer has a taper angle of 50° or less.

6. The display of claim 1, wherein the first insulating layer is a passivation layer.

7. The display of claim 6, wherein the first insulating layer further includes a planarization layer arranged on the passivation layer.

8. The display of claim 7, wherein the second via hole has a taper angle of 50° or less.

9. The display of claim 7, wherein the planarization layer includes an opening which exposes the circuit measuring pad region, and the second via hole is arranged in the passivation layer.

10. A method of fabricating an organic light emitting display, comprising:

preparing a substrate having a display region and a circuit measuring pad region;
depositing and patterning a conductive layer on the substrate to form a first conductive layer above the circuit measuring pad region while forming source and drain electrodes above the display region;
forming a first insulating layer on the source and drain electrodes and the first conductive layer;
simultaneously forming first and second via holes in the first insulating layer, the first via hole exposing the source or drain electrode, the second via hole exposing the first conductive layer;
depositing and patterning a conductive layer to form a pixel electrode contacting the source or drain electrode through the first via hole, and a second conductive layer contacting the first conductive layer through the second via hole; and
depositing and patterning an insulating layer to form a pixel defining layer which exposes the pixel electrode above the display region and covers the second conductive layer above the circuit measuring pad region.

11. The method of claim 10, wherein forming the first insulating layer includes forming a passivation layer.

12. The method of claim 11, wherein forming the first insulating layer further includes forming a planarization layer on the passivation layer.

13. The method of claim 12, wherein the second via hole has a taper angle of 50° or less.

14. The method of claim 12, wherein while the first and second via holes are formed using a halftone mask, an opening which exposes the circuit measuring pad region is formed in the planarization layer.

15. The method of claim 10, further comprising forming an organic layer having an emission layer on the exposed pixel electrode, and forming an opposite electrode above the display region having the organic layer and above the circuit measuring pad region having the second insulating layer.

16. The method of claim 10, wherein the second conductive layer has a thickness in a range of 100 to 1,000 .

17. The method of claim 10, wherein the pixel defining layer has a thickness of 3,000 or less.

18. The method of claim 10, wherein the first via hole has a taper angle of 50° or less.

19. The method of claim 10, wherein an edge of the first conductive layer has a taper angle of 50° or less.

FIG. 1

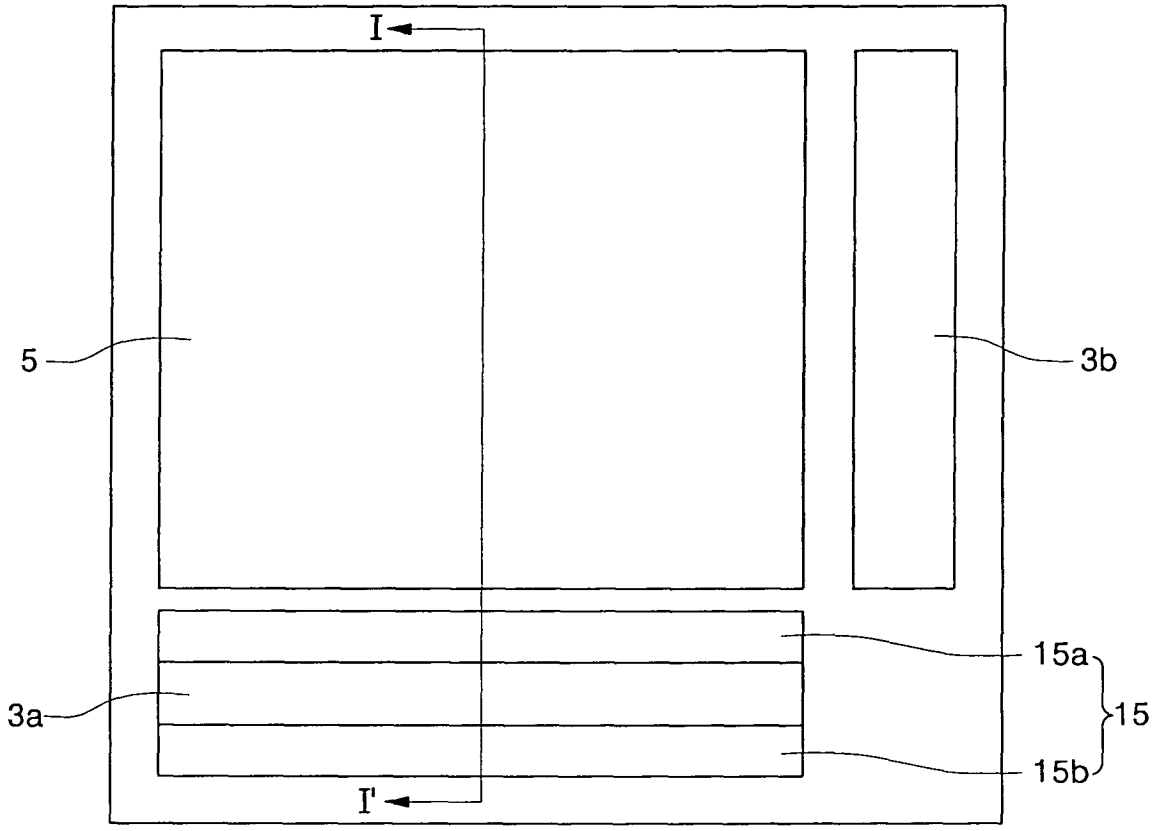


FIG. 2

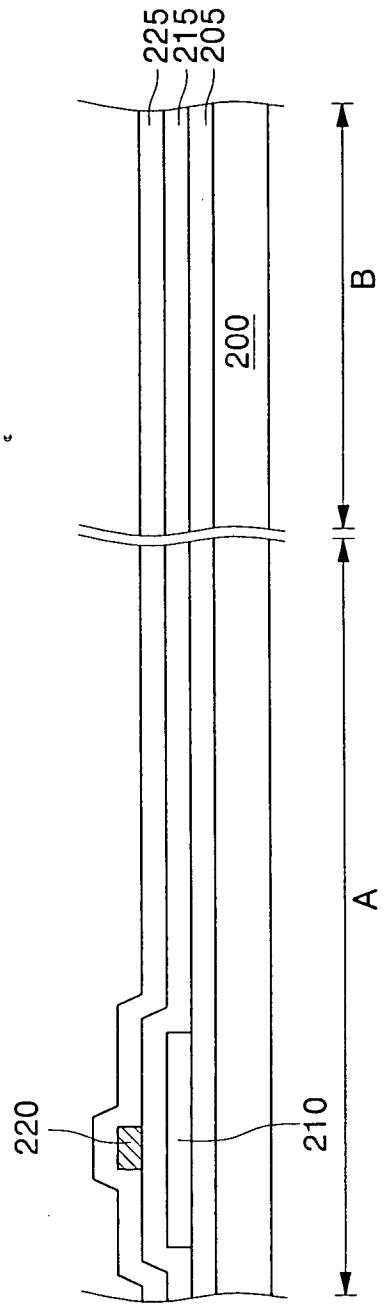


FIG. 3

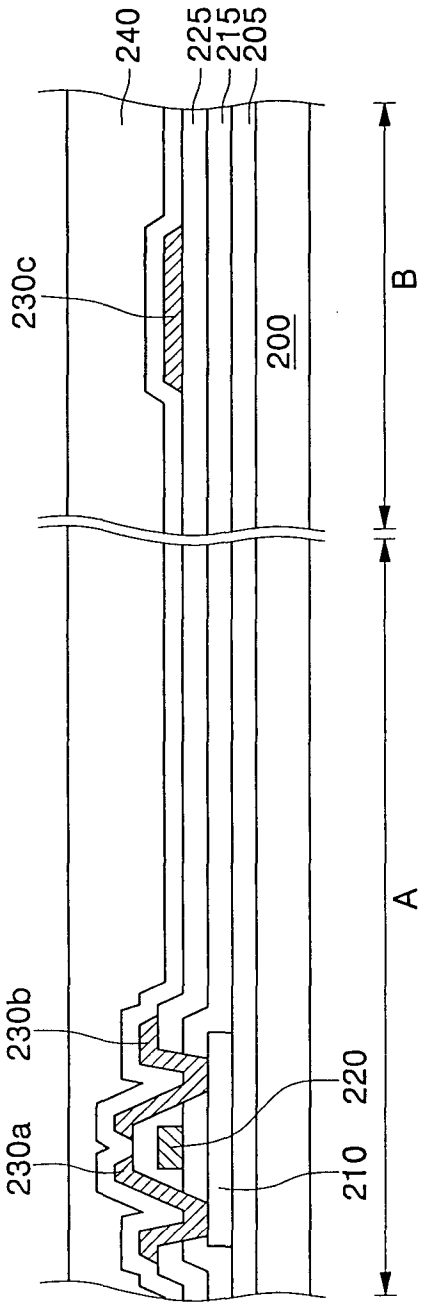


FIG. 4

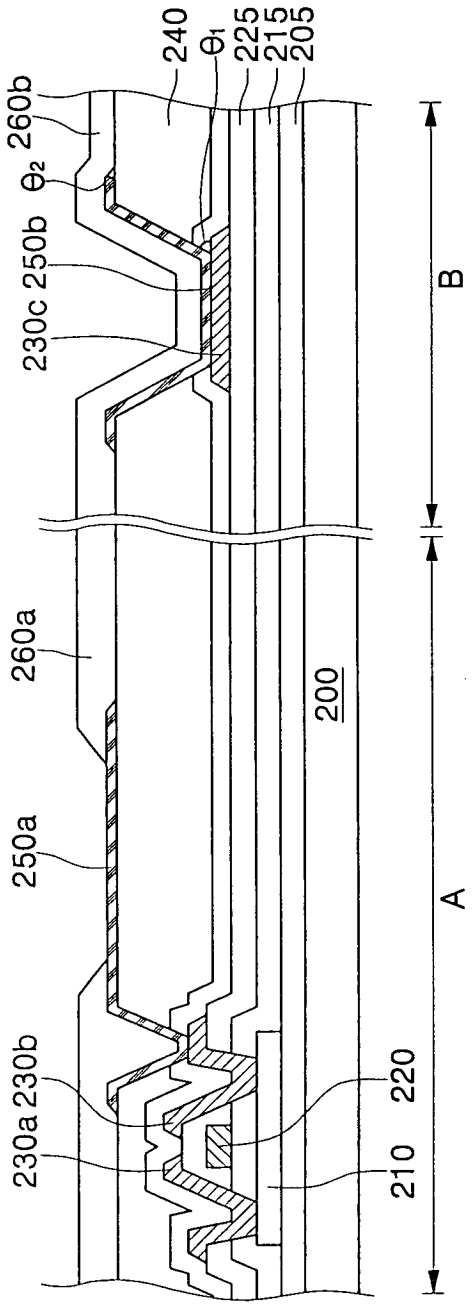
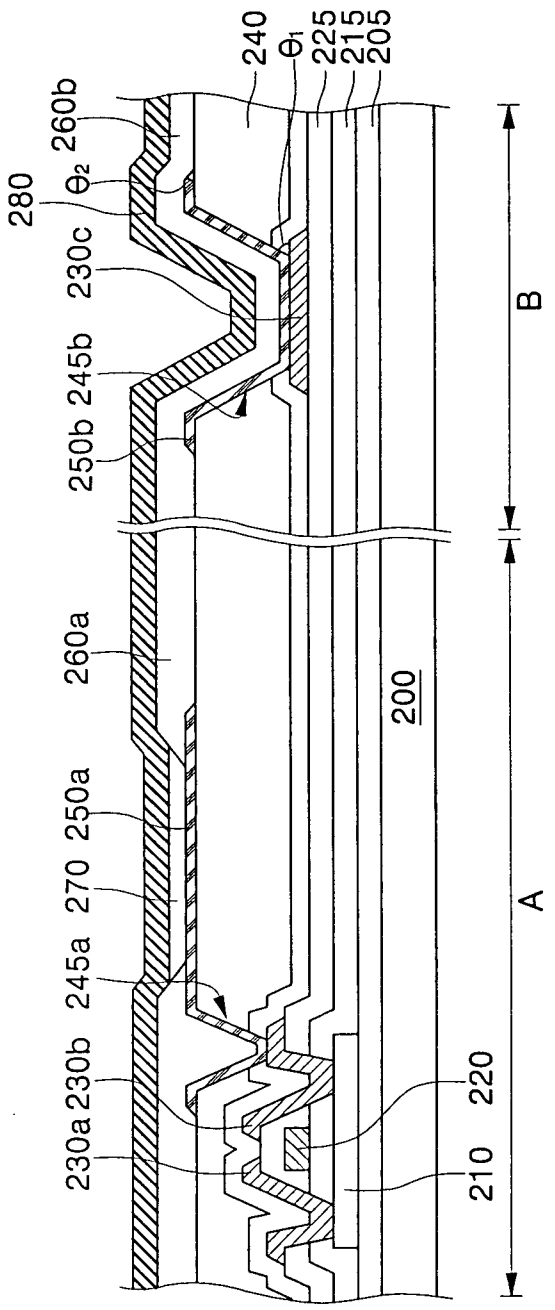

240
θ1
225
215
205
260b
θ2
250b
230c
B
260a
200
250a
A
230b
220
230a
210

FIG. 5


240
θ1
225
215
205
260b
θ2
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230c
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250b
260a
250a
270
245a
230b
230a
200
220
210
B
A

FIG. 6

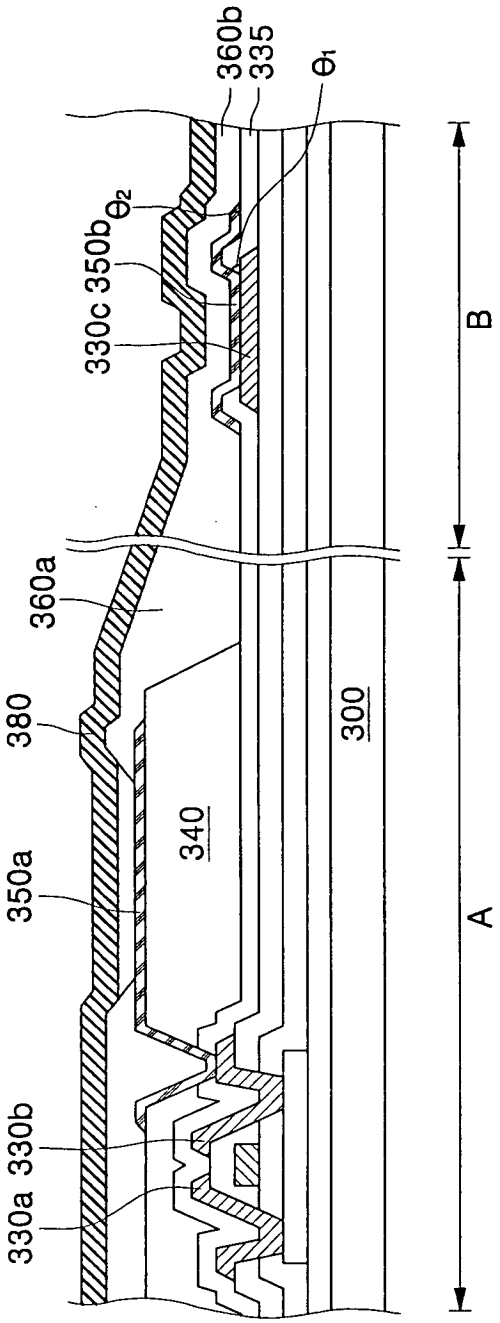
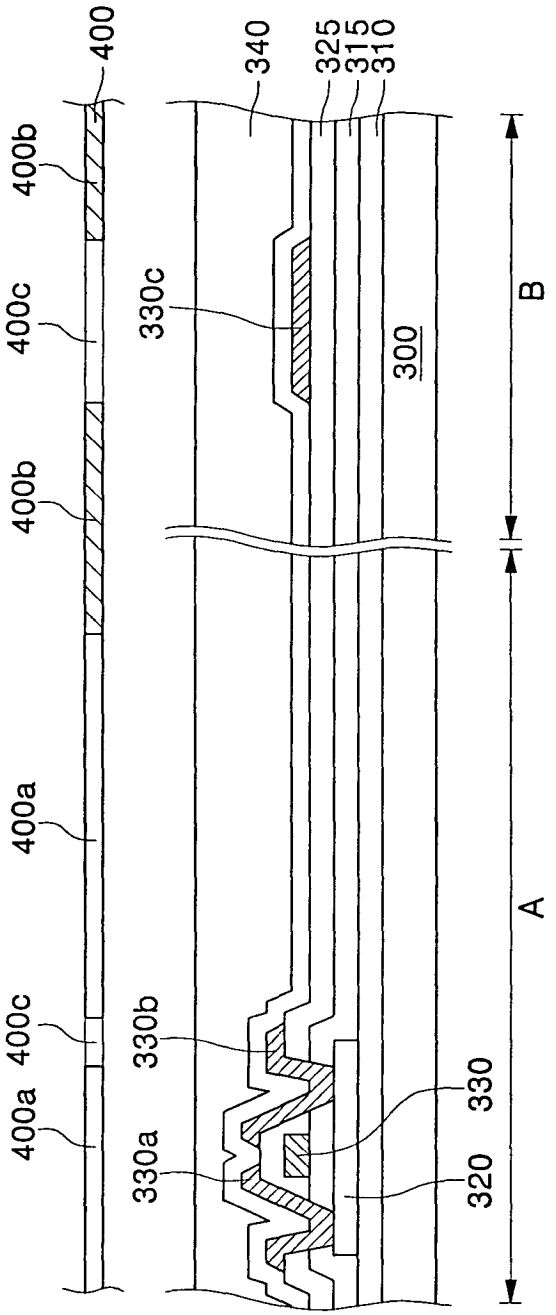


FIG. 7


400
340
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315
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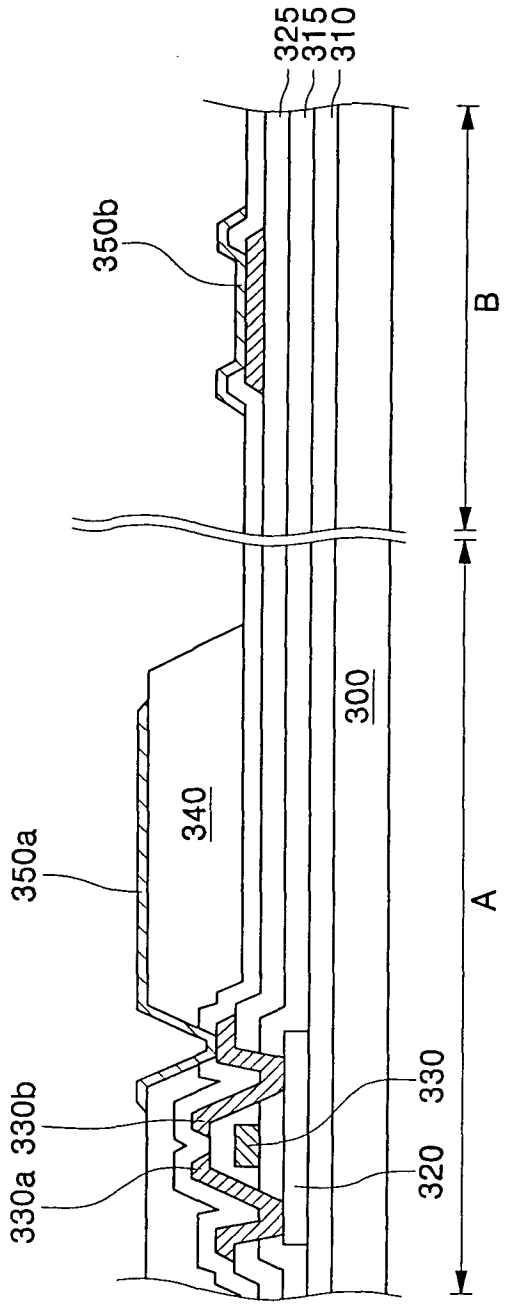
FIG. 8



European Patent Office

PARTIAL EUROPEAN SEARCH REPORT

which under Rule 45 of the European Patent Convention shall be considered, for the purposes of subsequent proceedings, as the European search report

Application Number EP 04 09 0505

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 2003/180975 A1 (FUJITA SHIN) 25 September 2003 (2003-09-25) * paragraphs [0114], [0116]; figures 5,7,9,21 *	1,4,6, 10,11, 13,18,19	H01L51/20 H01L21/66 H01L51/40
A		7-9, 12-15	

A	WO 2004/062323 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD) 22 July 2004 (2004-07-22) * the whole document *	1,4-15, 18,19	
P,A	-& US 2004/246432 A1 (TSUCHIYA KAORU ET AL) 9 December 2004 (2004-12-09)		

A	US 2003/140982 A1 (SEKI SHUNICHI ET AL) 31 July 2003 (2003-07-31) * paragraphs [0097], [0098]; figures 2a,3 *	1,7-10, 12-14	

	-/--		TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L

INCOMPLETE SEARCH

The Search Division considers that the present application, or one or more of its claims, does/do not comply with the EPC to such an extent that a meaningful search into the state of the art cannot be carried out, or can only be carried out partially, for these claims.

Claims searched completely :

Claims searched incompletely :

Claims not searched :

Reason for the limitation of the search:

see sheet C

Place of search	Date of completion of the search	Examiner
Berlin	10 May 2005	Voignier, V

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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EPO FORM 1503 03.82 (P04C07)

European Patent Office

PARTIAL EUROPEAN SEARCH REPORT

Application Number
EP 04 09 0505

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 11, 30 September 1999 (1999-09-30) -& JP 11 168214 A (SEMICONDUCTOR ENERGY LAB CO LTD), 22 June 1999 (1999-06-22) * abstract; figures 2,8 * -----	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)

EPO FORM 1503 03.82 (P04C10) 2

European Patent Office

INCOMPLETE SEARCH SHEET C

Application Number
EP 04 09 0505

Claim(s) searched completely:
1,4-15,18,19

Claim(s) not searched:
2,3,16,17

Reason for the limitation of the search:

The claims do not indicate any units, and it is not possible to derive this information from the description where the units are missing as well.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 09 0505

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The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

10-05-2005

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	具有电路测量垫的有机发光显示器及其制造方法		
公开(公告)号	EP1635407A1	公开(公告)日	2006-03-15
申请号	EP2004090505	申请日	2004-12-22
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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IPC分类号	H01L51/50 H01L51/56 H01L27/32 H01L21/66		
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代理机构(译)	hengelhaupt，Jürgen		
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其他公开文献	EP1635407B1		
外部链接	Espacenet		

摘要(译)

公开了一种有机发光显示器及其制造方法。发光显示器包括：具有显示区域和电路测量垫区域的基板;布置在显示区域上方的源电极和漏电极以及布置在电路测量焊盘区域上方的第一导电层与源电极和漏电极在同一层上;源电极和漏电极上的第一绝缘层和第一导电层;第一和第二通孔形成在第一绝缘层中，第一通孔暴露源或漏电极，第二通孔暴露第一导电层;像素电极通过第一通孔与源电极或漏电极接触，第二导电层通过第二通孔与第一导电层接触;像素限定层，其暴露像素电极并形成在第二导电层上。

FIG. 5