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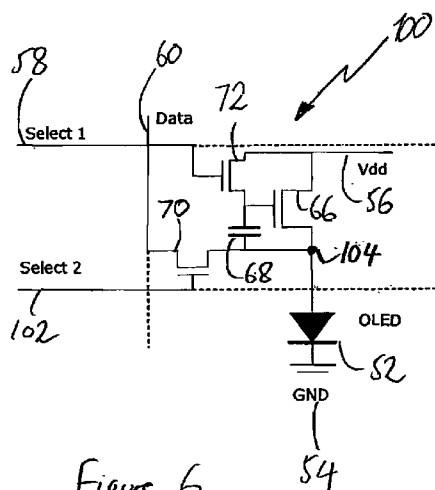


Figure 6

(57) Abstract: A pixel driver circuit is provided for active matrix driving of an organic light emitting diode (OLED). The pixel circuit is characterised by comprising a drive transistor having a current path connected to a first voltage supply line at one end and to an OLED at the other end and a gate terminal connected to a storage element connected between gate and source of the drive transistor to memorise a drive signal for the drive transistor under the control of a first switch transistor having a gate connection to a first selection line and a current path connected between gate and drain of the drive transistor; a second switch transistor having a gate connection to a second selection line, wherein the second switch transistor has a current path connected to the data line at one end and a node at the other end located between the drive transistor and the OLED.

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## PIXEL CIRCUIT

The present invention relates, in general, to a pixel circuit for an active matrix driven organic electroluminescent device.

5

Organic light emitting diodes (OLEDs) comprise a particularly preferred form of electro-optic emitter. Displays fabricated using OLEDs provide a number of advantages over LCD and other flat panel technologies. They are bright, fast switching (compared to LCDs), provide a wide viewing angle and are easy and cheap to fabricate on a variety of substrates.

10

Organic (which here includes organometallic) LEDs may be fabricated using materials including polymers, small molecules and dendrimers, in a range of colours which depend upon the materials employed. Examples of polymer-based OLEDs are described in WO 90/13148, WO 95/06400 and WO 99/48160; examples of dendrimer-based materials are described in WO 99/21935 and WO 02/067343; and examples of so-called small molecule based devices are described in US 4539507.

15

With reference to Figure 1, the general device architecture of an OLED comprises a transparent glass or plastic substrate 1, and anode 2 of indium tin oxide and a cathode 4. An organic electroluminescent layer 3 is provided between anode 2 and cathode 4. Further layers may be located between anode 2 and cathode 4, such as charge transporting, charge injecting or charge blocking layers.

25

Electroluminescent layer 3 may be patterned or unpatterned. For example, a device used as an illumination source may be unpatterned. A device comprising a patterned layer may be a passive matrix display or an active matrix display. In a passive matrix display, the anode 2 is formed of parallel stripes of anode material and the electroluminescent layer 3 is deposited over the striped anode 2. Parallel stripes of the cathode 4 are arranged over the

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electroluminescent layer 3 orthogonal to the parallel stripes of the anode 2. Adjacent stripes of cathode 4 are typically separated by stripes of insulating material – so called “cathode separators”, formed by photolithography. Passive matrix displays are driven using column and row drivers by repetitively scanning the display to address individual pixels along columns and rows represented by the orthogonal anode and cathode stripes respectively. So-called active matrix displays typically have a patterned electroluminescent layer 3 used in combination with a patterned anode 2 and an unpatterned cathode 4. In an active matrix driving scheme each pixel of a display comprises its own associated drive circuitry. The driver circuitry typically comprising at least a memory element such as a capacitor, an address transistor or switching transistor and a drive transistor.

An OLED device may be fully transparent where both anode 2 and cathode 4 are transparent. So called “Top-emitting” OLED devices having transparent cathodes are particularly advantageous for active matrix devices because emission through a transparent anode in such devices is at least partially blocked by drive circuitry located underneath the emissive pixels.

It will be appreciated that a transparent cathode device need not have a transparent anode (unless of course a fully transparent device is desired) and so the transparent anode used for bottom emitting devices may be replaced or supplemented with a layer of reflective material such as a layer of aluminium. Examples of transparent cathode devices are disclosed in, for example, GB 2348316.

Figure 2 shows an example of a voltage controlled OLED active matrix pixel circuit 10. A pixel circuit 10 is provided for each pixel of the display and ground 12, Vss 14, row select 16 and column data 18 bus lines are provided interconnecting the pixels. Accordingly, each pixel has a power and ground connection and each row of pixels has a common row select line 16 and each column of pixels has a common data line 18.

Each pixel has an OLED 20 connected in series with a driver transistor 22 between ground and power lines 12, 14. A gate terminal 24 of driver transistor 22 is connected to a storage capacitor 26 and an addressing transistor 28 connects gate terminal 24 to column data line 18 under the control of row select line 16. The addressing transistor 28 is a thin film Field Effect Transistor (FET) switch which connects column data line 18 to the gate terminal 24 and the capacitor 26 when row select line 16 is activated. In this way, when the addressing transistor 28 is ON a voltage on column data line 18 can be stored on the capacitor 26. This is generally known as programming the pixel circuit. The voltage is retained on the capacitor 26 for at least the frame refresh period because of the relatively high impedances of the gate connection to the driver transistor 22 and of the addressing transistor 28 in an OFF state.

The driver transistor 22 is typically also a FET transistor and passes a (drain-source) current which is dependent upon the transistor's gate voltage less a threshold voltage. The voltage at gate terminal 24 therefore controls the current through OLED 20 and in turn the brightness of OLED 20. The voltage controlled circuit of Figure 2 may suffer from a number of drawbacks, in particular because the OLED 20 emission depends non-linearly on the applied voltage and current control is preferable since the light output from an OLED is proportional to the current it passes. Figure 3 (in which like elements to those of Figure 2 are represented by like reference numerals) illustrates a variant of the circuit of Figure 2 which employs current control. A current on the (column) data line, set by current generator 30 "programs" the current through FET 32, which in turn sets the current through OLED 20 since when transistor 28a is ON (matched) transistors 32 and drive transistor 22 form a current mirror.

Where the active matrix drive circuitry comprises organic thin film transistors (OTFTs) or transistors fabricated in LTPs (Low Temperature Polysilicon) the transistors are generally referred to as p-type devices.

Where the active matrix drive circuitry comprises transistors fabricated in hydrogenated amorphous silicon (a-Si:H) the transistors are generally referred to as n-type devices.

- 5 One problem encountered in FET technology (a-Si:H and LTPs) is shift in threshold voltage ( $V_{th}$ ) for continuous operation. Generally, the shift in  $V_{th}$  for a-Si:H transistors is very sensitive to voltage stress. Application of the high voltages above threshold needed for a drive transistor causes large changes in threshold voltage. This manifests itself as different driving transistors passing  
10 different driving currents to an OLED for the same applied programming signal. Accordingly, this may result in a problem of non-linearities in brightness of pixels across a display.

One approach to solve the aforementioned problem has been put forward by  
15 Shirasaki, T et al (hereinafter Shirasaki) in "Solution for Large-Area Full-Color OLED Television Light Emitting Polymer and a-Si TFT Technologies" vol II, p275-278, December 2004 in Proceedings of International Display Workshop (IDW) and available on-line at [http://hat-lab.ed.kyusha-u.ac.jp/Documents/AMD3\\_OLED5-1.pdf](http://hat-lab.ed.kyusha-u.ac.jp/Documents/AMD3_OLED5-1.pdf). This paper discloses a three  
20 transistor a-Si TFT pixel circuit in which it is purported that the pixel circuit and driving scheme can compensate for instability caused by a shift in threshold voltage.

Referring to Figures 4a and 4b which illustrate in Figure 4a, a pixel circuit of  
25 Shirasaki and in Figure 4b an associated timing chart for the pixel circuit of Figure 4a, it is seen that during driving of the pixel circuit, the source voltage,  $V_{Source}$  must be varied such that during the writing stage  $V_{Source}$  is low and during the holding or driving stage  $V_{Source}$  returns to high. In some cases this may not be desirable, for example, if existing "off the shelf" driver components are used,  
30 a standard LCD row driver may not be able to provide these varying non-standard signals. The modulation of  $V_{Source}$  can also cause some modification of the capacitance thereby reducing the drive current  $I_{T3}$  below that intended.

Other methods suggested for compensation schemes require more complicated pixel circuit configurations and drive schemes. In any device, there exists an upper limit on the amount of "real-estate" for additional devices together with a need to keep fabrication simple. Moreover, an aperture ratio of a display, defined generally as the space occupied by viewable emitting pixels compared to that used by bus lines or devices is reduced the more devices or lines that are included as a device.

10 A further parameter which affects the light emission of an OLED over time comes from the OLED itself and in particular due to aging of the OLED. As OLEDs age they generally become less efficient causing a loss of light output. The loss of light output is generally thought to arise from a decrease in current-to-photon conversion efficiency and from an increase in OLED resistance that results in a reduction of current through the OLED for a given drive signal.

15 It is desirable to provide an improved pixel circuit which seeks to compensate for threshold variation in a drive transistor of the pixel circuit.

20 It is also desirable to provide an improved pixel circuit which seeks to compensate for OLED aging.

It is also desirable to provide an improved pixel circuit that reduces the number of bus lines so that the aperture ratio of the device can be increased.

25

According to a first aspect of the present invention there is provided a pixel driver pixel driver circuit for driving an organic light-emitting diode (OLED) comprising: a first selection line; a second selection line; a data line; a first voltage supply line; and a drive transistor having a current path connected to the first voltage supply line at one end and the OLED at the other end and a gate terminal connected to a storage element connected between gate and source of the drive transistor to memorise a drive signal for the drive transistor under the control of a first switch transistor having a gate connection to the first selection line and a current path connected between gate and drain of the drive transistor; a second switch transistor having a gate connection to the second selection line, wherein the second switch transistor has a current path connected to the data line at one end and a node at the other end located between the drive transistor and the OLED.

15 In a further embodiment, a third selection line and a third switch transistor having a gate connection to the third selection line is provided, wherein the third switch transistor is located in the current path of the drive transistor in series between the OLED and drive transistor.

20 Preferably, the first selection line is a non-inverted selection line and the third selection line is an inverted selection line such that when the first selection line is HIGH the third selection line is LOW.

More preferably, the first and second selection lines are common.

25

Preferably, the first voltage supply line and another selection line are formed as a combined voltage supply and selection line.

30 Preferably, the first voltage supply line and another selection line are formed as a combined voltage supply and selection line and wherein the first and second selection lines are common.

In a further embodiment, the another selection line is the first selection line of a neighbouring pixel circuit sharing a common data line.

In embodiments of the present invention, the drive transistor is an n-type transistor and preferably fabricated from amorphous silicon.

Preferably, the OLED has a current path such that an anode terminal of the OLED is connected to the drive transistor.

10 The present invention also provides a plurality of pixel driver circuits as described above and arranged in row and columns, each data line being shared by each pixel circuit in a column and each combined voltage supply line and all selection lines being shared by each pixel circuit in a row, wherein, for a particular column and during addressing the combined voltage supply and  
15 selection line of the n-1th pixel driver circuit acts as the first voltage supply line to the nth pixel driver circuit and the combined voltage supply and selection line of the n+1th pixel driver circuit acts as a selection line to the nth pixel driver circuit.

20 Preferably, the pixel driver circuits are arranged in row and columns to form the display and each data line is shared by each pixel circuit in a column and each selection line is shared by each pixel circuit in a row.

Preferably, the second switch transistor is connected to a voltage sensing  
25 device for sensing a voltage drop across an OLED and for generating a sensed voltage drop signal to a controller for adjusting the drive signal in response to the sensed voltage drop signal.

More preferably, the sensed voltage drop signal is provided to a lookup table for  
30 storing voltage data representing a relationship between voltage and drive signal for a characteristic OLED and the controller being programmed to adjust the drive signal in response to the relationship.

In embodiments the voltage sensing device is for sensing the voltage drop of all the OLEDs of the display and a plurality of voltage sensing devices are provided, each for sensing a voltage drop on a sub-set of the OLEDs of the display. The sensed voltage drop sensed by the voltage sensing device can be a combination of the voltage drops across a plurality of the OLEDs.

Preferably, the present invention further provides an active matrix display device further comprising a module for determining a transistor characteristic of a transistor of a pixel driver circuit from the sensed voltage drop signal.

The determined transistor characteristic can be a threshold voltage shift of the drive transistor. Particularly, the pixel driver circuits are current-programmed.

According to a second aspect of the present invention, there is provided a pixel driver circuit for driving an organic light-emitting diode (OLED) comprising: a first selection line; a data line; a first voltage supply line; and a drive transistor having a current path connected to the first voltage supply line at one end and the OLED at the other end and a gate terminal connected to a storage element connected to the data line to memorise a drive signal for the drive transistor under the control of first and second switch transistors having gate connections to the first selection line; a third switch transistor having a gate connection to a second selection line, wherein the third switch transistor is located in the current path of the drive transistor in series between the OLED and drive transistor.

25

Preferably, the first selection line is a non-inverted selection line and the second selection line is an inverted selection line such that when the first selection line is HIGH the second selection line is LOW. More preferably, the first voltage supply line and another selection line are formed as a combined voltage supply and selection line and optionally the another selection line is the first selection line.

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Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a prior art example of an organic electroluminescent device;

5 Figure 2 is a prior art example of a voltage driven active matrix OLED pixel circuit;

Figure 3 is a prior art example of a current driven active matrix OLED pixel circuit;

10 Figure 4a is a prior art example of a current driven active matrix OLED pixel circuit;

Figure 4b is a timing diagram for the pixel circuit illustrated in Figure 4a;

Figure 5 is a pixel circuit according to a first embodiment of the present invention;

15 Figure 6 is a pixel circuit according to a second embodiment of the present invention; and

Figure 7 is a pixel circuit according to a third embodiment of the present invention.

20 Referring to Figure 5, a first embodiment of the present invention illustrates a pixel circuit 50. Such a pixel circuit 50 is provided for each OLED 52 of the overall display (not shown) of pixels. A ground 54, supply voltage rail 56, first row select 58 and column data 60 lines are provided interconnecting the pixels.

25 A second row select line 62 is also provided interconnecting the pixels. Accordingly each pixel circuit 50 has a common ground 54, supply voltage rail 56, and each pixel has a common first and second row select line 58, 62 and column data line 60.

30 The OLED 52 is connected in series with a first transistor 64 and a drive transistor 66 between supply voltage rail 56 and ground 54. The cathode terminal of the OLED 52 is connected to ground 54 and the anode terminal is connected to the supply voltage rail 56 by way of the series connection with the

first transistor 64 and drive transistor 66. A gate terminal of the first transistor 64 is connected to and thereby under the control of the second row select line 62.

5 The drive transistor 66 has a gate terminal connected to a first terminal of a storage capacitor 68, a second terminal of which is connected to a first terminal of a switch transistor 70. A gate terminal of the switch transistor 70 is connected to and thereby under the control of the first row select line 58. A second terminal of the switch transistor 70 is connected to the column data line  
10 60. A second transistor 72 has a gate terminal connected to and thereby under the control of the first row select line 58, a first terminal connected to the first terminal of storage capacitor 68 and gate terminal of the drive transistor 66 and a second terminal connected to the supply voltage rail 56.

15 In operation, the pixel circuit 50 comprises a supply voltage V<sub>dd</sub> being applied across the pixel circuit 50 from the supply voltage rail 56 to ground 54. The programming stage comprises the first row select line 58 being HIGH thereby turning ON the switch transistor 70 and second transistor 72. At the same time, the second row select line 62 which is an inverted row select line compared to  
20 the first row select line 58 is LOW and switches off the first transistor 64. Thus OLED 52 is isolated from the voltage supply line removing a need to modulate the supply voltage between low and high levels. A voltage on column data line 60 can therefore be stored on capacitor 68. During an emission stage the first row select line is LOW thereby turning off the switch transistor 70 and second  
25 transistor 72. At the same time, the second row select line 62 is HIGH enabling the drive transistor 66 and the first transistor 64 to pass a (drain-source) current to the OLED 52.

The pixel circuit 50 of Figure 5 (and Figures 6 and 7 below) are current-  
30 controlled with the addition of a current generator (not shown) on the column data line 60 as is known in the art.

Referring to Figure 6, in which like elements to those of Figure 5 are indicated by like reference numerals, a second embodiment of the present invention illustrates a pixel circuit 100. The pixel circuit 100 comprises an additional row select line 102.

5

The switch transistor 70 has a gate terminal connected to the additional row select line 102 and thereby under the control of the additional row select line 102, and a first terminal connected to a second terminal of a storage capacitor 68 and a first terminal connected to a column data line 60.

10

In operation, in a programming stage of the pixel circuit 100, a supply voltage V<sub>dd</sub> is held at a low potential such that there is a substantially zero potential difference across the OLED 52. During the programming stage both the first row select line 58 and additional row select line 102 are HIGH thereby a voltage on column data line 60 can be stored on the capacitor 68. During the emission stage, the supply voltage V<sub>dd</sub> goes to a high potential and the first row select line 58 and additional row select line 102 are LOW. Accordingly, the drive transistor 66 enables a (drain-source) current to pass through the OLED 52.

15

The present embodiment as illustrated in Figure 6 includes a measurement stage whereby the additional select line 102 is HIGH and enabling a voltage drop on the column data line 60 to be measured across the OLED 52 from node 104 to ground 54. Since it is known that the voltage drop across an OLED can vary due to aging of the organic materials, the measured voltage drop is indicative of and can be used to compensate for such aging. Such a voltage drop may be measured and compared with a look up table which via a controller may require the pixel circuit 100 to be programmed with a higher or lower drive signal (voltage or current) on the column data line 60. Individual pixels may be compensated for in this way or a number of pixels may be measured and compensated for row by row or the device may be compensated for as a whole. A voltage drop over a number of OLEDs 52 may be obtained by a combination of voltage drops across a number of OLEDs 52.

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Referring to Figure 7, a third embodiment of the present invention illustrates two pixel circuits 200 and 250. In Figure 7 like elements to these described in Figures 5 and 7 are indicated by like reference numerals. Referring to Figure 7,  
5 a voltage supply line 252 of the pixel circuit 250 is shared with the row select line 254 of adjacent pixel circuit 200. Accordingly, the number of bus lines of the device is reduced. Thus the voltage supply line and row select line are combined and shared between a number of pixel circuits.

10 This embodiment of pixel circuit may be incorporated with embodiments 1 and 2 together or alone if a reduction in the overall number of bus lines in the device is required. Moreover, embodiment 1 may be combined with embodiment 2 if it is desired to implement a pixel circuit capable of providing a compensation for OLED aging without a need to modulate the supply voltage.

15

No doubt many other effective alternatives will occur to the skilled person. It will be understood that the invention is not limited to the described embodiments and encompasses modifications apparent to those skilled in the art lying within the spirit and scope of the claims appended hereto.

**CLAIMS**

1. A pixel driver circuit for driving an organic light-emitting diode (OLED) comprising:
  - 5 a first selection line;
  - a second selection line;
  - a data line;
  - a first voltage supply line; and
  - 10 a drive transistor having a current path connected to the first voltage supply line at one end and the OLED at the other end and a gate terminal connected to a storage element connected between gate and source of the drive transistor to memorise a drive signal for the drive transistor under the control of a first switch transistor having a gate connection to the first selection line and a current path
  - 15 connected between gate and drain of the drive transistor; a second switch transistor having a gate connection to the second selection line, wherein the second switch transistor has a current path connected to the data line at one end and a node at the other end located between the drive transistor and the OLED.
  - 20
2. A pixel driver circuit as claimed in claim 1, further comprising a third selection line and a third switch transistor having a gate connection to the third selection line, wherein the third switch transistor is located in the current path of the drive transistor in series between the OLED and drive
- 25 transistor.
3. A pixel driver circuit as claimed in claim 2, wherein the first selection line is a non-inverted selection line and the third selection line is an inverted selection line such that when the first selection line is HIGH the third
- 30 selection line is LOW.

4. A pixel driver circuit as claimed in 2 or 3, wherein the first and second selection lines are common.
5. A pixel driver circuit as claimed in any one of claims 1 to 4, wherein the first voltage supply line and another selection line are formed as a combined voltage supply and selection line.
10. 6. A pixel driver circuit as claimed in claim 1, wherein the first voltage supply line and another selection line are formed as a combined voltage supply and selection line and wherein the first and second selection lines are common.
15. 7. A pixel driver circuit as claimed in claim 5 or 6, wherein the another selection line is the first selection line of a neighbouring pixel circuit sharing a common data line.
8. A pixel driver circuit as claimed in any preceding claim, wherein the drive transistor is an n-type transistor.
20. 9. A pixel circuit as claimed in claim 8, wherein the drive transistor is an amorphous silicon transistor.
25. 10. A pixel circuit as claimed in any preceding claim, wherein the OLED has a current path such that an anode terminal of the OLED is connected to the drive transistor.
30. 11. A plurality of pixel driver circuits as claimed in any one of claims 5 to 10 and arranged in row and columns, each data line being shared by each pixel circuit in a column and each combined voltage supply line and all selection lines being shared by each pixel circuit in a row, wherein, for a particular column and during addressing the combined voltage supply and selection line of the n-1th pixel driver circuit acts as the first voltage

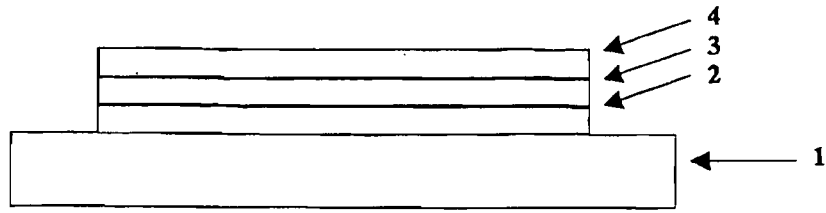
supply line to the nth pixel driver circuit and the combined voltage supply and selection line of the n+1th pixel driver circuit acts as a selection line to the nth pixel driver circuit.

- 5 12. An active matrix display device comprising an array of pixel driver circuits as claimed in any preceding claim, wherein the pixel driver circuits are arranged in row and columns to form the display and each data line is shared by each pixel circuit in a column and each selection line is shared by each pixel circuit in a row.
- 10 13. An active matrix display device as claimed in claim 12, wherein the second switch transistor is connected to a voltage sensing device for sensing a voltage drop across an OLED and for generating a sensed voltage drop signal to a controller for adjusting the drive signal in response to the sensed voltage drop signal.
- 15 14. An active matrix display device as claimed in claim 13, wherein the sensed voltage drop signal is provided to a lookup table for storing voltage data representing a relationship between voltage and drive signal for a characteristic OLED and the controller being programmed to adjust the drive signal in response to the relationship.
- 20 15. An active matrix display device as claimed in claim 13 or 14, wherein the voltage sensing device is for sensing the voltage drop of all the OLEDs of the display.
- 25 16. An active matrix display device as claimed in claim 13 or 14, wherein a plurality of voltage sensing devices are provided, each for sensing a voltage drop on a sub-set of the OLEDs of the display.

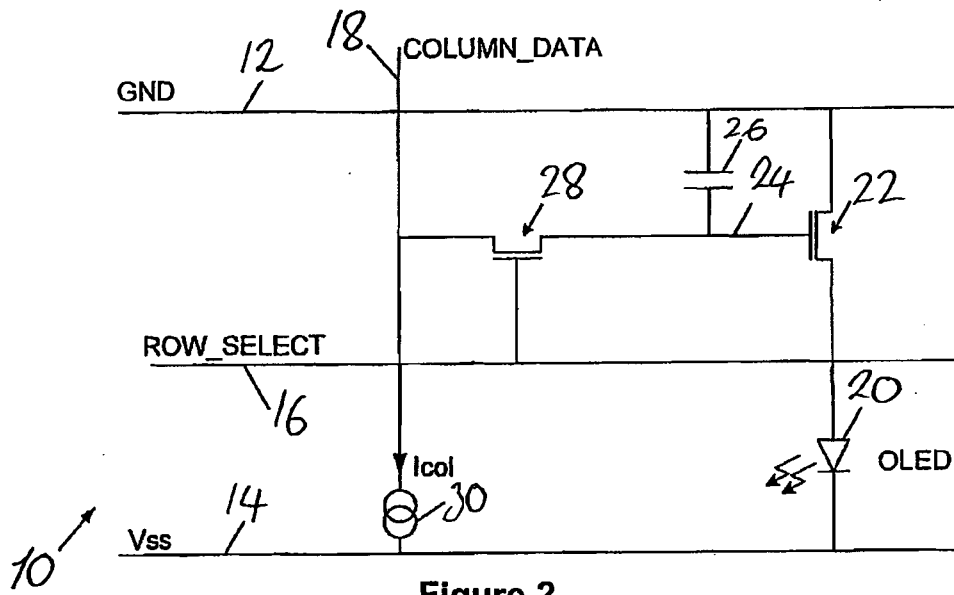
17. An active matrix display device as claimed in any one of claims 13 to 16, wherein the sensed voltage drop sensed by the voltage sensing device is a combination of the voltage drops across a plurality of the OLEDs.
- 5 18. An active matrix display device as claimed in any one of claims 13 to 17, further comprising a module for determining a transistor characteristic of a transistor of a pixel driver circuit from the sensed voltage drop signal.
19. An active matrix display device as claimed in claim 18, wherein the  
10 transistor characteristic is a threshold voltage shift of the drive transistor.
20. An active matrix display device as claimed in any one of claims 11 to 18, wherein the pixel driver circuits are current-programmed.
- 15 21. A pixel driver circuit for driving an organic light-emitting diode (OLED) comprising:  
a first selection line;  
a data line;  
a first voltage supply line; and  
20 a drive transistor having a current path connected to the first voltage supply line at one end and the OLED at the other end and a gate terminal connected to a storage element connected to the data line to memorise a drive signal for the drive transistor under the control of first and second switch transistors having gate connections  
25 to the first selection line;  
a third switch transistor having a gate connection to a second selection line, wherein the third switch transistor is located in the current path of the drive transistor in series between the OLED and drive transistor.
- 30 21. A pixel driver circuit as claimed in claim 20, wherein the first selection line is a non-inverted selection line and the second selection line is an

inverted selection line such that when the first selection line is HIGH the second selection line is LOW.

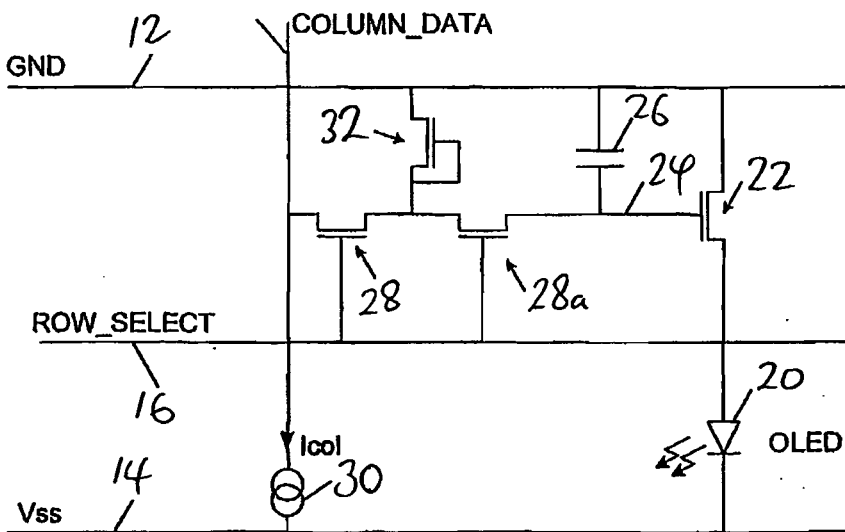
- 5 22. A pixel driver circuit as claimed in claim 20 or 21, wherein the first voltage supply line and another selection line are formed as a combined voltage supply and selection line.
23. A pixel driver circuit as claimed in claim 22, wherein the another selection line is the first selection line.
- 10 24. A pixel driver circuit substantially as hereinbefore described and/or with reference to Figures 5, 6 and 7 of the accompanying drawings.
- 15 25. An active matrix display device substantially as hereinbefore described and/or with reference to Figures 5, 6 and 7 of the accompanying drawings.



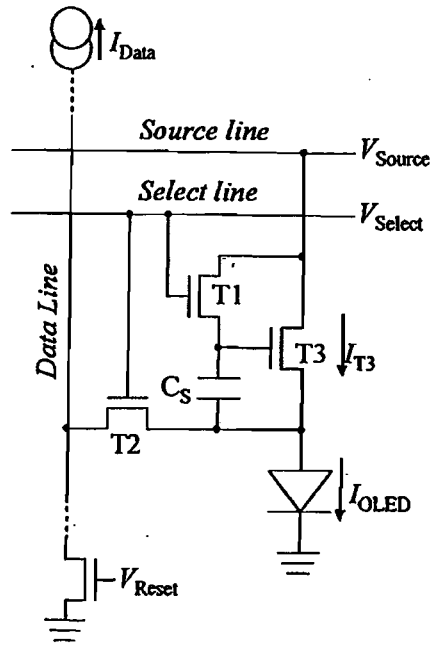
**Figure 1**



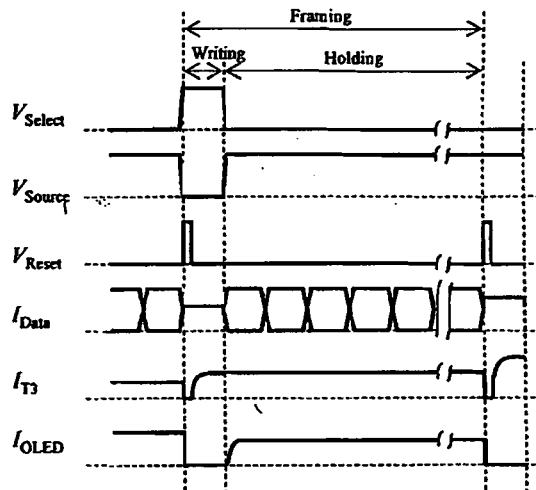
**Figure 2**



**Figure 3**



**Figure 4a**



**Figure 4b**

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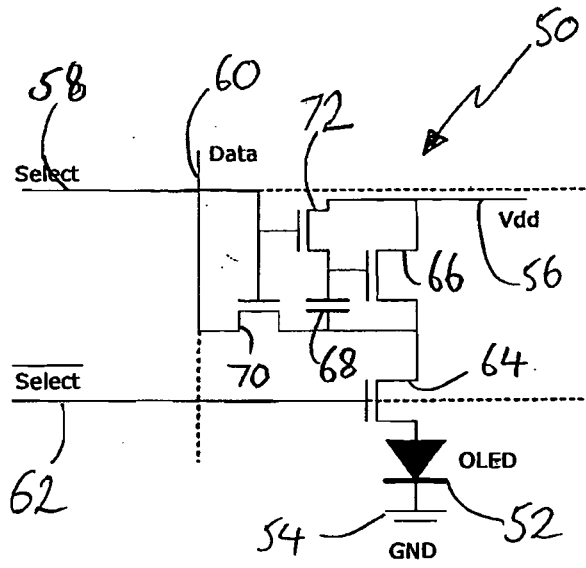


Figure 5

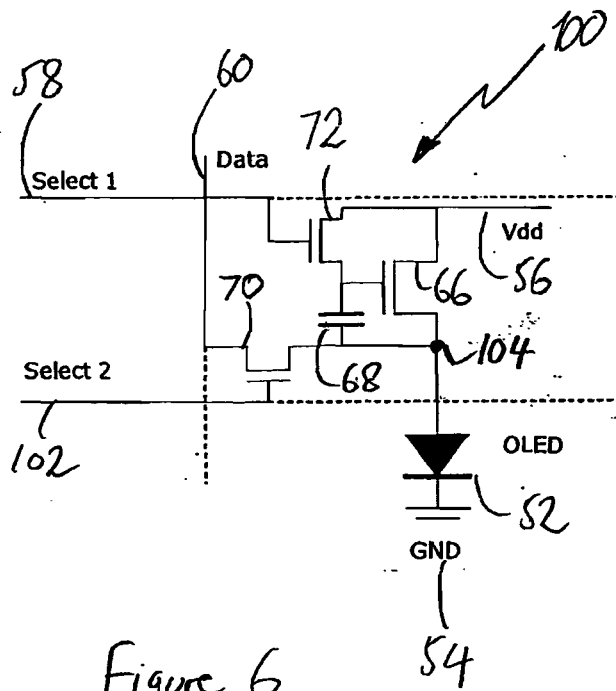


Figure 6

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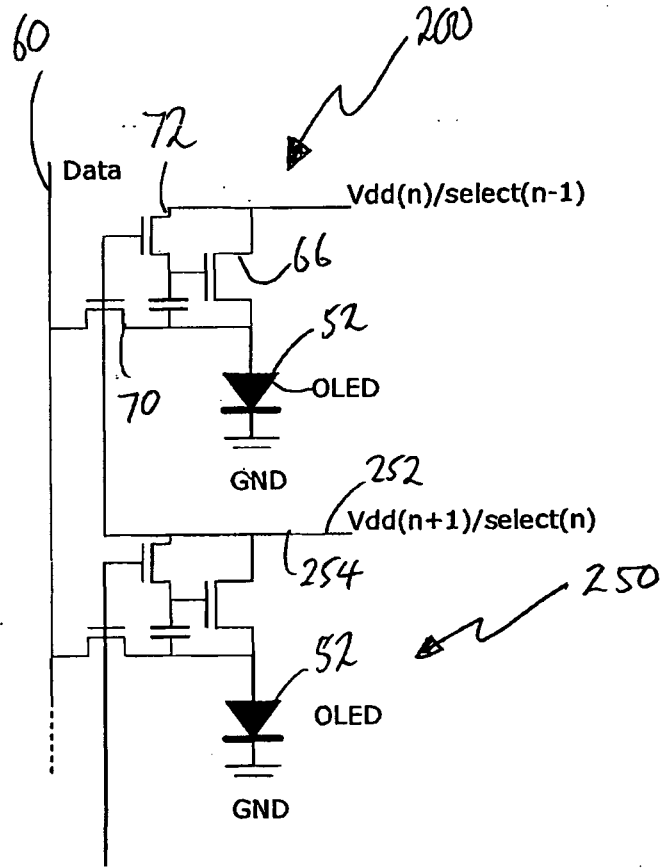


Figure 7

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/GB2008/003300

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. G09G3/32

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/088103 A1 (KAGEYAMA HIROSHI [JP] ET AL) 28 April 2005 (2005-04-28) paragraphs [0039] - [0043], [0054] figures 1,2,4	1,2, 8-10,12
X	US 6 229 506 B1 (DAWSON ROBIN MARK ADRIAN [US] ET AL) 8 May 2001 (2001-05-08)	1-4, 8-10,12, 20,21
Y	column 2, line 55 - column 4, line 34 figure 2	5-7,11, 13-19, 23-26
Y	US 2005/140304 A1 (CHANG HUNG J [TW] ET AL) 30 June 2005 (2005-06-30) paragraphs [0009], [0022] - [0026] figure 2	5-7,11, 23-26
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Further documents are listed in the continuation of Box C.

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## INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/040441 A1 (KIMURA HAJIME [JP]) 24 February 2005 (2005-02-24) paragraphs [0016], [0079], [0080] figure 3 -----	5-7, 11, 23-26
Y	US 2007/195020 A1 (NATHAN AROKIA [CA] ET AL) 23 August 2007 (2007-08-23) paragraphs [0071] - [0078] paragraphs [0115] - [0122] figures 7, 22 -----	13-19
Y	US 2005/110420 A1 (ARNOLD ANDREW D [US] ET AL) 26 May 2005 (2005-05-26) paragraphs [0022] - [0024] figure 1a -----	13-19
X	US 2004/246241 A1 (SATO KAZUHITO [JP] ET AL) 9 December 2004 (2004-12-09) -----	1, 8-10, 12
Y	paragraphs [0063], [0065], [0095] figure 6 -----	5-7, 11, 13-19, 23-26

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/GB2008/003300
---

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005088103	A1	28-04-2005	CN 1612192 A 04-05-2005
			JP 2005134435 A 26-05-2005
			KR 20050040679 A 03-05-2005
US 6229506	B1	08-05-2001	NONE
US 2005140304	A1	30-06-2005	TW 227651 B 01-02-2005
US 2005040441	A1	24-02-2005	NONE
US 2007195020	A1	23-08-2007	WO 2007090287 A1 16-08-2007
			EP 1987507 A1 05-11-2008
US 2005110420	A1	26-05-2005	CN 1886774 A 27-12-2006
			JP 2007514966 T 07-06-2007
			KR 20060134938 A 28-12-2006
			WO 2005055186 A1 16-06-2005
US 2004246241	A1	09-12-2004	AU 2003238700 A1 06-01-2004
			CA 2460747 A1 31-12-2003
			CN 1565013 A 12-01-2005
			CN 101071538 A 14-11-2007
			EP 1417670 A1 12-05-2004
			HK 1073379 A1 29-08-2008
			WO 2004001714 A1 31-12-2003
			JP 2004021219 A 22-01-2004
			MX PA04002755 A 29-06-2004
			NO 20041152 A 19-01-2005
			TW 250483 B 01-03-2006

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优先权	2007019511 2007-10-05 GB		
外部链接	<a href="#">Espacenet</a>		

#### 摘要(译)

提供像素驱动电路用于有机发光二极管 ( OLED ) 的有源矩阵驱动。该像素电路的特征在于包括驱动晶体管，该驱动晶体管具有连接到一端的第一电压供应线和另一端的OLED的电流路径，以及连接到连接在驱动晶体管的栅极和源极之间的存储元件的栅极端子。在第一开关晶体的控制下记忆驱动晶体管的驱动信号，该第一开关晶体管具有到第一选择线的栅极连接和连接在驱动晶体管的栅极和漏极之间的电流路径;第二开关晶体管，具有到第二选择线的栅极连接，其中第二开关晶体管具有在一端连接到数据线的电流路径和在驱动晶体管和OLED之间连接到另一端的节点。