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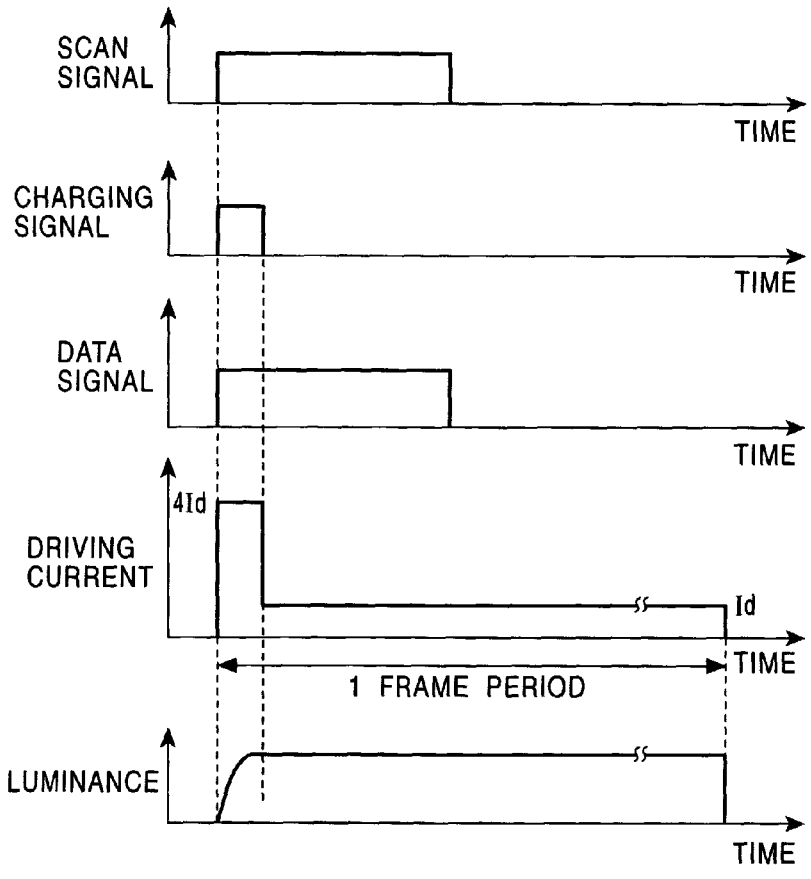
(54) Title: LIGHT EMITTING CIRCUIT FOR ORGANIC ELCTROLUMINESCENCE ELEMENT AND DISPLAY DEVICE



(57) Abstract: A light emitting circuit and a display device which supply a forward driving current to an organic electroluminescence element in response to generation of a light emit command to cause to light-emit the organic electroluminescence element, and supply a charging current to the organic electroluminescence element after the generation of the light emit command to charge the capacity component of the organic electroluminescence element.

WO 03/049074 A1

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DESCRIPTION

LIGHT EMITTING CIRCUIT FOR ORGANIC ELECTROLUMINESCENCE ELEMENT AND DISPLAY DEVICE

Technical Field

The present invention relates to a light emitting circuit for an organic electroluminescence element and a display device.

Background Art

An electroluminescence element (hereinafter referred to as 'EL element'), which is a capacitive light emitting element, can be electrically expressed as an equivalent circuit, as shown in Fig. 1. As can be understood from Fig. 1, an element can be substituted by a constitution of a capacity component C and a component E having a diode characteristic coupled in parallel to the capacity component. Therefore, an EL element can be considered to be a capacitive light emitting element. When a light emitting driving DC voltage is applied between the electrodes of the EL element, electric charge is accumulated in the capacity component C. When the voltage across the electrodes exceeds the barrier voltage or the light emission threshold voltage peculiar to the EL element, electric current starts flowing from the electrode (the anode side of the diode component E) to an organic functional layer forming a light emitting layer. As a result, the EL element emits light at light intensity proportional to the current.

The voltage V-current I-luminance L characteristic of the EL element is, as shown in Fig. 2, similar to the characteristic of a diode in that the current I is very small

at a voltage lower than the light emission threshold voltage Vth and increases at a voltage higher than the light emission threshold voltage Vth. Further, the current I and the luminance L are nearly proportional to each other. The EL element shows light emitting luminance proportional to the current I which flows in accordance with a driving voltage V when the driving voltage applied to the EL element exceeds the light emission threshold voltage Vth, and shows no light emitting luminance when the driving voltage V applied to the EL element is equal to or lower than the light emission threshold voltage Vth.

A display panel on which a plurality of EL elements are mounted in a matrix shape is already known. A display device that actively drives a display panel with EL elements is mounted with light emitting circuits configured as illustrated in Fig. 3 for respective pixels.

As shown in Fig. 3, the light emitting circuit for a single pixel includes two FETs (Field Effect Transistor) 1 and 2 and a capacitor 3 so as to drive an EL element 5. The gate G of the FET 1 is connected to a scan line Ai supplied with a scan signal, and the source S of the FET 1 is connected to a data line Bj supplied with a data signal. The Drain D of the FET 1 is connected to the gate G of the FET 2 and one terminal of the capacitor 3. The source S of the FET 2 is connected to a common power supply line 6 as well as the other terminal of the capacitor 3. The drain D of the FET 2 is connected to the anode of the EL element 5. The cathode of the EL element 5 is

grounded. The earth, to which the power supply line 6 and the cathode of the EL element 5 are connected, is connected to a power source (not shown).

Although the El element 5 is shown in Fig. 3 by a symbol for a diode, it can more exactly be shown in an equivalent circuit as shown in Fig. 1. The same thing can be said for a later stated EL element 25.

With regard to the operation of the light emitting circuit, first, a scan signal is supplied to the gate G of the FET 1 through the scan line Ai, and then, the FET 1 turns on to pass a current from the source S to the drain D. The current is flowed in accordance with the voltage of a data signal supplied to the source S. The capacitor 3 is charged during the period of the ON-state of the FET 1, and the charged voltage is supplied to the gate G of the FET 2 to turn the FET 2 into the ON-state (active or saturation state). In the ON-state of the FET 2, a driving current flows from the power supply line 6 through the source S and the drain D of the FET 2 and to the EL element 5 to make the EL element 5 emit light. When the supply of the scan signal to the gate G of the FET 1 disappears, the FET 1 turns into an OPEN-state. Then, the voltage of the gate G of the FET 2 is maintained by the accumulated charge in the capacitor 3, whereby the driving current is maintained until a next scanning and the light emission of the EL element 5 is maintained as well.

The light emitting luminance of the EL element 5 is controlled to obtain a display gradation in accordance with

image data. Here, either a driving current modulation system, which controls luminance by the level of the driving current for each frame, or a frame modulation system, which controls the driving period in one frame with a constant current driving level, can be applied for luminance control. As shown in Fig. 4, the driving current modulation system uses the FET 1 in an active state in accordance with image data to vary the driving current, whereby luminance is varied for each frame. On the other hand, the frame modulation system, as shown in Fig. 5, divides one frame into a plurality of sub frames of SF1, SF2, SF3,…. and uses the FET 1 in a saturation state only for the sub frame periods selected in accordance with image data to supply the driving current with a constant level, whereby light is emitted or not in the unit of sub frame.

However, since an EL element has a capacity component as stated above, when the flow of a driving current into the EL element is started, the forward voltage of the EL element gradually increases by charge accumulated in its capacity component. It may take time for the forward voltage to exceed the light emission threshold voltage. Particularly in gradation driving of a driving current modulation system, the driving current is controlled in accordance with the display gradation of a pixel. If the driving current level is low as shown in Fig. 6A, the forward voltage of the EL element gradually increases to exceed the light emission threshold voltage Vth. Accordingly, as shown in Fig. 6B, the EL element emits light only for the last short period of one frame. The

light emitting luminance gradually increases and is not constant, and thus it is not allowed to obtain desired luminance.

In addition, even when flowing the driving current with a constant level at the start of supplying the driving current to the EL element, the time required for exceeding the light emission threshold voltage varies in accordance with the quantity of accumulated charge left in the capacity component of the EL element then. Particularly in a frame modulation system, if a large quantity of accumulated charge is left in the capacity component of the EL element, as shown in Fig. 7A, at the time of starting the supply of the driving current, the forward voltage of the EL element is present with a level in accordance with the quantity of accumulated charge, and the voltage starts increasing from this voltage level. Accordingly, it takes a short time for the voltage to exceed the light emission threshold voltage Vth, and the EL element, as shown in Fig. 7B, starts emitting light in a comparatively short time after the start of the supply of the driving current. On the other hand, if a quantity of accumulated charge is hardly left in the capacity component in the EL element, as shown in Fig. 8A, at the time of starting the supply of the driving current, the forward voltage level of the EL element in accordance with the quantity of accumulated charge is nearly zero volts, and the voltage starts increasing from this low voltage level of nearly zero volts. Accordingly, it takes a long time for the voltage to exceed

the light emission threshold voltage Vth. The EL element, as shown in Fig. 8B, starts emitting light at a late time after the start of the supply of the driving current. As a result, even when supplying the driving current to the EL element with the same level for the same period of time, the light emitting luminance varies in accordance with the quantity of accumulated charge left in the capacity component of the EL element at the start of supplying the driving current to the EL element. Thus it is not allowed to obtain desired luminance.

Disclosure of Invention

An object of the present invention is to provide an active driving light emitting circuit, which can provide desired luminance whatever the quantity of accumulated charge of an EL element at the start of supply of a driving current to the EL element is, and also to provide a display device using the circuit.

A light emitting circuit according to the present invention makes an organic electroluminescence element emit light by supplying, in response to generation of a light emit command, a forward driving current to the organic electroluminescence element, the light emitting circuit comprising charging current supply means for supplying a charging current to the organic electroluminescence element so as to charge a capacity component of the organic electroluminescence element after the generation of the light emit command.

A display device according to the present invention comprises: a display panel having a plurality of drive lines, a plurality of scan lines intersecting with the plurality of drive lines, and a plurality of sets of an organic electroluminescence element and a light emitting circuit of an active driving method, the plurality of sets being arranged at a plurality of intersecting positions by the drive lines and the scan lines, respectively; and control means for supplying a scan signal to one scan line of the plurality of scan lines in sequence at a specified timing and supplying a data signal to a data line of the plurality of data lines which is associated to at least an organic electroluminescence element to be driven to emit light on the one scan line, wherein the light emitting circuit includes: a switching element for turning on in response to the scan signal to allow the data signal to pass therethrough; a capacitor which is charged by the data signal supplied through the switching element; an EL driving element for activating in accordance with a charged voltage of the capacitor to supply a driving current to the organic electroluminescence element in the same set; and charging current supply means for supplying a charging current to the organic electroluminescence element in the same set immediately after the supply of the scan signal to charge a capacity component of the organic electroluminescence element in the same set.

Brief Description of Drawings

Fig. 1 illustrates an equivalent circuit of an EL

element;

Fig. 2 schematically illustrates the driving voltage-current-light emitting luminance characteristic of the EL element;

Fig. 3 is a diagram illustrating a configuration of a conventional light emitting circuit;

Fig. 4 is the light emitting luminance characteristic diagram of an EL element by a light emitting circuit to which gradation driving of a driving current modulation system is applied;

Fig. 5 is the light emitting luminance characteristic diagram of an EL element by a light emitting circuit to which gradation driving of a frame modulation system is applied;

Fig. 6A and Fig. 6B respectively illustrate the forward voltage and luminance of an EL element in the case of gradation driving of a driving current modulation system;

Fig. 7A and Fig. 7B respectively illustrate the forward voltage and luminance of an EL element in the case of gradation driving of a frame modulation system;

Fig. 8A and Fig. 8B respectively illustrate the forward voltage and luminance of an EL element for gradation driving of a frame modulation system;

Fig. 9 is a block diagram illustrating the configuration of a display device according to the present invention;

Fig. 10 is a circuit diagram illustrating a configuration of a light emitting circuit in the device in Fig. 9;

Figs. 11A-11E are waveform diagrams illustrating the

operation of the light emitting circuit in the Fig. 10;

Fig. 12 is a circuit diagram illustrating another configuration of the light emitting circuit in the device in Fig. 9;

Fig. 13 is a circuit diagram illustrating still another configuration of the light emitting circuit in the device in Fig. 9;

Fig. 14 illustrates a voltage superimposing circuit for supplying a data signal to the light emitting circuit in Fig. 13;

Figs. 15A-15D are waveform diagrams illustrating the operation of the light emitting circuit in Fig. 13;

Fig. 16 illustrates another voltage superimposing circuit for supplying a data signal to the light emitting circuit in Fig. 13;

Fig. 17 is a circuit diagram illustrating another configuration of the light emitting circuit in the device in Fig. 9;

Figs. 18A-18E are waveform diagrams illustrating the operation of the light emitting circuit in Fig. 16; and

Fig. 19 is a circuit diagram illustrating another configuration of the light emitting circuit in the device in Fig. 9.

Detailed Description of the Invention

Preferred embodiments of the invention will be described as follows, with reference to the drawings.

Fig. 9 illustrates a display device using a matrix

display panel according to the present invention. The display device includes a display panel 11, a scan line driving circuit 12, a data line driving circuit 13, a charging control line driving circuit 14, and a controller 15.

The display panel 11 is an active matrix type constituted of m x n pixels, and has EL light emitting circuits $11_{1,1}$-$11_{m,n}$ for respective pixels as shown in Fig. 9. The EL light emitting circuits $11_{1,1}$-$11_{m,n}$ all have the same configuration, and are connected to the scan line driving circuit 12 through scan lines A1-An, to the data line driving circuit 13 through data lines B1-Bm, and to the charging control line driving circuit 14 through charging control lines C1-Cn. The controller 15 generates a scan control signal, a data control signal, and a charging control signal in accordance with input image data. The scan control signal indicates a scan line to be selected and is supplied to the scan line driving circuit 12. The data control signal indicate the data lines corresponding to EL elements to be driven to emit light and is supplied to the data line driving circuit 13. The charging control signal indicates the charging control lines corresponding to the EL elements to be driven to emit light and is supplied to the charging control line driving circuit 14.

The scan line driving circuit 12, the data line driving circuit 13, and the charging control line driving circuit 14, which are not shown specifically, are respectively constituted of a power source and a switch circuit. The scan line driving

circuit 12 selects from the scan lines A1-An in sequence for each frame in accordance with a scanning control signal, and supply a scan signal to a selected scan line. The data line driving circuit 13 selects from the data lines B1-Bm in accordance with a light emitting control signal, and supplies a data signal to a selected data line. The charging control driving circuit 14 selects from the charging control lines C1-Cn in accordance with a charging control signal, and supplies a charging signal to a charging control line.

As described above, since the light emitting circuits $11_{1,1}$-$11_{m,n}$ all have the same configuration, the configuration of the light emitting circuit $11_{1,1}$ will be explained as follows.

The light emitting circuit $11_{1,1}$, as shown in Fig. 10, includes three FETs 21-23 and a capacitor 24 to drive an EL element 25. The gate G of the FET 21 is connected to a scan line A1 to which a scan signal is supplied, and the source S of the FET 21 is connected to a data line B1 to which a data signal is supplied. The drain D of the FET 21 is connected to the gate G of the FET 22 and one terminal of the capacitor 24. The source S of the FET 22 is connected to a common power supply line 26 as well as the other terminal of the capacitor 24. The drain D of the FET 22 is connected to the anode of the EL element 5 as well as the drain D of the FET 23, and the cathode of the EL element 25 is grounded. The source S of the FET 23 is connected to a power supply line 27, and the gate G thereof is connected to a charging control line C1. A specified voltage V_A is supplied to the power supply line 26,

and a specified voltage V_s is supplied to the power supply line 27.

With regard to the operation of the light emitting circuit $11_{1,1}$, first, a scan signal is supplied to the gate G of the FET 21 through the scan line A1, and at the same time, a charging signal is supplied to the gate G of the FET 23 through the charging control line C1. The scan signal is a pulse voltage having a waveform as shown in Fig. 11B. The charging signal is a pulse voltage having a waveform as shown in Fig. 11A and has a shorter pulse width than that of a scan signal.

The FET 21 is turned on by the supply of the scan signal, and flows a current in accordance with the voltage of the data signal supplied to the source S through the data line B1 from the source S to the drain D. The capacitor 24 is charged, and its voltage is supplied to the gate G of the FET 22 to turn the FET 22 on (saturation or active state). On the other hand, the FET 23 turns on by the supply of the charging signal. Therefore, the FET 22 and the FET 23 almost simultaneously turn on. Consequently, the FET 22 supplies the EL element 25, from the specified Voltage V_A, with a driving current in accordance with the data signal supplied to the gate G, and the specified voltage V_s is applied to the EL element 25 through the source S - drain D of the FET 23. If the EL element 25 has a small quantity of accumulated charge then, a driving current by the specified voltage V_s flows to the EL element 25 through the source S - drain D of the FET

23. This driving current flows in order to charge the capacity component of the EL element 25 rapidly. That is, a driving current flows into the EL element 25 as shown in Fig. 11C. As the capacity component of the EL element 25 is charged, the driving current decreases. When the charging signal disappears, the driving current in accordance with the data signal supplied to the gate G of the FET 22 flows into the EL element 25. This driving current by the specified voltage V_A flows with a constant level.

By supplying the driving current to the EL element 25 in this way, a voltage is applied to the EL element 25, for example as shown in Fig. 11D, with a constant level, and the light emitting luminance level of the EL element 25 is almost constant, as shown in Fig. 11E, from the start of supplying the driving current to the EL element 25.

Fig. 12 shows another embodiment of the configuration of the light emitting circuit $11_{1,1}$. The light emitting circuit $11_{1,1}$ in Fig. 12 includes three FETs 21-23, a capacitor 24, and an EL element 25 as in the circuit of Fig. 10. The light emitting circuit $11_{1,1}$ in Fig. 12 is different from the circuit in Fig. 10 in that, instead of a charging signal, a scan signal is supplied to the gate G of the FET 23 in addition to the gate G of the FET 21 in the circuit $11_{1,1}$ in Fig. 12. Accordingly, a driving current by the specified voltage V_S flows into the EL element 25 through the source S - drain D of the FET 23 during the full period when the scan signal is being supplied, whereby the capacity component of the EL

element 25 is rapidly charged. In a display device using the light emitting circuit $11_{1,1}$ in Fig. 12, neither a charging control line driving circuit 14 nor charging control lines C1-Cn are needed.

FIG. 13 shows still another embodiment of the configuration of the light emitting circuit $11_{1,1}$. The circuit $11_{1,1}$ in Fig. 13 is not provided with the FET 23 that is included in the circuit in Fig. 10, but is provided with the two FETs 21 and 22, capacitor 24, and EL element 25 only. In other words, the light emitting circuit $11_{1,1}$ in Fig. 13 has the same configuration as one shown in Fig. 3. Also, in a display device using the light emitting circuit $11_{1,1}$ in Fig. 13, neither a charging control line driving circuit 14 nor charging control lines C1-Cn are needed.

In the data line driving circuit 13 or the controller 15 of the display device, as shown in Fig. 14, a voltage for charging is added to a data signal by a voltage adding circuit 30. This addition is applied to each data signal line. To each of the light emitting circuits $11_{1,1}$-$11_{m,n}$, the data signal having a waveform as shown in Fig. 15A is supplied from the data line driving circuit 13. The signal level is higher by the voltage for charging during a specified period from the start of the supply of the data signal, and becomes a normal level after the specified period. The voltage for charging is set in accordance with the gradation of the pixel corresponding to the image data for each of the light emitting circuits.

Also, as shown in Fig. 16, the voltage for charging and the data signal may be switched by a changeover switch 40 in accordance with the charging signal.

With regard to the operation of the light emitting circuit $11_{1,1}$ in Fig. 13, first, the scan signal is supplied to the gate G of the FET 21 through the scan line A1 as shown in Fig. 15B, and then, the FET 21 turns on in accordance with the scan signal to flow a current from the source S to the drain D in accordance with the voltage of the data signal supplied to the source S through the data line B1. The capacitor 24 is charged, and its voltage is supplied to the gate G of the FET 22 to make it an ON-state (saturation or active state). Due to the ON-state of the FET 22, the driving current in accordance with the data signal supplied to the gate G of the FET 22 flows into the EL element 25. Since the signal level is higher by the voltage for charging during a specified period from the start of supply of the data signal, the level of the driving current increases, as shown in Fig. 15C, for a specified period, whereby the capacity component of the EL element 25 is rapidly charged. After the specified period, the level of the data signal returns to a normal signal level. Consequently, the resistance between the source S - drain D of the FET 22 increases, whereby the driving current decreases. Therefore, the light emitting luminance of the EL element 25 increases rapidly from the start of supply of the driving current to the EL element 25 as shown in Fig. 15D, and then maintains almost a constant level.

FIG. 17 shows still another embodiment of the configuration of the light emitting circuit $11_{1,1}$. The light emitting circuit $11_{1,1}$ in Fig. 17 is not provided with the FET 23 that is provided to the circuit in Fig. 10, but provided with the two FETs 21 and 22, capacitor 24, and EL element 25, and still further provided with FETs 31 and 32. The source S of the FET 31 is connected to the power supply line 26, and its drain D is connected to the source S of the FET 32. The drain D of the FET 32 is connected to the anode of the EL element 25 as well as the drain D of the FET 22. The gate G of the FET 31 is connected to the charging control line C1, and the gate G of the FET 32 is connected to the connection line of the gate G of the FET 22. When the FET 32 turns into an ON-state, FET 22 also turns into an ON-state. In this case, the circuit is designed such that the current flowing through the FET 32 is 3 times as high as the current flowing through the FET 22 while both FETs are in the On-state.

With regard to the operation of the light emitting circuit $11_{1,1}$ in Fig. 17, when a scan signal is supplied to the gate G of the FET 21 through the scan line A1, a charging signal is simultaneously supplied to the gate G of the FET 32 through the charging control line C1. The scan signal is a pulse voltage having a waveform as shown in Fig. 18A. The charging signal is a pulse voltage having a waveform as shown in Fig. 18B, and for example, has a pulse width shorter than the pulse width of the scan signal.

The FET 21 turns on in response to the supply of the scan

signal, and flows a current from the source S to the drain D in accordance with the voltage of the data signal (Fig. 18C) that is supplied to the source S through the data line B1. The capacitor 24 is charged, and its voltage is supplied to the respective gates G of the FETs 22 and 32 to turn the FETs 22 and 32 on. On the other hand, the FET 31 turns on by the supply of the charging signal. Accordingly, the FETs 22, 31, and 32 turn on almost at the same time, and then, the driving current through the source S - drain D of the FET 22 and the driving current through the source S - drain D of the FET 31 and through the source S - drain D of the FET 32 flow into the EL element 25.

As described above, when the FET 32 is in the ON-state, a current flowing into the FET 32 is 3 times as high as the current flowing into the FET 22 which turns on simultaneously. Accordingly, high current, as shown in Fig. 18D, flows into the EL element 25 for the period when the charging signal is supplied. If Id is defined as the driving current through the source S - drain D of the FET22, then the driving current through the source S - drain D of the FET 31 and through the source S - drain D of the FET 32 is added to Id, whereby 4Id flows into the EL element 25. As a result, the capacity component of the EL element 25 is rapidly charged by the driving current of 4Id during the period when this charging signal is supplied.

When the charging signal disappears, the FET 31 turns off, and the supply of the driving current to the EL element

25 through the source S - drain D of the FET 31 and through the source S - drain D of the FET 32 is stopped. As a result, only the driving current of Id by the FET 22 is supplied to the EL element 25. Accordingly, the light emitting luminance of the EL element 25, as shown in Fig. 18E, rapidly increases from the start of the supply of the driving current to the EL element 25, and then maintains almost a constant luminance level.

FIG. 19 illustrates yet another embodiment of the configuration of the light emitting circuit $11_{1,1}$. The light emitting circuit $11_{1,1}$ in Fig. 19 is a variation of the circuit configuration in Fig. 17, wherein a voltage signal V_H in accordance with the display gradation of each pixel is supplied to the gate G of the FET 32 from the controller 15. The rest of the configuration is the same as that of the circuit in Fig. 17, and the operation of the circuit $11_{1,1}$ in Fig. 19 is the same as that of the circuit in Fig. 17.

In the embodiments described above, light emitting circuits for a single pixel are explained. In the case of color display, three light emitting circuits of RGB form one pixel.

As stated above, according to the present invention, desired luminance can be obtained whatever the quantity of accumulated charge of the EL element is at the start of the supply of the driving current to the EL element.

CLAIMS

1. A light emitting circuit for making an organic electroluminescence element emit light by supplying, in response to generation of a light emit command, a forward driving current to said organic electroluminescence element, the light emitting circuit comprising:

charging current supply means for supplying a charging current to said organic electroluminescence element so as to charge a capacity component of said organic electroluminescence element after the generation of said light emit command.

2. A light emitting circuit according to claim 1, wherein said charging current supply means is voltage applying means for applying a specified voltage to the organic electroluminescence element in a forward direction during a specified period of time after the generation of said light emit command.

3. A light emitting circuit according to claim 2, wherein said specified voltage is set in accordance with light emitting luminance to be obtained by said organic electroluminescence element.

4. A light emitting circuit according to claim 2, wherein said specified voltage is set to a light emission threshold voltage of said organic electroluminescence element.

5. A light emitting circuit according to claim 1, wherein said charging current supply means causes to increase said driving current only during a specified period after the

generation of said light emit command.

6. A light emitting circuit according to claim 5, wherein an amount of said driving current to be increased is set in accordance with light emitting luminance to be obtained by said organic electroluminescence element.

7. A display device comprising:

a display panel having a plurality of drive lines, a plurality of scan lines intersecting with said plurality of drive lines, and a plurality of sets of an organic electroluminescence element and a light emitting circuit of an active driving method, said plurality of sets being arranged at a plurality of intersecting positions by said drive lines and said scan lines, respectively; and

control means for supplying a scan signal to one scan line of said plurality of scan lines in sequence at a specified timing and supplying a data signal to a data line of said plurality of data lines which is associated to at least an organic electroluminescence element to be driven to emit light on said one scan line, wherein

said light emitting circuit includes: a switching element for turning on in response to said scan signal to allow said data signal to pass therethrough; a capacitor which is charged by said data signal supplied through said switching element; an EL driving element for activating in accordance with a charged voltage of said capacitor to supply a driving current to said organic electroluminescence element in the same set; and charging current supply means for supplying a charging

current to said organic electroluminescence element in the same set immediately after the supply of said scan signal to charge a capacity component of said organic electroluminescence element in the same set.

8. A display device according to claim 7, wherein said charging current supply means is means for applying a specified voltage to said organic electroluminescence element during a period shorter than a time width of said scan signal immediately after the supply of said scan signal.

9. A display device according to claim 7, wherein said charging current supply means is means for applying a specified voltage to said organic electroluminescence element during a period of a time width of said scan signal immediately after the supply of said scan signal.

10. A display device according to claim 7, wherein said charging current supply means is current increasing means for increasing said driving current during a period shorter than a time width of said scan signal immediately after the supply of said scan signal.

11. A display device according to claim 7, wherein said charging current supply means is current increasing means for increasing said driving current during a period of a time width of said scan signal immediately after the supply of said scan signal.

12. A display device according to claim 7, wherein said current increasing means is a switching element connected with said EL driving element in parallel.

13. A display device according to claim 7, wherein an amount of current increased by said current increasing means varies in accordance with a display gradation.

14. A display device according to claim 7, wherein said charging current supply means is voltage adding means for increasing a voltage level of said data signal during a period shorter than a time width of said scan signal immediately after the supply of said scan signal.

15. A display device according to claim 7, wherein said charging current supply means supplies said data line with a voltage for charging during a period shorter than a time width of said scan signal immediately after the supply of said scan signal.

FIG. 1

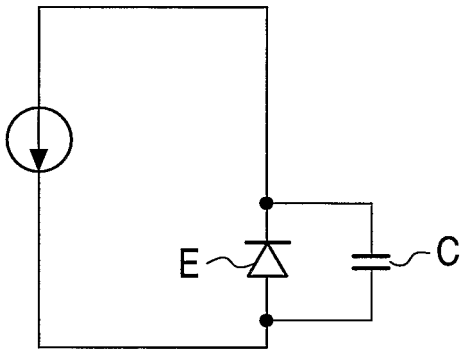


FIG. 2

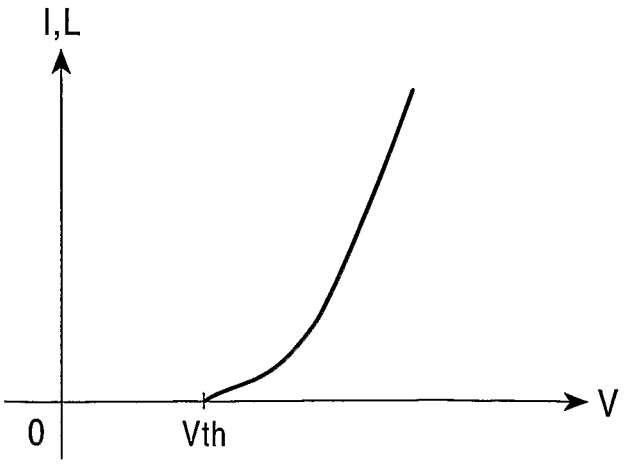


FIG. 3

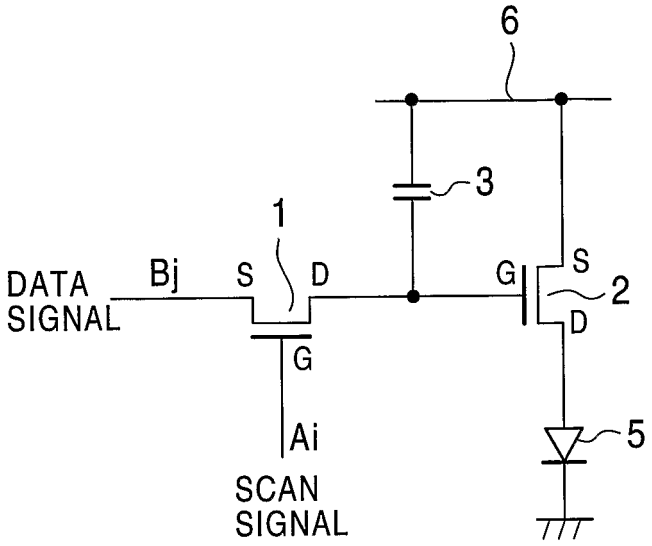


FIG. 4

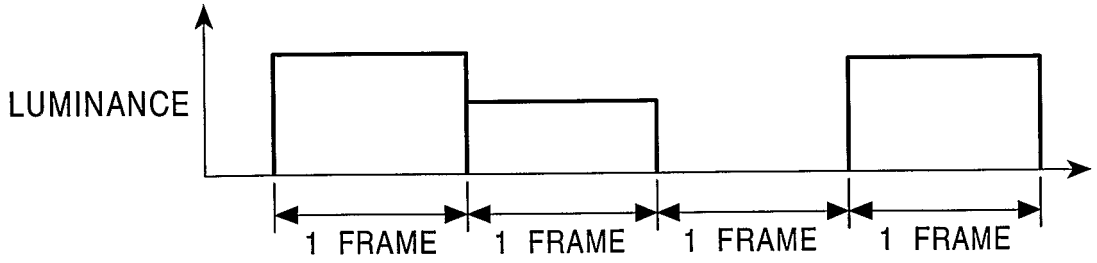


FIG. 5

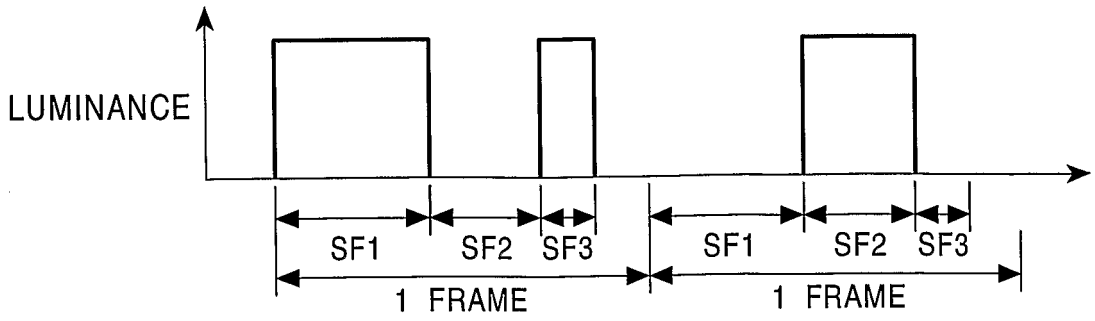


FIG. 6A

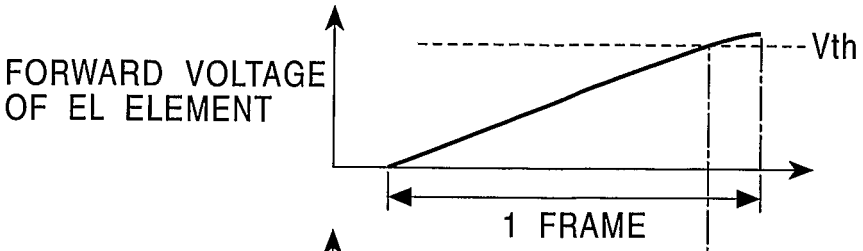


FIG. 6B

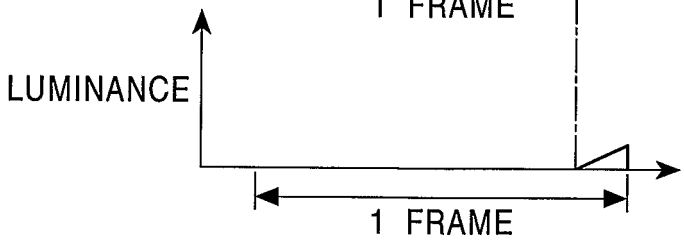


FIG. 7A

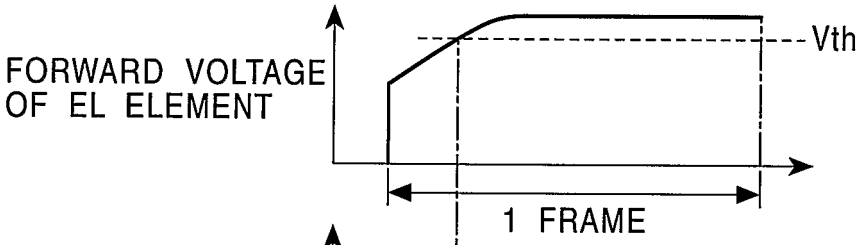


FIG. 7B

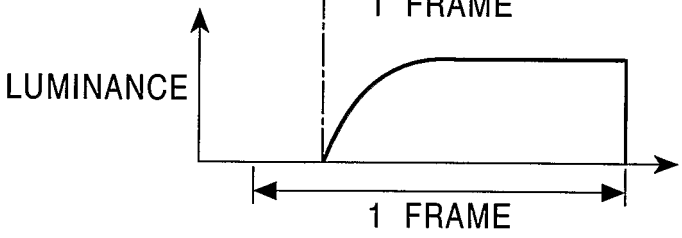


FIG. 8A

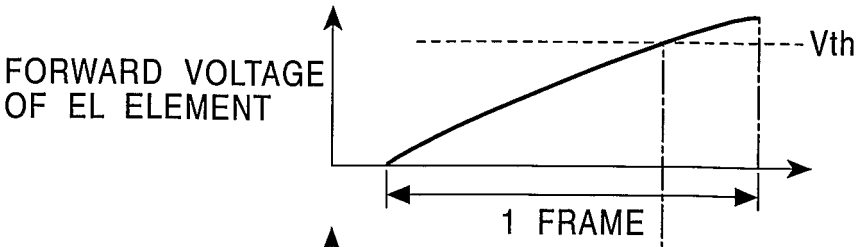


FIG. 8B

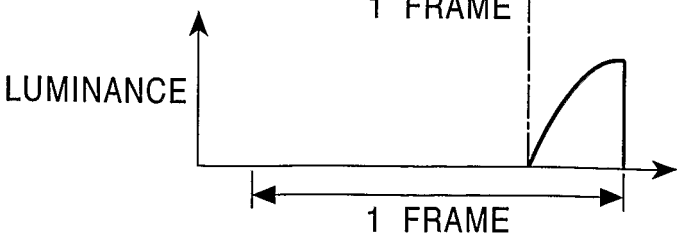


FIG. 9

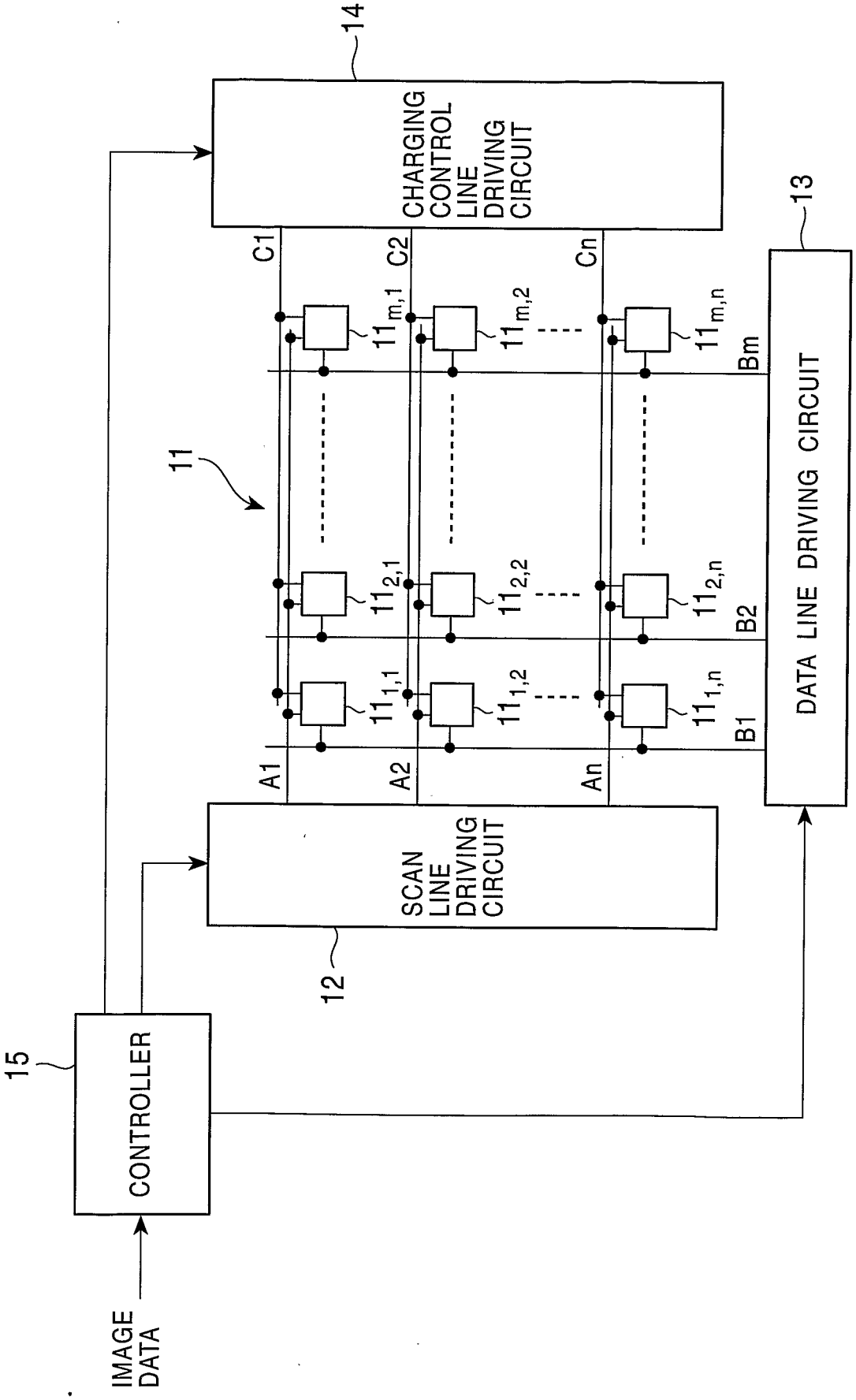

14
CHARGING CONTROL LINE DRIVING CIRCUIT
C1
C2
Cn
13
DATA LINE DRIVING CIRCUIT
Bm
B2
B1
11
$11_{m,1}$
$11_{m,2}$
$11_{m,n}$
$11_{2,1}$
$11_{2,2}$
$11_{2,n}$
$11_{1,1}$
$11_{1,2}$
$11_{1,n}$
A1
A2
An
12
SCAN LINE DRIVING CIRCUIT
15
CONTROLLER
IMAGE DATA

FIG. 10

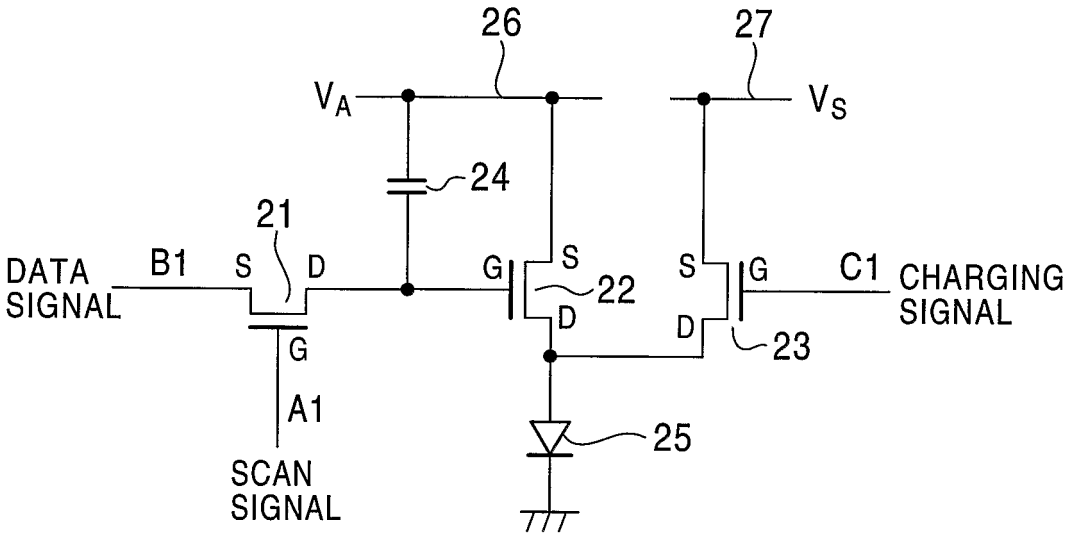

26
27
V_A
V_S
24
21
DATA SIGNAL
B1
S
D
G
S
22
D
S
G
C1
CHARGING SIGNAL
D
23
G
A1
SCAN SIGNAL
25

FIG. 11A

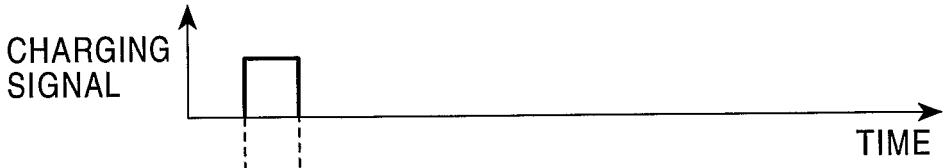


FIG. 11B

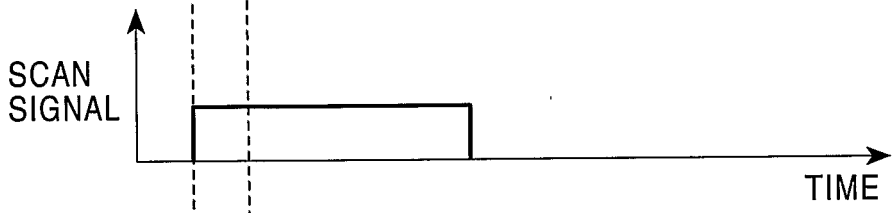


FIG. 11C

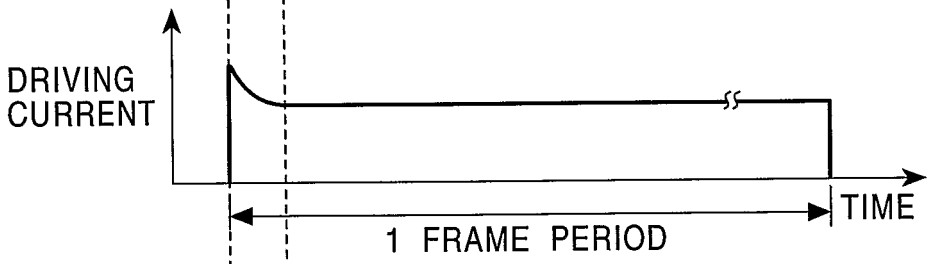


FIG. 11D

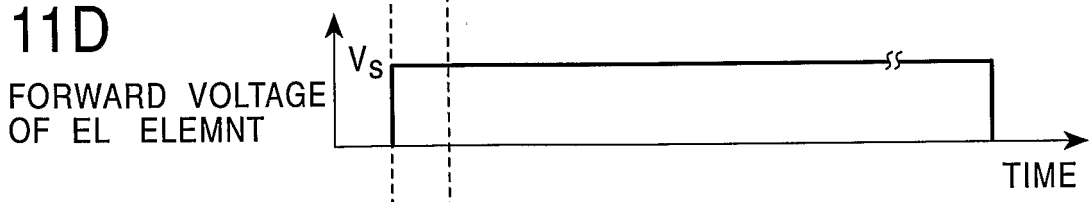


FIG. 11E

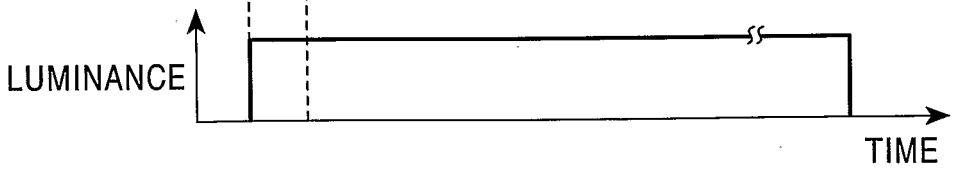


FIG. 12

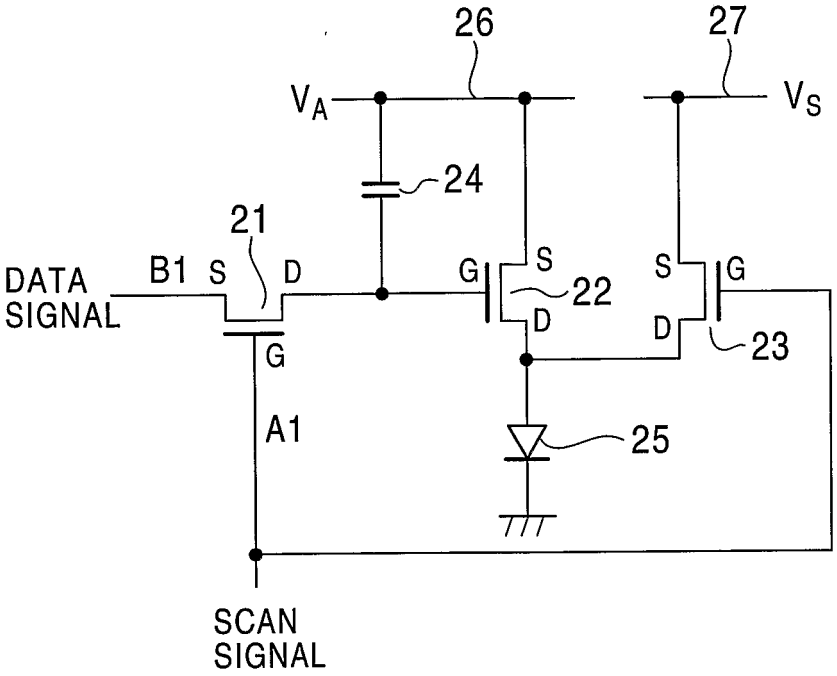
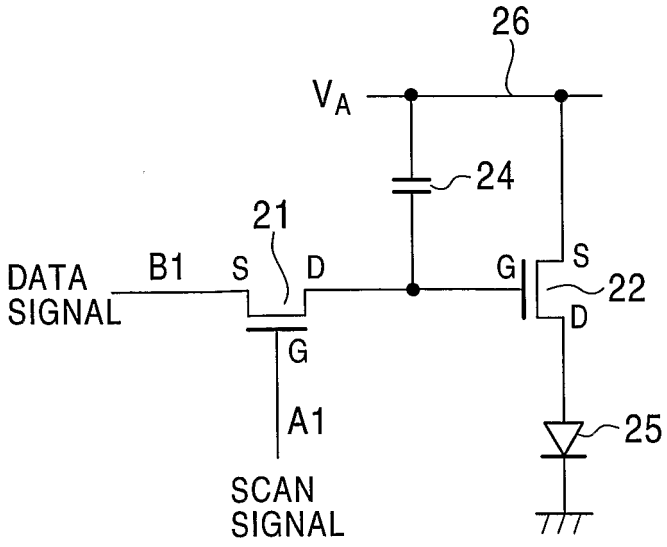

26
27
V_A
V_S
24
21
DATA SIGNAL
B1
S
D
G
S
22
D
S
G
D
23
G
A1
25
SCAN SIGNAL

FIG. 13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V_A
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DATA SIGNAL
B1
S
D
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S
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D
G
A1
25
SCAN SIGNAL

FIG. 14

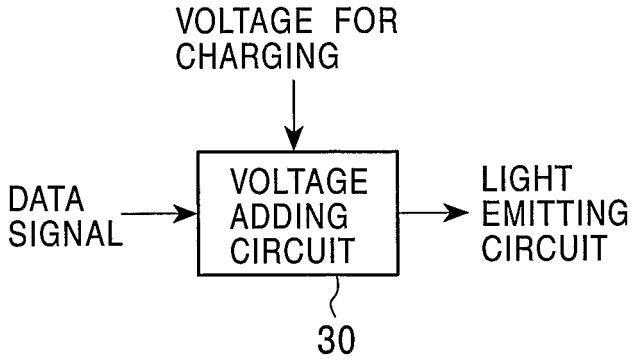


FIG. 15A

FIG. 15B

FIG. 15C

FIG. 15D

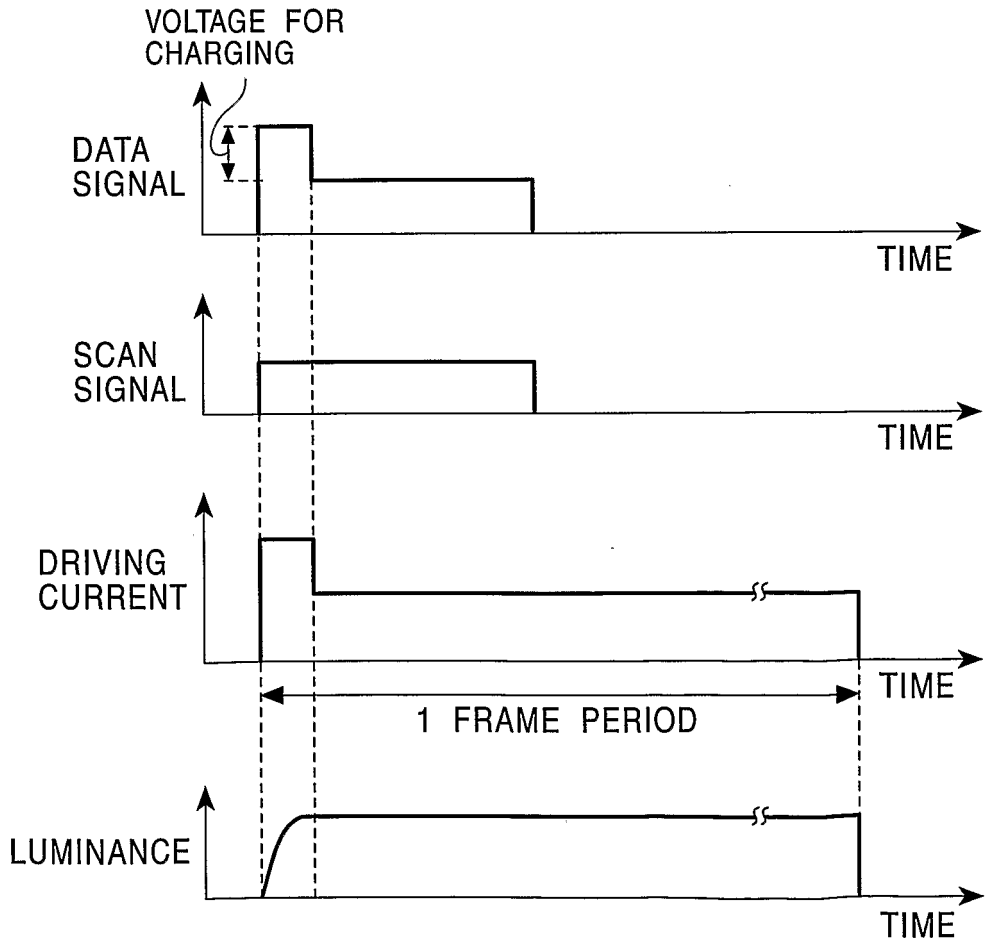


FIG. 16

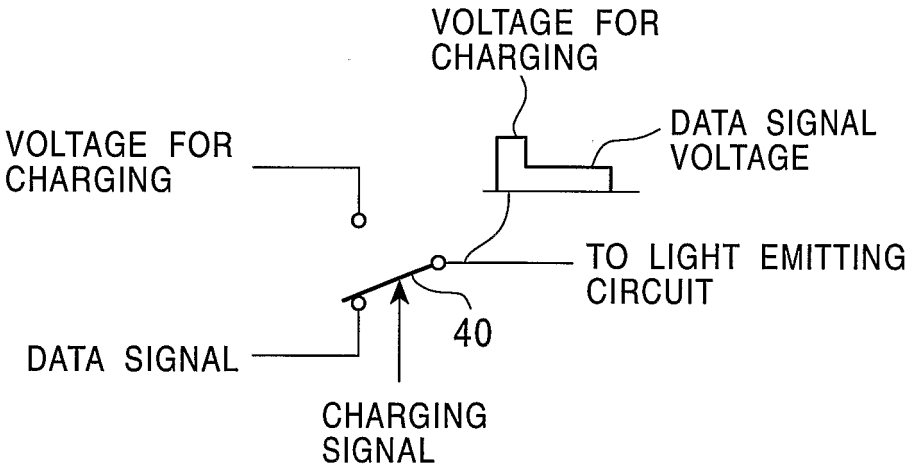
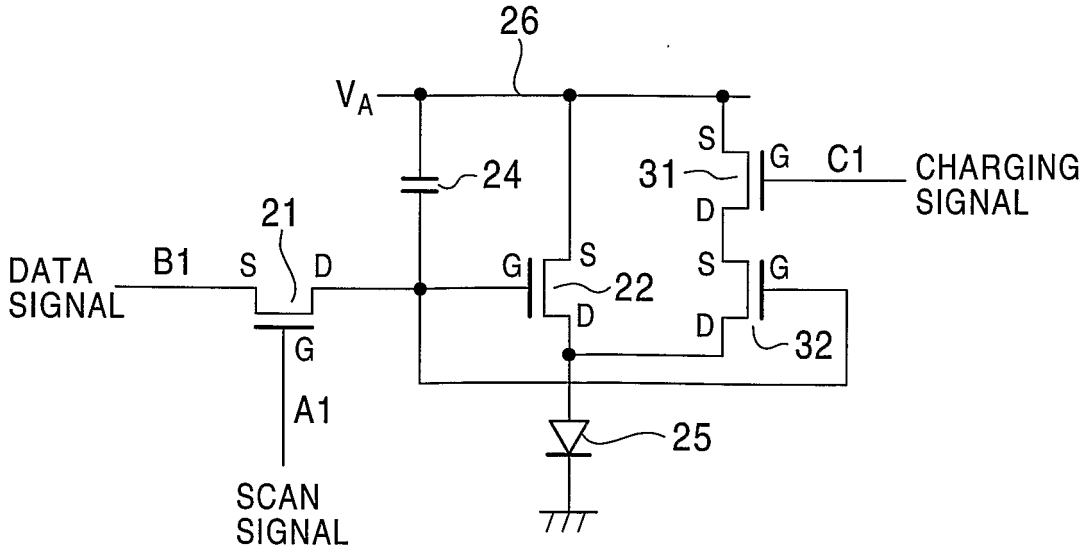

VOLTAGE FOR CHARGING
DATA SIGNAL VOLTAGE
VOLTAGE FOR CHARGING
TO LIGHT EMITTING CIRCUIT
40
DATA SIGNAL
CHARGING SIGNAL

FIG. 17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V_A
24
21
DATA SIGNAL
B1
S
D
G
A1
SCAN SIGNAL
G
S
D
22
25
S
G
C1
31
D
CHARGING SIGNAL
S
G
D
32

FIG. 18A

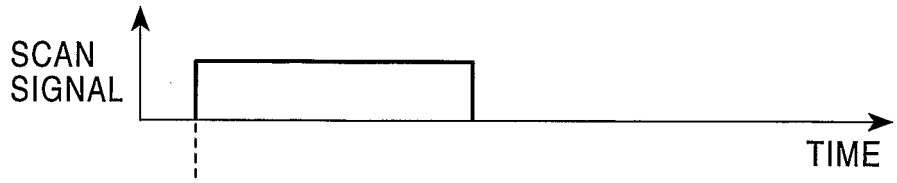


FIG. 18B

FIG. 18C

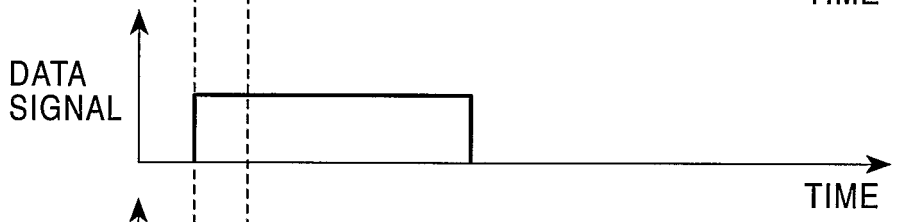


FIG. 18D

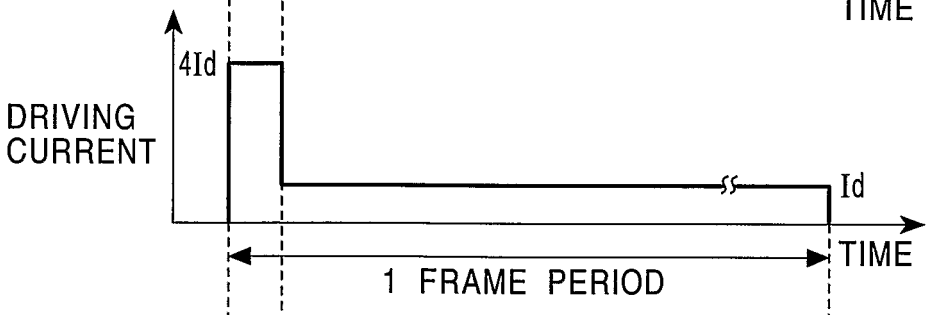


FIG. 18E

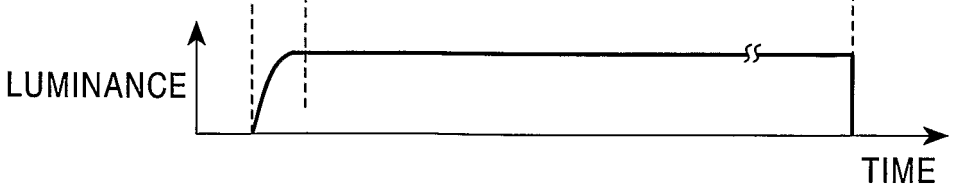
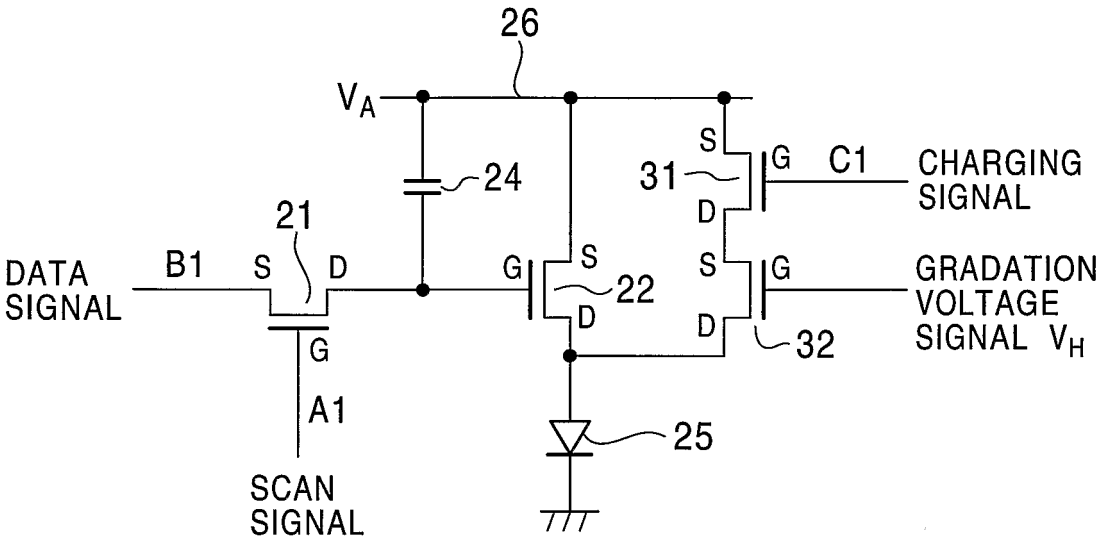


FIG. 19


26
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DATA SIGNAL
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D
G
A1
SCAN SIGNAL
S
22
D
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G
C1
31
D
CHARGING SIGNAL
S
G
GRADATION VOLTAGE SIGNAL V_H
D
32

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 02/12742

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 723 950 A (SO FRANKY ET AL) 3 March 1998 (1998-03-03) abstract; figure 3 the whole document	1-5 7-15
X Y	US 5 552 677 A (PAGONES ANDREW) 3 September 1996 (1996-09-03) the whole document	1-5 7-15
E	EP 1 282 104 A (SEIKO EPSON CORP) 5 February 2003 (2003-02-05) abstract the whole document	1-15
P,A	WO 02 071379 A (EMAGIN CORP) 12 September 2002 (2002-09-12) the whole document	1-15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
17 April 2003	07/05/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Wolff, L

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 02/12742

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5723950	A	03-03-1998	NONE		
US 5552677	A	03-09-1996	FR	2733852 A1	08-11-1996
			JP	8305318 A	22-11-1996
EP 1282104	A	05-02-2003	EP	1282104 A1	05-02-2003
			US	2003030602 A1	13-02-2003
WO 02071379	A	12-09-2002	WO	02071379 A2	12-09-2002

专利名称(译)	用于有机电致发光元件的发光电路和显示装置		
公开(公告)号	EP1451798A1	公开(公告)日	2004-09-01
申请号	EP2002788730	申请日	2002-12-05
[标]申请(专利权)人(译)	日本先锋公司		
申请(专利权)人(译)	先锋公司		
当前申请(专利权)人(译)	先锋公司		
[标]发明人	ISHIZUKA SHINICHI C O PIONEER CORPORATION TSUCHIDA MASAMI C O PIONEER CORPORATION		
发明人	ISHIZUKA, SHINICHI,C/O PIONEER CORPORATION TSUCHIDA, MASAMI,C/O PIONEER CORPORATION		
IPC分类号	H01L51/50 G09G3/20 G09G3/30 G09G3/32		
CPC分类号	G09G3/3233 G09G3/2022 G09G3/3291 G09G2300/0842 G09G2300/0861 G09G2310/0248 G09G2310/0251 G09G2320/0223 G09G2320/0233 G09G2320/0252		
优先权	2001372883 2001-12-06 JP		
外部链接	Espacenet		

摘要(译)

一种发光电路和显示装置，其响应于发光命令的产生而向有机电致发光元件提供正向驱动电流以使有机电致发光元件发光，并且在有机电致发光元件之后向有机电致发光元件提供充电电流。产生发光命令以对有机电致发光元件的电容成分充电。