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(71) Applicant: **LG Display Co., Ltd.**
SEOUL, 07336 (KR)

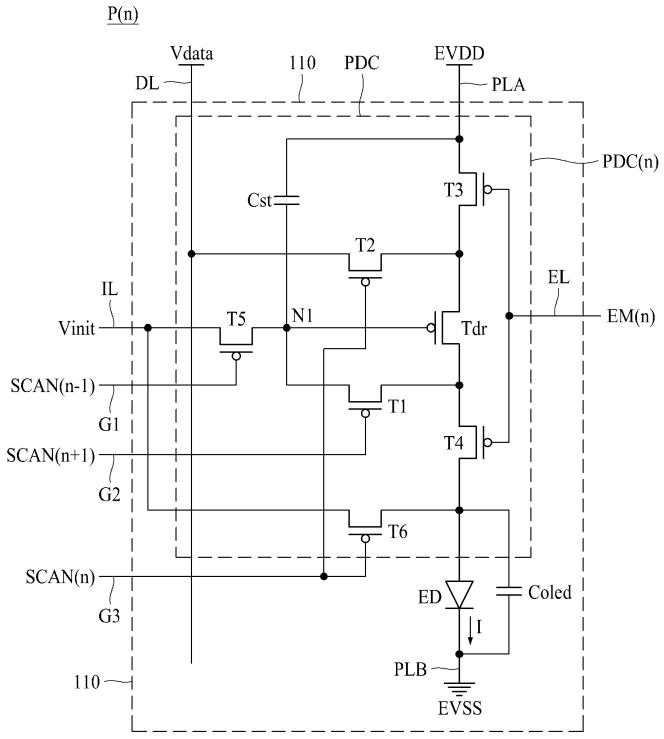
(72) Inventors:
- **CHO, Youngsung**
  10845 Paju-si (KR)
- **SO, Byeong-Seong**
  10845 Paju-si (KR)

(74) Representative: **Morrall, Jonathan Ian McLachlan et al**
Kilburn & Strode LLP
Lacon London
84 Theobalds Road
London WC1X 8NL (GB)

(54) LIGHT EMITTING DISPLAY APPARATUS

(57) Disclosed is a light emitting display apparatus in which two of three scan signals used by a pixel driving circuit provided in one pixel are supplied through two scan lines provided in the pixel and the other remaining signal is supplied through a scan line provided in another pixel adjacent to the pixel.

FIG. 2



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Description

BACKGROUND

Field of the Invention

[0001] The present disclosure relates to a light emitting display apparatus using an internal compensation scheme.

Discussion of the Related Art

[0002] When a light emitting display panel is used for a long time, a driving transistor supplying current to a light emitting device may be deteriorated, and deterioration of driving transistor leads to deterioration of image quality.

[0003] In order to compensate for the deterioration of driving transistor as described above, a pixel driving circuit for controlling the light emitting device includes a plurality of transistors other than driving transistor.

[0004] In particular, in the pixel driving circuit having the plurality of transistors for internal compensation, an operation of sensing a threshold voltage of driving transistor must be performed.

[0005] However, as the light emitting display apparatus is developed to have a high resolution, a time that may be allocated to the sensing is gradually decreased, resultantly reducing sensing performance of a threshold voltage for internal compensation.

SUMMARY

[0006] Accordingly, the present disclosure is directed to providing a light emitting display apparatus that substantially obviate one or more problems due to limitations and disadvantages of the related art. An invention is defined in the claims.

[0007] An example of the present disclosure is directed to providing a light emitting display apparatus in which two of three scan signals used by a pixel driving circuit provided in one pixel are supplied through two scan lines provided in the pixel and the other scan signal is supplied through a scan line provided in another pixel adjacent to the pixel.

[0008] Additional advantages and features of the disclosure will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the disclosure. The objectives and other advantages of the disclosure may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0009] To achieve these and other advantages and in accordance with the purpose of the disclosure, as embodied and broadly described herein, there is provided a light emitting display apparatus including: pixels each including a light emitting device outputting light and a pixel driving circuit driving the light emitting device, and signal lines connected to the pixel driving circuit. An nth pixel driving circuit driving a light emitting device included in an nth pixel among the pixels uses three scan signals, and two of the three scan signals are provided through two scan lines provided in the nth pixel driving circuit, and the remaining one scan signal is supplied through a scan line provided in an (n+1)th pixel adjacent to the nth pixel, n being an integer greater than or equal to 2.

[0010] It is to be understood that both the foregoing general description and the following detailed description of the present disclosure are exemplary and explanatory and are intended to provide further explanation of the disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this application, illustrate examples of the disclosure and together with the description serve to explain the principle of the disclosure. In the drawings:

FIG. 1 is a diagram schematically showing a configuration of a light emitting display apparatus according to the present disclosure.

FIG. 2 is a view showing a configuration of a pixel applied to a light emitting display apparatus according to the present disclosure.

FIGS. 3 to 8 are views illustrating a method of manufacturing a light emitting display panel applied to a light emitting display apparatus according to the present disclosure.

FIG. 9 is a plan view of an example of an organic light emitting display panel according to the present disclosure.

FIG. 10 is a view illustrating waveforms of signals applied to an organic light emitting display apparatus according to the present disclosure.

FIGS. 11 to 15 are views illustrating a method of driving a light emitting display apparatus according to an example of the present disclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0012] Reference will now be made in detail to the examples of the present disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0013] Advantages and features of the present disclosure, and implementation methods thereof will be clarified through following examples described with reference to the accompanying drawings. The present disclosure may, however, be embodied in different forms and should not be construed as limited to the examples set forth herein. Rather, these examples are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present disclosure to those skilled in the art. Furthermore, the present disclosure is only defined by scopes of claims.

[0014] In the specification, in adding reference numerals for elements in each drawing, it should be noted that like reference numerals already used to denote like elements in other drawings are used for elements wherever possible.

[0015] A shape, a size, a ratio, an angle, and a number disclosed in the drawings for describing examples of the present disclosure are merely an example, and thus, the present disclosure is not limited to the illustrated details. Like reference numerals refer to like elements throughout. In the following description, when the detailed description of the relevant known technology is determined to unnecessarily obscure the important point of the present disclosure, the detailed description will be omitted. In a case where 'comprise', 'have', and 'include' described in the present specification are used, another part may be added unless 'only~' is used. The terms of a singular form may include plural forms unless referred to the contrary.

[0016] In construing an element, the element is construed as including an error range although there is no explicit description.

[0017] In describing a position relationship, for example, when a position relation between two parts is described as 'on~', 'over~', 'under~', and 'next~', one or more other parts may be disposed between the two parts unless 'just' or 'direct' is used.

[0018] In describing a time relationship, for example, when the temporal order is described as 'after~', 'subsequent~', 'next~', and 'before~', a case which is not continuous may be included unless 'just' or 'direct' is used.

[0019] The term "at least one" should be understood as including any and all combinations of one or more of the associated listed items. For example, the meaning of "at least one of a first item, a second item, and a third item" denotes the combination of all items proposed from two or more of the first item, the second item, and the third item as well as the first item, the second item, or the third item.

[0020] It will be understood that, although the terms "first", "second", etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure.

[0021] Features of various examples of the present disclosure may be partially or overall coupled to or combined with each other, and may be variously inter-operated with each other and driven technically as those skilled in the art can sufficiently understand. The examples of the present disclosure may be carried out independently from each other, or may be carried out together in co-dependent relationship.

[0022] Hereinafter, examples of the present disclosure will be described in detail with reference to the accompanying drawings.

[0023] FIG. 1 is a view schematically showing a configuration of a light emitting display apparatus according to the present disclosure, and FIG. 2 is a view showing a configuration of a pixel applied to the light emitting display apparatus according to the present disclosure. Although P-type transistors are shown in FIG. 2, the light emitting display apparatus according to the present disclosure is not limited to the P-type transistors. FIG. 2 also shows an nth pixel driving circuit PDC(n) and a light emitting device ED provided in the nth pixel P(n) among the pixels 110 applied to the present disclosure, and n being an integer greater than or equal to 2.

[0024] As illustrated in FIGS. 1 and 2, the light emitting display apparatus according to the present disclosure includes pixels 110 including a light emitting device outputting light and a pixel driving circuit PDC driving the light emitting device ED and a driver supplying data voltages Vdata to signal lines connected to the pixel driving circuit PDC and data lines DL1 to DLd connected to the pixels 110 and supplying scan signals to the scan lines G connected to the pixels 110. G illustrated in FIG. 1 denotes the scan lines. The signal lines include the data lines DL1 to DLd and the scan line G.

[0025] A driver may include a data driver 300 supplying data voltages Vdata to the pixel driving circuits PDC provided in the pixels 110 through the data lines DL1 to DLd, a gate driver 200 supplying scan signals to the scan lines G and supplying an emission signal EM(n) to an emission line EL, and a controller 400 controlling driving of the data driver 300 and the gate driver 200. In addition, the light emitting display apparatus may include a power supply unit supplying

necessary power to the components.

[0026] In the present disclosure, an nth pixel driving circuit PDC(n) driving the light emitting device ED provided in an nth pixel P(n), among the pixels 110, use three scan signals SCAN(n-1), SCAN(n+1), and SCAN(n).

[0027] In this case, two scan signals SCAN(n-1), SCAN(n+1), among the three scan signals SCAN(n-1), SCAN(n+1), SCAN(n), are supplied through two scan lines G1 and G2 provided in the nth pixel P(n), and the other scan signal SCAN(n) is supplied through a scan line G3 included in the (n+1)th pixel.

[0028] Hereinafter, the above-described components will be sequentially described.

[0029] First, the pixels 110 and the signal lines are provided in a light emitting display panel 100.

[0030] As illustrated in FIGS. 1 and 2, the light emitting display panel 100 includes the pixels 110, the data lines DL1 to DLd, and the scan lines G1, G2, and G3, initialization lines IL to which an initialization voltage is supplied, emission lines EL, first driving voltage lines PLA, and second driving voltage lines PLB.

[0031] The scan lines G1, G2, and G3 may be formed in a first direction, for example, a widthwise direction, of the light emitting display panel 100.

[0032] Scan signals are supplied from the gate driver 200 to the pixel driving circuits PDC through the scan lines G1, G2, and G3.

[0033] In the nth pixel P(n), a (n-1)th scan signal SCAN(n-1) is applied to the first scan line G1, among the scan lines G1, G2, and G3, a (n+1)th scan signal SCAN(n+1) is supplied to the second scan line G2, and an nth scan signal SCAN(n) is supplied to the third scan line G3.

[0034] The data lines DL are formed to be parallel to each other at predetermined intervals in a second direction, e.g., a lengthwise direction, of the organic light emitting display panel 100 to intersect the first scan line G1, the second scan line G2, the third scan line G3, the initialization line IL, and the emission line EL. A data voltage Vdata is supplied to the data lines DL.

[0035] The first driving voltage lines PLA are formed to be parallel to the data lines DL in the second direction and are spaced apart from the data lines DL at regular intervals. The first driving voltage lines PLA are connected to the power supply unit and supply first driving voltages EVDD supplied from the power supply unit to the pixels 110.

[0036] The second driving voltage lines PLB supply a second driving voltage EVSS supplied from the power supply unit to the pixels 110.

[0037] The emission lines EL extend in the first direction and supply an emission signal EM for controlling light emission timing of the light emitting device ED to the pixels 110.

[0038] The initialization lines IL extend in the first direction and supply initialization voltages Vinit to the pixels 110. The initialization voltage Vinit may be supplied from the power supply unit or the gate driver 200 to the initialization lines IL.

[0039] Each of the pixels 110 includes the light emitting device ED and the pixel driving circuit PDC.

[0040] The pixel driving circuit PDC includes a driving transistor Tdr and a storage capacitor Cst for controlling the amount of current supplied to the light emitting device ED. In addition to driving transistor Tdr and the storage capacitor Cst, the pixel driving circuit PDC includes first to sixth transistors T1 to T6 and a light emitting device capacitor Coled.

[0041] That is, the pixel driving circuit PDC includes driving transistor Tdr having a first terminal, a second terminal, and a gate, a first transistor T1 having a gate connected to the second scan line G2, a first terminal connected to driving transistor Tdr, and a second terminal connected to the second terminal of driving transistor Tdr, a second transistor T2 having a gate connected to the third scan line G3, a first terminal connected to the data line DL, and a second terminal connected to the first terminal of driving transistor Tdr, a third transistor T3 having a first terminal connected to the first driving voltage line PLA, a second terminal connected to the first terminal of driving transistor Tdr, and a gate connected to the emission line EL, a fourth transistor T4 having a first terminal connected to the second terminal of driving transistor Tdr, a second terminal connected to the light emitting device ED, and a gate connected to the emission line EL, a fifth transistor having a gate connected to the first scan line G1, a first terminal connected to the initialization line IL, and a second terminal connected to the gate of driving transistor Tdr, a sixth transistor having a gate connected to the third scan line G3, a first terminal connected to the initialization line IL, and a second terminal connected to the second terminal of the fourth transistor and the light emitting device ED, and a storage capacitor Cst connected to the first terminal of the third transistor T3 and the gate of driving transistor Tdr. The gate of driving transistor Tdr is referred to as a first node N1. A first terminal and a second terminal of the light emitting device capacitor Coled may be connected to the first terminal and the second terminal of the light emitting device ED.

[0042] In this case, the first terminal of the light emitting device ED is connected to the second terminal of the fourth transistor T4 and the second terminal of the sixth transistor T6, and the second terminal thereof is connected to the second driving voltage line PLB.

[0043] One end of the storage capacitor Cst is connected to the first terminal of the third transistor T3 and the other end of the storage capacitor Cst is connected to the gate of driving transistor Tdr, i.e., a node N1, a second terminal of the fifth transistor T5, and a first terminal of the first transistor T1.

[0044] The storage capacitor Cst may charge the data voltage Vdata supplied through the data line DL and a threshold voltage of driving transistor Tdr.

[0045] Driving transistor Tdr is turned on by the data voltage Vdata stored in the storage capacitor Cst and controls the amount of current flowing from the first driving voltage line PLA to the light emitting device ED according to the data voltage Vdata.

[0046] The light emitting device ED emits light by a current I supplied from driving transistor Tdr and emits light having a luminance corresponding to the current I.

[0047] The third transistor T3 and the fourth transistor T4 are turned on by the emission signal EM transmitted through the emission line EL to control a light emission timing of the light emitting device ED.

[0048] The light emitting device capacitor Coled may serve to constantly maintain a voltage applied to the light emitting device ED.

[0049] The fifth transistor T5 supplies the initialization voltage Vinit to the first node N1.

[0050] The sixth transistor T6 supplies the initialization voltage Vinit to the light emitting device ED.

[0051] The first to sixth transistors T1 to T6 and the storage capacitor Cst perform a function of compensating for a change in a threshold voltage of driving transistor Tdr.

[0052] A method of compensating for the change in the threshold voltage of driving transistor Tdr by the first to sixth transistors T1 to T6 and the storage capacitor Cst will be described below with reference to FIGS. 1 to 15.

[0053] A detailed arrangement and form of the first to third scan lines G1, G2, and G3 and the emission line EL will be described in detail below with reference to FIGS. 1 to 9.

[0054] The light emitting device ED includes a first electrode, a light emitting layer provided on the first electrode, and a second electrode provided on the light emitting layer. The light emitting layer may include any one of a blue light emitting portion, a green light emitting portion, and a red light emitting portion for emitting light having a color corresponding to a color set in the pixel 110. The light emitting layer may include any one of an organic light emitting layer, an inorganic light emitting layer, or a quantum dot light emitting layer, or may include a stacked or mixed structure of the organic light emitting layer (or the inorganic light emitting layer) and the quantum dot light emitting layer.

[0055] Second, the gate driver 200 supplies a gate-on signal to the first to third scan lines G1, G2, and G3 using the gate control signals GCS transmitted from the controller 400.

[0056] Here, the gate-on signal refers to a signal capable of turning on the transistors connected to the first to third scan lines G1, G2 and G3. A signal capable of turning off the transistors is called a gate-off signal. The gate-on signal and the gate-off signal are collectively referred to as a scan signal.

[0057] A scan signal supplied to the first scan line G1 is referred to as a first scan signal, a scan signal supplied to the second scan line G2 is referred to as a second scan signal, and a scan signal supplied to the scan electrode G3 is referred to as a third scan signal.

[0058] Also, the gate driver 200 supplies the emission signals EM to the emission lines EL. The emission signal EM includes a gate-on signal capable of turning on the third transistor T3 and the fourth transistor T4 and a gate-off signal capable of turning off the third transistor T3 and the fourth transistor T4.

[0059] The gate driver 200 may be formed independently of the organic light emitting display panel 100 and may be connected to the organic light emitting display panel 100 through a tape carrier package TCP, a chip on film COF or a flexible printed circuit board (FPCB). However, the gate driver 200 may be directly formed on an outer portion of the organic light emitting display panel 100 through a manufacturing process of the pixel driving circuits PDCs using a gate in panel (GIP) scheme.

[0060] Third, the power supply unit supplies power to the gate driver 200, the data driver, and the controller 400. In particular, the power supply unit may supply the initialization voltages Vinit to the initialization lines IL.

[0061] Fourth, the controller 400 generates a gate control signal GCS for controlling driving of the gate driver 200 and a data control signal DCS for controlling driving the data driver 300 using a timing synchronization signal input from an external system. Further, the controller converts input image data input from the external system into image data Data and transmits the image data Data to the data driver 300.

[0062] In order to perform the functions as described above, the controller 400 may include a data aligning unit re-aligning input image data transmitted from the external system using the timing synchronization signal transmitted from the external system and supplying the re-aligned image data to the data driver 300, a control signal generating unit generating the gate control signal GCS and the data control signal DCS using the timing synchronization signal, an input unit distributing the timing synchronization signal transmitted from the external system and the input image data to the data aligning unit and the control signal generating unit, and an output unit outputting the image data generated by the data aligning unit and the control signals DCS and GCS generated by the control signal generating unit to the data driver 300 or the gate driver 200.

[0063] Fifth, the data driver 300 converts the image data Data transmitted from the controller 400 into data voltages, and supplies the data voltages to the data lines DL1 to DLd.

[0064] FIGS. 3 to 8 illustrate a method of manufacturing a light emitting display panel applied to a light emitting display apparatus according to an example of the present disclosure.

[0065] First, a multi-buffer is formed on a base substrate.

[0066] The base substrate may be formed by stacking polyimide (PI), silicon oxide (SiO_2), and polyimide (PI). In addition, the base substrate may be formed of glass.

[0067] The multi-buffer may include at least one of a buffer formed of silicon nitride (SiNx) and a buffer formed of silicon oxide (SiO_2).

[0068] For example, the buffer formed of silicon oxide (SiO_2) may be deposited on top of the buffer formed of silicon nitride (SiNx) to form the multi-buffer. Further, silicon oxide (SiO_2) may be deposited on top of the buffer formed of silicon nitride (SiNx) to form the multi-buffer.

[0069] Next, semiconductor patterns 10 may be formed on top of the multi-buffer in such a form as shown in FIG. 3. For example, the semiconductor pattern may be formed of amorphous silicon (a-Si), polysilicon, and an oxide semiconductor.

[0070] Next, the semiconductor pattern 10 and the entire surface of the multi-buffer are covered with a gate insulating layer. The gate insulating layer may be formed of silicon oxide (SiO_2).

[0071] Next, first metal patterns are formed on top of the gate insulating layer in such a form as shown in FIG. 4. The first metal patterns may be formed of a metal such as molybdenum (Mo), for example.

[0072] The first metal pattern disposed at the top of one of one pixel 110, among the first metal patterns, is used as the first scan line G1 and the first metal pattern disposed under the first scan line G1 is used as the second scan line G2, and the first metal pattern disposed below the second scan line G2 is used as the emission line EL.

[0073] That is, the first scan line G1, the second scan line G2, and the emission line EL are formed through the same process using the same material, and therefore, the first scan line G1, the second scan line G2, and the emission line EL are provided in the same layer.

[0074] In this case, the first scan line G1, the second scan line G2, and the emission line EL extend to all the pixels arranged in the first direction of the organic light emitting display panel 100.

[0075] Among the first metal patterns, the first metal pattern disposed between the second scan line G2 and the emission line EL forms any one terminal CT1 of the storage capacitor Cst. The first metal pattern forming any one terminal CT1 of the storage capacitor Cst is independently provided in each pixel 110 as shown in FIG. 4.

[0076] Next, the first metal patterns and the entire surface of the gate insulating layer are covered with the first insulating layer. The first insulating layer may be formed of silicon nitride (SiNx).

[0077] Next, first contact holes CNT0 are formed on the first insulating layer as shown in FIG. 5.

[0078] Next, second metal patterns are formed on the first insulating layer in such a form as shown in FIG. 6. The second metal patterns may be formed of, for example, a metal such as molybdenum (Mo).

[0079] Among the second metal patterns, the second metal pattern extending in the first direction may be used as the initialization line IL. In addition, the second metal pattern provided under the initialization line IL forms another terminal CT2 of the storage capacitor Cst. The second metal pattern forming another terminal CT2 of the storage capacitor Cst is independently provided at each pixel 110 as shown in FIG. 6.

[0080] Next, the second metal patterns and the entire surface of the first insulating layer are covered with a second insulating layer. The second insulating layer may be formed of silicon nitride (SiNx) or silicon oxide (SiO_2).

[0081] Next, second contact holes CNTs are formed on top of the second insulating layer in the form as shown in FIG. 7.

[0082] Next, third metal patterns are formed on top of the second insulating layer in such a form as shown in FIG. 8. The third metal patterns may be formed of at least one of titanium (Ti) and aluminum (Al), for example.

[0083] Any one of the third metal patterns is used as the data line DL and another third metal pattern is used as the first driving voltage line PLA.

[0084] In addition, among the third metal patterns, the third metal patterns other than the third metal patterns configuring the data line DL and the first driving voltage line PLA may electrically connect the first metal patterns to each other, electrically connect the second metal patterns to each other, or electrically connect the first metal patterns and the second metal patterns to each other.

[0085] That is, the data line DL and the first driving voltage line PLA are formed through the same process using the same material, and therefore, they are provided in the same layer.

[0086] Also, since the data line DL and the first driving voltage line PLA are provided on top of the second insulating layer covering the initialization line IL, the first driving voltage line PLA and the data line DL are provided in a layer different from the initialization line IL.

[0087] Since the initialization line IL is provided on top of the first insulating layer covering the first scan line G1, the second scan line G2, and the emission line EL, the initialization line IL is provided on a different layer from the first scan line G1, the second scan line G2 and the emission line EL.

[0088] Therefore, the first driving voltage line PLA and the data line DL are provided on a layer different from the initialization line IL, the first scan line G1, the second scan line G2, and the emission line EL.

[0089] In this case, the third metal patterns forming the data line DL and the first driving voltage line PLA extend to all the pixels 110 arranged in the second direction.

[0090] Among the third metal patterns, the third metal patterns other than the third metal patterns forming the data

line DL and the first driving voltage line PLA are present in an independent form in one pixel 110 and serve to electrically connect the metal patterns to each other as described above.

[0091] In addition, the third metal patterns may perform the functions of the first terminal and the second terminal of the transistors.

[0092] Finally, the third metal patterns and entire surface of the second insulating layer are covered with a passivation layer, various metal layers, an insulating layer, or the like, for completing the pixel driving circuit PDC are formed on top of the passivation layer, and the light emitting device ED may be provided. Accordingly, the organic light emitting display panel according to the present disclosure may be manufactured.

[0093] Here, the process after the third metal patterns are formed is the same as or similar to those of the method of manufacturing a current general organic light emitting display panel and is not a feature of the present disclosure. Therefore, a detailed description of the process after the third metal patterns are formed is omitted.

[0094] FIG. 9 is a plan view of an organic light emitting display panel according to an example of the present disclosure. In particular, FIG. 9 is a plan view illustrating all the components manufactured through FIGS. 3 to 8. FIG. 9 shows an nth pixel P(n) and an (n+1)th pixel P(n+1) manufactured through the above processes.

[0095] As described in the background of the invention, in the light emitting display panel of the related art, in order to perform the operation of sensing a threshold voltage during two horizontal periods (period corresponding to twice the period (1 horizontal period) in which the data voltage is supplied to the data lines), three scan signals must be supplied to the pixel driving circuit, and in this case, three scan lines must be provided in one pixel.

[0096] However, as the light emitting display apparatuses have been developed to have high resolution, a width of one pixel has been reduced, and thus, it is increasingly difficult to provide three scan lines in one pixel.

[0097] In order to solve this problem, in the light emitting display apparatus according to the present disclosure, two of the three scan signals used by the pixel driving circuit PDC included in one pixel 110 are supplied through two scan lines provided in the pixel and the other remaining scan signal is supplied through a scan line included in another pixel adjacent to the pixel 110.

[0098] For example, when FIG. 2 shows an nth pixel driving circuit PDC(n) and a light emitting device ED (n) provided in an nth pixel P(n) among the pixels 110 applied to the present disclosure and FIG. 9 shows the nth pixel P(n) and the (n+1)th pixel P(n+1), the nth pixel driving circuit PDC(n) for driving the light emitting device ED included in the nth pixel P(n) among the pixels 110 uses three scan signals, i.e., the first scan signal SCAN(n-1), the second scan signal SCAN(n+1) and the third scan signal SCAN(n).

[0099] In this case, two of the three scan signals SCAN(n-1), SCAN(n+1), and SCAN(n), that is, the first scan signal SCAN(n-1) and the second scan signal SCAN(n+1) are supplied through two scan lines, i.e., the first scan line G1 and the second scan line G2, provided in the nth pixel driving circuit PDC(n).

[0100] The other remaining one of the three scan signals SCAN(n-1), SCAN(n+1), and SCAN(n) is supplied through the third scan line G3 provided in the (n+1)th pixel P(n+1) adjacent to the nth pixel P(n).

[0101] In this case, the nth pixel P(n) and the (n+1)th pixel P(n+1) are adjacent to each other along the data line DL for supplying the data voltage Vdata to the pixels P(n) and P(n+1).

[0102] In other words, the three scan signals used in the nth pixel driving circuit PDC(n) are the (n-1)th scan signal SCAN(n-1), nth scan signal SCAN(n), and (n+1)th scan signal SCAN(n+1).

[0103] Here, the (n-1)th scan signal SCAN(n-1) is supplied through the first scan line G1 provided in the nth pixel driving circuit PDC(n) of the nth pixel P(n), the (n+1)th scan signal SCAN(n+1) is supplied through the second scan line G2 provided in the nth pixel driving circuit PDC(n) of the nth pixel P(n), and the nth scan signal SCAN(n) is supplied through the third scan signal G3 provided in the (n+1)th pixel driving circuit of the (n+1)th pixel P(n+1).

[0104] In this case, the emission line EL provided in the nth pixel driving circuit PDC(n) of the nth pixel P(n) and supplying the emission signal EM to the emission transistors T3 and T4 controlling light emission timing of the light emitting device ED is provided in a boundary portion of the nth pixel P(n) and the (n+1)th pixel P(n+1).

[0105] The second scan line G2 to which the (n+1)th scan signal SCAN(n+1) is supplied is further spaced apart from the boundary portion than the emission line EL.

[0106] The first scan line G1 supplied with the (n-1)th scan signal SCAN(n-1) is further spaced apart from the boundary portion than the second scan line G2.

[0107] The driving transistor Tdr is provided between the second scan line G2 and the emission line EL.

[0108] At least one of the transistors configuring the nth pixel driving circuit PDC(n) is provided in the (n+1)th pixel P(n+1).

[0109] That is, at least one of the transistors configuring the nth pixel driving circuit PDC(n) is driven by the nth scan signal SCAN(n) supplied through the third scan line G3 included in the (n+1)th pixel P(n+1).

[0110] For example, the transistors driven by the scan line, i.e., the third scan line G3, configuring the nth pixel driving circuit PDC(n) and provided in the (n+1)th pixel P(n+1) are the second transistor T2 and the sixth transistor T6 as shown in FIG. 9.

[0111] In addition to the second transistor T2 and the sixth transistor T6 configuring the nth pixel driving circuit PDC(n),

a fifth transistor T5' configuring the (n+1)th pixel driving circuit provided in the (n+1)th pixel P(n+1) may be connected to the third scan line G3. That is, two transistors T2 and T6 of the nth pixel P(n) and one transistor T5' of the (n+1)th pixel P(n+1) may be connected to the third scan line G3.

[0112] In this case, in the (n+1)th pixel P(n+1), the scan line supplied with the nth scan signal SCAN(n) is the first scan line G1', the scan line supplied with the (n+2)th scan signal SCAN(n+2) is the second scan line G2', and the scan line supplied with the (n+1)th scan signal SCAN(n+1) is the third scan line. The (n+1)th scan signal to be used in the (n+1)th pixel P(n+1) is provided in the (n+2)th pixel.

[0113] Among the transistors configuring the (n+1)th pixel driving circuit applied to the (n+1)th pixel P(n+1), the third transistor T3', the first transistor T1', the fourth transistor T4', the fifth transistor T5', and the driving transistor Tdr' are provided in the (n+1)th pixel P(n+1), and the second transistor and the sixth transistor are provided in the (n+2)th pixel.

[0114] Hereinafter, a method of driving a light emitting display apparatus according to the present disclosure will be described with reference to FIGS. 1 to 15. In the following description, the same or similar contents as those described with reference to FIGS. 1 to 9 are omitted or briefly described.

[0115] FIG. 10 is a view illustrating waveforms of signals applied to an organic light emitting display apparatus according to the present disclosure, and FIGS. 11 to 15 are views illustrating a method of driving a light emitting display apparatus according to the present disclosure.

[0116] First, as illustrated in FIG. 10, during a first period A, the first scan signal SCAN(n-1) having a low level is supplied to the fifth transistor T5, the second scan signal SCAN(n+1) having a high level is supplied to the first transistor T1, the third scan signal SCAN(n) having a low level is supplied to the second transistor T2 and the sixth transistor T6, and the emission signal EM having a high level is supplied to the third transistor T3 and the fourth transistor T4.

[0117] Therefore, as shown in FIG. 11, the fifth transistor T5, the second transistor T2, and the sixth transistor T6 are turned on, and the first transistor T1, the third transistor T3, and the fourth transistor T4 are all turned off.

[0118] In this case, the first node N1 connected to the gate of driving transistor Tdr is initialized by the initialization voltage. That is, a voltage of the first node N1 is the initialization voltage.

[0119] Since the initialization voltage Vinit is also transferred to the light emitting device ED through the sixth transistor T6, the light emitting device ED is also initialized to the initialization voltage Vinit.

[0120] Next, as shown in FIG. 10, during a second period B, the first scan signal SCAN(n-1) having a high level is supplied to the fifth transistor T5, the second scan signal SCAN(n+1) having a low level is supplied to the first transistor T1, the third scan signal SCAN(n) having a low level is supplied to the second transistor T2 and the sixth transistor, and the emission signal EM having a high level is supplied to the third transistor T3 and the fourth transistor T4.

[0121] Accordingly, as shown in FIG. 12, the first transistor T1, the second transistor T2, driving transistor Tdr, and the sixth transistor T6 are turned on, and the third to fifth transistors T3 to T5 are all turned off.

[0122] In this case, the data voltage Vdata is supplied to the first node N1 through the data line DL, the second transistor T2, driving transistor Tdr, and the first transistor T1.

[0123] Accordingly, the data voltage Vdata and a threshold voltage of driving transistor Tdr are supplied to the first node N1. Accordingly, the data voltage Vdata and the threshold voltage are charged in the storage capacitor Cst.

[0124] Also, the light emitting device ED is continuously initialized to the initialization voltage Vinit.

[0125] Next, as shown in FIG. 10, during a third period C, the first scan signal SCAN(n-1) having a high level is supplied to the fifth transistor T5, the second scan signal SCAN(n+1) having a low level is supplied to the first transistor T1, the third scan signal SCAN(n) having a high level is supplied to the second transistor T2 and the sixth transistor T6, and the emission signal EM having a high level is supplied to the third transistor T3 and the fourth transistor T4.

[0126] Thus, as shown in FIG. 13, the first transistor T1 is turned on and the second to sixth transistors T2 to T6 are all turned off.

[0127] In this case, the data voltage Vdata supplied to the first terminal of driving transistor Tdr, that is, to the second node N2 shown in FIG. 13, during the second period B is not supplied to the second node N2 any longer because the second transistor T2 is turned off during the third period C. In this case, the driving transistor Tdr may be turned on by the data voltage supplied to the first node N1 during the second period B, and thus, the data voltage Vdata applied to the first node N1 in a floating state may be supplied to the first node N1 through driving transistor Tdr. In this case, the threshold voltage of driving transistor Tdr may also be applied to the first node N1.

[0128] Therefore, the threshold voltage of driving transistor Tdr may be continuously charged in the storage capacitor Cst connected to the first node N1.

[0129] That is, in the present disclosure, the threshold voltage of driving transistor Tdr is charged in the storage capacitor Cst during the second period B and the third period C, that is, during two horizontal periods. Accordingly, the threshold voltage of driving transistor Tdr may be sufficiently stored in the storage capacitor Cst, and thus, compensation efficiency of the threshold voltage may be increased.

[0130] Next, as shown in FIG. 10, during a fourth period D and a fifth period E, the first scan signal SCAN(n-1) having a high level is supplied to the fifth transistor T5, the second scan signal SCAN(n+1) having a high level is supplied to the first transistor T1, the third scan signal SCAN(n) having a high level is supplied to the second transistor T2 and the

sixth transistor T6, and the emission signal EM having a high level is supplied to the third transistor T3 and the fourth transistor T4.

[0131] Thus, as shown in FIG. 14, the first to sixth transistors T1 to T6 all turned off.

[0132] In this case, the voltage of the first node N1 is maintained as the sum of the threshold voltage Vth of driving transistor Tdr and the data voltage Vdata. That is, the storage capacitor Cst is charged with the threshold voltage and the data voltage.

[0133] Lastly, as shown in FIG. 10, during a sixth period F, the first scan signal SCAN(n-1) having a high level is supplied to the fifth transistor T5, the second signal SCAN(n-1) having a high level is supplied to the first transistor T1, the third scan signal SCAN(n) having a high level is supplied to the second transistor T2 and the sixth transistor, and the emission signal EM having a low level is supplied to the third transistor T3 and the fourth transistor T4.

[0134] Accordingly, as shown in FIG. 15, the first transistor T1, the second transistor T2, the fifth transistor T5, and the sixth transistor T6 are turned off, and the third transistor T3, the driving transistor Tdr, and the fourth transistor T4 are all turned on.

[0135] Since the data voltage Vdata and the threshold voltage Vth are supplied to the gate of driving transistor Tdr, the driving transistor Tdr is also turned on.

[0136] Accordingly, a current may be supplied to the light emitting device ED through the third transistor T3, the driving transistor Tdr, and the fourth transistor T4, and the light emitting device ED may output light having a brightness corresponding to the current.

[0137] In this case, the voltage applied to the gate of the driving transistor Tdr is [Vdata+Vth], the voltage applied to the source of the driving transistor Tdr is the first driving voltage EVDD, and the current passing through the driving transistor Tdr is proportional to a voltage obtained by subtracting the threshold voltage Vth of the driving transistor Tdr from a difference voltage (Vgs=Vdata+Vth-EVDD) between the gate and the source of the driving transistor Tdr.

[0138] That is, the current I supplied to the light emitting device ED through the driving transistor Tdr may be expressed by Equation 1 below.

$$[\, I \propto (Vgs-Vth)^2 = (Vdata+Vth-EVDD-Vth))^2 = (Vdata-EVDD)^2] \quad \text{--- [1]}$$

[0139] The current supplied to the light emitting device ED through the driving transistor Tdr is determined by the data voltage Vdata and the first driving voltage EVDD and is not determined by the threshold voltage Vth of the driving transistor Tdr.

[0140] In general, the driving transistor Tdr may be deteriorated as the organic light emitting display apparatus is used for a long time, and thus, the threshold voltage Vth of the driving transistor Tdr may be changed.

[0141] In addition, the degree of deterioration of the driving transistor Tdr included in the pixel 110 formed in the organic light emitting display panel 100 may be varied depending on various reasons.

[0142] When the degrees of deterioration of the driving transistors Tdr are different, the threshold voltages of the driving transistors Tdr are also different from each other.

[0143] When the threshold voltages of driving transistors Tdr are different from each other, even if the same data voltage Vdata is supplied to the driving transistors Tdr, the magnitudes of the currents supplied to the light emitting devices ED through the driving transistors Tdr may be varied. As a result, the light emitting devices ED included in the pixels supplied with the same data voltage Vdata may output light of different brightness.

[0144] In order to solve the above problem, the present disclosure is configured such that the current flowing through driving transistor Tdr is not affected by the threshold voltage Vth of the driving transistor Tdr.

[0145] That is, in the present disclosure, by the structure of the pixel as shown in FIG. 2 and the driving method described with reference to FIGS. 10 to 15, the magnitude of the current I passing through the driving transistor Tdr is not affected by the threshold voltage of the driving transistor Tdr as shown in Equation [1].

[0146] Therefore, according to the present disclosure, even if the driving transistors Tdr are degraded, a normal current corresponding to the data voltage Vdata may be supplied to the light emitting device ED in each pixel, and accordingly, the light emitting device ED may output light having a brightness proportional to the data voltage Vdata.

[0147] In particular, in the present disclosure, two of the three scan lines required for the operation described above are arranged in one pixel, and the other scan line is disposed in another pixel adjacent to the pixel.

[0148] Thus, according to the present disclosure, even if the width of a pixel is reduced as the light emitting display apparatus is developed to have high resolution, the pixel driving circuit may accurately detect the threshold voltage of driving transistor during two horizontal periods using three scan signals. Further, in the above description, the storage capacitor Cst is charged with the threshold voltage of driving transistor Tdr during two horizontal periods, that is, the second period B and the third period C, but, if the width of the scan signals is increased to three horizontal periods, the storage capacitor may be charged with the threshold voltage of the driving transistor Tdr during three horizontal periods.

[0149] For example, in FIG. 10, if the (n-1)th scan signal SCAN(n-1) is increased by 1 horizontal period in a forward direction of the first period A, the nth scan signal SCAN(n) is also increased by 1 horizontal period in the forward direction of the first period A, and the (n+2)th scan signal having the width of 1 horizontal period in the direction of the fourth period D replaces the (n+1)th scan signal SCAN(n+1) illustrated in FIG. 10, then the storage capacitor may be charged with the threshold voltage of the driving transistor Tdr during a total of three horizontal periods from the second period B to the fourth period D.

[0150] That is, in the present disclosure, the period during which the threshold voltage of driving transistor Tdr is charged is not limited to the two horizontal periods but may be increased to three horizontal periods or longer depending on a pulse width of the scan signals and order of the scan signals.

[0151] According to the present disclosure, the threshold voltage of the driving transistor may be sensed during two horizontal periods using three scan signals. Accordingly, the threshold voltage may be more accurately sensed when compared with the light emitting display apparatus of the related art.

[0152] In addition, according to the present disclosure, in order to sense the threshold voltage of the driving transistor during two horizontal periods, two of the three scanning signals used by the pixel driving circuit provided in one pixel may be supplied through two scan lines provided in the pixel and the other remaining one scan signal may be supplied through a scan line provided in another pixel adjacent to the pixel. Therefore, even if the width of one pixel is reduced as the light emitting display apparatus is developed to have a high resolution, the pixel driving circuit may accurately sense the threshold voltage of the driving transistor during two horizontal periods using three scan signals.

[0153] The above-described feature, structure, and effect of the present disclosure are included in at least one example of the present disclosure, but are not limited to only one example. Furthermore, the feature, structure, and effect described in at least one example of the present disclosure may be implemented through combination or modification of other examples by those skilled in the art. Therefore, content associated with the combination and modification should be construed as being within the scope of the present disclosure.

Further examples of the present disclosure are provided in the following numbered clauses.

Clause 1. A light emitting display apparatus comprising: pixels each including a light emitting device outputting light and a pixel driving circuit driving the light emitting device; and signal lines connected to the pixel driving circuit, wherein an nth pixel driving circuit driving a light emitting device included in an nth pixel among the pixels uses three scan signals, and two of the three scan signals are provided through two scan lines provided in the nth pixel driving circuit, and the remaining one scan signal is supplied through a scan line provided in an (n+1)th pixel adjacent to the nth pixel.

Clause 2. The light emitting display apparatus of clause 1, wherein at least one of transistors configuring the nth pixel driving circuit is provided in the (n+1)th pixel driving circuit and driven by the scan line provided in the (n+1)th pixel.

Clause 3. The light emitting display apparatus of clause 1 or clause 2, wherein the nth pixel and the (n+1)th pixel are adjacent along data lines supplying data voltages to the pixels.

Clause 4. The light emitting display apparatus of any preceding clause, wherein the three scan signals used in the nth pixel driving circuit are (n-1)th scan signal, nth scan signal, and (n+1)th scan signal.

Clause 5. The light emitting display apparatus of clause 4, wherein the (n-1)th scan signal is supplied through a first scan line provided in the nth pixel driving circuit, the (n+1)th scan signal is supplied through a second scan line provided in the nth pixel driving circuit, and the nth scan signal is supplied through a third scan line provided in the (n+1)th pixel driving circuit.

Clause 6. The light emitting display apparatus of any preceding clause, wherein an emission line provided in the nth pixel driving circuit and supplying an emission signal to an emission transistor controlling a light emission timing of the light emitting device is provided in a boundary portion of the nth pixel and the (n+1) pixel among the pixels, the second scan line supplied with the (n+1)th scan signal is spaced apart from the boundary portion further than the emission line, the first scan line supplied with the (n-1)th scan signal is spaced apart from the boundary portion further than the second scan line, and a driving transistor is provided between the second scan line and the emission line.

Clause 7. The light emitting display apparatus of any of any preceding clause, wherein at least one of transistors configuring the nth pixel driving circuit is provided in the (n+1)th pixel.

Clause 8. The light emitting display apparatus of any of any preceding clause, wherein at least one of transistors configuring the nth pixel driving circuit is driven by an nth scan signal supplied through the third scan line provided in the (n+1)th pixel.

Clause 9. The light emitting display apparatus of any preceding clause, wherein the pixel driving circuit comprises: a driving transistor having a first terminal, a second terminal, and a gate; a first transistor having a gate connected to a second scan line, a first terminal connected to the gate of the driving transistor, and a second terminal connected to the second terminal of the driving transistor; a second transistor having a gate connected to a third scan line, a first terminal connected to a data line, and a second terminal connected to the first terminal of the driving transistor;

a third transistor having a first terminal connected to a first driving voltage line, a second terminal connected to the first terminal of the driving transistor, and a gate connected to an emission line; a fourth transistor having a first terminal connected to the second terminal of the driving transistor, a second terminal connected to the light emitting device, and a gate connected to the emission line; a fifth transistor having a gate connected to a first scan line, a first terminal connected to an initialization line, and a second terminal connected to the gate of the driving transistor; a sixth transistor having a gate connected to the third scan line, a first terminal connected to the initialization line, and a second terminal connected to the second terminal of the fourth transistor and the light emitting device; and a storage capacitor connected to the first terminal of the third transistor and the gate of the driving transistor.

Clause 10. The light emitting display apparatus of clause 9, wherein the second transistor and the sixth transistor configuring the nth pixel driving circuit are provided in the (n+1)th pixel.

Clause 11. The light emitting display apparatus of any preceding clause, wherein during a first period, a first node connected to a gate of a driving transistor controlling a magnitude of a current flowing to the light emitting device is initialized by an initialization voltage, during a second period, a storage capacitor connected to the first node is charged with a data voltage and a threshold voltage of the driving transistor, during a third period, the storage capacitor is charged with the data voltage and the threshold voltage of the driving transistor, during fourth and fifth periods, a voltage of the storage capacitor is maintained as the sum of the data voltage and the threshold voltage, and during a sixth period, a current corresponding to the data voltage is supplied to the light emitting device through the driving transistor.

[0154] It will be apparent to those skilled in the art that various modifications and variations may be made in the present disclosure without departing from the spirit or scope of the disclosures. Thus, it is intended that the present disclosure covers the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

Claims

1. A light emitting display apparatus (100) comprising:

a plurality of pixels (110), each pixel including:

a light emitting device (ED) configured to output light; and
a pixel driving circuit (PDC) configured to drive the light emitting device, the light emitting display apparatus further comprising:

signal lines connected to the pixel driving circuit,
wherein an nth pixel (P(n)) of the plurality of pixels comprises an nth pixel driving circuit (PDC(n)) configured to drive a corresponding light emitting device, the nth pixel driving circuit configured to use first, second and third scan signals, and
first and second scan lines (G1, G2) provided in the nth pixel driving circuit are configured to supply the first and second scan signals, and a third scan line (G3) provided in an (n+1)th pixel (P(n+1)) adjacent to the nth pixel is configured to supply the third scan signal, n being an integer greater than or equal to 2.

2. The light emitting display apparatus of claim 1 or claim 2, wherein
the nth pixel comprises a plurality of transistors (Tdr, T1, T2, T3, T4, T5, T6), one of the plurality of transistors being provided in the (n+1)th pixel, and wherein the third scan line is configured to drive the one of the plurality of transistors.

3. The light emitting display apparatus of any preceding claim, wherein
the nth pixel and the (n+1)th pixel are each positioned on a single data line, the data line configured to supply a data voltage to each of the nth and (n+1)th pixels.

4. The light emitting display apparatus of any preceding claim, wherein
the first scan signal is an (n-1)th scan signal, the second scan signal is an (n+1)th scan signal, and the third scan signal is an nth scan signal.

5. The light emitting display apparatus of claim 4, wherein
the (n-1)th scan signal is supplied through the first scan line , the (n+1)th scan signal is supplied through the second scan line , and the nth scan signal is supplied through the third scan line.

6. The light emitting display apparatus of any preceding claim, wherein
an emission line provided in the nth pixel driving circuit and supplying an emission signal to an emission transistor configured to control a light emission timing of the light emitting device corresponding to the nth pixel driving circuit, is provided in a boundary portion of the nth pixel and the (n+1) pixel, wherein the second scan line is further spaced apart from the boundary portion than the emission line, the first scan line is further spaced apart from the boundary portion than the second scan line, and a driving transistor (Tdr) is provided between the second scan line and the emission line.

7. The light emitting display apparatus of any of claims 1, 3, 4, 5 and 6, wherein
the nth pixel comprises a plurality of transistors and at least one of the plurality of transistors is provided in the (n+1)th pixel.

8. The light emitting display apparatus of any of claims 1, 3, 4, 5 and 6, wherein
the nth pixel comprises a plurality of transistors and the third scan line is configured to drive at least one of the plurality of transistors.

9. The light emitting display apparatus of claim 1, wherein
the nth pixel driving circuit comprises:

a driving transistor (Tdr) having a first terminal, a second terminal, and a gate;
a first transistor (T1) having a gate connected to a second scan line, a first terminal connected to the gate of the driving transistor, and a second terminal connected to the second terminal of the driving transistor;
a second transistor (T2) having a gate connected to a third scan line, a first terminal connected to a data line, and a second terminal connected to the first terminal of the driving transistor;
a third transistor (T3) having a first terminal connected to a first driving voltage line, a second terminal connected to the first terminal of the driving transistor, and a gate connected to an emission line;
a fourth transistor (T4) having a first terminal connected to the second terminal of the driving transistor, a second terminal connected to the light emitting device, and a gate connected to the emission line;
a fifth transistor (T5) having a gate connected to a first scan line, a first terminal connected to an initialization line, and a second terminal connected to the gate of the driving transistor;
a sixth transistor (T6) having a gate connected to the third scan line, a first terminal connected to the initialization line, and a second terminal connected to the second terminal of the fourth transistor and the light emitting device; and
a storage capacitor (Cst) connected to the first terminal of the third transistor and the gate of the driving transistor.

10. The light emitting display apparatus of claim 9, wherein
the second transistor (T2) and the sixth transistor (T6) are provided in the (n+1)th pixel.

11. The light emitting display apparatus of claim 1, configured such that:

during a first period, a first node (N1) connected to a gate of a driving transistor (Tdr) controlling a magnitude of a current flowing to the light emitting device is initialized by an initialization voltage,
during a second period, a storage capacitor (Cst) connected to the first node is charged with a data voltage and a threshold voltage of the driving transistor,
during a third period, the storage capacitor is charged with the data voltage and the threshold voltage of the driving transistor,
during fourth and fifth periods, a voltage of the storage capacitor is maintained as the sum of the data voltage and the threshold voltage, and
during a sixth period, a current corresponding to the data voltage is supplied to the light emitting device through the driving transistor.

FIG. 1

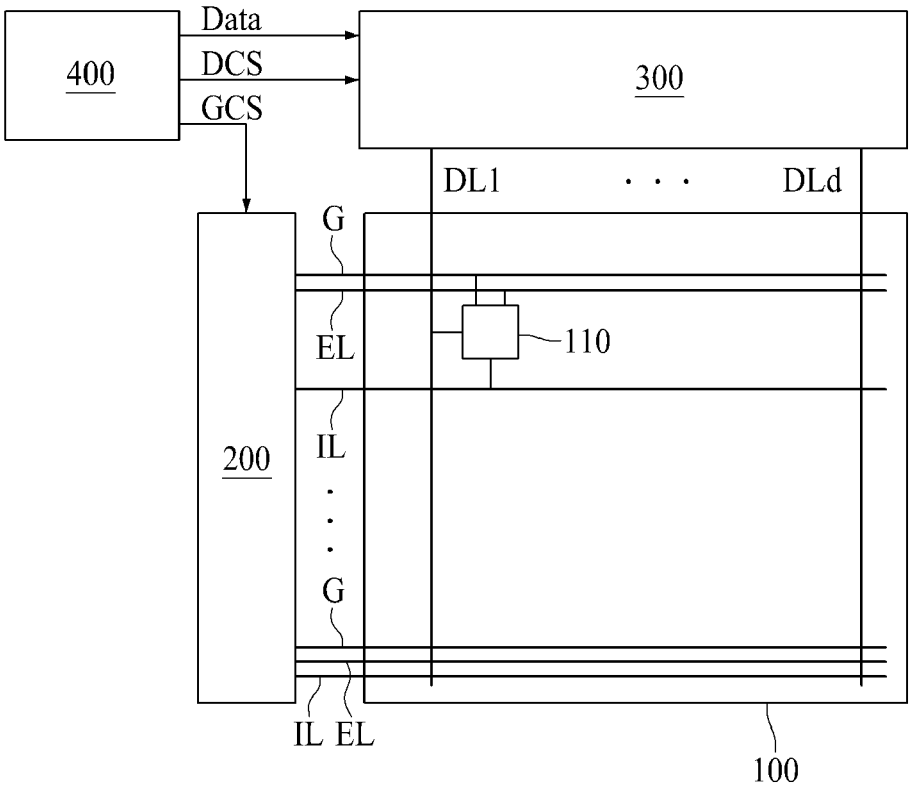


FIG. 2

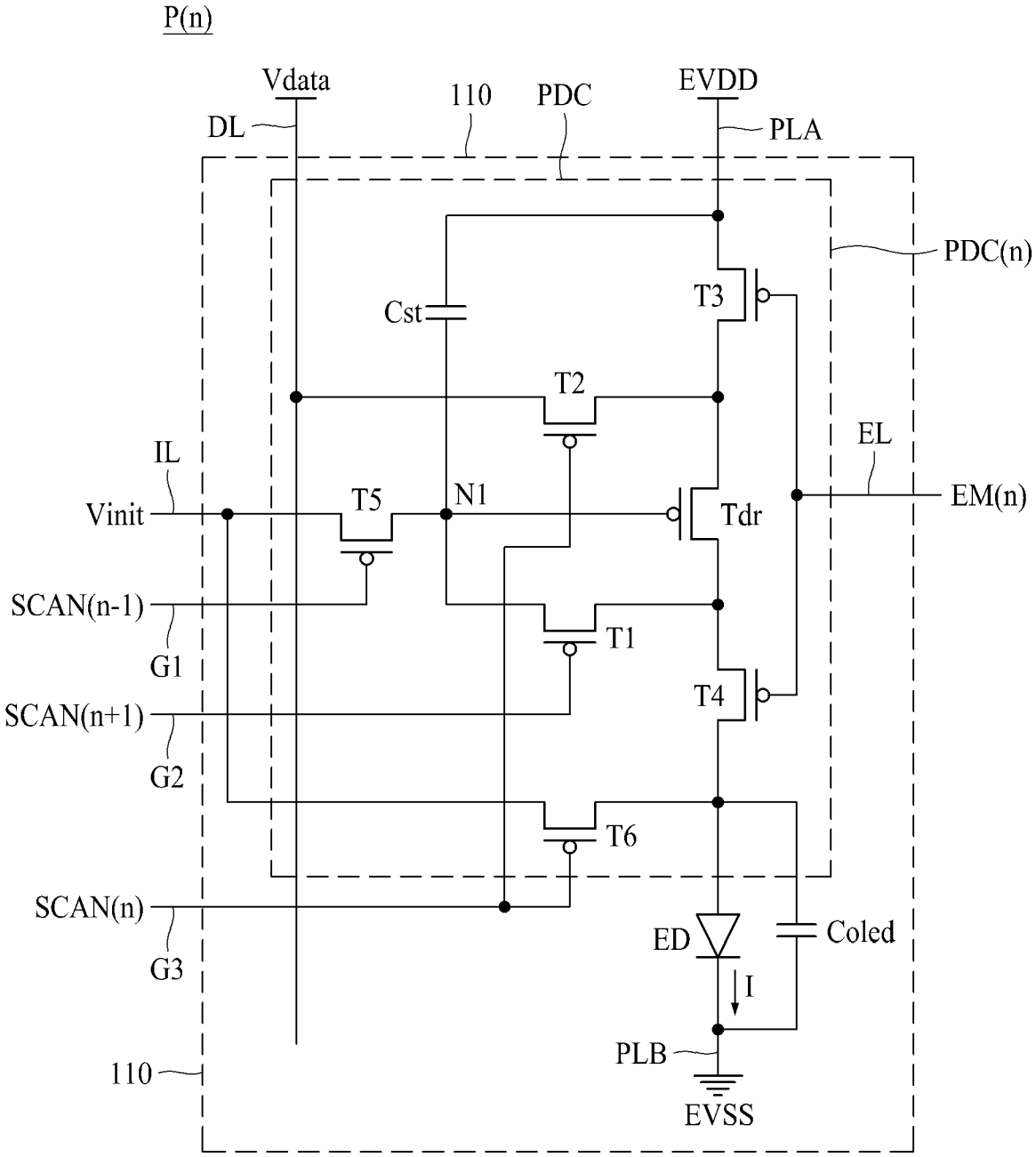

P(n)
Vdata
110
PDC
EVDD
DL
PLA
PDC(n)
Cst
T3
T2
EL
IL
Vinit
T5
N1
Tdr
EM(n)
SCAN(n-1)
G1
T1
T4
SCAN(n+1)
G2
T6
SCAN(n)
G3
ED
Coled
I
PLB
110
EVSS

FIG. 3

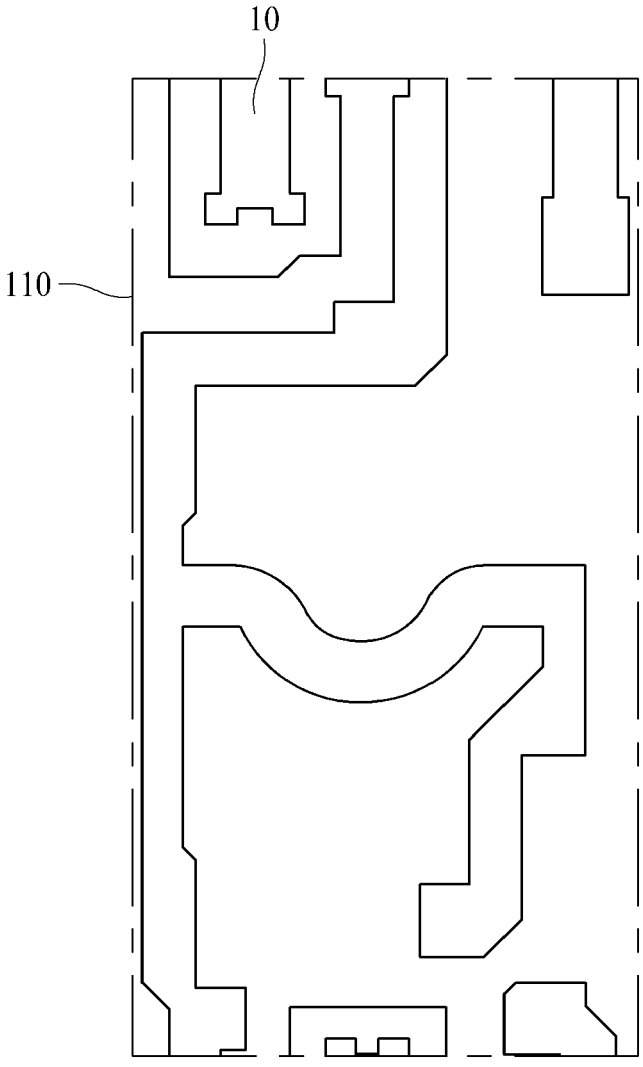


FIG. 4

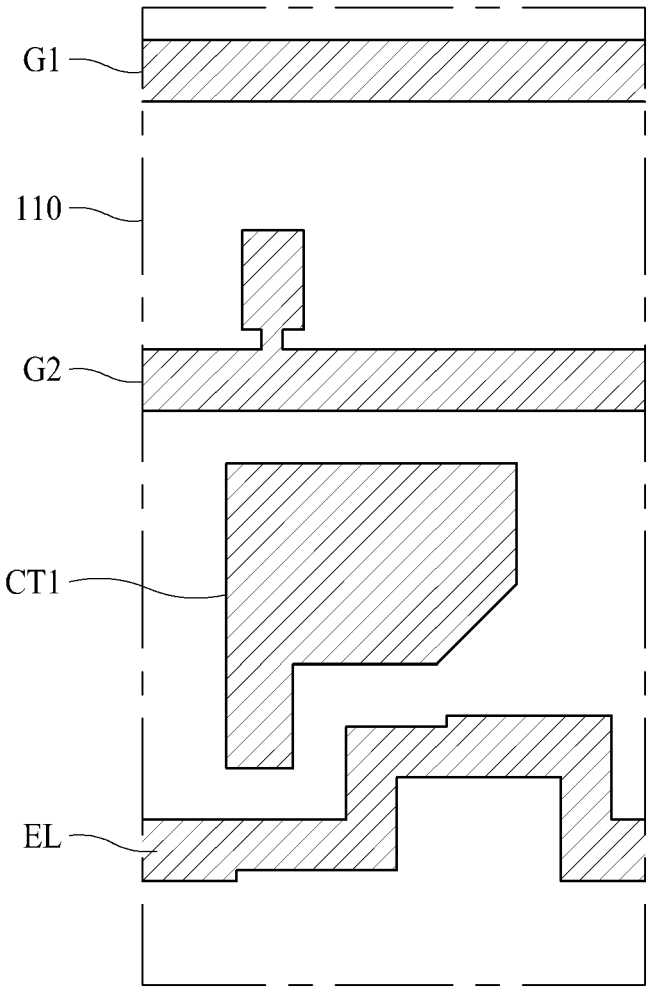


FIG. 5

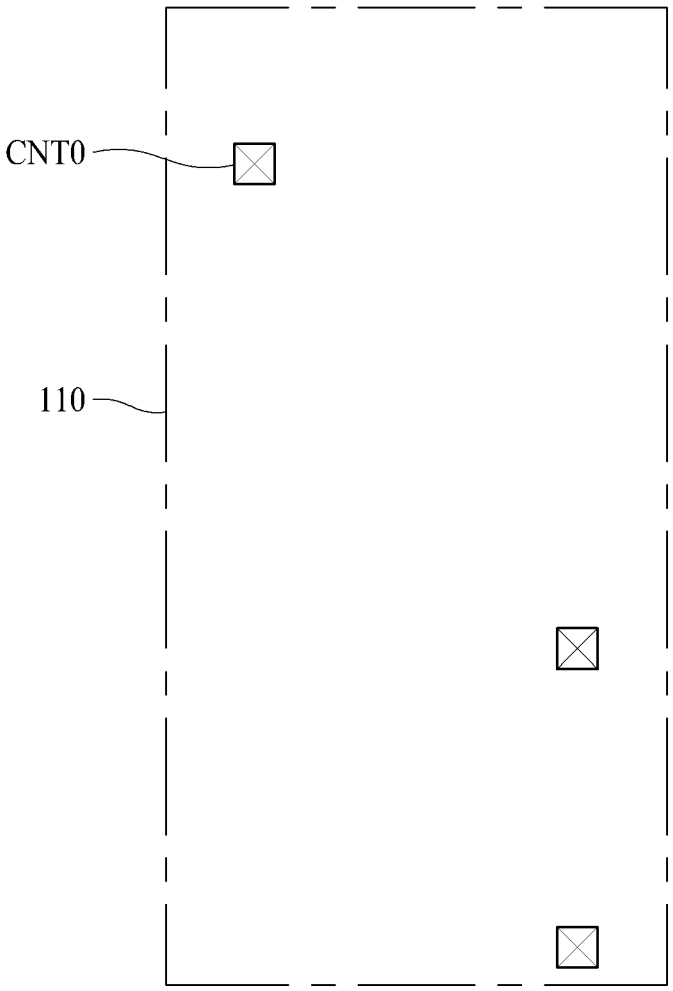


FIG. 6

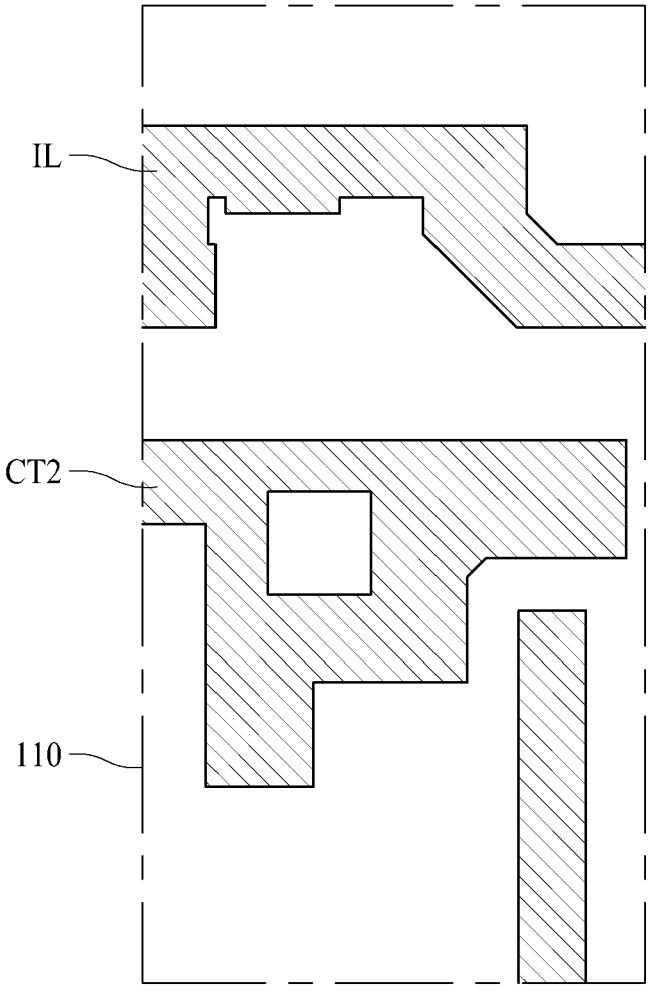


FIG. 7

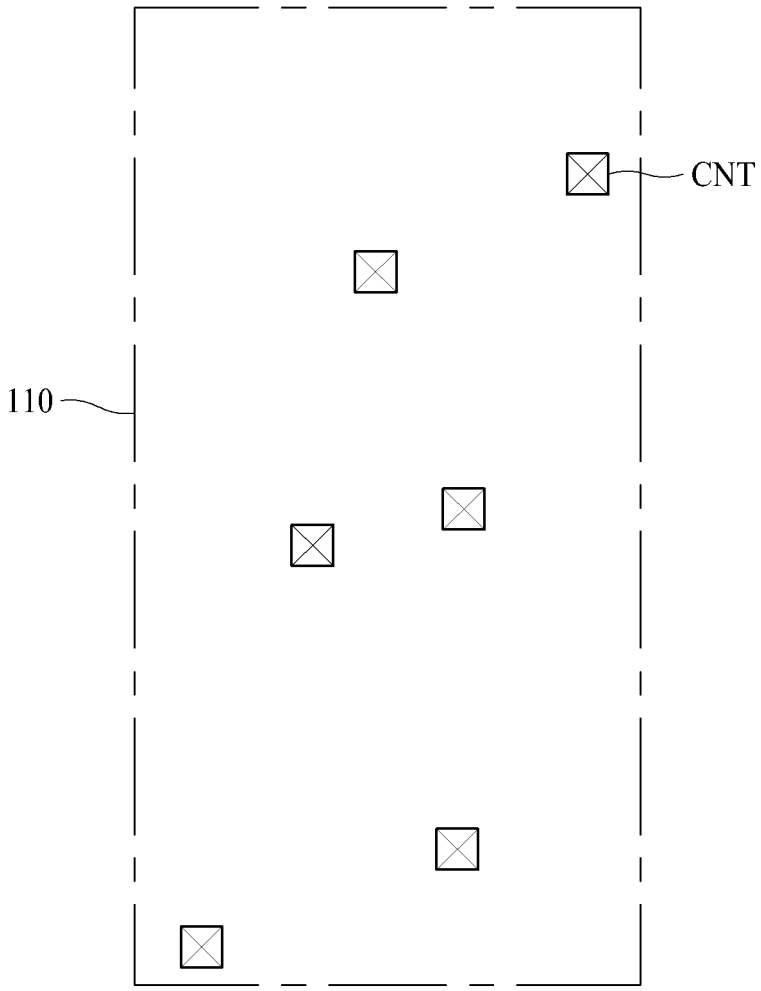


FIG. 8

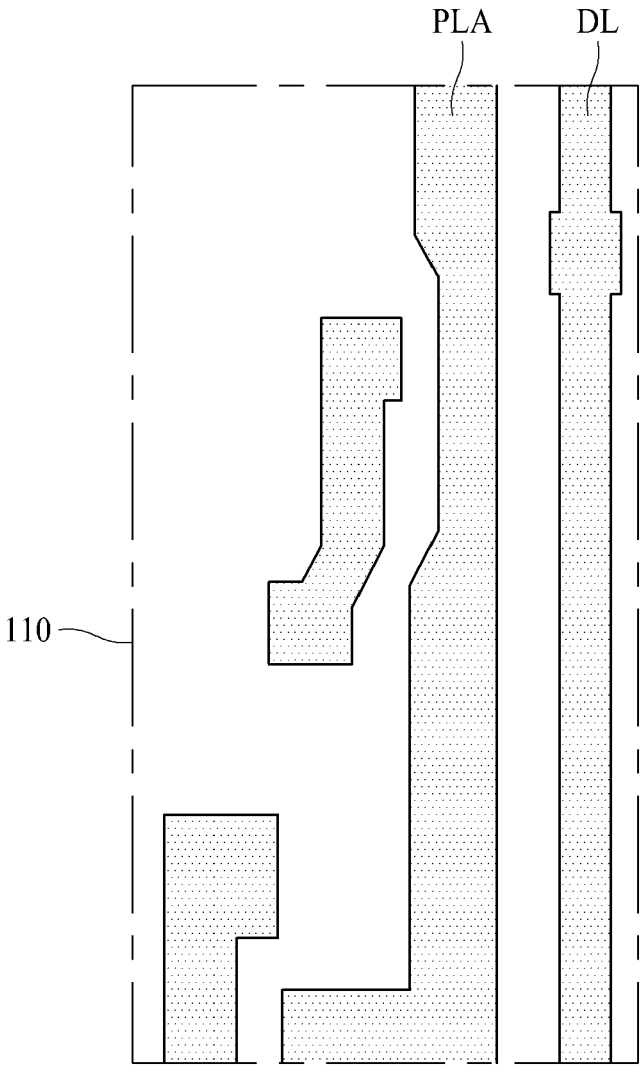


FIG. 9

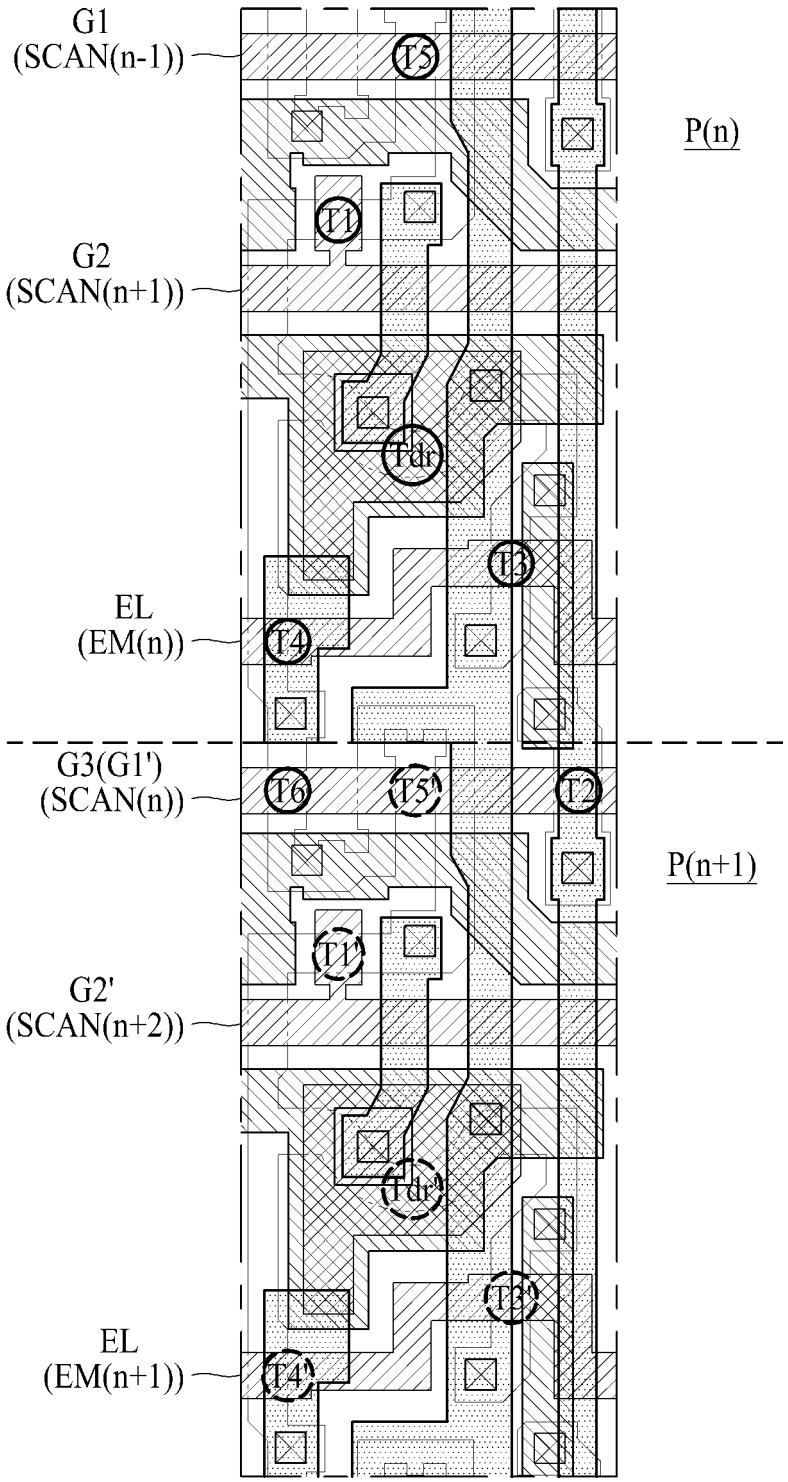

G1
(SCAN(n-1))
T5
P(n)
T1
G2
(SCAN(n+1))
Tdr
T3
EL
(EM(n))
T4
G3(G1')
(SCAN(n))
T6
T5'
T2
P(n+1)
T1'
G2'
(SCAN(n+2))
Tdr'
T3'
EL
(EM(n+1))
T4'

FIG. 10

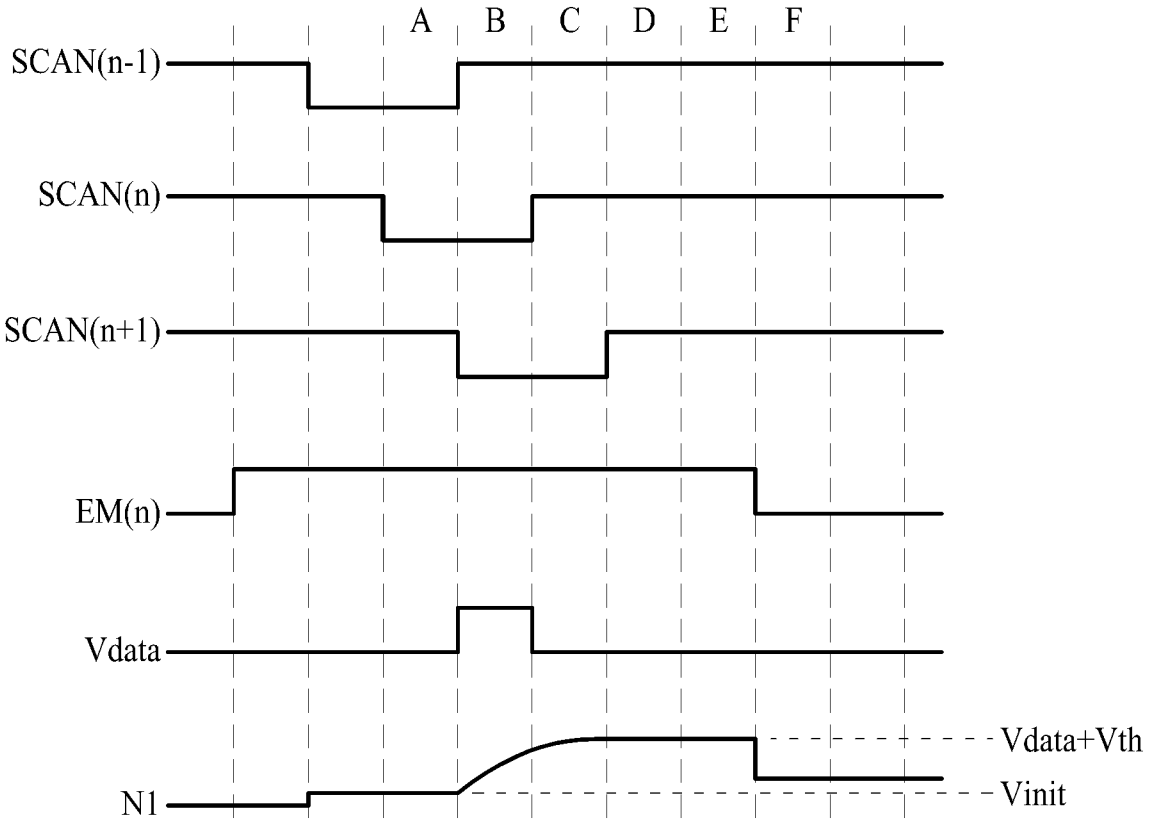


FIG. 11

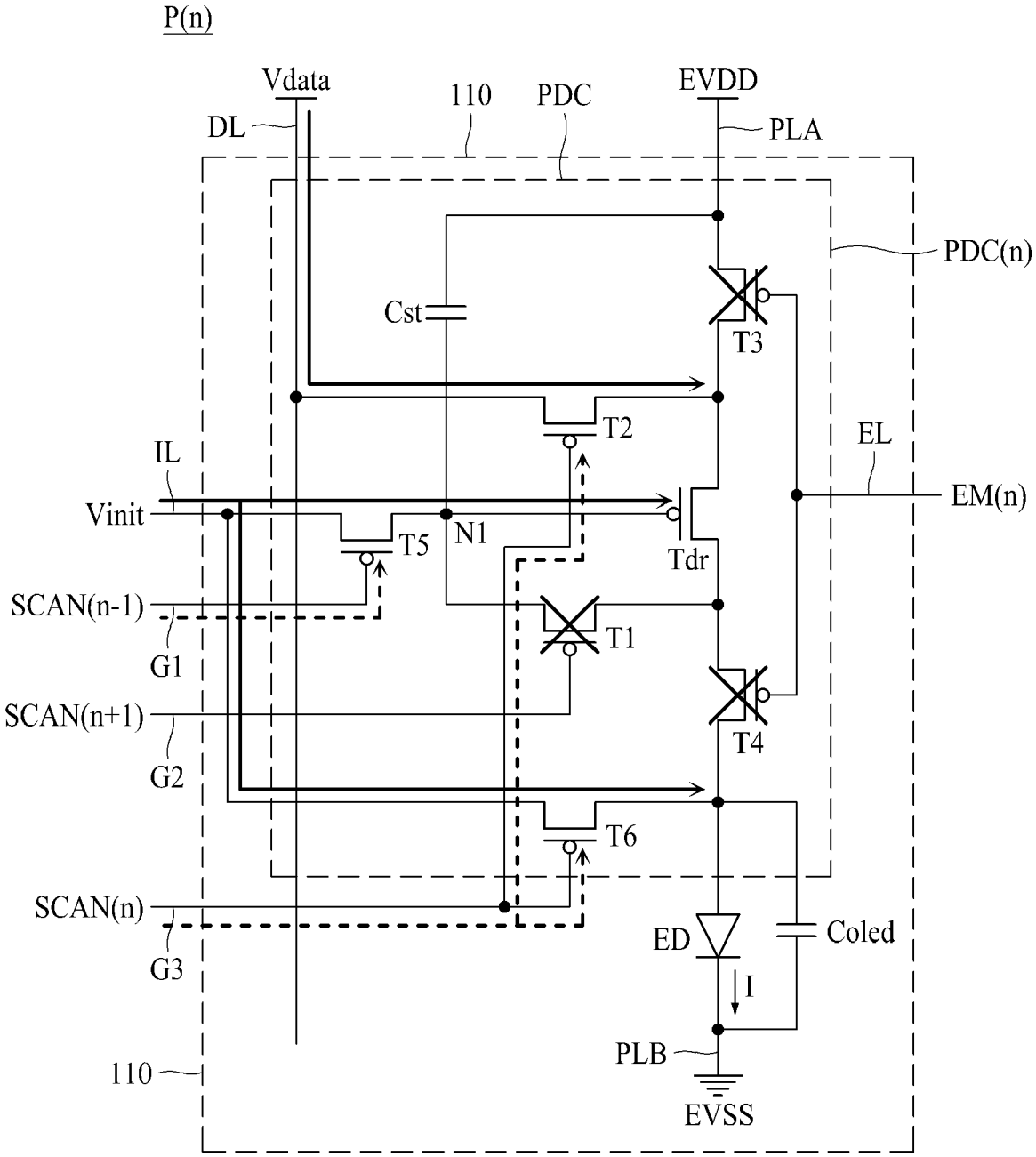

P(n)
Vdata
110
PDC
EVDD
DL
PLA
PDC(n)
Cst
T3
T2
EL
IL
EM(n)
Vinit
T5
N1
Tdr
SCAN(n-1)
T1
G1
SCAN(n+1)
T4
G2
T6
SCAN(n)
ED
Coled
G3
I
PLB
110
EVSS

FIG. 12

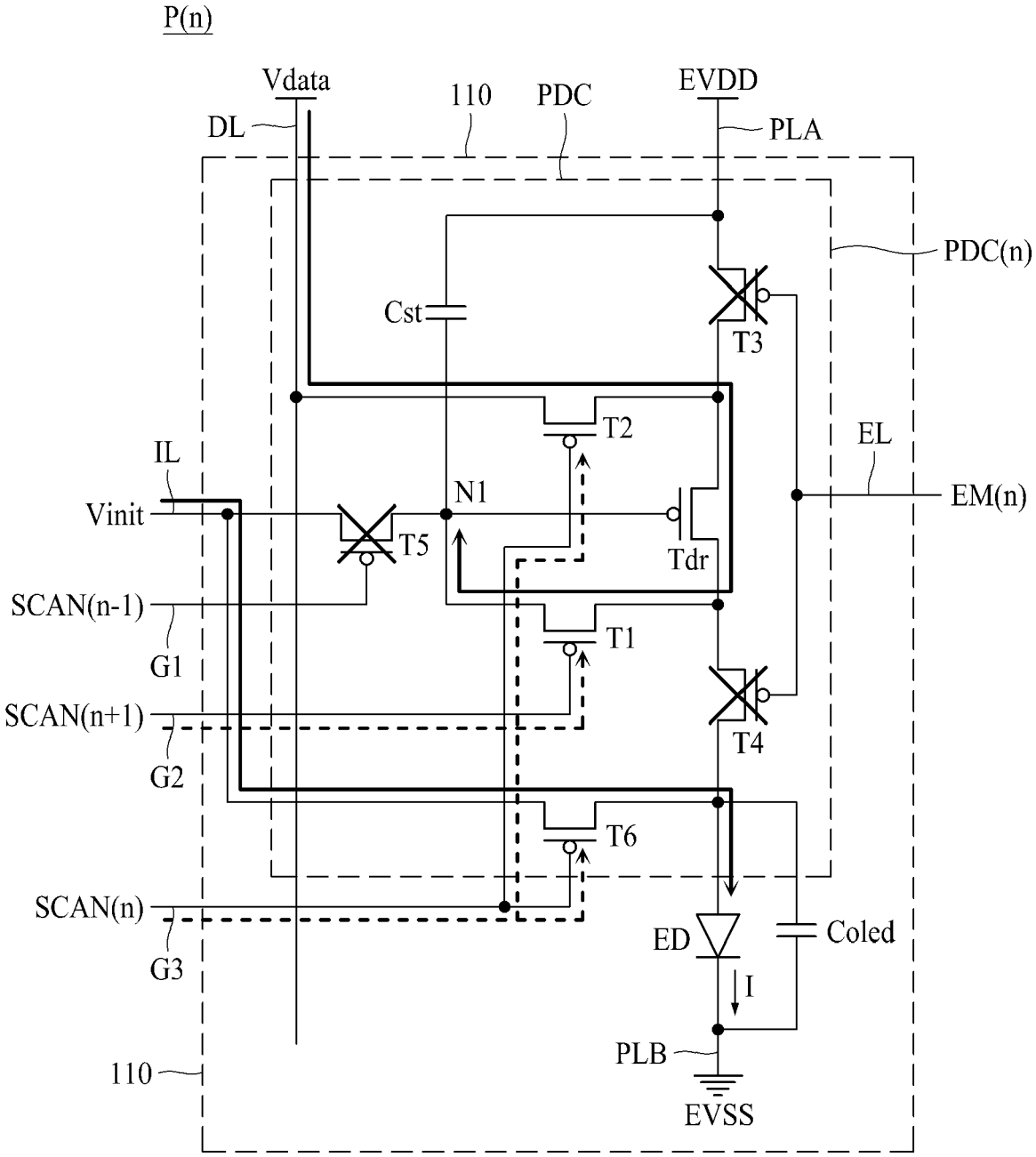

P(n)
Vdata
110
PDC
EVDD
DL
PLA
PDC(n)
Cst
T3
T2
EL
IL
N1
EM(n)
Vinit
T5
Tdr
SCAN(n-1)
T1
G1
SCAN(n+1)
T4
G2
T6
SCAN(n)
ED
Coled
G3
I
PLB
110
EVSS

FIG. 13

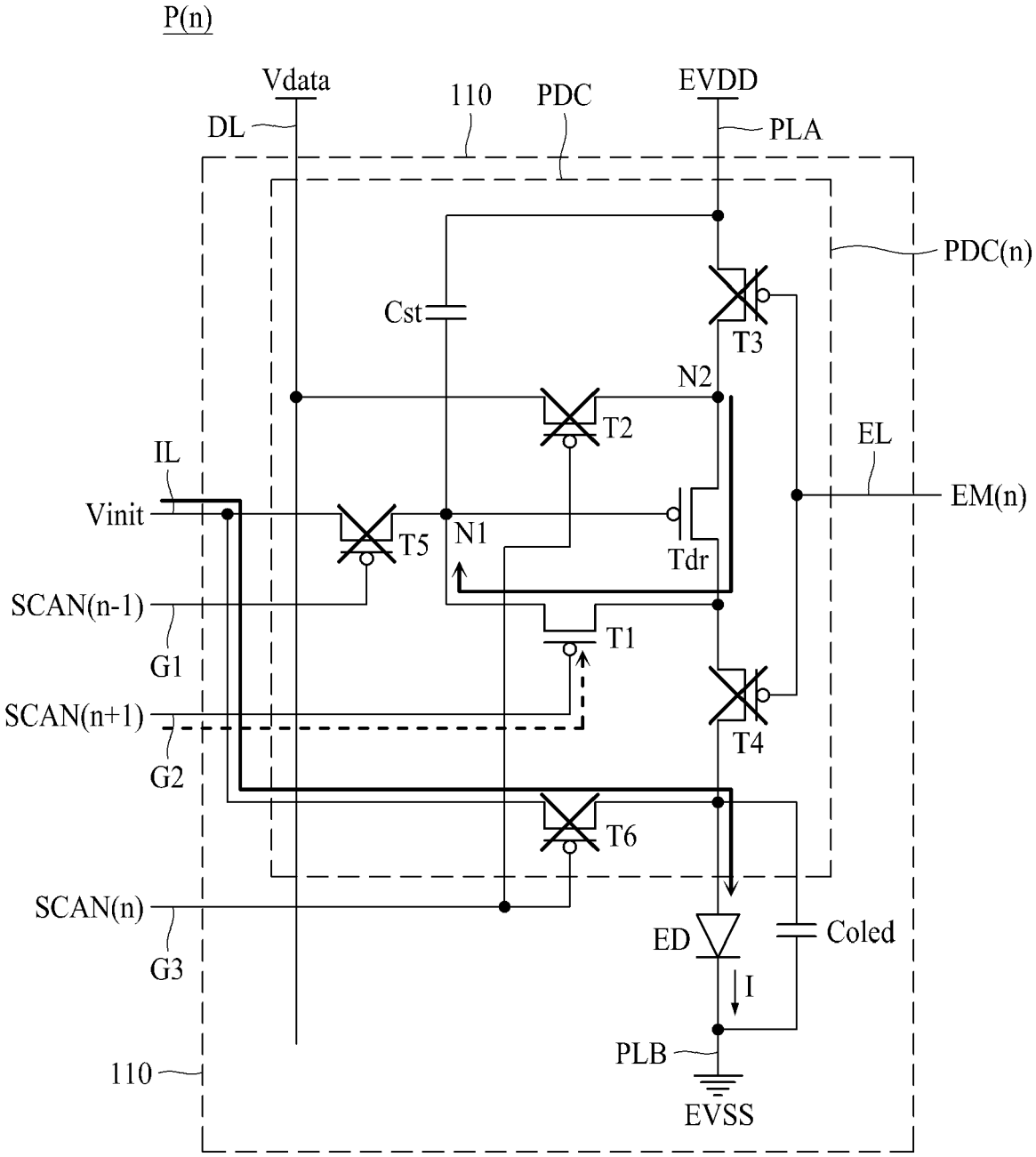
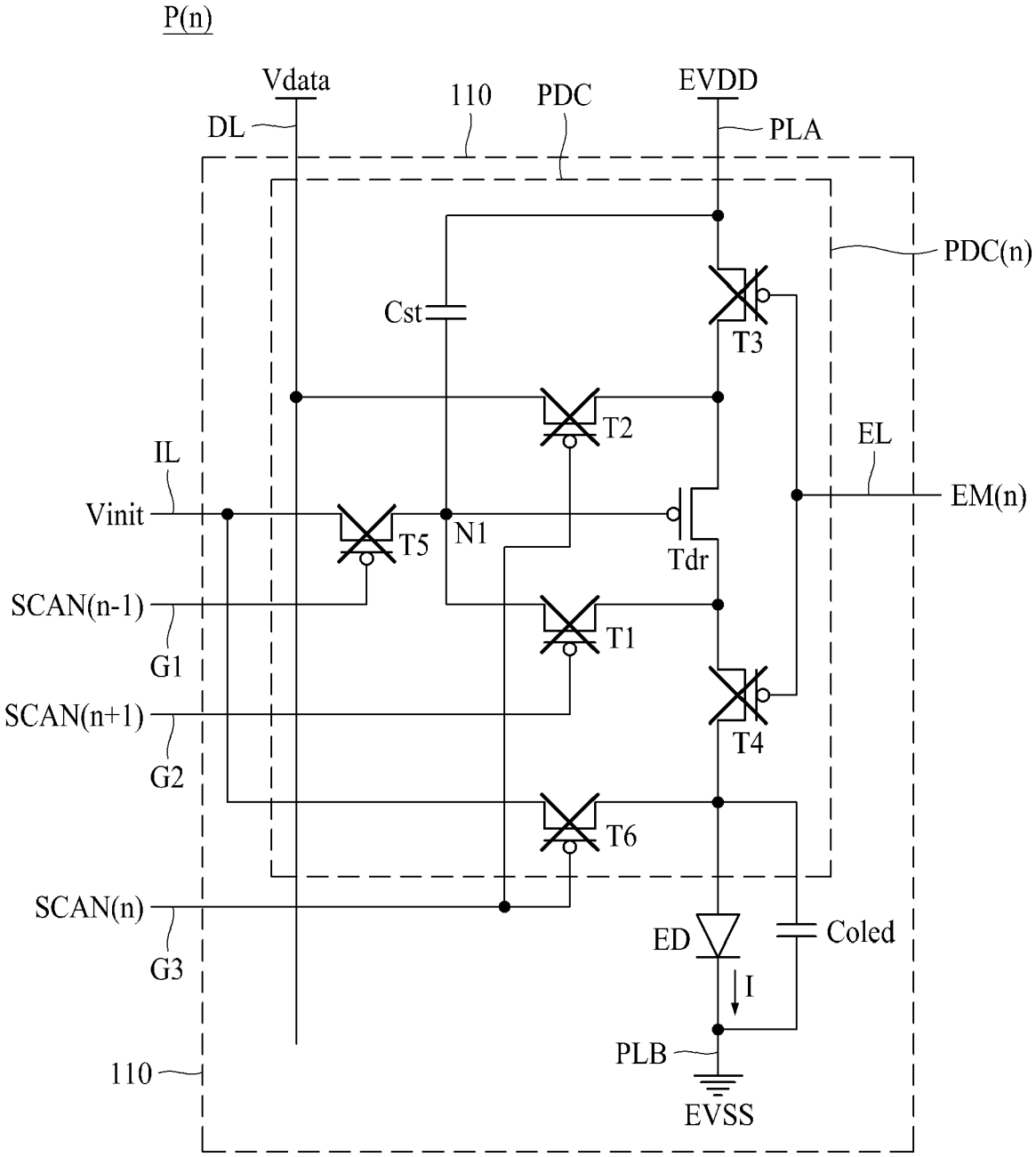

P(n)
Vdata
110
PDC
EVDD
DL
PLA
PDC(n)
Cst
T3
N2
T2
EL
IL
EM(n)
Vinit
T5
N1
Tdr
SCAN(n-1)
T1
G1
SCAN(n+1)
T4
G2
T6
SCAN(n)
ED
Coled
G3
I
PLB
110
EVSS

FIG. 14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PDC
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PLA
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IL
Vinit
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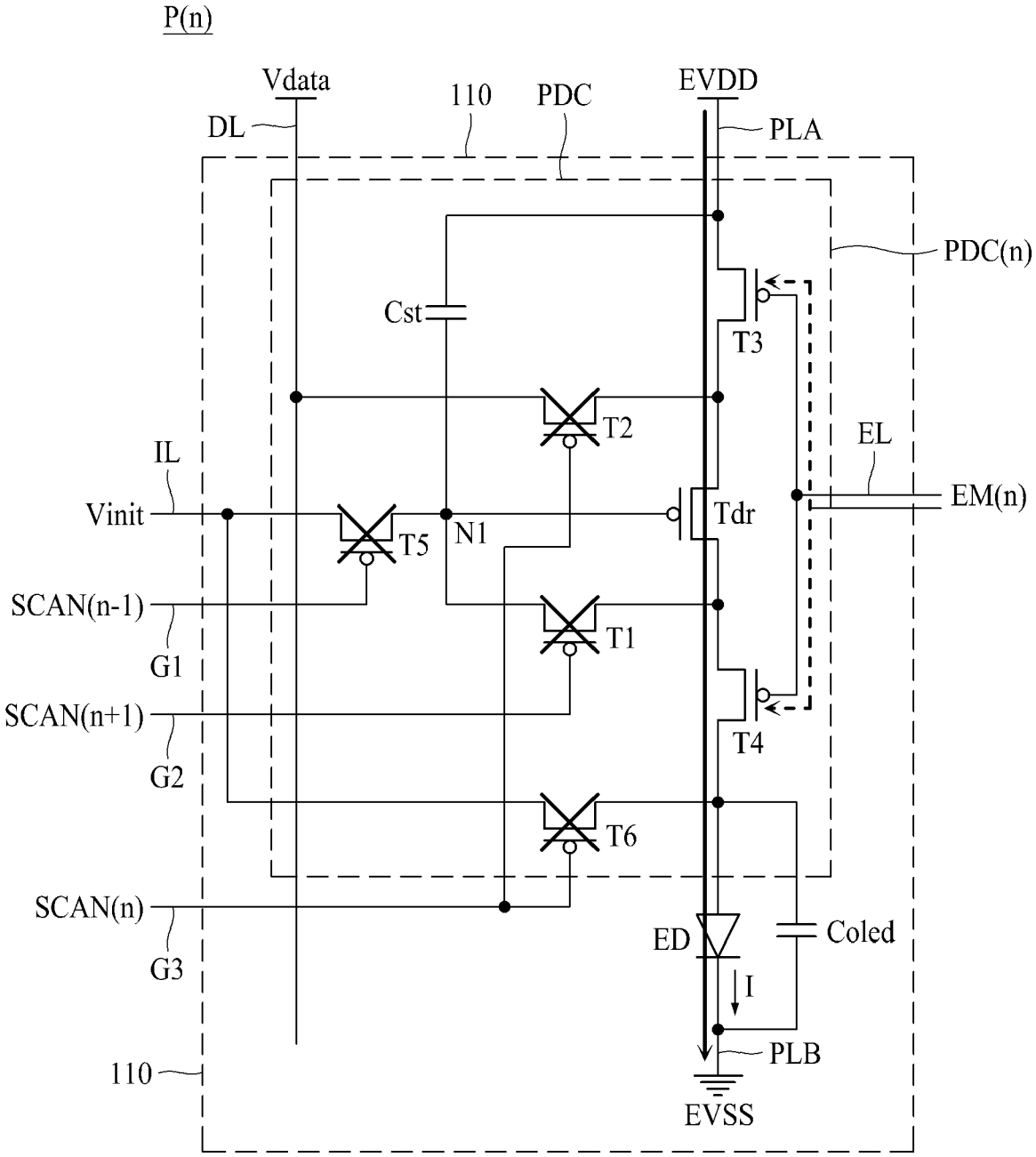
EM(n)
SCAN(n-1)
G1
T1
SCAN(n+1)
G2
T4
T6
SCAN(n)
G3
ED
Coled
I
PLB
110
EVSS

FIG. 15


P(n)
Vdata
110
PDC
EVDD
DL
PLA
PDC(n)
Cst
T3
T2
EL
IL
Vinit
T5
N1
Tdr
EM(n)
SCAN(n-1)
G1
T1
SCAN(n+1)
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T4
T6
SCAN(n)
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EUROPEAN SEARCH REPORT

Application Number
EP 19 21 7510

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2018/342571 A1 (KWON WONJU [KR] ET AL) 29 November 2018 (2018-11-29) * paragraphs [0005], [0060], [0072] - [0082]; figures 1,2,3,4F,7F *	1-11	INV. G09G3/3233 H01L27/32
X	US 2005/258466 A1 (KWAK WON-KYU [KR] ET AL) 24 November 2005 (2005-11-24) * paragraphs [0062] - [0067]; figures 5,6 *	1	

TECHNICAL FIELDS SEARCHED (IPC)
G09G
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	7 April 2020	Ladiray, Olivier

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 19 21 7510

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07-04-2020

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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	电致发光显示器		
公开(公告)号	EP3675108A1	公开(公告)日	2020-07-01
申请号	EP2019217510	申请日	2019-12-18
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	CHO YOUNGSUNG SO BYEONG SEONG		
发明人	CHO, YOUNGSUNG SO, BYEONG-SEONG		
IPC分类号	G09G3/3233 H01L27/32		
CPC分类号	G09G3/3233 G09G2300/0426 G09G2300/0465 G09G2300/0819 G09G2300/0842 G09G2300/0861 H01L27/3276 G09G3/3258 G09G3/3266 G09G3/3291		
审查员(译)	LADIRAY , OLIVIER		
优先权	1020180172037 2018-12-28 KR		
外部链接	Espacenet		

摘要(译)

公开了一种发光显示装置,其中通过设置在像素中的两条扫描线提供由设置在一个像素中的像素驱动电路使用的三个扫描信号中的两个,并且通过设置在相邻的另一个像素中的扫描线提供另一个剩余信号。 像素。

FIG. 2